GREEN Silicon: ICT FET Project No. 257750
Deliverable D2.1 Delivery of Thick Strain-Balanced Si/SiGe Superlattice Thermoelectric Material

21st February 2011

In the first 6 months of the project, 8 thick, strain-symmetrised Ge/SiGe superlattice wafers with 10 μm thick superlattice stacks have been delivered to the project partners by Polimi (Table I). A further 6 calibration wafers have also been grown with thinner 50 period superlattice stacks to allow XRD calibration measurements (e.g. Fig. 1) to improve the heterolayer thicknesses and Ge contents for future growths. Here a brief overview of the initial material characterisation will be presented to demonstrate the delivery of wafers as required for D2.1 but a full review of all the electrical, thermal and physical characterisation will be presented in D2.2 due at month 12.

The first wafers have been designed to be Ge quantum well structures with p-type modulation doping in $Si_{1-x}Ge_x$ barriers on relaxed $Si_{1-y}Ge_y$ virtual substrates grown on silicon-on-insulator (SOI) wafers for lateral electrical transport along the quantum well. Table II provides a detailed list of the heterolayers for one of the designs grown. n-Si/SiGe designs have also been undertaken and will be grown in the next 6 weeks once a new source of PH_3 doping gas has been delivered to Polimi (the new EC regulations for transportation have significantly delayed the delivery). The full list of delivered wafers is given in Table I.

One issue that has appeared is that some of the early thin virtual substrates wafers grown on SOI wafers had exfoliation issues (some of the material peeled off at the top Si/SiO_2 interface of the SOI wafer - see Fig. 2). A solution to this problem has now been found by cooling the wafers back to room temperature at a slow rate. We also believe that a poor batch of SOI wafers has been the cause and a new supply of SOI wafers is already being procured.

The intial XRD measurements (see for example Fig. 1) indicate that further calibration is necessary to meet exact design criteria to within a few percent. However, the heterolayer thickness and Ge contents are all sufficiently close to the design parameters to allow useful data on the thermoelectric properties and how the properties change with QW thickness, Ge content and doping. The TEM and further XRD characterisation will allow future wafers to be grown far closer to the design specification as further calibration is achieved of the growth process. No other wafers have been produced anywhere near these designs previously and we are pushing the present growth technology to the beyond many of the demonstrated limits.

A first set of thermal conductivity measurements have been undetaken using the 3ω technique on wafer 8482. This produced a vertical thermal conductivity of 1.5 ± 1.0 W/m.K which is one of the lowest values reported in the SiGe system. Process development is underway to produce Ohmic contacts on sloping sidewalls to allow electrical contacts to all 378 quantum wells over a depth of around 10 μm from the surface of the wafer. Fig. 3 shows some of the initial etch development using SF_6 / C_4F_8 ICP-RIE to produce a sloping sidewall. Electrical measurements on the first wafers should now be completed within the next month allowing the electrical conductivity and Seebeck coefficient to be extracted. The full details of electrical, thermal and ZT characterisation will be delivered at month 12.

Wafer ID	Date Delivered	Growth T	Design	N_A (cm^{-3})	Notes
8482	13/09/2010	525 °C	2	10^{18}	graded buffer
8542	10/12/2010	475 °C	2	10^{18}	exfoliation
8557	27/12/2010	475 °C	2	10^{19}	exfoliation, broken in transit (usable)
8564	10/01/2011	475 °C	2	10^{18}	8hr cooling - exfoliation
8568	13/01/2011	475 °C	2	10^{19}	8 hr cooling - exfoliation
8569	20/01/2011	475 °C	2	10^{18}	16 hr cooling - no exfoliation
8572	26/01/2011	475 °C	2	10^{19}	16 hr cooling - no exfoliation
8579	31/01/2011	475 °C	1	10^{19}	16 hr cooling - no exfoliation

Table I: The full list of 8 delivered p-Ge/SiGe superlattices with 10 µm of active thermoelectric heterolayer material.

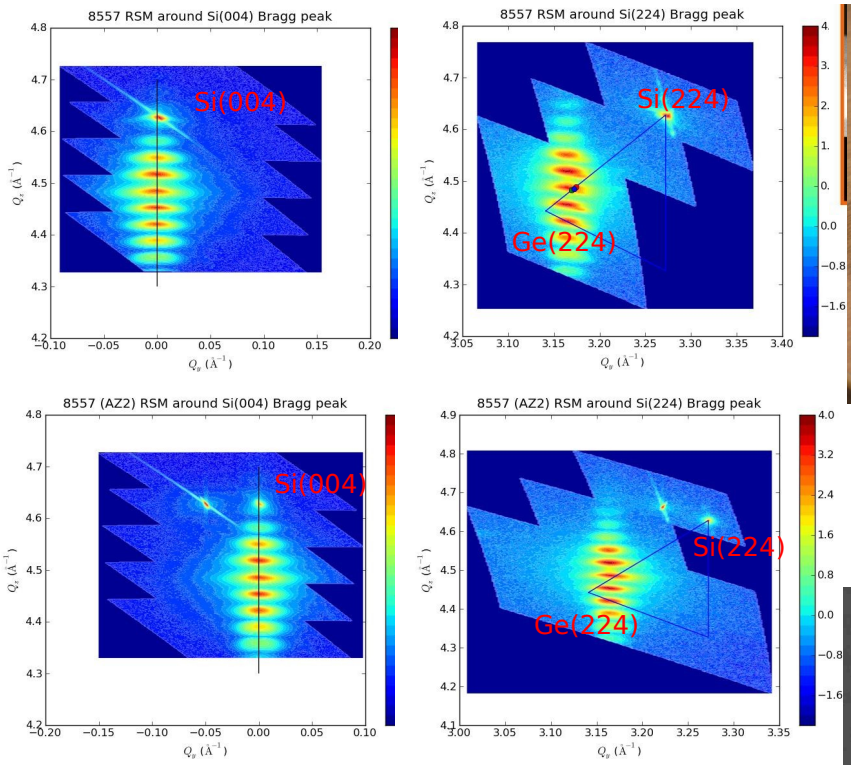

Fig. 1: *XRD RSM measurements undertaken at Linz along (004) and (224) planes on wafer 8564. The heterolayers are strain symmetrised and lattice matched to the virtual substrate of $Si_{0.23}Ge_{0.77}$ (2% higher than the design). The period is measured as 22.0 nm compared to the design parameter of 26.7 nm.*

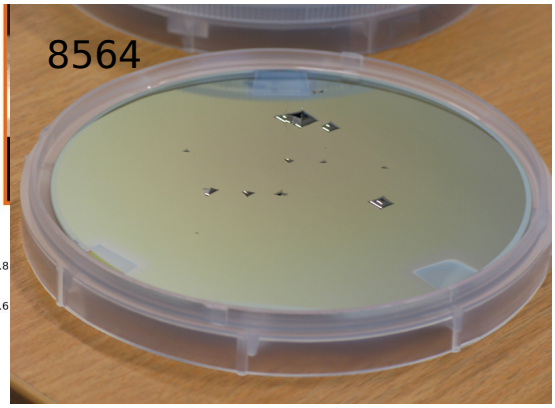

Fig. 2: *An example of the exfoliation with sections of wafer 8564 peeling off the SOI substrate at the top Si/SiO_2 interface.*

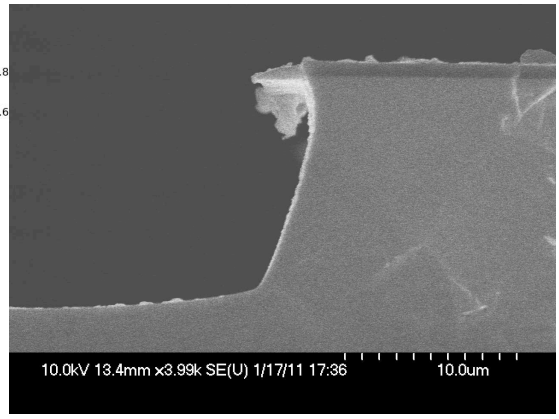

Fig. 3: *An SEM picture showing a sloping sidewall over a depth of >10 µm on wafer 8482 to allow metal to be deposited on the sidewall for an Ohmic contact to all 378 quantum wells in the material.*

Design 2	Material	Doping
surface		
4.0 nm	i-Si	
30.0 nm	i-$Si_{0.25}Ge_{0.75}$	
5.0 nm	i-$Si_{0.4}Ge_{0.6}$	
7.66 nm	p-$Si_{0.4}Ge_{0.6}$	N_A (splits of 0.1, 0.5 and 1x10^{19} cm^{-3})
5.0 nm	i-$Si_{0.4}Ge_{0.6}$	
repeat	(378 repeats for 10 μm active region)	
9.0 nm	i-Ge QW	
5.0 nm	i-$Si_{0.4}Ge_{0.6}$	
7.66 nm	p-$Si_{0.4}Ge_{0.6}$	N_A (splits of 0.1, 0.5 and 1x10^{19} cm^{-3})
5.0 nm	i-$Si_{0.4}Ge_{0.6}$	
substrate		
9.0 nm	i-Ge QW	
5.0 nm	i-$Si_{0.4}Ge_{0.6}$	
3.83 nm	p-$Si_{0.4}Ge_{0.6}$	N_A (splits of 0.1, 0.5 and 1x10^{19} cm^{-3})
8.83 nm	i-$Si_{0.4}Ge_{0.6}$	
$Si_{0.25}Ge_{0.75}$ virtual substrate (process splits with thick and thin VS)		
SOI substrate with thin top Si thickness (<200 nm) and oxide >300 nm - doping not too important but preferably quite low (i.e. 10^{15} cm^{-3} or lower).		

Table II: The complete heterolayer stack and doping splits for a lateral QW p-type thermoelectric design.