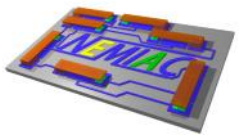


NEMIAC 1 Year Publishable Summary

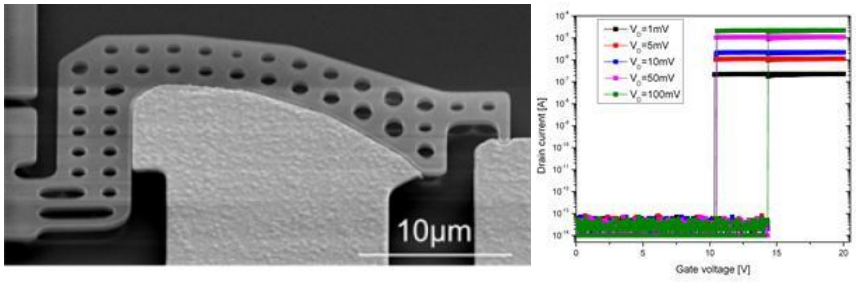
Contract N° INFSO-ICT-*288670*

NEMIAC
Nano-Electro-Mechanical Integration And Computation

To overcome the power issue of current CMOS technology, the microelectronic industry needs radically new devices, which drastically improve the energy efficiency of microelectronic systems. One promising but largely unexplored technology is nano-electromechanical (NEM) switches, which potentially achieve >10x improvement in energy efficiency. NEMIAC aims to demonstrate the viability of this technology through the development of a competitive and manufacturable device, materials research to address the inherent reliability issue, and the development of tools and methodologies to build complex logic based on the new NEM switch device.

In the first year of the NEMIAC project, suitable switches and their manufacturability have been designed and evaluated. A study to identify optimized NEM switches topologies, design and fabrication process for low power logic applications has been conducted. Taking in consideration the NEM switch circuit system aspects, we have designed and implemented a robust scalable, switch technology. The initial design is an in-plane topology (see figure). As highlighted in the table, our scaling study suggests that it is possible to achieve the performance aims in NEMIAC using a 100 nm lithography technology. The switch is based on an in-plane curved cantilever design that is compact and robust due to a good control of the actuation gap in the closed position. The contact and actuation gap are not lithographically defined but through the thickness of the same sacrificial layer. This allows for a low number of process steps and enables scaling to the nano-scale. Tilting the actuation electrodes with respect to the normal plane, reduces the closing of the actuation gap and results in a minimum electric field from gate to cantilever in the closed position allowing a better scalability of the switch.

An approach for integrating the NEM switches on top of the interconnect wiring layers and, optionally, on top of the CMOS circuitry, has been developed during the first year of the project. This process is based on wafer bonding and enables the NEM switch integration on top of interconnect wiring levels or on top of BEOL CMOS wafers. In addition, viable packaging strategies for the NEM switch circuits have been developed. This wafer-level packaging strategy will be evaluated during the remaining project time.



SEM image of a micro-size, 29.5-µm-long switch (left) and its I_D–V_G characteristics with ohmic contact at low V_D (right).

Switch Parameters	**NEMIAC Target**	**NEMIAC switch technology (predicted performance at 100 nm lithography)**
Area	3 µm x 3 µm	3 µm x 0.4 µm
Latency	50-100ns	<50 ns (f_{res}≈ 18 MHz)
Air gap	<100 nm	10 nm
Reliability	10^{10} hot events	NA
Voltage	5V	~1V

Switch performance targeted in NEMIAC and predicted performance with NEMIAC NEM Switch technology

Moreover, within this first year of the NEMIAC project, we investigated the architecture, design, and energy optimization of NEM switch based logic as well as the creation of a first logic library based on NEM switches. An important contribution to achieve these objectives was the creation of a new multi-domain model for NEM switches that accurately predicts the switch energy. Based on this model, we were able to show that logic gates based on scaled NEM switches are competitive when compared to ultra-low power CMOS logic. Designs based on dynamic logic have the potential to multiply this advantage and will be studied in depth in the coming year.

We have paved the basement of a circuit designer tool kit with the setting-up of a NEM Switch model in a circuit simulator environment to evaluate both mechanical and electrical behaviours. The model is based on 3D Finite Element Analysis (FEA) with a Verilog-A interface. We have show the validity of the model by comparing the simulation outputs with characteristics of fabricated device. In addition, a parasitic extraction flow based on existing EDA commercial tool has been developed. First simulation design flows have been exercised on simple circuit such as inverter.

As the major challenge of NEM Switch technology is the relability of nanoscale contact we intitated a focus effort on the study of best suitable ohmic contacts for the NEMS relays. Contact material screening have been performed in the first characterization phase for Carbon-Carbon and Ruthenium contacts achieving over $4x10^3$ cycles lifetime. The effect of the gate voltage rising time on the bouncing response has been also analyzed in terms of the degradation performance (contact resistance and current vs. cycling). A fast and low-parasitic long-term reliability setup has been conceived in a dry enviroment for future ageing and cycling testing as well as dedicated test structures have been proposed to analyze the propagation delay and process variability.

On the dissemination side, we have raised the awareness of the project at multiple forums with high profile activities, make potential end users aware of the research being carried out, and solicit coverage in mainstream media to highlight the use of relays with moving parts to replace solid-state devices. Members of the consortium have delivered 5 invited talks that highlight or mention NEMIAC, with 2 more to be delivered in October. Several of these talks were delivered at well-known international events. We have secured a publication in a popular electronics magazine that caters to a wide audience, EE Times Europe and also been featured in an article in the global edition of EE Times, which has secured international publicity. Members of the consortium have also published 2 conference papers and submitted further 2 journal articles. Finally, the NEMIAC concepts have already been incorporated into educational activities, in lecture material as well as student projects.