NANOSIL

Silicon-based nanostructures and nanodevices for long term nanoelectronics applications

Network of Excellence

WP 5 “Integration and spreading of excellence”

Deliverable 5.3 “Annual review of integrating and spreading of excellence activities.”

Main Author(s): Denis Flandre and Valeria Kilchytska

Due date of deliverable: M39

Actual submission date: M39

Project funded by the European Commission under grant agreement n°216171

LIST OF CONTRIBUTORS

Partner	Acronym	Laboratory Name	Name of the contact
2	Grenoble INP		Dr. Mireille Mouis
3	WARWICK		Prof. David Leadley
4	RWTH		Dr. Bernd Spangenberg
5	KTH		Prof. Mikail Ostling
6	IUNET		Prof. Enrico Sangiorgi
7	UCL		Prof. Denis Flandre
11	ISEN		Prof. Emmanuel Dubois
12	UPS		Prof. Philippe Dollfus
13	AMO		Dr. Matthias Baus
14	FZJ		Prof. Siegfried Mantl
16	TUBS		Prof. B. Meinerzhagen
17	USTUTT		Prof. Erich Kasper
18	NCSR"D"		Dr. Androula Nassiopoulou
19	Tyndall		Prof. Jean-Pierre Colinge
20	WUT		Prof. Romuald Beck
21	URV/UGR		Prof. Benjamin Inigues, Prof. Francisco Gamiz
22	Chalmers		Prof. Olof Engstrom
24	ETHZ		Prof. Andreas Schenk
26	GU		Prof. Asen Asenov
27	Livuni		Prof. Steve Hall
28	UNEW		Dr. Sarah Olsen
29	SINANO		Pascale Caulier

TABLE OF CONTENTS

Deliverable Summary

This deliverable summarizes the integration/dissemination/spreading activities within NoE Nanosil performed during 2010-11.

Integration activities is addressed through the number of joint processing (JP), joint characterization (JC) and modeling (JM) activities organized within each FP(s), WP(s) as well as cross-FP (WP) activities. Furthermore, the number of FP (WP) as well as cross FP (WP) meetings is chosen as a measure of integration activities. Common PhD students (10 in 2010-11) reinforce the integration between partners (particularly with industrial partners) as well as between process- and characterization/modelling-related WPs. Exchanges of personnel (29 exchanges of total 111 weeks during 2010-11, including 5 exchanges of total 23 weeks with Beyond Nanosil partners) further strengthened the expertise exchange and complementarity between partners. It is worth to point out 14 cross-WP exchanges, which serve not only as exchange of knowledge/expertise, but in the same time intensifies cooperation between WPs.

Additionally to the integration within Nanosil, the cooperation with other EU and national projects is encouraged. High number of EU and national projects launched by Nanosil members in 2010-11 (submitted for 2011-12) demonstrates a high activity level of the network.

Spreading of excellence within and beyond Nanosil is addressed through the support and organization of workshops/schools/trainings, which were available for a wide scientific community. Dissemination of knowledge is realized also through the regularly updated Nanosil-website, presentations given by Nanosil partners at different international scientific events, as well as publications in high-level international journals listed in the deliverable. Furthermore, 2 books and 31 book chapters were published by Nanosil partners during this last period of Nanosil allowing durable dissemination of Nanosil results.

1. Integration

1.1. Coordination by WPs (FPs) leaders

Integration within Nanosil is carried out by WPs and FPs leaders through the coordinated programming of the partners' activities. 4 Work Packages (WPs) are defined within Nanosil. WP1 and WP2 are then subdivided to 3 and 4 Flagship projects (FPs), respectively. Additionally, these WPs are completed by Visionary projects (VP) in order to reinforce/stimulate the exchange of new ideas / provoke the disputes /exchange of opinions between partners.

58 joint processing (JP), characterization (JC) and modeling (JM) activities have been performed by Nanosil partners during 2010-11, among which 18 are cross-activities between different WPs (FPs). About half of them are JP activities; more than 150 wafers were processed during 2010-11.

#	Subject/Topic	Partners involved	Measurable progress (if identifiable)	Industrial contact
		FP1.1 – Strain materials		
1.	**JP:** Creation of highly strained Si on insulator and strained Ge on insulator platforms	Warwick. FZJ, MPI Halle,		
2.	**JP:** Fabrication of Germanium on Insulators	Warwick, FZJ (MPI Halle subcontractor)	20 wafers (200mm)	
3.	**JP:** Fabrication of highly strained Si on Insulators	Warwick, FZJ (MPI Halle subcontractor)	10 wafers (200mm)	
4.	**JP & JC:** Study of high-k/ strained and relaxed Ge	Warwick, FZJ	10 wafers (4 inch)	
5.	**JM:** Mobility simulation for pMOSFETs	FZJ, TUBS	Good agreement with exper.results	
		FP1.2 – Schottky barriers		
1.	**JP:** Processing of p- and n-type transistors to fabricate CMOS dopant-segregated MOS inverters	ISEN-IEMN, UCL	Wafer thinning from UCL and successful device integration at ISEN-IEMN	
2.	**JP:** Processing of back-to-back test structures for characterization of various Er and Yb-based silicides with and without dopant segregation	ISEN-IEMN, UCL	6 wafers co-processed at ISEN-IEMN and UCL	
3.	**JC:** RF characterization of NiSi SB-MOSFET with dopant segregation	FZJ, UCL	RF measurements on n-type dopant segregated NiSi SB-MOSFETs at UCL	
4.	**JC:** XPS analysis of rare earth silicide layers and sensitivity of oxygen contamination	UCL, ISEN-IEMN	XPS surface and depth and study of capping layer efficiency	
5.	**JC & JM:** Barrier extraction and simulation of low temperature transport	UCL, ISEN-IEMN	Barrier extraction and model refinement	
		FP1.3 – Gate stacks		
1.	**JP:** TiN/LaLuO3/n-Si, MOS-cap samples	FZJ, AMO, Chalmers	10 wafers processed	
2.	**JP:** TiN/LaLuO3/n-Si, MOS-cap samples	FZJ, AMO	10 wafers processed	
3.	**JP:** TiN/AlN/LaLuO3/p-Si, MOS-cap samples	FZJ, AMO	5 wafers processed	
4.	**JP:** TiN/Al2O3/LaLuO3/n-Si, MOS-cap samples	FZJ, AMO, Chalmers	5 wafers processed	
5.	**JP:** Overview of gate stack technology	Chalmers, LIVUNI, AMO, Tyndall	Book chapter, "Nanoscale CMOS", Wiley, 2010, Chap. 2	
6.	**JC:** characterization and	Sapienza, AMO	Conf. contribution, Wodim, 2010	

	modeling of defects in GdSiO		Publication, J. of Vac. Sci. and Tech. B, 2011	
7.	**JC:** characterization of the GdSiO/Si interface.	WUT, AMO	Conference contribution, 10th ELTE Conference, 2010Publication, Microelectronics Reliability, 2011	
8.	**JC:** determination of the TiN/GdSiO/Si energy band scheme	ITE, AMO	Conference contribution, Wodim, 2010	
9.	**JC:** electrical characterization of interface states at $LaLuO_3$	Tyndall, AMO, FZJ	Conference contribution, Wodim, 2010	
10.	**JC:** Physical characterization (XPS, TEM, VASE) of $LaLuO_3$	LIVUNI, FZJ	Conference contributions: Wodim, 2010 & INFOS 2011	
11.	**JC:** characterization and modeling of hole capture at $LaLuO_3$/Si	Chalmers, IMEP/LAHC,FZJ,AMO	Conference contribution, Wodim, 2010	
12.	**JC:** MPAS characterization of $LaLuO_3$	Chalmers, ITE, AMO, Tyndall, FZJ	Conference contributions: Wodim, 2010 & 218th ECS Meeting, 2010	
13.	**JC:** 3-pulse C-V characterization and modeling of defects in $LaLuO_3$	LIVUNI, FZJ	Conference contributions: 41st IEEE SISC 2010; 219th ECS Meeting, 2011. Publication: Journal of Vacuum Science and Technology B, 2011	
14.	**JC:** influence of annealing temperature on the quality of $LaLuO_3$	WUT, FZJ	Conference contribution, 10th ELTE Conference, 2010	
15.	**JC:** Overview of electrical measurement techniques for interface state characterization	Tyndall, Chalmers, IMEP/LAHC	Book chapter, "Nanoscale CMOS", , Wiley, 2010, Chap.15	
16.	**JC:** characterization of electron and hole trapping in $LaLuO_3$	LIVUNI, FZJ	Publication, ECS Transactions, 2010	
	FP2.1 – Si Nanowires			
1.	**JP:** fabrication of Si NWs for electromechanical characterization and gas sensing	ISEN-IEMN, UCL	7 wafers processed	J.-P. Simonato (CEA)
2.	**JP:** fabrication of Si NWs for mechanical characterization – fracture strain of Si at nanometer scale	Chalmers, UCL	6 wafers processed	
3.	**JP:** fabrication of released Si NWs arrays to analyze stiction issues when released Si nanostructures	Chalmers, UCL	2 wafers processed	
4.	**JC:** characterization of Junctionless MuGFETs under mechanical strain	Tyndall, UCL	2 wafers measured (p- and n-types), approximately 50 devices measured	
5.	**JC:** fracture strain and surface roughness of released strained Si NWs	UNEW, UCL	Fracture strain extraction: more than 300 devices measured. Surface roughness as a function of traction strain: 15 devices measured	
6.	**JM:** Si NWs simulations to study their sensitivity to gas as a function of their cross-section	IUNET, UCL	More than 10 various Si NWs simulated	
	FP2.4 – Template self-organization			
1.	**JP:** Ge dot growth by MBE on wafer with oxide windows defined by Alumina Template Patterning	IMEL, USTUTT	2 wafers with large oxide windows: one for testing chemical cleaning and the second for testing in-situ thermal cleaning and Ge growth. Ge dot growth on one wafer patterned with Alumina Template Patterning. Related reports exchanged between partners.	
2.	**JP:** Pt nanosphere catalyst dispersion and NW growth	Tyndall, CEA, INPG	- Exchange of blank Si (111) substrates and SOI electrode chips. - Six batches, each batch contain 4 samples with dispersed Pt nanospheres (Pt NS): Batch 1 (29nm Pt NS), n-doped	

			substrate Batch 2 (48nm Pt NS), n-doped substrate Batch 3 (77nm Pt NS), n-doped substrate Batch 4 (29nm Pt NS), undoped substrate Batch 5 (48nm Pt NS), undoped substrate Batch 6 (77nm Pt NS), undoped substrate - Three sample vials containing diluted aqueous samples of Pt nanospheres with three different sizes: 29nm, 48nm and 77nm.	
3.	**JC:** Carrier capture / emission from Ge quantum dots	Chalmers / ITE, USTUTT	- One chip with reference Si PIN diodes. - One chip with Si PIN diodes with 4MLs of Ge wetting layer. - One chip with Si PIN diodes with 8MLs of Ge wetting layer and QDs. - p-Si Reference structure for DLTS and one chip with Schottky diodes processed from this structure. - e-CV and I-V characterizations.	
WP4 – JOINT CHARACTERIZAION				
1.	**JM:** Final deliverable D4.6: "Benchmarking semi-classical and full quantum transport modeling tools"	IUNET, IMEP, ETH,UGLA,PSUD,SYNOPSYS	Release of deliverable D4.6 submission of joint publication	
2.	**JM:** benchmarking of modeling approaches	IUNET, IMEP, ETH,UGLA,PSUD,SYNOPSYS,UG	IWCE publication	
3.	**JM:** Modelling of QB transport	IUNET, IMEP	IUNET Ph.D. student to IMEP	
4.	**JM:** Quantum Transport	IUNET, IMEP	IUNET Ph.D. student to IMEP	
5.	**JC:** Wide frequency band characterization of UT2B MOSFETs	UCL, UNEW, Leti	Analog and RF FoM extracted and compared with other technologies	Leti

Joint cross-WP activities (notice, that all WP3 activities are joint as well)

#	Subject/Topic	WPs involved	Partners involved	Measurable indicators (if identifiable)
1.	**JP:** Investigation of temperature budget of $LaLuO_3$/TiN gate stack	WP3, WP1	KTH, AMO, FZJ	4 processed wafers
2.	**JP:** $LaLuO_3$/TiN gate stack on sSOI and SOI with DS SB contacts	WP1, WP3, WP4	KTH, FZJ, AMO, IUNET	9 wafers
3.	**JP:** DS SB contacts in 60 nm sSOI MOSFETs	WP1, WP3	IEMN, KTH	6 wafers processed
4.	**JP:** sGe PMOSFETs with SB-contacts	WP1, WP3	Warwick, KTH	24 wafers grown 4 wafers with MOSFETs (60 % of process completed)
5.	**JP:** Ge dot channel MOSFETs	WP2, WP3	USTUTT, KTH	4 wafers processed
6.	**JP:** Fabrication of Nanowire-based gas sensors	FSP1.2 &FSP2.1	ISEN-IEMN, UCL	4 Wafers processed
7.	**JP:** Electron-beam lithography for memory devices	FSP1.2 &FSP2.1	ISEN-IEMN, UCL	2 Wafers processed
8.	**JP:** Processing of bottom-up Si NWs at CEA starting from silicided pad contacts built at UCL from a SOI wafer	FP2.1 & FP2.4	CEA, UCL	3 wafers processed
9.	**JP:** Patterning of Si NWs of various widths from a strained SOI wafer: biaxial vs. uniaxial strain impact on Si surface roughness	FP2.1 & FP1.1	Juelich, UCL, UNEW	1 wafer processed
10.	**JP:** Si nanowires	FP2.1 & FP2.4	INPG, CEA, Tyndall, UCL	Exchange substrates with UCL presenting predefined metallic contacts for nanowires growth

11.	**JP:** MOS on buried Ge stressors	FP2.4 &WP3	USTUTT KTH	- One wafer with Ge dot layer for n-MOSFET - One reference wafer without Ge dot layer for n-MOSFET - One wafer with Ge dot layer for p-MOSFET - One reference wafer without Ge dot layer for p-MOSFET
12.	**JC:** Characterization of bulk, SOI,, sSOI MOSFETs with LaLuO3/TiN gate stack and DS SB contacts	WP1, WP3, WP4	KTH, FZJ, IUNET, Warwick,	Feedback for the process optimization
13.	**JC:** Tunneling through high-k oxides	FP1.3 & WP4	IU.NET, Tyndall	Contribution to final report.
14.	**JM**: Simulation of benchmark devices	WP1, WP3, WP4	KTH, IUNET, FZJ, Warwick	
15.	**JM**: Simulation of strained Ge devices	WP1, WP4	Warwick, UGR, UG	Papers at ULIS 2010 and ULIS 2011
16.	**JM:** Numerical simulation of tunneling through high-k gate dielectrics targeting the 16 nm technology node	WP4 and FSP1.3	IUNET, CHALMERS	
17.	**JM:** Simulation of strained Ge transistors in SOI substrates	WP4 and FSP1.1	TUBS, FZJ	
18.	Workshop beyond CMOS	2.5 and 2.2	AMO, RWTH, KTH, USTUTT	Deliverable 2.9

41 meetings between partners (among which 10 cross WP (FP) meetings) were organized in order to stimulate the joint activities, to follow up the progress within WPs (FPs), discuss the obtained results and smooth the transfer/integration between different WPs.

Date	**Place**	**Topic**	**Participants (not names, but institutions/partners)**	**Number of persons present***
12 April, 2010	Conf. call	WP1 progress follow up	Warwick, KTH, FZ-Juelich, IUNET	6
18 May, 2010	Conf. call	WP1 progress follow up	Warwick, KTH, IUNET, FZ-Juelich, ISEN-IEMN,	8
Sept 13, 2010	Sevilla	WP1 Nanosil Meeting	Warwick, KTH, FZJ, IUNET, AMO, ISEN	10
FP1.1 – Strain materials				
14 Jan, 2010	Conf. call	FP 1.1	Warwick, FZ-Juelich, MPI Halle	5
17 Mar 2010	ULIS, Glasgow	WP1 Meeting + FP 1.1	Warwick, KTH, FZ-Juelich, MPI Halle, IUNET, Granada, URV	8
every 3months	Teleconf.	Progress follow-up	Warwick, KTH, FZJ, IUNET	5-8
FP1.2 – Schottky barriers				
10 Sep	Seville	progress follow up	Warwick, KTH, FZ-Juelich, IUNET, ISEN-IEMN, Tyndall	6
FP1.3 – Gate stacks				
2010-01-27	Grenoble	Up-date and planning	LIVUNI, Tyndall, AMO, FZJ, IMEP/LAHC, Sapienza, WUT, ITE, URV, Chalmers	12
2010-03-05	Telephone meeting	Up-date (mainly after new FGA results) and planning	LIVUNI, Tyndall, AMO, FZJ, IMEP/LAHC, Sapienza, WUT, ITE, URV,Chalmers	12
2010-07-01	Bratislava	Up-date and planning of final activities	LIVUNI, Tyndall, AMO, FZJ, IMEP/LAHC, Sapienza, ITE ,Chalmers	13
2010-10-21	Telephone meeting	Up-date and planning of final activities	LIVUNI, Tyndall, AMO, FZJ, IMEP/LAHC, Sapienza, WUT, ITE ,Chalmers	13
2010-11-25	Telephone meeting	Up-date and planning of final activities	LIVUNI, Tyndall, AMO, FZJ, IMEP/LAHC, Sapienza, WUT, ITE ,IU.NET, Chalmers	15
2011-01-12	Grenoble	Up-date of results for Final Report	LIVUNI, Tyndall, AMO, FZJ, IMEP/LAHC, Sapienza, WUT, ITE ,IU.NET, URV	14
VP1.4 – More Moore Forum				
26/01/ 2010	Grenoble	Panel session: "SOI technologies: What kind or research for what	All Nanosil partners	~110 (~70 from

		kind of products?		Nanosil)
17/03 2010	Glasgow	Workshop and panel: "High mobility nMOS substrates: strained-Si, Ge or III-V?"	All Nanosil partners	~90 (~70 from Nanosil)
09/09 2010	Bologna,	Workshop and panel "Simulation and Characterization of Statistical CMOS Variability and Reliability"	All Nanosil partners	~55
17/09/ 2010	Seville	Workshop "At the convergence between More Moore and More Than Moore / Beyond CMOS activities".	All Nanosil partners	~70
FP2.1 – Si Nanowires				
25/03/2010	Louvain-la-Neuve	One-day Workshop about Silicon Nanowires	Tyndall, ISEN-IEMN, Juelich, EPFL, IUNET, INPG, invited speaker from Intel (Ireland)	45
15/06/2010	Louvain-la-Neuve	Simulation of Si NWs for gas sensing applications	IUNET, UCL	4
11/10/2010	Louvain-la-Neuve	Characterization of SHE in FinFETs	UNEW, UCL	5
FP2.2 – Carbon electronics				
7/13-7/14 2010	Aachen	Joint workshop on Carbon electronics	AMO, RWTH Aachen, IUNET, Chalmers,	**12** (Nanonsil) + *43* = 55
FP2.4 – Template self-organization				
14/03/ 2011	Cork	3rd periodic report	USTUTT, Chalmers, Julich	3
11/02/ 2011	LLN	Nanowires FET	FMNT/INPG, UCL	3
15/10/ 2010	Teleconf. Cork	Nanowires on colloids	Tundall, INPG, CEA, USTUTT	5
23/01/ 2010	Aachen	Manufactoring potential	RWTH Aachen, USTUTT, Chalmers	3
17/01/ 2010	Phoenix	High frequency response	UCL, USTUTT	2
VP2.5 – Beyond CMOS Vision				
26/02/ 2011	Aachen	Joint workshop on "Beyond CMOS Routes" More details reported in Deliverable D 2.7	RWTH Aachen, AMO, Chalmers, USTUTT	12 (Nanosil) + 5 = 17
WP4 – JOINT CHARACTERIZATION				
27/01 2010	Grenoble	State of the art of the Deliverables and actions to answer Reviewers recommendations	IUNET, SNPS, IMEP, UGL, UCL	15

Cross-meetings

Date	Place	Topic	WPs	Participants	Number of persons present
27-28/01 2010	Grenoble	Annual Nanosil meeting + FP 1.1, 1.2, 1.3 Meetings	All	All Nanosil participants	
17/09/2010	Sevilla	Nanosil Workshop	All	Most partners	approx. 60
6 Oct 2010	Conf Call	Progress follow-up	WP1 & WP3	Warwick, KTH, FZ-Juelich, IUNET, ISEN-IEMN	8
11 Nov 2010	Conf Call	Progress follow-up	WP1 & WP3	Warwick, KTH, FZ-Juelich, IUNET, ISEN-IEMN	8
15 Dec 2010	Conf Call	Progress follow-up	WP1 & WP3	Warwick, KTH, FZ-Juelich, IUNET, ISEN-IEMN	8
01 Feb 2011	Conf Call	Progress follow-up	WP1 & WP3	Warwick, KTH, FZ-Juelich, IUNET, ISEN-IEMN	8
01 Mar 2011	Conf Call	Progress follow-up	WP1 & WP3	Warwick, KTH, FZ-Juelich, IUNET, ISEN-IEMN	8
30 Mar 2011	Conf Call	Progress follow-up	WP1 & WP3	Warwick, KTH, FZ-Juelich, IUNET, ISEN-IEMN	8
24.05. 2010	Stockholm	Processing of QD layers	WP3 & WP2	KTH, USTUTT, Chalmers	4
Oct 2010	Stockholm	Implementation of SB-contacts in MC simulator.	WP1, WP3, WP4	IUNET, KTH	4

1.2. Common PhD students

NoE integration is reinforced by the common/joint PhD students between different partners. In 2010-11 there were **10 common PhD students**, 2 of them defended PhD Thesis during 2010. It is Interesting to notice, that most of these PhD students are working within WP4. Additionally, it is worth to point out that six of ten PhD works devoted to two WPs (1, 2 and 4) in the same time, thus reinforcing cooperation between processing- and chatacterization/simulation- related WPs. Furthermore, majority of these PhD students being joint between industrial and academic partners enhances industry-academia interactions.

Nanosil partner 1	Nanosil partner 2	Topic	WP(s)
STM	FMNT/INPG, CEA/LETI	Influence of gate stack materials on transistor performance at 32/22nm technological nodes	1, 4
FMNT/INPG	CEA/LETI	Electrical conduction in high-k dielectric materials (defended 26/11/2010)	1, 4
CEA/LETI	FMNT/INPG	Compact modeling of multi-gate MOSFETs for integrated circuits design (defended 24/09/2010)	4
CEA/LETI	FMNT/INPG	Characterization of 3D-NW MOSFETs	2, 4
INPG/FMNT	CEA	Characterization of low thermal budget high-k/metal gate MOS transistors	1, 4
Grenoble INP	ST	Electrical properties of ultra-thin film SOI MOSFETs	4
INPG/FMNT	CEA	Intégration of Si and SiGe nanowires	2
UCL	IEMN-ISEN	Fabrication guidelines for electromechanical and gas sensors based on Si nanowires	2
UNEW	UCL	Wideband characterization of advanced MOS output characteristics	2, 4
UNEW	UCL	Raman spectroscopy of strained Si nanodevices	1, 4

1.3. "Web-site", "Who is Who guide", "open questions", "Breaking News".

Nanosil web-site helps integration of Nanosil partners and ease exchange of information between them. A lot of useful information/documents/links can be found on the site. There exists a restricted area limited to consortium members (institutions) only where one can find for example ppt/pdf-files with presentations given by Nanosil partners or those given during different events supported by Nanosil; annual reports, selected exchanges, etc.

Updated version (2010) of Who is Who guide is available through the Nanosil web-site Public Area. Interactive information in the "partners list" and search by "competence" are introduced.

Request for Beyond Nanosil institutions to be included in "Who is Who" of associated partners is available on the web-site (public area). **"Who is Who" of associated partners** gathers "who is who" of institutions participated in exchanges with Nanosil partners as well as institutions involved in national projects or other collaborative actions (those interested). Updated 2010 version is available on the web-site (http://www.nanosil-noe.eu/data/document/who-who-beyond-nanosil.pdf).

We encouraged partners to provide us information about "**technical problems** they encounter **and open questions** they imagine". We request partners to provide us such information twice a year. Similarly to the previous period, no any problem/question inputs from partners were received, assuming that these issues were discussed/solved on the level of FP/WP team and were not worth to be discussed at ESC meetings.

"Breaking news" initiated last year and placed on the web-site in public area to widely advertise top-level achievements/developments within Nanosil was regularly updated.

1.4. Interaction with industrial partners

Interaction with industrial partners aims at roadmapping, assessing the results and assure theirs transferability to industry. With this regards, each FPs of Nanosil has industrial contact person or "**industrial monitor**". Industrial partners are invited to participate in **Executive & Scientific Committee Meetings** to develop a general strategy of network progressing/developing.

Additionally, common industry/academia **PhD students** (seven in 2010-11) and common industry (within and beyond Nanosil, as e.g. Intel, Infineon, SMEs, …) & academia **projects** (19 running and 14 newly submitted/accepted) reinforce this exchange of knowledge.

Furthermore, academia/industry **meetings** organized by some partners (see section 5.2 for details) and **joint publications/presentations** reinforce collaboration and transfer of knowledge between academic and industrial partners.

Web-links to the **scholarships/trainings/PhD positions/etc. available at the industry** are placed on the Nanosil web-site (http://www.nanosil-noe.eu/nanosil/wp5/scholarships-and-trainin.html).

2. Collaboration with other European and national projects

During 2010-11 **thirteen European projects** (from which 10 are FP7 projects), **three international projects** (involving European countries, USA, Japan and Korea) and **twenty two national projects** (7 in UK, 5 in Poland 2 in Irland, France, Germany and Sweden, 1 in Italy and Switzerland) in the fields relevant to Nanosil are running with participation of Nanosil partners, which naturally assure a good links with this projects. As example we can talk about collaboration and exchange of knowledge between Nanosil and EuroSOI+, COMON, GRAND, STEEPER, SQWIRE…projects.

Lists of European and National projects of relevance are available on the Nanosil web-site (updated yearly), web-links to the corresponded project sites are introduced whenever possible.

Nanosil partner	Other Partners	Title of the project	National/ European/ International	Funding source
URV, UGR, UCL, IMEC, Tyndall, Chalmers LIVUNI, WUT, INPG, LETI, EPFL	Grenoble INP, URG, SOITEC, VTT, Cissoid, Phillips, ISP, IUE, WUT, Xfab, Chalmers, QUB, CSIC-CNM, IMMS, Polito, UAB, USAL, DITOCOM, ISEP, UT	EUROSOI+	European	FP7, Cooperation Programme, ICT, Coordination Action
URV, UCL, EPFL	UniK (NO), TUC (GR), UdS (FR), TU-Ilmenau (DE), ITE (PL), Infineon (DE), AMS (DE), RFMD Ltd (UK), AdMOS GmbH (DE), DOLPHIN Integration SA (FR), Melexis Inc (UA), AIM-Software (NO)	COMON (Compact Modelling Network)	European	FP7, People Programme, Industry-Academia Partnership & Pathway
KTH, URV, ETHZ	28 other partners	OSIRIS	European	EU FP6

IUNET, AMO, LETI, Tyndall	UCAM DPHYS (UK)	Graphene-based Nanoelectronic Devices (GRAND)	European	EU FP7
FZJ		DECISIF (Catrene)	European	National
FZJ, EPFL, IUNET, CEA/LETI	Infineon, IBM, Global foundries, Technical Univ. Dortmund, Sciprom Sarl	Steep Subthreshold Slope Switches for Energy Efficient Electronics (STEEPER)	European	EU FP7
Tyndall, IMEC, INPG, CEA/LETI, URV	Intel_Irland, Magwel nv, Soitec	Silicon Quantum wire transistors (SQWIRE)	European	EU FP7
UoG IMEC	INTEL	TRAMS	European	EU FP7
UoG ST, IUNET, LETI	Infenion, NXP	MODERN	European	ENIAC
GU IMEC, LETI, ST, Demokritos	IBM	DUALLOGIC: Dual-channel CMOS for sub-22 nm high performance logic	European	FP7
EPFL, IUNET CEA-LETI FZJ	Global Foundries, IBM Zurich, Infineon	Steep subthreshold slope switches for energy efficient nanoelectronics circuits (STEEPER)	European	FP7
ST, CNRS, Synopsys, UNEW, ETHZ		ATEMOX : Advanced TEchnology MOdelling for eXtra-functionality devices	European	FP7
UCL, KTH, Grenoble-INP, CEA-LETI, Tyndall, IUNET, IMEC, AMO	VTT, Catalan inst. of nanotechnology,	Nanofunction, NoE	European	FP7
Tyndall	Queens University Belfast, Dublin City University, University of Texas at Dallas	Future Oxides and Channel Materials for Ultimate Scaling (FOCUS)	International	Science Foundation Ireland (www.sfi.ie), Invest Northern Ireland and National Science Foundation
INPG/FMNT	U. Stanford, Korea University	CORE - transport in core/shell nanowires	International	Nanoscience Foundation
USTUTT	-RIEC, Tohoku Univ. Sendai, Japan. - IHP, Berlin Institute of Technology, Germany. - IMEC Leuven, Belgium - CINaM-CNRS, France. - New Materials group (FA-3) University of Vigo, Spain. -Massachusetts Inst. of Technology (MIT), USA. - Princeton Univ., USA	The Excellence Initiative for New Group IV Semiconductor Material & Processing, (EI4GroupIV)	International	Institute resources
Warwick	IMEC, Glasgow, Sheffield	Renaissance Germanium	National	EPCRC
RWTH AACHEN	AMO	Experimentelle und theoretische Untersuchung der Wirkungsweise von Silizium-Nanodraht-MOSFETs (experimental and theoretical investigations of Si NW MOSFETs)	National	DFG
KTH		SB nanowire MOSFETs	National	Swedish Research Council

KTH		1/f noise in advanced MOSFETs	National	Swedish Research Council
IUNET-Udine, Bologna, Pisa		Modellistica e simulazione di transistori in grafene per applicazioni logiche ad alte prestazioni e bassa dissipazione di potenza (GRANFET)	National	Italian Ministry of University and Research
UPS, CEA/LETI	LPMCN, IMS	ACCENT: Multiscale simulation of carbon nanotube devices	National	ANR
UPS, IEMN, CEA/LETI	OMMIC, CIMAP	MOS35: Low-bandgap MOSFETs for high frequency/low power applications	National	ANR
Tyndall		Grant 05/IN/I888: Advanced Scalable Silicon-on-Insulator Devices for Beyond-End-of-Roadmap Semiconductors.	National	Science Foundation Ireland
Tyndall	Dublin City University, Trinity College Dublin and INTEL	Investigating Emerging Non Silicon Transistors (INVENT)	National	Science Foundation Ireland
ETHZ EPFL	IBM Zurich	ENABLER	National	Swiss NanoTera
LIVUNI	University of Ulster	A biologically plausible spiking neuron in hardware	National	EPSRC, £436k
LIVUNI		e-FuturesXD: university research in electronics	National	EPSRC with UK semiconductor and circuit designer, £650k
LIVUNI		e-Futures: university research in electronics	National	EPSRC with UK semiconductor and circuit designer, £150k
UNEW		ALD of piezoelectrics and ferroelectrics	National	CPI (Commercial)
UNEW		NanoLAB cross disciplinary research	National	EPSRC
UNEW		Ferroelectrics for nanoelectronics	National	EPSRC
WUT		Electrical characterization of dielectric-semiconductor interface in advanced MOS structures	National	Polish Ministry of Science and Higher Education
WUT		Modelling of silicon structures with low-dimensional electron gas	National	Polish Ministry of Science and Higher Education
WUT		Technology and characterization of MIS devices with double gate dielectric stacks for non-volatile semiconductor memories (NVSM) applications	National	Polish Ministry of Science and Higher Education
WUT		Modeling and investigation of the double barrier metal-oxide-semiconductor tunnel structures	National	Polish Ministry of Science and Higher Education
WUT		Technology and characterization of MIS structures with double gate dielectric stacks for non-volatile semiconductor memory (NVSM) applications	National	Polish Ministry of Science and Higher Education
FZJ		KZWEI	National	National

It is worth to mention that **25 new projects** (the same number as in 2009) have been submitted/accepted during 2010-11 by members of Nanosil, among which 6 EU projects within FP7, 1 CATRENE and 18 national projects (5 in France, 3 in UK, 2 in Spain, 2 in Ireland, 2 in Poland, 2 in Belgium, 1 in Germany, 1 in Switzerland). It is worth to point high number (14) of the projects submitted in the collaboration between two (or more) Nanosil partners, which evidence strong integration/collaboration between Nanosil partners. Surely, good collaboration between Nanosil and these new projects is foreseen.

Nanosil partner	Other Partners	Title of the project	National/ European/ International	Funding source	Status (submitted/ accepted/ started)
STM, CEA/LETI, INPG/FMNT, GU, UCL, FZJ, EPFL, UGR, IUNET	Infineon, Global Foundaries, Soitec, SMEs	REsearch on optimal ArCHitecture and INteGration of 22/20nm node core digital CMOS technology-Electrical proof of concept REACHING 22	EU/National	CATRENE	Accepted
FZJ, EPFL, IUNET, CEA/LETI	Infineon, IBM, Global foundries, Technical Univ. Dortmund, Sciprom Sarl	Steep Subthreshold Slope Switches for Energy Efficient Electronics (STEEPER)	European	EU	Started on july 2010
EPFL, ETH, CEA, CNRS, UCL, Imec, KTH, ST, Sinano, Tyndall-UCC	CTTC, HIQSCREEN, IBM, Intel, Infineon, KU Leuven, NXP, VTT, ITE, Thales, ULUND, UCAM, SIE, SARD	" Guardian Angels for a Smarter Planet " (GA) FET Flagship	EU	FP7	Accepted
UCL, KTH, Grenoble-INP, CEA-LETI, Tyndall, IUNET, IMEC, AMO	VTT, Catalan inst. of nanotechnology,	Nanofunction, NoE	EU	FP7	started
Tyndall, IMEC, INPG, CEA/LETI, URV	Intel_Irland, Magwel nv, Soitec	Silicon Quantum wire transistors (SQWIRE)	EU	EU FP7	started
ETHZ, CNRS STM, SNPS, UNEW	Fraunhofer, Semilab, Probion EXCICO	ATEMOX 258547	European	FP7-ICT STREP	started
LIVUNI, RWTH, AMO, Tyndall-UCC	National University of Ireland, Lot Oriel, X-FAB, SAFC Hitech Ltd	Selecting high-k for analog and RF process technologies	European	ECC, STREP	Not funded, £189k
INPG/FMNT, IEMN, CEA/ LETI, STM	IM2NP, CEA/INAC, I. Néel	QUASANOVA	National	ANR	Started
UCL	-	Towards 10 nm MOSFET	national	FNRS	started
UCL		Graphene nanoelectromechanics - A step towards a new field: StressTronics -	national	FNRS	Started 2011
ISEN-IEMN CEA-LITEN	Id3	CAMIGAZ Capteurs Autonomes MIniatures communicants pour la détection de GAZ de combats	National (ANR-Agence Nationale de la Recherche)	ANR	Accepted
RWTH, AMO		Experimentelle und theoretische Untersuchung der Wirkungsweise von Silizium-Nanodraht-MOSFETs (experimental and theoretical investigations of silicon nanowire MOSFETs)	National	DFG	Request for extension submitted in 2010

UPS, CEA/INAC & LETI,	Néel Inst., LPS, Nanotimes	NANOSIM_GRAPHENE: Simulation of Graphene-based Nanomaterials and Nanodevices : Multiscale Approaches	National	ANR	started
UPS, IEMN,	LPA, LPN	MIGRAQUEL: MIcrowave GRAphene QUantum ELectronics	National	ANR	started
UPS; CEA/LITEN,	LFPINAC, CIMAP, IPCM	SQUID PV: Silicon QUantum Dots and Investigation of Transport and Doping Phenomena for PhotoVoltaic Applications	National	ANR	submitted
UGR		Development of 1T-DRAMs cells.	National	Regional Govern-ment	Accepted
UGR		A-RAM family: the first step towards a universal memory (URAM)	National	National Govern-ment	Submitted
Tyndall		Semiconductor nanowire Transistors	National	Science Foundation Ireland	started
Tyndall	Dublin City University, Trinity College Dublin and INTEL	Investigating Emerging Non Silicon Transistors (INVENT)	National	Science Foundation Ireland	started
ETHZ EPFL	IBM Zurich	ENABLER	National	Swiss NanoTera	started
LIVUNI	University of Cambridge, Liverpool John Moores University	High permittivity dielectrics on Ge for end of Roadmap application	National	EPSRC	Started, £522k
LIVUNI	Industry: TWI, Plessey, Zarlink, Unisem, and Leeds University; and 2 SMEs: Qudos and JLS	Precision Passive Component Design & Manufacture in Micro-Module Electronics (PPM2)	National	UK Technolog y Strategy Board	Started, £320k
LIVUNI		High-efficiency rectenna arrays for solar energy collection	National	EPSRC	Submitted, £875k
WUT		Investigations on photonic sources for coherent emission from silicon integrated systems	National	Polish Ministry of Science and Higher Education	started
WUT		Application of ultrashallow fluorine implantation for improvement of radiation hardness of MOS structures for 1MeV electrons	National	Polish Ministry of Science and Higher Education	started

3. Exchanges

Four **calls for exchanges** have been issued electronically. Requests from partners have been then discussed during E&SC meetings. Last call was issued in September. However, in view of project extension, partners were allowed to perform their planned/selected exchanges untill end of February 2011.

30 exchanges (including 6 exchanges with beyond Nanosil) for the total **duration of 98 weeks** (including 24 weeks with beyond Nanosil) have been selected to be supported (call 8^{th} to 11^{th}). These numbers are about the same as in 2009 (and impressively higher comparing to 2008), indicating that good networking activity installed in 2009 continued in 2010.

29 exchanges (including 5 with beyond Nanosil and 2 postponed from 2009) for the total duration of **111** weeks (including 23 with beyond Nanosil) have been done during 2010-11. It is worth to point out 15 cross-WP exchanges, which serve not only as exchange of knowledge/expertise, but in the same time intensifies cooperation between WPs (particularly processing vs. simulations/modeling).

From Nanosil partner	To Nanosil partner	Topic	Duration (weeks)	WP	Comments
UCL	Chalmers	Si Nanowires fabrication	9	2	5th call 2009-15
FZJ	UCL	RF measurements of dopant segregated SB-MOSFETs	1	1, 4	7th call 2009-23
UCL	UNEW	1°Piezoresistance coefficient measurements; 2°Interface characterization of Si NW	12	2, 4	8th call 2010-1
IUNET	UCL	Development of modeling and simulation methodologies for silicon nanowire FinFETs	13	2, 4	8th call, 2010-2
IUNET	LIVUNI	Aligning the two pulsed C-V set-ups; starting to develop a model of trapping/ detrapping in high-k which takes into account obtained results	2	1, 4	8th call 2010-3
UCL	UNEW	Characterization of the two-dimensional crystal-lne network of graphene by AFM and Raman Spectroscopy.	2	2, 4	8th call 2010-4
IMEP/LAHC	Chalmers	Tunneling in metal/HfO2/Si stacks	2	1.3	8th call 2010-5
Warwick	Julich	High-k gate stacks on Ge channel MOSFETs	1	1	8th call 2010-7
Warwick	Glasgow	Scattering from high-k dielectric interface	1	1, 4	8 th call 2010-8
Warwick	Julich	PtSi Schottky barrier contacts	1	1	8th call 2010-9
UCL	FZJ	New steep slope device (RT-FETs with DS SB devices)	1	2, 4	8th call 2010-11
UCL welcome	Synopsis	Si Nanowires	3 days	2, 4	8th call 2010-12
IUNET welcome	EPFL	Monte Carlo simulation of tunnel-FETs	12	2, 4	9th call 2010-14
INPG/FMNT	Tyndall	Electrical characterization of GIDL effects	4	1, 4	9th call 2010-15
UNEW	INPG	1/f noise measurements in Si NWs with various levels of strain in order to understand the effects of interface quality on piezoresistance in Si	2	2, 4	9th 2010-16
IMEC	INPG	Tunnel FETs	1	2, 4	10th call 2010-19
IUNET	INPG	Quantum transport in the NEGF formalism	4	4	10th call 2010-20
IUNET	INPG	Validation of characterization techniques for back-scattering parameters by means of Monte Carlo simulations	4	4	10th call 2010-21
UNEW	UDINE	Strained Si mobility enhancement	1	1, 4	10th call 2010-22
UCL	IEMN	Si Nanowires fabrication and characterization	9	2	7th call 2009-24
IMEL	IMEP	Electrical characterization of silicon nanowires systems	1	2, 4	11th call 2010-25
IUNET	INPG	Discussion about deliverable D46 and lectures to PhD students	1	4	11th call 2010-26
UCL	CEA	Functionalization of Si Nanowires	1	2	11th call 2010-27
UNEW	UCL	Wide f-band characterization of UTB and ultra thin buried oxide devices	2	4	11th call 2010-28

BEYOND NANOSIL					
UCL welcome	ISP-Kiev	Characterization of advanced SOI-based MOSFETs	8	4	9th call 2010-17
IUNET welcome	IPT-RUS	Development of simulation programs for the analysis of advanced optical sensors and solar cells based on Si nanowires	4	4	9th call 2010-18
Tyndall welcome	ISP-Kiev	Noise measurement on junctionless transistors	6	2, 4	10th call 2010-23
IUNET	IPT-RUS	Upgrade of simulator developed in previous exchange (2010-18) in order to apply it to 3 dimensional devices	4	4	10th call 2010-24
RWTH welcome	Univ. Washington	Participation of Jeremy Witzens (Univ. of Washington) in "Beyond CMOS" workshop,	1	2	11th call 2010-30

4. Spreading of excellence

4.1. Support of International Schools/Workshops

Four Calls were issued for the conference/workshops/seminars support to gather the requests for such actions. Thanks to careful use of funds within WP5 (particularly because partners were asked to provide budget estimation together with their request for exchange) as well as economy from certain exchanges, this year we were able to support higher number of workshops/schools/etc.: 14 in 2010-11 comparing to 5 during previous years. Following workshops were selected by E&S Committee:

- ULIS 2010, UK (10kEuro)
- Silicon Nanowires Workshop, Belgium (750Euro),
- International SiGe Technology and device meeting, Sweden (2.5kEuro),
- International Workshop on Nanoscaled Sem-OI materials, sensors and devices, Belgium-Ukraine (11kEuro).
- SINANO Summer School, Italy (14kEuro)
- Simulation and characterization of statistical CMOS variability and reliability, Italy (2.5kEuro)
- Graduate student meeting on electronic engineering JOINTLY with training course on Compact modelling, Spain (3.5kEuro)
- MIGAS 2010, France (10kEuro)
- Workshop on Carbon Electronics "EuroCarbon Symposium", Germany (2.5kEuro)
- SINANO-NANOSIL workshop "on the convergence between More Moore, More than Moore and beyond CMOS", Spain (5kEuro)
- Workshop "Nanoelectronics: a tool to face the future", Spain (2.25kEuro)
- Final Nanosil Workshop devoted to ENI2 (European nanoelectronic infrastructure for innovation) "Nanoscale FET", Ireland (4kEuro)
- International conference "Micro&Nano", Greece (2kEuro).

More details about these events can be found in the following section and in summary-table below.

4.2. Organization of seminars/courses/workshops/tutorials

Joint **SINANO-NANOSIL Workshop** "On the convergence between More Moore, More than Moore and beyond CMOS" aiming to establish a discussion forum on the links and future of these 3 domains was organized on Sept. 13th (jointly with VP1.4), where all Nanosil partners were represented. Lectures were given by Nanosil partners from one side and by industry (Infineon, Global Foundries, IBM) from another side. Traditionally, workshop was open to a general public. More details about this event can be found in D1.10.

Special attention is worth paying to higher number of events targeting particularly **young researchers** as graduate and post-graduate students pursuing their PhD. We can refer to Sinano Sumer school organized in Italy, MIGAS organized in France, 2 workshops in Spain, etc.

It would be worth to mention that one of above-listed workshops financially supported by Nanosil was organized **jointly with beyond-Nanosil** partner and held in Kiev, Ukraine, thus allowing wider dissemination of Nanosil knowledge and intensification of **collaboration with East Europe and former Soviet Union countries**. Moreover, selected invited speakers were proposed to prepare chapters for the book which was published by Springer in 2011 (see section 5.2 for more details).

Furthermore, as was already mentioned above, **two Visionary projects** (VP 1.4 “More Moor Forum” and VP 2.5 “Beyond CMOS vision”) are launched within Nanosil WP1 and WP2 in order to stimulate discussions on the new hot-topics and identify areas where the partners of the Network can make a contribution. The **discussions/workshops organized by these VPs** are open to participants within Nanosil free of charge as well as to wide audience beyond Nanosil.

Four workshops and panel sessions were organized **within VP1.4** during 2010-11 (one of them jointly with Sinano-Nanosil workshop cited above). All of them are continuation and further extension of the discussions initiated in 2008-2009 and address the four topics related to particular aspects of Ultimate CMOS. First meeting or a panel session: “SOI technologies: What kind or research for what kind of products ?” organized during EuroSOI Conference (January 2010, in Grenoble, France) addressed a topic related to the “Electrostatic effects in Ultimate CMOS”. 6 experts (both from academia and industry) were asked to prepare in advance a couple of slides to discuss the future of research of SOI technologies versus application. Second meeting organized as a satellite event of the ULIS 2010 (March 2010, Glasgow, UK) was related to the “Alternative channel and substrate materials”. Through four presentations followed by panel discussion it has addressed the issue of “High-mobility n-type substrates: strained silicon, germanium or III-V?”. Third meeting organized as a satellite event of the SISPAD 2010 (September 2010, Bologna, Italy) was related to the topic “Fluctuations in ultimate CMOS”. This one-day workshop provided an in depth review of the modelling, simulation and characterisation of variability and reliability issues for future CMOS. Presentations were given by industrial and academic experts. Fourth meeting was organized jointly with SINANO-NANOSIL meeting and already referred above. Brief details on VP1.4 workshops are given in the table below. More detailed description of the meetings, speakers and conclusions can be found in D1.10.

One workshop was organized **within VP2.5**. Workshop on “Beyond CMOS Routes” is also the continuation of the discussion started at 2008-2009. The workshop held in Aachen on Feb 23 2011 was devoted to a critical assessment of the “Beyond CMOS” area, specifically to the analysis of the activities within WP 2. The workshop addressed the most interesting alternatives to the current mainstream philosophy documented in the excellent presentations of competent speakers. Starting from an actual review of the potentials that current future CMOS technology will offer and first steps into non-conventional Si-CMOS transistors as tunnel FETs, it covered then role of specific quantum structures, prospects of Si photonics, graphene and spintronics. Please, see D2.7 for more details.

Additionally to the abovementioned workshops financially supported by Nanosil, it is worth to mention **following events (14 in a total) organized by Nanosil partners** in 2010-11 without direct funding

from Nanosil and open to wide public. Among them it is worth to cite a high number of large **well-known international events** as ESSDERC, EuroSOI, ULIS organized by Nanosil partners in 2010-11. Moreover, it would be important to emphasize couple meetings between **academic and industrial teams** allowing rather open discussion with direct transfer of knowledge accumulated within academia to industry (both within and beyond Nanosil) and industrial feedback on roadmapping/ perspectives/ their short- and long-term interests.

Brief details about all workshops/seminars/school/etc. organized by Nanosil partners (32 in a total) are listed in the table below.

Nanosil partner	Meeting/ seminar/ workshop/ etc.	Topic	Date & Place	Participants (institutions)	Number of persons present *	Support from Nanosil (yes/no)
GU	Workshop	ULIS 2010	March 2010, Glasgow	All Nanosil partners+ beyond	80	Yes
UCL	Workshop	Si Nanowires	March 2010	UCL, Intel-Irland, IMEC, INP-renoble, IUNET, UNEW, Tyndall, FZJ, EPFL	30/*1*	Yes
KTH	ISTDM	International SiGe Technology Device Meeting	May 2010		>100	Yes
UCL	Workshop	Semiconductor on Insulator	Oct. 2010	UCL, Leti, Imec, INP-Grenoble, UG, WUT, ISP-Kiev, ISP-Novosibirsk, Soitec, URV/UGR, Tyndall	+-20/*40*	Yes
IUNET	School	4th Sinano Summer School (mostly focused on topics related to the modeling, characterization and variability-related issues for silicon-based devices, tacking into consideration several applications (logic, memory and analog-RF). In addition, we had one special sessions related to energy-harvesting devices and solar cells.	Bertinoro, Italy on July 20th – 23rd 2010	Mostly from NANOSIL institutions, + NXP, INFINEON, APPLIED MATERIALS, Fraunhofer, US Universities, 4 from China 16 lecturers, mostly Europe (6 from NANOSIL) and 1 from US	40 total (about half from Nanosil)	Yes
GU	Workshop	Simulations and characterization of statistical CMOS variability and reliability	Sept. 2010, Bologna			Yes
URV	First Training Course on Compact Modeling (TCCM 2010)	The first edition of the Training Courses on Compact Modeling (TCCM) will consist of a set of lectures addressing relevant topics in the compact modeling of advanced electron devices. Most of the courses will target compact modeling issues applicable to many electron devices. In particular, emphasis will be given on MOSFETs (bulk, SOI, Multi-Gate and High Voltage MOS structures) and HEMTs.	June 30 – July 1, 2010	TUC, ITE, TU-Ilmenau, Silvaco, RFMD, Infineon (Intel), McMaster University, UGR, CINVESTAV, UniK, TU WIEN, Politecnico di Torino, CSEM SA, Univ. Of Salamanca, AdMOS GmbH, CNM, IMEP, UCL, Univ. Of Montpellier, AMS, Tyndall Institute, ON Semiconductor, UIB, Chalmers, EPFL, USTUTT, IMO (Poland), GMC Suisse, Univ. Of Giessen	20 *60*	Yes

URV	8th Graduate Student Meeting on Electronic Engineering	-Nanoelectronics and Nanophotonics -Micro and Nanosystems - Power Electronics & Renewable Energy Systems - Signal Processing and Data Mining - Automatic Control	June 28-29, 2010	TUC, Univ. of Montpellier, CINVESTAV, McMaster University, Univ. of Giessen	30	Yes
INPG/ FMNT	International Summer school	MIGAS 2010, MEMS & NEMS: New Technologies and Advanced Devices	Autrans, France, June 2010			Yes
AMO	Workshop	Carbon Electronics	13/14 July 2010, Aachen	AMO, RWTH Aachen, IUNET, Chalmers	12 (Nanonsil) + *43* = 55	Yes
Grenoble INP -Sinano Institute	Workshop	SINANO-NANOSIL and VP1.4 Workshop: "On the convergence between More Moore, More Than Moore and Beyond CMOS"	Sept. 2010, Seville	All Nanosil Partners + beyond (Infineon, IBM-switzerland, etc.)	75 *(30)*	Yes
UGR	Seminar	Nanoelectronics: a tool to face the future	September 13-2010	UGR	30	Yes
INPG	Workshop	ENI2-NanoFET	March 2011, Cork	Most of Nanosil partners + industry+ SME	~50 (half from Nanosil)	Yes
IMEL/ NCSR	International Conference	Micro&Nano2010-International Conference on Microelectronics, Nanoelectronics, Nanotechnologies and MEMs	12-15 December 2010, Athens-Greece	IMEL, IMEP and several others	Inside Nanosil : 25 Outside Nanosil : 135	Yes
LETI & INPG	Panel session	SOI technologies : What kind or research for what kind of products ?	January 26th, 2010 Grenoble, France	All Nanosil partners + Soitec, SOI Consortium, Global Foundries, Stanford Univ., etc.	110 (~70 from Nanosil)	Yes/ VP1.4
IMEC	Workshop and panel	"High mobility nMOS substrates: strained-Si, Ge or III-V?"	17/01/2010 Glasgow, UK	All Nanosil partners	~90 (~70 from Nanosil)	Yes/ VP1.4
GU & IUNET	Workshop and panel	"Simulation and Characterization of Statistical CMOS Variability and Reliability"	September 9th, 2010 Bologna, Italy	All Nanosil partners + Toshiba, Univ. of California, Tokyo Univ., TCAD vendors, ets.	~55	Yes/ VP1.4
RWTH Aachen	Workshop	Beyond CMOS Routes (More details reported in Deliverable D2.7)	26 Feb 2011	RWTH Aachen, AMO, Chalmers, USTUTT, CEA-LETI, FZ Jülich, *University of Washington, University of Dortmund*	12 / *55*	Yes/ VP2.5
UGR	Conference	ESSDERC-2010	13-17/09 2010, Seville, Spain	All NANOSIL + number of other	700	No
INPG/ FMNT	Conference	Euro-SOI 2010	Grenoble, France, January 2010	All Nanosil + beyond	~100	No
UGR	Workshop	EuroSOI 2011	19th-21st January 2011	All Nanosil + beyond (UT Dallas, IBM, Soitec, LEAP, etc.)	80 (about 2/3 Nanosil)	No
Tyndall	Conference	Ultimate Integration on Silicon (ULIS 2011)	Cork, Ireland, 14-16 /03/ 2011	23 countries	80	Nanofunction
INPG/ FMNT	Conference	INFOS 2011	Grenoble, France, June 2011			No

INPG/ FMNT	International Summer school	Nano-KISS (Intenational Summer School on Nanoelectronics)	Daegu, Korea, April 2011			No
INPG & UGR	Roundtable	The contribution of SOI in the brilliant future of Nanoelectronics	January 2011, Granada	Most of Nanosil partners + UT Dallas, IBM, Soitec, LEAP	~100 (half from Nanosil)	No
UGR	SOI technologies for future electronics	SOI & Nanoelectronics	January 16th, 2011	UGR	60	No
UCL	Meeting	Characterization of advanced devices	Dec. 2010	UCL + Infineon	8	No
UCL	Meeting	Design low power, Characterization	May 2010	UCL + ST	12	No
UCL	Meetings	Perspectives of UTB SOI MOSFETs for analog and RF applications	March 2011	UCL + Soitec	5	No
WUT	Meeting	Recent developments and challenges in nano- and micro-electronics	November 26th 2010 WUT	Students	approx. 50	No
WUT	Meeting	Research carried out in Division of Microelectronics and Nanoelectronics Devices	October 15th 2010 WUT	Students	approx. 80	No
WUT	Meeting	Flash Memories	March 4th WUT	Samsung, WUT	15 (6 WUT, *9 Samsung*)	No

***** *in* ***bold*** *the ones inside NANOSIL, in Italic - outside NANOSIL*

4.3. University courses.

Three **new university courses** (total of 65 h) in Nanosil field have been started during 2010, which is smaller than in 2009. However, we should not consider it as a bad sign, firstly, because courses introduced in 2009 most probably continued this year and secondly, 4 meetings/schools cited above targeted particularly last-years and PhD students.

Nanosil partner	Title	Author	Hours
UPS	"Nanostructures for Electronics", lecture which is a part of the new Nanosciences Master co-accredited by Université Paris Sud 11 (UPS), the Institut d'optique Graduate School, the École normale supérieure (ESN) in Cachan, the École polytechnique, the École centrale Paris, SUPÉLEC et and Université de Versailles Saint-Quentin-en-Yvelines	P. Dollfus	27
USTUTT	Quantenelektronik	Prof. J. Schulze	20
WUT	Fundamentals of devices, circuits and systems technology	R. Mroczyński	18

5. Dissemination of knowledge

5.1. Inside of NoE

Dissemination of knowledge within Nanosil is provided through **the Executive & Scientific Committee meetings** (each 3 months), **Governing Board meeting**, **kick-off, regular and cross WPs/FPs meetings** (see section 1.1 for details). Additionally, **exchanges/ trainings** of personnel played an important role in information/ideas/competences exchange between partners.

5.2. Beyond NoE

Web-site of Nanosil was created in 2008. It aims to promote NoE, its activities such as workshops/ trainings and competences of Nanosil partners. Taking into account recommendations from the reviewers, during 2009 web-site was modified rather strongly in order to make information wider available to public and not restricted to consortium area and clearly identify processing, characterization & modeling platforms existing in Nanosil. Number of useful information (links, pdf files) can be found on the site even in a public area, as e.g. pdf-version of Who is Who guide (as well as Who is Who guide of beyond Nanosil partners), List of national and EU projects of relevance, training/courses/PhD thesis topics available, Agenda of Workshops, Conferences, etc.

During 2010-11 we did regular (routine) update of the information available on our web-site:

- national and EU projects;
- list of joint Nanosil publications (with corresponding doi to ease the access to the published papers);
- breaking (or “hot”) news;
- agenda of conferences/workshops/schools relevant to Nanosil fields;
- list of workshops/schools supported (partially funded) by Nanosil;
- open positions;
- trainings/workshops available on the site of industrial (and semi-industrial) partners;
- etc.

32 workshops/schools/conferences/tutorials have been organized during 2010-11 by Nanosil partners, i.e. about 30% more than during 2009. Such events accessible not only to Nanosil partners but to a wide scientific community are very important to disseminate a knowledge gathered by Nanosil members and to widely promote our Network.

It is worth to point out an active participation of Nanosil partners in the **ENI2** initiative. It aims a creation of long and lasting **R&D infrastructure** (in another words ecosystem) for **European nanoelectronic innovations**, thus allowing **long-term integration** of academic institutions together with institutes, industries and SMEs. Different actions targeted strengthening the durable integraton of the partners are grouped in Annex 1.

Nanosil News letter 2009 was issued in February 2010. It groups the most impressive Nanosil achievements during 2009. All flagship projects as well as simulation/characterization and processing workpackages presented their most important results. Additionally, targeting beyond Nanosil auditorium, some general information about Nanosil as well as WP5 information on the possibility for Beyond Nanosil institution to participate in the network (e.g. through exchanges and Who is Who guide on the Nanosil web-site) are included.

Nanosil NewsLetter 2009 is available on Nanosil web-site in a public area and was also e-mailed to the available mail lists.

Nanosil News letter 2010-11 is under preparation. When finished it will also be available on Nanosil and SINANO Inst. web-sites as well as e-mailed to the available mail lists.

Finally, achievements / knowledge gathered within Nanosil are widely disseminated through the **publications in major international journals** and **participation** of Nanosil members in **international conferences/workshops**.

2 books jointly edited by Nanosil partners were published during 2010-11. First one, **"Nanoscale CMOS: Innovative Materials, Modeling and Characterization"**, is entirely devoted to the results obtained by the groups involved in Nanosil. It addresses all WPs of Nanosil and covers both processing and characterization/modelling aspects. More details about this book can be found in D5.4. Second book **"Semiconductor-on-Insulator Materials for nanoelectronics applications"** was published by SPRINGER in 2011 as a result of SemOI Workshop jointly organized by UCL and ISP-Kiev and financially supported by Nanosil (see section 4.2). Comparing to the first one, it goes a bit further in addressing "more than moore" and "beyond CMOS" fields. It groups selected keynote works in the four areas: 1° new semiconductor-on-insulato r materials; 2° physics of modern SemOI devices; 3° diagnostics of the SOI devices; 4° sensors and M EMS on SOI. More than half of chapters in this book were prepared by Nanosil partners.

33 Book chapters (see Annex 2, separately for joint and single-partner) were prepared by Nanosil partners in 2010-11; **12** of them are **joint**. It is worth to point out very high number of book chapters written by Nanosil partners during this last period of NANOSIL.

114 papers (see lists of joint and single-partner papers separately in Annex 2) in high-level international journals have been prepared by Nanosil members in 2010-11, among which **98** articles are already published and **16** are accepted for publication in 2011. **40** of them are **joint papers**, among which **32** articles are already published, **8** are accepted for publication in 2011. Here we included only journal publications in peer reviewed journals (+IEDM conference), while the numbers will be well greater if we would take into account publications in a conference proceedings (which follow almost all conferences listed below). Only publications clearly acknowledged Nanosil are listed.

165 conference/workshop presentations (see list of references in Annex 2) were given by Nanosil partners in 2010-11, among which **32 are invited presentations**. **52** and **5** of them, respectively, are **joint** presentations.

Moreover, **7 other dissemination** items (thesis, film, etc., see the list below) were done by Nanosil partners (**3** of them are **joint**).

ANNEX 1. Actions for strengthening the durable integration of the partners

All these activities will contribute to the durable integration of the partners. However, some very important specific actions have been launched for the strengthening of this durable integration:

- One partner of Nanosil NoE (Tyndall-Cork) became Members of the Sinano Institute in 2009, which is a legal entity (Scientific Association) created in January 2008 for the coordination of the European Academic Community working in the field of Nanoelectronics (launched for the durable integration of the FP6 Sinano NoE). Furthermore, six other European Institutions became Members of the Sinano Institute in 2011, in line with the new FP7 NoE Nanofunction launched at the end of the Nanosil NoE (ICN-Barcelona, VTT-Helsinki, Twente University, IES-Montpellier University, IMS Demokritos-Athens, Uppsala University).

- The Joint Processing, Joint Characterization and Modelling Platforms, which have been developed and used in the framework of the Nanosil NoE for our joint research activities are now integrated as open Research Infrastructures in the Sinano Institute and can be used by the European Academic Community, SMEs and Industry. The movie describing our platforms was realized in January 2011 in order to promote our available facilities and their accessibility to a wide scientific/industrial community.

- Nanosil Partners and Sinano Institute Members have been strongly associated to the new initiative launched in 2010 by STMicroelectronics called ENI2 (European Nanoelectronics Infrastructure for Innovation). This Infrastructure (or in another words, eco-system) is proposed to coordinate the three levels of R&D activities needed in the nanoelectronics domain. The 1st level is coordinated by the Academic Community (the main contact is the Sinano Institute, it will ensure the coordination of this level) for long term researches (fundamental understanding, test and validation of innovative materials, processes and architectures in order to identify the most promising topics for future ICT). The 2nd level is coordinated by the Integration Centres (large European pre-industrial Institutes) for technology implementation and performance assessment of the most promising topics defined at level 1 on R&D equipments, and development of high performance logic, memories and derivatives (medium term). The 3rd level is coordinated by the European industrial companies for technology exploitation as functional products, process optimisation, yield, product reliability, device and interconnect architecture and design (short term).

- A significant part of Nanosil Partners have launched a new FP7 NoE, Nanofunction, devoted to Beyond-CMOS nanodevices for adding functionalities to CMOS in the More than Moore domain (nanosensing, energy harvesting, nanocooling, RF). An important part of Nanosil

results, especially those devoted to Nanowires mainly developed in Nanosil for ultimate CMOS applications, will be used in Nanofunction for the development of advanced nanodevices to be used in future nanosystems. On the other hand, many Nanosil Partners have been involved in the FET Flagship “Guardian Angels” proposal dedicated to future autonomous ultra low power systems for health and environmental monitoring. It has been selected as a pilot project (beginning in May 2011). Some other examples of new projects launched by and involved number of Nanosil partners are FP7 STREPs STEEPER and SQWIRE.

ANNEX 2 References

A2.1. Books/Book chapters (joint): 2+12

NO.	Type of activities	Main leader/ author Partners involved	Title of event	Title of paper/presentation/etc. Emphasize if invited	WP/ FP	Date
1	Book	INPG/FMNT (Editor), Almost all partners (see D5.4 for details)	ISTE-Wiley book (650 pages)	Nanoscale CMOS: Innovative Materials, Modeling and Characterization	1-4	2010
2	Book	Tyndall, ISP-Kiev, INPG/FMNT, UCL, UGR	Springer (450 pages) Doi : 10.1007/978-3-642-151868-1	Semiconductor-On-Insulator Materials for NanoElectronics Applications	1, 2, 4	2011
3	Book chapter	O. Engstrom Chalmers, LIVUNI, Tyndall, AMO	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 2 : Gate Stacks	1.3	2010
4	Book chapter	B. Majkusiak et al WUT, IUNET, ETZH	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 7: Modeling and simulation approaches for gate current computation	4	2010
5	Book chapter	Q. Rafhay et al. INPG, IUNET	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 9: Modeling of end of the roadmap nMOSFET with Alternative channel material	4	2010
6	Book chapter	Martinez et al INPG, GU	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 10: NEGF for 3D device simulation of nanometric inhomogenities	4	2010
7	Book chapter	G. Iannaccone et al, IUNET, INPG	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 12 : Beyond CMOS	4	2010
8	Book chapter	P. Hurley et al Tyndall-UCC, Chalmers, INPG	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 15: Characterization of interface defects	4	2010
9	Book chapter	Lecestre et al. IEMN/ISEN, STM	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Confined and guided vapor-liquid-solid catalytic growth of Silicon nanoribbons: from nanowires to structured silicon-on-insultor layers	2	2011
10	Book chapter	Afzalian, et al. UCL, Tyndall-UCC	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Gate modulated resonant tunneling transistor (RT-FET): performance investigation of a steep slope, high on-current device through 3D non-equilibrium green function simulations", chapter in "Semiconductor-On-Insulator Materials for NanoElectronics Applications"	4	2011
11	Book chapter	T. Rudenko et al ISP-Kiev, UCL	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on " Special features of the back-gate effects in ultra-thin body SOI MOSFETs", chapter in "Semiconductor-On-Insulator Materials for NanoElectronics Applications"	4	2011
12	Book chapter	M. Bawedin et al. INPG, Leti	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Floating-body SOI memory: the scaling tournament"	4	2011
13	Book chapter	S. Cristoloveanu et al. INPG, Leti, ST	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "A selection of SOI puzzles and tentative answers"	4	2011
14	Book chapter	W. van den Daele et al INPG, IMEC	Wiley (S. Luryi et al. eds) "Future Trends in Microelectronics, from Nanophotonics to Sensors and Energy"	GeOI as a platform for ultimate devices	1, 4	2010

A2.2. Book chapters (single-partner): 21

NO.	Type of activities	Main leader/ author Partners involved	Title of event	Title of paper/presentation/etc. Emphasize if invited	WP/ FP	Date
1	Book Chapter	D. Leadley et al Warwick	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 1: Introduction to Part 1: Novel materials for nanoscale CMOS	1	2010
2	Book chapter	D.R. Leadley, et al	Book, "Nanoscale CMOS: Innovative	Chapter 3: Strained Si and Ge Channels	1	2010

		Warwick	Materials, Modeling and Characterization", ISTE – Wiley			
3	Book chapter	S. Mantl, D ; Buca, FZJ	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 4: From thin Si/SiGe buffers to SSOI	1	2010
4	Book chapter	E. Dubois et al, IEMN/ISEN	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 5: Intorduction to Schottky-barrier MOS architectures: concept, challenges, material engineering and deivce integration	1	2010
5	Book chapter	E. Sangiorgi IUNET	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 6: Introduction to Part 2: Advanced modeling and simulation for nano-MOSFETs and beyond-CMOS devices	4	2010
6	Book chapter	M. Vasicek et al. IUNET	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 8: Modeling and simulation approaches for drain current computation	4	2010
7	Book chapter	B. Iniguez et al. URV	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 11: Compact models for advanced CMOS devices	4	2010
8	Book chapter	D. Flandre UCL	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 13: Introduction to Part 3: Nanocharacterization methods	4	2010
9	Book chapter	M. Mouis INPG	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 14: Accurate determination of transport parameters in sub-65 nm MOS transistors	4	2010
10	Book chapter	A. O'Neill et al. UNEW	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 16 : Strain determination	4	2010
11	Book chapter	D. Flandre et al. UCL	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 17: Wide frequency band characterization	4	2010
12	Book chapter	J.-P. Raskin UCL	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "SOI SMOS: A mature and still improving technology for RF applications"	4	2011
13	Book chapter	F. Balestra INPG	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Silicon-based devices and materials for nanoscale FETs"	1-4	2011
14	Book chapter	F. Gamiz et al. UGR	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on « Ultrathin n-channel and p-channel SOI MOSFETs"	4	2011
15	Book chapter	J.-P. Colinge et al. Tyndall-UCC	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Junctionless transistors: physics and properties"	2, 4	2011
16	Book chapter	H.-N. Nguyen et al UPS	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on " Ohmic and Schottky contact SNTFET: transport properties and device performance using semi-classical and quantum particle simulation""	2, 4	2011
17	Book chapter	M. Pala, INPG	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on « Quantum simulation of Silicon-Nanowire FETs"	2, 4	2011
18	Book chapter	G. Gibaudo, INPG	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Mobility characterization in advanced FD-SOI CMOS devices"	4	2011
19	Book chapter	J.-P. Raskin et al UCL	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on " Sensing and MEMS devices in thin-film SOI MOS technology"	2	2011
20	Book chapter	INPG/FMNT	Wiley (S. Luryi et al. eds) "Future Trends in Microelectronics, from Nanophotonics to Sensors and Energy"	Silicon-based devices and materials for nanoscale CMOS and beyond-CMO, chapter in	1, 2, 4	2010
21	Publication	E. Kasper, USTUTT	Horizons in World Physics. Volume 273 (ISBN: 978-1-61728-995-8)	Positioning Ge-Dots on Si for Device Applications/Book chapter /pp. 171-185	2.4	2010

A2.3. Journal publications (joint): 32+8

NO.	Title	Main author, Partners involved	WP/ FP	Title of the periodical	Vol., No .	Year	Pages	Permanent identifiers DOI
1	Defect-related excess low-frequency noise in Ge-on-Si pMOSFETs	E. Simoen, et al Warwick, IMEC	1	Electron Device Letter	Vol 32	2011	pp 87-89	http://dx.doi.org/10.1109/LED.2010.2089968
2	A quasi-analytical model for anowires FETs with arbitrary polygonal cross section	L. De Michielis, et al IUNET, EPFL	4	Solid-State Electronics	Sept	2010	929 – 934	doi :10.1016/j.sse.2010.04.039
3	Physics of Gate Modulated Resonant Tunneling (RT)-FETs: Multi-Barrier MOSFET for Steep Slope and High On-Current	Afzalian et al UCL, Tyndall	4	Solid State Electronics		2011	pp. 50-61	doi :10.1016/j.sse.2011.01.016
4	Quantum Confinement Effects in Capacitance Behavior of Multigate Silicon Nanowire MOSFETs	A. Afzalian et al. : Tyndall, UCL	4	IEEE Trans. On Nano-technology	vol. 10, march	2010	pp. 300-309	10.1109/TNANO.2009.2039800
5	Low temperature tunneling current enhancement in silicide/Si Schottky contacts with nanoscale barrier width	N. Reckinger et al UCL, IEMN	1.2	Appl. Phys. Lett.	No 98, 2011	2011	112102	10.1063/1.3567546
6	Gate-edge charges related effects and performance degradation in advanced multiple-gate MOSFETs	V. Kilchytska, UCL, IMEC	4	Solid State Electronics	Vol. 59, 2011	2011	pp. 18-24	10.1016/j.sse.2011.01.008

7	Experimental study of transconductance and mobility behaviors in ultra-thin SOI MOSFETs with standard and thin buried oxides	T. Rudenko, ISP_kiev, UCL, Leti	4	Solid State Electronics	Vol. 54, Feb. 2010	2010	pp. 164-170	10.1016/j.sse.2009.12.014
8	Substrate impact on threshold voltage and subthreshold slope of sub-32 nm ultra thin SOI MOSFETs with thin buried oxide and undoped channel	S. Burignant, et al UCL, Leti	4	Solid State Electronics	Vol. 54, Feb 2010	2010	pp. 213-219.	10.1016/j.sse.2009.12.021
9	Gm/Id Method for Threshold Voltage Extraction Applicable in Advanced MOSFETs With Nonlinear Behavior Above Threshold	D. Flandre, et al UCL, ISP-Kiev	4	IEEE Electron Dev. Lett.	Vol. 31, Sept. 2010	2010	pp. 930-932	10.1109/LED.2010.2055829
10	Radio-Frequency Study of Dopant-Segregated n-Type SB-MOSFETs on Thin-Body SOI	C. Urban et al FZJ, UCL	1.1 &1.2	Electron Device Letters	Vol. 32, Issue 6	April 2010	537 – 539	10.1109/LED.2010.2045220
11	Strain tensors in layer systems by precision ion channeling measurements	Trinkaus et al FZJ, Leti	1.1	J. of Applied Physics	Vol. 107 Issue 12	2010	124906 (8 pp)	doi :10.1063/1.3415530
12	Reduced electric field in junctionless transistors	JP Colinge et al, Tyndall, ISP-Kiev	2	Applied Phys. Letters	Vol. 96	2010	073510	10.1063/1.3299014
13	Low subthreshold slope in junctionless multigate transistors	JP Colinge et al, Tyndall, ISP-Kiev	2	Applied Phys. Letters	Vol. 96	2010	102106	doi :10.1063/1.3358131
14	Mobility Improvement in Nanowire Junctionless Transistors by Uniaxial Strain	JP Raskin et al, UCL, Tyndall	2, 4	Applied Physics Letters	Vol. 97	2010	042114	doi :10.1063/1.3474608
15	Effect of intravalley acoustic phonon scattering on quantum transport in multigate silicon nanowires metal-oxide-semiconductor field-effect transistors	N.D. Akhavan et al, Tyndall, UCL	2, 4	Journal of Applied Physics	Vol. 108	2010	034510	doi :10.1063/1.3457848
16	Random telegraph-signal noise in junctionless transistors	A. Nazarov, ISP-Ukraine,Tyndall	2, 4	Applied Phys. Letters	Vol. 98,	2011	103510. 1-3	10.1063/1.3557505
17	Low-frequency noise in junctionless multigate transistors	D. Jang et al INPG, Tyndall	2, 4	Applied Phys. Letters	Vol. 98	2011	p. 133502	doi:10.1063/1.3569724
18	Electrical Properties of LaLuO3/Si(100) Structures Prepared by Molecular Beam Deposition	Yu. Gomeniuk, et al. ISP-Kiev, Tyndall-UCC, AMO, FZJ, Chalmers	1.3	ECS Transactions	33 (3)	2010	pp. 221-227	10.1149/1.3481609
19	Implementation of the symmetric doped double-gate MOSFET model in Verilog-A for circuit simulation	J. Alvarado, et al URV, UCL	4	Int. J. of Numerical Modelling: Electronic Networks, Devices and Fields	Vol 23 (2)	2010	pp. 88-106	10.1002/jnm.725
20	Accurate prediction of the volume inversion impact on undoped Double Gate MOSFET capacitances	O. Moldovan, et al URV, UCL	4	Int. J. of Numerical Modelling: Electronic Networks, Devices and Fields	Vol 23 (6)	2010	pp.447-457	10.1002/jnm.725
21	The equivalent thickness concept for doped symmetric DG MOSFETs	J-M. Sallese et al URV, EPFL	4	IEEE Trans. On Electron Devices	Vol 57 (11)	2010	pp. 2917-2924	10.1109/TED.2010.2071090
22	Why the Universal Mobility Is Not	S. Cristoloveanu, et al UGR, INPG	4	IEEE Trans. On Electron Devices	Vol 57	2010	1327-1333	10.1109/TED.2010.2046109
23	Charging Phenomena at the Interface Between High-k Dielectrics and SiOx Interlayers	O. Engstrom Chalmers, Livuni, Tyndall, AMO	1.3	J. Telecomm. Inf. Tech.	1	2010	10 – 18	NOT available
24	CV Measurements on $LaLuO_3$ Stack MOS Capacitor Using a New 3-Pulse Technique	N. Sedghi LIVUNI, Julich	1.3	J. of Vacuum Scie. And Technology B	Vol. 29, issue 1,	2011	01AB03-1 – 6	10.1116/1.3533267
25	The high-mobility bended n-channel silicon nanowires transistor	KE Moselund, et al EPFL, UNEW	2	IEEE Trans. On Electron Devices	vol. 57, no. 4	2010	p. 866-876	10.1109/TED.2010.2040939
26	Silicon nanowires with lateral uniaxial tensile stress profiles for high electron mobility gate-all-around MOSFETs	M Najmzadeh, et al. EPFL, UNEW	2	Microelectronic Engineering	vol. 87	2010	pp. 1561-1565	10.1016/j.mee.2009.11.024
27	Strained Si heterojunction bipolar transistor	S Persson et al UNEW, KTH	1	IEEE Trans. On Electron Devices	vol 57,	2010	p. 1243	10.1109/TED.2010.2045667
28	Low-temperature characterization and modeling of advanced GeOI pMOSFETs: Mobility mechanisms and origin of the parasitic conduction	W. Van Den Daele, INPG, CEA/Leti	1, 4	SSE	Vol. 54	2010	pp. 205-212	10.1016/j.sse.2009.12.020
29	Direct measurement of MOSFET channel strain by means of backside etching and Raman spectroscopy on long channel devices	RMB Agaiby, et al UNEW, IMEC	1, 4	IEEE Electron Device Letters	vol. 31, no. 5	2010	pp. 419-421	10.1109/LED.2010.2043496
30	Detailed investigation of effective field, hole mobility and scattering mechanisms in GeOI and Ge pMOSFETs	Van den Daele et al, INPG, Leti, Imec	1, 4	SSE	Vol. 59	2011	pp. 25-33	10.1016/j.sse.2011.01.014

31	Double-gate 1T-DRAM cell using nonvolatile memory function for improved performance	K-H. Park et al, INPG, Korea	4	SSE	Vol. 59	2011	pp. 39-43	10.1016/j.sse.2011.01.007
32	Capacitor-less A-RAM SOI memory: Principles, scaling and expected performance	N. Rodriguez et al INPG, UGR	4	SSE	Vol. 59	2011	pp.44-49	10.1016/j.sse.2011.01.006
ACCEPTED PAPERS – IN PRESS								
1	High hole mobility in 65nm strained Ge-pFETs with HfO_2 gate dielectric	J. Mitard, et al Warwick, IMEC	1	Japanese Journal of Applied Physics	Accepted Nov 2010,	2011 April		
2	Investigation of strain engineering in FinFETs comprising experimental analysis and numerical simulations	F. Conzatti, et al IUNET, Warwick, IMEC	1, 4	IEEE Trans Electron Devices		Accepted 2010		
3	Erbium silicide growth in the presence of residual oxygen	N. Reckinger, et al UCL, IEMN	1.2	J. Electrochem. Soc.		2011		
4	Transport and Interface States in High-k LaSiOx Dielectric	Yu. Gomeniuk ISP NAS of Ukraine, Tyndall-UCC	1.3	Microelectronic Engineering INFOS'2011		2011	accepted	
5	Studies of the quality of GdSiO-Si interface	M. Iwanowicz (WUT, AMO)	1.3	Microelectronics Reliability	2011 - accepted	2011		
6	A Simplified Physical DC Model for Undoped UTB SOI and Asymmetric DGMOSFETs with Independent Gate Operation	F. Lime, et al URV, Leti	4	Solid-State Electronics	accepted			
7	Investigation of Electron and Hole Charge Trapping in $LaLuO_3$ Stack MOS Capacitor Using the 3-Pulse CV Technique	N. Sedghi LIVUNI, Julich	1.3	ECS Transactions	April 2011	2011	In print	
8	A comparative study of surface-roughness induced variability in silicon nanowire and double-gate FETs	INPG/FMNT, IUNET	2, 4	IEEE Trans. on Electron Devices	Special Issue on Variability	2011	7 pages	Not yet available. Accepted

A2.4. Journal publications (only single-partner): 66+8

NO.	Title	Main author, Partners involved	WP/ FP	Title of the periodical	Vol., No.	Year	Pages	Permanent identifiers DOI
1	Effect of growth rate on the threading dislocation density in relaxed SiGe buffers grown by reduced pressure chemical vapour deposition at high temperature	A Dobbie, et al Warwick	1	Semiconductor Science and Technology	Vol 25,	2010	085007	10.1088/0268-1242/25/8/085007
2	Highly strained Si epilayers grown on SiGe/Si(100) virtual substrate by Reduced Pressure Chemical Vapour Deposition	M. Myronov, et al Warwick	1	Physica Status Solidi C	Vol 8	2011	pp 952-955	DOI: 10.1002/pssc.201000255
3	Mobility Enhancement in Strained n-FinFETs: Basic Insight and Stress Engineering	N. Serra and D. Esseni; IUNET-Udine	4	IEEE Trans. on Electron Devices	February	2010	482-490	10.1109/TED.2009.2037369
4	An improved empirical approach to introduce quantization effects in the transport direction in multi-subband Monte Carlo simulations	P.Palestri, et al IUNET-Udine	4	Semiconductor Science and technology	vol. 25, No. 5	2010	055011	10.1088/0268-1242/25/5/055011
5	Simple and efficient modeling of the E–k relationship and low-field mobility in Graphene Nano-Ribbons	M. Bresciani, et al IUNET-Udine	4	Solid-State Electronics	Sept.	2010	1015-1021	10.1016/j.sse.2010.04.038
6	Failure of the Scalar Dielectric Function Approach for the Screening Modeling in Double-Gate SOI MOSFETs and in FinFETs	P.Toniutti, et al IUNET-Udine	4	IEEE Trans. on Electron Devices	Nov.	2010	3074-3083	10.1109/TED.2010.2068990
7	Pseudospectral Methods for the Efficient Simulation of Quantization Effects in Nanoscale MOS Transistors	Alan Paussa et al. IUNET	4	IEEE Trans. on Electron Devices	Dec.	2010	3239-3249	10.1109/TED.2010.2081673
8	Electric Field Control of Spin Rotation in Bilayer Graphene	P. Michetti, et al IUNET Pisa	4, 2	Nano Letters	10,11	2010	4463 – 4469	10.1021/nl102298n
9	Simulation of hydrogenated graphene field-effect transistors through a multiscale approach	G. Fiori, et al I UNET Pisa	4, 2	Phys. Rev. B	82, 15	2010	153404	10.1103/PhysRevB.82.153404
10	Barrier Lowering and Backscattering Extraction in Short-Channel MOSFETs	G. Giusi, et al IUNET	4	IEEE Trans. on Electron Devices	57, 9	2010	2132 – 2137	10.1109/TED.2010.2055273
11	Model and Performance Evaluation of Field-Effect Transistors Based on Epitaxial Graphene on SiC	M.Cheli, P.Michetti, G.Iannaccone - IUNET Pisa	4, 2	IEEE Trans. on Electron Devices	57, 8	2010	1936 – 1941	10.1109/TED.2010.2051487
12	Analytical Model of One-Dimensional Carbon-Based Schottky-Barrier Transistors	P.Michetti, G.Iannaccone - IUNET Pisa	4, 2	IEEE Trans. on Electron Devices	57, 7	2010	1616 – 1625	10.1109/TED.2010.2049219
13	Statistical Theory of shot noise in quasi-one-dimensional field-effect transistors in the presence of electron-electron interaction	A. Betti, G. Fiori, G. Iannaccone - IUNET Pisa	4	Physical Review B	81, 7	2010	035329	10.1103/PhysRevB.81.035329

14	Model of tunneling transistors based on graphene on SiC	P.Michetti, et al IUNET Pisa	4, 2	Applied Physics Letters	96	2010	133508 – 1/3	10.1063/1.3361657
15	Effects due to backscattering and pseudogap features in graphene nanoribbons with single vacancies	I. Deretzis et al IUNET Pisa	4, 2	Physical Review B	81, 8	2010	085427 – 1/5	10.1103/PhysRevB.81.085427
16	Effective Mobility in Nanowire FETs under Quasi-Ballistic Conditions	E. Gnani, et al IUNET-Bologna	4	IEEE Trans. on Electron Devices	Vol. 57	2010	336 – 343	10.1109/TED.2009.2035545
17	A Low-Field Mobility Model for Bulk, Ultrathin Body SOI and Double-Gate n-MOSFETs With Different Surface and Channel Orientations—Part I: Fundamental Principles	L. Silvestri, et al IUNET-Bologna	4	IEEE Transactions on Electron Devices	Vol. 57	2010	1567 – 1574	10.1109/TED.2010.2049210
18	A Low-Field Mobility Model for Bulk, Ultrathin Body SOI and Double-Gate n-MOSFETs With Different Surface and Channel Orientations—Part II: Ultra-Thin Silicon Films	L. Silvestri, et al IUNET-Bologna	4	IEEE Transactions on Electron Devices	Vol. 57	2010	1575 – 1582	10.1109/TED.2010.2049211
19	A Low-Field Mobility Model for Bulk and Ultrathin-Body SOI p-MOSFETs With Different Surface and Channel Orientations	L. Silvestri, et al IUNET-Bologna	4	IEEE Transactions on Electron Devices	Vol. 57	2010	3287 – 3294	10.1109/TED.2010.2078821
20	3D simulation of triple-gate MOSFETs with different mobility regions	J. Conde et al, UCL, Mexico, Brazil	4	Microelectronic Engineering	2011	2011		10.1016/j.mee.2011.03.013
21	Realization of ultra dense arrays of vertical silicon NWs with defect free surface and perfect anisotropy using a top-down approach	X-L. Han, et al ISEN-IEMN	2.1	Microelectronic Engineering		2011	on-line 4 january 2011	10.1016/j.mee.2010.12.102
22	Realization of vertical silicon nanowire networks with an ultra high density by top-down approach	X.L. Han, et al ISEN-IEMN	2.1	J. of Nano-scie. and Nanotechnology	10	2010	7423-7427	10.1166/jnn.2010.2841
23	Conduction gap in double gate bilayer graphene structure'	V. Hung Nguyen, UPS	2.2	J. Phys.: Condens. Matter	No 22	2010	115304 (6 pages)	10.1088/0953-8984/22/11/115304
24	Negative differential resistance in zigzag-edge graphene nanoribbon junctions	V. Nam Do UPS	2.2	J. Appl. Phys.	No 107	2010	063705 (5 pages)	10.1063/1.3340834
25	Implementation of the Wigner-Boltzmann transport equation within particle Monte Carlo simulation	D. Querlioz, UPS	2 & 4	J. Comput. Electron.	No 9	2010	224-231	10.1007/s10825-009-0281-3
26	Semi-classical and quantum transport in CNTFETs using Monte Carlo simulation	H. Nha Nguyen UPS	2.2, 4	IEEE Trans. Electron Devices	No 58	2011	798-804	10.1109/TED.2010.2096820
27	Electrical characterization of strained and unstrained silicon nanowires with nickel silicide contacts	S. Habicht, FZJ	1.1 & 1.2, 4	Nanotechnology	Vol. 21, No. 10, 2010	2010	105701 (5 pages)	10.1088/0957-4484/21/10/105701
28	Ultrathin Ni Silicides With Low Contact Resistance on Strained and Unstrained Silicon	L. Knoll et al FZJ	1.1 &1.2	Electron Device Letters	Vol. 31 ,Issue 4	April 2010	350 - 352	10.1109/LED.2010.2041028
29	Electrical characterization of $TbScO_3$/TiN gate stacks in MOS capacitors and MOSFETs on strained and unstrained SOI	Özben et al FZJ	1.1 & 3	ECS Transactions	Vol.33. No3	2010	195-202	10.1149/1.3481606
30	Formation of steep, low Schottky-barrier contacts by dopant segregation during nickel silicidation	Feste et al FZJ	1.1 &1.2	Journal of Applied Physics	Vol. 107 Issue 4	Jan. 2010	044510 (6 pages)	10.1063/1.3284089
31	Elastic strain and dopant activation in ion implanted strained Si nanowires	Minamisawa et al FZJ	1.1	J. of Applied Physics	Vol. 108, Issue 12	Dec. 2010	124908 (9 pages)	10.1063/1.3520665
32	Integration of $LaLuO_3$ as High-k Dielectric on Strained and Unstrained SOI MOSFETs With a Replacement Gate Process	Özben et al FZJ	1.1 & 1.3 & 3	Electron Device Letters	Vol. 32, Issue 1	Jan. 2011	15-17	10.1109/LED.2010.2089423
33	Rare-earth oxide/TiN gate stacks on high mobility strained silicon on insulator for fully depleted metal-oxide-semiconductor field-effect transistors	Özben et al FZJ	1 & 3	Journal of Vacuum Science & Technology B	Volume 29 / Issue 1	Jan 2011	01A903-1 to 01A903-5	10.1116/1.3533760
34	Rare-Earth Scandate/TiN Gate Stacks in SOI MOSFETs Fabricated With a Full Replacement Gate Process	Özben et al FZJ	1.1 & 3	Trans. Electron Devices	Vol. 58, No 3	March 2011	617 - 622	10.1109/TED.2010.2096509
35	Ge quantum dot tunneling diode with room temperature negative differential resistance	M. Oehme, USTUTT	2.4	APPLIED PHYS. LETTERS	Vol 97, Issue 1	2010	012101 (3 pages)	doi:10.1063/1.3462069
36	Multiwavelength micro-Raman analysis of strain in nanopatterned ultrathin strained silicon-on-insulator	O. Moutanabbir, et al USTUTT	1.1 & 1.2	APPLIED PHYS. LETTERS	Vol 97, Issue 5	2010	053105 (3 pages)	doi:10.1063/1.3475399

37	Composition and strain in thin Si_{1-x} Ge_x virtual substrates measured by micro-Raman spectroscopy and x-ray diffraction	T. S. Perova, et al USTUTT	2.4	JOURNAL OF APPLIED PHYSICS	Vol 109, Issue 3 Feb. 2011	2011	033502 (11 pages)	doi:10.1063/1.3536508
38	Lateral electronic transport in 2D arrays of oxidized Si nanocrystals on quartz: Coulomb blockade effect and role of hydrogen passivation	P. Manousiadis, et al NCSR/ IMEL	2.2	Journal of Applied Physics	Twice a month	April 2011	Not known yet	DOI: 1063/1.3575331
39	Nanowire transistors without junctions	JP Colinge et al Tyndall	2	Nature Nano-technology	Vol. 5, No. 3	2010	225-229	10.1038/NNANO.2010.15
40	LDD and Back-Gate Engineering for Fully Depleted Planar SOI Transistors with Thin Buried Oxide	R. Yan et al , Tyndall	2	IEEE Trans. on Electron Devices	Vol. 57, no 6	2010	1319-1326	10.1109/TED.2010.2046097
41	Variable temperature characterization of low-dimensional effects in tri-gate SOI MOSFETs	C. Barrette et al, Tyndall	2	Solid-State Electronics	Vol. 54	2010	1273–1277	doi:10.1016/j.sse.2010.05.035
42	Junctionless 6T SRAM cell	JP Colinge, Tyndall	2	Electronics Letters	Vol. 46, No. 22	2010	1491–1492	10.1049/el.2010.2736
43	Improvement of carrier ballisticity in junctionless nanowire transistors	N.D.Akhavan et al, Tyndall	2	Applied Phys. Letters	Vol. 98	2011	103510.1-3	doi:10.1063/1.3559625
44	A systematic study of „NH4…2S passivation „22%, 10%, 5%, or 1% on the interface properties of the Al2O3 / In0.53Ga0.47As/InP system for n-type and p-type In0.53Ga0.47As epitaxial layers	Eamon O'Connor Tyndall-UCC	1.3	Journal of Applied Physics	109	2011	pp. 024101-1 to 024101-10	10.1063/1.3533959
45	Compact capacitance modeling of a 3-terminal FET at zero drain-source voltage	B. Iñiguez, O. Moldovan URV	4	Solid-State Electronics	vol 54	2010	pp. 520-523	10.1016/j.sse.2009.12.039
46	High-frequency compact analytical noise model of gate-all-around MOSFETs	A. Lázaro, et al URV	2, 4	Semiconductor Science & Technology	Vol. 25 (3)	2010	pp. 035015 (1-10)	10.1088/0268-1242/25/3/035015
47	Analytical Modeling of the Gate Tunneling Leakage for the Determination of Adequate High-K Dielectrics in 22 nm Double-Gate SOI MOSFETs	G. Darbandy et al URV, Cinestav, Mexico	1, 4	Solid-State Electronics	Vol 54 (10)	2010	pp. 1083-1087	10.1016/j.sse.2010.06.015
48	Compact model for long-channel cylindrical surrounding-gate MOSFETs valid from low to high doping concentrations	M. Cheralathan, et al URV, Mexico	2, 4	Solid-State Electronics	Vol. 55 (1)	2011	pp. 13-18	10.1016/j.sse.2010.08.015
49	An analytical model for square GAA MOSFETs including quantum effects	E. Moreno, et al UGR	4	Solid State Electronics	Vol. 54	2010	1463-1469	10.1016/j.sse.2010.05.032
50	Hole transport in DGSOI devices: Orientation and silicon thickness effects	L. Donetti et al UGR	4, 1	Solid State Electronics	Vol 54	2010	191-195	10.1016/j.sse.2009.12.018
51	An in-depth simulation study of Coulomb mobility in ultra-thin-body SOI MOSFETs	F Jimenez-Molinos, et al UGR	4	Semiconductor Science and technology	Vol 25	2010	055002 (8pp)	10.1088/0268-1242/25/5/055002
52	A Model of the Gate Capacitance of Surrounding Gate Transistors: Comparison With Double-Gate MOSFETs	F. Ruiz, et al UGR	4, 1	IEEE Transaction on Electron Devices		2010		10.1109/TED.2010.2058630
53	An Analytical I–V Model for Surrounding-Gate Transistors That Includes Quantum and Velocity Overshoot Effects	J. B. Roldán, et al. UGR	4	IEEE Trans. on Electron Devices	Vol57	2010	2925-2933	10.1109/TED.2010.2067217
54	Simulation of the electrostatic and transport properties of 3D-stacked GAA silicon nanowire FETs	F.G. Ruiz et al UGR	4	Solid State Electronics	Vol 59	2011	62-69	doi:10.1016/j.sse.2011.01.005
55	Multiparameter admittance spectroscopy as a diagnostic tool for interface states at oxide/semiconductor interfaces	B. Raeissi Chalmers	1.3	IEEE Trans. Electron Dev.	35	2010	1702 - 1705	10.1109/TED.2010.2049064
56	Multiparameter admittance spectroscopy	O, Engstrom, et al Chalmers	1.3	ECS Transactions	35(3)	2010	257-	10.1109/TED.2010.2049064
57	Characterization of traps in the transition region at the HfO2/SiOx interface by thermally stimulated currents	B. Raeissi Chalmers	1.3	J. Electrochem. Soc.	158(3)	2011	G63 – G70	10.1149/1.3530845
58	Suppression of gate-induced drain leakage by optimization of junction profiles in 22 nm and 32 nm SOI nFETs	Andreas Schenk ETHZ	4	Solid-State Electronics	No 54	2010	pp. 115 - 122	doi:10.1016/j.sse.2009.12.005.
59	Linearity and mobility degradation in strained Si MOSFETs with thin gate dielectrics	OM Alatise, et al, UNEW	1, 4	Solid State Electronics	vol. 54, no. 6,	2010	pp. 628-634,	10.1016/j.sse.2009.12.036
60	The impact of self-heating and SiGe strain-relaxed buffer thickness on the analog performance of strained Si nMOSFETs	OM Alatise et al. UNEW	1, 4	Solid State ectronics	vol. 54, no. 3,	2010	pp. 327-335	10.1016/j.sse.2009.09.029
61	Statistical-Variability Compact-Modeling Strategies for BSIM4 and PSP	B. Cheng et al, GU	4	IEEE Design & Test of Computers	March Vol. 27, No.2	2010	26-35	10.1109/MDT.2010.53
62	Surface-energy triggered phase formation and epitaxy in nanometer-thick Ni1-xPtx silicide films	J. Luo, et al KTH	1	Applied Physics Letters	96	2010	0319111-3	10.1063/1.3291679
63	Interaction of NiSi with dopants for metallic source/dran	J. Luo, et al.	1	Journal of	B28	2010	C1 1-11	10.1116/1.32482

	applications	KTH		Vaccum Science Technology				67
64	Analytical modeling of direct tunneling current through gate stacks for the determination of suitable high-k dielectrics for nanoscale double-gate MOSFETs	G. Darbandy, URV, Mexico	1, 4	Semiconductor Science and Technology	Vol. 26 (4)	2011		10.1088/0268-1242/26/4/045002
65	Simulation study of the on-current improvements in Ge and sGe versus Si and sSi nano-MOSFETs	F. Conzatti et al IUNET	4	IEDM	Dec.	2010		
66	Full band assessment of phonon-limited mobility in Graphene NanoRibbons	A. Betti, et al IUNET Pisa	4, 2	Proceeding of the IEDM Tech. Dig.		2010	32.2.1-4	
ACCEPTED PAPERS – IN PRESS								
1	Effect of Ge/Si (001) epilayer thickness on structural quality	V.A. Shah, et al Warwick	1	Thin Solid Films		Acc. In 2010		
2	High quality relaxed Ge layers grown directly on a Si (001) substrate	V.A. Shah, et al Warwick	1	Solid State Electronics		Acc. in 2010		
3	CMOS Inverter based on Schottky Source-Drain MOS Technology with Low Temperature Dopant Segregation	G. Larrieu, E. Dubois (ISEN-IEMN)	1.2	IEEE Electron Dev. Lett.		2011	Accept.	
4	Improvement of immunity on MeV electron radiation of MOS structures by means of ultra-shallow fluorine implantation	M. Kalisz (WUT)	4	Microelectronics Reliability	accepted	2011		
5	Local strained silicon platform based on differential SiGe/Si epitaxy	A. Karmous, USTUTT	2.4	J. of Crystal Growth		2011		
6	Electron states in MOS system	O. Engström Chalmers	1.3	ECS Transaction 2011		2011		
7	Computational Comparison of Conductivity and Mobility Models for Silicon Nanowire Devices	Martin Frey ETHZ	4	Jour. Appl. Phys.	109 (7), Apr.2011	2011		
8	Study of interfaces and band offsets in TiN/amorphous $LaLuO_3$ gate stacks'	I.Z. Mitrovic LIVUNI	1.3	Microelectron. Engineering	April 2011	2011	In print	

A2.5. Presentation at the Conferences and Workshops (joint): 5 + 52

NO.	Type of activities	Main leader/ author Partners involved	Title of event	Title of paper/presentation/etc. Emphasize if invited	WP/ FP	Date	Place
1	Worskhop	INPG/FMNT, NCSR	Euro Nano Day	**Invited,** European Nanoelectronics: the Initiatives and Networks of the Academic Community	1-4	May 2010	Grenoble, France
2	Conference	T. Rudenko et al. ISP-Kiev, UCL	SemOI conference	**Invited:** Special Features of back-gate the back gate effect in ultra-thin body SOI MOSFETs	4	Oct 25-28, 2010	Kiev, Ukraine
3	Conference	Afzalian et al. UCL, Tyndall	SemOI conference	**Invited:** Barrier Resonant Tunneling Transistor: Performance investigation of a Steep Slope, High On-Current device	4	Oct 25-28, 2010	Kiev, Ukraine
4	Conference	O. Engström Chalmers/ITE	INFOS 2011	**Invited:**Future high-k gate stacks: Report from a tour in the periodic system (Tutorial to be given)	1.3	June 2011	Grenoble
5	Workshop	INPG/FMNT, Warwick, AMO Gmbh, RWTH Aachen, KTH, IUNET, UCL	INC6	**Invited:** NANOSIL FP7 European Network of Excellence	1-4	May 2010	Grenoble, France
1	Conference	INPG/FMNT, IMEC	ESSDERC'2010	Experimental Analysis of Surface Roughness Scattering in FinFET devices, pp 305-308	4	September 2010,	Sevilla, Spain
2	Conference	L. Donetti, et al Granada, Warwick, KTH	ULIS 2011	On the effective mass of holes in inversion layers	1	Mar 14-16, 2011	Cork, Ireland
3	Conference	E. Simoen, et al Warwick, IMEC	10th Int. Conf. on Solid-State and Integrated Circuit Technology (IC-SICT 2010)	Low-frequency noise in strained and relaxed Ge pMOSFETs, p891	1	Nov 1-4, (2010)	Shanghai, China
4	Conference	J. Mitard, et al Warwick, IMEC	2010 Int. Conf. on Solid State Devices and Materials (SSDM 2010)	High Hole-Mobility 65nm Biaxially-Strained Ge-pFETs: Fabrication, Analysis and Optimization, p. C-9-2	1	22-24 Sept (2010)	Tokyo, Japan
5	Conference	S.M.Thomas, et al Warwick, Glasgow,	ULIS 2010	Low temperature effective mobility measurements and modelling of high-k gated Si n-MOS and p-MOS	1	17-19 March 2010	Glasgow, UK

		NXP		devices			
6	Conference	Afzalian et al. UCL, Tyndall	EUROSOI Conference	Variable Barrier Resonant Tunneling Transistor: A New Path Towards Steep Slope and High On-Current?	4	25-27 January, 2010	Grenoble, France
7	Conference	Vikram Passi et al UCL, IEMN, LITEN-CEA	Electrochemical Society Conference - 2011	Functionalization of Silicon Nanowires for Specific Sensing	2	1-May-2011 – 5-May-2011	Montreal, Canada
8	Conference	V. Kilchytska et al. UCL, IMEC	EuroSOI 2010	Gate-edge charges related effects and performance degradation in advanced multiple-gate MOSFETs	4	January 2010	Grenoble, France
9	Conference	M.K.Md Arshad et al. UCL, Leti	ULIS 2010	Improved DIBL in Ultra Thin Body SOI MOSFETs with Ultra Thin Buried Oxide and Inverted Substrate	4	March 2010	Glasgow, UK
10	Conference	V. Kilchytska et al. UCL, IMEC	ESREF 2010	High-energy neutrons effect on strained and non-strained SOI MuGFETs and planar MOSFETs	4	October 2010	Gaeta, Italy
11	Conference	V. Kilchytska et al. UCL, Leti, UNEW	EuroSOI 2011	Ultra-thin body and BOX SOI Analog Figures of Merit	4	January 2011	Granada, Spain
12	Conference	T. Rudenko et al. UCL, ISP-Kiev	EuroSOI 2011	Impact of mobility variation on threshold voltage extraction by transconductance change and gm/Id methods in advanced SOI MOSFETs	4	January 2011	Granada, Spain
13	Conference	V. Kilchytska et al. UCL,Leti	ULIS 2011	High-temperature perspectives of UTB SOI MOSFETs	4	March 2011	Cork, Irland
14	Conference	T. Rudenko et al. UCL, ISP-Kiev	ULIS 2011	Influence of Drain Voltage on MOSFET Threshold Voltage Determination by Transconductance Change and gm/Id Methods	4	March 2011	Cork, Irland
15	Conference	S. Makoveev et al. UNEW, UCL, Leti	ULIS 2011	Self-Heating and Substrate Effects in Ultra-Thin Body Ultra-Thin BOX Devices	4	January 2011	Cork, Irland
16	Conference	V. Passi et al. UCL,ISEN-IEMN	Micro Electro Mechanical Systems Conf., MEMS'2010	Backgate bias and stress level impact on giant piezoresistance effect in thin silicon films and nanowires'	2.1	2010	Hong-Kong
17	Conference	F.M. Bufler, Synopsys, ETHZ, UPS, IUNET	14th International Workshop on Computational Electronics (IWCE 2010)	Comparison of semiclassical transport formulations including quantum corrections for advanced devices with high-k gate stacks, Proc.: p.319-322	4	27-29 October 2010	Pisa, Italy
18	Conference	Turchanikov, V., et al. IMEL, ISP-Kiev	27th International Conference on Microelectronics, MIEL 2010 - Proceedings	"Comparative studies of single- and double-nanocrystal layer NVM structures: Charge accumulation and retention", pp. 103-104	2.2	2010	Nis, Serbia
19	Conference	JP Raskin, UCL, Tyndall	IEEE International SOI Conference	Mobility Improvement in Nanowire Junctionless Transistors by Uniaxial Strain	2	Oct 2010	USA
20	Conference	A. Nazarov, ISP-Ukraine, Tyndall	EUROSOI 2011	Extraction of flat-band voltage and parasitic resistance in junctionless MuGFETs	2	Jan 2011	Spain
21	Conference	Yuri Y. Gomeniuk ISP Kiev, Tyndall-UCC	INFOS 2011	Transport and Interface States in High-k LaSiOx Dielectric	1.3	21 June 2011	Grenoble
22	Conference	Yuri Y. Gomeniuk ISP –Kiev, Tyndall-UCC, KTH, AMO,FZJ	6th SemOI Conference and 1st Ukrainian-French Seminar	Electrical properties of high-k LaLuO3 gate oxide for SOI MOSFETs	1.3	24-26 October 2010	Kyiv
23	Conference	Yuri Y. Gomeniuk ISP-Kiev, Tyndall-UCC, AMO, FZJ, Chalmers	ECS-218 (2010)	Electrical Properties of LaLuO3/Si(100) Structures Prepared by Molecular Beam Deposition	1.3	13 October 2010	Las Vegas
24	Conference	Tyndall-UCC, AMO, Jülich	WoDiM 2010	The onset of electrical stress in 3nm and 6nm molecular beam deposited LaLuO3 MOSCAPs on n-Si(100) substrates using a TiN metal gate and an Al back contact	1.3	28-30th June 2010	Bratislava, Slovakia
25	Conference	M. Balaguer, et al, URV, UGR	EUROSOI	An analytical compact model for Schottky-Barrier Double Gate MOSFETs	1, 4	January 2010	Grenoble (France)
26	Conference	R. Ritzenthaler, et al. URV, CEA/Leti, INPG	EUROSOI	A 2D analytical model of threshold voltage for Pi-gate FinFET transistors	4	January 2010	Grenoble (France)
27	Conference	R. Ritzenthaler, et al. URV, CEA/Let, INPG	40th European Solid-State Device Research conference (ESSDERC)	3D Analytical Modelling of Subthreshold Characteristics in Pi-gate FinFET Transistors	4	September 2010	Sevilla (Spain)
28	Conference	R. Ritzenthaler et al. URV, CEA/Let, INPG	IEEE International SOI conference	Parasitic Back-Inferface Conduction in Planar and Triple-Gate SOI Transistors	4	2010	San Diego (USA)
29	Conference	R. Ritzenthaler, et al URV, CEA/Let, INPG	EUROSOI	A Short-Channel Analytical Model for Triple-gate and Planar FDSOI Transistors	4	2011	Granada (Spain)

30	Conference	M. Cheralathan, et al URV, UGR	EUROSOI	A Compact Double-Gate MOSFET Model Consistent with a MultiSubband Ensemble Monte Carlo Model	4	2011	Granada (Spain)
31	Conference	M. Cheralathan,et al URV, UGR, IUNET	ULIS	Analytical Drain Current Model Reproducing Advanced Transport Models in nanoscale Double-Gate (DG) MOSFETs	4	2011	Cork (Ireland)
32	Conference	B. Raeissi, Chalmers, ITE, AMO, FZ Julich	16th Workshop on Dielectrics in Microelectronics (Wodim)	Interface state properties of high-k/SiOx/Si interfaces portrayed by multiparameter admittance spectroscopy	1.3	June 28 – 30, 2010	Bratislava
33	Conference	O. Engström Chalmers, INPG, FZJ, AMO	16th Workshop on Dielectrics in Microelectronics (Wodim)	Capture cross sections for holes at LaLuO/Si interfaces	1.3	June 28 – 30, 2010	Bratislava
34	Conference	I.Z. Mitrovic et al LIVUNI, Julich	INFOS'2011	Study of interfaces and band offsets in TiN/amorphous $LaLuO_3$ gate stacks'	1.3	21-24 June 2011	Grenoble, France
35	Conference	N. Sedghi et al LIVUNI, Julich	219th ECS Meeting	Investigation of Electron and Hole Charge Trapping in $LaLuO_3$ Stack MOS Capacitor Using the 3-Pulse CV Technique	1.3	1-6 May 2011	Montreal, Canada
36	Workshop	N. Sedghi et al LIVUNI, Julich	Wodim 2010	CV Measurements on $LaLuO_3$ Stack MOS Capacitor Using a New 3-Pulse Technique	1.3	28-30 June 2010	Bratislava, Slovakia
37	Conference	N. Sedghi/ LIVUNI, Julich	41st IEEE SISC 2010	Charge Trapping in $LaLuO_3$ MOS Capacitors using a New 3-Pulse CV Technique	1.3	December 2010	San Diego, USA
38	Conference	S Makovejev, et al UNEW, UCL	SiRF	RF extraction of self-heating effects in FinFETs of various geometries	4	January 2011	Phoenix ,USA
39	Conference	S Makovejev, et al UNEW, UCL	ULIS	Self-heating effect characterisation in SOI FinFETs	4	March 2010	Glasgow, UK
40	Conference	E Escobedo-Cousin et al UNEW, UCL	MRS	Characterizing the effect of uniaxial strain on the surface roughness of Si nanowire MEMS-based microstructures	1, 2, 4	November 2010	Boston, USA
41	conference	E. Sangiorgi et al. IUNET, WUT, GU, UPS,	MIEL conference	Drain Current Computation in Nanoscale nMOSFETs: Comparison of Transport Models	4	May 2010	Serbia
42	Conference	V.Gudmundssonet al. IUNET-Udine and KTH	International Conference on Ultimate Integration	Multi-subband Monte Carlo simulation of fully-depleted silicon-on-insulator Schottky barrier MOSFETs	4, 1	March 2010	UK
43	Conference	M. Schmidt, et al AMO, RWTH	11th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)	Mobility Extraction in sub 10nm Nanowire nMOSFETs with Gadolinium-Silicate as Gate Dielectric	1.3, 2.1	Feb. 2011	USA
44	Conference	J. Jasiński (WUT, FZJ)	10th ELTE Conference 2010	Influence of annealing temperature on MOSCAPs with LaLuO gate oxide	1.3	2010	Poland
45	Conference	M. Iwanowicz (WUT, AMO)	10th ELTE Conference 2010	Studies of the quality of GdSiO-Si interface	1.3	2010	Poland
46	Conference	I. Ben-Akkez et al INPG, ST, CEA/Let	ULIS	Characterization and modeling of capacitances in FD-SOI devices	4	2011	Irland
47	Conference	A.Nazarov et al Tyndall-UCC, ISP-Kiev	ULIS	Extraction of channel mobility in nanowires MOSFETs using Id(Vg) characteristics	2, 4	2011	Irland
48	Conference	Q. Rafhay, et al. INPG, Cea/Leti	ULIS	Revised approach for the characterization of GIDL	4	2011	Irland
49	Conference	M. Schmidt, et al FZJ, CEA/Let	ULIS	Impact of strain and Ge concentration on the performance of planar SiGe band-to-band tunneling transistors	1	2011	Irland
50	Conference	A. Hubert et al INPG, Leti	ESSDERC	Experimental comparison of programming mechanisms in 1T-DRAM	4	2010	Spain
51	Conference	K. Tachi et al INPG/FMNT, CEA/Leti, ST,	ESSDERC'2010	SD Source/Drain doping optimization in multi-channel MOSFET	4	13-17 September 2010,	Sevilla, Spain
52	Conference	N. Rodrigez, et al. INPG/FMNT, UGR	ESSDERC'2010	Origins of universal mobility violation in SOI MOSFETs	4	13-17 Sept. 2010	Sevilla, Spain

A2.6. Presentation at the Conferences and Workshops (single-partner): 27+81

NO.	Type of activities	Main leader/ author Partners involved	Title of event	Title of paper/presentation/etc. Emphasize if invited	WP/ FP	Date	Place
1	Conference	INPG/FMNT	French−Ukrainian symposium and SemOI conference	**Invited:** Elastic and inelastic scattering in SiNWs	2.4, 4	October 2010	Kiev, Ukraine
2	Workshop	INPG/FMNT	Nanosil SiNano Workshop	**Invited:** Nanowires in the Beyond CMOS and More than Moore perspectives: Electro-mechanical properties	2, 4	17 Sept. 2010	Sevilla, Spain
3	Workshop	INPG/FMNT	Minatec Crossroads	**Invited:** European Research Roadmap for Nanoelectronics	1-4	June 2010	Grenoble, France
4	Conference	INPG/FMNT	6th International SemOI Conference & 1st Ukrainian-French Seminar on SOI	**Invited:** Silicon-based devices and materials for nanoscale FETs	1, 2, 4	October 2010	Kiev, Ukrainia
5	Conference	INPG/FMNT	4th International Conference on Micro-Nanoelectronics, Nanotechnologies & MEMs	**Invited:** The Sinano Institute: European Networks and Projects in the fields of More Moore, More than Moore and Beyond-CMOS	1-4	December 2010	Athens, Greece
6	Invited talk	KTH	27th International Conference on Microelectronics (MIEL)	**Invited:** Nanoscaling of MOSFETs and Implementation of Schottky Barrier S/D contacts	1, 3	16-19 May 2010	NIS, Serbia
7	Invited talk	KTH	18th International Conference on Advanced Semiconductor Devices and Microssystems (ASDAM)	**Invited:** Nanoscaled SiGe based MOSFETs	1, 3	2010	Smolenice, Slovakia
8	Invited talk	KTH	10th IEEE International Conference on Solid-State and Integrated Circuit Technology	**Invited:** Integration of metallic source/drain (MSD) contacts in nanoscaled CMOS technology	1, 3	2010	Shanghai
9	Conference	G. Iannaccone IUNET	European Conference on Nanotechnologies	**Invited:** Graphene as a material for nanoelectronics (invited - ab #1198	2, 4	26 April 2010	Vancouver
10	Conference	G.Iannaccone IUNET	SISPAD	**Invited:** Transport and noise properties of graphene-based transistors revealed through atomistic modelling)	2, 4	6 September 2010	Bologna
11	Conference	V. Kilchytska et al. UCL	SemOI conference	**Invited:** Effects of high–energy neutrons on advanced SOI MOSFETs	4	Oct 25-28, 2010	Kiev, Ukraine
12	Conference	P. Dollfus, UPS	1st Ukrainian-French Seminar on SOI materials, devices and cicuits	**Invited:** Ohmic and Schottky contact CNTFET: Transport properties and device performance using semi-classical and quantum particle simulation	2.2, 4	24-28 October 2010	Kiev, Ukrainia
13	Conference	P. Dollfus, UPS	14th International Workshop on Computational Electronics (IWCE 2010)	**Invited:** Quantum transport of Dirac fermions in graphene nanostructures, Proc.: p.39-44	2.2, 4	27-29 October 2010	Pisa, Italy
14	Invited lecture	FZJ/ Buca	Seminar Invitation	**Invited:** From Strained Si to strained Si on Insulator	1.1	08.Nov. 2010	Shanghai China
15	Invited lecture	FZJ/ Mantl	Conference	**Invited:** High mobility Si-Ge channel and high-k materials for NanoMOSFETs	1, 3	24-May 2010	Stockholm/ Sweden
16	Invited lecture	FZJ/ Mantl	Nanosil Workshop		1, 3	13.09. 2010	Seville, Spain
17	Conference	A. G. Nassiopoulou, IMEL	International Conference on Nanomaterials (ICN 2010)	**Invited:** "Nanostructures on Si by Electrochemistry and their Applications"	2	27-29 April 2010	Kottayam, India
18	Conference	A. G. Nassiopoulou, IMEL	7th International Conference on Porous Semiconductors Science and Technology – PSST 2010	**Tutorial:** "Porous Si for Electronics and Sensors"	2.2	14-19 March 2010	Valencia, Spain
19	Conference	A. G. Nassiopoulou, IMEL	VCIAN Conference on Interactions Among Nanostructures 2010	**Invited:** "Photoluminescence from silicon nanocrystal ensembles: effect of exciton migration and role of surface vibration modes"	2.2	21-25 June 2010	Santorini, Greece
20	Conference	JP Colinge, Tyndall	6th International SemOI Workshop on Nanoscaled Semiconductor-on-Insulator Materials, Sensors an Devices	**Invited:** Junctionless transistors: physics and properties	2	Nov. 2010	Ukraine
21	lecture	R. Mroczyński WUT	12th Polish Seminar "Ion techniques"	**Invited:** Plasma techniques applications in the technology of non-volatile semiconductor memory (NVSM) devices	1.3	2-5 March 2011	Szklarska Poręba,

							Poland
22	lecture	R. Mroczyński WUT	XII Warsaw Festival of Science	**Invited:** How the integrated circuit is made…?	1	September 2010	Warsaw
23	Tutorial Course	B. Iñiguez URV	ESSDERC	**Invited:** Compact Thin-Film SOI MOSFET Modelling	1, 2, 4,	2010	Sevilla (Spain)
24	Tutorial Course	B. Iñiguez URV	TCCM	**Invited:** Compact Small-Signal FET Modelling	4	2010	Tarragona (Spain)
25	Conference	O. Engström Chalmers	219 ECS Meeting	**Invited:** Electron states in MOS system (to be presented)	1.3	May 1 – 6, 2011	Montreal
26	Conference	O, Engstrom Chalmers	218 ECS Meeting,	**Invited:** Multiparameter Admittance Sepctroscopy	1.3	Oct. 10 – 15, 2010	Las Vegas
27	Invited lecture	FZJ/ Mantl	International Symposium on Integrated Functionalities	**Invited:** Ternary high-k oxides for nanoscale logic devices	1, 3	13.06. 2010	Puerto Rico
1	Conference	M. Myronov, et al Warwick,	14th International Conference on Vapor Growth and Epitaxy (ICVGE-14)	Monolayer thickness control during epitaxial growth of high Ge content strained Ge/SiGe multilayers by RP-CVD	1	August 8-13, 2010	Beijing, China
2	Conference	Van Huy Nguyen, et al Warwick,	UK Semiconductors,	Defect Evaluation in Ge and $Si_{1-x}Ge_x$ Epitaxial Layers using an Iodine-Based Selective Etchant	1	July 7-8 (2010)	Sheffield, UK
3	Conference	A. Dobbie, et al Warwick,	UK Semiconductors,	Thermal Stability of Strained Ge Layers Grown on Reverse-Graded $Si_{0.2}Ge_{0.8}$ Relaxed Buffers by RP-CVD	1	July 7-8 (2010)	Sheffield, UK
4	Conference	V.A. Shah et al. Warwick,	UK Semiconductors,	Thickness studies of high quality Ge layers on Si (001) substrates.	1	July 7-8 (2010)	Sheffield, UK
5	Conference	Xue-Chao Liu, et al Warwick,	UK Semiconductors,	Growth and characterization of $Ge/Si_{0.4}Ge_{0.6}$ multiple quantum wells	1	July 7-8 (2010)	Sheffield, UK
6	Conference	A. Dobbie, et al Warwick,	E-MRS 2010 Spring Meeting	Relaxation of Strained Germanium Layers Grown on $Si_{0.2}Ge_{0.8}$ Relaxed Buffers by RP-CVD with in-situ H_2 Annealing	1	June 7-11, 2010	Strasbourg, France
7	Conference	M. Myronov, et al. Warwick,	E-MRS 2010 Spring Meeting	Epitaxial growth of Ge layers by RP-CVD using Digermane precursor	1	June 7-11, 2010	Strasbourg, France
8	Conference	M. Myronov et al. Warwick,	E-MRS 2010 Spring Meeting	Highly strained Si epilayers grown on SiGe/Si(100) virtual substrates by RP-CVD	1	June 7-11, 2010	Strasbourg, France
9	Conference	V.A. Shah, Warwick,	ISTDM 2010	High quality relaxed Ge layers grown directly on a Si (001) substrate.	1	24-26 May 2010	Stockholm, Sweden
10	Conference	Xue-Chao Liu et al Warwick,	ISTDM 2010	Non-destructive thickness characterization of Si and Ge based heterostructure by x-ray diffraction and reflectivity	1	24-26 May 2010	Stockholm, Sweden
11	Conference	A. Dobbie et al Warwick,	MRS Spring Meeting	Investigation of the Thermal Stability of Strained Ge Layers by Reduced-Pressure Chemical Vapour Deposition on Relaxed $Si_{0.2}Ge_{0.8}$ Buffers	1	April 5-9 2010	San Francisco, USA
12	Conference	G. Iannaccone IUNET	International Workshop on Computational Electronics	A multi-scale approach for performance assessment of hydrogenated graphene Field-Effect Transistors	2, 4	28 October 2010	Pisa
13	Conference	A. Betti IUNET	International Workshop on Computational Electronics	Enhanced shot noise in carbon nanotube FETs due to electron-hole interaction	2, 4	28 october 2010	Pisa
14	Conference	V.Bonfiglio IUNET	International Workshop on Computational Electronics	Evaluation of threshold voltage dispersion in 45 nm CMOS technology with TCAD-based sensitivity analysis	4	27 october 2010	Pisa
15	Conference	A. Betti IUNET	IEDM 2010	Full band assessment of phonon-limited mobility in Graphene NanoRibbons,	2, 4	december 2010	San Francisco
16	Conference	Afzalian et al. UCL	ESSDERC	Breaching the kT/Q Limit with Dopant Segregated Schottky Barrier Resonant Tunneling MOSFETs: a Computationnal Study	4	Sept. 13-17 2010	Sevilla, Spain
17	Conference	J. Conde at al. UCL,Cinestav-Mexico	MIEL 2010	3D Simulation of Triple-Gate MOSFETs	4	May 2010	Nis, Serbia
18	Conference	I. Garduno et al, UCL, Cinestav-Mexico	MIEL 2010	Modeling of main leakage currents and their contribution to channel current in Fin-FETs	4	May 2010	Nis, Serbia
19	Conference	X.L. Han et al.	European Material Research	Fabrication and electrical characterization of dense	2.1	June	Strasbo

		ISEN-IEMN	Society Spring Meeting	vertical Si nanowires arrays		2010	urg France
20	Conference	X.L. Han ISEN-IEMN	36th International Conference on Micro & Nano Engineering (MNE2010)	Realization of ultra dense arrays of vertical silicon NWs with defect free surface and perfect anisotropy using a top-down approach	2.1	19-22 Sept 2010	Genoa Italy
21	Conference	V. Talbo, UPS	14th International Workshop on Computational Electronics (IWCE 2010)	Fully self-consistent simulation of silicon nanocrystal-based single-electron transistors, Proc.: p. 151-154	2.4	27-29 October 2010	Pisa, Italy
22	Conference	V. Hung Nguyen, UPS	15th International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)	Quantum transport of Dirac fermions in graphene field effect transistors, Proc.: p. 9-12	2.2	6-8 Septem ber 2010	Bologna , Italy
23	Conference	M. Schmidt, et al AMO	Ultimate Integration on Silicon (ULIS)	Mobility Extraction in sub 10nm Nanowire nMOSFETs with Gadolinium-Silicate as Gate Dielectric	1.3, 2.1	16 March 2011	Cork, Ireland
24	Conference	A. Karmous, USTUTT	Ultimate Integration on Si ULIS2011	Ge Quantum Dot Schottky diode operated in a 89GHz Rectenna / Poster / Proc. pp. 74-76	2.4	March 2011	Cork, Ireland
25	Workshop	E. Kasper, USTUTT	NANOSIL-Workshop Beyond-CMOS	Quantum Structures beyond CMOS / Presentation	2	Februar y 2011	Aachen, German y
26	Conference	H. Xu, USTUTT	The Eleventh Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, SiRF 2011	Integrated W-Band RECTENNA (Rectifying Antenna) with Ge Quantum Dot Schottky Diode/ Presentation	2.4	17-19 January 2011	Phoenix , Arizona, USA
27	Workshop	E. Kasper, USTUTT	5th International WorkShop on New Group IV Semiconductor Nanoelectronics	High frequency behaviour of Ge pin junctions / Presentation / Digest of Papers (2010)1-3.	2	29-30 January 2010	Sendai, Japan
28	Conference	S. Gardelis and A. G. Nassiopoulou, IMEL	7th International Conference on Porous Semiconductors Science and Technology – PSST 2010	Colleration of light emission properties with exciton migration in silicon nanocrystal ensembles	2.2	14-19 March 2010	Valenci a, Spain
29	Conference	JP Colinge, Tyndall	EUROSOI Conference	Substrate bias effects in MuGFETs	2	Jan. 2011	Grenob le
30	Conference	JP Colinge, Tyndall	EUROSOI Conference	3D Simulation of RTS Amplitude in Accumulation-Mode and Inversion-Mode Trigate SOI MOSFETs	2, 4	Jan. 2011	Grenob le
31	Conference	JP Colinge, Tyndall	EUROSOI Conference	Comparison of Breakdown Voltage in Bulk and SOI FinFETs	2, 4	Jan. 2010	Grenob le
32	Conference	JP Colinge, Tyndall	WOLTE 9 - Ninth International Workshop on Low Temperature Electronics	Low Temperature Behavior of Junctionless Multiple Gate nMOSFETs	2, 4	Aug 2010	Brazil
33	Conference	JP Colinge, Tyndall	ESSDERC	Junctionless Nanowire Transistor (JNT): Properties and Design Guidelines	2	Sept 2010	Spain
34	Conference	JP Colinge, Tyndall	Solid-State Devices and Materials Conference (SSDM)	Analysis of the Junctionless Transistor Architecture	2	Sept 2010	Japan
35	Conference	JP Colinge, Tyndall	Solid-State Devices and Materials Conference (SSDM)	Short-Channel Junctionless Nanowire Transistors	2	Sept 2010	Japan
36	Conference	JP Colinge, Tyndall	EUROSOI 2011	Comparison of the switching speed in junctionless and accumulation-mode gate-all-around nanowire transistors	2	Jan 2011	Spain
37	Conference	R. T. Doria, USP-Brazil, Tyndall	EUROSOI 2011	Analytical Model for the Threshold Voltage of Junctionless Nanowire Transistors	2, 4	Jan 2011	Spain
38	Conference	JP Colinge, Tyndall	ULIS 2011	Performance Investigation of Short-channel Junctionless Multigate Transistors	2	March 2011	Ireland
39	Conference	Tyndall-UCC	INFOS 2011	Investigation of bulk defects in amorphous and crystalline HfO2 thin films	1.3	21 June 2011	Grenobl e
40	Conference	G. Darbandy, et al, URV	EUROSOI	Analytical Modeling of Direct Tunnelling Current through SiO2/high-k Gate Stacks for the Determination of Suitable High-k Dielectrics for Nanoscale Double-Gate MOSFETs	1, 4	January 2010	Grenobl e (France)
41	Conference	M. Cheralathan, et al URV	ULIS	Compact potential and current model for long-channel doped cylindrical surrounding-gate MOSFETs	2, 4	March 2010	Glasgo w (UK)
42	Conference	M. Schwarz, et al URV	ULIS	2D closed-form model for the source/drain orthogonal electric field in lightly-doped Schottky-Barrier Double-Gate MOSFETs	1, 4	2010	Glasgo w (UK)
43	Conference	M. Schwarz, et al URV	ESSDERC Fringe Poster Session	2D Analytical Calculation of the Tunneling Current in Lightly Doped Schottky Barrier Double-Gate MOSFET	1, 4	2010	Sevilla (Spain)
44	Conference	M. Schwarz, et al URV	MIXDES	Analytical 2D Model for the Channel Electric Field in Undoped Schottky Barrier Double-Gate MOSFET	1, 4	2010	Wrocla w (Poland)

45	Conference	G. Darbandy, et al URV	EUROSOI	Study of Potential High-k Dielectrics for sub 15 nm UTB SOI MOSFETs, Using Analytical Models of the Gate Tunneling Leakage	1, 4	2011	Granada (Spain)
46	Conference	M. Schwarz, et al URV	EUROSOI	2D Analytical Calculation of the Current in Lightly Doped Schottky Barrier DG MOSFET	1, 4	2011	Granada (Spain)
47	Conference	T. Holtij,et al URV	ULIS	2D Analytical Calculation of the Source/Drain Access Resistance in DG-MOSFET Structures	4	2011	Cork (Ireland)
48	Conference	M. Schwarz, et al URV	ULIS	2D Analysis of Source/Drain Carrier Tunneling in Lightly Doped Schottky Barrier DG-MOSFETs Using a Fully Analytical Model	4	2011	Cork (Ireland)
49	Conference	UGR Jose Luis Padilla, Francisco Gamiz	ULIS-2010	Barrier lowering implementation in SB-MOSFETs on SOI substrates	1, 4	16-18 March	Glasgow
50	Conference	UGR Carlos Sampedro, Francisco Gamiz et al.	ULIS-2010	Channel Length impact on Velocity Overshoot in UTB-DGSOI	4	16-18 March	Glasgow
51	Conference	R Kapoor, et al UNEW	ESREF	Characterising gate dielectrics in high mobility devices using novel nanoscale techniques	1, 4	October 2010	Italy
52	conference	A. Asenov et al., GU	Custom Integrated Circuits Conference (CICC), 2010 IEEE	Modeling and Simulation of Transistor and Circuit Variability and Reliability	4	Sept. 2010	USA
53	Conference	A. Asenoc et al., GU	Design, Automation & Test in Europe Conference & Exhibition (DATE), 2010	Capturing Intrinsic Parameter Fluctuations using the PSP Compact Model	4	March 2010	Dresden
54	Conference	A. Paussa et al. IUNET-Udine	International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)	Pseudo-Spectral Method for the Modelling of Quantization Effects in Nanoscale MOS Transistors	4	March 2010	UK
55	Conference	P.Toniutti, et al IUNET-Udine	International Conference on Ultimate Integration on Silicon (ULIS)	Understanding the mobility reduction in MOSFETs featuring high-κ dielectrics	4	March 2010	UK
56	Conference	A. Betti, G. Fiori, G.Iannaccone - IUNET Pisa	IEDM Tech. Dig.	Full band assessment of phonon-limited mobility in Graphene NanoRibbons	4	Dec. 2010	USA
57	Conference	A. Betti G. Fiori, G. Iannaccone - IUNET Pisa	14th International Workshop on Computational Electronics, (IWCE 2010)	Enhanced shot noise in carbon nanotube FETs due to electron-hole interaction	4	Oct. 2010	Pisa, Italy
58	Conference	G. Giusi, G. Iannaccone, D. Maji, F. Crupi - IUNET Pisa	10th IEEE International Conference on Solid-State and Integrated Circuit Technology (CSICT-2010)	Experimental extraction of barrier lowering and backscattering in saturated short-channel MOSFETs	4	Nov. 2010	
59	Conference	G. Iannaccone, A. Betti, G. Fiori - IUNET Pisa	International Conference on Simulation of Semiconductor Processes and Devices, (SISPAD)	Transport and noise properties of graphene-based transistors revealed through atomistic modeling	2, 4	March 2010	Italy
60	Conference	G. Fiori, et al IUNET Pisa	14th International Workshop on Computational Electronics, (IWCE 2010)	A multi-scale approach for performance assessment of hydrogenated graphene Field-Effect Transistors	2, 4	Oct. 2010	Pisa, Italy
61	Conference	V. Bonfiglio, G. Iannaccone - IUNET Pisa	14th International Workshop on Computational Electronics, (IWCE 2010)	Evaluation of threshold voltage dispersion in 45 nm CMOS technology with TCAD-based sensitivity analysis	4	Oct. 2010	Pisa, Italy
62	Conference	L. Silvestri, et al IUNET-Bologna	International Conference on Ultimate Integration on Silicon (ULIS)	Mobility Model for Electrons and Holes in FinFETs with High-κ Stacks, Metal Gate and Stress	4	March 2010	UK
63	Conference	A.T. Pham, TUBS	IWCE	Simulation of Landau quantization effects due to strong magnetic fields in(110) Si hole inversion layers	4	Oct. 2010	Pisa, Italy
64	Conference	A.T. Pham, TUBS	ESSDERC	Comparison of Strained SiGe Heterostructure on Insulator (001) and (110) PMOSFETSs: C-V Characteristics, Mobility, and ON current	4	Sept. 2010	Spain
65	Conference	H. Xu, USTUTT	11th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)	Integrated W-band RECTENNA (rectifying antenna) with Ge quantum dot Schottky Diode	2.4	Feb. 2011	USA
66	Conference	M. Iwanowicz (WUT)	10th ELTE Conference 2010	Vector generator for pulse characterization of MOS devices	1.3	2010	Poland
67	Conference	J. Jasiński (WUT)	10th ELTE Conference 2010	Electrical characterization of MOSFETs with HfSiON gate	1.3	2010	Poland
68	Conference	R. Mroczyński (WUT)	WoDiM 2010	Reliability issues of double gate dielectric stacks based on hafnium dioxide (HfO_2) layers for non-volatile semiconductor memory (NVSM) applications	1.3	2010	Bratislava, Slovakia
69	Conference	M. Kalisz (WUT)	5th Wide Bandgap Materials -	Effect of the Fluorine Implantation from r.f. CF_4 plasma	1.3	2010	Poland

			progress in synthesis and applications and 7th Diamond & Related Films jointly with 2nd International Workshop on Science and Applications of Nanoscale Diamond Materials, Zakopane, Poland	on Electrical Characteristics of MIS Structures with PECVD Silicon Oxynitride Layers			
70	Conference	M. Kalisz (WUT)	10th Conference "Electron Technology", ELTE 2010, Wrocław, Poland	Improvement of immunity on MeV electron radiation of MOS structures by means of ultra-shallow fluorine implantation	1.3	2010	Poland
71	Conference	E. Gnani et al IUNET	ULIS 2011	Numerical Investigation on the Junctionless Nanowire FET	2, 4	2011	Irland
72	Conference	L. Knoll et al FZJ	ULIS 2011	20 nm gate length Schottky MOSFETs with ultra thin NiSi/epitaxial NiSi2 source/drain	1	2011	Irland
73	Conference	A. Martinez UG	ULIS	NEGF simulations of a junctionless Si gate-all-around nanowires transistor with discrete dopants	2, 4	2011	Irland
74	Conference	A. Kranti et al UCL	ULIS	Source/Drain engineering ultra low power analog/RF UTBB MOSFETs	4	2011	Irland
75	Conference	J. El Husseini et al URV, IES Monrpelllier	ULIS	A surface potential based compact model for lightly doped FD SOI MOSFETs with ultra-thin body	4	2011	Irland
76	Conference	A. Nichau et al FZJ	ULIS	Lanthanum Lutetium oxide integration in a gate-first process on SOI MOSFETs	1	2011	Irland
77	Conference	X. Wand, et al GU	ULIS	Channel length dependence of statistical threshold voltage variability in extremely scaled HKMG MOSFETs	4	2011	Irland
78	Conference	C. Sampedro et al UGR	ESSDERC	Multi-subband Monte Carlo Simulation of bulk MOSFETs for the 32nm-Node and beyond	4	2010	Spain
79	Conference	S.Narasimhamoorthy et al INPG/FMNT	ESSDERC'2010	Parameter extraction of nanoscale MOSFETs using modified Y function method	4	September 2010,	Sevilla, Spain
80	Conference	K. Boucart, et al. EPFL	ESSDERC'2010	A simulation-based study of sensitivity to parameter fluctuations of Si tunnel FETs	2, 4	September 2010,	Sevilla, Spain
81	Conference	S. Habicht, et al FZJ	ESSDERC'2010	Hole mobilities and electrical characteristics of omega-gated silicon nanowires array FETs with 110- and 100-channel orientation	2, 4	September 2010,	Sevilla, Spain

A2.7. Other dissemination actions (joint): 3

NO.	Type of activities	Main leader/ author Partners involved	Title of paper/presentation/etc.	WP/ FP	Date
1	Web site	Sinano Institute, -Grenoble INP, -UCL	Nanosil Project, regular update	All	2010-11
2	Film	Sinano Institute, Grenoble INP, KTH, IUNET, UCL	Sinano Institute	All	2011
3	News Letter	UCL, Sinano Institute, Grenoble INP, IEMN, FZJ, Warwik, KTH, USTUTT, AMO, RWTH, IUNET, Chalmers, EPFL	Nanosil News Letter 2009	All	2010

A2.8. Other dissemination actions (single-partner): 4

NO.	Type of activities	Main leader/ author Partners involved	Title of paper/presentation/etc. Emphasize if invited	WP/ FP	Date	Place
1	Thesis	N. Reckinger UCL	Fabrication and characterization of rare-earth silicide thin films	1.2	11.02. 2011	Louvain-la-Neuve
2	Thesis	B. Raeissi Chalmers	Charge carrier traffic at interfaces in nanoelectronic structures, ISSN 1652-0769, 2010	1.3	2010	
3	Thesis	ETHZ	Scattering in Nanoscale Devices	4	2010	Zurich
4	Thesis	ETHZ	Band Structure Effects and Quantum Transport	4	2010	Zurich