NANOSIL FINAL REPORT

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TABLE OF CONTENTS

4.1 Final publishable summary report

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- Logo:

4.1.1 Executive summary

- **Introduction**: The shrinking dimensions of electronic components will continue in the next two decades. In the sub-10nm range, "Beyond-CMOS" devices will certainly play an important role and could be integrated on CMOS platforms in order to pursue integration down to nm structures. The needed performance improvements for the end of the roadmap will lead to a substantial enlargement of the number of materials, technologies and device architectures. Therefore, new generations of Nanoelectronic ICs present increasingly formidable multidisciplinary challenges at the most fundamental level resulting in an urgent need of academic research, using joint flexible processing, characterization and modelling platforms. During Nanosil, close links with other European Projects, the ENIAC ETP, the AENEAS organization and National projects in the same fields have been established in order to enhance the overall efficiency of the European Research in Nanoelectronics. The interaction between the Scientific Community and the European Industry has also been strenghened. Many Nanosil Partners and Sinano Institute Members have contributed to the "Sinano Institute vision", driven by the European Academic Community, in order to determine the most promising research topics in the More Moore, More than Moore and Beyond CMOS Nanoelectronic domains. During the project, we have studied some of the main scientific and technical challenges put forward by the International ITRS Roadmap and European ENIAC Strategic Research Agenda. Some very important specific actions have also been launched for the strengthening of the durable integration of the NoE: i) seven new Partners became Members of the Sinano Institute in 2009, which is a legal entity (Scientific Association) created in January 2008 for the coordination of the European Academic Community working in the field of Nanoelectronics ; ii) the Joint Processing, Joint Characterization and Modelling Platforms, which have been developed and used in the framework of the Nanosil NoE for our joint research activities are now integrated as open Research Infrastructures in the Sinano Institute ; iii) Nanosil Partners and Sinano Institute Members have been strongly associated, as representatives of the academic community, to the new initiative launched in 2010 by STMicroelectronics called ENI2 (European Nanoelectronics Infrastructure for Innovation).; iv) a significant part of Nanosil Partners have launched a new FP7 complementary NoE, Nanofunction, and the FET Flagship "Guardian Angels" proposal that has been selected as a pilot project.

- **WP1:** Many of the aspirations coming out of the SiNANO NoE in terms of network interactions and technological advancements have been realized in NANOSIL, with a a new Flagship Project (FP) concept proved to be effective, and with good cross-FP interactions allowing the realisation of some very challenging device fabrication activity on the processing platform (via WP3). We were also able to very effectively engage related simulation work from WP4. At the onset we knew that the objectives of this WP were very ambitious and certainly world leading. The big results from WP1 include some very significant progress on the realisation of new 'platforms' for future CMOS, primarily based on Ge. Significantly enhanced device hole mobilities were realised, both on insulator (OI) and on new designs of virtual substrates. In the latter case we were able to access IMEC's world leading work on short channel Ge device process, together with the development an implant-free process that is yielding excellent short channel characteristics - initially on bulk Ge. Cumulative network activity strongly suggests that the (110) orientation is required to get the most out of strained Ge, but this has to be on a OI platform to achieve ultimate p-channel performance, and shows excellent prospects for the Ge n-channel. As channel lengths approach the 10 nm regime, contact resistance

looms as a major performance limiter, particularly so with the concurrent restrictions in thermal budgets imposed by the new channel and gate stack materials. Here we made some very significant advancements using dopant segregation (DS) to reduce Schottky barrier heights to acceptable levels (<0.1eV). DS processes were developed with temperatures generally <600ºC, primarily for Pt but also included the first study on Er, which produced the required dopant pile-up of either As (for n- channel) or B (for p-channel) close to the silicide/channel interface. Scaling/integration issues were also addressed, obtaining good short channel device behaviour and enhanced on-currents - requiring low Schottky barrier height and low contact-channel resistance under the spacer layer. Studies of Ni silicide contacts were also undertaken and 80nm DS-NiSi nMOSFETS showed excellent RF performance with good prospects for further downscaling. It was also found that epitaxial Ni produced very low contact resistance on both SOI and SSOI devices. Very recently, we also showed for the first time, that DS can be used to good effect in Schottky barriers to SSOI, giving low barrier heights that decrease with increasing strain (0-40% equivalent), aided by dopant segregation. Early work on Ge channels produced some excellent results, showing very low barriers heights (<0.1eV) for both holes and electrons with DS techniques. On the new gate stack we soon decided to put all our eggs into the $LaLuO_3$ basket. Undoubtedly HfO_2 has more life left in it, but a new material with higher energy offsets and high k value will be needed by the end of this decade. Our results strongly suggest that this material could meet the required spec of gate leakage, interface state density and bulk oxide trap density. This is a very exciting result coming out of our Network. Without question, however, control of the interfacial $LaLuO_3$/Si layer will be critical to achieve low EOT- and maintain high k- values, and here lower processing temperatures could be key. Our forward look (Visionary Project) proved to be a fascinating foray into future nanoelectronics, coming up with the view that Europe should focus activity on FD-SOI technologies including relevant More Moore and Beyond CMOS work, and that there is money to be made in advanced More-than-Moore technologies!

- **WP2:** The main objectives of WP2 within Nanosil are to explore the horizon beyond CMOS and/or beyond MOORE by following closely the emerging technologies for alternative silicon-based post nano-electronic devices. Embedded within the other work packages of Nanosil, WP2 activities cover a wide spectrum ranging from new fabrication methods and novel switching memory concepts to new functionalities and architectures. These activities were fairly balanced among the different groups working on five sub-tasks: i) Si-Nanowires, ii) Carbon Electronics, iii) Small Slope Switches, iv) Templated Self-Organization and v) Visionary Beyond CMOS. Significant progress has been made in these focused efforts, exemplified by the following selected highlights: i) Fabrication of junctionless multi-gate MOSFET (MuGFET), ii) Significant advances in small-slope switches with a grant of the STREP project STEEPER (steep subthreshold slope switches for energy efficient nanoelectronic circuits), iii) Fabrication of Single Electron Memory Devices, iv) Implementation of Ge-QDs in electrical devices, especially in QD-Schottky diodes with cut-off frequency up to 1,1 THz implemented in mm-wave detection circuits. In general these focused research attempts within the network have provided substantial insight in both the confidence of individual groups as well as the ability to collaborate. A large body of “beyond CMOS knowledge” has been accumulated among leading groups in Europe, providing an excellent platform for future projects as well as a decisive orientation for future industrial roadmaps beyond CMOS.

- **WP3:** The JPP has executed 7 batches of fully processed MOSFETs within NANOSIL. Process modules that have been integrated and evaluated in the MOSFET process line are Dopant Segregated Schottky Barrier contacts and LaLuO3/TiN gate stack on bulk-Si, FD SOI and FD strained SOI. Strained Ge channel PMOSFETs and embedded Ge stressors in N and P bulk MOSFETs have also been fabricated. Substantial work has been performed to adopt and tailor the process modules and the MOSFET fabrication line in order to successfully fabricate MOSFETS with new and innovative architectures and materials. The close collaboration between partners involved in the integration of process modules from FPs into the JPPs MOSFET process line has spurred several collaborations and activities that are envisioned to continue many years after the end of NANOSIL.

- **WP4:** WP4 main objective has been to set in operation and strengthen the Joint Characterization and Modelling Platform that was established in the SINANO NoE, by integrating and validating the modelling approaches and tools against ad-hoc, well-characterized template devices. The core of the activity stemmed from the early definition of common template devices for benchmarking simulation models, including 32 nm and 22 nm gate length Bulk and Double gate MOSFETs and nanowire FETs.

Based on these common work-benches, a number of comprehensive investigations were performed, involving several partners in a truly cooperative effort. The topics spanned from the thorough understanding of the low-field mobility in biaxially-strained n-MOS and p-MOS transistors, to a comparison of up to eight different transport models, ranging from a 3D NEGF solver including the scattering mechanisms, to a deterministic solver of the one-dimensional Boltzmann transport equation, applied to DG-MOSFETS and nanowires.
Other highlights of WP4 include the development of an analytical electron and hole mobility model for ultra-thin body FETs on different crystallographic orientations for simulation of SOI-FETs, FinFETs and Silicon nanowires, implemented in the commercial simulator Sentaurus by Synopsys, the calibration of the compact models based also on numerical simulations carried out by NANOSIL partners on template devices, and advances in characterization including a new method to measure the threshold voltage VT in nanoscale transistors and the investigation on the origins of high-field mobility enhancements in uniaxially strained Si by high resolution AFM measurements on strained Si beams with varying degrees of uniaxial strain.

- ***WP5***: Large and growing from year to year number of joint activities (38 in 2008, 47 in 2009, 58 in 2010-11), indicates good and progressive integration of Nanosil partners. It is also reflected by increasing number of within- and cross-WPs/FPs "technical meetings" (18 in 2008, 32 in 2009 and 41 in 2010-11). Partners' integration was reinforced by common PhD students. Then, exchange of personnel served for further strengthening the exchange of knowledge/competence and complementarity between partners. 59 exchanges with total duration of 227 weeks were done during the project. Interaction with industrial partners aiming at roadmapping, assessing the results and assuring theirs transferability to industry was realized through their participation in E&SC Meetings, technical meetings/seminars/workshops; common industry-academia PhD students. Efficiency of partners' integration is proven by high number of joint papers (>100) and joint conference presentations (>130); many newly submitted projects involved 2 or more Nanosil partners, both academia and industry (7 in 2008, 15 in 2009 and 14 in 2010-11). Targeting dissemination of Nanosil knowledge for a wide scientific community, 66 schools/ whorkshops/conferences were organized by Nanosil partners (13 in 2008, 21 in 2009 and 32 in 2010-11) either with or without financial support from Nanosil. Then, Nanosil poster, News Letters, monthly updated Breaking News available on the Nanosil web-site further promote Nanosil achievements. Moreover, 2 books and 33 book chapters published by Nanosil partners assure durable accessibility to the knowledge and developments gathered within Nanosil.

4.1.2 Summary description of project context and objectives

- ***WP1*** was devoted to "More Moore" activities that aim to improve CMOS performance for the 22nm node technology and beyond. It has become increasingly clear that for all the exciting developments of "More than Moore" activities there is still a strong requirement for developments of the underlying transistor performance (see D1.10). The outcomes of WP1 should be applicable both in pushing forward highly scaled devices and as technology boosters that allow longer life to existing geometries. Joint activity has focused on three areas that can be expected to provide significant impact on future CMOS – materials for high speed channels, low access resistance, and high dielectric constant gate stacks.Each flagship project has integrated activities in design, fabrication, characterization and modelling, and has been supported in carrying out that work by the Joint Platforms of WP3 & WP4. A fourth activity has provided a forum for discussing hot topics in ultimate CMOS and identifying areas where the partners of this Network can make a contribution, now and in future.

  Flagship Project 1.1 New Channel Materials (coordinated by FZJ)
  Flagship Project 1.2 Very Low Schottky Barrier MOSFETs (coordinated by ISEN-IEMN)
  Flagship Project 1.3 Advanced gate stacks/ High k dielectric materials (coordinated by Chalmers)
  Visionary Project 1.4 More Moore Forum (coordinated by GRENOBLE INP-FMNT)

Objective 1.1: *To fabricate and investigate new channel materials enabling enhanced mobilities and to assess their properties when transferred to insulator platforms. Specifically to identify the material, platform design, crystallographic orientation, channel direction, layer thickness and strain that maximises electron and hole mobility.*

Objective 1.2: *To develop a global approach to very low Schottky barrier (SB) MOSFETs, including material aspects, device integration challenges, and assessment of this technology as a potential end-of-roadmap solution.*
Objective 1.3: *To find gate stack candidates for the final chapters of scaling that fulfil the ITRS leakage current targets for high performance, low power and low standby power devices for the 16 nm node. Activities focused on $LaLuO_3$ to improve leakage of TiN/$LaLuO_3$/Si stacks, increase understanding of the $LaLuO_3$/Si interface including the nature of the interlayer and tune the TiN/$LaLuO_3$ workfunction*
Objective 1.4: *To hold discussions that will gather information and understanding, and to generate ideas (brainstorming) from academic partners about some hot topics related to ultimate CMOS devices*

- ***WP2:*** In WP2 many different research aspects have to be considered to explore the future emerging CMOS technologies for fabrication of alternative Si-based Nano-Devices. The investigated approaches include the improving of top-down and bottom-up methods for fabrication of nanostructures for Si-NW devices, novel logic switching devices and devices with new functionalities and/or architectures. In the reporting period an enforced cooperation was established between the WP2 partners and expanded to other Nanosil partners, especially to WP1, WP3 and WP4. The direct collaborations between the partners are clearly visible now. The most activities and achievements were in full accordance to the plan of the FSP proposals. The WP2 network activity has been designed to cover the following flagship projects:

FSP2.1 Si-Nanowires
The aim of this project was to define advanced fabrication processes in order to move to high performance devices to assure the availabilities of Si nanowires (NW) for characterization, modeling and simulation tasks. In the reporting period the research activities of FSP2.1 were concentrated on investigation and fabrication of Si nanowires by vertical and horizontal growing techniques for new NW-MOSFETs, the fabrication and characterization of Junctionless Si-nanowire MOSFETs, the investigation of dynamic self-heating effects in Fin-FETs including the influence and correlation between the surface roughness and the induced strain on such structures.
The Junctionless multiple-gate MOSFET (MuGFET) proposed and fabricated by the Tyndall group is the most important highlight, published as Breaking News. This device has demonstrated near-ideal sub-threshold slope, extremely low leakage currents, and less degradation of mobility with gate voltage and temperature than classical transistors.

P2.2. (Associated STREP) **Carbon Electronics**
The goal of this associated project was to establish collaboration between European Research Institutions on carbon based electronics.

FSP2.3 Small slope nanoelectronic switch for low power integrated circuits
In this task, key technological, simulation and modeling contributions for beyond CMOS nanoelectronic switches focused on *Tunnel FET* with very abrupt transition (small slope) between the off and on states were developed. In 2009 a joint STREP FP7 Call 5 proposal STEEPER (Steep subthreshold slope switches for energy efficient nanoelectronics circuits) was prepared. The proposal was evaluated and accepted spring 2010 and is successfully running currently. This STREP proposal coordinated by EPFL based on the participation of four core Nanosil partners and three external industrial partners (Global Foundries, IBM Zurich and Infineon).

FSP2.4 Templated Self-Organization
This project opened a route from defined positioning of self-organized nanostructures, to functionalization and to fabrication schemes for new integrated devices. The research focus was concentrated on templated growth of Si NWs (vertical and horizontal growth) including electrical operation of NW test devices. Various NW transistors were investigated in comparison to top-down versus bottom-up approaches. In addition the implementation of space charge techniques for characterization of Ge-QDs embedded in Si was investigated. Furthermore Single Electron Memory devices (SEM) were fabricated and electrically characterized. Finally, Ge-QDs were implemented successful in electrical devices in response of the reviewer comments.
The main highlight is obtained by a subtractive process which allowed the successful fabrication of single Si/SiGe-QD floating gate self-aligned to Si-NW channel of Single Electron Memory (SEM) structure. For the

fabricated SEM, single electron injection in the floating gate has been demonstrated. Additionally, QD Schottky diodes with cut-off frequency up to 1.1THz have been fabricated and successfully implemented in an mm-wave detection circuit (89GHz RECTENNA). Also, room temperature NDR of Ge QD interband tunneling diodes have been achieved.

Visionary Project 2.5 Beyond CMOS Vision
The goal of this project was to provide a forum (especially workshops) between European Research Institutions on innovative visionary "Beyond CMOS" ideas. A lot of workshops were provided, for example on ***Brain-Inspired Electronic Systems (BIECS),*** on ***Convergence of Electronics and Photonics*** and on ***Beyond CMOS routes.***

- ***WP3:*** Work package 3 is devoted to the Joint Processing Platform (JPP) within NANOSIL. The main objective is to provide partners with a flexible processing platform that can fabricate MOSFETs down to 60 nm gate length. Academic partners within work package 1, 2 and 4 perform research on selected areas such as a particular process module e.g. new channel materials, new high-k/metal gate stacks or Schottky barrier contacts. The purpose of WP3 is to provide a full MOSFET process line where a particular process module can be inserted to evaluate and exploit the potential in fully processed P and NMOSFETs. The JPP is designed to be able to provide short gate length devices but still flexible enough to allow the insertion of new materials and architecture in an early stage of the research. The main objectives are as follows: 1) execuction of MOSFET batches for the flagship projects (FPs), 2) to ensure 3,5 months turn-around time, 3) to coordinate processing between different partners, 4) to fabricate test structures and MOSFETs for WP4 and 5) to develop and integrate processes especially needed for the FPs. KTH coordinated WP3 and had the responsibility to coordinate the MOSFET batches in the JPP for the other work packages and FPs. The JPP is to be seen as a support to the FPs and work within WP3 was dedicated both to tailor and adopt process modules from the FPs as well as tailoring the MOSFET fabrication line in order to integrate the work performed within the FPs. The JPP takes the overall responsibility for the MOSFET fabrication and in close collaboration with partners in WP1 and WP2 coordinate and execute the work needed to integrate a particular process module within a full MOSFET process. Academic partners within WP1 and 2 is thus provided with knowledge and know-how of a flexible full device processing line in order to successfully integrate their work into short gate length MOSFETs. Finally JPP executed batches of MOSFETs with the most promising or scientifically most important process modules as determined in mutual agreement between partners in WP1,2 and 4.

- ***WP4:*** The European semiconductor research community has a long-standing tradition in the development of tools for electron device simulation, both in Academia and Industry. Over the years, several research groups have tackled the issue of modelling nanoscale transistors adopting different approaches and transport models. Among them, Full Quantum models based on the tight-binding (TB) Hamiltonian provide a detailed physical description of nano-structures, while Semi-classical models based on the solution of the Boltzmann Transport Equation (e.g. by Monte Carlo techniques) have been recently extended to the description of nano-FET inversion layers for both the low field and the far from equilibrium quasi-ballistic regime where conventional TCAD tools become inaccurate. These models underpins the recent developments in the modelling and characterization of strain induced mobility enhancements in advanced CMOS technologies concern both the understanding of the underlying physical mechanisms for the mobility modulation and the design and optimization of the devices.
From the experimental point of view, the electrical characterisation of advanced CMOS devices featuring short channel length and ultra thin gate oxides presents major difficulties. This is mainly due to gate length or gate width shortening, which renders effective channel length/width extraction problematic. Moreover, huge gate leakage makes very difficult to get reliable measurements of C-V characteristics, which prevent correct extraction of basic parameters of MOS structures. Main challenges concern the dielectric-channel interface characterization, the transport assessment in ultra-short devices where ballistic effect should occur, and, reliability or instability issues related to few carrier and few dopant number phenomena.

The main objective of WP4 has been to set in operation and strengthen the Joint Characterization and Modelling Platform that was established in the SINANO NoE. This has been accomplished by a two-fold approach: from one end specific problems were tackled by single partners or by a small cluster of partners; on the other end a relatively large number of partners joined forces to integrate and

validate the most advanced modelling approaches and tools against ad-hoc, well-characterized template devices. Successful examples of this truly cooperative activity, are: the results reported in D4.1 (definition of template devices), a thoroughly comparison between the MC simulators (semi-classical model) for a subset of template devices [1], and a comprehensive comparison of full-quantum vs. semi-classical models carried out on the most advanced template devices, including model assessment.
We believe this is an important objective of the NANOSIL Network of Excellence, since such a systematic comparison can be a useful guide to a young researcher entering the field, and can represent in an objective way the relative merits of different tools to a large group potential users, both in Industry and in Academia.
[1] F. Bufler, et al., the 14th International Workshop on Computational Electronics (IWCE-14) Conference, Pisa 2010.

- ***WP5:*** The main goal of WP5 is to reinforce the integration and spread of knowledge between Nanosil partners as well as promoting the network and its achievements towards the whole scientific community. The particular objectives are as follows:

- coordination/stimulation of joint activities between partners by WPs leaders;
- integration between partners through common PhD students, personnel exchanges, etc.
- collaboration with other European and national projects;
- Spreading of excellence / dissemination of knowledge inside and beyond Nanosil through the organization/participation in workshops, courses, conferences, etc.

4.1.3 A description of the main S&T results/foregrounds

- ***WP1:***

FP1.1 New Channel Materials

Strain inducing platforms

Throughout NANOSIL strain continued to be one of the prime performance boosters with no sign, at least from simulation, of significant saturation up to ≈4GPa. Although primarily achieved by local processing techniques, global inducement remains a good approach for at least development work. Also the leverage for a move to on-insulator(OI) platforms for mainstream production remains high and certainly in the low power regime where many of the killer applications are.
There was significant related activity in NANOSIL in these areas, the highlights being:

a) Reverse graded (100) virtual substrates

By compositionally "reverse" grading from a Ge layer grown on Si it was found possible to produce relatively thin and smooth high Ge strain tuning platforms compared to growth directly from Si. A CVD process was developped(Warwick) giving platforms of 80% Ge content with a roughness of ≈2.5nm (Fig 2). These were used for sGe device fabrication at IMEC and KTH.

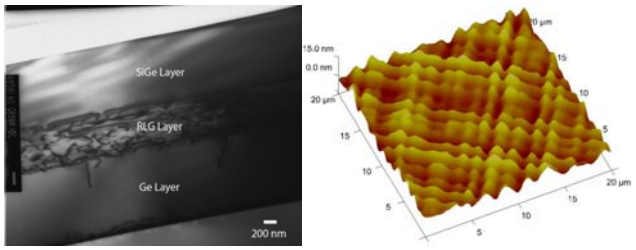


Fig 2. Reverse graded virtual substrate in cross section TEM view and surface profile from AFM.

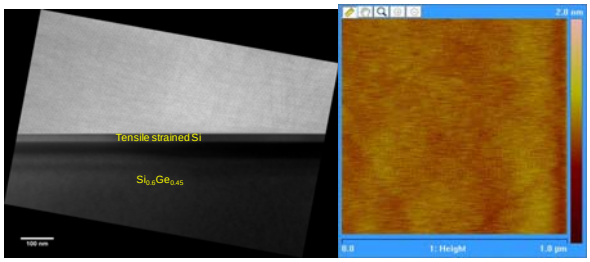


Fig 3. XTEM of re-grown 24 nm strained Si layer on 45%Ge VS, AFM image indicates a smooth surface (roughness < 1 nm).

b) High strained SOI and sGeOI platforms

Development work to create high strain (up to≈ 6GPa) SOI and sGeOI platforms was initiated on Nanosil though a collaboration with Juelich and MPI-Halle (sub-contracted to Juelich). For high sSOI a CMP process was developed at IMEC on 30, 40, 50% and 80% virtual substrates yielding a smooth (roughness in range 0.4 to 0.1nm) and clean surface, Fig. 3 . Si CVD regrowth on these VSs yielded a comparably smooth sSi layer. sGe layers on reverse graded VSs were also shipped to Halle for early development work on a sGeOI process, but as with the high sSOI, only very limited layer transfer work has been possible at Halle due to resource limitations. But this remains an on-going activity involving Juelich, MPI-Halle and Warwick.

Ge MOSFETS

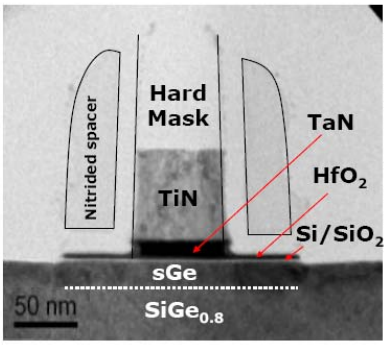


Fig 4: 65 nm strained Ge MOSFET fabricated at IMEC on wafers grown at Warwick.

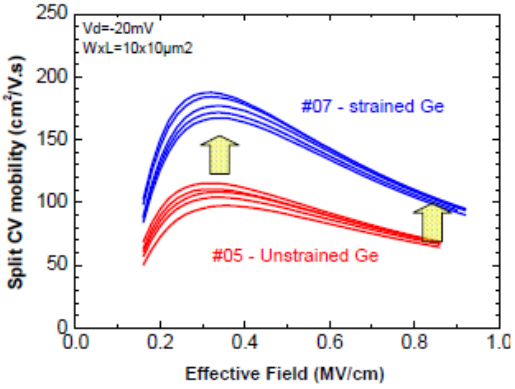


Fig 5: Hole mobility boost from strained Ge by 70%, including boost at high field (long channel devices).

Interest in the Ge channel remains intense particularly as n-channel work now looks as promising as the initial p-channel. There has been very significant work looking at sGe devices on the reverse graded 80% VSs. These VSs were considered sufficiently smooth for this early work and 25, 200mm wafers complete with sGe overgrowth were shipped to IMEC to access their low temperature short-channel process (Fig 4). These produced some very interesting device data showing that this level strain yielded significant mobility enhancements (up to 70% compared to the bulk Ge devices) (Fig 5) and drive current enhancement up to 35% in 100nm devices. Short channel device performance was, however, compromised by local strain relaxation in the halo implanted regions causing a progressive loss of the mobility advantage in shorter channel devices (Fig 6). Following this work an implant-free process is being developed at IMEC, showing considerable promise in short channel bulk Ge MOSFETs.

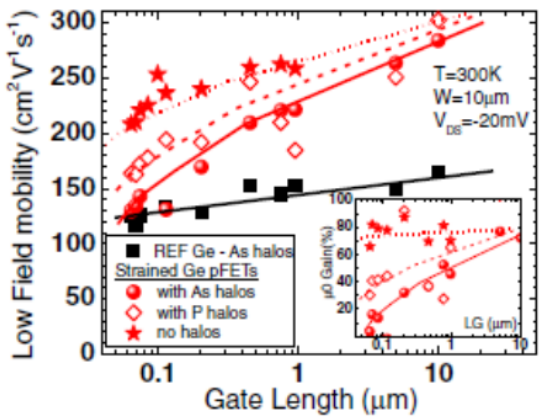


Fig 6. Low-field mobility of holes in strained and relaxed Ge pMOSFETs as a function of gate length showing the effects of different halo implants.

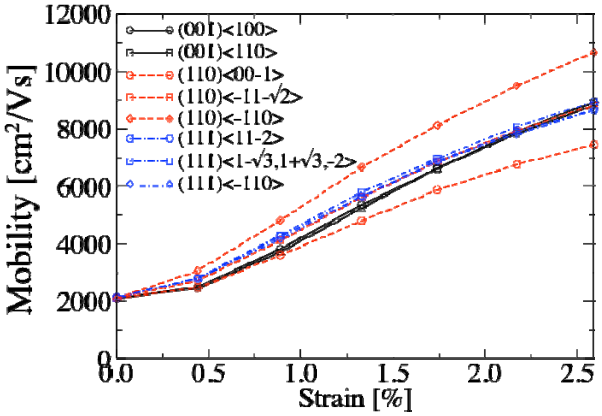


Fig 7: Variation of Ge hole mobility with strain for different substrate/channel orientations. The maximum strain of 2.6% corresponds to 60% Si in the relaxed $Si_{1-x}Ge_x$ substrate.

Related simulation work (Glasgow) indicating the advantage of sGe as a channel material particularly for different crystallographic orientations (Fig. 7), with (110) showing particular promise, especially with OI

platforms, which avoid high channel doping – which can kill this advantage. This activity continues looking at both hole and electron mobility enhancements in (110) and (111) orientations and new funding is being sort.
A further batch of sGe devices is being undertaken very recently at KTH. It was intended that the gate dielectric was to be the Juelich's very exciting $LaLuO_3$ and work was carried out involving a passivating Al_2O_3 layer to produce a working gate stack (TiN gate metal) on r-Ge and s-Ge channel layers (Fig 8). This was however not ready in time and an alternative gate stack fabricated at KTH is being used. This device batch complete with a qualified NiGe contacts is scheduled for completion very shortly. This work on sGe devices involving KTH, Warwick and Juelich will continue beyond Nanosil.

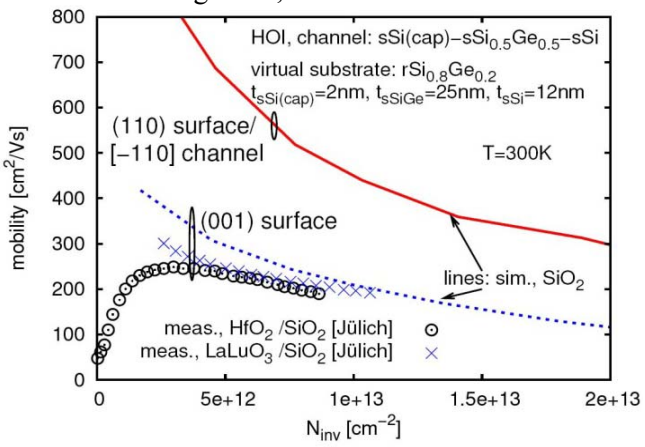


Fig 8: Mobility characteristics of strained SiGe HOI (001) and (110) PMOS with different gate oxide dielectrics.

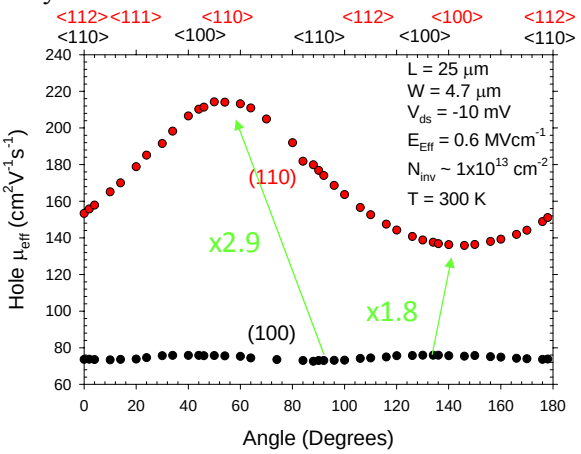


Fig 9: Mobility in (110) Si depending on channel direction.

(100) heterostructure-on-Insulator (HOI) Platforms

These structures enable enhancement of both electron and hole mobilities by combining tensile strained Si and compressively strained SiGe layer OI. In all cases high k dielectrics were used in the gate stack. High mobility short channel p-MOSFETs with compressively strained $Si_{0.5}Ge_{0.5}$/sSOI channel and TiN/HfO_2 or TiN/$GdScO_3$ gate stacks were demonstrated (Juelich).
Good short channel (100 nm) behaviour was seen and hole mobilities as high as 260 cm^2/Vs were achieved and approx 200 cm^2/Vs was obtained in strong inversion, about a 2.5x enhancement compared to Si/SiO_2 devices. This all indicates good potential for further scaling. Simulation work (TUBS) showed good agreement with this mobility behaviour and that further enhancements were to be had from comparable (110) platforms (Fig 8).

(110) Platforms

Some early work was undertaken involving (110) oriented Si substrates.

a) Hole mobility enhancement

Hole mobilities were measured (Warwick) in devices fabricated at KTH in high inversion on (110) Si layers grown by CVD. Mobility enhancements approaching x3 were seen depending on channel direction, similar to previously reported (Fig 9). However, simulation by Granada indicated these arose from variations in effective mass in the heavy hole band as opposed to scattering variations.

b) Global uniaxial strain

Uniaxial strain is optimal for mobility enhancement in many cases and a global uniaxially strain platform is a potentially significant development. A thin (50nm) SiGe layer was deposited on (110) Si, followed by a 5nm thick Si layer(LETI). The SiGe was then relaxed using the Juelich process, creating a smooth tensile strained top Si layer where strain relaxation was predominantly in the [100] direction (Fig 10).

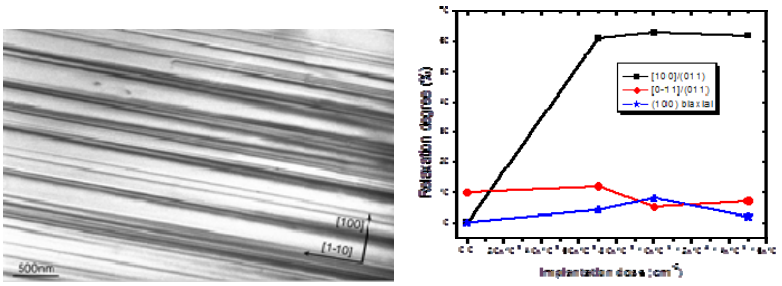


Fig 10: Uniaxial strained (110) Si, showing anisotropic relaxation

FP1.2 Very Low Schottky Barrier (SB) MOSFETs

It is widely recognized that source/drain (S/D) engineering takes an increasing importance in the development of leading edge CMOS generations because of the increasing impact of S/D series resistances on transistor performance. To address this challenge, Flagship project 1.2 has proposed to implement metallic S/D combined to a dopant segregation (DS) strategy to control the doping profile of S/D regions and to mitigate the impact of high thermal budget on new sensitive materials introduced in the gate stack. The first benefit is to potentially reduce the specific contact resistance of the metal/semiconductor junction, while keeping activated dopants sharply localized at the interface. The second benefit is to dramatically lower the junction annealing temperatures to ensure compatibility with many candidate material systems used in alternative gate stacks that cannot stand high temperature processing. By demonstrating performance comparable to conventional implanted and annealed contacts, the DS-SB technique becomes highly relevant for future implementation. Over the of entire duration of the NANOSIL project, significant advances have been achieved within the framework of FSP1.2 bearing on 'Very Low Schottky Barrier MOSFETs', through the seven complementary tasks below: Over the full duration of the Nanosil project, the activity in this FSP1.2 has been the object of 48 peer-reviewed international publications, 30 of which in journals and 18 in conferences/workshops.

Schottky contact engineering by dopant segregation,

As far material engineering is concerned, dopant segregation has been extensively investigated for producing very low Schottky barrier heights, including some work on contact resistance for both n- and p-type source/drain. Many silicide/dopant couples have been studied and included rare earth silicides (erbium, ytterbium), the use of plasma doping, and how carbon incorporation can improve arsenic pile-up leading to a concomitant barrier lowering. The targeted sub-0.1 eV effective barrier height has been demonstrated through several dopant/silicide systems.

Integration issues and compatibility associated to alternative silicides

This task focused on integration strategies and issues associated to segregated Schottky S/D contacts. Original achievements have been obtained, such as the selective etching method of Pt with respect to PtSi using a sacrificial low-temperature germanidation process, the validation of Ti-capping layer strategies to protect rare-earth silicides from oxidation, the determination of the volume expansion upon platinum silicidation applied to nanowires and the dramatic yield improvement in SB-MOS process through accurate placement and engineering of gate-to-S/D spacers.

Scalability of the DS technique

The scalability of the S/D dopant segregation on ultra-thin SOI has been consolidated through the integration of many different flavours of dopant segregated contacts. State-of-the-art results have been obtained like the demonstration of DS CMOS technology, the in-depth study of variability directly related to the DS Schottky architecture or the extremely low contact resistivity of the NiSi2 phase.

Impact of strained silicon on dopant segregated Schottky contacts

The integration of Schottky S/D on strained SOI and the coupling of n- and p-type DS Ni and Pt silicides to strained SOI layers has been systematically studied for the first time. It has been shown that bi-axial tensile strained SOI layers (0-40% equivalent strain) contribute to lower the effective SB, as expected from valence

and conduction band shifts, and was amenable to the DS technique. Complementarily, ultra-thin epitaxial NiSi2 on highly doped SOI and on biaxially tensile strained SOI substrates was found to be about one order of magnitude lower than that of a NiSi layer on both As and B doped SOI and sSOI (Fig. 11). The measured SBHs for PtSi on sSOI are given in the table below.

	No DS(ϕ_{bp} meV)	B ITS DS(ϕ_{bp} meV)	As ITS DS (ϕ_{bn} meV)
Unstrained SOI	250	125	270
sSOI (20% Ge buffer)	210	115	220
sSOI (40% Ge buffer)	183	105	160

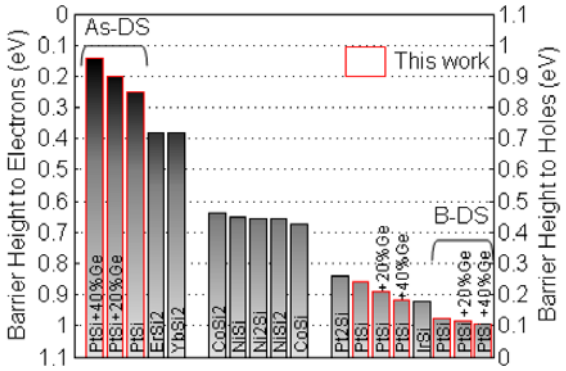
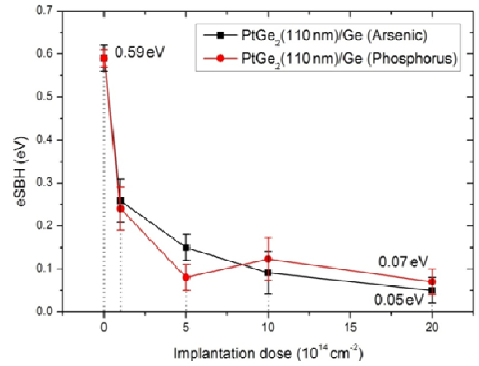


Fig 11: Extracted SBHs in strained Si, showing reduction with increasing strain and DS.



Fig, 12: Extractred SBH of PtGe2/n-Ge contacts as a function of implantation dose.

Relevance of the DS technique on germanium

The synthesis of uniform NiGe and PtGe2 layers has been demonstrated on GOI and SiGe. Extremely low SBs to holes (<0.1eV) were obtained for both silicides. For PtGe2, As and P dopant segregation leads to less than 70 meV SBH to electrons (Fig 12), although it is not as effective in NiGe. The morphology of NiSiGe layer was shown to improve with C implantation into the SiGe, which increases the thermal stability of NiSiGe by about 200 ºC.

Benchmarking of the DS technique

The DS SB-MOS technology has been further consolidated with the demonstration (Fig 13) of state-of-the-art RF performance of 80 nm As-segregated NiSi n-MOSFETs featuring a unity current gain cut-off frequency of 140 GHz. This result completes similar performance at 180 GHz previously obtained for 30 nm p-MOSFETs.

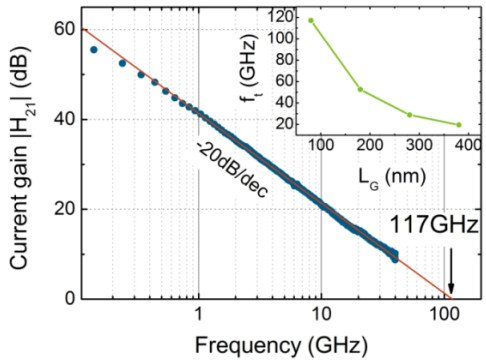
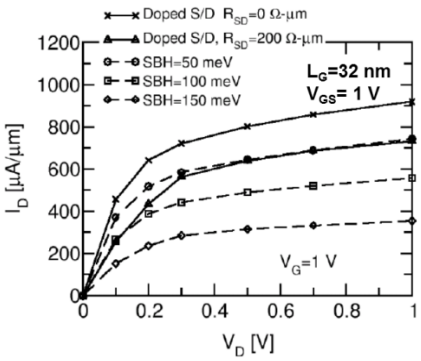


Fig 13:.RF performance of 80 nm NiSi SB-n-MOSFET



Fig, 14: Multi-subband Monte Carlo simulation of FD-SOI SB MOSFET at 32 nm gate length.

Simulation and modelling of DS systems.

Finally, simulation studies based on drift-diffusion, Monte Carlo (Fig 14) and Green's function have supported the analysis and understanding of SB-MOSFETs operation in many respects encompassing both static and dynamic modes.

FP1.3 Appraisal of Gate Stack Materials for End of CMOS Era

Focused activities on LaLuO3

At an early stage of NANOSIL, two gate dielectrics, GdSiO and $LaLuO_3$, were selected as interesting choices for fulfilling the targets set in the DoW. As described in Delivery D.1.12, for GdSiO, which was successfully used for the 22 nm ITRS node in the PULLNANO project, the lower EOT values needed for the present project made it unpractical by technological reasons. Taking into consideration the outstanding properties of $LaLuO_3$, we decided at the end of 2008 to focus on this oxide.

Sample preparation and measurement techniques

For the investigation of current leakage, electrical interface properties and bulk oxide traps, MOS capacitors have been used throughout the project, prepared on 3 inch, 1 – 10 ohm·cm n- and p- silicon wafers. The $LaLuO_3$ dielectric was deposited by molecular beam deposition (MBD) at FZ Jülich, combined with TiN metal contact preparation by sputtering at AMO. For n-type wafers an n^+ backside doping has been necessary, which was prepared at Chalmers. Samples were processed with physical oxide thicknesses of 3, 6, 20 and 40 nm in each set, and were sent out to all experimental groups. Special samples have been prepared for physical investigations (VASE, XPS, MEIS, AFM, STEM, EELS, IPE and Raman spectroscopy) at Liverpool, ITE and Tyndall. The rest of the experimental groups, including Liverpool, ITE, Tyndall, WUT, AMO, INPG/FMNT, Sapienza and Chalmers have been engaged in electrical characterization (C-V, I-V, G-V and multi-parameter admittance spectroscopy (MPAS)). FD SOI transistors were prepared by FZ-Jülich.

Current leakage

For our MOS-capacitor samples with EOT in the range 0.9 – 1.0 nm, a current density of 0.3 A/cm^2 was obtained at 1.5 V gate voltage. A simulation for "calibrating" results from MOS-capacitors to corresponding data for FD SOI transistors with 16 nm gate length was performed. From this, we found that MOS-capacitors with the materials data used are expected to have a 1.5 times higher leakage than the corresponding FD SOI devices. Therefore, in our comparison with the ITRS Roadmap, we use a leakage current vaue of 0.2 A/cm^2, which fulfils ITRS requirements for LSTP and for 14 – 12 nm gate lengths. (Fig.15, below).

Year of prod.	2013	2015	2017	2019	2021	2023	This work
Physical gate length	22	17	14	11.7	9.7	8.1	
Bulk,EOT (nm)	0.9						
Bulk, gate leak. (A/cm^2)	0.15						
MuG SO , EOT (nm)		1.1	1	0.9	0.8	0.7	0.9 – 1.0
MuG SO , gate leak. (A/cm^2)		0.19	0.23	0.30	0.38	0.45	0.2
Interface state dens. (10^{11} cm^{-2})		2	2.2	1.8	1.9	1.9	3.0
Oxide state dens. (10^{18} cm^{-3})		0.89	1.3	1.0	1.8	1.2	1.3
Supply voltage (V)		0.95	0.85	0.85	0.75	0.75	
Sat. drive current (mA/µm)		0.51	0.97	1.16	1.08	1.29	
Off-state current (nA/µm)		0.1	0.1	0.1	0.1	0.1	

Fig. 15 Data for LaLuO3 obtained in FP 1.3 (green) compared with ITRS requirements for LSTP, 14 – 11.7 nm gate lengths.

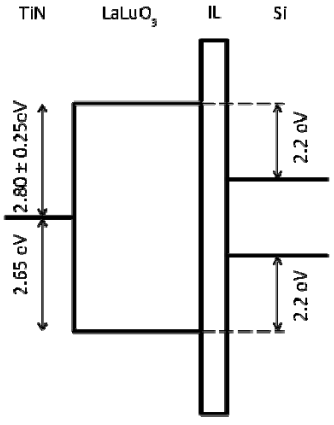


Fig.16: Band diagram for the TiN/LaLuO3/Interlayer/Si stack with barriers measured by XPS and IPE

Interface states and interlayer

Similar to all high-*k*/Si interfaces investigated by us earlier (HfO_2, PrO_2, $HfPrO_2$, Gd_2O_3, GdSiO, LaSiO), the P_b centre is recognized also at the interface between $LaLuO_3$ and silicon. Furthermore, a second type of centres with a different mechanism for electron capture was found. The interface state concentrations obtained

were found to be close to the specifications for the 14 – 12 nm gate length requirements by ITRS (Fig. 15). Controlling the high-*k*/Si interlayer will be a crucial issue for reaching the end of the Roadmap at 8 – 5 nm gate length. The $LaLuO_3$ interlayer was investigated by XPS and found to be an SiO_x like layer with a clear content of the metals included in the high-k dielectric, without a significant deviation from $k \approx 4$ of this material. This was also supported by preliminary MEIS data.

Bulk oxide traps
Bulk oxide traps were investigated by C-V, pulse C-V, variable angle spectroscopic ellipsometry (VASE), luminescence and charge carrier statistical considerations. An interesting agreement with theoretical literature estimates of energy level positions for oxygen vacancies in HfO_2 and with charge carrier statistics was found. Corresponding theoretical considerations for $LaLuO_3$ predict energy a level scheme for oxygen vacancies very similar to that of HfO_2. Continued experimental confirmation in this area is vital for future development. The total concentration of bulk oxide traps, in the ITRS definition fulfils the requirements for 14–12 nm gate lengths.

Energy barriers
$TiN/LaLuO_3$ and $LaLuO_3$ energy barriers were measured by XPS and internal photo emission (IPE) with results as shown in Fig. 16.

Transistor data
Test transistors with $LaLuO_3$ gate dielectrics were prepared by FZ Jülich. Strained and unstrained SOI n/p-MOSFETs were fabricated with a full replacement gate process. The LaLuO3/Si interface showed a Dit level of 4.5 × 1011 (eV cm2)−1. Fully depleted n/p-MOSFETs with LaLuO3/TiN gate stacks indicated very good performance with steep subthreshold slopes of ~ 70 mV/dec and high Ion/Ioff ratios. In addition, strained SOI showed enhanced electron mobilities with a factor of 1.7 compared to SOI. Both electron and hole mobilities for LaLuO3 on SOI were similar to the mobilities reported for Hf-based high-k devices.

Relation to the ITRS Roadmap and conclusion
ITRS relevant data for the $LaLuO_3$ dielectrics investigated in FSP1.3 is shown in Fig. 15. Depending on future development of the $LaLuO_3$/Si interlayer, we consider this dielectric as a potential candidate for fulfilling the requirements along the ITRS Road down to the tapered 8 – 5 nm end.

VP1.4 More Moore Forum

The visionary project was designed as a forum to exchange ideas, create discussion and debate, and generate synergies between partners on the topic of advanced CMOS. It was also the opportunity to discuss challenges that are not addressed within flagship projects. Finally, as these meetings also gather non-Nanosil speakers, it is also the occasion to embrace research carried out outside the network, and outside Europe.
Ten workshops were organised during Nanosil, details of which appear in D1.1, D1.5 and D1.10:

1. Satellite event of the Third SINANO Device Modelling Summer School, Bertoni, Italy, 2008
   "Low Field Transport in Advanced MOSFETs"
2. Satellite event of ESSDERC 2008, Edinburg, UK
   "*CMOS variability research in Europe: from atomic scale to circuits and systems*"
3. Panel session at EUROSOI 2009,
   "*What is the killing advantage of multiple-gate SOI MOSFETs: electrostatics and scalability, transport or functionality?"*
4. Fringe workshop at ULIS 2009, Glasgow, UK
   "*Open questions in the Ion Ioff optimisation in Advanced MOSFETs*",
5. Panel session at the 2nd International Conference on CMOS Variability (ICCS).
   "Are we ready for Design for Variability at sub 32 nm ?",
6. Satellite event of the European MRS Meeting, Symposium I on "Silicon and Germanium issues for future CMOS devices"
   "High-Mobility Channel Materials and Device Performance",
7. Panel session organized during EuroSOI meeting in 2010 Grenoble :
   "*SOI technologies : What kind or research for what kind of products ?*"
8. Workshop and panel before ULIS 2010 Glasgow, 17th March 2010 :
   "High mobility nMOS substrates: strained-Si, Ge or III-V ?"

9. Workshop and panel before SISPAD 2010 Bologna, 9th September 2010 :
   "*Simulation and Characterization of Statistical CMOS Variability and Reliability*"
10. Workshop after ESSDERC 2010, Friday, Sept. 17th, 2010
   "*At the convergence between More Moore and More Than Moore / Beyond CMOS activities*".

Recommendations for European R&D:

1. European R&D should pursue effort in developing FDSOI technologies, as it is now or never for SOI
2. More Than Moore activities should be encouraged and supported; however, without neglecting More Moore and Beyond CMOS. Projects that develop the three activities all together should be encouraged.
3. As highlighted by variability, technology and design should work in closer contact. Europe has expertise in both areas. Research and projects integrating technology and design should thus be promoted.

- ***WP2:*** The main scientific and technical results of WP2 can be described and distributed by the following selected contributions delivered by the mainly experimental flagship project groups FP 2.1, FP2.3 and FP 2.4.

FP2.1 "Nanowires"

Vertical Si nanowires

Vertical nanowires based FET is an interesting opportunity for nanoscale devices because of its miniaturization capabilities and its compatibility with wires produced by top-down but also by bottom-up approaches. Nevertheless, this technology is faced on specific technological challenges due to the 3-dimensionnal configuration. One example is the contacting of each termination of the Si NWs in order to electrically characterize the structures and to reproduce the configuration of S/D contacts of a future FET device. Previously we demonstrated the formation of highly dense vertical NW arrays by a top-down approach, with 100% reproducibility, and a perfect control of the diameter and the position. In a present work, we demonstrated the fabrication and characterization of two-terminal structures implemented on such NWs arrays defined by a top-down approach, as presented in Fig.1. Each termination of NWs is silicided and contacted to an external metal line. Thanks to a precise control of the radius and number of NWs in an array, we demonstrate a perfect reproducibility in the *I-V* characteristics (Fig.2) when a large number of NWs is considered (up to 5100 NWs in parallel) compared to a single NW, which proved to be efficient to considerably attenuate variability associated to the stochastic nature fabrication process steps at nanoscale. The temperature dependence and the non-linearity of I-V characteristics (inset Fig.2) are identified as a clear signature indicating that contacts dominate the overall resistance of the NWs arrays.

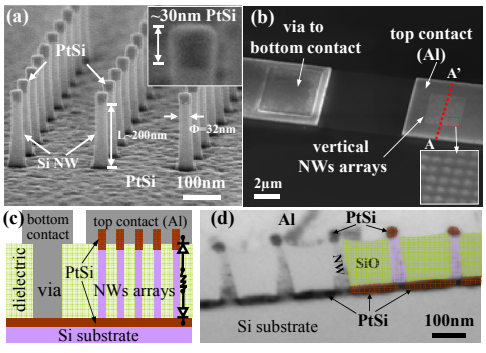


Fig. 1. (a) SEM image of vertical NW arrays (18x18=324 in parallel) with Φ=32nm, L~200nm, 100% reproducibility and hetero structure PtSi/Si. (b) SEM image (40° titled view) of Al extrinsic measurement pads. Inset: Image zoom on NWs arrays. (c) Schematic cross section view of the measurement set-up that can be schematized by two back to back metal-semiconductor

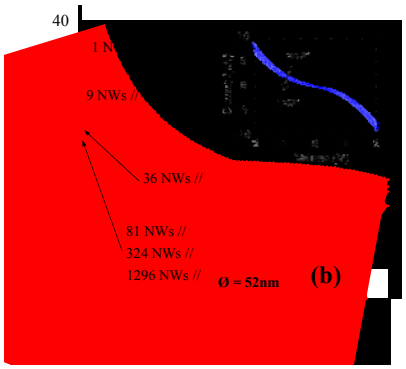


Fig. 2. average current per NW as function of the applied voltage @ 20°C of 2 contacts device with several NWs in parallel from 1 to 1296 with Φ=52nm with, in inset, current evolution with the temperature.

junctions separated by a series resistance. (d) TEM image (cross-section view) of a NWs array embedded in a dielectric SiOx planarization layer. Al is deposited to act as a top contact.

Self-heating characterization at UNEW of strained Si nanowires from EPFL

100 nm wide Si nanowires were fabricated using a bulk top-down Si nanowire platform, 0.8 μm lithography, hard mask and spacer technology. In the process, a sacrificial oxidation step was used to diminish the size of the wires and introduce tensile strain. Direct strain characterization on the suspended bucked Si NWs represents non-uniform lateral uniaxial tensile stress with a maximum almost at the middle of the Si NW. Strain measurements on EPFL devices have been performed by University of Newcastle. The maximum found tensile stress was 2.6 GPa and the peak of stress depends on the dimensions of the wire (thickness and length), oxidation conditions (temperature and duration) and hard mask. The wire length and wire width on the mask varies from 2.0-20.0 μm and 0.8-1.8 μm, respectively, offering a wide range of Si NWs with different strain and cross-sections (the longer and narrower wires offer suspended and buckled triangular Si NWs after oxidation and stripping steps suitable for gate-all-around architecture after gate stack deposition, however the shorter and wider wires offer attached wires to the substrate suitable for omega-gate architecture). The gate-stack includes ~15 nm SiO_2 (thermal oxide) and 300 nm of in-situ N+ doped poly-Si.

In collaboration with the Newcastle University, the self-heating effects in those devices have been investigated as a function of the wire cross-section. A clear increase of the self-heating impact for narrower wires was observed.

Junctionless Si nanowire MOSFETs

Prof. J.-P. Colinge and his research group at Tyndall have been working on the static characterization of junctionless Si nanowire multigate MOSFETs (uniformly and highly doped from the source to drain contacts). The Si nanowire is completed depleted at OFF state (V_g = 0 V) and is neutral at ON state ($V_g > V_{th}$). The advantages related to the absence of source-to-channel and drain-to-channel junctions and the volume conduction in ON state have been highlighted. They have a near-ideal subthreshold slope, close to 60 mV/dec at room temperature, extremely low leakage currents, exhibit less degradation of mobility than classical transistors when the gate voltage is increased. Of course, due to the high doping level in the channel the poor carrier mobility is the major limitation of those novel devices. However, as for other advanced MOSFETs, strain channel engineering might be applied to improve the carrier mobility. Recently, in collaboration with UCL, static characterizations of junctionless multigate MOSFETs (MuGFET) as a function of an applied mechanical stress using a 4-point bending setup (Fig.3) have been performed. Improvement of current drive in n- and p-type silicon junctionless MOSFETs using strain has been demonstrated. The extracted piezoresistance coefficients are in good agreement with the piezoresistive theory and the published coefficients for bulk silicon even for 10 nm-thick silicon nanowires as narrow as 20 nm (Fig.4). These experimental results demonstrate the possibility of enhancing mobility in heavily doped silicon junctionless MOSFETs using strain technology. These results have been recently published[2].

[2] J.-P. Raskin, J.-P. Colinge, I. Ferain, A. Kranti, C.-W. Lee, N. Dehdashti Akhavan, R. Yan, P. Razavi, R. Yu, "Mobility improvement in nanowire junctionless transistors by uniaxial strain", *Applied Physics Letters* **97**, 042114 (2010).

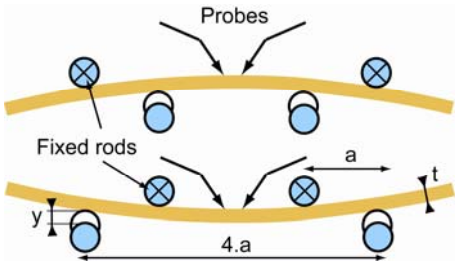


Fig. 3. 4-point bending measurement setup and relationship between the induced stress (σ) and vertical displacement (y) of the bottom movable rods. For all measurements, the spacing "a" was equal to 20 mm.

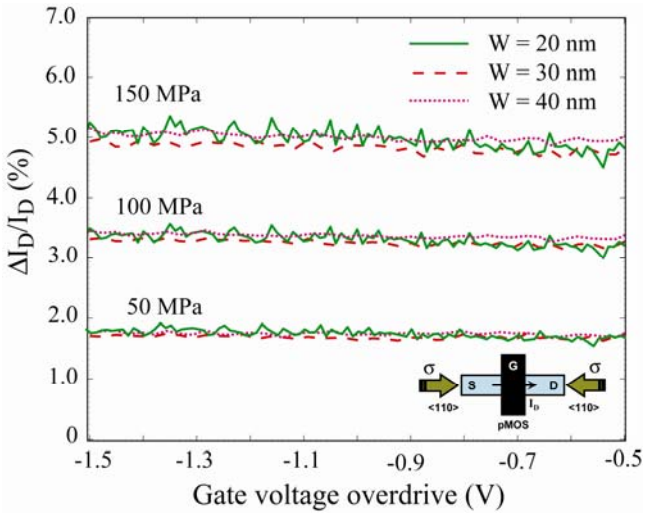


Fig. 4. The variation of drain current, ΔID/ID, as a function of gate voltage overdrive, VGS-VTH, in a p-type junctionless MuGFET characterized by fin width of 20, 30 or 40 nm for various applied compressive stresses.

Low frequency noise characteristics of silicon nanowires (FMNT-IMEP)

Low-frequency noise has been studied by INPG in collaboration with CEA-LETI in compressively strained $Si_{0.8}Ge_{0.2}$ core-shell nanowire (NW) p-channel transistors compared with un-strained NWs. The noise has been well interpreted using the carrier number with correlated mobility fluctuation model. As a result, un-strained devices present more surface mode operation than c-strained ones, rendering more efficient the remote Coulomb scattering from oxide/Si cap interface charges and, thereby, increasing the α coefficient in CMF process. According to the remote Coulomb scattering theory, a reduction of one decade of α corresponds to about 1.7 nm additional remoteness for c-strained NWs, which is in agreement with the effect of silicon cap around 1~1.5 nm.

Dynamic self-heating in Fin-FETs

Dynamic self-heating effect has been characterized in n-channel FinFETs on Silicon-on-Insulator (SOI) platform. RF extraction technique has been deeply analyzed and dependence of thermal resistance on fin width (W_{fin}), number of parallel fins (N_{fin}) and fin spacing (S_{fin}) was studied.

One of the conventional techniques to characterize self-heating effect in MOSFET which does not require special structures is small-signal AC conductance. It is based on the assumption that at high frequencies channel temperature does not follow voltage oscillations, hence dynamic self-heating is removed. Conductance difference at low and high frequencies (where AC self-heating is removed) can be translated into device thermal resistance. Typical frequencies used in the AC conductance technique are in kHz-MHz range. However, as devices scale down thermal time constants are reducing into ns values and higher frequencies are required to reach self-heating-free characteristics. Indeed, thermal time constant is the product of thermal resistance and thermal capacitance. Whereas thermal resistance is inversely proportional to the surface area of the device, the thermal capacitance is related to its volume. In advanced non-planar devices volume-to-surface ratio is drastically decreasing which leads to smaller time constants. RF extraction technique up to a few GHz was applied to extract self-heating effect parameters in n-channel SOI FinFETs of various geometries. It was found that self-heating is mostly sensitive to number of parallel fins per gate finger (Fig. 9) and less to the fin width and fin spacing. Higher number of parallel fins, increased fin width and fin spacing improve thermal properties of Fin-FETs, however it may introduce additional issues into chip design, poorer electrostatic control and reduced integration density. These results have been obtained in collaboration between UCL and Newcastle University.

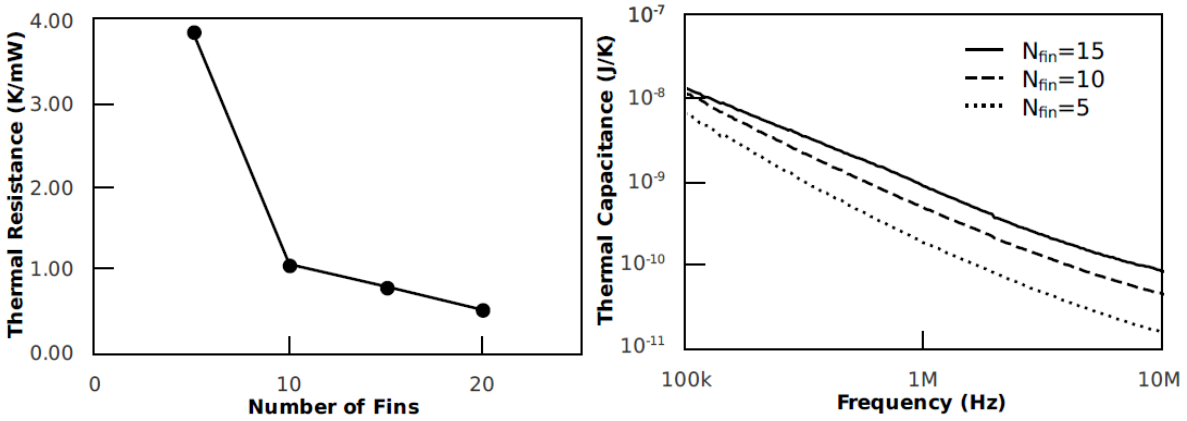


Fig. 9. Variation of thermal (a) resistance and (b) capacitance in the devices with different number of parallel fins per gate finger. W_{fin} = 22 nm, S_{fin} = 328 nm

Nanomechanical characterization of Si nanowires

Nanomechanical characterization of released silicon nanowires using on-chip loading has been investigated. The aim of this action is to experimentally study the electro-mechanical properties of Si nanowires using the proprietary lab-on-chip methodology developed at UCL. The basic idea is to use internal stress present in one film (named actuator) to provide the actuation for deforming another film (named specimen) attached to the first film on one side and to the substrate on the other side. The measurement of the displacement resulting from the release of both films gives access to the stress and the strain applied to the test specimen provided the Young's modulus and mismatch strain of the actuator film are known. The Si nanomachines have been fabricated at Chalmers University of Technology and released and characterized at UCL. The fracture strain of Si nanowires as a function of the nanowire cross-section and length has been investigated (Fig. 11). Fracture stress as high as 9 GPa has been measured for nanowires with a cross-section of 50 nm x 50 nm. The next step is to measure the I-V characteristics of these strained Si nanowires to extract piezoresistance coefficients in two-dimensional confined Si nanostructures at high level of strain.

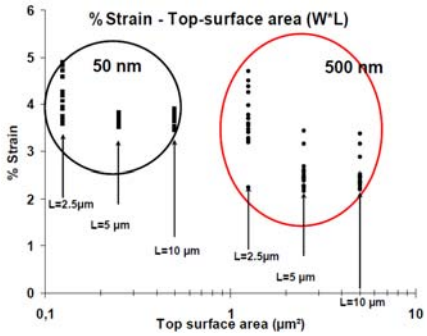


Fig. 11. Fracture strain in Si as a function of nanowire dimensions.

Si nanowires as gas sensors

Doped and undoped Si nanowires presenting cross-sections from 100 nm x 50 nm down to 25 nm x 50 nm have been functionalized and used to detect specific gases. A shift of more than 10 V (Fig. 12) of the Si NWs transfer characteristic has been observed when exposed to acetic acid vapour. The observed current change factor for a fixed back gate voltage of 10 V is of approximately 500 (Fig. 13). The sensitivity of Si NWs to other gases and for different dimensions is currently analyzed.

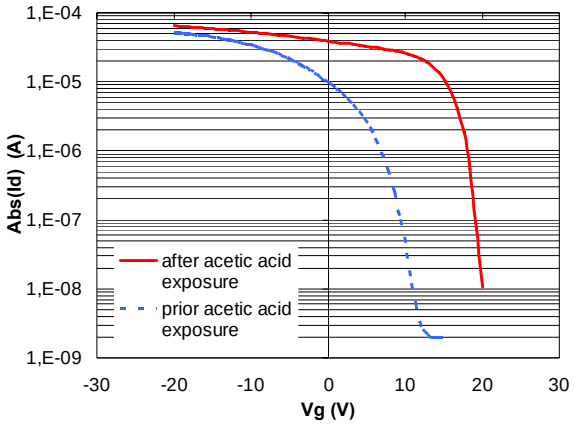


Fig. 12. Transfer characteristics of a Si NW presenting a cross-section of 100 nm x 50 nm before and after exposure to acetic acid vapour.

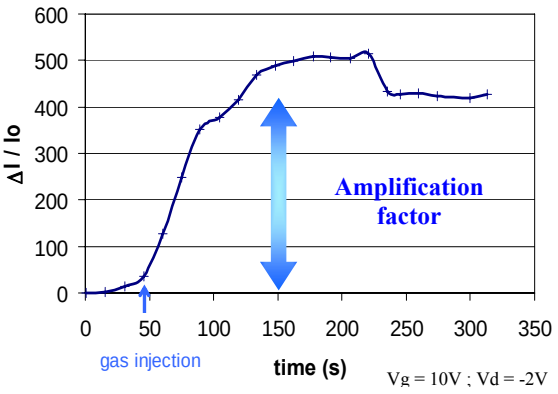


Fig. 13. Relative current change as a function of time at fixed back gate and drain drain bias conditions.

Correlation between surface roughness and induced strain

The rms surface roughness and correlation length are key parameters to model carrier mobility in MOSFET inversion layers. Simulations indicate that only a reduction in rms roughness compared with bulk Si values can explain the high values of electron mobility observed experimentally in tensile strained silicon devices. However due to the limited characterization techniques available to measure roughness accurately on a nano and sub-nanoscale, to date such assertions have remained largely unconfirmed. Using the proprietary lab-on-chip concept of UCL, the paucity of roughness measurements by reporting on roughness parameters in uniaxial strained Si beams relevant for state of the art MOSFETs, nanowire and MEMS devices, with varying degrees of strain have been addressed. Nanoscale roughness is characterized high resolution AFM. The test structures comprise a silicon nitride actuator to induce a wide range of deformation levels in the Si beams, from 0.2% to 2.8%, equivalent to a stress range from 0.3 to 4.9 GPa. The rms roughness was found to reduce gradually from 0.29 nm for unstrained Si to 0.07 nm for 2.8% of strain. Similarly, the correlation length of nanoscale surface undulations in the direction of the applied stress reduced from 5.3 to 4.3 nm for the same range of strain values (Fig. 14). These results provide unequivocal confirmation that a reduction in rms roughness accompanies increasing tensile strain.

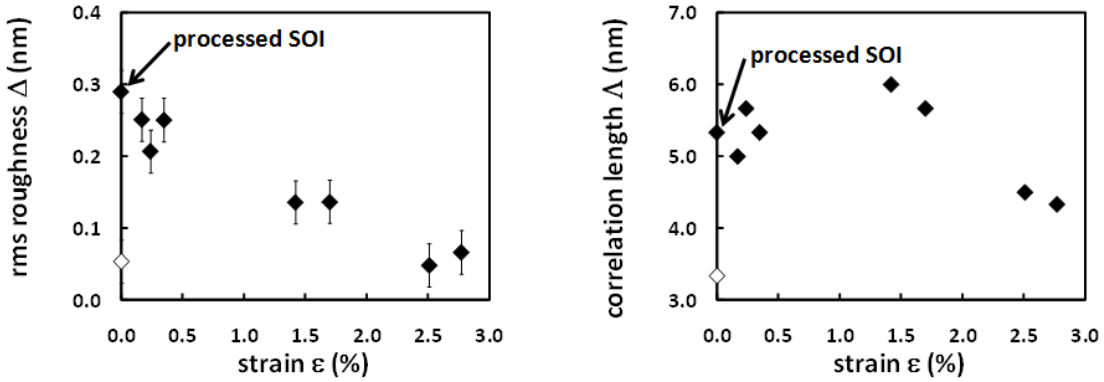


Fig. 14. Δ and Λ as a function of strain in the Si beam for 95 x 95 nm^2 images. Error bars correspond to the maximum variation in rms calculation.

FP2.3 "Small Slope Switch"

The work corresponding to the 3rd periodic report of FSP2.3 was carried out on the topics and based on the collaborations described below.

Ferroelectric Tunnel FET (Fe-TFET) with a SiO2/Al2O3/P(VDF-TrFE) gate stack

Tunnel FETs have been fabricated with a ferroelectric polymer layer inserted into their gate stack (*Fig. 1(a) and 1(b),* SiO_2/Al_2O_3/PVDF gate stack). This fabrication activity explains also why EPFL has used some resources under the consumable category. This novel family of devices combines the low subthreshold current of band-to-band tunneling transistors with the retention characteristics of ferroelectric devices, enabling interesting features for future one-transistor (1T) memory cells. Hysteretic behaviour of such devices is revealed by experimental measurements and its principle confirmed by calibrated two-dimensional numerical simulations. Low temperature measurements confirm the reduced sensitivity of the Tunnel FET subthreshold swing to temperature, and distinguish them from fabricated reference Fe-MOSFETs.

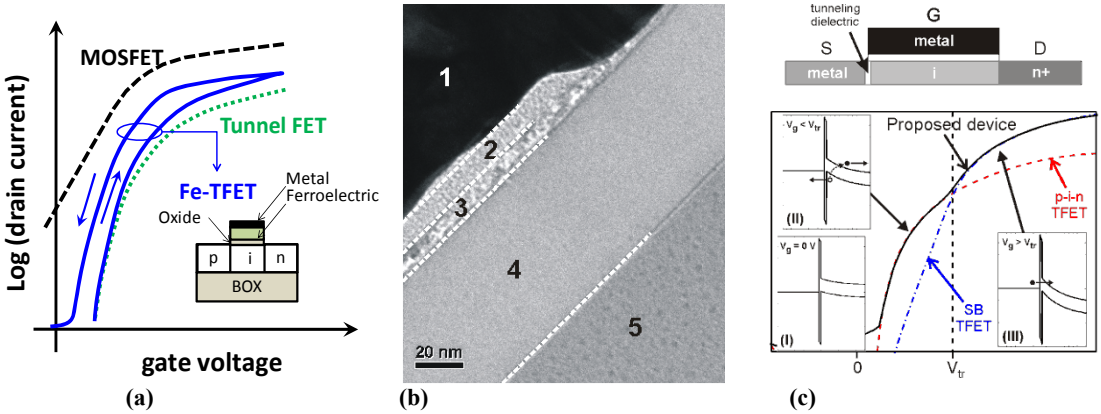
Abrupt switch based on internally combined Band-To-Band and Barrier Tunneling mechanisms

A novel Tunnel FET concept has been designed (*Fig. 1(c)*), which makes use of internally combined quantum mechanical band-to-band and barrier Tunneling mechanisms to achieve improved performances and overcome the intrinsic low current drive limitations of conventional Tunnel FETs and the 60 mV/dec limitation of MOSFETs at room temperature. This new structure, including an ultra-thin dielectric between metal source and silicon channel, allows a sub-60 mV/dec average subthreshold slope (SS ~43 mV/dec) and a uniquely high I_{ON}/I_{OFF} ratio (~10^{11}). The device principle and the potential performances are investigated by numerical simulation. (This project is developed under Nanosil in collaboration with the Steeper project, particularly in collaboration with partners from IUNET and also with additional funding from the Swiss Nanotera project. The thesis of the doctoral student (Luca De Michielis) is co-advised by professor Adrian Ionescu of EPFL and Luca Selmi of University of Udine. Luca De MIchielis received in 2011 the IBM Fellowship Award, which is an extraordinary achievement.

Advanced modelling and simulation of Tunnel-FET devices

Thanks to a specific mobility action EPFL and IUNET-Udine collaborated to the assessment of device architectures and models for simulation of silicon Tunnel-FETs. As it is well known, differently from conventional MOSFETs, where the injection mechanism is governed by the emission above the source barrier, in Tunnel-FETs the carrier injection mechanism is replaced by the quantum mechanical band to band tunneling. Being inherently based on a quantum effect, a proper modeling of Tunnel-FETs in principle requires a full quantum transport approach, which is however extremely demanding from a computational point of view when applied to realist devices. In order to include the B2BT in TCAD simulations based on the drift-diffusion theory, several different models that describe the local and non-local B2BT as an additional generation-recombination mechanism have been proposed (Fig. 2a).

In the framework of the above mentioned researcher mobility, we have thus used a semiclassical modeling approach based on the solution of the BTE by Monte Carlo techniques made available by the IUNET-Udine partner to comparatively evaluate some of the limitations of current models for an accurate description of B2BT generation mechanisms and to examine conventional Tunnel FET architectures. In particular we explored the impact of different modeling assumptions (e.g. that on the shape of the tunneling path) on the relative performance of different device architectures (Fig. 2b). These analyses proved useful to assess the potentials of the different approaches for the optimization of the architecture of these new devices. Moreover they proved extremely useful to gain a deep insight in the impact of the B2BT mechanism on the device characteristics and led to new ideas on how to optimize Tunnel-FETs for enhanced performance. (This project is developed under Nanosil in collaboration with the Steeper project).



(a) (b) (c)

Figure 1: (a) Fe-TFET concept (qualitative comparison with Tunnel FET and Fe-MOSFET) suggesting more abrupt transitions than Tunnel FET and hysteretic behavior. (b) FIB-cut showing the cross section of the SOI and gate stack at the level of the transistor channel. (c) Band diagrams of a Schottky Tunnel FET with thin interfacial dielectric at source under different gate bias conditions.

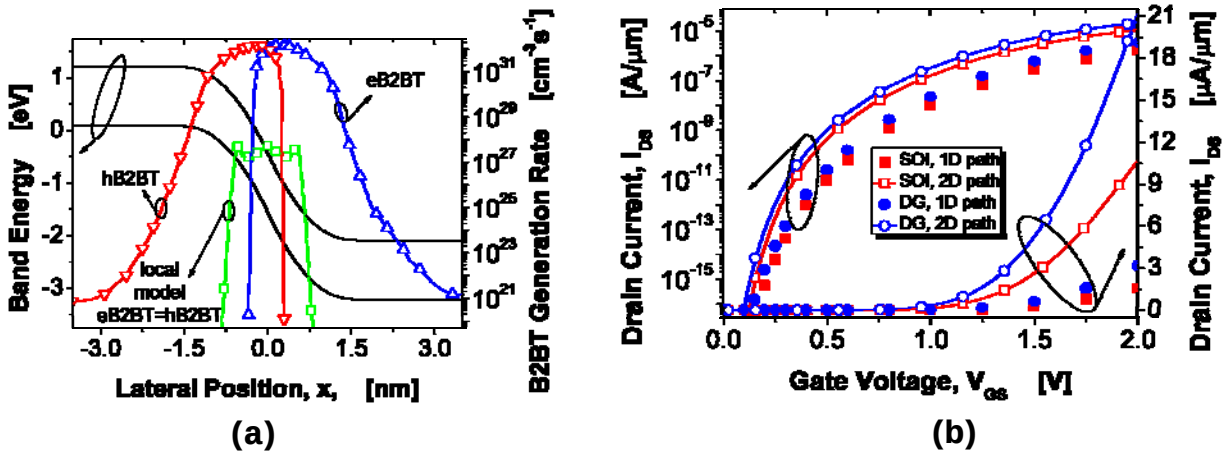


Figure 2: (a) Numerical simulation of a highly doped p-n junction showing the relevant differences between a local band-to-band tunneling model and a non-local one. (b) Comparison of the choice of the tunneling path on a SOI and a DG device. 1D path means tunneling parallel to the transport direction, whereas 2D path means tunnelling in the direction of the maximum valence band gradient.

FP2.4 "Templated Self-Organization"

In this report, technical progress is described for activities (NW transistors, Single Electron memories and QD characterization and devices) defined in the previous annual report. These activities have been further focused for the last project period (starting from 06/2010) in accordance to the remarks of the reviewers, and, to the project tasks, Deliverable and Milestone ("D2.6 Nanowires fabricated by Templated Self-Organization", and "M2.7 Electrical operation of nanowire test devices fabricated by Templated Self-Organization). In accordance to the recommendations of the reviewers (2nd review, recommendation #6) the growth of Ge QD wafers was finished by 04/2010. The further activities have been concentrated on the implementation of these layers in devices and circuits and their characterization.

Bottom up Si-NW transistor (CEA, INPG, Tyndall), cooperation with FSP 2.1

We have investigated the way to improve the nanowires/metal contact resistance. In order to fabricate devices, nanowires were sonicated in IPA and then dispersed onto a p++ Si <100> substrate covered with a 200 nm thick Si_3N_4 layer. Optical lithography was then used to define drain and source contacts. After development, contacts were metalized (Ni 80 nm / Al 120 nm) using an e-beam evaporator. A lift-off step was performed to remove resist and an O_2 plasma step was used to clean the wires from all resist wastes which could perturb electrical transport. Finally metallic contacts were silicided at 400 °C under Nitrogen flow using a Rapid Thermal Annealing (RTA) furnace and at varying duration. The electronic properties of the Si NW FETs as a function of gate and source-drain biases were measured using a semiconductor parameter analyzer (Keithley 4200) at room temperature and in ambient air.

In the present case, we have studied the kinetics of Ni silicide growth for an annealing temperature of 400 °C under N_2 gas by varying the process time. The temperature has been chosen to obtain the less resistive NiSi. Measurements of silicide length were performed using a Scanning Electron Microscope (SEM) allowing us to differentiate the silicide from the silicon nanowire from the contrast observed in the secondary electrons images.

Prior to silicidation, devices were characterized with a probe station. A comparison of the behaviour of a device before and after silicidation is given in **figure 2.4.1** showing a 100 fold increase in the current passing through the nanowire. Measurement of the saturation current flowing through the channel at V_{gs} = 0 V gives

I_{sat} = 0.5 A.cm^{-2}. This can be interpreted in the frame of a pure thermoionic emission model and gives a barrier height of $\Phi_B \approx 0.45$ eV, close to one of the two expected values for NiSi/Si barriers (eV), and shows that our nanowires have residual p type doping.

Typical I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristics of silicided devices are shown in **figures 2.4.1 and 2.4.2**. The devices exhibit I_{ON}/I_{OFF} ratio up to 10^5 with a maximum ON current obtained for negative V_{GS} values of the order of ~ 5 µA giving a current density around 28 kA/cm². The characteristic in the ON state is linear with a device resistance around 300 kΩ, which corresponds to a resistivity of 133 mΩ.cm. However, this resistance is likely arising from one of the two diodes obtained at the contact between the silicide and the Si channel under backward bias, where transparency is increased by the strong band bending at the junction for decreasing V_G.

We obtained a transconductance g_m~1.2 µS giving us a hole mobility close to 200 cm²/Vs at 300K.

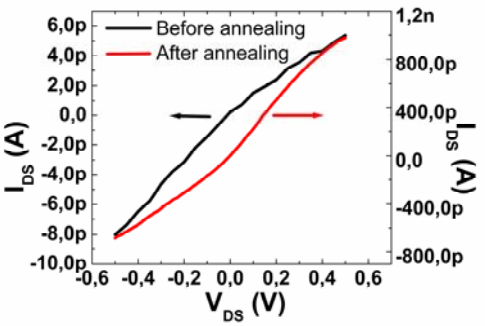


Figure 1.4.1 I_{DS}-V_{DS} characteristic of a SiNW FET with nickel contacts before and after annealing step at 400 °C for 30 s.

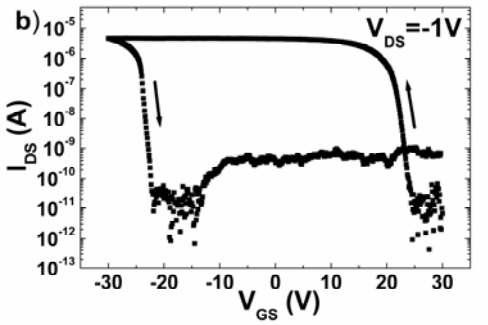


Figure 2.4.2 I_{DS}-V_{GS} characteristic of a SiNW FET with 200 nm Si_3N_4 back gate insulator recorded at V_{DS} =- 1 V. The on-off current ratio of this device is 2x10^5. Arrows indicate either the positive to negative or negative to positive gate voltage sweep.

Joint flagship activity between FP 2.1 and FP 2.4 (horizontal growth & doping of NW)

For Si-NW transistor fabrication based on simultaneously grown networks of connected NWs between predefined Si pads on SOI, NW horizontal growth onto SiO_2 between the pad sidewalls has been investigated. Growth recipes using gold colloids dispersed via drop casting on test wafers patterned by UCL have been developed. When placed in contact with a pad sidewall, a gold colloid gives rise to a horizontal nanowire starting from the pad, as seen in the **fig. 2.4.3** below. UCL patterned test wafer was sent to Tyndall for selective area deposition of gold and CMOS compatible Pt colloids at the source and drain pads using the dielectrophoresis technique.

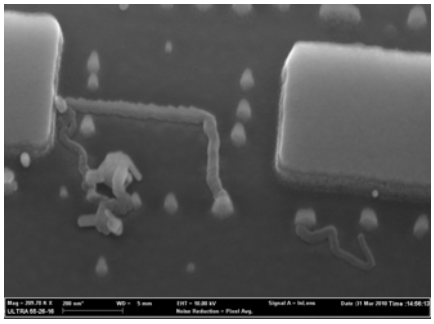


Figure 2.4.3 undoped Si NW grown from an Au colloid localized at the pad sidewall.

In addition to the above-mentioned work on the localization, the doping of nanowires using diborane (p type doping) and phosphine (n type doping) precursors mixed with silane has been characterized. The resistivities of single nanowires (see in **figure 2.4.4**) have been measured and incorporation of boron and phosphorous in nanowires has been checked.

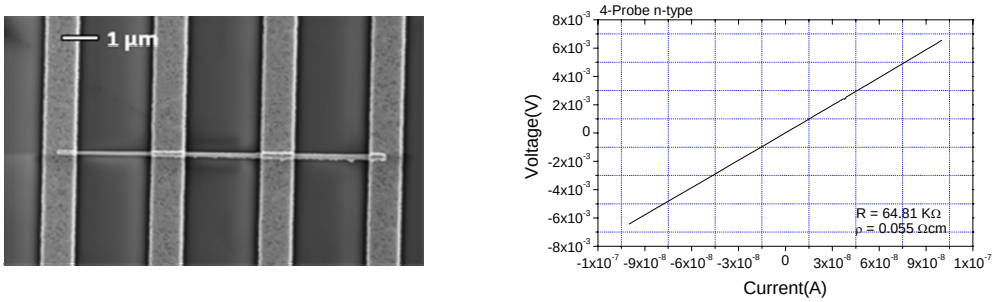


Figure 2.4.4 Single nanowire connected in a four probe configuration (left) and corresponding resistance measurement (right).

Moreover, doping modulation along a nanowire has been achieved by tuning the reactive mixture composition in the CVD tube during the growth (**fig. 2.4.5**). As an example, a nanowire Schottky diode has been fabricated with a heavily p doped end while the other was set p doped (**fig. 2.4.6**).

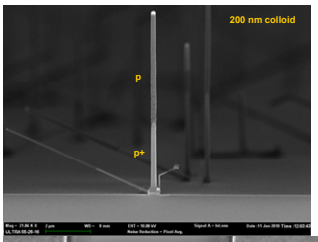


Figure 2.4.5 Si nanowire with a doping gradient.

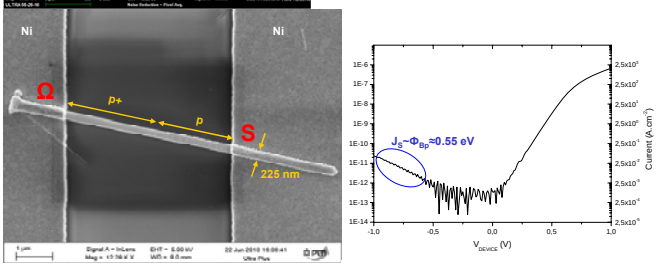


Figure 2.4.6 single nanowire connected between a strongly and lightly p doped ends (left) and corresponding I(V) curve (right).

Single electron memory (UCL, USTUTT)

The objective of this work is to realize a self-aligned single-electron memory (SEM). In order to obtain a long data retention time, single-electron memories with double nano floating-gates (**fig. 2.4.7**) have been fabricated, in which the upper floating-gate is charged/discharged by a few (ideally one) electrons from the MOSFET channel through a double tunnel junction separated by the lower floating-gate. When the size of the lower floating-gate is below 10nm, the quantum confinement and Coulomb Blockade effect induce the splitting of the energy band into a number of energy level at room temperature. The band-offset between the upper and lower floating-gates prevents the charge in the upper floating-gate from returning to the channel, thereby resulting in longer data retention time. In other words, the double floating-gates are analogous to an 'artificial dipole', which is embedded in the gate oxide between the control gate and the MOSFET channel. The electric field surrounding the 'artificial dipole' is weaker than that surrounding the floating-gate in the conventional single-electron memory device. Therefore, the charge can be stored in the upper floating-gate for a long time.

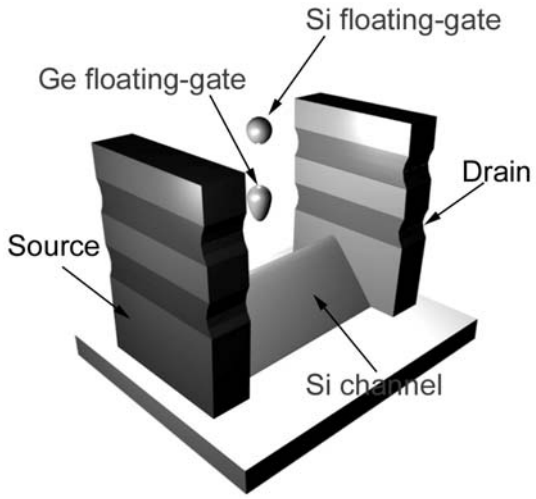


Figure 2.4.7 Schematic view of a self-aligned double floating-gate single-electron memory.

The heterostructure used in this fabrication is composed of a Si/$Si_{0.7}Ge_{0.3}$/Si stack (20/20/50 nm) on a 145-nm thick buried oxide. A
pattern as shown in **fig. 2.4.8a** is then obtained on the heterostructure by lithography and Reactive Ion Etching with a hard mask of silicon nitride. The pattern is composed of a central circle connected to wider source/drain regions by narrow paths. After wet oxidation, the double tunnel oxides separated by the $Si_{0.7}Ge_{0.3}$ layer is formed in the circle as shown in **fig. 2.4.8b**. The reason is that the interfaces between Si and Ge layers have fast etching and oxidation rates. In this case, the tunnel oxides vertically separate the circle region into top Si dot, middle Ge dot and bottom triangular channel, which are used as the upper floating-gate, lower floating-gate and the channel of the present memory device, respectively. The floating-gates are restricted to the central circle since the Si and Ge dots are completely oxidized in the narrow paths (**fig. 2.4.8c**). In the wide source/drain regions, their widths are large enough to avoid the formation of the tunnel oxides in the interfaces (**fig. 2.4.8d**). Therefore, the floating-gates are self-aligned to the channel and restricted in the central region. The structure is doped by arsenic for reducing the resistance of the source/drain regions. This step results in an n-type junctionless nanowire channel. Then a control gate is formed by depositing a layer of polysilicon or Pt layer. To further simplify the fabrication process, we also design the memory device with two side gates.
The hysteretic behavior of the device at room temperature is shown in **figure 2.4.9 a**. When the gate voltage is swept from 0 to 10 V, three shifts are observed, while two back shifts are observed when sweep is reversed. This indicates that single electron is injected into the upper floating-gate. The diameter of the upper floating-gate obtained from **figure 2.4.9 b** is 7.5 nm which is compatible with the Coulomb charging and quantization energy at room temperature so that the memory operation can be performed by one electron only. To further support single-charge injection, the time evolution of the drain current is carried out, in which a negative pulse of 10 V is first applied to empty the floating-gates, then a constant voltage of 8.2 V is set and hold on during the measurements. **Figure 2.4.9 b** demonstrates a typical I_d-t characteristic. When one electron is injected into the floating gate, an abrupt reduction of drain current is observed. The quantization of the current steps, of ΔI_d = 0.3 nA, confirms that they stem from single electron injection in the floating-gate.
To conclude, we have reported a new method for fabricating fully self-aligned double floating gate single-electron memory devices using a Si/ $Si_{1-x}Ge_x$ /Si heterostructure. The fabricated devices have an upper Si nanocrystal floating gate (~5 nm) and a lower Ge nanocrystal floating gate (~20 nm). Both floating gates and the nano-scale channel of the device are fully self-aligned. The size of each floating gate can be precisely controlled by modulating the thicknesses of the Si and $Si_{1-x}Ge_x$ alloy layers. The energy barrier for preventing charge leakage is induced not only by quantum effects but also by the conduction band-offset between Ge and Si, which makes the energy barrier higher and relaxes the limitation of the lower floating gate size. The present memory devices demonstrate a long retention time and a quantized threshold voltage shift at room temperature. They have basically the same write/erase speed as single-electron memories with single floating gate.

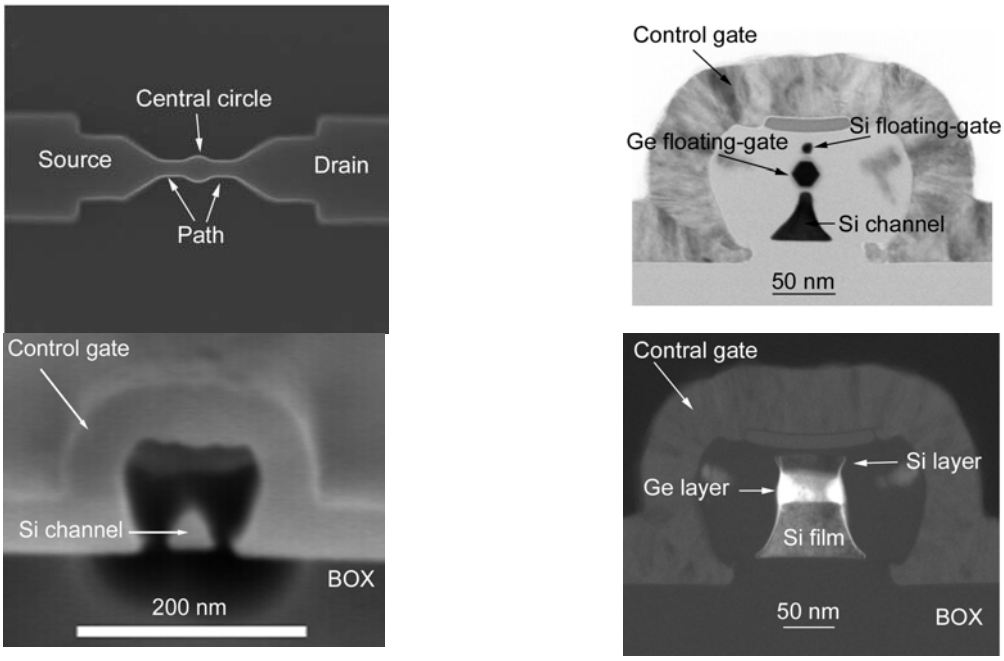


Figure 2.4.8 (a) The top view of the single-electron memories with double nano floating-gate fabricated on the heterostructure. (b) Cross-sectional picture of a SEM device in the centre. (c) Cross-sectional picture of a SEM device in the path. (d) Cross-sectional picture of SEM device in the source/drain regions.

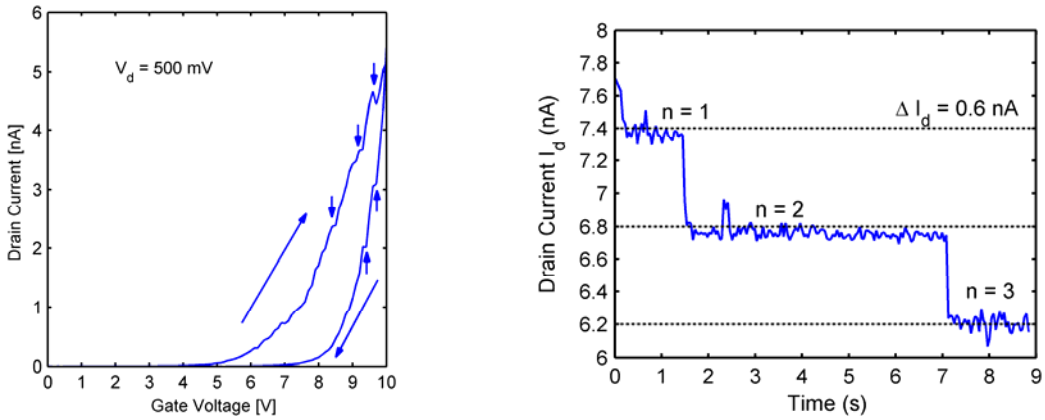


Figure 2.4.9 (a) The hysteretic behavior of a SEM device at room temperature at Vd = 500 mV. Many Id shift can be seen when the gate voltage is swept forth and back. (b) Time evolution of drain current for a constant gate voltage of 8V. The different steps in Id-t are an evidence for single electron injection in the floating-gate.

QD-Tunneling Device and Circuits (USTUTT, Chalmers, IMEL, RWTH, UPS):
Interband tunneling at room temperature, high frequency circuit demonstration

Tunneling is a fast phenomenon and the corresponding negative differential resistance (NDR) I-V curve allows device applications in high frequency and multi-value storage. Ge-dots in Si open that field for Si based nanoelectronics.

Carrier tunneling requires very thin barrier width which results in high capacitance. By the introduction of Single or vertically aligned dot multilayers in the barrier region, the barrier width can be tailored and made wider. Hence the device capacitance is decreased and the high frequency performance is improved. In the case of use of vertically aligned dot multilayers, the layer separation should be small enough to allow carrier tunneling from one dot to the other.

Interband tunneling junctions with a single Ge small QD layer have been fabricated. The device layer structure and the energy band diagram schematic representations are shown in **figure 2.4.10a**. The Ge dot layer is included in the barrier region stacked between two very thin (1-3 nm) intrinsic Si layers. As shown in the AFM image (**figure 2.4.10b**) the QD diameter is below 20 nm. The growth of the dots and capping layer was performed at low temperature (350°C) in order to form pure small Ge dots and to avoid their intermixing with Si.

RT-NDR with Ge-QD was demonstrated. Earlier attempts required high temperature annealing leading to intermixing. **Figure 2.4.10b** shows the current density as function of the applied voltage measured at room temperature. A figure of merit for NDR devices is the peak to valley current ratio (PVCR). For the realized diodes a maximum PVCR of 1.6 has been achieved.
Refined understanding needs knowledge of capture/emission processes. For this a cooperative effort (Chalmers/ Warsaw) in DLTS experiments and Quantum effect based interpretation is performed.

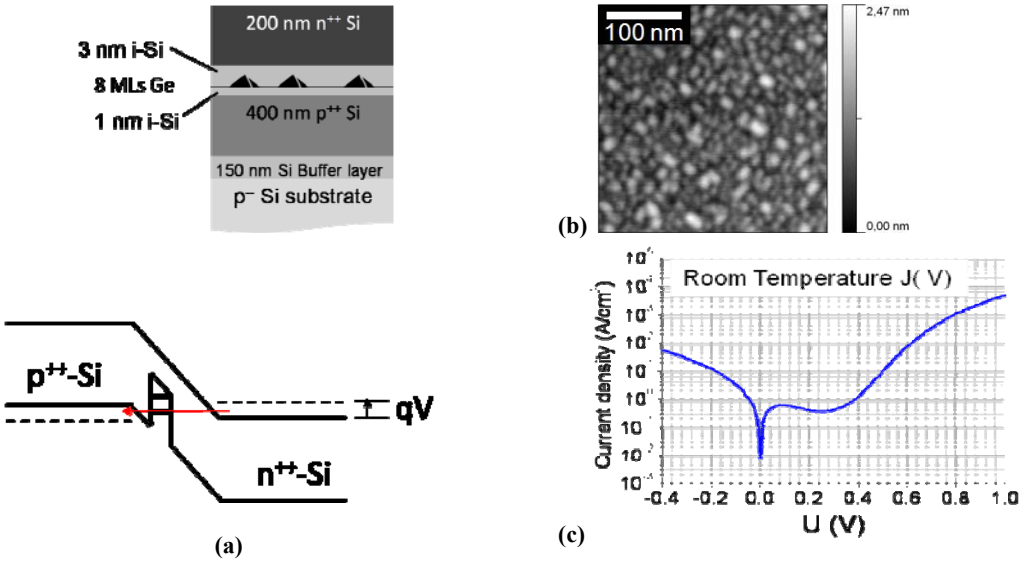


Figure 2.4.10 (a) schematic representations of the structure of interband tunneling junction with a single Ge QD layer and of the corresponding energy band diagram. (b) AFM image of Ge quantum dots obtained following the deposition of 8ML Ge at 350°C by MBE. (c) Current voltage characteristic at room temperature of interband tunneling junction with a single Ge QD layer.

In addition, NiSi Schottky diodes with Ge dots buried below the metal-semiconductor junctions have been fabricated. These diodes have cut-off frequencies up to 1.1THz (calculated from S-parameter measurements up to 110GHz). The implementation of Ge QD Schottky diode in an 89GHz RECTENNA for mm-wave power detection is demonstrated.
The RECTENNA layout is shown in **fig. 2.4.11**. It consists of an antenna unit, a rectifying unit and a filter unit. The antenna unit is formed by an integrated microstrip single patch antenna. The rectifying unit (detector) is made of a radial stub as RF short and a Ge QD Schottky diode which structure is described below. The filter unit is a low pass three stages LC-filter.
The whole RECTENNA is designed in microstrip topology. To suppress resonances within the substrate and to keep attenuation low, the substrate is thinned to a thickness of 200µm.
The antenna operates as a band pass and only its resonant frequency is received. One half of the received signal is shortened to the virtual mass using a radial stub while the remaining half is smoothed by the low pass filter.

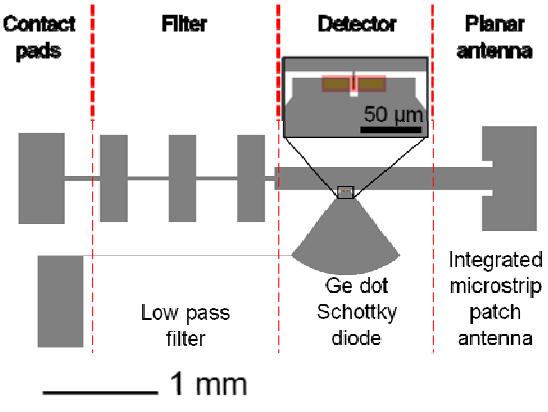


Figure 2.4.11 Layout of the RECTENNA with single patch antenna.

The Schottky diode structures with Ge QDs have been grown by Molecular Beam Epitaxy (MBE). The MBE growth starts by 150nm thick intrinsic silicon buffer layer deposited at 600°C. Then 500nm of an antimony highly doped ($10^{20}cm^{-3}$) silicon layer (HDL) is grown at 375°C. It is used as the ground contact of the diodes. Finally, the so-called Schottky Layer (SL) is deposited. The SL is made of a Ge dot layer stacked between two intrinsic silicon layers which total thickness is 300nm. The dot layer is formed by 6ML of Ge grown at 500°C. The intrinsic silicon layers are grown at 600°C except the first 8nm of the dot capping layer which are deposited at 330°C to prevent QD shape modifications or intermixing with Si. An example of Schottky layer with embedded Ge dot layer at 20nm from the surface is given in **fig. 2.4.12a**.
The dot capping layer thickness in SL is chosen taking into account the Si consumption during NiSi device metallization to obtain the dot layer embedded at the desired distance from the NiSi-Si Schottky junction. **Figure 2.4.12b** shows an example of Schottky layer with embedded Ge dot layer at 40nm from the surface as it can be seen below the oxide where no NiSi has been formed. After the NiSi formation, the dot layer is only at about 7nm from the NiSi-Si interface.

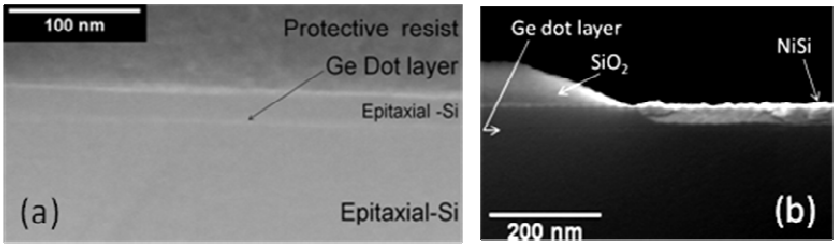


Figure 2.4.12 Cross-section Scanning Electron Microscopy micrographs of Schottky layers (with embedded Ge QDs) near the surface (a) following MBE growth and (b) following NiSi formation and unreacted Ni removal.

Following MBE growth, the integration process in RECTENNA circuit begins. First, the upper mesa is defined by dry etching the Schottky layer outside the mesa area until the HDL is unveiled. Second, the HDL is dry etched down to the substrate outside the lower mesa area which includes the upper mesa. This ensures the isolation of each diode from the others. The etch edges are passivated with SiO_2. Contact holes are then opened by removing the oxide from upper and lower mesa portions for Schottky and ground contacts, respectively. The removal of 90% of the oxide thickness is performed by dry etching. The remaining oxide is wet etched by Buffered HF in order to prevent active layer thickness modification or dry etching induced surface damage. For the formation of the NiSi-Si junctions, a thin Ni layer is sputter deposited then reacted with Si inside the contact windows during an annealing at 450°C (under N_2 ambient) to form NiSi. Outside the contact windows the remaining unreacted Ni is removed. Finally, for the interconnect aluminum is deposited and structured. The resulting Ge QD Schottky diode is schematically represented in **fig. 2.4.13a**.
The Ge QD Schottky diode considered in what follow has a dot capping layer thickness of 25nm. 10nm of Ni has been used for NiSi formation which consumes about 17nm of Si from the cap layer. Therefore, the Ge QD layer is at about 8nm from the NiSi-Si Schottky junction.
In order to extract the series resistance (R_s), the ideality factor (η) and Schottky barrier (Φ_B) DC-IV measurements have been carried out. **Fig. 2.4.13b** shows the DC-IV characteristic of Ge QD Schottky diode having 6µm length and 1µm width. The ideality factor η is equal to 1.05 while the diode saturation current density J_s is equal to $1.4x10^{-4}$ Acm^{-2}. This J_s value corresponds to a Schottky barrier Φ_B of 0.66V. Also, a value of 40Ω for the series resistance (R_s) has been extracted.
Vector Network Analyzer (VNA, Anritsu 3700 system, up to 110GHz) is employed for high frequency characterizations. The diode high frequency cannot be obtained directly but through a de-embedding procedure. New de-embedding procedure proposed recently by H. Xu and E. Kasper in SiRF 2010 has been applied. It uses open and short structures having the same design as the measured diode.
The cut-off frequency is $f_{co} = 1/(2\pi R_S C_0)$. The calculated cut-off frequency of 6µm long and 1µm wide diode is 1.1 THz considering R_S of 40Ω and C_0 of 3.8fF. This f_{co} is only valid when the diode is under Mott operation, i.e. when the full Schottky layer is depleted which corresponds to minimum diode capacitance. Forward biasing the diode above the Mott voltage causes the depletion layer width to shrink and therefore a diode capacitance increase and cut-off frequency decrease. The Mott voltage of the current diode is 0.3V.
In order to characterize the RECTENNA, the Vector Network Analyzer (Anritsu 3700 system) and a horn

antenna are employed as power source and as radiation element, respectively (**fig. 2.4.14-a**). A Keithley 2400 Digital SourceMeter is used to supply a biasing current and to measure the output DC voltage. The conversion voltage ΔV is measured as follow. At a given biasing current in the RECTENNA, output voltages are measured without (V_0) and with (V_{RF}) RF power radiation from the horn antenna. Then ΔV is obtained as the difference between V_{RF} and V_0. **Fig. 2.4.14-b** shows the measured conversion voltage as a function of the frequency at a fixed biasing I=10μA. The frequency dependence of the conversion voltage demonstrates clearly the detector function. The middle frequency (89GHz) and half width of the detector are mainly defined by antenna dimension.

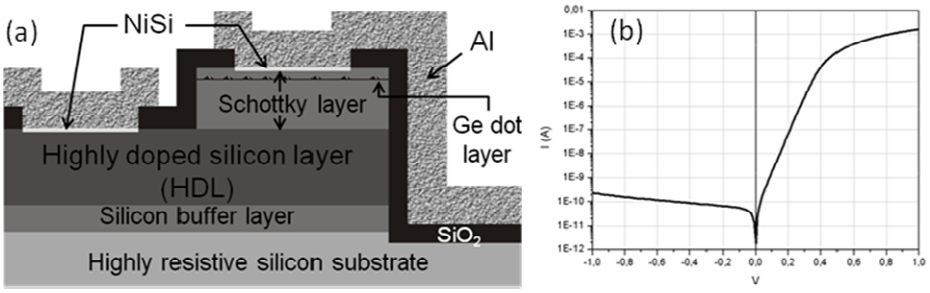


Figure 2.4.13 (a) Schematic representation of Ge QD Schottky diode. (b) DC-IV characteristic of Ge QD Schottky diode having 6μm length and 1μm width.

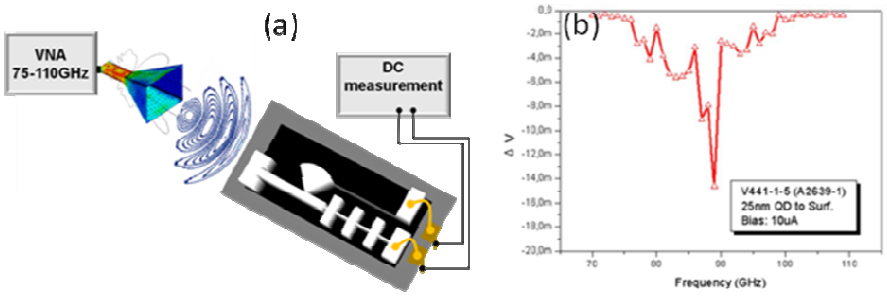


Figure 2.4.14 (a) Schematic representation of the measuring setup for the RECTENNA. (b) Conversion voltage of the RECTENNA as a function of RF radiation frequency.

Carrier capture / emission from Ge QD

When quantum dots (QDs) are used as electronic device elements, information about capture and emission mechanisms is important for achieving a detailed structural design. Influences of thermal and tunneling processes in relation to the distributions of confined energy states and charging effects are crucial for such applications.

In the present investigations, two types of structures were prepared, which differed with respect to the conditions of the Ge-layer deposition and capping processes. In the first group, the Ge layer was deposited at 550°C at a growth rate of 0.2 ML/s using a two-step process for the capping, including a first 5 nm thick Si:B cap layer grown at 330°C followed by deposition at 600°C to approach a final thickness of 400 nm. In order to have the QDs placed in a depletion region for DLTS investigations, Schottky diodes were prepared by evaporating Al dots on the cap surface. By the same reason, structures of the second type were made as n^{++}-p-p^{++} junctions. Here, the Ge layer located in the p-type Si was 125 nm below the n^{++}-Si:Sb layer. Both the Ge and p-Si layers were grown at 350°C, whereas a 200 nm of n^{++}-Si was deposited at 431 °C. In both cases, QDs were formed from an 8-ML thick Ge layer.

Deformation in Ge (3.3-ML)/Si quantum well (QW) structures of the first type has been characterized by HRTEM and DLTS. Strain distribution in the QW and a modulation in the Ge layer dark contrast were investigated in terms of QW thickness variation. DLTS spectra plotted as contour maps on a reverse voltage (V_R) versus temperature (T) plane reveal large variations of the energy level distributions in the QW across the wafer area. The developed method can be used as a tool for diagnosis of QW uniformity.

MOS on buried Ge stressors (USTUTT, Cooperation with WP3)

The effect of Ge dot layer buried in the channel region of a MOSFET is investigated. MBE growth (USTUTT) of reference and buried Ge dot layers (4 wafers, **fig. 2.4.21**) for both n- and p-type MOSFET have been performed. The QD layer as a stressor is placed 10 nm below the channel. The structure is retrograde doped to allow for a low channel doping. The depth of the QD (**fig. 2.4.21**) was set back to 10nm from the surface, to allow small Si removal by processing. The lateral size of the Ge dots (15 nm) was chosen smaller as the applied gate length so that a mean value for the stress effect will be measured. Size of the dot and its Ge content can be tailored by the growth conditions. Here we used a low growth temperature (350 °C) to get pure Ge dots. Earlier investigations with higher growth temperatures resulted in SiGe dots because of intermixing of Ge atoms with the underlying Si substrate atoms. The doping (10^{18} cm^{-3}) was set back 50nm from the surface to allow for diffusion during processing. B and Sb (Sb is a slow diffusing species) were used as dopant atoms for p-type and n-type doping, respectively. Uniform doping levels and abrupt junctions were obtained by specific dopant incorporation techniques (pre build up, flash off of adatom layers). The processing of the devices is performed and reported within WP3.

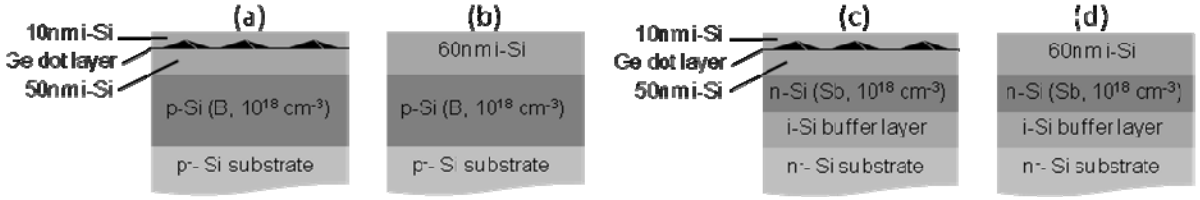


Figure 2.4.21 Schematic representations of the layer structures for (a) n-MOS and (c) p-MOS with buried Ge stressors and for reference (b) n-MOS and (d) p-MOS devices. The doped layer below the channel is grown as step doped (10^{18} cm^{-3} at about 50 nm below the channel). After implant anneal this should result in a retrograde doping with low doped channel and increasingly doped well.

Assessment of manufacturing potential

Self-organized structures offer a rich variety of shapes and geometries which are claimed to be useful for nanoelectronics for mainly two reasons:

- Novel or improved electronic and photonic properties. This is caused by size and shape dependent quantum effects and by the specific surface and interface quality of self-organized created nano-objects. These follow a route which is frequently dictated by free energy minimization. A famous example is the three-dimensional (3D) formation of quantum dots from lattice mismatched materials. Layer formation and etching will result in an interface with a misfit dislocation network if the layer thickness is above a critical thickness. Self-organized growth follows a 3D mode with pseudomorphic (dislocation free) interface but higher stress values.

- Reduction of critical process steps in conventional device fabrication or even design of a new manufacturing paradigm for nanoelectronic integrated circuits. The first idea is rather straightforward, its successful implementation will depend on compatibility aspects with already existing conventional manufacturing. In this specific network activity we focused on the latter topic of a new manufacturing paradigm. The group brought in a broad background knowledge of different nanostructures, a European sight on research potentials and manufacturing efforts, and a strong emphasis on the need for a complete chain from nanoelectronics to information and communication products.

The Paradigm of Self-Organized Nanoelectronic Manufacturing

In conventional manufacturing a nearly unbelievable progress in lithography allowed the radical scaling of device dimensions and the tremendous increase in integrated circuit complexity. The Europeans are underrepresented in this market although they invented essential processes to pave the way to the existing status.

Europe has to come up with nanoelectronic manufacturing models otherwise we will be cut from modern growth areas like information and communication.

We propose to ground on self-organized structures for the future scaling of device dimensions.

Targeted manufacturing is based on minifabs which increase flexibility for new products, reduce the time frame to mass production, and minimize investment costs.

Within this network we explored technical routes, we identified roadblocks and technical challenges, and we suggest directions of future efforts.

Technical Routes and Challenges
Details of the different routes are given in the technical reports. Here we summarize the categories.

- Silicon nanowires grown on predefined dots. Main progress was shown in using CMOS compatible materials (silicides) and in templated deposition of starting dots (electrophoresis on given S/D metal). Roadblocks could be given by the need for lateral wire growth in predefined directions.

- Subtractive Si/ Ge wire and dot formation by templated etching and oxidation processes. This process is highly compatible with conventional processing tools. Single electron demonstrators could be realized. Technical challenges are process control and interface quality.

- Silicon dots embedded in oxide. Strengths of this method are small sized dots (2-5nm) and easy fabrication. Roadblocks for nanoelectronics are the low on-currents and their variability caused by the tunneling through the embedding oxide. We see application potential outside in photovoltaics because of the extended and tunable bandgap.

- Germanium dots in Si produced by Stransky-Krastanov (S-K) growth. High Ge content and small dot size was realized by low growth temperatures in prepatterned oxide windows. Self-organized prepatterning with Si technology compatible materials was demonstated. We call a sequence of selforganized processes coupled selforganization.

Table 1: Assessment of investigated methods

Method	Si wire growth	subtractive wire/dot	Si dot in oxide	Ge-dot
Roadblocks	lateral wires	-	on-current	-
Challenges	seed	interface	variability	size
Prospects	FET	single electron device	photovoltaics	high f

Recommendations
Fabrication schemes following a deterministic patterning dominates now completely microelectronics manufacturing. Far East region benefitted most, Europe least from these manufacturing routes.
For improving Europe´s competition position research in a different manufacturing route is advised.
This new manufacturing paradigm is based on coupled self-organization processes for future aggressive nanopatterning. By this measure the investment volume increase will be stopped, allowing smaller plants (minifabs) and higher flexibility to introduce different products.
Research on new self-organized manufacturing routes should be intensified. Recommended routes are based on templated nanowire/-dot formation from subtractive processing and S-K growth.

Conclusion and Outlook
Progress in NW transistor fabrication (CMOS compatible seeds), in successful realization of SEM (with single charge injection into the floating gate) and in Ge QD devices (RT- NDR device, QD Schottky diode)/circuits (89GHz RECTENNA) and characterizations has been reported. Moreover, the manufacturing routes using the different self-organized processes investigated in this project (FSP2.4 “Templated Self-Organization”) have been assessed with respect to their roadblocks, their challenges and their prospected application fields.

- ***WP3:*** Within WP3 a substantial amount of work has been performed in order to integrate process modules developed within the FPs into the MOSFET process line of the JPP. Results from this work includes research results as described in the joint publications by the partners but also development of the process modules and tailoring of the MOSFET process line in the JPP in order to integrate new materials and/or new architectures. The integration work has been performed in a close connection with the planning and execution of the MOSFET batches within WP3. First a condensed description of the integration work is provided

followed by description of the batches of MOSFETs fabricated within the JPP of NANOSIL. An extensive description of the integration work and the batches can be found in deliverable D3.2, D3.3, D3.4 and D3.5.

Development of process modules
The process modules that was incorporated in MOSFET batches were 1) sSOI on standard wafer size in JPP, 2) $LaLuO_3$/TiN gate stack, 3) SB source/drain (S/D) contacts, 4) extremely low temperature (T_{max}<450 °C) MOSFET process for strained Ge channels (described in sGe batch below) and 5) a gate last process for long channel devices (T_{max}<150 C).

sSOI on the standard wafer size in JPP
Strained silicon on insulator (sSOI) wafers was delivered to the consortium by SOITEC. The wafer size was 200 mm and the top Si layer was strained 1% (20% Ge equivalent). The buried oxide was 145 nm thick and the silicon thickness was 15 nm. These wafers were used in the JPP batches processed for the FPs.. In the JPP the standard wafer size is 100 mm and integration work was conducted to use 200 mm sSOI wafers as starting material. The sSOI wafers were thinned and resized with major wafer flats for use in 100 mm semiconductor tools. Each 200 mm wafer yielded two 100 mm wafers. A significant result is that the resize process has been qualified and is used within the JPP for all starting material on 200 mm wafers such as SOI, sSOI and sGe on virtual substrates.

Integration of LaLuO3/TiN gate stack
During NANOSIL several experiments and batches has been performed to adopt the MOSFET process line and the LaLuO3/TiN deposition for successful integration in the JPP platform. An improved MESA isolation technique was developed to reduce possible gate leakage due to non-conformal MBE deposition of LaLuO3. A chemical oxide process was developed and inserted before MBE growth and was shown to reduce gate leakage. The JPP MOSFET process was designed to accommodate a relatively low temperature (Tmax<700 °C) process after LaLuO3/TiN deposition since it is known that high temperature processing is detrimental to the performance of the gate stack. The integration work included the formation of thin spacers, formation of low resistance SB S/D contacts and finally adoption of a low temperature contact hole and metallization process. At the end of NANOSIL a gate last process was developed in order to be able to fabricate LaLuO3/TiN MOSFETs with an extremely low (T<150 °C) temperature process that allows the evaluation of the temperature budget of the gate stack. Source/drain implantation and activation was performed before the gate stack using a dummy gate as mask. Patterning of the high-k/MG stack was aligned to S/D implants using I-line lithography and a 0.1 µm gate to S/D overlap. The gate last process enables fast (<1 week) fabrication of MOSFETs after high-k/MG deposition

SB S/D contacts
The dopant segregated SB S/D technology researched within FP1.2 was integrated as a S/D technology in the JPP. Dopant segregation of B and As was employed to modulate the effective barrier height of PtSi close to the conduction (As) and close to the valence band (B). PtSi was placed in close proximity of the inversion channel by the use of thin oxide/nitride (t_{TEOS}=5 nm/t_{SiN}=10 nm) spacers (see Fig. 2). The DS SB contact processes yielded an R_{SD} of about 1 kΩµm on NMOSFETs (see Fig. 3) on fully depleted SOI with As segregation (at 700°C drive in) in PtSi. The developed process module was used in several batches of the JPP for PMOS and NMOSFETs.

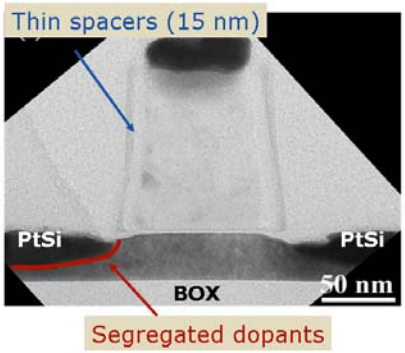


Fig. 2 XTEM of dopant segregated PtSi Schottky Barrier MOSFET on SOI. The thin spacer process was developed within the JPP.

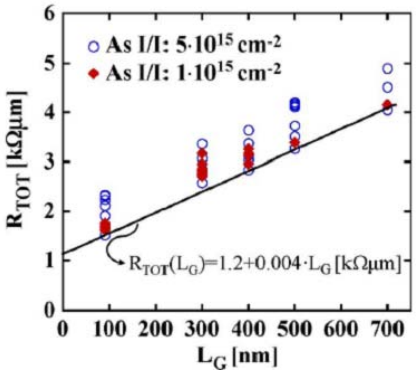


Fig. 3 The integrated low temperature process yields a R_{SD} of about 1 kΩμm for NMOSFETs

Processed batches within the Joint Processing Platform

Batches with LaLuO3/TiN and DS SB contacts

In total 4 batches with $LaLuO_3$/TiN gate stack were processed with the JPP of NANOSIL. Three of them had the DS SB contacts integrated and one of the used conventional implanted S/D with a gate last process. Batch 2 (bulk-Si) and batch 3 (SOI) was the first batches the used the $LaLuO_3$TiN gate stack developed in FP1.3 and the DS SB contacts from FP1.2. Device processing was conducted at KTH and MBE deposition of $LaLuO_3$ and PVD of TIN was performed at Julich and AMO, respectively. The SiO_2 references showed almost 100 % yield and from the device characteristics it was estimated that R_{SD} was below 1 kΩμm. The excellent uniformity achieved for both for NMOS and PMOSFETs on bulk-Si and on SOI wafers showed that the low temperature DS SB PtSi process can be used both on bulk-Si and SOI. Batch 2 and 3 also showed that gate leakage was drastically increased if $LaLuO_3$ was deposited directly on an HF last Si surface. With a 5 nm thick SiO_2 layer between $LaLuO_3$ and the Si channel the gate leakage was as low as for the SiO_2 references and the yield was almost 100%. Clearly a thin interlayer (to achieve low EOT) was needed between the $LaLuO_3$ and the Si channel. A chemical oxide was developed for this purpose and inserted in batch 4.

The aim of the batch 4 was to integrate the $LaLuO_3$ improved with a chemical oxide interlayer and DS SB contacts on 60 nm gate length sSOI. The starting material was 200 mm SOI and sSOI wafers from SOITEC. The wafers were resized to fit the standard wafer size within JPP. The BOX was 145 nm and silicon thickness (t_{Si}) was 20 nm for SOI and 15 nm for sSOI. Fig. 4 shows a schematic cross-section of the device. The Si channel was fully depleted for both strained and unstrained devices. Table I depicts the experimental split between the devices.

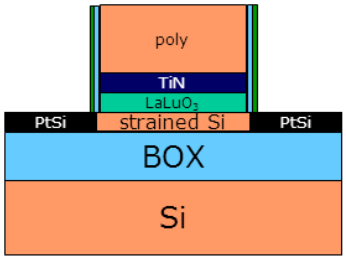


Fig. 4 Schematic ross-section of FD sSOI with DS SB contact and high-k/MG

Table I Split of wafers in batch 4

Strain [GPa]	*$LaLuO_3$ [nm]*	*SiO_2 [nm]*
1.4	*3*	
1.4	*6*	
1.4		*4.4*
0	*3*	
0	*6*	
0		*4.4*

During the gate pattering the hard mask was unfortunately not cleared properly and this lead to poly-Si/TiN residues along the gate edge and partly non cleared gate material. In an effort to save the wafers an extended gate etch was performed that cleared the residues but it also degraded the integrity of the S/D areas and consequently to a non-uniform PtSi and dopant segregation process. Although working 60 nm devices were found the drain current scattered too much (due to non-uniform parasitic S/D resistance) for any reliable interpretation of the results. Instead characterization were extensively performed on long channel devices

(L=10 µm). The reference (SiO_2) SOI wafer had 80 % yield on PMOS and 70 % yield on NMOS. For wafers with $LaLuO_3$ acceptable uniformity and yield was achieved for PMOSFETs but NMOSFETs had virtually zero yield. Extensive characterization of the PMOSFET uniformity was conducted and here only the representative characteristic is presented. The insertion of a chemical oxide was successful and CET was 4.4, 2.8 and 2.0 nm for SiO_2, 3 nm $LaLuO_3$ and 6 nm $LaLuO_3$, respectively. Fig. 5 shows I_{dlin} and $LaLuO_3$ devices exhibits a higher g_m compared to the reference. A significant result was that the hole mobility was not degraded in $LaLuO_3$ devices (μ_{hole}=62-68 cm^2/Vs for both reference and $LaLuO_3$ devices). The higher g_m and improved sub-threshold slope (see Fig. 6) of the $LaLuO_3$ devices are due to the reduced CET and non-degraded mobility. As expected PMOS devices were not affected by tensile biaxial strain in the Si channel (see Fig. 7). sSOI is expected to improve the NMOSFETs. Unfortunately (except for 70 % yield on the SiO_2 ref.) no working NMOSFETs was found on the wafers. All 100 NMOSFETs on all wafers have been measured. Previous work in FP1.3 had showed working long channel NMOSFETs on sSOI with a process that had a maximum temperature of 450 °C. Therefore a gate last process was developed and 4 wafers with $LaLuO_3$/TiN were fabricated to study the effect of temperature on NMOSFETs. Unfortunately the first of these wafer showed a substantial gate leakage (both for PMOS and NMOS) and so far the JPP has not been able to reproduce the results from FP1.3.

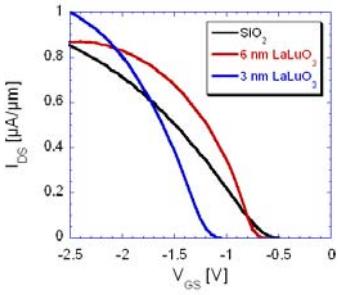


Fig. 5 I_D-V_G characteristics of representative $LaLuO_3$ devices on SOI.

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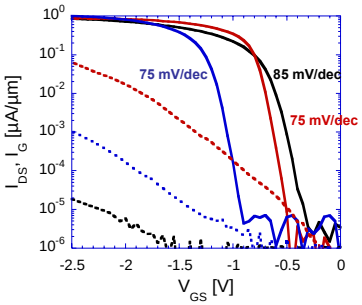

Fig. 6 $LaLuO_3$ devices exhibit an improved sub-threshold slope compared to SiO_2 ref. indicating low D_{it}.

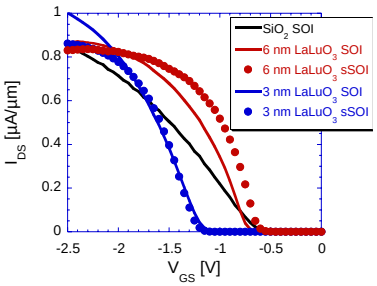

Fig. 7 LaLuO3 PMOS devices are not degraded by the tensile biaxial strained Si channels (sSOI).

Strained Ge channel PMOSFETs

Strained Ge (sGe) is a promising material for enhancing performance of PMOSFETs and up to 4 times higher mobility compared to strained Si MOSFETs has been reported. Within the JPP epitaxial growth of high quality, compressively strained Ge layer heterostructures on a Si (100) substrate has been demonstrated by industrially compatible RP-CVD and a threading dislocation density of 2 x10^6 cm^{-2} has been achieved. The maximum thickness of sGe layer that could be grown while maintaining full strain depended strongly on the growth temperature. For the sGe PMOSFT batch an optimized growth temperature of 400 °C and 20 nm thick sGe was used. Fig. 8 shows a schematic cross-section picture of the reverse graded SiGe virtual substrates and the sGe layer on top. The sGe layer was fully strained according to XRD and smooth surfaces were obtained with an rms surface roughness of just 2.2 nm. The JPPs MOSFET process was adopted to have a maximum temperature of 450 °C to ensure fully strained Ge after device processing (see Fig. 9). In order to control short channel effects and avoid ion implantation with associated anneals for damage repair the layers were in-situ doped during the growth. A total of 24 200 mm Ge wafers were grown for the JPP.

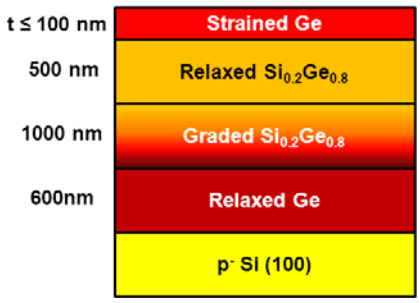

Fig. 8 The reverse graded SiGe virtual substrates with sGe layer at the top.

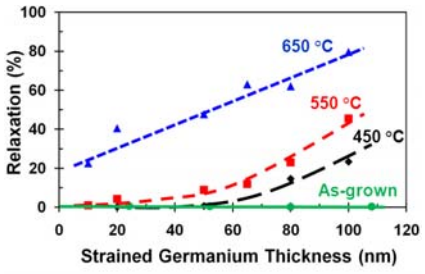

Fig. 9 train relaxation after 10 min H_2 annealing at various temperatures. Relaxation was determined by XRD

To take full advantage of the increased hole mobility of sGe PMOSFET the issue of passivation of the Ge channel surface in direct contact to a high-k gate dielectric has to be addressed. To avoid the formation and volatilization of GeO a low temperature passivation method was developed in combination with the formation of a high-k dielectric gate stack. Different oxidation treatments were applied to form a thin GeO_2 passivation layer using either an ozone-based (O_3) or and atmospheric pressure oxidation (APO) step. The oxidation temperatures applied were in a range from 400 to 450°C. Afterwards a high-k dielectric layer of Al_2O_3 was deposited by ALD at 200°C followed by ALD TiN at 350°C. Fig. 10 shows the results of capacitance-voltage characteristics of the structured high-k metal gate capacitor stacks after dry etching. The layer structure consists of the relaxed Ge substrate described above, the thin APO GeO_2 interface passivation layer and the adjacent ALD Al_2O_3 capped by ALD TiN. The findings of the different low temperature oxidation processes for the formation of the GeO_2 interface passivation layer are shown in Fig. 11. It was found that the atmospheric pressure oxidation is advantageous compared to the ozone oxidation treatment of the Ge surface, leading to low interface trap densities D_{it} near midgap of ~ $4 \cdot 10^{11} eV^{-1} cm^{-2}$, whereat the ozone treatment resulted in D_{it} of ~ $6 \cdot 10^{11} eV^{-1} cm^{-2}$. After the structuring of the TiN metal gate SiN spacers were formed and S/D region was opened be selective wet etch of Al_2O_3.In order to implement an implant free low temperature PMOSFET germanides were evaluated as metallic S/D. Germanides offer the required low formation temperature as well as a low sheet resistance.

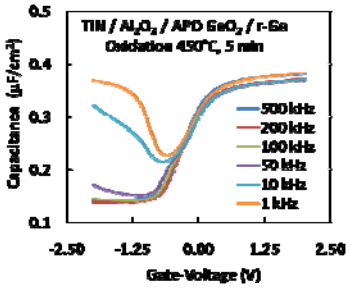

Fig. 10 CV of TiN/Al_2O_3/APO GeO_2/rGe MOS gate stack. The formation of GeO_2 in O_2 atmosphere was applied at 450°C for 5 minutes.

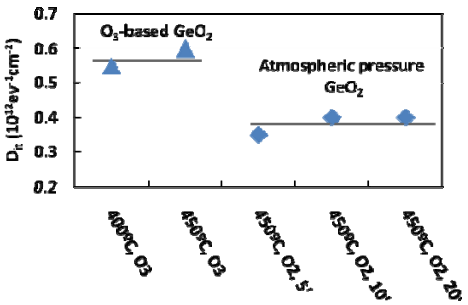

Fig. 11 Interface trap density for O_3 or O_2 oxidation prior to the deposition of 10 nm ALD Al_2O_3..

The formation of S/D contacts was investigated in more detail to compare different promising material candidates of nickel-germanide (NiGe), platinum-germanide (PtGe) and palladium-germanide (PdGe). These germanides were formed during vacuum annealing with investigated formation temperatures ranging from 150 to 350°C. A low resistivity phase at formation temperatures at or below 300°C in case of NiGe and PdGe and at or below 325°C in case of PtGe is found. Fig. 12 shows the influence of the annealing temperature on the measured sheet resistance on either 25 nm Pt, 25 nm Pd or 30 nm Ni deposited on the relaxed Ge surface. Fig. 13 summarizes these results in more detail giving the formation temperature as well as the respective sheet resistance of the lowest resistivity phase observed. For the metal Ni experiments on the selective etch removal were successfully performed. In order to remove the unreacted Ni metal from the wafer surface layer a selective wet etch using diluted HCl was applied. Although all formed germanides additionally offer the required low contact resistance to the p-type channel, we find that NiGe is the most promising candidate to be

implemented into the S/D region of Ge p-MOSFET devices due to its readily available selective wet etch process.

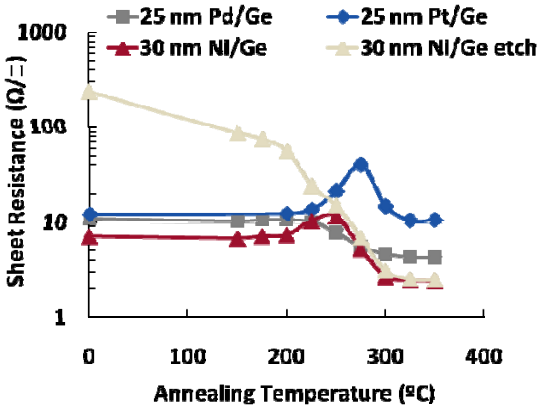

Fig. 12 Sheet resistance (R_s) of 25 nm Pd, Pt or 30 nm Ni deposited on Ge as function of vacuum annealing temperature. Additionally, R_s of NiGe after selective wet etching is also plotted.

	T_{Form} (°C)	Sheet resistance (Ω/□)
PtGe	~ 325	10.5 (25 nm)
PdGe	~ 300	4.2 (25 nm)
NiGe	~ 300	2.4 (30 nm)
NiGe etched	~ 300	2.5 (30 nm)

Fig. 13 Summary of experiments for the formation of source and drain regions used in the self-aligned process flow.

The results of the process optimization show that the demonstrated process scheme allows a suitable low temperature integration of the devices with relaxed rGe and sGe wafers, taking advantage of the low temperature processes applied. Furthermore, the highest process temperatures of 450°C applied in the process flow, will maintain the full strained Ge top layers in case of sGe. In the JPPs sGe PMOSFET batch there are 2 sGe wafers and 2 relaxed Ge wafers ($5{\cdot}10^{16}$ or 10^{18} cm^{-3} channel doping) that have the developed APO/Al_2O_3/TiN gate stack and NiGe as source/drain contacts. At the time of writing this report contact hole formation and metallization is left to process before complete MOSFETs are available. The JPP will continue developing the sGe process using that material grown with NANOSIL.

MOSFETs with buried Ge stressors

In WP2 a technology to locally strain Si has been developed. Small range (5-20) nm strain fields are introduced in Si by embedding Ge islands in Si. This locally strain Si was used as starting material for NMOS and PMOSFET fabrication within the JPP. The aim was to study the influence of the small range strain fields and Ge dot quantization levels on mobility and threshold voltage in MOSFETs. MBE growth of reference and buried Ge dot layers (4 wafers, Fig. 14) for both n- and p-type MOSFET have been performed. The Ge dot layer as a stressor is placed 10 nm below the channel. The lateral size of the Ge dots was 15 nm so the mean value for the stress effect was measured at fabricated gate lengths. A low growth temperature of 350 °C was used to get pure Ge dots. B and Sb (10^{18} cm^{-3}) were used as dopant atoms for p-type and n-type doping, respectively.

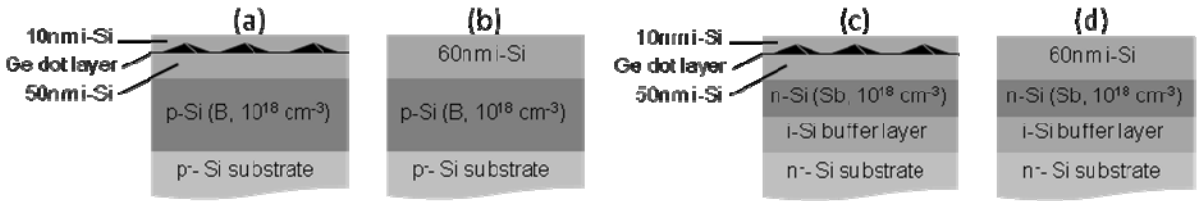

Fig. 14 Schematic representations of the layer structures for (a) n-MOS and (c) p-MOS with buried Ge stressors and for reference (b) n-MOS and (d) p-MOS devices. The doped layer below the channel is grown as step doped (10^{18} cm^{-3} at about 50 nm below the channel).

After a low temperature (400 °C) isolation scheme 4.2 nm SiO2 gate oxide was grown followed by CVD deposition of heavily doped poly silicon. The gate was patterned and oxide/nitride spacers were formed followed by S/D implantations (PMOS: Boron 2·1015 at 10 keV, NMOS: Phosphor: 2·1015 cm-2 at 30 keV). Activation of S/D implants was performed at 900 °C for 30 sec. Metallization consisted of 20 nm NiSi formed

at 450 °C, contact hole formation and TiN/Al deposition and patterning and FGA ended the processing. Processing started Nov. 2010 and finished Feb. 2011. Initial measurements show working PMOSFETs and NMOSFETs with Ge dots in the channel. The wafers are currently evaluated electrically by partners from WP2 and WP3.

Rsd of DS SB MOSFETs on sSOI
Flagship Project 1.2 devoted to DS SB contacts has investigated techniques to reduce the SBH between the metallic S/D and the channel of the MOSFET. Results on diodes have been achieved for different silicides, dopants, strained/unstrained Si and process temperatures. It has been shown that it is possible to achieve low SBH below 0.1 eV and that strain in Si aids in reducing the SBH further. However the real important parameter for devices is the excessive source/drain resistance (Rsd) associated with the S/D contacts. Because of the low resistivity of the silicide used as metallic S/D contacts Rsd is dominated by the effective SBH between the metal and the channel of the MOSFET. The aim of the last batch within JPP of NANOSIL is to measure Rsd in DS SB MOSFETs with short gate lengths of 60 nm. The short gate length device is needed in order to measure low Rsd. The batch was delayed because partners within NANOSIL had difficulties deciding whether the LaLuO3/TiN gate stack would be used or not. Initially the ambition was to be able to make 60 nm gate length devices with good electrostatic control with the LaLuO3/TiN EOT of 1 nm. Because of the uncertainty in the repeatability of the LaLuO3/TiN gate stack it was finally decided to use SiO2 (EOT=4.2 nm) with the main purpose to provide accurate Rsd measurements for FP 1.2. The batch was started in the last phase of the project and it is anticipated that electrical results will be available at the final NANOSIL review meeting in May.

- ***WP4:*** WP4 is organized in five tasks. The main results achieved in each task are reported below.

Task 4.1 (Benchmarking of modelling approaches and simulation tools)
Deliverable 4.1 defines the template devices for benchmarking simulation models and includes template MOSFETs (32 nm and 22 nm gate length Bulk and Double gate MOSFETs and nanowire MOSFETs). Several devices were defined in collaboration with the fabrication Partners of WP1 and WP2 to ease the goal of model validation, calibration and comparison with experiments.

A new method for the 1D deterministic solution of the Boltzmann transport equation has been conceived and tested: we first solve the coupled Schrödinger–Poisson equations to extract the profiles of the 1-D subbands along the channel; next, the coupled multisubband Boltzmann equations are tackled. The deterministic solution allows to obtain smooth carrier-distribution functions on a range of several orders of magnitude. Some peculiar features of the low-field mobility as a function of the wire diameter and gate bias have been discussed and justified based on the subband energy and wave-function behavior within the cylindrical geometry of the investigated nanowire.

New solution method for 1D quantum transport with full subband shape taken into account: the band-structure effects on the transport characteristics of ultrascaled silicon nanowire (SNW) FETs have been accounted for by means of a new approach for the solution of the open boundary Schrödinger equation in the SNW. The model has been validated by comparison with 3-D atomistic simulations based on the tight binding approach, and simulation results are compared with a simpler effective-mass model with either constant and fitted (not bulk-like) transport effective masses.

The simulation of advanced nanometre scale MOSFETs and the investigation of new device architectures is nowadays a very challenging task, because technology is exploring a large number of technology options not considered so far during the development of previous ITRS technology nodes.
For most of these options (SOI and UTB substrates, non-conventional crystal orientation of the channel material, high-k dielectric, metal gate, strain, etc….) no established models are available and actually it is not even clear what will be the most appropriate modelling approach to calculate device characteristics for such nanoMOSFETs.
In this framework, the device modelling community is challenged to provide predictive simulation capabilities to technology developers, in order to reduce the technology development effort and cost.

Such tools are required to address the typical issues of transport at the nanoscale: i) partially ballistic transport, which is very far from the realm of validity of the drift-diffusion model, ii) quantum confinement in the channel, which alters both electrostatics and scattering rates, and iii) source-to-drain tunneling, which affects not only subthreshold behaviour but also the on-state current.

Different groups are pursuing different modelling approaches to cope with these difficulties (Conventional Drift Diffusion with Density Gradient Corrections, Quantum Drift Diffusion, NEGF, conventional Monte Carlo, Multi Subband Monte Carlo, Wigner function solvers, etc…) but no winning approach has been found yet. The degree of maturity of nanoMOSFET modelling is such that none of the available models is able to cover all the technology variants currently under investigation. It is therefore of extreme importance to be able to compare on a fair basis the different models in order to establish the relative importance of the different model approximations made.
Deliverable D4.3, compares the results obtained by a first category of simulation approaches (semi-classical) approaches including Quantum Drift Diffusion, conventional Monte Carlo, Multi Subband Monte Carlo in terms of low-field mobility and trans-characteristics Ids(Vgs) at low and high Vds; internal quantities as inversion charge and carrier velocity along the channel are presented as well. The structures adopted for such comparison are the template devices (that is, idealized transistor structures representative of the forthcoming technology nodes and suitable to be simulated with all available models) described in the Nanosil Deliverable D4.1. The simulated devices were five MOSFETs with gate length ranging from 32 nm down to 16 nm and two Silicon nanowire FETs.
The five different Monte Carlo (MC) device simulators gave very consistent results. The differences are mostly rather small for the SOI–FET with quantum effects having a minor effect on threshold voltage due to the lowly doped channel, while the two multi–subband MC simulators show some prominent deviations in the case of the DG–FET. High-k mobility degradation by remote phonon scattering (RPS) in free carrier
MC approximation leads to smaller performance degradation compared to multi–subband MC with remote Coulomb scattering (RCS) and RPS, but requires further investigations.
Results were presented at the at the 14th International Workshop on Computational Electronics (IWCE-14) Conference in 2010.

A more comprehensive set of tools, including full-quantum models, and more aggressive template devices, including those representative of the 16nm node, have been tested and compared during the third year of the project and the results presented in D4.6.
In order to be able to ascribe differences in electrical characteristics to differences in the adopted models or in implementation, we have first aligned the considered codes from the point of view of electrostatics simulation, by modeling devices at zero drain-to-source voltage, and ensuring excellent agreement in the charge and potential profiles obtained. After this necessary step, we have investigated both low-field and large-bias transport. Differences in simulation results obtained when using different models can be directly linked to differences in the transport model adopted. A few issues clearly emerged: First, source-to-drain tunneling is extremely important both for the 10 nm double-gate MOSFET and for the 6 nm nanowire FET, especially in evaluating the subthreshold behavior. Not considering tunneling and wave function penetration in the gap can result in the inability to recover the actual subthreshold behavior.
As a second point, all transport models consistently point out that scattering with phonons, impurities, and surface roughness, bring all considered devices far from fully ballistic transport. Even in the case of the FET with 6 nm channel length, the cutoff frequency of the intrinsic device (i.e., excluding parasitic capacitances) is cut by roughly a factor two when the main scattering mechanisms are considered, but still above the THz range.
Furthermore assumptions on the scattering mechanisms are apparently at least as important as the adopted transport model. Indeed, differences among results obtained with different transport models are limited from a qualitative point of view: by performing different calibrations, all transport models considered should be able to provide the same current-voltage characteristics.

A colaboration between IU.NET and KTH is devoted to the modeling of MOSFETs with metallic S/D. On one side, simple 1D models and drift-diffusion simulations are used to obtain a better understanding of the Shottky barrier lowering associated to dopant segregation. On the other side, Shottky barrier contacts have been implemented in a Multi-subband simulator, using a simple approach (based on the effective potential) to

account for tunneling across the image force lowered Shottky barrier. In particular, in the framework of Task 4.1, the developed model has been used to compare the current drive of the 32nm nanosil template with devices featuring the same silicon film thickness, gate length and gate stack, but with metallic source and drain. It has been found that very low Shottky barrier heights (below approximately 50meV) are needed in order to obtain an On-current comparable to the one of a doped source/drain device. Otherwise, the current is strongly limited by electron injection at the metal/semiconductor interface. Results have been interpreted based on a the well-known Lundstrom model for quasi-ballistic transport. Results were presented at the ULIS 2010 conference.

Finally, for the first time device simulations of p-MOSFETs have been performed by solving the multi-subband Boltzmann Transport Equation including the 2D carrier confinement with realistic scattering processes for the 6x6 k.p band structure, without band structure approximations. Theses simulations demonstrate that the simultaneous solution of kp-SE, PE and BTE is possible for realistic devices with TCAD like properties concerning convergence speed and numerical precision.

TASK 2 (Gate leakage and generation-related off-currents)

The 3D full-band quantum-transport code GreenSolver was extended for the simulation of gate leakage currents in Si nanowire transistors. A real-space Schrödinger-Poisson solver has to be used instead of the popular mode-space. It was found that the leakage currents calculated with the 2D approach are significantly larger due to diffraction of the electron waves at both edges of the gate contact. This effect had never been explained and quantitatively treated before.

Deliverable 4.4 mainly deals with the evaluation of the gate leakage currents in the template devices which were defined within D 4.1, the refinement of the leakage conduction model and the study of the impact of the interface transition layer on the electronic structure of the substrate and the gate leakage current.
The devices investigated include bulk MOS transistors as well as single-and double-gate devices and a CNT FET, each equipped with high-K dielectrics. The drain and gate currents and a comparison between the different architectures is attempted, pointing out the difficulties in comparing different devices where the edge component of the leakage current plays a dominant role. Then, the leakage current in a 20×20 μm2 MOSFET with HfO2 dielectric is investigated in more detail, looking at the temperature dependence of experimental data provided by Tyndall University. It is shown that the overlap amount controls the leakage at low fields, while at high voltages the bias and temperature dependences cannot be reproduced. Simulations via existing trap-assisted tunnelling (TAT) models are carried out, suggesting that this could be the probable mechanism.
Finally, the impact of the interface transition layer between silicon and the dielectric is investigated, assuming a gradual transition of the conduction band edge rather than an abrupt one. The effects on the carrier quantization at the interface are discussed, showing that the leakage current can increase by an order of magnitude as a consequence of the different penetration of the wave-functions

In collaboration with F1.3 (High-k Flagship) a detailed theoretical comparison of the gate leakage characteristics of bulk MOS capacitors (fabricated and characterized in F1.3) and FD SOI (data required by the ITRS Roadmap) have been carried out.
The comparison of the gate leakage of the two structures at 1.5 V is expected to give a factor of 1.5 as a “safety margin” by using bulk MOS-cap data in evaluating dielectrics for use in DG SOI devices.

TASK 3 (Understanding of mobility and interface effects in presence of strain and high-k dielectrics)
The experimental characterization of mobility for different architectures of high-K based transistors and, on the other hand, an extensive simulation activity which includes a systematic comparison to experiments either performed inside the NANOSIL project or retrieved from the recent literature, have been carried out and the results presented in D4.2.
Several groups have been involved in an effort to gain thorough understanding of the low-field mobility in biaxially-strained n-MOS and p-MOS transistors. The activities started with a careful selection of experimental data, including both data provided by partners of the NANOSIL consortium and data retrieved in

the literature. The comparison between the different simulation results and with the experiments are discussed in detail in the deliverable D1.3.
Further efforts have been devoted to the modelling and the understanding of strain effects on the mobility of planar as well as FinFETs. In particular the effect of the biaxial strain on the Coulomb limited mobility was investigated and a comprehensive study was developed about the potentials for strain induced mobility enhancements in FinFETs.

An analytical electron and hole mobility models has been developed for ultra-thin body FETs on different crystallographic orientations for simulation of SOI-FETs, FinFETs and Silicon Nanowires; furthermore, it has been implemented through the Physical Model Interface (PMI) in the commercial simulator Sentaurus by Synopsys.

Very recently the mobility and the ION of Ge MOSFETs were compared to Si MOSFETs (an activity very synergetic with FSP1.1) by using state-of-the-art multisubband Monte Carlo (MSMC) simulations, that account for the quantization in the inversion layer, for a wide set of scattering mechanisms and for the non-local transport in nanoscale MOSFETs. The simulation results have shown that strained Ge n-MOSFETs have great potentials for beating the Si counterparts, however the engineering of the series resistance is a crucial issue. The already developed low-field electron and hole mobility models for (100), (110) and (111) UTB MOSFETs have been applied to FinFETs by accounting for different surface orientations, for extremely small silicon thicknesses as well as for the strain. A nice agreement with experiments available in the literature has been obtained for different stress configurations.
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TASK 4 (Compact modelling)
The compact modelling activity in NANOSIL is concentrated on three main issues: i) Electrostatics, ii) Partially ballistic transport and iii) Variability.
The introduction of ultra-thin-body and multi-gate structures for nanoscale FETs with the aim of improving the electrostatic control of the channel by the gate poses significant challenges to the definition of accurate analytical models. This topic has been particularly addressed by groups in URVUGR and UCL. Here, a series of compact models for several types of Multi-Gate MOSFETs are presented (double-gate, tri-gate, gate-all-around, ultra-thin body). All models are based on a unified charge control model derived from the solution of the 1D Poisson's equation in the direction perpendicular to the channel. Short-channel electrostatic effects are incorporated using equations derived from the remaining 2D or 3D equation. All models are favourably compared with a series of TCAD simulations and experiments. UCL has also investigated the impact of the substrate bias and space-charge conditions at substrate-buried oxide interface on the behavior of UTB and UTB2 (i.e. ultra-thin-body with thin BOX) SOI MOSFETs by both electrical measurements and 2D Atlas Simulations. The inclusion of partially ballistic transport in compact models of nanoscale MOSFETs is now a necessity, given the extremely small channel lengths of CMOS technology. Existing models, such as the backscattering models are very intriguing from the conceptual point of view but too simplistic. This issue has been tackled by groups in INPG-IMEP and IUNET. They propose here improvements to the Lundstrom Backscattering model, and an alternative macromodel capable to seamlessly cover ballistic and drift-diffusion transport in two- and one-dimensional FETs, also in the presence of Schottky-barrier contacts.
How to address FET variability with compact and analytical models has been the subject of investigation for GU and IUNET. In particular, GU proposes and evaluates different statistical compact model generation strategy on the basis of the accuracy of statistical circuit simulation. IUNET proposes a methodology to extract information on the variability of device electrical parameters based on a limited number of TCAD simulations and on dedicated analytical models.
As a final remark, results from this activity led to the publication of 21 papers in peer-reviewed journals and 12 papers in proceedings of international conferences.

TASK 5 (RF and ultra fast I-V characterization and modeling)
A detailed DC and LF noise characterization of FinFETs has been carried out. Parameter extraction conducted at room and low temperature clearly indicates that the mobility is degraded at small gate length in sub 100nm FinFETs, as was already found for GAA, FD-SOI and DG-MOS devices. By proper extraction technique,

sidewall and top conductions are analysed, showing that sidewall mobility is about 25-30% degraded as compared to the top surface conduction, likely resulting from Fin patterning-induced defects and/or crystal orientation difference. Trap density in high-k/metal gate stack is found much larger than in pure SiO2 MOSFETs but with no further degradation at small Fin widths.
RF measurements were performed at UCL on three types of devices coming from UNEW: 1) strained Si HBT, for which high performance at DC was demonstrated (IEDM 2008); 2) Si BJT and 3) SiGe HBT. These transistors had been fabricated in parallel, so direct comparison between them is relevant. Extractions of fT and fmax were made on all types of transistors and for different layout options. • In collaboration with UNEW, the self-heating effects in Si, SiGe and strained Si HBTs have been investigated. Based on RF measurements of the transconductance, it appears that the impact of self-heating is much more pronounced for strained Si HBTs.
Fully-depleted (FD) Schottky barrier (SB) MOSFETs with dopant-segregated NiSi source/drain junctions built by FZJ have been characterized over a wide frequency band at UCL. SB-MOSFETs with a channel length of 80 nm show high on-currents of 900 μA/μm for n-type devices with As segregation and 427 μA/μm for p-type devices with B segregation. A detailed RF characterization proves the high performance of the devices with cut-off frequencies fT of 117 GHz for n-type and 63 GHz for p-type SB-MOSFETs and clearly elucidates the effects of extrinsic and intrinsic device parameters as a function of gate length. Results have been presented at ESSDERC 2009.
More recently, researchers of FZJ and UCL have investigated the DC, RF and linearity performance of new optimized FD SB-MOSFETs on thin-body SOI. N-type NiSi source/drain SB-MOSFETs with a channel length of 80 nm using silicidation induced dopant segregation at 450°C show on-currents as high as 1152 μA/μm and exhibit a cut-off frequency of 140 GHz. This is the highest fT achieved for n-type SB-MOSFETs so far. On-wafer S-parameter measurements facilitate the extraction of the device parameters as a function of the implanted ion dose.

Very recently UNEW investigated the origins of high-field mobility enhancements in uniaxially strained Si by high resolution AFM measurements on strained Si beams with varying degrees of uniaxial strain. Rms roughness reduces from 0.29 nm to 0.07 nm as uniaxial strain increases from 0 to 2.77% and is accompanied by an increase in roughness correlation length compared with bulk Si (up to ~1.5% strain) before reducing at higher levels of strain. The results indicate that accurately determined correlation lengths should be considered in transport modelling of strained Si.

4.1.4 The potential impact (including the socio-economic impact and the wider societal implications of the project so far) and the main dissemination activities and exploitation of results.

- ***Introduction:*** The shrinking dimensions of electronic components will continue in the next two decades. The critical feature size of the elementary devices (technology node) will drop from 65nm in 2007 to 8nm in 2025. In the sub-10nm range, “Beyond-CMOS” devices will certainly play an important role and could be integrated on CMOS platforms in order to pursue integration down to nm structures. Si will remain the main semiconductor material in a foreseeable future, but the needed performance improvements for the end of the roadmap will lead to a substantial enlargement of the number of materials, technologies and device architectures. Therefore, new generations of Nanoelectronic ICs present increasingly formidable multidisciplinary challenges at the most fundamental level (novel materials, new physical phenomena, ultimate technological processes, innovative device architectures, etc.) resulting in an urgent need of academic research, in order to explore new concepts and to understand the underlying physical mechanisms for N+4 technology nodes and beyond, which was the focus of the Nanosil NoE. This long term research activity will allow to speed up technological innovation and to prepare the path for future industrial applications in the field of communications, computing, consumer electronics, health, environment, etc.
In Nanosil, joint processing, characterization and modelling platforms, detailed on the Nanosil web site, were developed and used for the realization of ambitious flagship projects. A strong link has been established between modelling/simulation, processing and characterization activities within each project. In addition,

visionary projects have also been defined in the More Moore and Beyond-CMOS domains. These projects focused on discussion Forums, brainstorming activities and Workshops and have generated new ideas and helped identifying the most promising topics for future information and communication technology.
A robust organisational, management and governance structure as well as decision-making mechanisms, based on a Governing Board, an Executive and Scientific Committee and WP Committees, have been realized in order to maximize the efficiency of the NoE. During Nanosil, close links with other European Projects (STREP GRAND, EUROSOI+ Thematic Network, STREP DUALOGIC, STREP NEMSIC, Compact Modelling Network COMON, STREP SQWIRE, STREP STEEPER, NoE NANOFUNCTION, etc.), the ENIAC Nanoelectronic Technology Platform (participation in the management team of the Scientific Community Council and several Working Groups devoted to research domains and infrastructures), the AENEAS organization (in charge of the ENIAC JU) and National projects in the same fields have been established in order to enhance the overall efficiency of the European Research in Nanoelectronics. NANOSIL acted as a cluster of projects, existing at the beginning or new ones, providing they were sufficiently forward-looking.
The interaction between the Scientific Community and the European Industry has also been strenghened (participation of representatives of the European industry in the Executive and Scientific Committee, industrial monitors for Flagship Projects, joint PhDs and Workshops, joint publications in high level Conference and Journals, etc.). Some STREPs including many industrial partners were also proposed by Nanosil Partners during ICT call 5 in October 2009 and have been launched in 2010 (SQUIRE, STEEPER).

Many Nanosil Partners and Sinano Institute Members have contributed to the "Sinano Institute vision", driven by the European Academic Community, in order to determine the most promising research topics in the More Moore, More than Moore and Beyond CMOS Nanoelectronic domains to be included in future FP7 Workprogrammes (document available on the Nanosil and Sinano Institute web sites - www.nanosil-noe.eu ; www.sinano.eu). Sinano and Nanosil Partners are also in charge to establish in 2011 an updated version of the ENIAC SRA concerning the Beyond-CMOS field.
During the project, we have studied some of the main scientific and technical challenges put forward by the International ITRS Roadmap and European ENIAC Strategic Research Agenda for the understanding of the limitations and the proposal of advanced solutions in the More Moore area: main boosters for the driving current and best solutions for reducing the offstate leakage current (screening of the most promising high k/metal gate stacks, development of low source/drain Schottky barrier MOSFETs, study of novel strain platforms). We have also developed the knowledge for future industrial roadmaps beyond the CMOS technology and proposed very innovative Si-based nanodevices: realization of nanowires by top-down and bottom-up approaches, investigation of advanced small slope switches (focus on the most promising approach: Tunnel FETs) and carbon electronic structures.
The scientific results obtained in the joint Nanosil projects, showing significant improvements over the state-of-the-art, and the integration and spreading of excellence activities organized by Nanosil Partners, are summarized below for all the Work Packages.

All these activities will contribute to the *durable integration of the partners*. However, some very important specific actions have been launched for the strengthening of this durable integration:

→ Two new Partners (Tyndall-Cork, Uppsala University) became Members of the Sinano Institute in 2009, which is a legal entity (Scientific Association) created in January 2008 for the coordination of the European Academic Community working in the field of Nanoelectronics (launched for the durable integration of the FP6 Sinano NoE).
Five other European Institutions became Members of the Sinano Institute in 2011, in line with the new FP7 NoE Nanofunction launched at the end of the Nanosil NoE (ICN-Barcelona, VTT-Helsinki, Twente University, IES-Montpellier University, IMS Demokritos-Athens)

→ The Joint Processing, Joint Characterization and Modelling Platforms, which have been developed and used in the framework of the Nanosil NoE for our joint research activities, are now integrated as open Research Infrastructures in the Sinano Institute and can be used by the European Academic Community, SMEs and Industry

→ Nanosil Partners and Sinano Institute Members have been strongly associated to the new initiative launched in 2010 by STMicroelectronics called ENI2 (European Nanoelectronics Infrastructure for Innovation). This Infrastructure propose to coordinate the three levels of R&D activities needed in the nanoelectronics domain. The 1st level is coordinated by the Academic Community (the main contact is the Sinano Institute, it will ensure the coordination of this level) for long term researches (basic understanding, test and validation of innovative materials, processes and architectures in order to identify the most promising topics for future ICT). The 2nd level is coordinated by the Integration Centres (large European pre-industrial Institutes) for technology implementation and performance assessment of the most promising topics defined at level 1 on R&D equipments, and development of high performance logic, memories and derivatives (medium term). The 3rd level is coordinated by the European industrial companies for technology exploitation as functional products, process optimisation, yield, product reliability, device and interconnect architecture and design (short term).

→ A significant part of Nanosil Partners have launched a new FP7 NoE, Nanofunction, devoted to Beyond-CMOS nanodevices for adding functionalities to CMOS in the More than Moore domain (nanosensing, energy harvesting, nanocooling, RF). An important part of Nanosil results, especially those devoted to Nanowires mainly developed in Nanosil for ultimate CMOS applications, will be used in Nanofunction for the development of advanced nanodevices to be used in future nanosystems. On the other hand, many Nanosil Partners have been involved in the FET Flagship "Guardian Angels" proposal dedicated to future autonomous ultra low power systems for health and environmental monitoring. It has been selected as a pilot project (beginning in May 2011).

- ***WP1:*** The impact of this NOE is primarily through the beneficial collaborations that have been established/ consolidated during this NOE period. This is especially so where device fabrication is involved. Many of the interactions will doubtless continue beyond Nanosil. This in turn helps maintain the processing, characterisation and simulation platforms that were created originally in the Sinano NoE. Nanosil also helps/helped at least some of the partners to secure additional funding at the national level for complimentary research activity. The European infrastructure (both industrial and academic sectors) will have benefitted from this work.

The main dissemination has been through publication in international journals (many of high impact), through presentation at national and international meetings including some at the prestigious IEDM, VLSI and SSDM and through visits to leading laboratories around the world. In total there have been well over 100 publications arising from WP1, of which 40 are joint, and over 100 conference presentations (see WP5 report for details).

Most of the work carried out in WP1 was world leading and in all cases, state-of-the-art. The ultimate exploitation will likely come primarily through continuing interactions with our pre- industrial institutes IMEC and LETI who have the critical links to the major semiconductor processing houses. Patented protection was undertaken by a few partners and this would be used to appropriate returns between the collaborating institutions.

- ***WP2:*** The primarily impact of WP2 within Nanosil is to explore the horizon beyond CMOS through the establishment of a lot of collaborations between the NoE partners. This includes especially the development of creative emerging technologies, characterization and simulation platforms for fabrication for alternative silicon-based post nanoelectronic devices. Embedded within the other work packages of Nanosil, WP2 activities cover a wide spectrum ranging from new fabrication methods and novel switching memory concepts to new functionalities and architectures. Furthermore the NoE helped to ensure additional funding for some partners at the EC level, for example the STEEPER project with four Nanosil partners and three industrial partners. In addition complimentary research activities were funded at the national level. Finally the European infrastructure (both industrial and academic sectors) will have benefitted from this work.

The main dissemination has been through publication in international journals (many of high impact), through presentation at national and international meetings documented in detail in the WP5 report. In addition through WP2 forums (especially workshops) between European Research Institutions on innovative visionary "Beyond CMOS" ideas were provided, for example on "Brain-Inspired Electronic Systems (BIECS)", on "Convergence of Electronics and Photonics" and on "Beyond CMOS Routes".

In general the focused research attempts within the network have provided substantial insight in both the confidence of individual groups as well as the ability to collaborate. A large body of "beyond CMOS knowledge" has been accumulated among leading groups in Europe, providing an excellent platform for future projects as well as a decisive orientation for future industrial roadmaps beyond CMOS.

- ***WP3:*** The work within the Joint Processing Platform has created direct scientific results as manifested in joint publications already published by partners. It is also anticipated that the work contacted during the last year of NANOSIL will produce several joint publications. The Joint Processing Platform has also had a major impact on the European academic research within nano-scaled MOSFETs because of the highly collaborative nature of the work. Several joint processing activities have been initiated and will continue e.g. in the area of sGe MOSFETs and high-k/metal gate dielectrics. These activities are also believed to create joint characterization and modeling activities in the future involving partners from the Joint Characterization and Modeling platform of NANOSIL. It is thus envisioned that the work initiated within the Joint Processing Platform will impact academic partners for several years beyond the end of NANOSIL. Furthermore the work has clarified the competence and skills between different partners possibly allowing for more effective research in the future if the collaborative spirit of NANOSIL can be continued. The collaborative work has also in some cases made partners differentiate and focus on their core competence and relied on collaboration to achieve research goals. One direct outcome of the WP3 is the new NoE Nanofunction which also will be similarly executed.
After the end of NANOSIL it is the ambition to incorporate the Joint Processing Platform into the SiNANO Institute enabling an open processing platform available to academic researcher in the EU. During NANOSIL WP3 has gathered and compiled information about the available resources within the processing platform. The information about the resources is accessible through the NANOSIL webpage. Furthermore, on the webpage an online request form has been set up where researcher can specify their processing needs. By filling in the request form they can send their requests directly to the coordinators of the Joint Processing Platform. It is believed that these activities will aid in that ambition to create an open processing platform to researcher with the EU community.

- ***WP4:*** The European semiconductor research community has a long-standing tradition in the development tools for electron device simulation, both in Academia and Industry. Over the years, several research groups have tackled the issue of modeling nanoscale transistors adopting different approaches and transport models.
One of the major objectives of the modelling and simulation activity in NANOSIL has been to compare and benchmark such simulation tools and transport models by comparing the results they provide when applied on a small set of representative template devices. We believe this is an important objective provided by the NANOSIL Network of Excellence, since such a systematic comparison can be a useful guide to a young researcher entering the field, and can represent in an objective way the relative merits of different tools to a large group potential users, both in Industry and in Academia. In this way it can certainly increase the potential impact of device simulation research outside the small community of developers of modeling tools.
The first large scale attempt to compare device models worldwide was carried out in 1993 by many groups involved in the development of Monte Carlo simulation techniques for the solution of the Boltzmann Transport Equation (BTE) [1]. At that time, Monte Carlo was seen as a reference technique, compared to simpler Energy Balance or Hydrodynamic transport models based on the momenta of the BTE, to solve in an exact way the BTE in short devices. The need for model benchmarking was reaffirmed within the European project SINANO. The SINANO workprogramme included benchmarking activities for both quantization and transport models. Thanks to a significant coordination effort it was possible to compare, analyze and debug seven Schroedinger-Poisson solvers and gate current models worldwide, until the results converged to a high degree of accuracy; residual discrepancies could be attributed to specific differences in the modelling approaches [2]. Monte Carlo Transport Models were also taken compared within SINANO, but the limited time and resources available made it impossible to reach definitive conclusions w.r.t. the accuracy and maturity of the models themselves. The success of this activity pushed the participants to the project to propose a similar, but broader scale activity, within the NANOSIL project and the main results of the comparison of a comprehensive set of tools, including semi-classical and full-quantum models, and more

aggressive template devices, including those representative of the 16nm node, have been tested and compared during the project and the results presented in [3] and D4.6 (a full publication is in progress).
Furthermore, a formidable vehicle of dissemination of the modelling results has been the well known SINANO Modeling School, held in 2008 and 2010 in University of Bologna Summer Campus of Bertinoro, where almost 100 among students and teachers from all over the scientific world had the unique opportunity of staying together and share knowledge and experience, giving often rise to new collaboration opportunities within and outside the NANOSIL Consortium.
Finally it is worth mentioning that within WP4 several exchanges occurred outside the Nanosil which involved new partners particularly from Eastern Europe coutries.

[1] A. Abramo et al., IEEE TED 1994.
[2] P. Palestri et al. IEEE TED 2007.
[3] F. Bufler et al, 14th IWCE 2010.

- ***WP5:***

1. Integration

1.1. Coordination by WPs (FPs) leaders

Integration within Nanosil is carried out by WPs and FPs leaders through the coordinated programming of the partners' activities. 4 Work Packages (WPs) are defined within Nanosil. WP1 and WP2 are then subdivided to 3 and 4 Flagship projects (FPs), respectively. Additionally, these WPs are completed by Visionary projects (VP) in order to reinforce/stimulate the exchange of new ideas / provoke the discussions / exchange of opinions between partners.
Integration within Nanosil is measured through numbers of **joint processing (JP), characterization (JC) and modeling (JM) activities** within each FPs/WPs as well as cross-FPs/ WPs activities. Firstly, good tendency with constant from year to year increasing number of joint activities (~20-25%/year) was observed over the project. Starting from **38 in 2008** (24 JP, 11 JC and 3 JM, respectively), it becomes **47 in 2009** (26, 15 and 9, respectively), and finally reaches **58 in 2010-11** (27, 21 and 11, respectively). Secondly, number of **cross-FP/WP** activities increases as well from **13 in 2008 to 18 in 2009 and 2010-11**. Thirdly, JP was very active over the whole project duration with **more than 300 wafers processed**. Integration of different WPs was observed particularly in JP during 2010-11. Fourthly, **clear increase in JC** in 2009 and especially in 2010-11 was observed as a result of very active processing during previous years.
Another integration measure is number of meetings between partners, organized in order to stimulate the joint activities, follow up the progress within WPs (FPs), discuss the obtained results and assure a smooth transfer/integration between different WPs. Similarly to joint activities, number of **"technical meetings"** between partners increased from year to year during the project: **from 18 in 2008 to 32 in 2009 and finally 41 in 2010-11,** proving intensification of collaboration between partners during the project. Number of cross-WP meetings increases strongly in 2010-11, being only 2 in 2008 and 2009, it becomes 10 in 2010-11. It was expected since 2010-11 was particularly devoted to process transfer/integration between WPs.

1.2. Common PhD students

NoE integration is reinforced by the common/joint PhD students between different partners.
About 10 common PhD students worked within Nanosil during each year of project (12 in 2008 and 10 in 2009 and 2010-11). Some of them already presented their PhD Thesis. It is interesting to note that most of them are related to the characterization activities (WP4). Some PhD works devoted to two WPs (1, 2 and 4) in the same time, thus reinforcing cooperation not only between partners, but between processing- and characterization/simulation- related WPs as well. Furthermore, majority of these PhD students being joint between industrial and academic partners enhances industry-academia interactions.

1.3. "Who is Who guide" of Nanosil partners was created in 2008 and made available through the Nanosil web-site Public Area. Interactive information is introduced in the "partners list". Moreover, the search by "competence" is available. Complete pdf-file is available on the site as well (http://www.nanosil-noe.eu/data/document/nanosil_who_is_who.pdf). It is updated yearly. Furthermore, **"Who is Who" of**

associated partners was initiated in 2009. **Request for Beyond Nanosil institutions to be included in "Who is Who"** of associated partners was made available on the web-site in public area. **"Who is Who" of associated partners** gathers "who is who" of institutions participated in exchanges with Nanosil partners as well as institutions involved in national projects or other collaborative actions (those interested). Updated 2010 version is available on the web-site (http://www.nanosil-noe.eu/data/document/ who-who-beyond-nanosil.pdf).
Additionally, we encouraged partners to provide us information about "**technical problems** they encounter **and open questions** they imagine" (requests were sent twice per year). Some problems/ questions were reported in 2008. Then, this information was discussed during E&S Committee meetings as well as put on the Nanosil web-site for the access of all Nanosil partners. No problem/ question inputs from partners were received during 2009-2010, assuming that these issues were discussed/solved on the level of FP/WP teams and were not worth to be discussed at ESC meetings.

1.4. Interaction with industrial partners aims at roadmapping, assessing the results and assures theirs transferability to industry. With this regards, each FP of Nanosil has industrial contact person or **"monitor"**. Industrial partners are invited to **participate in Executive & Scientific Committee Meetings** to develop a general strategy of network progressing/ developing. Additionally, common industry/academia **PhD students** (6 in 2008, 7 in 2009 and in 2010-11) stimulate collaboration and free discussions between industrial and academic partners. Furthermore, **projects involved both academia and industry**, number of which, moreover, increases from year to year (~ 15 submitted/accepted in 2008, 11 running and 8 newly submitted/accepted in 2009 and 19 running and 14 newly submitted/accepted in 2010-11) reinforce exchange of knowledge with industrial partners within and beyond Nanosil. Finally, information about **scholarships/trainings/PhD positions/etc. available at the industry** with web-links is accessible through the Nanosil site (http://www.nanosil-noe.eu/nanosil/wp5/scholarships-and-trainin.html).

2. Collaboration with other European and national projects

Screening of **national projects** of relevance has been performed by the participants from each country in 2008. In total 61 national projects were mentioned in a complete list available on the Nanosil web-site. The repartition between countries was as follows: 17 in UK, 4 in Ireland, 1 in Switzerland, 8 in Spain, 7 in Germany, 16 in France, 1 in Sweden, 3 in Belgium, 1 in Greece and 3 in Poland. E&S Committee members have selected 11 among them to participate in a common **Workshop Nanosil/National projects** which was held on January 30th 2009 in Grenoble. The idea of this workshop was to familiarize Nanosil partners with on-going activities within each country, put those interested in contact and hence initiate new possible collaborations.
Furthermore, information on the on-going European and national projects as well as about newly submitted/accepted ones was requested to be updated by partners at the end of each year. **Lists of European and National projects** of relevance are **placed on the Nanosil web-site** (with update once a year), web-links to the corresponded project sites are introduced whenever possible.
Number of on-going European and national projects with participation of Nanosil partners was reported every year. Naturally, **good links between Nanosil and these projects** were established. As example we can talk about collaboration and exchange of knowledge between Nanosil and **FP6** (Pullnano, Metamos) and **FP7** (EuroSOI+, ANNA, COMON, GRAND, MODERN, STEEPER, SQWIRE, Nanofunction, etc. …) **projects**.
Additionally, number of the **newly submitted/accepted European, international and national projects** launched by (or with participation of) Nanosil partners increases from year to year: being **13** in **2008**, it becomes **25** in **2009** and in **2010-11**.
Finally, it is worth to point out **high** (and increasing) **number of the projects submitted in the collaboration between** two (or more) **Nanosil partners** (**7** in **2008**, **15** in **2009** and **14** in **2010-11**), which evidence strong and durable integration/collaboration between Nanosil partners.

3. Exchanges

Exchange of personnel within the project serves for further strengthening the exchange of expertise/knowledge/competence and complementarity between partners. **Calls** for exchanges were issued electronically **every 3 months**. In order to get access to the specific knowledge missing inside Nanosil, **Exchanges with Beyond Nanosil** partners (not only within, but also outside of Europe) were launched during 2009. This option included possibility to welcome selected researchers outside Nanosil and to stay/train of

Nanosil researches in the selected labs beyond Nanosil. Requests for such exchanges could be submitted by Nanosil partners only.
Requests from partners have been then **discussed during E&SC meetings and** those worth of support have been **selected**. Last call was issued in September. However, in view of project extension, partners were allowed to perform their planned exchanges until end of February 2011.
67 exchanges with total duration of **238 weeks** (including **10 exchanges** of total **60 weeks** with **Beyond Nanosil** partners) were **selected** for support **during 3 years** of project. The number of requests clearly **increased from year to year,** thus indicating **enhancement of network activity**.
59 exchanges (including **9 with Beyond Nanosil**) with total duration of **227 weeks** (including **48 with Beyond Nanosil**) were done during the whole project. We observe **increase from year to year both in number and duration of exchanges**, especially impressive during 2nd period: being only **7** exchanges with total duration of **12 weeks in 2008**, it becomes **23** exchanges of **104 weeks in 2009** and **29** exchanges of **111 weeks in 2010-11**. If we would look on the repartition between different WPs, it is interesting to point out that about **half of these exchanges were devoted to characterization/modeling activity**, i.e. WP4. Then, most of Beyond Nanosil exchanges were focused on WP4. It would be worth to emphasize **increasing number of cross-WP exchanges** (i.e. devoted to couple WPs in the same time): **7** (with total duration of 49 weeks) **in 2009** and **15** (with total duration of 60 weeks) **in 2010-11**. Such exchanges serve not only as exchange of knowledge/expertise, but in the same time intensifies cooperation between WPs (particularly processing vs. simulations/modeling).

4. Spreading of excellence

4.1. Support of International Schools/Workshops

As for the exchanges, **calls** for the **conference/workshops/seminars support** were issued electronically **every 3 months**. The requests for such actions were gathered and the best ones were selected by E&S Committee. During 2008-2009 we were able to support mainly events explicitly mentioned in DoW. However, thanks to careful use of funds within WP5 as well as economy from certain exchanges, we were able to support higher number of workshops/ schools/etc. during last period: **14 in 2010-11 comparing to 5 per year during 2008-2009**. Following workshops were selected by E&S Committee for support over the whole project:

- MIGAS'08, France (10kEuro);
- SINANO-NANOSIL Workshop 2008, UK (5kEuro);
- 3rd SINANO International Summer School 2008, Italy (12kEuro);
- Postgraduate student meeting on electronic engineering, Spain (2.5kEuro);
- ULIS 2009, Germany (10kEuro);
- MIGAS'09, Fance (10kEuro);
- SINANO-NANOSIL Workshop 2009, Greece (5kEuro);
- Workshop "Convergence of Electronics and Photonics", Germany (5kEuro);
- D&Y Symposium: Advanced Devices and Technologies for ULSI Era, Poland (2.5kEuro);
- Postgraduate student meeting on electronic engineering, Spain (2.5kEuro);
- ULIS 2010, UK (10kEuro);
- Silicon Nanowires Workshop, Belgium (750Euro);
- International SiGe Technology and device meeting, Sweden (2.5kEuro);
- International Workshop on Sem-OI materials, sensors and devices, Belgium-Ukraine (11kEuro);
- SINANO Summer School, Italy, 2010 (14kEuro);
- Simulation and characterization of statistical CMOS variability and reliability, Italy (2.5kEuro);
- Graduate student meeting on electronic engineering JOINTLY with training course on Compact modelling, Spain (3.5kEuro);
- MIGAS 2010, France (10kEuro);
- Workshop on Carbon Electronics "EuroCarbon Symposium", Germany (2.5kEuro);
- SINANO-NANOSIL workshop 2009, Spain (5kEuro);
- Workshop "Nanoelectronics: a tool to face the future", Spain (2.25kEuro);
- Final Nanosil Workshop devoted to ENI2 "Nanoscale FET", Ireland (4kEuro);
- International conference "Micro&Nano", Greece (2kEuro).

4.2. Organization of seminars/courses/workshops/tutorials

Number of scientific events as workshops, conferences, schools, trainings, etc was organized by Nanosil in different countries over whole Europe during 3 years of project either with or without direct financial support from Nanosil.

First of all, common **SINANO-NANOSIL Workshops** aimed establishing a discussion forum in the field of nanoelectronics devices were organized every year as satellite events of ESSDERC/ESSIRC Conferences in order to ease attendance not only for Nanosil partners but to wide range of researchers/engineers/PhD students/etc. Lectures were given by Nanosil partners and by representatives from industry. Two first workshops were devoted to "Si-based Nanodevices for ultimate CMOS and beyond-CMOS" and the last one (jointly with VP1.4) discussed the topic "On the convergence between More Moore, More than Moore and beyond CMOS". Traditionally, these workshops were open to a general public and free of charge.

Secondly, special attention is worth paying to high number of events targeting particularly **young researchers** as graduate and post-graduate students pursuing their PhD. We can refer to two Sinano Sumer schools, three MIGAS, yearly postgraduate student workshops in Spain, etc.

Thirdly, it would be worth to emphasize that couple of above mentioned workshops financially supported by Nanosil were organized in **Warsaw, Poland** and in **Kiev, Ukraine** (the last one **jointly with beyond-Nanosil** partner) thus allowing wider dissemination of Nanosil knowledge and intensification of **collaboration with East Europe and former Soviet Union countries**.

Fourthly, as was already mentioned above, **two Visionary projects** (VP 1.4 "More Moore Forum" and VP 2.5 "Beyond CMOS vision") were launched within Nanosil WP1 and WP2 in order to stimulate discussions on the new hot-topics and identify areas where the partners of the Network can make a contribution. The **discussions/workshops organized by these VPs** are open to participants within Nanosil free of charge as well as to wide audience beyond Nanosil. **Ten workshops and panel sessions** were organized **within VP1.4** during 2008-2010 and addressed the four topics related to particular aspects of Ultimate CMOS: electrostatic effects; transport, fluctuations and alternative channel & substrate materials. **Four workshops** were organized **within VP2.5 during 2008-2011 and addressed innovative Beyond CMOS ideas**. Such topics were discussed: "Brain-inspired Electronic Systems", "Convergence of electronics and photonics" and "Beyond CMOS Routes".

Fifthly, additionally to the abovementioned workshops financially supported by Nanosil (either through WP5 funds or VPs funds), it is worth to mention increasing from year to year number of **scientific events organized by Nanosil partners without direct funding from Nanosil** and open to wide public (**6 in 2008; 9 in 2009 and 14 in 2010-11**). Among them it is worth to cite a high number of large **well-known international events** as ESSDERC, EuroSOI, etc. Moreover, it would be important to emphasize **meetings/workshops organized by academic partners** (Livuni, UCL, WUT) **and targeted industrial teams** (ARM, ST, Soitec, …) allowing rather open discussion with direct transfer of knowledge accumulated within academia to industry (both within and beyond Nanosil) and industrial feedback on roadmapping/ perspectives/ their short- and long-term interests.

In addition to workshops/schools for young researchers, **ten new university courses** (of more than **250 hours** in a total) in Nanosil-related fields have been initiated by Nanosil members during 2008-2010, promoting the Nanosil knowledge to students.

A **database of NoE experienced lecturers** (similarly to IEEE distinguished lecturers) with existing high-level/high-quality lectures is created Yearly updated pdf-version is available on the Nanosil web-site.

5. Dissemination of knowledge

5.1. Inside of NoE

Dissemination of knowledge within Nanosil is provided through **the Executive & Scientific Committee meetings** (every 3 months), **Governing Board meetings**, **kick-off, inter-WP/FP and cross-WPs/FPs meetings**.

Nanosil web-site eases exchange of information between partners. There exists a restricted area limited to consortium members where one can find for example ppt/pdf-files with presentations given by Nanosil partners or those given during different events supported by Nanosil; annual reports, selected exchanges, etc.

Additionally, **exchanges/ trainings** of personnel played an important role in information/ideas/competences exchange between partners.

5.2. Beyond NoE

Web-site of Nanosil was created in 2008. It aims to **promote NoE activities** such as workshops/ trainings and competences of Nanosil partners. Taking into account recommendations from the reviewers, during 2009 web-site was **modified** with particular attention to make it **available, useful and attractive to a wider community**, while some parts are still confidential (restricted to consortium area through the login-password). Additionally, **processing, characterization and modeling platforms** existing in Nanosil explicitly appear on the web-site. Furthermore, **number of useful links and pdf files** can be found on the site even in a public area, as e.g. pdf-version of Who is Who guide (as well as Who is Who guide of beyond Nanosil partners), List of national and EU projects of relevance, training/courses/PhD thesis topics available, open positions, some general Nanosil presentations, Agenda of Workshops, Conferences, etc. All the information on the web-site is regularly updated. **"Breaking news"** was initiated in 2009 and serve as another visual point to widely advertise top-level achievements/developments within Nanosil. It is available on the web-site and updated every month.

66 whorkshops/conferences/schools/etc were **organized by Nanosil partners** during 3 years of project: **13** in **2008**, **21** in **2009** and **32** in **2010-11** either with or without direct financial support from Nanosil. It is interesting to point out that the numbers of organized events increases rather strongly from year to year. Such events accessible not only to Nanosil partners but to a wide scientific community are very important to disseminate knowledge gathered by Nanosil members and to widely promote our Network. Additionally, **8 researchers** (mainly FP leaders) **represented Nanosil** at the **EU-Russia Workshop** organized in Moscow by the European Commission with support from the Russian National ICT Contact Point and the Ministry of Science and Education with objective of intensification of R&D cooperation between actors of the ICT value chain from both sides. Participation of Nanosil members participating in this event **have been supported through the "exchanges procedure".**

Nanosil poster was prepared end of 2008. It was then offered to all Nanosil partners to be posted in their labs and promote in such a way the research activities / networking within Nanosil.
Nanosil News letter 2009 was issued. It groups the most impressive Nanosil achievements during 2009. All flagship projects as well as simulation/characterization and processing workpackages presented their most important results. Additionally, targeting beyond Nanosil auditorium, some general information about Nanosil as well as WP5 information on the possibility for Beyond Nanosil institution to participate in the network (e.g. through exchanges and Who is Who guide on the Nanosil web-site) were included. Nanosil NewsLetter 2009 is available on Nanosil web-site in a public area and was also e-mailed to the available mail lists.
Nanosil News letter 2010-11 is under preparation. When finished it will also be available on Nanosil and SINANO Inst. web-sites as well as e-mailed to the available mail lists.

Furthermore, it is worth to point out an active participation of Nanosil partners in the **ENI2** initiative. It aims a creation of long and lasting **R&D infrastructure** (in another words ecosystem) for **European nanoelectronic innovations**, thus allowing **long-term integration** of academic institutions together with institutes, industries and SMEs.

Finally, achievements/knowledge gathered within Nanosil are widely disseminated through the **publications in major international journals** and **participation** of Nanosil members in **international conferences/workshops**. Table 5.1 summarizes number of publications and conference presentations prepared by Nanosil partners per year of the project. Only papers clearly acknowledged Nanosil were counted. One can see very **high numbers of papers** (**more than 250**) and **presentations** (**about 400**) were prepared by Nanosil partners over the 3 years of the project. Moreover, **good evolution** of both values over the project duration can be observed. It would be worth to pay attention that about **1/3 of the Nanosil conference presentations are invited**, confirming recognition of expertise of Nanosil partners in related fields. We emphasize separately "joint" (i.e. prepared in collaboration between two or more partners) publications/presentations: **about 40% of papers and 35% of presentations are joint**.

Table 5.1. Summary on Nanosil publications and presentations.

	Papers		**Conferences**	
	Joint	Total	Joint	Total
2008	**38** *30 published;* *5 accepted; 3 submitted*	**N/A**	**41**	**87** *82 done; 5 accepted*
2009	**45** *36 published;* *4 accepted, 5 submitted*	**104** *77 published; 12 accepted;* *15 submitted*	**43** *38 done; 5accepted*	**142** *133 done; 9 accepted*
2010-11	**40** *32 published; 8 accepted*	**114** *98 published; 16 accepted*	**52**	**165**

Furthermore, **2 books** jointly edited by Nanosil partners were published during 2010-11. First one, **"Nanoscale CMOS: Innovative Materials, Modeling and Characterization"**, is entirely devoted to the results obtained by the groups involved in Nanosil. It addresses all WPs of Nanosil and covers both processing and characterization/modelling aspects. Second book **"Semiconductor-on-Insulator Materials for nanoelectronics applications"** was published by SPRINGER in 2011 as a result of SemOI Workshop jointly organized by UCL and ISP-Kiev and financially supported by Nanosil (see section 4.2). Comparing to the first one, it goes a bit further in addressing "more than moore" and "beyond CMOS" fields. It groups selected keynote works in the four areas: 1° new semiconductor-on-insulator materials; 2° physics of modern SemOI devices; 3° diagnostics of the SOI devices; 4° sensors and MEMS on SOI. More than half of chapters in this book were prepared by Nanosil partners. **33 Book chapters** were prepared by Nanosil partners; **12** of them are **joint**. It is worth to point out that these very high number of book chapters were written by Nanosil partners during last period of NANOSIL.

To demonstrate the **high level of research** performed within Nanosil and **their significant impact** on the scientific community, here below we show the **ratios of Nanosil partners' publications to the total number of publications** in selected journals with a high citation index and in major international conferences in 2010. (*in brackets are numbers for 2009 and 2008, respectively*).

- **IEEE Electron Device Letters:** 1.5%; i.e. 7 over 461 *(4%, 15 over 419 and 3%; 13 over 392)*
- **IEEE Trans. on Electron Dev.:** 7.9%, i.e. 36 over 458 (*6.4%, 27 over 420 and 6% 28 over 462)*
- **Journal of Applied Physics:** 0.5%, i.e. 11 over 2082 *(0.6%, 14 over 2390, 0.3%; 11 over 3492)*
- **Applied Physics Letters:** 1.1%; i.e. 27 over 2459 *(0.52%, 15 over 2903 and 0.07%; 4 over 5419)*
- **Solid State Electronics:** 11.5%, i.e. 33 over 288 *(16.5%, 46 over 279and 13%; 41 over 312)*
- **IEDM:** 3.9-5.4 % ; i.e. 8-11 over 205 *(3.2-4.6%, 7-10 over 218 and 3-7%; 7-17 over 220)*
- **ESSDERC:** 23.8 %; i.e. 24 over 101 *(25%, 25 over 100 and 21%; 17 over 80)*

We can see a clear tendency of increase in both numbers of publications and in percentages in 2009 comparing to 2008, which is especially strong in Physical journals. Then, in 2010 some change in balance between different journals (e.g. increase in IEEE TED, JAP and decrease in IEEE EDL) with about the same global numbers comparing to 2009 is observed. Finally, one can see a strong correlation between Nanosil penetration in more-EU based journals and conferences (SSE and ESSDERC) versus more US-based ones.

4.2 Use and dissemination of foreground

Section A (public)

TEMPLATE A1: LIST OF SCIENTIFIC (PEER REVIEWED) PUBLICATIONS, STARTING WITH THE MOST IMPORTANT ONES										
NO.	Title	Main author	Title of the periodical or the series	Number, date or frequency	Publisher	Place of publication	Year of publi-cation	Relevant pages	Permanent identifiers[3] (if available)	Is/Will open access[4] provided to this publication?
1.	Capacitor-less A-RAM SOI memory: Principles, scaling and expected performance	N. Rodriguez et al	Solid-State Electronics	Volume 59, Issue 1	Elsevier		2011	pp. 44-49	10.1016/j.sse.2011.01.006	No
2.	Double-gate 1T-DRAM cell using nonvolatile memory function for improved performance	K-H. Park et al, INPG, Korea	Solid-State Electronics	Volume 59, Issue 1	Elsevier		2011	pp. 39-43	10.1016/j.sse.2011.01.007	No
3.	Detailed investigation of effective field, hole mobility and scattering mechanisms in GeOI and Ge pMOSFETs	Van den Daele, INPG	Solid-State Electronics	Volume: 59, Issue 1	Elsevier		2011	pp. 25-33	Doi:10.1016/j.sse.2011.01.014	No
4.	Effect of growth rate on the threading dislocation density in relaxed SiGe buffers grown by reduced pressure chemical vapour deposition at high temperature	A Dobbie, et al	Semiconductor Science and Technology	Vol 25	Institute of Physics		2010	085007	doi:10.1088/0268-1242/25/8/085007	No
5.	Highly strained Si epilayers grown on SiGe/Si(100) virtual substrate by Reduced Pressure Chemical Vapour Deposition	M. Myronov, et al	Physica Status Solidi C	Vol 8	Wiley		2011	pp 952-955	doi:10.1002/pssc.201000255	No

[3] A permanent identifier should be a persistent link to the published version full text if open access or abstract if article is pay per view) or to the final manuscript accepted for publication (link to article in repository).

[4] Open Access is defined as free of charge access for anyone via Internet. Please answer "yes" if the open access to the publication is already established and also if the embargo period for open access is not yet over but you intend to establish open access afterwards.

6.	Defect-related excess low-frequency noise in Ge-on-Si pMOSFETs	E. Simoen, et al	Electron Device Letter	Vol 32	IEEE	Piscataway, NJ 08855-1331, USA	2011	pp 87-89	http://dx.doi.org/10.1109/LED.2010.2089968	No
7.	Mobility Enhancement in Strained n-FinFETs: Basic Insight and Stress Engineering	N. Serra et al;	IEEE Trans. on Electron Devices	February	IEEE	Piscataway, NJ 08855-1331, USA	2010	482-490	doi:10.1109/TED.2009.2037369	No
8.	An improved empirical approach to introduce quantization effects in the transport direction in multi-subband Monte Carlo simulations	P.Palestri	Semiconductor Science and technology	Volume: 25, No. 5	IOP Publishing		2010	055011	doi: 10.1088/0268-1242/25/5/055011	No
9.	Simple and efficient modeling of the E–k relationship and low-field mobility in Graphene Nano-Ribbons	M. Brescianiet al	Solid-State Electronics	Sept.	Elsevier		2010	1015-1021	doi:10.1016/j.sse.2010.04.038	No
10.	A quasi-analytical model for nanowire FETs with arbitrary polygonal cross section	L. De Michielis et al	Solid-State Electronics	Sept	Elsevier		2010	929 - 934	doi:10.1016/j.sse.2010.04.039	No
11.	Failure of the Scalar Dielectric Function Approach for the Screening Modeling in Double-Gate SOI MOSFETs and in FinFETs	P.Toniutti et al	IEEE Transactions on Electron Devices	Nov.	The Inst. of Electrical and Electronics Eng	Piscataway, NJ 08855-1331, USA	2010	3074-3083	doi:10.1109/TED.2010.2068990	No
12.	Pseudospectral Methods for the Efficient Simulation of Quantization Effects in Nanoscale MOS Transistors	Alan Paussa et al.	IEEE Transactions on Electron Devices	Dec.	The Inst. of Electrical and Electronics Eng	Piscataway, NJ 08855-1331, USA	2010	3239-3249	doi:10.1109/TED.2010.2081673	No
13.	Electric Field Control of Spin Rotation in Bilayer Graphene	P. Michetti, et al	Nano Letters	10,11	American Chemical Society	1155 Sixteenth Street N.W., Washington, DC 20036	2010	4463 – 4469	doi:10.1021/nl102298n	No
14.	Simulation of hydrogenated graphene field-effect transistors through a multiscale approach	G. Fiori, et al	Phys. Rev. B	82, 15	American Physical Society	One Physics Ellipse College Park, MD 20740	2010	153404	doi:10.1103/PhysRevB.82.153404	No
15.	Barrier Lowering and Backscattering Extraction in Short-Channel MOSFETs	G. Giusi, et al	IEEE Trans. on Electron Devices	57, 9	IEEE	Piscataway, NJ 08855-1331, USA	2010	2132 – 2137	doi:10.1109/TED.2010.2055273	No
16.	Model and Performance Evaluation of Field-Effect Transistors Based on Epitaxial Graphene on SiC	M.Cheli, et al - IUNET Pisa	IEEE Transactions on Electron Devices	57, 8	The Inst. of Electrical and Electronics Eng	Piscataway, NJ 08855-1331, USA	2010	1936 – 1941	doi:10.1109/TED.2010.2051487	No
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227.	Study of interfaces and band offsets in TiN/amorphous LaLuO3 gate stacks'	I.Z. Mitrovic et al.	Microelectronic Engineering	April 2011	Elsevier B.V.		2011			No
228.	Investigation of Electron and Hole Charge Trapping in LaLuO3 Stack MOS Capacitor Using the 3-Pulse CV Technique	N. Sedghi LIVUNI, Julich	ECS Transactions	April 2011	The Electrochemical Society, USA		2011			No
229.	Mobility Extraction in sub 10nm Nanowire nMOSFETs with Gadolinium-Silicate as Gate Dielectric	M. Schmidt, et al AMO, RWTH		March 2011		IEEE Xplore	2011			Yes
230.	A comparative study of surface-roughness induced variability in silicon nanowire and double-gate FETs	INPG/FMNT, IUNET	IEEE Trans. on Electron Devices	Special Issue on Variability	IEEE	USA	2011			No

TEMPLATE A2: LIST OF DISSEMINATION ACTIVITIES FOR PERIOD 3

NO.	Type of activities[5]	Main leader	Title	Title of paper/ presentation	Date	Place	Type of audience[6]	Size of audience	Countries addressed
1.	Book	GRENOBLE INP/FMNT (Editor), Nanosil consortium (see D5.4 for details)	ISTE-Wiley book (650 pages)	Nanoscale CMOS: Innovative Materials, Modeling and Characterization	2010		Scientific Community, Industry		International
2.	Book	Tyndall, ISP-Kiev, GRENOBLE INP/FMNT, UCL, UGR	Springer (450 pages) Doi: 10.1007/978-3-642-151868-1	Semiconductor-On-Insulator Materials for NanoElectronics Applications	2011		Scientific Community, Industry		International
3.	Book Chapter	D. Leadley et al Warwick	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 1: Introduction to Part 1: Novel materials for nanoscale CMOS	2010		Scientific Community, Industry		International
4.	Book chapter	O. Engstrom Chalmers, LIVUNI, Tyndall, AMO	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 2: Gate Stacks	2010		Scientific Community, Industry		International
5.	Book chapter	D.R. Leadley, et al Warwick	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 3: Strained Si and Ge Channels	2010		Scientific Research Community, Industry		International
6.	Book chapter	S. Mantl, D; Buca, FZJ	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 4: From thin Si/SiGe buffers to SSOI	2010		Scientific Research Community, Industry		International
7.	Book chapter	E. Dubois et al, IEMN/ISEN	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 5: Intorduction to Schottky-barrier MOS architectures: concept, challenges, material engineering and deivce integration	2010		Scientific Research Community, Industry		International
8.	Book chapter	E. Sangiorgi IUNET	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 6: Introduction to Part 2: Advanced modeling and simulation for nano-MOSFETs and beyond-CMOS devices	2010		Scientific Research Community, Industry		International
9.	Book chapter	B. Majkusiak et al	Book, "Nanoscale CMOS: Innovative	Chapter 7: Modeling and simulation	2010		Scientific		International

[5] A drop down list allows choosing the dissemination activity: publications, conferences, workshops, web, press releases, flyers, articles published in the popular press, videos, media briefings, presentations, exhibitions, thesis, interviews, films, TV clips, posters, Other.

[6] A drop down list allows choosing the type of public: Scientific Community (higher education, Research), Industry, Civil Society, Policy makers, Medias ('multiple choices' is possible.

		WUT, IUNET, ETZH	Materials, Modeling and Characterization", ISTE – Wiley	approaches for gate current computation			Research Community, Industry		
10.	Book chapter	M. Vasicek et al. IUNET	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 8: Modeling and simulation approaches for drain current computation	2010		Scientific Research Community, Industry		International
11.	Book chapter	Q. Rafhay et al. GRENOBLE INP, IUNET	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 9: Modeling of end of the roadmap nMOSFET with Alternative channel material	2010		Scientific Research Community, Industry		International
12.	Book chapter	A. Martinez et al GRENOBLE INP, GU	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 10: NEGF for 3D device simulation of nanometric inhomogenities	2010		Scientific Research Community, Industry		International
13.	Book chapter	B. Iniguez et al. URV	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 11: Compact models for advanced CMOS devices	2010		Scientific Research Community, Industry		International
14.	Book chapter	G. Iannaccone et al, IUNET, GRENOBLE INP	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 12: Beyond CMOS	2010		Scientific Research Community, Industry		International
15.	Book chapter	D. Flandre UCL	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 13: Introduction to Part 3: Nanocharacterization methods	2010		Scientific Research Community, Industry		International
16.	Book chapter	M. Mouis GRENOBLE INP	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 14: Accurate determination of transport parameters in sub-65 nm MOS transistors	2010		Scientific Research Community, Industry		International
17.	Book chapter	P. Hurley et al Tyndall-UCC, Chalmers, GRENOBLE INP	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 15: Characterization of interface defects	2010		Scientific Research Community, Industry		International
18.	Book chapter	A. O'Neill et al. UNEW	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 16: Strain determination	2010		Scientific Research Community, Industry		International
19.	Book chapter	D. Flandre et al. UCL	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 17: Wide frequency band characterization	2010		Scientific Research Community, Industry		International
20.	Book chapter	A. Lecestre et al. IEMN/ISEN, STM	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Confined and guided vapor-liquid-solid catalytic growth of Silicon nanoribbons: from nanowires to structured	2011		Scientific Community, Industry		International

				silicon-on-insultor layers					
21.	Book chapter	J.-P. Raskin UCL	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "SOI SMOS: A mature and still improving technology for RF applications"	2011		Scientific Community, Industry		International
22.	Book chapter	F. Balestra GRENOBLE INP	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Silicon-based devices and materials for nanoscale FETs"	2011		Scientific Community, Industry		International
23.	Book chapter	F. Gamiz et al. UGR	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Ultrathin n-channel and p-channel SOI MOSFETs"	2011		Scientific Community, Industry		International
24.	Book chapter	J.-P. Colinge et al. Tyndall-UCC	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Junctionless transistors: physics and properties"	2011		Scientific Community, Industry		International
25.	Book chapter	A. Afzalian, et al. UCL, Tyndall-UCC	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Gate modulated resonant tunneling transistor (RT-FET): performance investigation of a steep slope, high on-current device through 3D non-equilibrium green function simulations", chapter in "Semiconductor-On-Insulator Materials for NanoElectronics Applications"	2011		Scientific Community, Industry		International
26.	Book chapter	T. Rudenko et al ISP-Kiev, UCL	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on " Special features of the back-gate effects in ultra-thin body SOI MOSFETs", chapter in "Semiconductor-On-Insulator Materials for NanoElectronics Applications"	2011		Scientific Community, Industry		International
27.	Book chapter	H.-N. Nguyen et al UPS	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on " Ohmic and Schottky contact SNTFET: transport properties and device performance using semi-classical and quantum particle simulation""	2011		Scientific Community, Industry		International
28.	Book chapter	M. Pala, GRENOBLE INP	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Quantum simulation of Silicon-Nanowire FETs"	2011		Scientific Community, Industry		International
29.	Book chapter	G. Gibaudo, GRENOBLE INP	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Mobility characterization in advanced FD-SOI CMOS devices"	2011		Scientific Community, Industry		International
30.	Book chapter	J.-P. Raskin et al UCL	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on " Sensing and MEMS devices in thin-film SOI MOS technology"	2011		Scientific Community, Industry		International
31.	Book chapter	M. Bawedin et al. GRENOBLE INP, Leti	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Floating-body SOI memory: the scaling tournament"	2011		Scientific Community, Industry		International
32.	Book chapter	W. van den Daele et al GRENOBLE INP, IMEC	Wiley (S. Luryi et al. eds) "Future Trends in Microelectronics, from Nanophotonics to Sensors and Energy	GeOI as a platform for ultimate devices	2010		Scientific Community, Industry		International
33.	Book chapter	S. Cristoloveanu et al. GRENOBLE INP, Leti, ST	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "A selection of SOI puzzles and tentative answers"	2011		Scientific Community, Industry		International

34.	Book chapter	GRENOBLE INP/FMNT	Wiley (S. Luryi et al. eds)	Silicon-based devices and materials for nanoscale CMOS and beyond-CMO, chapter in "Future Trends in Microelectronics, from Nanophotonics to Sensors and Energy"	2010		Scientific Community, Industry		International
35.	Publication	E. Kasper, USTUTT	Horizons in World Physics. Volume 273 (ISBN: 978-1-61728-995-8)	Positioning Ge-Dots on Si for Device Applications/Book chapter /pp. 171-185	2010		Scientific Community, Industry		International
36.	Thesis	N. Reckinger UCL, IEMN, FZ Jülich, CNRS/LPN		Fabrication and characterization of rare-earth silicide thin films	11 February 2011	Louvain-la-Neuve	Scientific Community	40	Belgium
37.	PhD Thesis	B. Raeissi Chalmers		Charge carrier traffic at interfaces in nanoelectronic structures, ISSN 1652-0769, 2010	2010		Scientific Community, Industry		Worldwide
38.	Thesis	ETHZ		Scattering in Nanoscale Devices	2010	Zurich	Scientific Community, Industry		International
39.	PhD Thesis	J. Piscator, Chalmers	ISBN 978-91-7385-281-4	Influence of electron charge states in nanoelectronic building blocks	2009		Scientific Community, Industry		Internationa
40.	Thesis	ETHZ		Band Structure Effects and Quantum Transport	2010	Zurich	Scientific Community, Industry		International
41.	Web site	-Sinano Institute -Grenoble INP -UCL		Nanosil Project					All
42.	Film	-Sinano Institute -Grenoble INP -KTH -IUNET, UCL		Sinano Institute					All (film on the web site)
43.	Poster	-UCL -Sinano Institute -Grenoble INP		Nanosil 2008					All
44.	Worskhop	GRENOBLE INP/FMNT, NCSR	Euro Nano Day	Invited, European Nanoelectronics: the Initiatives and Networks of the Academic Community	May 2010	Grenoble, France	Scientific Community, Industry, Policy makers		International
45.	Workshop	GRENOBLE INP/FMNT	Minatec Crossroads	Invited, European Research Roadmap for Nanoelectronics	June 2010	Grenoble, France	Scientific Community, Industry, Policy makers		International
46.	Workshop	INPG/FMNT, Warwick, AMO Gmbh, RWTH Aachen, KTH, IUNET, UCL	INC6	NANOSIL FP7 European Network of Excellence	May 2010	Grenoble, France	Scientific Community, Industry, Policy makers		International
47.	Workshop	E. Kasper, USTUTT	5th International WorkShop on New	High frequency behaviour of Ge pin junctions	29-30	Sendai,	Scientific		International

			Group IV Semiconductor Nanoelectronics	/ Presentation / Digest of Papers (2010)1-3.	January 2010	Japan	Community, Industry		
48.	Workshop	E. Kasper, USTUTT	NANOSIL-Workshop Beyond-CMOS	Quantum Structures beyond CMOS / Presentation	23 February 2011	Aachen, Germany	Scientific Community, Industry		International
49.	Workshop	N. Sedghi et al LIVUNI, Julich	Wodim 2010	CV Measurements on $LaLuO_3$ Stack MOS Capacitor Using a New 3-Pulse Technique	28-30 June 2010	Bratislava, Slovakia	Scientific Community, Industry	150	worldwide
50.	Tutorial Course	B. Iñiguez	ESSDERC	Compact Thin-Film SOI MOSFET Modelling	2010	Sevilla (Spain)	Scientific Community, Industry		International
51.	Tutorial Course	B. Iñiguez	TCCM	Compact Small-Signal FET Modelling	2010	Tarragona (Spain)	Scientific Community, Industry		International
52.	Invited talk	KTH	27th International Conference on Microelectronics (MIEL)	Nanoscaling of MOSFETs and Implementation of Schottky Barrier S/D contacts	16-19 May 2010	NIS, Serbia	Scientific Community, Industry		International
53.	Invited talk	KTH	18th International Conference on Advanced Semiconductor Devices and Microssystems (ASDAM)	Nanoscaled SiGe based MOSFETs	2010	Smolenice , Slovakia	Scientific Community, Industry		International
54.	Invited talk	KTH	10th IEEE International Conference on Solid-State and Integrated Circuit Technology	Integration of metallic source/drain (MSD) contacts in nanoscaled CMOS technology	2010	Shanghai	Scientific Community, Industry		International
55.	Invited lecture	FZJ/ Buca	Seminar Invitation	Invited : From Strained Si to strained Si on Insulator	08.Nov. 2010	Shanghai China	Scientific Community, Industry	20	International
56.	Invited lecture	FZJ/ Mantl	Conference	High mobility Si-Ge channel and high-k materials for NanoMOSFETs	24-May 2010	Stockholm / Sweden	Scientific Community, Industry	100	International
57.	Invited lecture	FZJ/ Mantl	Nanosil Workshop		13.09. 2010	Seville, Spain	Scientific Community, Industry	50	International
58.	Invited lecture	R. Mroczyński	12th Polish Seminar “Ion techniques”	Plasma techniques applications in the technology of non-volatile semiconductor memory (NVSM) devices	2-5 March 2011	Szklarska Poręba, Poland	Scientific Community, Industry	approx. 100	PL
59.	Invited lecture	R. Mroczyński	XII Warsaw Festival of Science	How the integrated circuit is made…?	18 September 2010	Warsaw	Civil Society	approx. 20	PL
60.	Invited lecture	FZJ/ Mantl	International Symposium on Integrated Functionalities	Ternary high-k oxides for nanoscale logic devices	13.06. 2010	San Juan, Puerto Rico	Scientific Community, Industry	100	International
61.	Conference	GRENOBLE INP/FMNT	French−Ukrainian symposium and SemOI conference	INVITED, Elastic and inelastic scattering in SiNWs	October 2010	Kiev, Ukraine	Scientific Community		International
62.	Conference	GRENOBLE INP/FMNT	6th International SemOI Conference & 1st Ukrainian-French Seminar on SOI	Invited, Silicon-based devices and materials for nanoscale FETs	October 2010	Kiev, Ukrainia	Scientific Community		International

63.	Conference	GRENOBLE INP/FMNT	4th International Conference on Micro-Nanoelectronics, Nanotechnologies & MEMs	Invited, The Sinano Institute: European Networks and Projects in the fields of More Moore, More than Moore and Beyond-CMOS	December 2010	Athens, Greece	Scientific Community		International
64.	Conference	G. Iannaccone (IUNET)	European Conference on Nanotechnologies	Graphene as a material for nanoelectronics (invited - ab #1198 (INVITED)	26 April 2010	Vancouver	Scientific Community, Industry	100	World
65.	Conference	G.Iannaccone (IUNET)	SISPAD	Transport and noise properties of graphene-based transistors revealed through atomistic modelling, (INVITED)	6 September 2010	Bologna	Scientific Community, Industry	100	World
66.	Conference	T. Rudenko et al. ISP-Kiev, UCL	SemOI conference	Invited: Special Features of back-gate the back gate effect in ultra-thin body SOI MOSFETs	Oct 25-28, 2010	Kiev, Ukraine	Scientific Community	60	worldwide
67.	Conference	V. Kilchytska et al. UCL	SemOI conference	Invited: Effects of high–energy neutrons on advanced SOI MOSFETs	Oct 25-28, 2010	Kiev, Ukraine	Scientific Community	60	worldwide
68.	Conference	Afzalian et al. UCL, Tyndall	SemOI conference	Invited: Barrier Resonant Tunneling Transistor: Performance investigation of a Steep Slope, High On-Current device (invited)	Oct 25-28, 2010	Kiev, Ukraine	Scientific Community	60	worldwide
69.	Conference	P. Dollfus, UPS	1st Ukrainian-French Seminar on SOI materials, devices and cicuits	Invited: Ohmic and Schottky contact CNTFET: Transport properties and device performance using semi-classical and quantum particle simulation	24-28 October 2010	Kiev, Ukrainia	Scientific Community, Industry	50	International
70.	Conference	P. Dollfus, UPS	14th International Workshop on Computational Electronics (IWCE 2010)	Invited: Quantum transport of Dirac fermions in graphene nanostructures, Proc.: p.39-44	27-29 October 2010	Pisa, Italy	Scientific Community, Industry	80	International
71.	Conference	A. G. Nassiopoulou, IMEL	International Conference on Nanomaterials (ICN 2010)	Invited talk: "Nanostructures on Si by Electrochemistry and their Applications"	27-29 April 2010	Kottayam, India	Scientific Community, Industry	250 people	International
72.	Conference	A. G. Nassiopoulou, IMEL	7th International Conference on Porous Semiconductors Science and Technology – PSST 2010	Tutorial: “Porous Si for Electronics and Sensors”	14-19 March 2010	Valencia, Spain	Scientific Community, Industry	220 people	International
73.	Conference	A. G. Nassiopoulou, IMEL	VCIAN Conference on Interactions Among Nanostructures 2010	Invited talk: “Photoluminescence from silicon nanocrystal ensembles: effect of exciton migration and role of surface vibration modes”	21-25 June 2010	Santorini, Greece	Scientific Community, Industry	80 people	International
74.	Conference	A. G. Nassiopoulou, F. Balestra, IMEL	Sixth International Nanotechnology Conference on Communication and Cooperation	Invited talk: “European Nanoelectronics: The Initiatives and Networks of the Academic Community”	17-20 May 2010	Grenoble, France	Scientific Community, Industry	80 people	International
75.	Conference	JP Colinge, Tyndall	6th International SemOI Workshop on Nanoscaled Semiconductor-on-Insulator Materials, Sensors an Devices	Junctionless transistors: physics and properties -INVITED	Nov. 2010	Ukraine	Scientific Community, Industry	100	All
76.	Conference	O. Engström Chalmers	219 ECS Meeting	Invited: Electron states in MOS system (to be presented)	May 1 – 6, 2011	Montreal	Scientific Community, Industry	Estimated 200	Worldwide
77.	Conference	O. Engström Chalmers/ITE	INFOS 2011	Invited:Future high-k gate stacks: Report from a tour in the periodic system (Tutorial to be	June 21 – 23, 2011	Grenoble	Scientific Community,	Estimated 100	Worldwide

				given)			Industry		
78.	Conference	O, Engstrom Chalmers	218 ECS Meeting,	Invited: Multiparameter Admittance Sepctroscopy	Oct. 10 – 15, 2010	Las Vegas	Scientific Community, Industry	150	Worldwide
79.	Conference	INPG/FMNT	IWCE	Influence of Ionized Impurities in Silicon Nanowire MOS Transistors, pp. 137	May 2009	Beijing, China	Scientific Community		International
80.	Conference	INPG/FMNT, IMEC	ESSDERC'2010	Experimental Analysis of Surface Roughness Scattering in FinFET devices, Proc. pp 305-308	13-17 September 2010,	Sevilla, Spain	Scientific Community		International
81.	Conference	L. Donetti, et al Granada, Warwick, KTH	ULIS 2011	On the effective mass of holes in inversion layers	Mar 14-16, 2011	Cork, Ireland	Scientific Community, Industry		International
82.	Conference	E. Simoen, et al Warwick, IMEC	10th Int. Conf. on Solid-State and Integrated Circuit Technology (IC-SICT 2010)	Low-frequency noise in strained and relaxed Ge pMOSFETs, p891	Nov 1-4, (2010)	Shanghai, China	Scientific Community, Industry		International
83.	Conference	J. Mitard, et al Warwick, IMEC	2010 Int. Conf. on Solid State Devices and Materials (SSDM 2010)	High Hole-Mobility 65nm Biaxially-Strained Ge-pFETs: Fabrication, Analysis and Optimization, p. C-9-2	22-24 Sept (2010)	Tokyo, Japan	Scientific Community, Industry		International
84.	Conference	M. Myronov, et al Warwick,	14th International Conference on Vapor Growth and Epitaxy (ICVGE-14)	Monolayer thickness control during epitaxial growth of high Ge content strained Ge/SiGe multilayers by RP-CVD	August 8-13, 2010	Beijing, China	Scientific Community, Industry		International
85.	Conference	Van Huy Nguyen, et al Warwick,	UK Semiconductors,	Defect Evaluation in Ge and $Si_{1-x}Ge_x$ Epitaxial Layers using an Iodine-Based Selective Etchant	July 7-8 (2010)	Sheffield, UK	Scientific Community, Industry		UK
86.	Conference	A. Dobbie, et al Warwick,	UK Semiconductors,	Thermal Stability of Strained Ge Layers Grown on Reverse-Graded $Si_{0.2}Ge_{0.8}$ Relaxed Buffers by RP-CVD	July 7-8 (2010)	Sheffield, UK	Scientific Community, Industry		UK
87.	Conference	V.A. Shah et al. Warwick,	UK Semiconductors,	Thickness studies of high quality Ge layers on Si (001) substrates.	July 7-8 (2010)	Sheffield, UK	Scientific Community, Industry		UK
88.	Conference	Xue-Chao Liu, et al Warwick,	UK Semiconductors,	Growth and characterization of $Ge/Si_{0.4}Ge_{0.6}$ multiple quantum wells	July 7-8 (2010)	Sheffield, UK	Scientific Community, Industry		UK
89.	Conference	A. Dobbie, et al Warwick,	E-MRS 2010 Spring Meeting	Relaxation of Strained Germanium Layers Grown on $Si_{0.2}Ge_{0.8}$ Relaxed Buffers by RP-CVD with in-situ H_2 Annealing	June 7-11, 2010	Strasbourg, France	Scientific Community, Industry		International
90.	Conference	M. Myronov, et al. Warwick,	E-MRS 2010 Spring Meeting	Epitaxial growth of Ge layers by RP-CVD using Digermane precursor	June 7-11, 2010	Strasbourg, France	Scientific Community, Industry		International
91.	Conference	M. Myronov et al. Warwick,	E-MRS 2010 Spring Meeting	Highly strained Si epilayers grown on SiGe/Si(100) virtual substrates by RP-CVD	June 7-11, 2010	Strasbourg, France	Scientific Community, Industry		International
92.	Conference	V.A. Shah,	ISTDM 2010	High quality relaxed Ge layers grown directly	24-26 May	Stockholm	Scientific		International

		Warwick,		on a Si (001) substrate.	2010	, Sweden	Community, Industry		
93.	Conference	Xue-Chao Liu et al Warwick,	ISTDM 2010	Non-destructive thickness characterization of Si and Ge based heterostructure by x-ray diffraction and reflectivity	24-26 May 2010	Stockholm , Sweden	Scientific Community, Industry		International
94.	Conference	A. Dobbie et al Warwick,	MRS Spring Meeting	Investigation of the Thermal Stability of Strained Ge Layers by Reduced-Pressure Chemical Vapour Deposition on Relaxed $Si_{0.2}Ge_{0.8}$ Buffers	April 5-9 2010	San Francisco, USA	Scientific Community, Industry		International
95.	Conference	S.M.Thomas, et al Warwick, Glasgow, NXP	ULIS 2010	Low temperature effective mobility measurements and modelling of high-k gated Si n-MOS and p-MOS devices	17-19 March 2010	Glasgow, UK	Scientific Community, Industry		International
96.	Conference	G. Iannaccone IUNET	International Workshop on Computational Electronics	A multi-scale approach for performance assessment of hydrogenated graphene Field-Effect Transistors	28 October 2010	Pisa	Scientific Community, Industry	150	World
97.	Conference	A. Betti IUNET	International Workshop on Computational Electronics	Enhanced shot noise in carbon nanotube FETs due to electron-hole interaction	28 october 2010	Pisa	Scientific Community, Industry	150	World
98.	Conference	V.Bonfiglio IUNET	International Workshop on Computational Electronics	Evaluation of threshold voltage dispersion in 45 nm CMOS technology with TCAD-based sensitivity analysis	27 october 2010	Pisa	Scientific Community, Industry	150	World
99.	Conference	A. Betti IUNET	IEDM 2010	Full band assessment of phonon-limited mobility in Graphene NanoRibbons,	8 december 2010	San Francisco	Scientific Community, Industry	100 (session) - 1200 Conf	World
100.	Conference	Afzalian et al. UCL	ESSDERC	Breaching the kT/Q Limit with Dopant Segregated Schottky Barrier Resonant Tunneling MOSFETs: a Computationnal Study	Sept. 13-17 2010	Sevilla, Spain	Scientific Community	600	worldwide
101.	Conference	Afzalian et al. UCL, Tyndall	EUROSOI Conference	Variable Barrier Resonant Tunneling Transistor: A New Path Towards Steep Slope and High On-Current?	25-27 January, 2010	Grenoble, France	Scientific Community	150	worldwide
102.	Conference	Vikram Passi et al UCL, IEMN, LITEN-CEA	Electrochemical Society Conference - 2011	Functionalization of Silicon Nanowires for Specific Sensing	1-May-2011 – 5-May-2011	Montreal, Canada	Scientific Community		worldwide
103.	Conference	V. Kilchytska et al. UCL, IMEC	EuroSOI 2010	Gate-edge charges related effects and performance degradation in advanced multiple-gate MOSFETs	January2010	Grenoble, France	Scientific Community	150	Worldwide
104.	Conference	M.K.Md Arshad et al. UCL, Leti	ULIS 2010	Improved DIBL in Ultra Thin Body SOI MOSFETs with Ultra Thin Buried Oxide and Inverted Substrate	March 2010	Glasgow, UK	Scientific Community	150	Worldwide
105.	Conference	V. Kilchytska et al. UCL, IMEC	ESREF 2010	High-energy neutrons effect on strained and non-strained SOI MuGFETs and planar MOSFETs	October 2010	Gaeta, Italy	Scientific Community	600	Worldwide
106.	Conference	J. Conde at al. UCL,Cinestav-Mexico	MIEL 2010	3D Simulation of Triple-Gate MOSFETs	May 2010	Nis, Serbia	Scientific Community		Worldwide

107.	Conference	I. Garduno et al, UCL, Cinestav-Mexico	MIEL 2010	Modeling of main leakage currents and their contribution to channel current in Fin-FETs	May 2010	Nis, Serbia	Scientific Community		Worldwide
108.	Conference	V. Kilchytska et al. UCL, Leti, UNEW	EuroSOI 2011	Ultra-thin body and BOX SOI Analog Figures of Merit	January2011	Granada, Spain	Scientific Community	150	Worldwide
109.	Conference	T. Rudenko et al. UCL, ISP-Kiev	EuroSOI 2011	Impact of mobility variation on threshold voltage extraction by transconductance change and gm/Id methods in advanced SOI MOSFETs	January2011	Granada, Spain	Scientific Community	150	Worldwide
110.	Conference	V. Kilchytska et al. UCL,Leti	ULIS 2011	High-temperature perspectives of UTB SOI MOSFETs	March 2011	Cork, Ireland	Scientific Community	100	Worldwide
111.	Conference	T. Rudenko et al. UCL, ISP-Kiev	ULIS 2011	Influence of Drain Voltage on MOSFET Threshold Voltage Determination by Transconductance Change and gm/Id Methods	March 2011	Cork, Ireland	Scientific Community	100	Worldwide
112.	Conference	S. Makoveev et al. UNEW, UCL, Leti	ULIS 2011	Self-Heating and Substrate Effects in Ultra-Thin Body Ultra-Thin BOX Devices	January2011	Cork, Ireland	Scientific Community	100	Worldwide
113.	Conference	V. Passi et al. (UCL,ISEN-IEMN)	Micro Electro Mechanical Systems Conf., MEMS'2010	Backgate bias and stress level impact on giant piezoresistance effect in thin silicon films and nanowires'	2010	Hong-Kong	Scientific Community, Industry	1000	International
114.	Conference	X.L. Han et al. (ISEN-IEMN)	European Material Research Society Spring Meeting	Fabrication and electrical characterization of dense vertical Si nanowires arrays	June 2010	Strasbourg France	Scientific Community, Industry	500	International
115.	Conference	X.L. Han (ISEN-IEMN)	36th International Conference on Micro & Nano Engineering (MNE2010)	Realization of ultra dense arrays of vertical silicon NWs with defect free surface and perfect anisotropy using a top-down approach	19-22 Sept 2010	Genoa Italy	Scientific Community, Industry	250	International
116.	Conference	F.M. Bufler, Synopsys, ETHZ, UPS, IUNET	14th International Workshop on Computational Electronics (IWCE 2010)	Comparison of semiclassical transport formulations including quantum corrections for advanced devices with high-k gate stacks, Proc.: p.319-322	27-29 October 2010	Pisa, Italy	Scientific Community, Industry	80	International
117.	Conference	V. Talbo, UPS	14th International Workshop on Computational Electronics (IWCE 2010)	Fully self-consistent simulation of silicon nanocrystal-based single-electron transistors, Proc.: p. 151-154	27-29 October 2010	Pisa, Italy	Scientific Community, Industry	80	International
118.	Conference	V. Hung Nguyen, UPS	15th International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2010), Proc. p.	Quantum transport of Dirac fermions in graphene field effect transistors, Proc.: p. 9-12	6-8 September 2010	Bologna, Italy	Scientific Community, Industry	80	International
119.	Conference	M. Schmidt, H.D.B. Gottlob, J. Bolten, T. Wahlbrink, H. Kurz / AMO	Ultimate Integration on Silicon (ULIS)	Mobility Extraction in sub 10nm Nanowire nMOSFETs with Gadolinium-Silicate as Gate Dielectric	16 March 2011	Cork, Ireland	Scientific Community, Industry	about 55	International
120.	Conference	A. Karmous, USTUTT	Ultimate Integration on Si ULIS2011	Ge Quantum Dot Schottky diode operated in a 89GHz Rectenna / Poster / ULIS2011 Proc.	14-16 March 2011	Cork, Ireland	Scientific Community,		International

				pp. 74-76			Industry		
121.	Conference	H. Xu, USTUTT	The Eleventh Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, SiRF 2011	Integrated W-Band RECTENNA (Rectifying Antenna) with Ge Quantum Dot Schottky Diode/ Presentation	17-19 January 2011	Phoenix, Arizona, USA	Scientific Community, Industry		International
122.	Conference	Turchanikov, V., et al. IMEL, ISP-Kiev	27th International Conference on Microelectronics, MIEL 2010 - Proceedings	"Comparative studies of single- and double-nanocrystal layer NVM structures: Charge accumulation and retention", pp. 103-104	2010	Nis, Serbia	Scientific Community, Industry	150 people	International
123.	Conference	S. Gardelis and A. G. Nassiopoulou, IMEL	7th International Conference on Porous Semiconductors Science and Technology – PSST 2010	Colleration of light emission properties with exciton migration in silicon nanocrystal ensembles	14-19 March 2010	Valencia, Spain	Scientific Community, Industry	220 people	International
124.	Conference	JP Colinge, Tyndall	EUROSOI Conference	Substrate bias effects in MuGFETs	Jan. 2011	Grenoble	Scientific Community, Industry	100	All
125.	Conference	JP Colinge, Tyndall	EUROSOI Conference	3D Simulation of RTS Amplitude in Accumulation-Mode and Inversion-Mode Trigate SOI MOSFETs	Jan. 2011	Grenoble	Scientific Community, Industry	100	All
126.	Conference	JP Colinge, Tyndall	EUROSOI Conference	Comparison of Breakdown Voltage in Bulk and SOI FinFETs	Jan. 2010	Grenoble	Scientific Community, Industry	100	All
127.	Conference	JP Colinge, Tyndall	WOLTE 9 - Ninth International Workshop on Low Temperature Electronics	Low Temperature Behavior of Junctionless Multiple Gate nMOSFETs	Aug 2010	Brazil	Scientific Community, Industry	100	All
128.	Conference	JP Colinge, Tyndall	ESSDERC	Junctionless Nanowire Transistor (JNT): Properties and Design Guidelines	Sept 2010	Spain	Scientific Community, Industry	200	All
129.	Conference	JP Colinge, Tyndall	Solid-State Devices and Materials Conference (SSDM)	Analysis of the Junctionless Transistor Architecture	Sept 2010	Japan	Scientific Community, Industry	200	All
130.	Conference	JP Colinge, Tyndall	Solid-State Devices and Materials Conference (SSDM)	Short-Channel Junctionless Nanowire Transistors	Sept 2010	Japan	Scientific Community, Industry	200	All
131.	Conference	JP Raskin, UCL, Tyndall	IEEE International SOI Conference	Mobility Improvement in Nanowire Junctionless Transistors by Uniaxial Strain	Oct 2010	USA	Scientific Community, Industry	100	All
132.	Conference	JP Colinge, Tyndall	EUROSOI 2011	Comparison of the switching speed in junctionless and accumulation-mode gate-all-around nanowire transistors	Jan 2011	Spain	Scientific Community, Industry	100	All
133.	Conference	A. Nazarov, ISP-Ukraine, Tyndall	EUROSOI 2011	Extraction of flat-band voltage and parasitic resistance in junctionless MuGFETs	Jan 2011	Spain	Scientific Community, Industry	100	All
134.	Conference	R. T. Doria, USP-Brazil, Tyndall	EUROSOI 2011	Analytical Model for the Threshold Voltage of Junctionless Nanowire Transistors	Jan 2011	Spain	Scientific Community, Industry	100	All
135.	Conference	JP Colinge, Tyndall	ULIS 2011	Performance Investigation of Short-channel Junctionless Multigate Transistors	March 2011	Ireland	Scientific Community, Industry	100	All

136.	Conference	Tyndall-UCC	INFOS 2011	Investigation of bulk defects in amorphous and crystalline HfO2 thin films	21 June 2011	Grenoble	Scientific Community, Industry	~ 150 to 200	International
137.	Conference	Yuri Y. Gomeniuk ISP Kiev, Tyndall-UCC	INFOS 2011	Transport and Interface States in High-k LaSiOx Dielectric	21 June 2011	Grenoble	Scientific Community, Industry	~ 150 to 200	International
138.	Conference	Yuri Y. Gomeniuk ISP –Kiev, yndall-UCC, KTH, AMO, Jülich	6th SemOI Conference and 1st Ukrainian-French Seminar	Electrical properties of high-k LaLuO3 gate oxide for SOI MOSFETs	24-26 October 2010	Kyiv	Scientific Community, Industry	~ 150	International
139.	Conference	Yuri Y. Gomeniuk ISP-Kiev, Tyndall-UCC, AMO, Jülich, Chalmers	ECS-218 (2010)	Electrical Properties of LaLuO3/Si(100) Structures Prepared by Molecular Beam Deposition	13 October 2010	Las Vegas	Scientific Community, Industry		International
140.	Conference	Tyndall-UCC, AMO, Jülich	WoDiM 2010	The onset of electrical stress in 3nm and 6nm molecular beam deposited LaLuO3 MOSCAPs on n-Si(100) substrates using a TiN metal gate and an Al back contact	28-30th June 2010	Bratislava, Slovakia	Scientific Community, Industry		International
141.	Conference	M. Balaguer, et al, URV, UGR	EUROSOI	An analytical compact model for Schottky-Barrier Double Gate MOSFETs	January 2010	Grenoble (France)	Scientific Community, Industry		International
142.	Conference	G. Darbandy, et al, URV	EUROSOI	Analytical Modeling of Direct Tunnelling Current through SiO2/high-k Gate Stacks for the Determination of Suitable High-k Dielectrics for Nanoscale Double-Gate MOSFETs	January 2010	Grenoble (France)	Scientific Community, Industry		International
143.	Conference	R. Ritzenthaler, et al. URV, CEA/Leti, INPG	EUROSOI	A 2D analytical model of threshold voltage for Pi-gate FinFET transistors	January 2010	Grenoble (France)	Scientific Community, Industry		International
144.	Conference	M. Cheralathan, et al URV	ULIS	Compact potential and current model for long-channel doped cylindrical surrounding-gate MOSFETs	March 2010	Glasgow (UK)	Scientific Community, Industry		International
145.	Conference	R. Ritzenthaler, et al. URV, CEA/Let, INPG	40th European Solid-State Device Research conference (ESSDERC)	3D Analytical Modelling of Subthreshold Characteristics in Pi-gate FinFET Transistors	September 2010	Sevilla (Spain)	Scientific Community, Industry		International
146.	Conference	R. Ritzenthaler et al. URV, CEA/Let, INPG	IEEE International SOI conference	Parasitic Back-Inferface Conduction in Planar and Triple-Gate SOI Transistors	2010	San Diego (USA)	Scientific Community, Industry		International
147.	Conference	M. Schwarz, et al URV	ULIS	2D closed-form model for the source/drain orthogonal electric field in lightly-doped Schottky-Barrier Double-Gate MOSFETs	2010	Glasgow (UK)	Scientific Community, Industry		International
148.	Conference	M. Schwarz, et al URV	ESSDERC Fringe Poster Session	2D Analytical Calculation of the Tunneling Current in Lightly Doped Schottky Barrier Double-Gate MOSFET	2010	Sevilla (Spain)	Scientific Community, Industry		International
149.	Conference	M. Schwarz, et al URV	MIXDES	Analytical 2D Model for the Channel Electric Field in Undoped Schottky Barrier Double-Gate MOSFET	2010	Wroclaw (Poland)	Scientific Community, Industry		International
150.	Conference	G. Darbandy, et al	EUROSOI	Study of Potential High-k Dielectrics for sub	2011	Granada	Scientific		International

		URV		15 nm UTB SOI MOSFETs, Using Analytical Models of the Gate Tunneling Leakage		(Spain)	Community, Industry		
151.	Conference	R. Ritzenthaler, et al URV, CEA/Let, INPG	EUROSOI	A Short-Channel Analytical Model for Triple-gate and Planar FDSOI Transistors	2011	Granada (Spain)	Scientific Community, Industry		International
152.	Conference	M. Cheralathan, et al URV, UGR	EUROSOI	A Compact Double-Gate MOSFET Model Consistent with a MultiSubband Ensemble Monte Carlo Model	2011	Granada (Spain)	Scientific Community, Industry		International
153.	Conference	M. Schwarz, et al URV	EUROSOI	2D Analytical Calculation of the Current in Lightly Doped Schottky Barrier DG MOSFET	2011	Granada (Spain)	Scientific Community, Industry		International
154.	Conference	M. Cheralathan,et al URV, UGR, IUNET	ULIS	Analytical Drain Current Model Reproducing Advanced Transport Models in nanoscale Double-Gate (DG) MOSFETs	2011	Cork (Ireland)	Scientific Community, Industry		International
155.	Conference	T. Holtij,et al URV	ULIS	2D Analytical Calculation of the Source/Drain Access Resistance in DG-MOSFET Structures	2011	Cork (Ireland)	Scientific Community, Industry		International
156.	Conference	M. Schwarz, et al URV	ULIS	2D Analysis of Source/Drain Carrier Tunneling in Lightly Doped Schottky Barrier DG-MOSFETs Using a Fully Analytical Model	2011	Cork (Ireland)	Scientific Community, Industry		International
157.	Conference	UGR Jose Luis Padilla, Francisco Gamiz	ULIS-2010	Barrier lowering implementation in SB-MOSFETs on SOI substrates	16-18 March	Glasgow	Scientific Community, Industry		UK
158.	Conference	UGR Carlos Sampedro, Francisco Gamiz et al.	ULIS-2010	Channel Length impact on Velocity Overshoot in UTB-DGSOI	16-18 March	Glasgow	Scientific Community, Industry		UK
159.	Conference	B. Raeissi, Chalmers, ITE, AMO, FZ Julich	16th Workshop on Dielectrics in Microelectronics (Wodim)	Interface state properties of high-k/SiOx/Si interfaces portrayed by multiparameter admittance spectroscopy	June 28 – 30, 2010	Bratislava	Scientific Community, Industry	120	Worldwide
160.	Conference	O. Engström Chalmers, IMEP-LAHC, FZ Julich, AMO	16th Workshop on Dielectrics in Microelectronics (Wodim)	Capture cross sections for holes at LaLuO/Si interfaces	June 28 – 30, 2010	Bratislava	Scientific Community, Industry	120	Mostly European
161.	Conference	I.Z. Mitrovic et al LIVUNI, Julich	INFOS'2011	Study of interfaces and band offsets in TiN/amorphous $LaLuO_3$ gate stacks'	21-24 June 2011	Grenoble, France	Scientific Community, Industry	200	worldwide
162.	Conference	N. Sedghi et al LIVUNI, Julich	219th ECS Meeting	Investigation of Electron and Hole Charge Trapping in $LaLuO_3$ Stack MOS Capacitor Using the 3-Pulse CV Technique	1-6 May 2011	Montreal, Canada	Scientific Community, Industry	200	worldwide
163.	Conference	N. Sedghi/ LIVUNI, Julich	41st IEEE SISC 2010	Charge Trapping in $LaLuO_3$ MOS Capacitors using a New 3-Pulse CV Technique	2-4 December 2010	San Diego, USA	Scientific Community, Industry	200	worldwide
164.	Conference	S Makovejev, et al UNEW, UCL	SiRF	RF extraction of self-heating effects in FinFETs of various geometries	January 2011	Phoenix,USA	Scientific Community, Industry		International
165.	Conference	R Kapoor, et al	ESREF	Characterising gate dielectrics in high mobility	October	Italy	Scientific		International

		UNEW		devices using novel nanoscale techniques	2010		Community, Industry		
166.	Conference	S Makovejev, et al UNEW, UCL	ULIS	Self-heating effect characterisation in SOI FinFETs	March 2010	Glasgow, UK	Scientific Community, Industry		International
167.	Conference	E Escobedo-Cousin et al UNEW, UCL	MRS	Characterizing the effect of uniaxial strain on the surface roughness of Si nanowire MEMS-based microstructures	November 2010	Boston, USA	Scientific Community, Industry		International
168.	Conference	A. Asenov et al., GU	Custom Integrated Circuits Conference (CICC), 2010 IEEE	Modeling and Simulation of Transistor and Circuit Variability and Reliability	Sept. 2010	USA	Scientific Community, Industry		International
169.	Conference	A. Asenoc et al., GU	Design, Automation & Test in Europe Conference & Exhibition (DATE), 2010	Capturing Intrinsic Parameter Fluctuations using the PSP Compact Model	March 2010	Dresden	Scientific Community, Industry		International
170.	Conference	E. Sangiorgi et al. IUNET, WUT, GU, UPS,	MIEL conference	Drain Current Computation in Nanoscale nMOSFETs: Comparison of Transport Models	May 2010		Scientific Community, Industry		International
171.	Conference	A. Paussa et al. IUNET-Udine	International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)	Pseudo-Spectral Method for the Modelling of Quantization Effects in Nanoscale MOS Transistors	March 2010		Scientific Community, Industry		International
172.	Conference	P.Toniutti, et al IUNET-Udine	International Conference on Ultimate Integration on Silicon (ULIS)	Understanding the mobility reduction in MOSFETs featuring high-κ dielectrics	March 2010		Scientific Community, Industry		International
173.	Conference	V.Gudmundssonet al. IUNET-Udine and KTH	International Conference on Ultimate Integration	Multi-subband Monte Carlo simulation of fully-depleted silicon-on-insulator Schottky barrier MOSFETs	March 2010	UK	Scientific Community, Industry		International
174.	Conference	A. Betti G. Fiori, G. Iannaccone - IUNET Pisa	14th International Workshop on Computational Electronics, (IWCE 2010)	Enhanced shot noise in carbon nanotube FETs due to electron-hole interaction	Oct. 2010		Scientific Community, Industry		International
175.	Conference	G. Giusi, G. Iannaccone, D. Maji, F. Crupi - IUNET Pisa	10th IEEE International Conference on Solid-State and Integrated Circuit Technology (CSICT-2010)	Experimental extraction of barrier lowering and backscattering in saturated short-channel MOSFETs	Nov. 2010		Scientific Community, Industry		International
176.	Conference	G. Iannaccone, A. Betti, G. Fiori - IUNET Pisa	International Conference on Simulation of Semiconductor Processes and Devices, (SISPAD 2010)	Transport and noise properties of graphene-based transistors revealed through atomistic modelling	March 2010		Scientific Community, Industry		International
177.	Conference	G. Fiori, et al IUNET Pisa	14th International Workshop on Computational Electronics, (IWCE 2010)	A multi-scale approach for performance assessment of hydrogenated graphene Field-Effect Transistors	Oct. 2010		Scientific Community, Industry		International
178.	Conference	V. Bonfiglio, G. Iannaccone - IUNET Pisa	14th International Workshop on Computational Electronics, (IWCE 2010)	Evaluation of threshold voltage dispersion in 45 nm CMOS technology with TCAD-based sensitivity analysis	Oct. 2010		Scientific Community, Industry		International
179.	Conference	L. Silvestri, et al IUNET-Bologna	International Conference on Ultimate Integration on Silicon (ULIS)	Mobility Model for Electrons and Holes in FinFETs with High-κ Stacks, Metal Gate and Stress	March 2010	UK	Scientific Community, Industry		International
180.	Conference	A.T. Pham, TUBS	IWCE	Simulation of Landau quantization effects due to strong magnetic fields in(110) Si hole inversion	Oct. 2010		Scientific Community,		International

				layers			Industry		
181.	Conference	A.T. Pham, TUBS	ESSDERC	Comparison of Strained SiGe Heterostructure on Insulator (001) and (110) PMOSFETSs: C-V Characteristics, Mobility, and ON current	Sept. 2010	Spain	Scientific Community, Industry		International
182.	Conference	H. Xu, USTUTT	11th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)	Integrated W-band RECTENNA (rectifying antenna) with Ge quantum dot Schottky Diode	Feb. 2011		Scientific Community, Industry		International
183.	Conference	M. Schmidt, et al AMO, RWTH	11th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)	Mobility Extraction in sub 10nm Nanowire nMOSFETs with Gadolinium-Silicate as Gate Dielectric	Feb. 2011		Scientific Community, Industry		International
184.	Conference	J. Jasiński (WUT, FZJ)	10th ELTE Conference 2010	Influence of annealing temperature on MOSCAPs with LaLuO gate oxide	2010		Scientific Community, Industry		International
185.	Conference	M. Iwanowicz (WUT, AMO)	10th ELTE Conference 2010	Studies of the quality of GdSiO-Si interface	2010		Scientific Community, Industry		International
186.	Conference	M. Iwanowicz (WUT)	10th ELTE Conference 2010	Vector generator for pulse characterization of MOS devices	2010		Scientific Community, Industry		International
187.	Conference	J. Jasiński (WUT)	10th ELTE Conference 2010	Electrical characterization of MOSFETs with HfSiON gate	2010		Scientific Community, Industry		International
188.	Conference	R. Mroczyński (WUT)	WoDiM 2010	Reliability issues of double gate dielectric stacks based on hafnium dioxide (HfO_2) layers for non-volatile semiconductor memory (NVSM) applications	2010		Scientific Community, Industry		International
189.	Conference	M. Kalisz (WUT)	5th Wide Bandgap Materials - progress in synthesis and applications and 7th Diamond & Related Films jointly with 2nd International Workshop on Science and Applications of Nanoscale Diamond Materials, Zakopane, Poland	Effect of the Fluorine Implantation from r.f. CF_4 plasma on Electrical Characteristics of MIS Structures with PECVD Silicon Oxynitride Layers	2010		Scientific Community, Industry		International
190.	Conference	M. Kalisz (WUT)	10th Conference "Electron Technology", ELTE 2010, Wrocław, Poland	Improvement of immunity on MeV electron radiation of MOS structures by means of ultra-shallow fluorine implantation	2010		Scientific Community, Industry		International
191.	Conference	E. Gnani et al IUNET	ULIS 2011	Numerical Investigation on the Junctionless Nanowire FET	2011	Ireland	Scientific Community, Industry		International
192.	Conference	L. Knoll et al FFZJ	ULIS 2011	20 nm gate length Schottky MOSFETs with ultra thin NiSi/epitaxial NiSi2 source/drain	2011	Ireland	Scientific Community, Industry		International
193.	Conference	A. Martinez UG	ULIS	NEGF simulations of a junctionless Si gate-all-around nanowires transistor with discrete dopants	2011	Ireland	Scientific Community, Industry		International
194.	Conference	I. Ben-Akkez et al INPG, ST, CEA/Let	ULIS	Characterization and modeling of capacitances in FD-SOI devices	2011	Ireland	Scientific Community,		International

							Industry		
195.	Conference	A.Nazarov et al Tyndall-UCC, ISP-Kiev	ULIS	Extraction of channel mobility in nanowires MOSFETs using Id(Vg) characteristics	2011	Ireland	Scientific Community, Industry		International
196.	Conference	A. Kranti et al UCL	ULIS	Source/Drain engineering ultra low power analog/RF UTBB MOSFETs	2011	Ireland	Scientific Community, Industry		International
197.	Conference	J. El Husseini et al URV, IES Monrpelllier	ULIS	A surface potential based compact model for lightly doped FD SOI MOSFETs with ultra-thin body	2011	Ireland	Scientific Community, Industry		International
198.	Conference	A. Nichau et al FZJ	ULIS	Lanthanum Lutetium oxide integration in a gate-first process on SOI MOSFETs	2011	Ireland	Scientific Community, Industry		International
199.	Conference	X. Wand, et al GU	ULIS	Channel length dependence of statistical threshold voltage variability in extremely scaled HKMG MOSFETs	2011	Ireland	Scientific Community, Industry		International
200.	Conference	Q. Rafhay, et al. INPG, Cea/Let	ULIS	Revised approach for the characterization of GIDL	2011	Ireland	Scientific Community, Industry		International
201.	Conference	M. Schmidt, et al FZJ, CEA/Let	ULIS	Impact of strain and Ge concentration on the performance of planar SiGe band-to-band tunneling transistors	2011	Ireland	Scientific Community, Industry		International
202.	Conference	A. Hubert et al INPG, Leti	ESSDERC	Experimental comparison of programming mechanisms in 1T-DRAM	2010	Spain	Scientific Community, Industry		International
203.	Conference	C. Sampedro et al	ESSDERC	Multi-subband Monte Carlo Simulation of bulk MOSFETs for the 32nm-Node and beyond	2010	Spain	Scientific Community, Industry		International
204.	Conference	S.Narasimhamoorthy et al INPG/FMT	ESSDERC'2010	Parameter extraction of nanoscale MOSFETs using modified Y function method	September 2010	Sevilla, Spain	Scientific Community		International
205.	Conference	K. Boucart, et al. EPFL	ESSDERC'2010	A simulation-based study of sensitivity to parameter fluctuations of Si tunnel FETs	13-17 September 2010,	Sevilla, Spain	Scientific Community		International
206.	Conference	K. Tachi et al INPG/FMNT, CEA/Leti, ST,	ESSDERC'2010	SD Source/Drain doping optimization in multi-channel MOSFET	13-17 September 2010	Sevilla, Spain	Scientific Community		International
207.	Conference	S. Habicht, et al FZJ	ESSDERC'2010	Hole mobilities and electrical characteristics of omega-gated silicon nanowires array FETs with 110- and 100-channel orientation	13-17 September 2010,	Sevilla, Spain	Scientific Community		International
208.	Conference	N. Rodrigez, et al. INPG/FMNT, UGR	ESSDERC'2010	Origins of universal mobility violation in SOI MOSFETs	13-17 Sept. 2010	Sevilla, Spain	Scientific Community		International

A2. LIST OF DISSEMINATION ACTIVITIES FOR PERIOD 2 AND 1 (EXTRACTED FROM D5.2 AND D5.1)

NO	Title of conferences and workshops	Author(s)	Nanosil partners	Conference/ Workshop (title)	Date & Location	Type of presenta-tion (oral/ poster/ invited)	Status (done/acc epted/ submitted)
209.	Electrical Transport characterization of nano CMOS devices with ultra-thin silicon film	G. Ghibaudo et al.	INPG/ FMNT, CEA/LETI, ST, IMEC	9th International Workshop on Junction Technology (IWJT 2009)	11-12 June 2009, Kyoto, Japan	Invited keynote paper	Done
210.	SOI as a platform for transition from micro to nano	F. Balestra	INPG-FMNT	ECS Int. Symp. SOI Technology & Devices,	May 2009, San Francisco USA	Invited	Done
211.	Silicon-based devices and materials for nanoscale CMOS and beyond-CMOS	F. Balestra	INPG-FMNT	FTM'2009	June 2009, Sardinia	Invited	Done
212.	SOI- a platform for transition from micro to nano	F. Balestra	INPG-FMNT	IEEE International Semiconductor Conference-CAS	Oct.2009, Sinaia, Romania	Invited	Done
213.	Multi-gate Devices for High Performance, Ultra Low Power and Memory applications	F. Balestra	INPG-FMNT	ECS Int. Symposium "ULSI Process Integration"	Vienna, Austria, Oct. 2009	Invited	Done
214.	3D quantum transport simulations of Si Nanowires: impact of elastic and inelastic scattering	M.G. Pala	FMNT/ INPG	SINANO-NANOSIL Workshop	18 September 2009, Athens (Greece)	Invited	Done
215.	Ultra compact FDSOI transistors including strain and orientation : processing and performance	C. Fenouillet-Beranger, L. Pham Nguyen, P. Perreau, S. Denorme, F. Andrieu, O. Faynot, L. Tosti, L. Brevard, C. Buj, O. Weber, C. Gallon, V. Fiori, F. Boeuf, S. Cristolovea-nu, T. Skotnicki	FMNT/INPG, CEA-LETI	14th Int. Symposium on Silicon on Insulator Technology and Devices, 215th Meeting of the Electrochemical Soc.,	San Francisco, USA (25–29 mai 2009)	INVITED paper	Done
216.	Floating-body SOI memory: concepts, physics and challenges	M. Bawedin, S. Cristoloveanu, D. Flandre, F. Udrea	INPG/FMNT, UCL	14th Int. Symposium on Silicon on Insulator Technology and Devices, 215th ECS Meeting	San Francisco, USA (25–29 mai 2009)	INVITED paper	Done
217.	Cooltronics – a new silicon technology	D.R.Leadley, M.Prest, T.E.Whall, EHC. Parker, M. Meschke, J. Muhonen, J.P. Pekola, J. Ahopelto and M Prunnila	Warwick	9th Symposium Diagnostics and Yield: Advanced silicon devices for the ULSI era	Warsaw (2009)	Oral Invited	Done
218.	Accurate effective mobility extraction in SOI MOS transistors	S.M. Thomas, T.E. Whall, E.H.C. Parker, D.R. Leadley, R.J.P Lander, G. Vellianitis, J.R. Watling,	Warwick	9th Symposium Diagnostics and Yield: Advanced silicon devices for the ULSI era,	Warsaw (2009).	Oral Invited	Done
219.	Realization of globally strained Ge layers	M. Myronov and D.R. Leadley	Warwick	E-MRS 2009	Strasbourg, France, June 8-12, (2009) oral	Oral Invited	Done
220.	Schottky-Barrier Source/Drain MOSFET technology	P.-E. Hellström, M. Östling, V Gudmundsson, J. Luo, Z. Zhang, B. G. Malm and S.-L. Zhang	KTH	Design and Yield 2009	22-24 June, Warzawa	Oral/ Invited	Done

221.	Implementation of Schottky Barrier contact technology in ultra scaled MOSFETs	V. Gudmundsson, M Östling, P.-E. Hellström, J. Luo, Z. Zhang, Z. Qiu, B. G. Malm and S.-L. Zhang	KTH	1st Int.Workshop on Si based nano-electronics and –photonics SiNEP-09	20- 23rd September 2009	Oral/ Invited	Done
222.	"Perspectives of graphene nanoelectronics: probing technological options with modeling"	G. Iannaccone, G. Fiori, M. Macucci, P. Michetti, M. Cheli, A. Betti, P. Marconcini	IUNET	International Electron Device Meeting	2009 Baltimore	Invited	Done
223.	Opportunities and limitations of SOI technology: for RF applications	J.-P. Raskin	UCL	8th Diagnostics & Yield Symposium	June 22-24, 2009, Warsaw, Poland	invited	Done
224.	Assessment of advanced SOI technologies for high-temperature applications	J. Alvarado, V. Kilchytska, D; Flandre	UCL	8th Diagnostics & Yield Symposium	June 22-24, 2009, Warsaw, Poland	invited	Done
225.	SOI technology: an opportunity for RF designers?	J.-P. Raskin	UCL	EUROSOI – 2009, Fifth Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits	January 19-21, 2009, Göteborg, Sweden	invited	Done
226.	Metallic Source/Drain Architecture for Advanced MOS Technology: an overview	E. Dubois, G. Larrieu, N. Breil, R. Valentin, F. Danneville, D. Yarekha, N. Reckinger, X. Tang, A. Halimaoui, R. Rengel, E. Pascual, A. Pouydebasque, X. Wallart, S. Godey, J. Ratajczak, A. Laszcz, J. Katcki, J.P. Raskin, G. Dambrine, A. Cros, T. Skotnicki	ISEN-IEMN UCL ST ITE USAL	8th Symposium Diagnostics & Yield Advanced Silicon Devices and Technologies for ULSI Era	June 22-24, 2009, Warszawa, Poland	Oral Invited	Done
227.	Metallic source/drain for advanced MOS architectures: from material engineering to device integration	E. Dubois, G. Larrieu, N. Breil, R. Valentin, F. Danneville, D. Yarekha, N. Reckinger, X. Tang, A. Halimaoui, R. Rengel, E. Pascual, A. Pouydebasque, X. Wallart, S. Godey, J. Ratajczak, A. Laszcz, J. Katcki, J.P. Raskin, G. Dambrine, A. Cros, T. Skotnicki	ISEN-IEMN UCL ST ITE USAL	SINANO-NANOSIL Workshop Silicon-based CMOS and Beyond-CMOS Nanodevices	September 18, 2009, Athens	Oral Invited	Done
228.	Novel channel and dielectric materials for nanoelectronics	S.F. Feste, D. Buca, R.A. Minimisawa, Q.T. Zhao, J.M. Lopes, J. Schubert, B. Holländer, S. Mantl	FZJ	International Workshop on Si based nanoelectronics and photonics	Vigo, Spain 20 - 23 September 2009	Invited	Done
229.	Porous Si as a local substrate technology platform for on-chip electronic and sensor applications	A. G. Nassiopoulou	NCSR	TUAT/TEL International Workshop "Innovations of the Silicon, by the Silicon, for the Silicon"	18-9-2009 Tokyo	Invited	Done
230.	"Ordered arrays of SiO2 nanodots with embedded Si nanocrystals: Fabrication and characterization"	A. G. Nassiopoulou	NCSR	216th ECS Meeting – Vienna, Austria, E1 – Analytical Techniques for Semiconductor Materials and Process Cha-racterization	6-10-2009	Invited	Done
231.	"Silicon nanostructuring through self-assempled masking layers"	Nassiopoulou	NCSR	EMRS 2009_ Symposium M, Strasbourg,	9-13 June 2009	Invited	Done
232.	Advances in SOI Compact Modeling	B. Iñiguez, R. Ritzenthaler	URV	MOS-AK Workshop	Dec. 9, 2009, Baltomore (MA, USA)	Invited	Done

233.	CMOS: Is this the end of the beginning or the end of the end?	O. Engström	Chalmers	Nordic Semiconductor Meeting,	June 15 - 17, 2009 Reykiavik	Invited	Done
234.	Charging phenomena at the interface between high-k dielectrics and SiOx interlayers	O. Engström, B. Raeissi, J. Piscator, I.Z.Mitrovic, S. Hall, H.D.B.Gottlob, M. Schmidt, P. Hurley, K. Cherkaoui,	Chalmers, Liverpool, AMO, Tyndall	8th Symposium Diagnostics & Yield Advanced Silicon Devices and Technologies for the ULSI Era	June 22 - 24, 2009 Warsaw	Invited	Done
235.	Limitations in future high-k materials	O. Engström	Chalmers	NANOSIL Workshop at ESSDERC	Athens, Sept. 14 - 18, 2009	Invited	Done
236.	Classification of energy levels in quantum dot structures by means of depletion layer spectroscopy methods.	M.Kaniewska, O. Engström, M. Kaczmarczyk	ITE, Chalmers	13th International Conference on Defects-Recognition, Imaging and Physics in Semiconductors	Wheeling, West Virginia, USA, September 13-17, 2009	Invited	Done
237.	Sub-kT/q subthreshold slope transistors	A.M. Ionescu	EPFL	ESSDERC 2009	Athens, Sept. 14, 2009	Invited Tutorial	Done
238.	Simulation of gate leakage currents in UTB MOSFETs and Nanowires	A. Schenk	ETHZ	SINANO-NANOSIL Workshop "Silicon-based CMOS and Beyond-CMOS Nanodevices	Athens, September 18, 2009	Invited talk	Done
239.	Simulation of band-to-band tunneling in Si nanoscale devices: The role of junction profiles	A. Schenk	ETHZ	NODE Device Workshop	IBM Rüschlikon, Zürich, June 11, 2009	Invited	Done
240.	Rare earth silicate formation – a route towards high-k for the 22 nm node and beyond	I.Z. Mitrovic, S. Hall	Livuni	Diagnostics&Yield 2009	Warsaw, Poland, June 2009	invited	Done
241.	Charging phenomena at the interface between high-k dielectrics and SiOx interlayers	O. Engstrom, B. Raeissi, J. Piscator, I.Z. Mitrovic, S. Hall, H.D.B. Gottlob, M. Schmidt, P.K. Hurley, K. Cherkaoui	High-K HGang	Diagnostics&Yield 2009	Warsaw, Poland, June 2009	invited	Done
242.	Variability in Nanoscale CMOS and Nanowires	A. Asenov	UoG	NANOSIL Workshop at ESSDERC	Sept 09 Athens	Invited	Done
243.	Statistical variability and compact model strategies	A. Asenov	UoG	ECS Meeting	Sept 09 Vienna	Invited	Done
244.	Statistical variability: a roadblock for future scaling	A. Asenov	UoG	INSIGHT	April 09 Napa	Invited	Done
245.	Static and Low Frequency Noise Characterization of FinFET Devices	K. Bennamane, T. Boutchacha, G. Ghibaudo, M. Mouis, N. Collaert	INPG/FMNT, IMEC	Ultimate Integration on Silicon Conference (ULIS'2009)	March 18-20, 2009, Aachen (DE)	Oral	Done
246.	Full-3D real-space treatment of surface roughness in double gate MOSFETs	C. Buran, M. G. Pala, S. Poli, M. Mouis	INPG/FMNT, IUNET	Ultimate Integration on Silicon Conference (ULIS'2009)	March 18-20, 2009, Aachen	Oral	Done
247.	Full-3D real-space simulation of surface-roughness effects in double gate MOSFETs	C. Buran, M.G. Pala, S. Poli and M. Mouis	INPG/FMNT, IUNET	13th International Workshop on Computational Electronics (IWCE'2009)	May 27-29, 2009, Beijing (China)	Oral	Done
248.	Full-3D Real-Space Simulation of Surface-Roughness Effects in Double-Gate MOSFETs	C. Buran, M.G. Pala, M. Mouis, S. Poli	FMNT-INPG, IUNET	IWCE 2009,	27-29 May 2009 Page(s):1 - 4		Done
249.	Special effects in triple gate MOSFETs fabricated on silicon-on-insulator (SOI)	Y. Bae, K-I. Na, S. Cristoloveanu, W. Xiong, C.R. Cleavelin, J.-H. Lee	INPG/FMNT	2009 International Semiconductor Conference (CAS 2009), Volume 1, Page(s):51 - 56	October 12-14, 2009, Sinaia (Romania)	Oral	Done
250.	Backscattering coefficient in gate-all-around 3C-SiC nanowire FETs	K. Rogdakis, S. Poli, E. Bano, K. Zekentes, M.G. Pala	FMNT/INPG, IUNET	IEEE NANO 2009	26-30 July 2009, Genoa (Italy)	Oral	Done

251.	Low-temperature measurements on Germanium-on-Insulator pMOSFETs: evaluation of the background doping level and modeling of the threshold voltage dependence	W. Van Den Daele, E. Augendre, K. Romanjek, C. Le Roeyr, L. Clavelier, J–F. Damlencourt, E. Guiot, B. Ghyselen, S. Cristoloveanu	INRG/FMNT, CEA-LETI	14th Int. Symposium on Silicon on Insulator Technology and Devices, 215th ECS Meeting	San Francisco, USA (25–29 mai 2009)	Oral	Done
252.	Scalability of MSD memory effect.	A. Hubert, S. Ccristoloveanu, M. Bawedin, T. Ernst	INPG/FMNT, CEA-LETI	10th Int. Conference on Ultimate Integration of Silicon (ULIS'09)	Aachen, Germany, (18–20 mars 2009)	Oral	Done
253.	Study of Si Nanowires Growth by CVD-VLS and Physical Properties	T. Baron, F. Dhalluin, S. Bassem, B. Salhi, H. Abed, A. Potie, M. Panabière, S. Decossas, M. Kogelschatz, L. Montès, F. Oehler, P. Gentile, N. Pauc, M. Den Hertog, J. Rouvière, P. Noe and P. Ferret	INPG, LETI	216th ECS Meeting	October 4 - October 9, 2009 , Vienna, Austria	Oral	Done
254.	Electrical Characterization of Silicon Nanowires FET	B. Salem, H. Abed, F. Dhalluin, M. Panabière, T. Baron, P. Noe, F. Oelher, N. Pauc and P. Gentile	INPG, LETI	216th ECS Meeting	October 4 - October 9, 2009 , Vienna, Austria	Oral	Done
255.	Reverse graded virtual substrates for strained Ge devices	D. R. Leadley, V.A. Shah, A. Dobbie and M. Myronov	Warwick	UK Semiconductors 2009	July 1-2, 2009, Sheffield, UK	Oral	Done
256.	Characterisation of Strained Ge Epitaxial Layers Grown by RPCVD on Reverse Graded Si0.2Ge0.8 Relaxed Buffers	V.H. Nguyen, A. Dobbiew, M. Myronov, V.A. Shah, X-C. Liu and D.R. Leadley	Warwick	Institute of Physics Condensed Matter and Materials Physics Conference	Warwick, Dec 17-19 (2009).	Poster	Done
257.	TEM analysis of Ge-on-Si MOSFET structures with HfO2 dielectric for high performance PMOS device technology	DJ Norris, T Walther, AG Cullis, M Myronov, A Dobbie, T Whall, EHC Parker, DR Leadley, B De Jaeger, W Lee, M Meuris, J Watling and A Asenov	Warwick, IMEC, Glasgow	Microscopy of Semiconducting Materials 16 (2009) [Journal of Physics: Conference Series]	Oxford, UK, March 2009	Poster	Done
258.	Epitaxial growth of compressive strained Ge layers on reverse linearly graded virtual substrate by RP-CVD	M. Myronov, A. Dobbie, V.A. Shah and D.R. Leadley	Warwick	E-MRS 2009,	Strasbourg, France, June 8-12, (2009)	Oral	Done
259.	Effect of Si1-xGex Growth Rate on the Threading Dislocation Density in Fully Relaxed Si1-xGex/Si(100) Virtual Substrates Grown at High Temperature by RP-CVD	A. Dobbie, M. Myronov, X. Liu, E. H. C. Parker and D. R. Leadley	Warwick	E-MRS 2009,	Strasbourg, France, June 8-12, (2009)	Poster	Done
260.	Low temperature epitaxial growth of compressive strained Ge layers on reverse linearly graded virtual substrate by RP-CVD	M. Myronov, A. Dobbie, V.A. Shah and D.R. Leadley	Warwick	ICSI-6: 6th Int. Conf. Silicon Epitaxy and Heterostructures,	Los Angeles, California, USA, May 17 – 22, (2009)	Oral	Done
261.	Accurate effective mobility extraction in SOI MOS transistors	S.M. Thomas, T.E. Whall, E.H.C. Parker, D.R. Leadley, R.J.P Lander, G. Vellianitis, J.R. Watling	Warwick	ULIS 2009	Aachen, Germany (2009)	Poster	Done
262.	Si/SiO2 Quantum Well Solar Cells Based on Lateral Charge Carrier Transport	B. Berghoff, S. Suckow, R. Rölver, B. Spangenberg, H. Kurz	RWTH	24th European Photovoltaic Solar Energy Conference and Exhibition (EU PVSEC)	Hamburg, 21-24.09. 2009	poster	Done
263.	Comparison of measurement and simulation of charge transport in selective energy contacts based on Si quantum dots	S. Suckow, B. Berghoff, B. Spangenberg, H. Kurz	RWTH	24th European Photovoltaic Solar Energy Conference and Exhibition (EU PVSEC)	Hamburg, 21-24.09. 2009	poster	Done

264.	Quantum wells based on Si/SiOx stacks for nano-structured absorbers	B. Berghoff, S. Suckow, R. Rölver, B. Spangenberg, H. Kurz, A. Sologubenko J. Mayer	RWTH	E-MRS Spring Meeting, Symposium B: Inorganic and Nanostruc-tured Photovoltaics	Strasbourg, June 8-12, 2009.	Oral	Done
265.	Geometric broadening in resonant tunneling through Si quantum dots	S. Suckow, B. Berghoff, B. Spangenberg, H. Kurz	RWTH	E-MRS Spring Meeting Symposium B: Inorganic and Nanostruc-tured Photovoltaics	Strasbourg, June 8-12, 2009.	Oral	Done
266.	Characterization of dopant segregated Schottky barrier source/drain contacts	V. Gudmundsson, P.-E. Hellström, S.-L. Zhang and M. Östling	KTH	ULIS2009	19-20 March, Aachen	Oral	Done
267.	"Performance analysis of graphene bilayer transistors through tight-binding simulations", pp. 85-88.	G. Fiori, G. Iannaccone	IUNET	13th International Workshop on Computational Electronics	2009 Bejing	Oral	Done
268.	"Model of 1D Schottky barrier transistor operating far from equilibrium".	P. Michetti, G. Iannaccone	IUNET	IEEE NANO 2009	2009 Genoa	Oral	Done
269.	"Physical insights on nanoscale FETs based on epitaxial graphene on Si".	M. Cheli, P. Michetti, G. Iannaccone	IUNET	ESSDERC 2009	2009 Athens	Oral	Done
270.	"Analytical and TCAD-supported Approach to Evaluate Intrinsic Process Variability in Nanoscale MOSFETs".	V. Bonfiglio, G. Iannaccone	IUNET	ESSDERC 2009	2009 Athens	Oral	Done
271.	"Shot noise analysis in quasi one-dimensional Field Effect Transistors"	A. Betti, G. Fiori, G. Iannaccone	IUNET	20th International Conference on Noise and Fluctuations	2009 Pisa	Oral	Done
272.	"Comparison of advanced transport models for nanoscale MOSFETs"	P. Palestri, C. Alexander, A. Asenov, G. Baccarani, A. Bournel, M. Braccioli, B. Cheng, P. Dollfus, A. Esposito, D. Esseni, A. Ghetti, C. Fiegna, G. Fiori, V. Aubry-Fortuna, G. Iannaccone, A. Martinez, Majkusiak B., S. Monfray, S. Reggiani, C. Riddet, J. Saint-Martin, E. Sangiorgi, A. Schenk, L. Selmi, L. Silvestri, J. Walczak	IUNET UGLAS IMEP ETHZ STM TUW L2M	10th International Conference on Ultimate Integration of Silicon	2009 Aachen	Oral	Done
273.	"Physical insights on graphene nanoribbon mobility through atomistic simulations"	A. Betti, G. Fiori, G. Iannaccone	IUNET	International Electron Device Meeting	2009 Baltimore	Oral	Done
274.	Revised analysis of Coulomb scattering limited mobility in biaxially strained silicon MOSFETs	F. Driussi and D.Esseni	IUNET-UD	European Solid State Device Research Conference (ESSDERC)	Athens, Sept. 2009	oral	Done
275.	Experimental and physics-based modeling assessment of strain induced mobility enhancement in FinFETs	N. Serra, F. Conzatti, D. Esseni, M. De Michielis, P. Palestri, L. Selmi, S. Thomas, T.E. Whall, E.H.C. Parker, D.R. Leadley, L. Witters, A. Hikavyy, M.J. H¨ytch, F. Houdellier, E. Snoeck, T.J. Wang, W.C. Lee, G. Vellianitis, M.J.H. van Dal, B. Duriez, G. Doornbos and R.J.P. Lander	IUNET-UD	Electron Device Meeting (IEDM), paper 4.2	Dec. 2009	oral	Done
276.	Drain / Substrate Coupling Impact on DIBL of Ultra Thin Body and Box SOI MOSFETs with undoped Channel	S. Burignat, MK. Md Arshad, D. Flandre, V. Kilchytska, F. Andrieux, O.Faynot P. Scheiblin and J.-P. Raskin	UCL, CEA-LETI	ESSDERC 2009 Conference	September 14-19, Athènes, Grèce (2009), pp.141-144.	Oral	Done

277.	Substrate effects in sub-32 nm Ultra Thin SOI MOSFETs with Thin Buried Oxide,.	S. Burignat, D. Flandre, V. Kilchytska, F. Andrieux, O.Faynot and J.-P. Raskin	UCL, CEA-LETI	EuroSOI Conference 2009,	January 19-21, Göteborg, Sweden (2009)	Oral	done
278.	Transconductance and Mobility Behaviors in UTB SOI MOSFETs with Standard and Thin BOX,	T. Rudenko, S. Burignat, V. Kilchytska, S. Burignat, J.-P. Raskin, F. Andrieu, O. Faynot, A. Nazarov, V. Lysenko, D. Flandre	UCL, CEA-LETI, ISP Kiev	EuroSOI Conference 2009,	January 19-21, Göteborg, Sweden (2009)	Oral	Done
279.	Continuous compact model for MuGFETs simulations.	J. Alvarado, V. Kilchytska, D; Flandrea, J. Conde, M. Estrada, A. Cerdeira,	UCL	16th Inernational Conf ; on Mixed Design of Integrated Circuits and Systems	25-27 June 2009, Lodz, Poland		Done
280.	Self-aligned single-electron memory fabrication based on Si/SiGe/Si heterostructures	X. Tang, F. Ravaux, E. Dubois, E. Kasper, A. Karmous, N. Reckinger, J.-P. Raskin	UCL, IEMN, USTUTT	35th International Conference on Micro & Nano Engineering (MNE),	28 Sept. - 1 Oct. 2009 Ghent, Belgium.	poster	Done
281.	TEM characterization of poly-silicon and silicide fin fabrication processes of FinFETs	J. Ratajczak, A. Aszcz, A. Czerwinski, J. Katcki, X. Tang, N. Reckinger, D. Yarecha, G. Larrieu, E. Dubois	UCL, IEMN	Polish National Conference - Nano2009	June 22-26, 2009, Warsaw	poster	Done
282.	Issues associated to rare earth silicide integration in ultra thin FD SOI Schottky barrier nMOSFETs	G. Larrieu, D. Yarekha, E. Dubois, N. Breil, N. Reckinger, X. Tang, A. Halimaoui	UCL, IEMN	215th ECS Meeting	24-29 may 2009 in San Francisco, USA	oral	Done
283.	UHV Fabrication of the Ytterbium Silicide as Potential low Schottky Barrier S/D Contact Material for n-type MOSFET	D. Yarekha, G. Larrieu, N. Breil, E. Dubois, S. Godey, X. Wallart, C. Soyer, D. Remiens, N. Reckinger, X. Tang, A. Laszcz, J. Ratajczak, A Halimaoui	UCL, IEMN	215th ECS Meeting	24-29 may 2009 in San Francisco, USA	poster	Done
284.	High-Frequency Performance of Dopant-Segregated NiSi S/D SOI SB-MOSFETs	C. Urban, M. Emam, C. Sandow, Q.-T. Zhao, A. Fox, J.-P. Raskin, S. Mantl	UCL, FZJ	ESSDERC 2009 Conference	September 14-19, Athènes, Grèce (2009)	oral	Done
285.	Realization of vertical silicon nanowire networks with an ultra high density by top-down approach	X.L. Han, G. Larrieu, E. Dubois	ISEN-IEMN	International Conference on Nanoscience and Technology	1-3 Sep 09, Shanghai, China	Oral	Done
286.	Monte Carlo study of ambipolar transport and quantum effects in carbon nanotube transistors	H. Nha Nguyen, S. Retailleau, D. Querlioz, A. Bournel, P. Dollfus	UPS	SISPAD 2009	September 9-11, 2009, San Diego, USA	poster	Done
287.	Effects of edge roughness on the spin-dependent transport in armchair graphene nanoribbon structures	V. Hung Nguyen, V. Nam Do, A. Bournel, V. Lien Nguyen, P. Dollfus	UPS	EDISON 16	August 20-24, 2009, Montpellier, France	poster	Done
288.	Decoherence due to electron-phonon scattering in semiconductor nanodevices	D. Querlioz, J. Saint-Martin, P. Dollfus	UPS	IWCE 2009	May 27-29 2009, Beijing, China	oral	Done
289.	Sequential transport in a two-dot device	A. Valentin, S. Galdin-Retailleau, P. Dollfus	UPS	IWCE 2009	May 27-29 2009, Beijing, China	oral	Done
290.	Wigner Monte Carlo simulation of CNTFET: Comparison between semi-classical and quantum transport	H. Nha Nguyen, D. Querlioz, S. Galdin-Retailleau, A. Bournel, P. Dollfus	UPS	IWCE 2009	May 27-29 2009, Beijing, China	oral	Done
291.	Effect of access resistance on apparent mobility reduction in nano-MOSFET	K. Huet, J. Saint-Martin, A. Bournel, D. Querlioz, P. Dollfus	UPS	ULIS 2009	March 18-20, Aachen, Germany	oral	Done

292.	Impact of strain on p-DGMOS performance using full-band Monte Carlo simulation	V. Aubry-Fortuna, K. Huet, A. Bournel, D. Rideau, C. Chassat, P. Dollfus	UPS	ULIS 2009	March 18-20, Aachen, Germany	oral	Done
293.	Mobility measurements in Gd silicate/TiN SOI and sSOI n-MOSFETs	M. Schmidt, H.D.B. Gottlob, D. Buca, S. Mantl and H. Kurz	AMO, FZ-Jülich	International Semiconductor Device Research Symposium (ISDRS 2009)	College Park, MD, USA, Dec. 9-11, 2009.	oral	Done
294.	Mobility Extraction of UTB n-MOSFETs down to 0.9 nm SOI thickness	M. Schmidt, M.C. Lemme, H.D.B. Gottlob, H. Kurz, F. Driussi, L. Selmi	AMO, IU.NET	International Conference on Ultimate Integration of Silicon (ULIS 2009)	March 18-20, 2009 - Aachen, Germany	oral	Done
295.	Scaling potential and MOSFET integration of thermally stable Gd silicate dielectrics	H.D.B. Gottlob, M. Schmidt, A. Stefani, M.C. Lemme, H. Kurz, I.Z. Mitrovic, W.M. Davey, S. Hall, M. Werner, P.R. Chalker, K. Cherkaoui, P.K. Hurley, J. Piscator, O. Engström, S.B. Newcomb	AMO, LIVUNI, Tyndall-UCC, Chalmers	Conference of Insulating Films on Semiconductors (INFOS 2009)	Cambridge, UK, June 29 - July 01, 2009	oral	Done
296.	Integration of Gd silicate / TiN gate stacks into SOI n-MOSFETs	M. Schmidt, H.D.B. Gottlob, A. Stefani, and H. Kurz	AMO	Conference of Insulating Films on Semiconductors (INFOS 2009)	Cambridge, UK, June 29 - July 01, 2009	poster	Done
297.	Platforms for planar & non-planar ultrathin silicon	M. Schmidt, H.D.B. Gottlob, J. Bolten, T. Wahlbrink, T. Mollenhauer, M. Bückins, T.E. Weirich, F. Dorn, J. Mayer, H. Kurz	AMO	EUROSOI 2009	Göteborg, Sweden, Jan. 19-21, 2009	oral	Done
298.	Uniaxial strain relaxation in He-implanted (110) oriented SiGe layers	D. Buca, RA. Minamisawa, H. Trinkaus, B. Holländer, V. Destefanis, JM. Hartmann, S. Mantl	FZJ	International Conference on Silicon Epitaxy and Hetero-structures	Los Angeles May 17-22, 2009	oral	Done
299.	Performance enhancement of uniaxially-tensile strained Si NW-nFETs fabricated by lateral strain relaxation of SSOI	Feste, S.F.; Knoch, J.; Habicht, S.; Buca, D.; Zhao, Q.T.; S. Mantl	FZJ	ULIS 2009	Aachen 18-20 March, 2009	oral	Done
300.	Strained and Unstrained Si Nanowire FETs	S.F. Feste, S. Habicht, Q.T. Zhao, D. Buca, and S. Mantl	FZJ	ESSDERC	Athens, Greece 14-18 Sept 2009	Oral	Done
301.	Investigation of Arsenic dopant segregation layers for scaled Schottky-Barrier MOSFETs	Feste, SF; Urban, C; Knoch, J; Zhao, QT; Buca, D; Breuer, U; Mantl S	FZJ	E-MRS Spring Meeting 2009	Strasbourg, June 08-12, 2009	Poster	Done
302.	Systematic study of SOI SB-MOSFETs with dopant segregation	C. Urban, Q. T. Zhao, C. Sandow, S. Lenk, S. Mantl	FZJ	EUROSOI 2009	Göteborg, Jan.19. – 21, 2009	Oral	Done
303.	Schottky Barrier Height tuning using Sb Segregation	C. Urban, Q. T. Zhao, C. Sandow, M. Müller, S. Mantl	FZJ	MAM 2009	Grenoble, Mar 8. – 9, 2009	Oral	Done
304.	High Performance Schottky Barrier MOSFETs on UTB SOI	C. Urban, C. Sandow, Q.-T. Zhao, S. Mantl	FZJ	ULIS 2009	Aachen, March 18-20, 2009	Oral	Done
305.	Ultra thin Ni-silicides with low contact resistance on SOI and strained-SOI	L. Knoll, Q.T. Zhao, S. Habicht, C. Urban, B. Ghyselen, S. Mantl	FZJ	Proc. of Intern. Conf. Solid State Dev. Mat.	Sendai, Japan, Oct. 7-9, 2009	Poster	Done
306.	Modeling of piezoresistive coefficients in Si hole inversion layers	A. T. Pham, C. Jungemann, B. Meinerzhagen	TUBS	Proceedings of ULIS, Aachen (Germany), 2009		oral	Done
307.	Simulation of mobility variation and drift velocity enhancement due to uniaxial stress combined with biaxial strain in Si PMOS	A. T. Pham, C. Jungemann, B. Meinerzhagen	TUBS	Proceedings of IWCE-13, pp. 45-48, Beijing (China), 2009		oral	Done

308.	MBE Growth of Ge Quantum Dot Structures in Oxide Windows	A. Karmous, O. Kirfel, M. Oehme, E. Kasper, and J. Schulze	USTUTT	E-MRS Symposium K: Semiconductor Nanostructures towards Electronic and Optoelectronic Device Applications II	June 8 - 12, 2009 Congress Center, Strasbourg, France	Oral	Done
309.	Charge pumping characterization of MOSFETs with HfSiON gate dielectric	K. Jasinski, G. Gluszko, L. Lukasiak, A. Jakubowski	WUT	14th Canadian Semiconductor Technology Conf. Nano and Giga Challenges in Electronics, Photonics and Renewable Energy	Aug. 10-14, 2009 Hamilton, Canada	poster	Done
310.	Signal generator for extensive characterization of MOS devices	M. Iwanowicz, Z. Pióro, L. Lukasiak, A. Jakubowski	WUT	14th Canadian Semiconductor Technology Conf. Nano and Giga Challenges in Electronics, Photonics and Renewable Energy	Aug. 10-14, 2009 Hamilton, Canada	poster	Done
311.	Charge pumping characterization of MOSFETs with SiO2/BaTiO3 as a gate stack	G. Gluszko, P. Firek, L. Lukasiak, J. Szmidt, A. Jakubowski	WUT	8th Symp. Diagnostics & Yield : Advanced Silicon Devices and Technologies for the ULSI Era	June 22-24 2009, Warszawa (Poland)	poster	Done
312.	Silicon oxynitride layers fabricated by Plasma Enhanced Chemical Vapor Deposition for CMOS devices	R. Mroczyński, R.B. Beck	WUT	216th Meeting of Electrochemical Society – EuroCVD-17 and CVD-17	October 4-9 2009, Vienna (Austria)	poster	Done
313.	Reliability issues of double gate dielectric stacks based of hafnium dioxide (HfO2) layers for non-volatile semiconductor memory (NVSM) applications	R. Mroczyński, R.B. Beck	WUT	8th Symp. Diagnostics & Yield : Advanced Silicon Devices and Technologies for the ULSI Era	June 22-24 2009, Warszawa (Poland)	poster	Done
314.	High Frequency and Noise Compact Model of Gate-All-Around MOSFETs Including Quantum Effects	B. Nae, A. Lázaro, B. Iñiguez	URV	EUROSOI Workshop	January 19-21 2009, Göteborg (Sweden)	Poster	Done
315.	A High Frequency Compact Noise Model for Double-Gate MOSFET Devices	A. Lázaro, A. Cerdeira, B. Nae, M. Estrada, B. Iñiguez	URV	20th International Conference on Noise and Fluctuations	June 14-19 2009, Pisa (Italy)	Oral	Done
316.	2D Physics-based Compact Model for Channel Length Modulation in Lightly Doped DG FETs	M. Weidemann, A. Kloes, M. Schwarz, B. Iñiguez	URV	International Conference on Mixed Design of Integrated Circuits (MIXDES)	June 25-27, Łódź (Poland)	Oral	Done
317.	2D physics-based compact model of channel length modulation for asymmetrically biased double-gate MOSFETs	M. Weidemann, A. Kloes, M. Schwarz, B. Iniguez	URV	ESSDERC Fringe	Sept. 14-19 2009, Athens (Greece)	Poster	Done
318.	2D analytical solution of potential in lightly doped Schottky barrier double-gate MOSFET	M. Schwarz, M. Weidemann, A.Kloes, B. Iñiguez	URV	ESSDERC Fringe	Sept. 14-19 2009, Athens (Greece)	Poster	Done
319.	2D Compact Modeling of the Threshold Voltage in Triple- and Pi-gate Transistors	R. Ritzenthaler, F. Lime, and B. Iñiguez, O. Faynot, S. Cristoloveanu	URV, CEA-LETI, INPG	International Semiconductor Device Research Conference (ISDRS 2009)	December 9-11, College Park, MA (USA)	Poster	Done
320.	Analytical Modeling of the Gate Tunneling Leakage for the Determination of Adequate High-K Dielectrics in 22 nm Double-Gate SOI MOSFETs	G. Darbandy, R. Ritzenthaler, F. Lime, I. Garduño, M. Estrada, A. Cerdeira and B. Iñiguez.	URV	International Semiconductor Device Research Conference (ISDRS 2009)	December 9-11 2009, College Park, MA (USA)	Oral	Done
321.	Two-Dimensional Model for the Potential Profile in a Short Channel Schottky Barrier DG-FET	M. Schwarz, M. Weidemann, A. Kloes, B. Iñíguez	URV	International Semiconductor Device Research Conference (ISDRS 2009)	December 9-11 2009, College Park, MA (USA)	Poster	Done

322.	Analysis and Modeling of the Pinch-Off Point in a Lightly Doped Asymmetrically Biased Double Gate MOSFET	M. Weidemann, A. Kloes, M. Schwarz, B. Iñiguez	URV	International Semiconductor Device Research Conference (ISDRS 2009)	Dec. 9-11 2009, College Park, MA (USA)	Poster	Done
323.	High frequency compact noise modelling of Multi-Gate MOSFETs	A. Lázaro, A. Cerdeira, B. Nae, M. Estrada and B. Iñiguez	URV	MOS-AK Workshop	April 3 2009, Frankfurt-Oder Germany	Poster	Done
324.	Modeling of the subthreshold characteristics of Triple-Gate Transistors: impact of the channel dimensions and back-gate bias	R. Ritzenthaler, F. Lime and B. Iñiguez	URV	MOS-AK Workshop	September 18 2009, Athens (Greece)	Poster	Done
325.	Wafer bonding strength increased by mobile ions.	Raeissi, Bahman; Sanz-Velasco, Anke; Engström, Olof:	Chalmes	EUROSOI 2009	Göteborg January 19 -21, 2009	Poster	Done
326.	The influence of orientation and strain on the transport properties of sal Trigate nMOSFETs	I.Tienda-Luna, A.Godoy, F.Ruiz, F.Gamiz	UGR	ESSDERC	Athens, Sept 209		Done
327.	Effect of arbitrary orientation and strain on Surrounding Gate Transistors	I.Tienda-Luna, A.Godoy, F.Ruiz, and F.Gamiz	UGR	International Workshop on Computational Electronics,	2009 (Beijing, China)		Done
328.	A-RAM: Novel capacitor-less DRAM memory	N.Rodriguez, S.Cristoloveanu, F.Gamiz	UGR, INP, LETI	IEEE Inetrnational SOI COnference	San FranciscoUSA		Done
329.	Quantization Effects in Silicided and Metal Gate MOSFETs	N.Rodriguez, F.Gamiz, R.Clerc, C.Sampedro, A.Godoy, G.Ghibaudo	UGR, INPG	ULIS 2009	March 2009 Aachen	oral	Done
330.	Comparison of the electrostatics of bulk and SOI trigate MOSFETs	F.Garcia-Ruiz, A.Godoy, I.Tienda-Luna, F.Gamiz	UGR	Symp. Of Elecrochemical Society	San Francisco		Done
331.	A model for robust electrostatic design of nanowire ETs with arbitrary polygonal cross sections	Luca de Michielis, Luca Selmi Adrian M. Ionescu	EPFL/ IUNET (Uni Udine)	ESSDERC 2009	Athens, Sept. 14, 2009	Oral	Done
332.	Improvement of the Effective Mass Approximation for Silicon Nanowires	A. Esposito, M. Frey, and A. Schenk	ETHZ	Colloque Numérique Suisse	University of Basel, April 24, 2009	poster	Done
333.	Boundary Conditions for Incoherent Quantum Transport	M. Frey, A. Esposito, and A. Schenk	ETHZ	International Workshop on Computational Electronics (IWCE-13)	Beijing, China, May 27-29, 2009		Done
334.	Impact of Strain on the Performance of high-k/metal replacement gate MOSFETs	X. Wang, S. Roy, and A. Asenov	UoG	Ultimate Integration on Silicon (ULIS 2009	Aachen Germany, March 18-20, 2009		Done
335.	Efficient simulation of 6s VT distribution due to random discrete dopants	D. Reid, C. Millar, G. Roy, S. Roy and A. Asenov	UoG	Ultimate Integration on Silicon (ULIS 2009	Aachen Germany, March 18-20, 2009	Oral	Done
336.	Estimate of Dielectric Density using Spectroscopic Ellipsometry	W. Davey, O. Buiu, I. Mitrovic, M. Werner, S. Hall, P. Chalker	Livuni	INFOS 2009	Cambridge UK June 2009	oral	Done
337.	3D analysis of strain in an electrically measured strained SiGe MOSFET	SH Olsen et al	UNEW	Microscopy of Semiconducting Materials (MSM)	Oxford, UK, March 2009	oral	Done
338.	A design methodology for maximizing the voltage gain of strained Si MOSFETs using the thickness of the silicon-germanium strain relaxed buffer as a design parameter	OM Alatise et al	UNEW	ISDRS	Washington DC, USA, December 2009	oral	Done

339.	Strain characterization of Si wires	L Sanderson, P Dobrosz, SH Olsen, SJ Bull, S Mantl and D Buca	UNEW, FZJ	International Conference on Metallurgical Coatings and Thin Films (ICMCTF)	San Diego, USA, April 2009	oral	Done
340.	Investigation of oxidation-induced strain in a top-down Si nanowire platform	M Najmzadeh, D Bouvet, A Ionescu, P Dobrosz and SH Olsen	UNEW, EPFL	INFOS	Cambridge, UK 2009	oral	Done
341.	Silicon nanowires with lateral uniaxial tensile stress profiles for high electron mobility gate-all-around MOSFETs	M Najmzadeh, L De Michielis, D Bouvet, P Dobrosz, SH Olsen and A Ionescu	UNEW, EPFL	Micro- Nano Engineering	Ghent, Belgium 2009	oral	Done
342.	Capturing intrinsic parameter fluctuations using the PSP compact model	B. Cheng, D. Dideban, N. Moezi, C. Millar, G. Roy, X. Wang, S.Roy, A. Asenov	UoG	DATE 2010			Done
343.	Analytical Modeling of Direct Tunnelling Current through SiO2/high-k Gate Stacks for the Determination of Suitable High-k Dielectrics for Nanoscale Double-Gate MOSFETs	G. Darbandy, R. Ritzenthaler, F. Lime, S. I. Garduño, M. Estrada, A. Cerdeira, and B. Iñiguez	URV	EUROSOI Workshop	January 25-27 2010, Grenoble (France)	poster	Done
344.	An analytical compact model for Schottky-Barrier Double Gate MOSFETs	M. Balaguer, B. Iñiguez, J. B. Roldán	URV, UGR	EUROSOI Workshop	January 25-27 2010, Grenoble	poster	Done
345.	A 2D analytical model of threshold voltage for Pi-gate FinFET transistors	R. Ritzenthaler, M. Tang, O. Faynot, F. Lime, F. Prégaldiny, C. Lallement, S. Cristoloveanu, and B. Iñiguez	URV, CEA-LETI, INPG	EUROSOI Workshop	January 25-27 2010, Grenoble (France)	oral	Done
346.	Substrate bias effects in MuGFETs	C.W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. Dehdashti-Akhavan, P. Razavi, J.P. Colinge	Tyndall, INPG, UCL	EUROSOI 2010	Grenoble, Jan 2010	Poster	Done
347.	3D Simulation of RTS Amplitude in Accumulation-Mode and Inversion-Mode Trigate SOI MOSFETs	Ran Yan, Ailbhe Cullen, Aryan Afzalian, Isabelle Ferain, Chi-Woo Lee, Nima Dehdashti, Pedram Razavi and J.P. Colinge	Tyndall, UCL	EUROSOI 2010	Grenoble, Jan 2010	Poster	Done
348.	Comparison of Breakdown Voltage in Bulk and SOI FinFETs	P. Razavi, R. Duane, R. Yan, I. Ferain, N. Dehdashti-Akhavan, R. Yu, C.W. Lee, J.P. Colinge	Tyndall	EUROSOI 2010	Grenoble, Jan 2010	Oral	Done
349.	Backgate bias and stress level impact on Giant Piezoresistance effect in thin silicon films and nanowires	V. Passi, F. Ravaux, E. Dubois, J.-P. Raskin	UCL IEMN	IEEE MEMS	23-28 January 2010 Hongkong	Poster	Done
350.	Gate-edge charges related effects and performance degradation in advanced multiple-gate MOSFETs	V. Kilchytska, J. Alvarado, N. Collaert, R. Rooyakers, S. Put, C. Claeys, D. Flandre	UCL, IMEC	EuroSOI 2010	January 2010, Grenoble	Oral	Done

351.	What is the killing advantage of multiple-gate SOI MOSFET?	F. Balestra	INPG-IMEP	5th EUROSOI Workshop	Goteborg, Sweden, January 2009	Invited, panel session	Done
351.	Status and trends in Nanoscale Si-based devices and materials	F. Balestra	Coordi-nator	9th International Conference on Solid-State and Integrated-Circuit Technology	Beijing, China (October 20-23, 2008)	Invited	Done
352.	New semiconductor Nanodevices	F. Balestra	Coordi-nator	International School on the Physics of Semiconducting Compounds 2008	Jaszowiec, Poland, June 2008	Invited	Done
353.	NANOSIL Network of Excellence: Silicon-based nanostructures and nanodevices for long-term nanoelectronics applications.	F. Balestra, E. Parker, D. Leadley, S. Mantl, E. Dubois, O. Engstrom, R. Clerc, S. Cristoloveanu, H. Kurz, J.P. Raskin, M. Lemme, A. Ionescu, E. Kasper, A. Karmous, M. Baus, B. Spangenberg, M. Ostling, E. Sangiogi, G. Ghibaudo, D. Flandre	All	European Materials Research Society (E-MRS 2008), Symposium J	Strasbourg, France (26-30 Mai 2008)	Invited	Done
354.	Mobility of strained and unstrained short channel MOSFETs: New insight by magnetoresistance	M. Cassé, F. Rochette, N. Bhouri, F. Andrieu, K. Romanjek, D.K. Maude, M. Mouis, G. Reimbold, F. Boulanger	CEA/LETI, INPG-IMEP	Symposium on VLSI Technology (VLSI 2008), Proceedings IEEE. pp. 170-1. Piscataway, NJ, USA	June 17-20, 2008, Honolulu, Hawaï (USA)	Oral	Done
355.	Emerging nanotechnology	T. Baron, B. Salem, F. Dhalluin, P. Gentile, N. Pauc, M. Den Hertog, J.L. Rouvière, P. Mur, B. De Salvo, P. Ferret, J. Dufourcq, S. Bodnar	FMNT-LTM, CEA	38th European Solid-State Device Research Conference (ESSDERC)	Edinburgh, UK (15-19 Sept 2008)	Invited	Done
356.	The Ge condensation technique: a solution for planar SOI/GeOI co-integration for advanced CMOS technologies?	B. Vincent, J.F. Damlencourt, Y. Morand, A. Pouydebasque, C. Le Royer, L. Clavelier, N. Dechoux, P. Rivallini, T. Nguyen, S. Cristoloveanu, Y. Campidelli, D. Rouchon, M. Mermoux, S. Deleonibus, D. Bensahel, T. Billon	STM, CEA-LETI, INPG-IMEP	European Materials Research Society (E-MRS 2008), Symposium J. Proceedings in Materials Science in Semiconductor Processing, Elsevier	Strasbourg, France (May 26-30, 2008)	Invited	Done
357.	A Mobility Extraction Method for 3D Multichannel Devices	C. Dupré, T. Ernst, E. Bernard, B. Guillaumot, N. Vulliet, P. Coronel, T. Skotnicki, S. Cristoloveanu, G. Ghibaudo and S. Deleonibus	CEA/LETI, STM, INPG-IMEP	38th European Solid-State Device Research Conference (ESSDERC'08)	Edinburgh, UK (15-19 Sept 2008)	Oral	Done
358.	Characterization methods for nanodevices.	S. Cristoloveanu	INPG-IMEP	38th European Solid-State Device Research Conference ESSDERC'08	Edinburgh, UK (15-19 Sept 2008)	Invited	Done
359.	Introduction of diamond into advanced FDSOI CMOS	J-P. Mazellier, O. Faynot, F. Andrieu, S. Cristoloveanu, S. Deleonibus	CEA-LETI, INPG-IMEP	4th EUROSOI Workshop	Cork, Ireland (23-25 janvier 2008)	Oral	Done
360.	Ge diffusion during Ge-condensation process	C.S. Beer, R.J.H. Morris, T.E. Whall, E.H.C. Parker and D.R. Leadley	Warwick	ISTDM	Taiwan, (May, 2008)	Poster	Done
361.	Ge-On-Insulator substrates formed by Ge condensation technique: fabrication, modeling and characterization.	J.F. Damlencourt, B. Vincent, C. Le Royer, P. Rivallin, E. Martinez, M.C. Roure, Y. Campidelli, D. Rouchon, T. Nguyen, S. Cristoloveanu, Y. Morand, S. Descombes, L. Clavelier	Grenoble INP	International Conference of Electronic Materials, sponsored by Int. Union of Materials Research Society (ICEM-IUMRS 2008)	Sydney, Australia (28 juillet - 1 août 2008)	Invited	Done

362.	Quantum transport in nanowire metal-oxide-semiconductor transistors: influence of dielectric confinement	M. Bescond, M. Lannoo, F. Michelini, N. Cavassilas, M. G. Pala	INPG, CNRS	ICPS	Rio de Janeiro, July 27- August 1, 2008	Poster	Done
363.	Full 3D Real-Space NEGF Simulation of Transport and Magnetotransport in Si-Nanowire FETs	C. Buran, M. G. Pala, M. Bescond and M. Mouis	INPG, CNRS	ESSDERC	Rio de Janeiro, July 27- August 1, 2008	Poster	Done
364.	Reverse graded SiGe/Ge/Si heterostructures for high-composition virtual substrates.	V.A.Shah, D.R.Leadley, D.Fulgoni, J.Parsons, E.H.C.Parker	Warwick	E-MRS	Strasbourg (May 2008)	Oral	Done
365.	Channel Backscattering Characteristics of High Performance Germanium pMOSFETs	A. Dobbie, B. De Jaeger, M. Meuris, T.E. Whall, E.H.C. Parker and D.R. Leadley	Warwick, IMEC	ULIS	Udine, Italy (March, 2008)	Oral	Done
366.	Anomalous Ge diffusion effects during Ge-condensation	C.S. Beer, T.E. Whall, R.J.H. Morris, E.H.C. Parker and D.R. Leadley	Warwick	ULIS	Udine, Italy (March, 2008)	Poster	Done
367.	The role of interface states in the low temperature mobility of hafnium-oxide gated Ge-pMOSFETs and the effect of a hydrogen anneal	C.S. Beer, T.E. Whall, E.H.C. Parker, D.R. Leadley, B. De Jaeger, G. Nicholas, P. Zimmerman and M. Meuris	Warwick, IMEC	ULIS	Udine, Italy (March, 2008)	Oral	Done
368.	Relaxation of Strained Silicon on Si0.5Ge0.5 Virtual Substrates	J. Parsons, R.J.H. Morris, D.R. Leadley and E.H.C. Parker	Warwick	ULIS	Udine, Italy (March, 2008)	Poster	Done
369.	Confinement and Transport in Silicon Based Quantum Structures	B. Berghoff, R. Rölver, B. Spangenberg, D. Bätzner, H. Kurz, A. Dimyati. A. Sologubenkoo, J. Mayer	RWTH	33rd IEEE Photovoltaic Specialists Conference,	San Diego, 11.05-16.05. (2008)	oral	Done
370.	Towards Schottky-Barrier Source/Drain MOSFETs	M. Östling, V. Gudmundsson, P.-E. Hellström, B.G. Malm, Z. Zhang, S.-L. Zhang	KTH	2008 9TH International Conference on Solid-State and Integrated-Circuit Technology	October 20-23, Beijing, China	Invited presentation	Done
371.	Substrate impact on sub-32 nm Ultra Thin SOI MOSFETs with Thin Buried Oxide	S. Burignat, D. Flandre, V. Kilchytska, F. Andrieux, O. Faynot and J.-P. Raskin	UCL, CEA	EuroSOI 2009	Jan. 2009 Gothenburg	oral	Done
372.	Transconductance and Mobility Behaviors in UTB SOI MOSFETs with Standard and Thin BOX	T. Rudenko, V. Kilchytska, S. Burignat, J.–P. Raskin, F. Andrieu, O. Faynot, A. Nazarov, V.S. Lysenko and D. Flandre	UCL, CEA	EuroSOI 2009	Jan. 2009 Gothenburg	oral	Done
373.	Impact of channel doping on Schottky barrier height and investigation on p-SB MOSFETs performance	G. Larrieu, E. Dubois, D. Yarekha, N. Breil, N. Reckinger, X. Tang, J. Ratajczak, A. Laszcz	IEMN UCL	e-MRS Spring Meeting	26-30 May 2008 Strasbourg	Oral	Done
374.	Selective etching of implanted silicon-dioxide in hydrofluoric acid	V. Passi, A. Lecestre, E. Dubois, J.P. Raskin	UCL IEMN	34th Conference on Micro and Nano Technology	September 15-18, 2008, Athens	Oral	Done
375.	Investigation on the Platinum Silicide Schottky Barrier Height Modulation using a Dopant Segregation Approach	N. Breil, A. Halimaoui, E. Dubois, E. Lampin, Ludovic Godet, George Papasouliotis, Guilhem Larrieu	IEMN	MRS-Spring Meeting, Mater. Res. Soc	24-28 April 2008 San Francisco	oral	Done
376.	Impact of channel doping on Schottky barrier height and investigation on p-SB MOSFETs performance	G. Larrieu, E. Dubois, D. Yarekha, N. Breil, N. Reckinger, X. Tang, J. Ratajczak, A. Laszcz	IEMN UCL	e-MRS Spring Meeting	26-30 May 2008 Strasbourg	Oral	Done
377.	Selective etching of implanted silicon-dioxide in hydrofluoric acid	V. Passi, A. Lecestre, E. Dubois, J.P. Raskin	UCL IEMN	34th Conference on Micro and Nano Technology	September 15-18, 2008, Athens	Oral	Done
378.	DC and RF characteristics of a 60 nm FinFET for a wide temperature range	J. C. Tinoco, B. Parvais, A. Mercha, S. Decoutere, J-P Raskin	UCL, IMEC	EUROSOI – 2008	Tyndall January 23-25, 2008	Oral	Done

379.	Revised RF extraction methods for deep submicron MOSFETs"	J. C. Tinoco and J.-P. Raskin,	UCL	38th European Microwave Week 2008	Amsterdam, October 28-31, 2008, pp. 127-130.	Oral	Done
380.	RF-extraction methods for MOSFET series resistances: a fair comparison	J. C. Tinoco and J.-P. Raskin,	UCL	Seventh International Caribbean Conference on Devices, Circuits and Systems	Cancun, Mexico, April 28-30, 2008, paper 64, pp. 1-6.	Oral	Done
381.	Optimizing FinFET Geometry and Parasitics for RF applications	A. Kranti, J.-P. Raskin and G. A. Armstrong,	UCL	IEEE International SOI Conference, SOI'2008,	New York, USA, October 6-9, 2008, pp. 123-124.	Oral	Done
382.	Impact of temperature reduction and channel engineering on the linearity of FD SOI nMOSFETs	M. de Souza1, D. Flandre, J. A. Martino, E. Simoen, C. Claeys, M. A. Pavanello;	UCL, IMEC	EuroSOI 2009	Jan. 2009, Gothenburg,	Oral	Done
383.	Experimental and Theoretical Analysis of Hole Transport in Uniaxially Strained pMOSFETs	K. Huet, M. Feraille, D. Rideau, R. Delamare V. Aubry-Fortuna, M. Kasbari, S. Blayac, C. Rivero, A. Bournel, C. Tavernier, P. Dollfus, H. Jaouen	UPS, STM	ESSDERC 2008	15-19 Sept., Edinburgh, UK	oral	Done
384.	Wigner Monte Carlo approach to quantum transport in nanodevices	P. Dollfus, D. Querlioz, J. Saint-Martin, V. Nam Do, A. Bournel	UPS	SISPAD 2008	9-11 Sept., Hakone Japan	invited	Done
385.	On the Wigner Formalism of Quantum Transport in Semi-conductor Nanodevices	P. Dollfus, D. Querlioz, J. Saint-Martin, V. Nam Do, A. Bournel	UPS	AMSN 2008	15-21 Sept., Nha Trang, Viet Nam	invited	Done
386.	Electron-phonon interaction in silicon quantum dots	A. Valentin, J. Sée, S. Galdin-Retailleau, P. Dollfus	UPS	ULIS 2008	13-14 March, Udine, Italy	oral	Done
387.	Particle Monte Carlo approach to semi-classical and quantum transport in CNTFET within a multiscale simulation framework from atoms to circuit	P. Dollfus, S. Galdin-Retailleau, H. Cazin d'Honincthun, H. Nha Nguyen, D. Querlioz, A. Bournel	UPS	CCTN 08	28 June, 2008 Mont-pellier, France	invited	Done
388.	Static and dynamic performance of CNTFETs using particle Monte Carlo simulation	H. Nha Nguyen, H. Cazin d'Honincthun, P. Dollfus, A. Bournel, S. Galdin-Retailleau	UPS	NT 08	29 Jun. - 4 Jul., Mont-pellier, France	poster	Done
389.	Electronic transport and spin polarization effects in single graphene barrier structures	V. Nam Do, V. Hung Nguyen, P. Dollfus, A. Bournel	UPS	NT 08	29 Jun. - 4 Jul., Mont-pellier, France	poster	Done
390.	Effect of edge disorder on the bandgap of graphene nanoribbons	D. Querlioz, Y. Apertet, A. Valentin, K. Huet, A. Bournel, S. Galdin-Retailleau, P. Dollfus	UPS	NT 08	29 Jun. - 4 Jul., Mont-pellier, France	poster	Done
391.	Platforms for planar & non-planar ultrathin silicon	M. Schmidt, H.D.B. Gottlob, J. Bolten, T. Wahlbrink, T. Mollenhauer, M. Bückins, T.E. Weirich, F. Dorn, J. Mayer, H. Kurz	AMO	EUROSOI 2009	19.01.2009 Gotenburg, Sweden	oral	Done
392.	Leakage current effects on C-V plots of high-k MOS capacitors	Y. Lu, S. Hall, L. Z. Tan, I. Z. Mitrovic, W. M. Davey, B. Raeissi, O. Engstrom, K. Cherkaoui, S. Monaghan, P. K. Hurley, H.D.B. Gottlob, and M. C. Lemme	LIVUNI, Chalmers, AMO, Tyndall	Workshop on Dielectrics in Microelectronics WoDiM 2008	June 23 – 25, 2008 in Bad Saarow (Berlin), Germany	poster	Done

393.	Quest for an Optimal Gadolinium Silicate Gate Dielectric Stack	I.Z. Mitrovic, M. Werner, W.M. Davey, S. Hall, P.R. Chalker, H.D.B. Gottlob, M.C. Lemme, O. Engstrom, K. Cherkaoui and P.K. Hurley	LIVUNI, Chalmers, AMO, Tyndall	39th IEEE Semiconductor Interface Specialists Conference SISC 2009	December 11-13, 2008 San Diego, (CA), USA	poster	Done
394.	Small-Signal Compact Modelling of Multi-Gate MOSFETs	B. Iñiguez	URV	IEEE EDS Mini-Colloquium on Advanced Electron Devices Technology & Modeling	Cambridge (UK), September 12 2008	Invited lecture	Done
395.	Porous anodic alumina thin films on Si as masking layers for silicon surface nanostructuring and as templates for nanostructure growth	A. G. Nassiopoulou, V. Gianneta, F. Zacharatos, M. Kokonou, M. Hauffman	IMEL	1st IC4N-2008: International Conference from Nanoparticles and Nanomaterials to Nanodevices and Nanosystems	Halkidiki, Greece, 16-18 June 2008	Invited	Done
396.	Structural, chemical and light emission properties of very thin anodic silicon films fabricated by short single current pulses	S. Gardelis, A. G. Nassiopoulou, F. Petraki, S. Kennou, I. Tsiaoussis, N. Frangis	IMEL	XXIV Panhellenic Conference on Solid State Physics and Materials Science	Heraklion, Crete, September 21-24, 2008	Invited	Done
397.	Advanced compact modeling techniques of nanoscale Multi-Gate MOSFETs	B. Iñiguez, A. Lázaro, O. Moldovan, B. Nae, A. Cerdeira	URV	IEEE Lester Eastman Conference	Newark (Delaware, USA), August 5-7 2008	Invited lecture	Done
398.	Compact Modeling Techniques in Thin Film SOI MOSFETs	B. Iñiguez, D. Flandre	URV, UCL	MOS-AK Workshop	Edinburgh (UK), September 19 2008	Invited lecture	Done
399.	Finite element Simulations of parasitic capacitances related to multiple-gate field-effect transistors Architectures	O. Moldovan, D. Lederer, B. Iñiguez, J. P. Raskin	URV, Tyndall, UCL	8th IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF 2008)	Orlando (FL, USA), January 23-25 2008	Poster	Done
400.	Compact Charge and Capacitance Modeling of Undoped Ultra-Thin-Body SOI MOSETs	O. Moldovan, F. A. Chaves, D. Jimenez, B. Iñiguez	URV	EUROSOI 2008 Workshop	Cork (Ireland), January 23-25 2008	Poster	Done
401.	DC, RF and Noise Compact Model for FinFETs Including Quantum Effects	B. Nae, A. Lázaro, B. Iñiguez, F. García, M. Tienda-Luna, A. Godoy	URV, UGR	Conference on Design of Circuits and Integrated Systems (DCIS)	Grenoble (France), November 12-14 2008	Oral	Done
402.	Study of Ballisticity in SOI Nano-MOSFETs at Very Low Drain Bias	C. Sampedro, F. Gámiz, A. Godoy, S. Cristoloveanu and I. M. Tienda-Luna	UGR, INPG	EUROSOI 2008 Workshop	Cork (Ireland), January 23-25 2008	Oral presentation	Done
403.	Equivalent Oxide Thickness of SOI-GAA devices	F. J. García Ruiz, I.M. Tienda-Luna, L.Donetti, A.Godoy, F. Gámiz	UGR	EUROSOI 2008 Workshop	Cork (Ireland), January 23-25 2008	Poster	Done
404.	In-depth characterization of quantum effects in SOI MOSFETs for modeling purposes	J. B. Roldán, M. Balaguer, A. Godoy, F. G. Ruiz, F. Gámiz	UGR	EUROSOI 2008 Workshop	Cork (Ireland), January 23-25 2008	Poster	Done
405.	Impact of the top surface density of states on the characteristics of ultrathin SOI pseudo-MOSFETs	N. Rodriguez, S. Cristoloveanu, T. Nguyen, F. Gámiz	UGR, INPG	EUROSOI 2008 Workshop	Cork (Ireland), January 23-25 2008	Poster	Done

406.	Enhanced Electron Transport by Carrier Overshoot in Ultrascaled Double Gate MOSFETs	N. Rodriguez, L.Donetti, C.Sampedro, F.Martinez-Carricondo, F.Gamiz	UGR, INPG	ULIS-2008, The 9th International Conference On Ultimate Integration On Silicon	Udine (Italy), March 12-14 2008	Poster	Done
407.	Fully self-consistent k p solver and Monte Carlo simulator for hole inversion layers	L.Donetti, F.Gamiz, A.Godoy, N.Rodriguez	UGR, INPG	ESSDERC-2008, European Solid State Device Research Conference	Edinburgh (UK), September 15-19	Oral	Done
408.	Simulation of CMOS inverters based on the novel Surrounding Gate Transistors. A Verilog-A implementation	A.Roldán, J.B.Roldán, F.Gamiz	UGR	MOS-AK Workshop	Edinburgh (UK), September 19	Poster	Done
409.	A Revisited Pseudo-MOSFET Model for Ultrathin SOI Films	N.Rodriguez, S.Cristoloveanu, F.Gamiz	UGR, INPG	2008 IEEE International SOI Conference	New Palz, NY (USA), October 6-9	Poster	Done
410.	Gd silicate: A High-k Dielectric Compatible with High Temperature Annealing,	H.D.B. Gottlob, M. Schmidt, M.C. Lemme, H. Kurz, I.Z. Mitrovic, M. Werner, W.M. Davey, S. Hall, P.R. Chalker, K. Cherkaoui, P.K. Hurley, B. Raeissi, O. Engström, and S.B. Newcomb	AMO, Liverpool, Tyndall, Chalmers	Workshop on Dielectrics in Microelectronics (WoDiM 2008)	June 23 – 25, 2008 in Bad Saarow (Berlin), Germany	Oral	Done
411.	A generalized methodology for oxide leakage current metric,	O. Engström, J. Piscator, B. Raeissi, P. K. Hurley, K. Charkaoui, S,Hall, M.C.Lemme and H.D.B. Gottlob	Chalmers, Tyndall, Liverpool, AMO	Ultimate Integration on Silicon Conference (ULIS08),	March 2008, Udine	Poster	Done
412.	Comprehensive study of InAs/GaAs quantum dots by means of complementary methods	M. Kaczmarczyk, O. Engström, J. Piscator, M. Kaniewska, B. Surma, S. Lin and A. R. Peaker,	ITE, Chalmers	9th Exmatec,	June 2008, Lodz	Poster	Done
413.	Method for identifying confined electron states in quantum dot structures	M. Kaczmarczyk, O. Engström and M. Kaniewska	ITE, Chalmers	9th Exmatec	June 2008, Lodz	Poster	Done
414.	Metastable behaviorof 1 eV trap in InAs/GaAs quantum dot structures	G. Zaremba, O. Engström, M. Kaniewska and M. Kaczmarczyk	ITE, Chalmers	9th Exmatec,	June, 2008, Lodz	Poster	Done
415.	Characterization of deep elvels and quantum confined energy levels in InAs/ GaAs quantum dot structures by electrical methods	M. Kaniewska, O. Engström, M. Kaczmarczyk and G. Zaremba	ITE, Chalmers	ICCE 16, Kunming, China	July 2008	Oral	Done
416.	Deep level transient spectroscopy in quantum dot characterization,	O. Engström and M. Kaniewska	Chalmers, ITE	Villa Conference on Interaction among Nanostructures	February 2008, Orlando, Florida	Oral	Done
417.	Multiphonon capture of electrons at high-k-silicon interfaces	O. Engström, B. Raeissi and J. Piscator	Chalmers	Gordon Conference	August,2008 New London, New Hampshire	Poster	Done
418.	Electron traps at HfO2/SiOx interfaces	B. Raeissi, Y. Y. Chen, J. Piscator, Z. H. Lai and O. Engström	Chalmers	ESSDERC 2008	September 2008, Edinburgh	Oral	Done
419.	Future high-k gate stack materials	O. Engström	Chalmers	Tutorial given at ESSDERC 08.	September 2008, Edinburgh	Invited	Done
420.	High-k dielectrics and metal gates	O. Engström	Chalmers	MIGAS'08,	July, 2008, Autrans, France	Invited	Done
421.	Small slope switches	A.M. Ionescu	EPFL	Nanosil workshop @ ESDERC 2008	September 18th, Edinburg	oral	Done

422.	Determination of Physical Parameters for HfO2/SiOx/TiN MOSFET Gate Stacks by Electrical Characterization and Reverse Modeling	S. Monaghan, P. K. Hurley, K. Cherkaoui, M. A. Negara, and A. Schenk	ETHZ, Tyndall	ULIS'2008	Udine, Italy, 12 - 14 March 2008	oral	Done
423.	Advanced simulation of statistical variability and reliability in nano CMOS transistors	A. Asenov, S. Roy, A. R. Brown, G. Roy, C. Alexander, C. Riddet, C. Millar, B. Cheng, A. Martinez, N. Seoane, D. Reid, M. F. Bukhori, X. Wang, U. Kovac	GU	IEDM	15 Dec San Francisco	Invited	Done
424.	Fabrication and characterisation of strained Si heterojunction bipolar transistors on virtual substrates	S. Persson, M. Fjer, E. Escobedo-Cousin, G. Malm, Y.-B. Wang, P.-E. Hellström, M. Östling, E. Parker, S.H. Olsen and A.G. O'Neill	UNEW, KTH, Warwick	IEDM	Dec 08, San Francisco		Done
425.	Piezomobility Description of Strain-Induced Mobility	A. O'Neill, Y. L. Tsang, B. J. Gallacher, S.H. Olsen	UNEW	ICSICT	Oct 08, Beijing	Invited paper	Done
426.	Strain engineering for high mobility channels	S Olsen, ZA Tarawneh, J Varzgar, E Escobedo-Cousin, R Agaiby, P Dobrosz, A O'Neill, P-E Hellström, M Östling, E Parker, R Loo and C Claeys	UNEW, KTH, Warwick, IMEC	ICST	March 08, Shanghai	Invited paper	Done
427.	Nanoscale strain characterisation for ultimate CMOS and post-CMOS devices	SH Olsen, P Dobrosz, RMB Agaiby, YL Tsang, O Alatise, SJ Bull, AG O'Neill, KE Moselund, AM Ionescu, P Majhi, D Buca, S Mantl and H Coulson	UNEW, EPFL, FZJ	EMRS	May 08, Strasbourg	Invited paper	Done
428.	Gate leakage in high mobility substrates: correlating macroscopic leakage with nanoscale measurements	SH Olsen et al	UNEW, IMEC	MRS Spring Meeting	April 09, San Francisco	Invited paper	Done
429.	Nanoscale strain characterisation in patterned SSOI structures	P Dobrosz, SH Olsen, SJ Bull, YL Tsang, RMB Agaiby, AG O'Neill, D Buca, S Mantl, B Ghyselen	UNEW, FZJ,	EMRS	May 08, Strasbourg		Done
430.	Nanometer scale strain profiling through Si/SiGe heterolayers	RMB Agaiby, SH Olsen, P Dobrosz, H Coulson, SJ Bull and AG O'Neill	UNEW	EMC	June 08, Santa Barbara		Done
431.	Improved analog performance of strained Si n-MOSFETs on thin SiGe strain relaxed buffers	O Alatise, KSK Kwa, S Olsen and A O'Neill	UNEW	ESSDERC	Sept 08, Edinburgh		Done
432.	Investigation of strain profile optimization in gate-all-around suspended silicon nanowire FET	M Najmzadeh, K Moselund, A Ionescu, P Dobrosz, S Olsen and A O'Neill	EPFL, UNEW	ESSDERC	Sept 08, Edinburgh		Done
433.	Top down and Bottom-up routes to nanoscale electronic components	A Houlton, BR Horrocks, NG Wright, S Olsen and A O'Neill	UNEW	Intel European Research and Innovation Conference	Sept 08, Dublin	Invited paper	Done
434.	Source-drain Engineering for Channel-limited PMOS Device Performance: Advances in Understanding of Amor-phization-Based Implant Techniques	NEB Cowern	UNEW	MRS Spring Meeting	April 08, San Francisco	Invited paper	Done
435.	Schottky source-drain contacts	E. Dubois	IEMN-ISEN	MIGAS'08	International Summer School on Advanced Microelectronics, 28.06 – 4.07. 2008	Invited	Done

Section B
Part B1

TEMPLATE B1: LIST OF APPLICATIONS FOR PATENTS, TRADEMARKS, REGISTERED DESIGNS, ETC.					
Type of IP Rights[7]:	Confidential Click on YES/NO	Foreseen embargo date dd/mm/yyyy	Application reference(s) (e.g. EP123456)	Subject or title of application	Applicant (s) (as on the application)
Patent	*NO*		*N° EN 07 08351*	*Elaboration process of horizontal nanowires*	*FMNT/CNRS, CEA*
Patent	*NO*		*N° 08 02573*	*Preparation process for nanowires elaboration*	*FMNT/CNRS, CEA*
Patent	*NO*		*PCT/EP2009/050031*	*Double gate memory device*	*FMNT/CNRS, UCL*
Patent	*NO*		*N° 09/52452*	*Single-transistor RAM cell*	*FMNT/GRENOBLE INP, UGR*
French Patents and international extensions	*YES*		FR2930073 (A1) published 2009-10-16 WO2009136095 (A2) 2009-11-12 WO2009136095 (A3) 2009-12-30 FR2930073 (B1) 2010-09-03 EP2279520 (A2) 2011-02-02	*Method for making complementary p and n MOSFET transistors, electronic device including such transistors, and processor including at least one such device*	*G. Larrieu, E. Dubois*

[7] A drop down list allows choosing the type of IP rights: Patents, Trademarks, Registered designs, Utility models, Others.

Part B2

Type of Exploitable Foreground[8]	**Description of exploitable foreground**	Confidential Click on YES/NO	Foreseen embargo date dd/mm/yyyy	**Exploitable product(s) or measure(s)**	**Sector(s) of application**[9]	**Timetable, commercial or any other use**	**Patents or other IPR exploitation (licences)**	**Owner & Other Beneficiary(s) involved**
Commercial Exploitation of R&D results	Electronic Semiconductor Characterization Tool (a)	YES		Application Software	1. Nano-Electronics. 2. DC to RF characterization 3. RF Noise 4. Non-linear Applications	2011 – 2013	Declaration of Invention at Universite catholique de Louvain	UCL: EMAM M. RODA NEVE C. RASKIN J.-P VANHOENACKER-JANVIER D.
General advancement of knowledge	Ge Quantum Dot Rectenna (b)	NO		mm wave detector	1. mm wave detection 2. Automotive safety systems 3. Energy harvesting			USTUTT
General advancement of knowledge	QD Esaki diodes (c)	NO		NDR Diodes	1. RF oscillators 2. Memories			USTUTT
General advancement of knowledge	Local strained silicon platform (d)	NO		Local strained silicon platform fabrication	1. High mobility MOSFETs 2. Low power electronics			USTUTT

Explanation of the Exploitable Foreground:

(a) The Electronic Semiconductor Characterization (ESC) tool is intended to provide a unique environment for a complete characterization flow for semiconductor devices (active or passive). The characterization flow includes dc and high frequency characterization modules based on small-signal equivalent circuits and direct extraction methods. It also includes non-linear behavior study as well as RF noise characterization based on different RF noise models and extraction routines. In a first step, this tool is targeting academic research centers. In a next step, industrial facilities should be considered as potential clients for the tool. The project is planned to reach its maturity in approximately four years. A declaration of invention at the Université catholique de Louvain (UCL) has been filed. Based on further advancement of the project, one or

[19] A drop down list allows choosing the type of foreground: General advancement of knowledge, Commercial exploitation of R&D results, Exploitation of R&D results via standards, exploitation of results through EU policies, exploitation of results through (social) innovation.

[9] A drop down list allows choosing the type sector (NACE nomenclature) : http://ec.europa.eu/competition/mergers/cases/index/nace_all.html

more patents could be considered. The final product of this tool should include a wide variety of devices (active and passive) along with a quasi-complete library of models and extraction methods. Hence, a continuous research effort is needed along with the development of the tool. The tool in itself is a mean to develop new methodologies for characterizing devices, hence a closed loop research cycle could be established. A market research is currently effective, however, one client has already acquired a license of the tool (an academic research center in Germany) whereas two other research centers in Europe are showing their interest and might acquire a license in the near future as well. The preliminary market study conducted in order to receive the funding from the Walloon Region indicated a promising potential for this tool based on the absence of strong competition at the actual time.

(b) Ge Quantum Dot Rectenna was developed at Stuttgart University (USTUTT, E. Kasper, A. Karmous, H. Xu). Its purpose is the detection of microwave radiation especially at mm-wave frequencies (30 GHz – 300 GHz). The high frequency radiation is converted into a direct current (DC) signal. This property may be implemented for energy harvesting to power wireless devices. It can be exploited by sensor manufacturers for battery-free remote sensors. It can also be employed by car manufacturing companies as a mm-wave detector in automotive safety systems for monitoring the surrounding of a vehicle. In order to meet each application requirements, further research efforts are necessary. For more specific applications, IPR exploitation is expected. The impact will depend on the additional research intensity. Internal (Stuttgart) activities will focus on patent survey for medical sensor applications.

(c) QD Esaki diodes with room temperature negative differential resistance (NDR) have been demonstrated at Stuttgart University (USTUTT, E. Kasper, A. Karmous, M. Oehme). NDR I-V curve allows device applications in high frequency and multi-value storage. In high frequency, it can be implemented in RF oscillator circuit intended for RF power generation systems which can be used by car manufacturing companies in automotive safety systems. High frequency performance of an Esaki diode is limited by its high capacitance which is due to its very thin barrier width required for carrier tunneling. The inclusion of Ge dots layer(s) in the barrier region allows the diode capacitance decrease and therefore performance improvement. Another potential application is their use in SRAM memories by chip manufacturers. The use of two low power tunneling diodes in addition to one transistor instead of six transistor CMOS SRAM would allow the improvement of the power consumption and the increase of the integration density. Moreover, multivalued cells at no area penalty can be obtained by vertical stacking of several tunneling diodes. Further research efforts are necessary in order to optimize the diode structure and electrical characteristics. The impact will depend on the additional research intensity. First suggestions aim to an inclusion into a national (German) project cluster(Forschergruppe).

(d) Local strained silicon (s-Si) platform was fabricated at Stuttgart University (USTUTT, E. Kasper, A. Karmous, M. Oehme). Its objective is to create s-Si layer on predefined areas on a Si/SOI wafer surface. Improved transistor performances can be obtained when s-Si is used as a channel material instead of bulk Si. However, different strain types and magnitudes are required for p-channels and n-channels in CMOS circuits. They can be obtained employing repeatedly the developed local strained silicon platform fabrication process. Local strained silicon platform can be implemented by microelectronic device manufacturer for high mobility MOSFETs and low power electronics. For low power electronic applications, further research efforts are necessary in order to extend the process used for bulk Si wafer to SOI by combining the developed bulk procedure with a SOI manufacturing. The impact will depend on the additional research intensity. Potential manufacturing routes will be elaborated and published in order to attract industrial interest.

4.3 Report on societal implications

A General Information *(completed automatically when **Grant Agreement number** is entered.*	
Grant Agreement Number:	216171
Title of Project:	NANOSIL
Name and Title of Coordinator:	DR Francis BALESTRA, project coordinator

B Ethics	
1. Did your project undergo an Ethics Review (and/or Screening)? • If Yes: have you described the progress of compliance with the relevant Ethics Review/Screening Requirements in the frame of the periodic/final project reports? Special Reminder: the progress of compliance with the Ethics Review/Screening Requirements should be described in the Period/Final Project Reports under the Section 3.2.2 *'Work Progress and Achievements'*	***No***
2. Please indicate whether your project involved any of the following issues (tick box) :	
RESEARCH ON HUMANS	
• Did the project involve children?	***No***
• Did the project involve patients?	***No***
• Did the project involve persons not able to give consent?	***No***
• Did the project involve adult healthy volunteers?	***No***
• Did the project involve Human genetic material?	***No***
• Did the project involve Human biological samples?	***No***
• Did the project involve Human data collection?	***No***
RESEARCH ON HUMAN EMBRYO/FOETUS	
• Did the project involve Human Embryos?	***No***
• Did the project involve Human Foetal Tissue / Cells?	***No***
• Did the project involve Human Embryonic Stem Cells (hESCs)?	***No***
• Did the project on human Embryonic Stem Cells involve cells in culture?	***No***
• Did the project on human Embryonic Stem Cells involve the derivation of cells from Embryos?	***No***
PRIVACY	
• Did the project involve processing of genetic information or personal data (eg. health, sexual lifestyle, ethnicity, political opinion, religious or philosophical conviction)?	***No***
• Did the project involve tracking the location or observation of people?	***No***
RESEARCH ON ANIMALS	
• Did the project involve research on animals?	***No***
• Were those animals transgenic small laboratory animals?	***No***
• Were those animals transgenic farm animals?	***No***
• Were those animals cloned farm animals?	***No***
• Were those animals non-human primates?	***No***
RESEARCH INVOLVING DEVELOPING COUNTRIES	
• Did the project involve the use of local resources (genetic, animal, plant etc)?	***No***
• Was the project of benefit to local community (capacity building, access to healthcare, education etc)?	***No***
DUAL USE	
• Research having direct military use	***No***
• Research having the potential for terrorist abuse	***No***

C Workforce Statistics

3. Workforce statistics for the project: Please indicate in the table below the number of people who worked on the project (on a headcount basis).

Type of Position	Number of Women	Number of Men
Scientific Coordinator		**1**
Work package leaders	**1**	**5**
Experienced researchers (i.e. PhD holders)	**13**	**75**
PhD Students	**14**	**53**
Other	**6**	**12**

4. How many additional researchers (in companies and universities) were recruited specifically for this project?	
Of which, indicate the number of men:	**11**

D Gender Aspects

5. Did you carry out specific Gender Equality Actions under the project?

○ Yes
● No

6. Which of the following actions did you carry out and how effective were they?

	Not at all effective				Very effective
❑ Design and implement an equal opportunity policy	○	○	○	○	○
❑ Set targets to achieve a gender balance in the workforce	○	○	○	○	○
❑ Organise conferences and workshops on gender	○	○	○	○	○
❑ Actions to improve work-life balance	○	○	○	○	○

○ Other:

7. Was there a gender dimension associated with the research content – i.e. wherever people were the focus of the research as, for example, consumers, users, patients or in trials, was the issue of gender considered and addressed?

○ Yes- please specify

● No

E Synergies with Science Education

8. Did your project involve working with students and/or school pupils (e.g. open days, participation in science festivals and events, prizes/competitions or joint projects)?

● Yes- please specify

Nanosil contributed to generate a French national project ANR Nano-Ecole with the objective of presenting advancements in nanoscience and nanotechnoloy to school pupils and to generate discussions on the societal aspects of nanoscience (UPS)

Other synergies with science education included:

- Yearly Girls Day (AMO GmbH)
- Organisation of the ULIS 2009 conference (FZJ)
- Best student award ULIS 2010 (FZJ)
- Organisation and contribution to MIGAS International Summer School (GRENOBLE INP)
- Student research within the course of microelectronics and optoelectronics (USTUTT)
- Final Year Project students (LIVUNI)

○ No

9. Did the project generate any science education material (e.g. kits, websites, explanatory booklets, DVDs)?

● Yes- please specify

The project generated Final Year Project posters at LIVUNI and the *Nanoscale CMOS: Innovative Materials, Modeling and Characterization* book edited by Francis Balestra (Grenoble INP).

○ No

F Interdisciplinarity

10. Which disciplines (see list below) are involved in your project?

- ● Main discipline[10]: 2.2
- ● Associated discipline[10]: 2.3
- ○ Associated discipline[10]:

G Engaging with Civil society and policy makers

11a Did your project engage with societal actors beyond the research community? *(if 'No', go to Question 14)*	●	Yes

11b If yes, did you engage with citizens (citizens' panels / juries) or organised civil society (NGOs, patients' groups etc.)?

- ○ No
- ○ Yes- in determining what research should be performed
- ○ Yes - in implementing the research
- ● Yes, in communicating /disseminating / using the results of the project

11c In doing so, did your project involve actors whose role is mainly to organise the dialogue with citizens and organised civil society (e.g. professional mediator; communication company, science museums)?	○ ●	Yes No

12. Did you engage with government / public bodies or policy makers (including international organisations)

- ○ No
- ● Yes- in framing the research agenda
- ○ Yes - in implementing the research agenda
- ● Yes, in communicating /disseminating / using the results of the project

13a Will the project generate outputs (expertise or scientific advice) which could be used by policy makers?

- ○ Yes – as a **primary** objective (please indicate areas below- multiple answers possible)
- ● Yes – as a **secondary** objective (please indicate areas below - multiple answer possible)
- ○ No

13b If Yes, in which fields?

Agriculture		Energy		Human rights	
Audiovisual and Media		Enlargement		● Information Society	
Budget		Enterprise		Institutional affairs	
Competition		Environment		Internal Market	
Consumers		External Relations		Justice, freedom and security	
Culture		External Trade		Public Health	
Customs		Fisheries and Maritime Affairs		● Regional Policy	
Development Economic and Monetary Affairs		Food Safety		● Research and Innovation	
Education, Training, Youth		Foreign and Security Policy		● Space	
Employment and Social Affairs		Fraud		Taxation	
		Humanitarian aid		Transport	

[10] Insert number from list below (Frascati Manual).

13c If Yes, at which level?

- ● Local / regional levels
- ● National level
- ● European level
- ○ International level

H Use and dissemination

14. How many Articles were published/accepted for publication in peer-reviewed journals?	**230**
To how many of these is open access[11] provided?	**1**
How many of these are published in open access journals?	**1**
How many of these are published in open repositories?	**1**
To how many of these is open access not provided?	**229**
Please check all applicable reasons for not providing open access:	
❑ publisher's licensing agreement would not permit publishing in a repository ❑ no suitable repository available ❑ no suitable open access journal available ❑ no funds available to publish in an open access journal ● lack of time and resources ● lack of information on open access ❑ other[12]: ……	

15. How many new patent applications ('priority filings') have been made? *("Technologically unique": multiple applications for the same invention in different jurisdictions should be counted as just one application of grant).*		**5**
16. Indicate how many of the following Intellectual Property Rights were applied for (give number in each box).	Trademark	**0**
	Registered design	**0**
	Other	**0**
17. How many spin-off companies were created / are planned as a direct result of the project?		**0**
Indicate the approximate number of additional jobs in these companies:		

18. Please indicate whether your project has a potential impact on employment, in comparison with the situation before your project:

❑ Increase in employment, or	❑ In small & medium-sized enterprises
❑ Safeguard employment, or	❑ In large companies
❑ Decrease in employment,	❑ None of the above / not relevant to the project
● Difficult to estimate / not possible to quantify	

19. For your project partnership please estimate the employment effect resulting directly from your participation in Full Time Equivalent (FTE = one person working fulltime for a year) jobs:	**23**

[11] Open Access is defined as free of charge access for anyone via Internet.
[12] For instance: classification for security project.

I Media and Communication to the general public

20. As part of the project, were any of the beneficiaries professionals in communication or media relations?

○ Yes ● No

21. As part of the project, have any beneficiaries received professional media / communication training / advice to improve communication with the general public?

○ Yes ● No

22 Which of the following have been used to communicate information about your project to the general public, or have resulted from your project?

●	Press Release	●	Coverage in specialist press
❑	Media briefing	❑	Coverage in general (non-specialist) press
❑	TV coverage / report	❑	Coverage in national press
❑	Radio coverage / report	❑	Coverage in international press
●	Brochures /posters / flyers	●	Website for the general public / internet
●	DVD /Film /Multimedia	●	Event targeting general public (festival, conference, exhibition, science café)

23 In which languages are the information products for the general public produced?

●	Language of the coordinator	●	English
❑	Other language(s)		