Laboratoire d'électronique et de technologie de l'information
Direction de la recherche technologique
Département NaNoTec

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TECHNICAL REPORT

Deliverable 2.2: SQWIRE – Silicon Quantum Wire Transistors Fabrication Process Specification for *junctionless* MOSFET

Projet / Project: SQWIRE N/Réf : D2NT/10.615/SB

	Nom / Fonction – Name / Function	*Date*	*Visa*
Auteur(s) : Author(s)	*Sylvain Barraud* *Tél : 04-38-78-98-45*	*November 23th, 2010*	
Approbateur : Assentor	*Olivier Faynot*	*November 23th, 2010*	

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Abstract

Nanowire (NW) and Tri-gated Complementary Metal Oxide Semiconductor (CMOS) technology appear as an attractive option to overcome standard CMOS bulk technology limits in terms of scaling, performances and power consumption [1-3]. The electrostatic control over the channel is indeed improved in NWs, leading to a significant reduction of short channel effects [4] and thus leakage currents in the OFF state.

Based on existing expertise in fabrication of FD-SOI nanowire devices, we will develop a fabrication route for n-channel and p-channel *junctionless* nanowire MOSFET transistor. Existing mask set will be used, with the exception of the active area level which will have to be redrawn. The FD-SOI route will be adapted in order to target *junctionless* NW with width varying from $10nm \leq W \leq 20nm$, silicon thickness T_{SOI}=10nm and with a gate length $L_G < 30nm$.

Those original devices have demonstrated near-ideal subthreshold slope, extremely low leakage current and less degradation of mobility with gate voltage and temperature than conventional transistors [5].

SQWIRE

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I. INTRODUCTION

The silicon nanowire field-effect transistor is one of the promising candidates for future ultra-scaled CMOS technology. It offers the best gate electrostatic control on short-channel-effects. The formation of ultra-shallow junctions is a limiting factor to scale and puts severe constraints on the processing thermal budget. Ultra-short-time annealing techniques are being employed to eliminate thermal diffusion of the source and drain doping impurities, but even the lateral impurity spread due to ion implantation itself is starting to cause problems. In addition to the difficulty of forming ultra-sharp junctions, random impurity fluctuations from source and drain dopants scattered in the channel region cause variability problems.

Here, a new type of transistor is investigated in which there are no junctions and no doping concentration gradients. These devices have full CMOS functionality and are made using Tri-gated silicon nanowires. Those original devices have demonstrated near-ideal subthreshold slope, extremely low leakage current and less degradation of mobility with gate voltage and temperature than conventional transistors [5].

The objective of this task (D2.2) is to propose an integration scheme and fabrication process specifications for *junctionless* Tri-gated MOSFET transistors on 300 mm wafers based on an adapted route from FD-SOI MOSFET devices developed at CEA-Leti.
First of all, the integration strategy used for the elaboration of *junctionless* tri-gated nanowire transistor is presented.

II. JUNCTIONLESS TRANSISTORS

The main difference between conventional and junctionless MOSFET transistors is that the channel doping is similar to the source-drain doping.

II.1. NANOWIRE ELABORATION ON 300 MM WAFERS FROM DUV193NM LITHOGRAPHY

Silicon-on-Insulator (SOI) structures with silicon layers of 12 nm in thickness are used. The key for the fabrication of junctionless gated resistor is the formation of a semiconductor layer that is

CEA, LETI, MINATEC Campus
Centre de Grenoble – 17 rue des Martyrs – 38054 Grenoble CEDEX 9
Tel : 33 – 04 38 78 10 34 – Fax : 33 – 04 38 78 06 24 – veronique.bourdon@cea.fr
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thin and narrow enough to allow full depletion of carriers when the device is turned off [7]. Then, **the silicon layer will be thinned down to 10nm**. The semiconductor also needs to be heavily doped to allow for a reasonable amount of current flow when the device is turned on. The implant energies and doses will be chosen (from process simulation – Athena Silvaco) to yield uniform **doping concentration ranging from $5x10^{18}$ cm^{-3} up to $5x10^{19}$ cm^{-3}**. Then, the silicon layer will be patterned to create the silicon nanowires by a mesa isolation technique. The active stack used in this work will be consisted of a 10nm doped Si, 2.5nm SiO_2 dielectric layer and an organic bottom anti-reflective coating (BARC) layer of around 24nm patterned using 193nm ArF resist. The thickness of the photoresist is around 160nm. The active zone (i.e. nanowire feature) will be carried out using the trimmed resist/BARC as a mask. Obviously, the final linewidth of nanowires will be determined mainly by the amount of trimmed resist.

The good electrostatic control being based on low dimensions of nanowire width (or diameter), shorter wavelengths are required for lithography. As a result, an alternative method to *e-beam* lithography is proposed in this study to achieve sub-15nm nanowire width in order to lower the manufacturing cost and shorten the development time.

Today's most advanced lithography uses 193nm wave-length for the production of integrated circuits devices. Following the same philosophy than for the gate patterning, we proposed to develop an approach based on resist trimming by dry plasma etching to elaborate our silicon nanowires. This approach has the advantage of reducing the dimensions without increasing the complexity of the lithography requirements. A schematic of the process flow of this trimming method is summarized in Fig. 1. First of all, HBr plasma curing process was performed in order to harden the 193nm ArF resist for better etching resistance. Then, the BARC opening is done using CF_4 chemistry. This chemistry will be used in order to ensure vertical resist/BARC profile and correct linewidth roughness [6]. Moreover, this sequence consuming a lot of photoresist, the thin thickness of the BARC layer is well suited to minimize the resist budget during the process. Then, the BARC/resist trimming process is performed just before the main etch to selectively pattern the silicon on the buried oxide. Trimming resist is performed to achieve nanowire

structures as small as **15nm in width** using the HBr/O_2 plasma. In order to smooth the resist patterns and then reduce the linewidth roughness, a curing step will be performed just before the trimming.

The investigated structures after the photolithography are shown in Fig. 2. They comprised isolated lines (NW) and arrays of lines with long and short dimensions. The arrays of lines with long dimensions will be used to extract the capacitance and the carrier mobility.
All the critical dimension (CD) measurements (after photolithography and after active patterning) will be done using in-line field-emission-scanning electron microscope (SEM).
The linewidth before etching –referred to as developed inspection critical dimension- is around 80nm. After etching, the reduction of the silicon nanowire width induces by the trimming is targeted to 65 nm in order to have nanowire width of around 15nm. Due to the dispersions induce by the photolithography, the NW width after etching is expected to vary between 10nm and 20nm.

I.2. GATE STACK DEPOSITION AND CHANNEL LENGTH

For the first run, the gate stack used will be composed of high-κ/metal gate. 2.3nm chemical vapour deposition (CVD) HfSiON with 5nm CVD TiN and Poly-Silicon (50nm) layers will be deposited. This corresponds to an equivalent oxide thickness (**EOT) of around 1.1nm**.

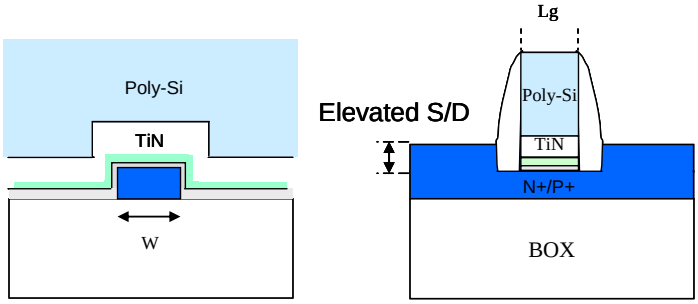
A HRTEM picture of the nanowire cross-section will be performed in order to reveal the good conformal gate stack deposition surrounding the nanowire and to evaluate the nanowire width. Fig. 3 shows a cross-sectional TEM micrograph of a conventional triple-gate silicon nanowire with high-k/metal gate stack (isolated devices).

As for the active patterning, 193nm lithography tool will be used with a resist trimming in order to address **gate lengths down to 25nm**. Firt results obtained on regular Tri-gated nanowire are shown in Fig. 4. Afterwards, a nitride spacer thickness of around 20nm will be formed on the

silicon source-drain. Then, low parasitic resistance will be realized by **epitaxial doped silicon growth on the source-drain (ΔT_{SI}=18nm)**. A schematic process flow is presented in Fig. 5.

For the second run, additional gate stack composed of SiO_2 (2-3nm)/Poly-Si will be processed to compare with high-κ/metal gate stack.

Finally, the main process specifications for the fabrication of junctionless MOSFET are the following:



Width W:	10nm ≤ W ≤ 20nm
Gate length L_g:	20nm ≤ L_g ≤ 10µm
Doping N^+/P^+:	$5\times10^{18}cm^{-3} \leq N \leq 5\times10^{19}cm^{-3}$
Silicon thickness	T_{SOI}=10nm
Gate stack:	0.8nm SiO_2 / 2.3nm HfSiON / 5nm TiN / 50nm Poly-Si
CD spacer:	20nm
Elevated source/drain:	18nm

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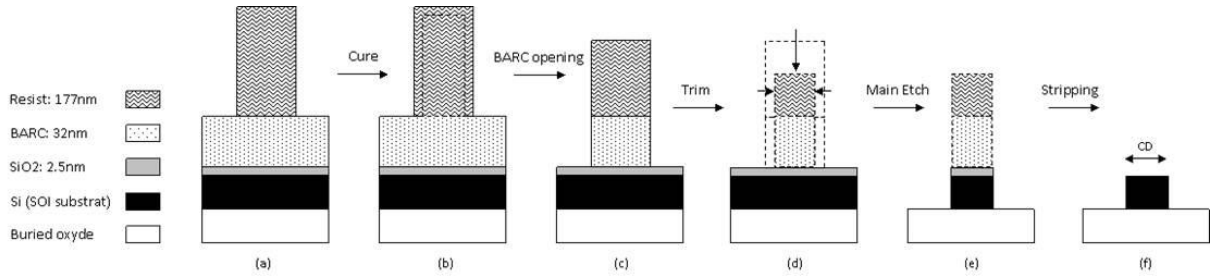

Figure 1: Schematic of the process flow for patterning the silicon nanowire

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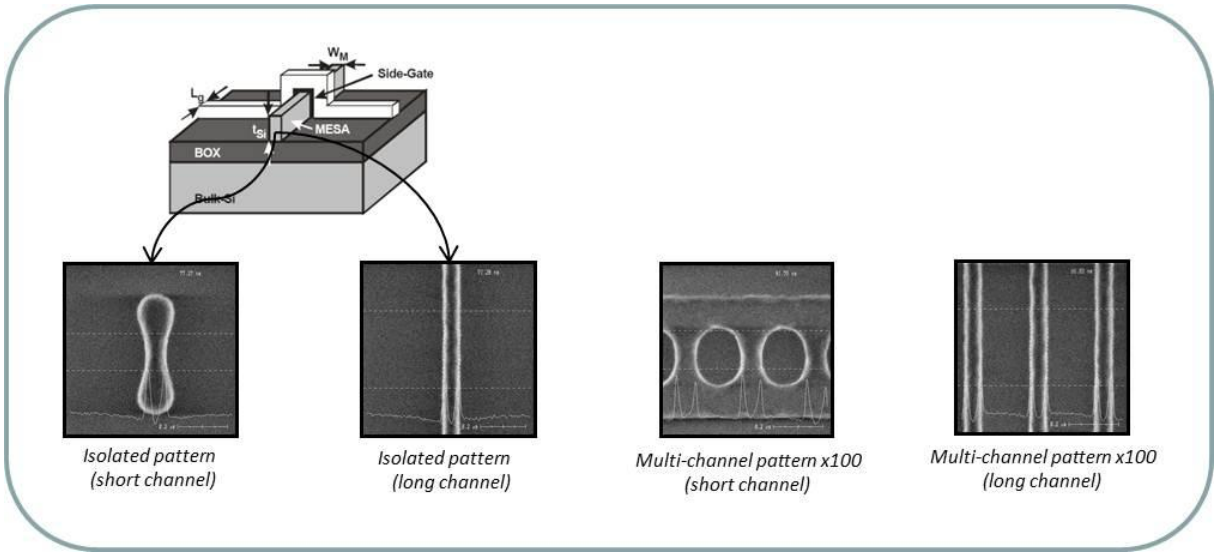

Figure 2: SEM pictures of the devices observed on various chips of the 300mm wafers after the photo-lithography. Long and short isolated devices with long and short arrays of devices (x100 fingers)

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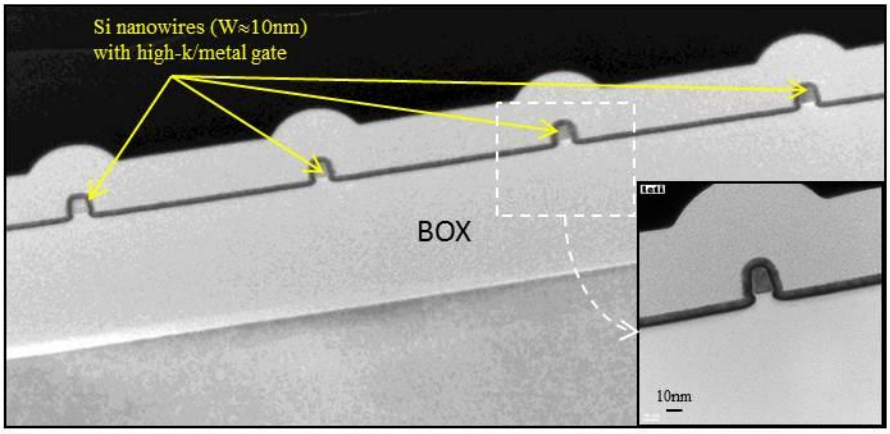

Cross-sectional TEM micrograph of triple-gate silicon nanowire with high-k/metal gate stack

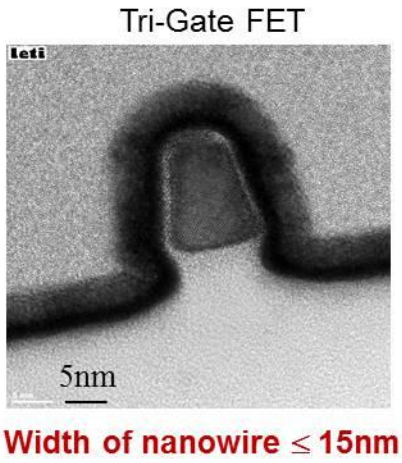

Figure 3: Cross-sectional TEM micrograph of a conventional triple-gate silicon nanowire with high-κ/metal gate stack

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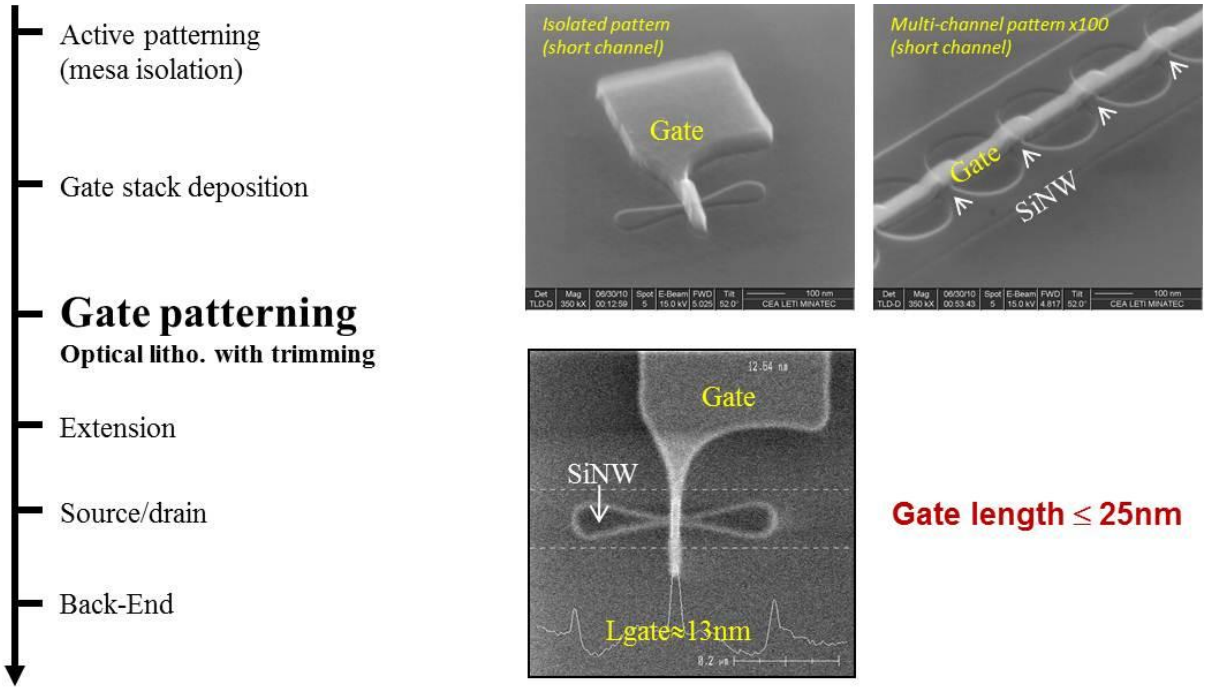

Figure 4: SEM picture of the gate after etching and trimming on regular Tri-gated nanowire transistors. Gate lengths below 25nm are obtained.

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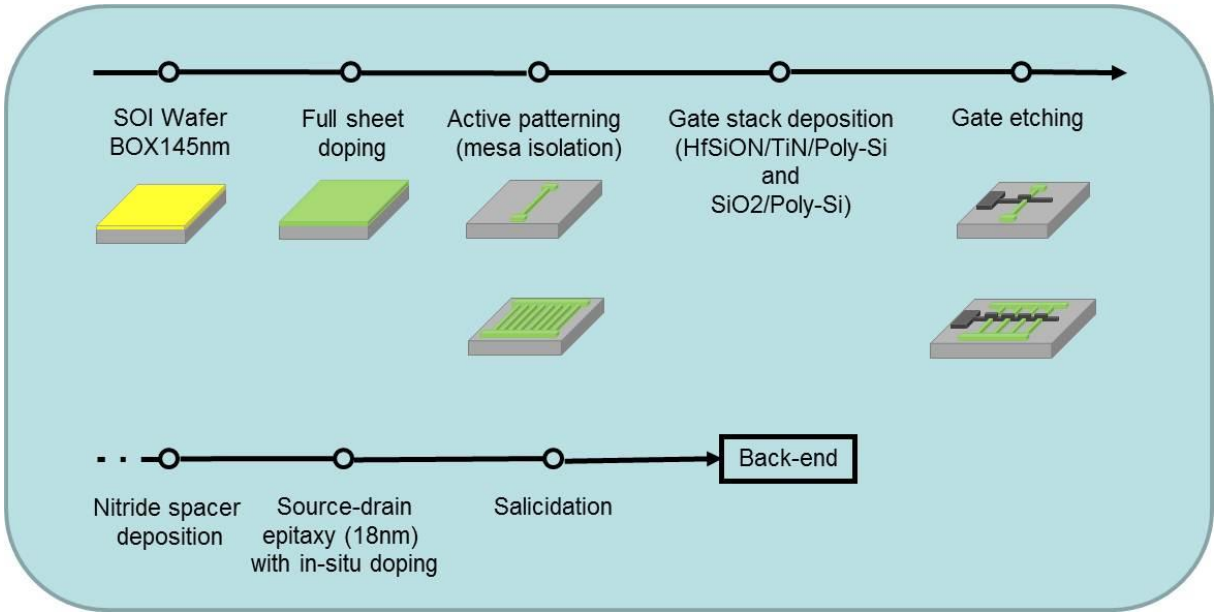

Figure 5: Process Flow chart for the fabrication of *junctionless* nanowire MOSFET devices