Gant Agreement N° 257111

SQWIRE

Silicon Quantum Wire Transistors

Start date of project:	3rd September 2010
Duration:	36 Months

Coordination Action
Information and Communication Technologies

Deliverable D3.2	
Nanometrology protocol for Gated Resistors	
Due date of deliverable:	November 30, 2011
Actual submission date:	November, 30 2011
Organisation name of lead contractor for this deliverable:	**CEA-LETI-Minatec**

Revision [ ]

Approval

WP Leader ☒	**SP Leader** ☐	**Coordinator** ☐

Partner	**Please, give a short description (1-3 sentences) of partners contribution to this deliverable**
INTEL	Contribution for TEM cross sections on prototyped gated resistors
SOITEC	SOITEC continue to develop UV/optical and AFM film thickness and roughness measurement on house. After the development of the corresponding techniques and protocols at CEA-LETI and IPLS a benchmarking will be performed.

Project co-funded by the European Commission within the Seventh Framework Programme (2007-2012)		
Dissemination Level		
PU	Public	**x**
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission	
CO	Confidential, only for members of the consortium (including the Commission Services)	

Table of contents:

1. Introduction

The nanoscale MOSFET devices fabricated within the SQWIRE project require advanced physical and electrical characterization. Then, a specific task for nanometrology is needed in order to clearly know the size of the nanowire *junctionless* transistors (JLT). The concept of nanometrology defined in this work is mainly based on the following techniques:

- Ellipsometry for the silicon thickness measurement
- SEM (Scanning Electron Microscopy) for the nanowire width and gate length measurement, etc.
- TEM (Transmission Electron Microscopy) for the nanowire width and gate length measurement, etc.

Its importance is highlighted through the necessity to measure key elements with dimensions in the range 1 to about 100 nm (with precision reaching 0.1 nm nowadays) and to correlate the measured sizes with electrical properties of JLT transistors. Here we are interested to have precise measurement of sizes in the nanometre range from the characterization techniques previously cited. This report provides a comprehensive review of the different samples characterized during the process as well as critical dimensions such as width, thickness and length.

2. Junctionless Nanowire Transistor

2.1. Process description

[110]-Tri-gate junctionless NWFETs (NMOS and PMOS) with high-k/metal gate stack were fabricated on (100) SOI wafers with BOX thickness of 145nm following the process shown in Fig. 2.1.1. The silicon film thickness is around 10nm. The channel implant for junctionless behaviour was performed on non-patterned wafers with Boron for P-MOSFETs and Phosphorus for N-MOSFETs. The targeted channel concentrations were $10^{19}cm^{-3}$, $2\times10^{19}cm^{-3}$ and $4-5\times10^{19}cm^{-3}$ for both N- and P-MOSFETs. The silicon layer is patterned to create the nanowires by using a mesa isolation technique. NW pattern is defined by optical (DUV) lithography and followed by a resist trimming process. It is performed to achieve nanowire structures as small as 10nm in width using HBr/O_2 plasma. The gate stack consists in 2.3nm CVD HfSiON, 5nm ALD

TiN and Poly-Silicon (50nm) layers (EOT≈1.2nm). The gate is wrapped around the channel in a Tri-gate configuration. As for the active patterning, the same photo-resist trimming is used to address gate lengths down to 20nm. Afterwards, a nitride spacer thickness of around 15nm is formed on the silicon source-drain (S/D). Then, low access resistances are realized by epitaxial silicon growth on S/D (ΔT_{Si}=18nm).

The objective of the next section is to show the measurement results of gate length, nanowire width and thicknesses of different junctionless devices which will be electrically characterized during the project.

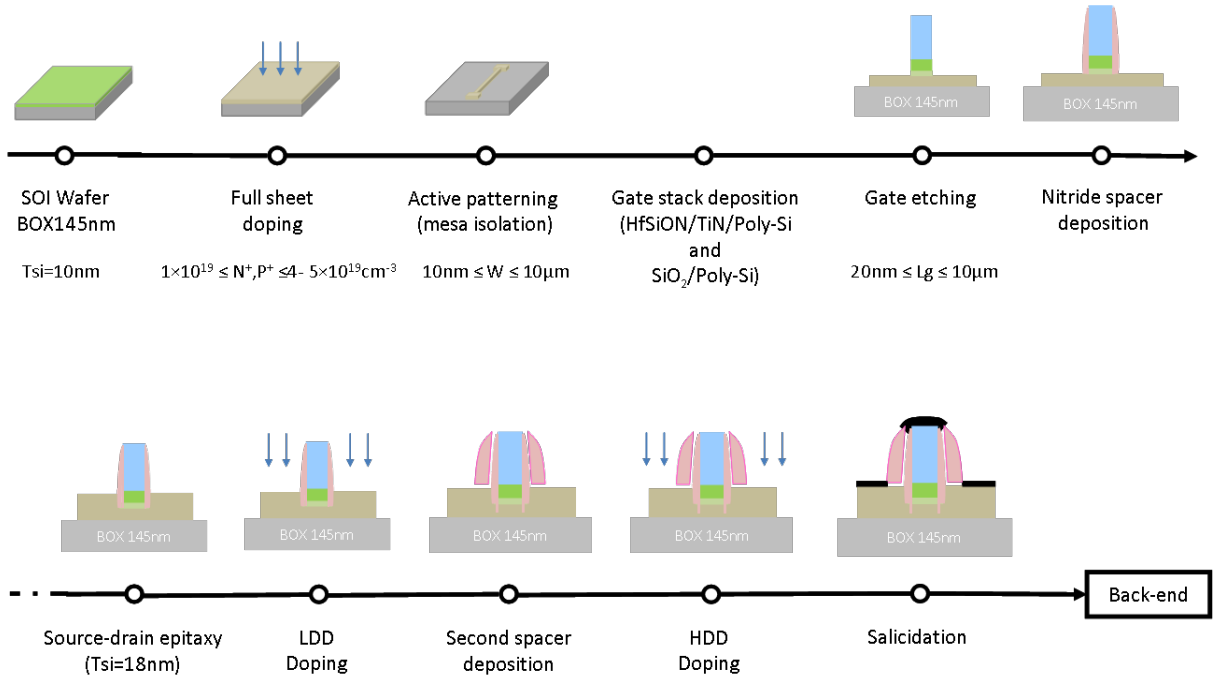


Figure 2.1.1: Simplified process flow for the fabrication of JLT transistors

2.2. Metrology and characterization

2.2.1. Ellipsometry

Ellipsometry is an optical technique, which enables measurements of thickness and optical properties of thin films. During the fabrication process of JLT transistors, it can be commonly used to evaluate thickness of silicon dioxide, silicon, photoresist, etc. An idea of ellipsometry is based on reflection polarised light from the sample under study. It can be shown that polarised light changes its polarisation state upon reflection and that this change is determined by thickness and optical properties of the measured film. After the measurement, calculations of the thickness should be performed.

During the process, ellipsometric thickness measurements are used at different steps to verify the deposited thicknesses or after etching process to verify its selectivity to other material.

In order to know the thickness of the doped channel, we have extracted on the SOI wafers the silicon thickness before the gate stack deposition.

The results are summarized in the table 1 (see below. Unity is in Angstrom). The measurement is performed using 25 points.

Wafer01	**Mean (A)**	**Min (A)**	**Max (A)**
BOX	1458	1457	1459
silicon	89.6	84.1	94.8
Wafer02			
BOX	1460	1459	1461
silicon	90.2	84.2	92.9
Wafer03			
BOX	1462	1461	1463
silicon	89.4	84.0	92.1
Wafer04			
BOX	1464	1463	1466
silicon	85.9	79.7	88.6
Wafer05			
BOX	1464.5	1463.9	1465.4
silicon	85.1	78.5	88.2
Wafer06			
BOX	1468	1465.7	1469
silicon	87.8	85.4	89.7
Wafer07			
BOX	1467.8	1465.2	1469.9
silicon	92.3	89.8	94.0
Wafer08			
BOX	1459	1457	1460.9
silicon	97.6	91.1	100.3
Wafer09			
BOX	1459.6	1458	1460.5

silicon	95.1	90.3	98.5
Wafer10			
BOX	1459.3	1457.7	1460.8
silicon	96.2	91.3	100.9
Wafer11			
BOX	1459.8	1458.6	1460.8
silicon	96.5	92.8	102
Wafer12			
BOX	1459.2	1457.5	1461.4
silicon	98.8	93.4	102.8

Table 1: Si channel and buried oxide thicknesses

Low access resistances being realized by epitaxial silicon growth on Source/Drain (target: ΔT_{Si}=18nm) the thickness measurement of raised S/D has been performed on all the wafers using the same technique. The result is given below.

Wafer 1	16.8nm	**Wafer 5**	17.1nm	**Wafer 9**	16.7nm
Wafer 2	16.7nm	**Wafer 6**	17.2nm	**Wafer 10**	16.5nm
Wafer 3	17.9nm	**Wafer 7**	16.8nm	**Wafer 11**	16.6nm
Wafer 4	16.8nm	**Wafer 8**	16.4nm	**Wafer 12**	16.6nm

The channel thickness of nanowire JLT transistors being known, we have to measure the width and gate length of the devices.

2.2.2. Scanning Electron microscopy (SEM)

Scanning Electron Microscopy (SEM) uses a focused electron beam across to scan the surface of a sample, providing high-resolution and long-depth-of-field images of the sample surface. In conventional SEM an electron beam with energy in the range 10 – 30 kV hits the sample surface exciting a range of signals which are recorded as the beam scans the surface of the sample. The combination of higher magnification, larger depth of focus, greater resolution, and ease of sample observation makes the SEM one of the most used instruments in research areas today.

Some scribes of the mask set used at CEA-LETI have been identified for characterization. As illustrated in Figure 2.2.1, different patterns dedicated to the fabrication of JLT transistors exist:

isolated or multi-channel patterns. Each of them is then measured at the following steps: active lithography, active etching, gate lithography, gate etching, spacer1 and spacer2 etching in order to know the nanowire size which will be later electrically characterized.

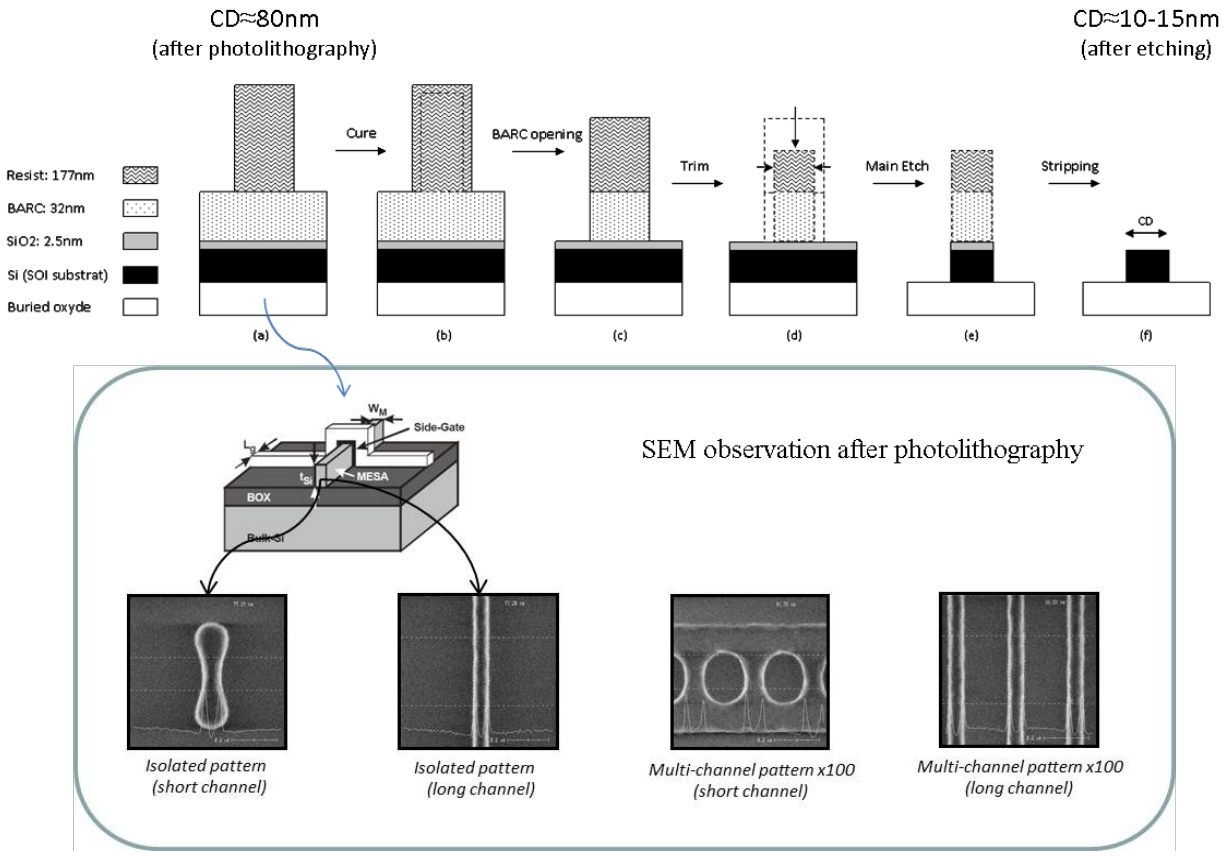
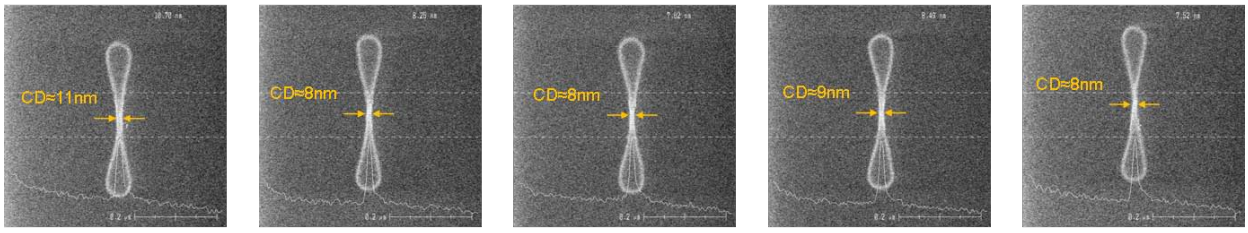


Figure 2.2.1: SEM pictures of the devices observed on various dies of the 300mm wafers after the photo-lithography. Long and short isolated devices with long and short arrays of devices (x100 fingers)

In this document, the dimension of only two patterns is reported -small isolated devices to extract I-V curves on short gate length and long array of devices to extract gate capacitance and carrier mobility. An example of devices observed after etching is shown in Fig 2.2.2.

A nanowire width down to 8nm is observed.

Devices dedicated for investigating short channel performances (short gate length Lg≈20nm)



Devices dedicated for extracting capacitances and carrier mobility (long gate length Lg ≈10µm)

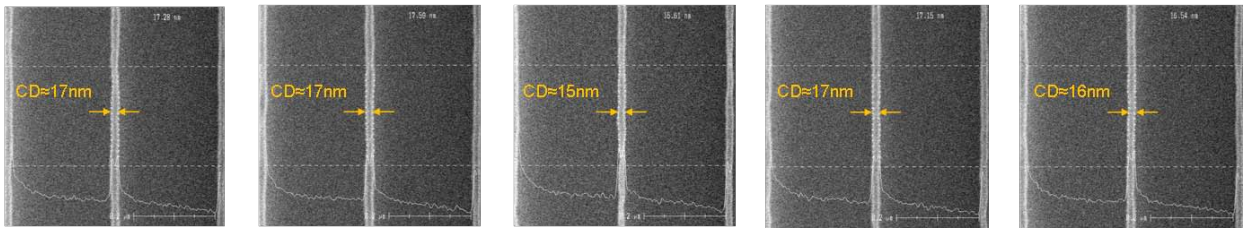


Figure 2.2.2: SEM pictures of the devices observed on various chips of the 300mm after active etching

The same observations on small isolated and short array of nanowires after gate etching are shown in Figure 2.2.3. Gate lengths down to 20nm are typically observed.

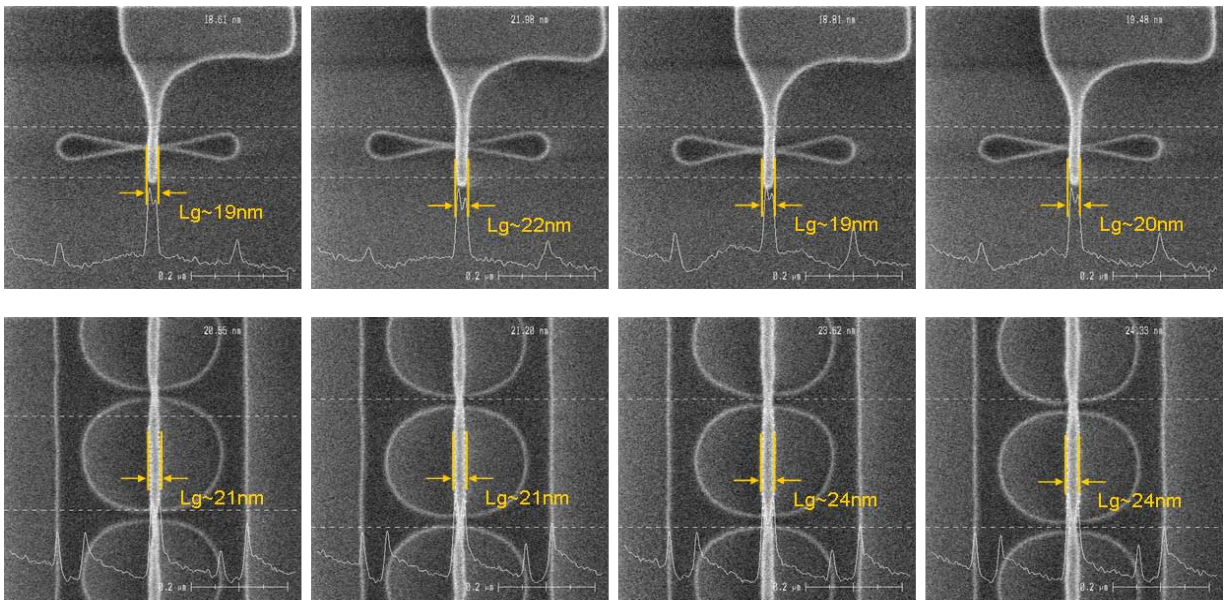


Figure 2.2.3: SEM pictures of the devices observed on various chips of the 300mm after gate etching

A summary of dimensions (width and gate length) related to different wafers (batch AAC422P) is given in Table 2. The values are averaged on 9 dies.

Scribe N1T: In order to extract Ion/Ioff plots, Subthreshold slope, DIBL, threshold voltage, etc.
Scribe N1W3: In order gate capacitance and carrier mobility, etc.

		N1T-1	N1T-2	N1T-3	N1T-4	N1T-5	N1T-6	N1T-7	N1W3-1	N1W3-2	N1W3-3	N1W3-4	N1W3-5	N1W3-5
P01	W Min (nm)	0,022	0,022	0,022	0,022	0,022	0,022	0,022	0,009	0,029	0,179	0,279	0,429	0,929
	W Mean (µm)	0,025	0,025	0,025	0,025	0,025	0,025	0,025	0,012	0,032	0,182	0,282	0,432	0,932
	W Max (nm)	0,028	0,028	0,028	0,028	0,028	0,028	0,028	0,014	0,034	0,184	0,284	0,434	0,934
	Lg (µm)	0,018	0,028	0,038	0,048	0,058	0,068	0,088	10	10	10	10	10	10
P02	W Min (nm)	0,007	0,007	0,007	0,007	0,007	0,007	0,007	too small	0,018	0,168	0,268	0,418	0,918
	W Mean (µm)	0,01	0,01	0,01	0,01	0,01	0,01	0,01	too small	0,021	0,171	0,271	0,421	0,921
	W Max (nm)	0,015	0,015	0,015	0,015	0,015	0,015	0,015	too small	0,022	0,172	0,272	0,422	0,922
	Lg (µm)	0,022	0,032	0,042	0,052	0,062	0,072	0,092	10	10	10	10	10	10
P03	W Min (nm)	0,026	0,026	0,026	0,026	0,026	0,026	0,026	0,015	0,035	0,185	0,285	0,435	0,935
	W Mean (µm)	0,029	0,029	0,029	0,029	0,029	0,029	0,029	0,017	0,037	0,187	0,287	0,437	0,937
	W Max (nm)	0,032	0,032	0,032	0,032	0,032	0,032	0,032	0,018	0,038	0,188	0,288	0,438	0,938
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P04	W Min (nm)	0,008	0,008	0,008	0,008	0,008	0,008	0,008	too small	0,02	0,17	0,27	0,42	0,92
	W Mean (µm)	0,013	0,013	0,013	0,013	0,013	0,013	0,013	too small	0,022	0,172	0,272	0,422	0,922
	W Max (nm)	0,019	0,019	0,019	0,019	0,019	0,019	0,019	too small	0,024	0,174	0,274	0,424	0,924
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P05	W Min (nm)	0,021	0,021	0,021	0,021	0,021	0,021	0,021	0,01	0,03	0,18	0,28	0,43	0,93
	W Mean (µm)	0,025	0,025	0,025	0,025	0,025	0,025	0,025	0,013	0,033	0,183	0,283	0,433	0,933
	W Max (nm)	0,029	0,029	0,029	0,029	0,029	0,029	0,029	0,016	0,036	0,186	0,286	0,436	0,936
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P06	W Min (nm)	0,009	0,009	0,009	0,009	0,009	0,009	0,009	too small	0,018	0,168	0,268	0,418	0,918
	W Mean (µm)	0,013	0,013	0,013	0,013	0,013	0,013	0,013	too small	0,021	0,171	0,271	0,421	0,921
	W Max (nm)	0,015	0,015	0,015	0,015	0,015	0,015	0,015	too small	0,023	0,173	0,273	0,423	0,923
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P07	W Min (nm)	0,021	0,021	0,021	0,021	0,021	0,021	0,021	0,011	0,031	0,181	0,281	0,431	0,931
	W Mean (µm)	0,026	0,026	0,026	0,026	0,026	0,026	0,026	0,014	0,034	0,184	0,284	0,434	0,934
	W Max (nm)	0,028	0,028	0,028	0,028	0,028	0,028	0,028	0,016	0,036	0,186	0,286	0,436	0,936
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P08	W Min (nm)	0,009	0,009	0,009	0,009	0,009	0,009	0,009	too small	0,021	0,171	0,271	0,421	0,921
	W Mean (µm)	0,013	0,013	0,013	0,013	0,013	0,013	0,013	too small	0,023	0,173	0,273	0,423	0,923
	W Max (nm)	0,017	0,017	0,017	0,017	0,017	0,017	0,017	too small	0,024	0,174	0,274	0,424	0,924
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P09	W Min (nm)	0,024	0,024	0,024	0,024	0,024	0,024	0,024	0,008	0,028	0,178	0,278	0,428	0,928
	W Mean (µm)	0,026	0,026	0,026	0,026	0,026	0,026	0,026	0,014	0,034	0,184	0,284	0,434	0,934
	W Max (nm)	0,028	0,028	0,028	0,028	0,028	0,028	0,028	0,017	0,037	0,187	0,287	0,437	0,937
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P10	W Min (nm)	0,008	0,008	0,008	0,008	0,008	0,008	0,008	too small	0,021	0,171	0,271	0,421	0,921
	W Mean (µm)	0,013	0,013	0,013	0,013	0,013	0,013	0,013	too small	0,023	0,173	0,273	0,423	0,923
	W Max (nm)	0,016	0,016	0,016	0,016	0,016	0,016	0,016	too small	0,025	0,175	0,275	0,425	0,925
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P11	W Min (nm)	0,023	0,023	0,023	0,023	0,023	0,023	0,023	0,011	0,031	0,181	0,281	0,431	0,931
	W Mean (µm)	0,028	0,028	0,028	0,028	0,028	0,028	0,028	0,015	0,035	0,185	0,285	0,435	0,935
	W Max (nm)	0,03	0,03	0,03	0,03	0,03	0,03	0,03	0,019	0,039	0,189	0,289	0,439	0,939
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P12	W Min (nm)	0,009	0,009	0,009	0,009	0,009	0,009	0,009	too small	0,021	0,171	0,271	0,421	0,921
	W Mean (µm)	0,014	0,014	0,014	0,014	0,014	0,014	0,014	too small	0,024	0,174	0,274	0,424	0,924
	W Max (nm)	0,017	0,017	0,017	0,017	0,017	0,017	0,017	too small	0,026	0,176	0,276	0,426	0,926
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10

Electrical characterization of these devices is now under investigation. TEM related to the devices showing the best electrical characteristics will be done later. However, preliminary results on junctionless NW transistors fabricated at Tyndall institute are presented below. The TEM have been done by Intel (IPLS).

2.2.3. Transmission Electron microscopy (TEM)

Transmission Electron Microscopy (TEM) and High Resolution Transmission Electron Microscopy (HRTEM) are related techniques that use an electron beam to image a sample. High energy electrons, incident on ultra-thin samples allow for image resolutions that are on the order of 1-2 Angstroms. Compared to SEM, TEM has a better spatial resolution, is capable of additional analytical measurements but requires significantly more sample preparation. Therefore, this technique cannot be used to morphologically characterize all the JLT transistors which will be electrically measured but can be employed to identify accurately the size of devices which are representative of the population.

TEM and high resolution TEM (HRTEM) are very useful tools for the characterisation of nanostructures such as nanowire transistors after complete processing. This technique is very useful to measure the following dimensions: the silicon thickness, the nanowire width, the gate length, etc.

In the following, TEM cross sections are illustrated to characterize the critical dimensions of the junctionless nanowire transistors fabricated at Tyndall institute.

The prototype samples delivered to IPLS consist of a half 4-inch SOI wafer with 7 fields containing 198 devices each. These devices are junctionless transistors with single or multiple fingers and different gate lengths and nanowire dimensions. The gate oxide is 10 nm thick, covered by a 50 nm polysilicon gate (schematic view in Figure 2.2.4).

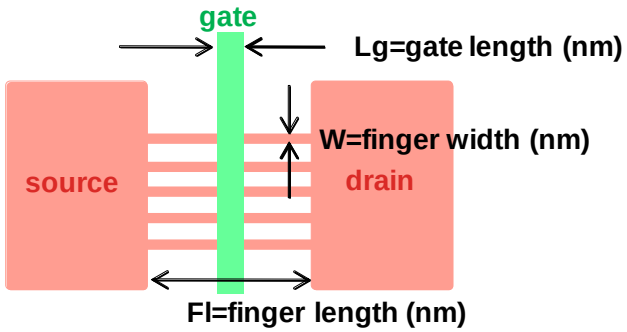


Figure 2.2.4. Top-down of the devices with critical dimensions.

For the analysis of nanowires with TEM the sample preparation is very critical in order to obtain excellent analysis results. This is done using an in-situ lift out technique on a dual-beam FEI Strata 400 focused ion-beam (FIB). The lift-out procedure consists on locating the area of interest using the FIB microscope capabilities. Then a layer of FIB-deposited Pt is placed over the area of interest to prevent milling or surface damaging. Using a large beam current, two trenches are created on either side of the Pt strap. A smaller beam current is used to thin the central part between the trenches and three cuts are made to frame the area of interest. The omniprobe is inserted and positioned on the membrane and is pasted to it by depositing Pt. Then, the membrane is lifted and brought to a premounted grid where is pasted. At this point, the omniprobe can be cut from the sample. Finally, once the sample is seated on the grid, it is thinned to a thickness of approx 100nm suitable for TEM imaging.

The transmission electron microscopy (TEM) analysis was performed on a FEI Technai G20 LaB6 operating at an accelerating voltage of 200 kV.

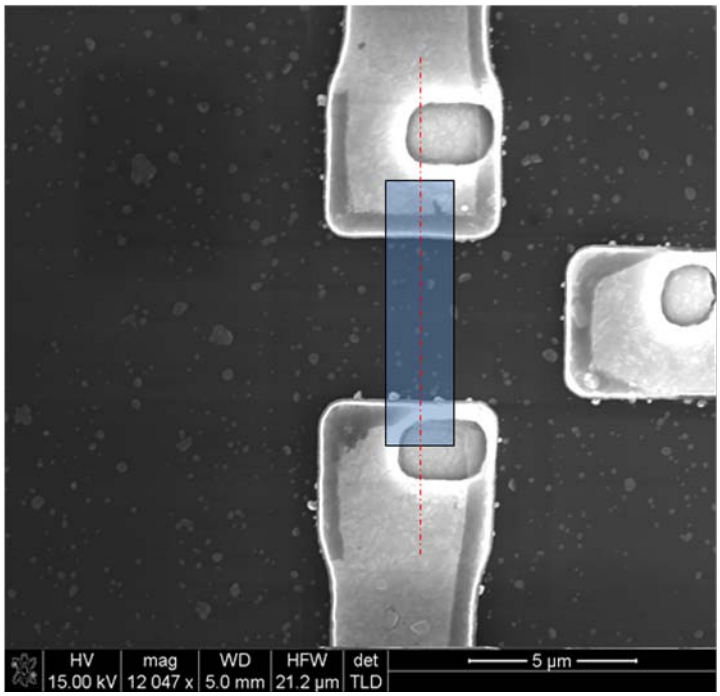


Figure 2.2.5. Top down SEM overview with Pt location and section direction.

The first TEM analysis was done on a wide single nanowire transistor along the nanowire length in order to check the silicon thickness, the effective gate length and quantify the gate undercut (see Figure 2.2.6).

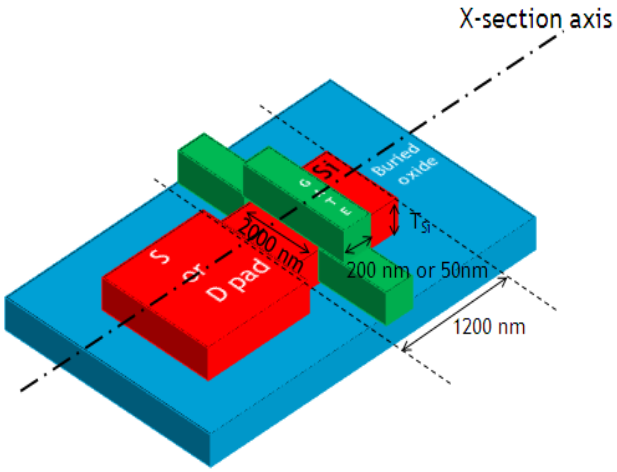


Figure 2.2.6 Schematic of the nanowire transistor structure used for the first TEM analysis and the cross section axis.

In Fig. 2.2.7 it can be seen that the gate hasn't been fully etched, still remaining around 8nm of poly-silicon. Tyndall is currently running a few test to optimise the gate etching sequence (breakthrough and softlanding times).

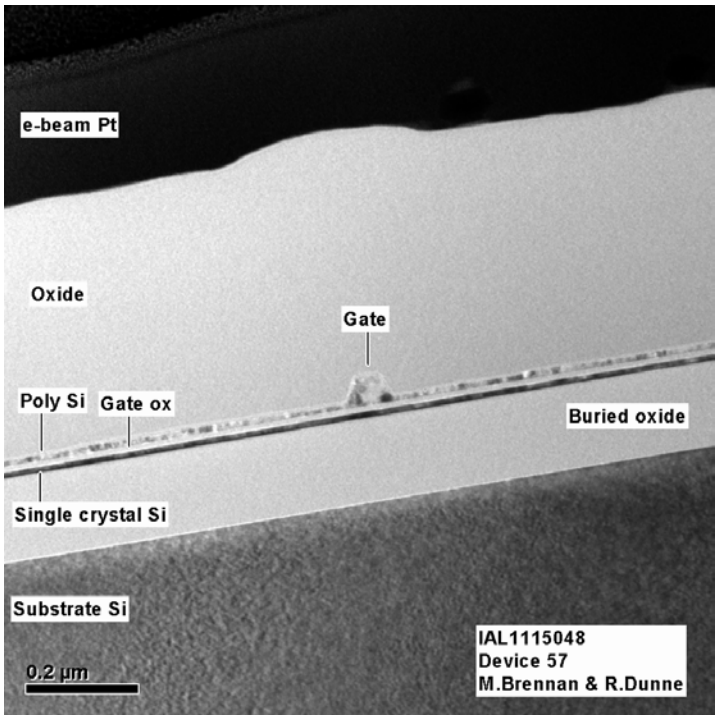


Fig. 2.2.7: TEM cross section along the nanowire showing the incomplete etching of the poly-silicon gate.

The nominal gate length for the 2 devices analysed was 50 and 200nm. The resulting gates as shown in Fig. 2.2.8 have a length at the base of 80 and 223nm respectively, which corresponds to 30 and 23 nm differences between the layout and the printed length, respectively. The poly gate

is a lso not s howing a s traight ve rtical pr ofile, with a s ignificant s idewall inc lination, which would suggest an excessive polymerizing gas flow during the dry etch.

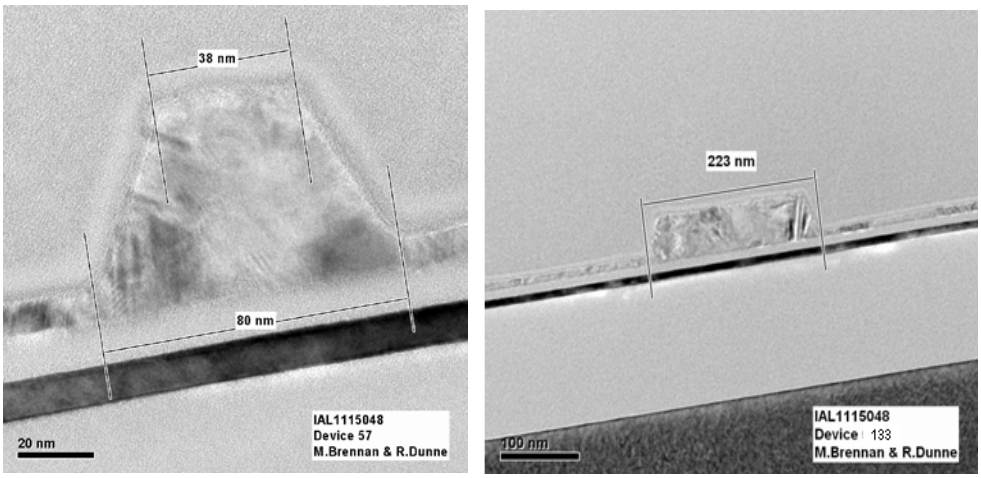


Figure 2.2.8: HRTEM of the polysilicon gate showing the effective gate length measurements.

The second TEM analysis was done on a multiple finger transistor and cutting along the gate to measure t he na nowire d imensions (Fig. 2.2.9). T he s tructure a nalysed consists of 20 f ingers which are 50nm wide with an expected Si thickness between 5 and 10 nm.

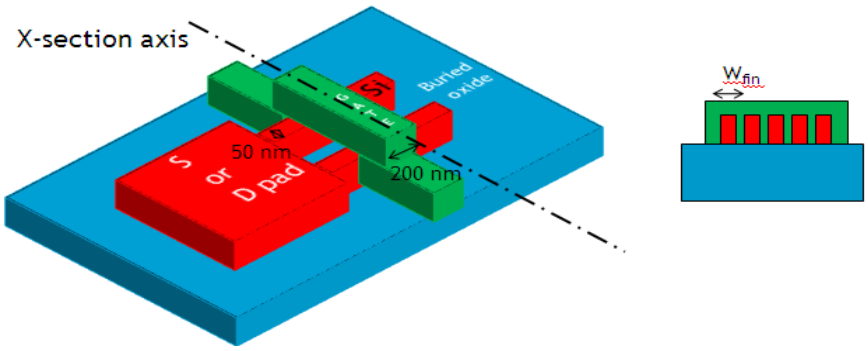


Figure 2.2.9: Schematic of the nanowire transistor structure used for the second TEM analysis and the cross section axis.

Fig 2.2.10 shows the TEM cross section of 3 consecutive fingers. They have a dog bone type of shape (thinner i n t he m iddle), a w idth of 40nm a nd a S i t hickness between 4.8 a nd 6.5 nm (Fig. 2.2.11). The width of the rest of nanowires in the structure hasn't been measured but it was consistently uniform across the structure.

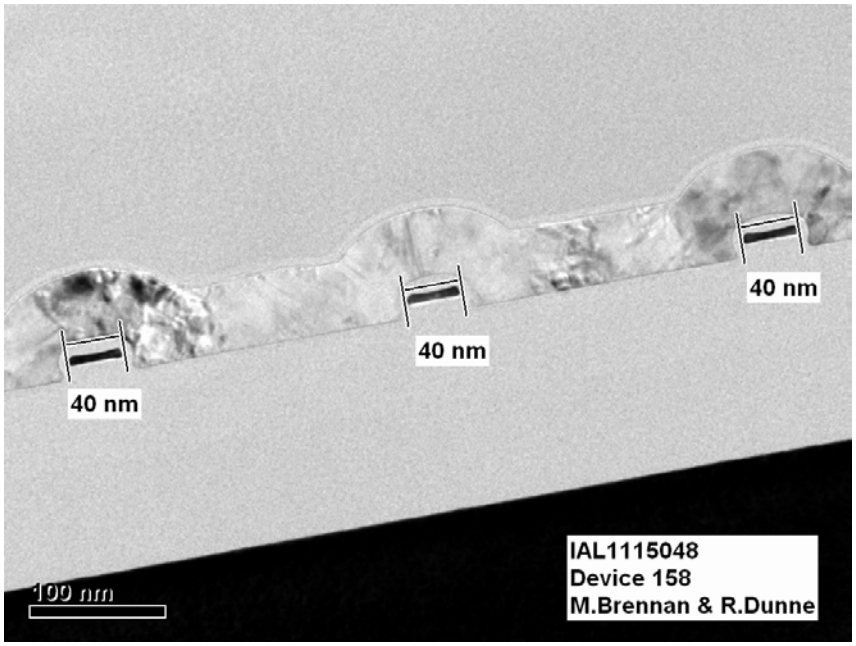


Figure 2.2.10: TEM cross section along the gate showing 3 adjacent nanowires.

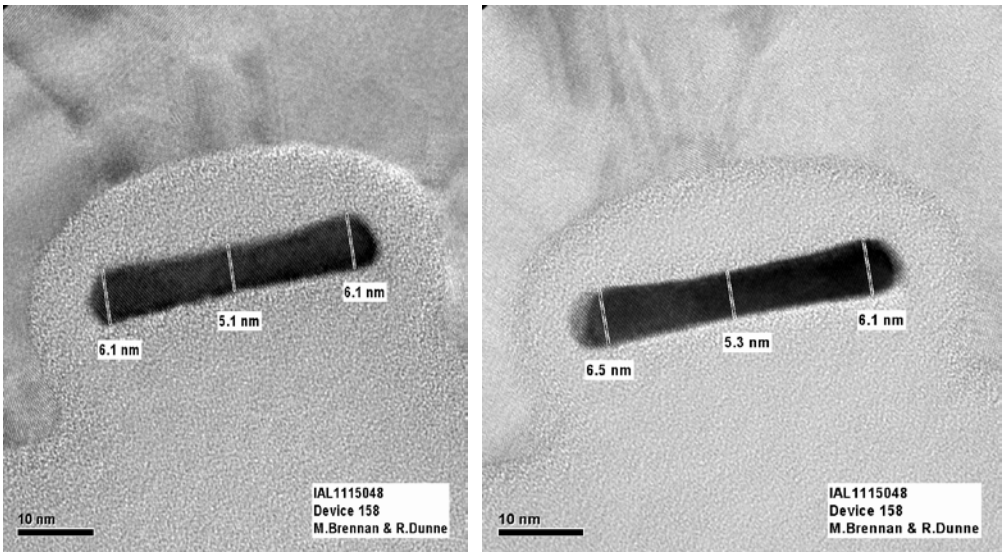


Figure 2.2.11: HRTEM image showing the nanowire Si thickness for 2 adjacent fingers.

The poly-silicon gate thickness is around 48 nm and the gate oxide thickness varies from 5.7 nm (at the edge, where is thinner) to 10.5 nm (at the centre, where is thicker) as seen in Fig 2.2.12.

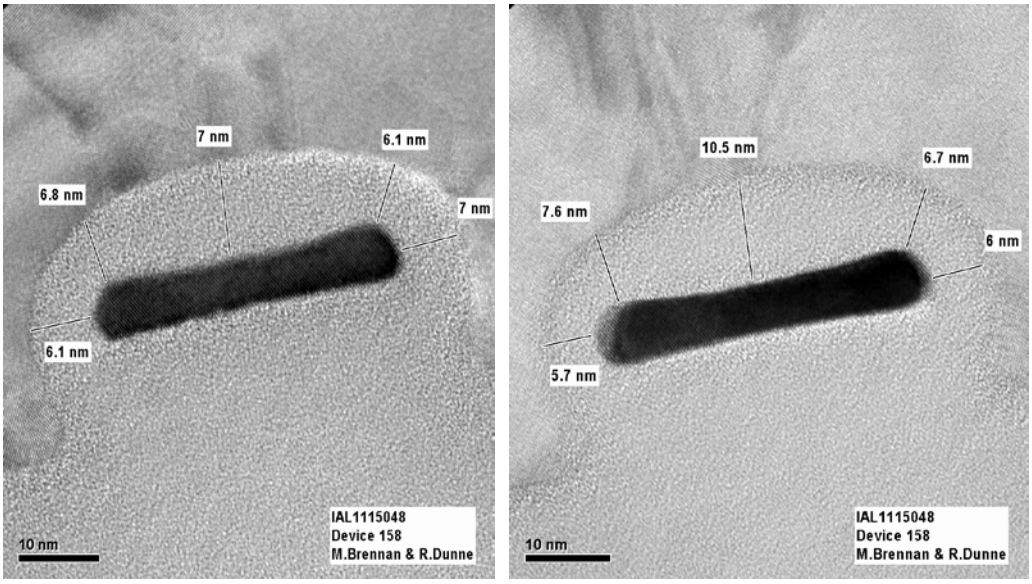


Figure 2.2.12: HRTEM image showing the gate oxide thickness measurements.

3. Conclusion

In conclusion, various morphological characterization techniques used in this work (ellipsometry, SEM, TEM) allow us to accurately measure the thickness, the width and the gate length of the fabricated nanowires to assess the influence of the processing on the nanowire geometry and quality.

Additional morphological characterization (TEM) will be done after electrical characterization of the junctionles nanowire transistors fabricated at CEA-LETI (batch AAC422P).