SQWIRE

FP7 - EU

Silicon Quantum Wire Transistors

month 12 report

Deliverable D5.2

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Project Coordinator Address

SQWIRE has now been running for a year. The junctionless transistor concept has gained acceptance worldwide and several articles on the device are published every month by different research groups worldwide. The highlights of this first year of research are:

- The SQWIRE consortium maintains its leadership with the experimental demonstration of junctionless transistors with a gate length of 15nm and a DIBL of 27 mV/V. The saturation subthreshold slope is 70 mV/decade for L=15 nm and 62 mV/decade for L=90 nm. I_{on} and I_{off} of 280 μA/μm @ V_{GS}=V_{DS}=0.9V and 0.36nA/μm @ V_{GS}=0V and V_{DS}=0.9V have been obtained.

- Devices have been delivered to different partners for characterization and evaluation.

- A simulator capable of simulating tunneling and other quantum effects is being implemented in a commercial GUI.

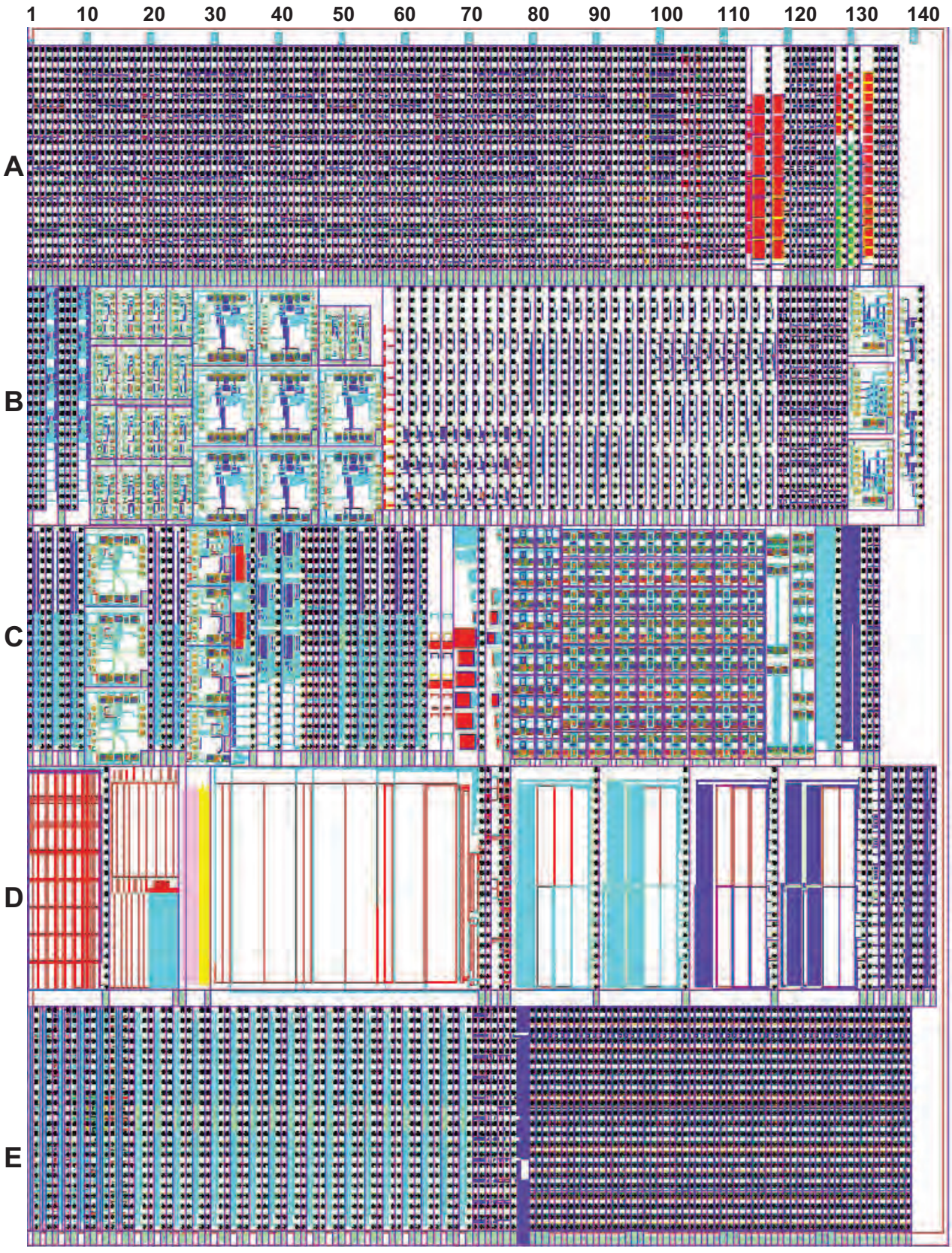
- A first joint publication “Low-frequency noise in junctionless multigate transistors” was issued in Appl. Phys. Lett. Vol. 98, p. 133502

We are now looking forward to characterizing the devices in detail and providing feedback to the partners developing device models.

J.P. Colinge, SQWIRE Project Coordinator, 2nd September 2011

Overall Die Description

Global view



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Milestone M2.3: Existing mask set adapted for Variable Barrier Transistors design

Sylvain Barraud

CEA-Leti, Minatec campus, 17 rue des martyrs
F-38690 Grenoble, Cedex09, France

Nanowire (NW) and Tri-gated Complementary Metal Oxide Semiconductor (CMOS) technology appear as an attractive option to overcome standard CMOS bulk technology limits in terms of scaling, performances and power consumption. The electrostatic control over the channel is indeed improved in NWs, leading to a significant reduction of short channel effects and thus leakage currents in the OFF state. Based on existing expertise in fabrication of FD-SOI nanowire devices, we will develop a fabrication route for n-channel and p-channel *Variable Barrier* nanowire transistor. We propose the fabrication of tri-gate nanowire transistors that include soft tunnel barriers which should strongly reduce source-to-drain tunneling and could even, in theory, achieve sub-60 mV/dec subthreshold slopes.

Existing mask set is used, with the exception of the active area level which will have to be redrawn. The FD-SOI route is adapted in order to target NW with width varying from $10\text{nm} \leq W \leq 20\text{nm}$, silicon thickness T_{SOI}=10nm and with a gate length $L_G < 30\text{nm}$. Below the results of the first run are presented.

I. SCRIBES DESCRIPTION

The fabrication of variable barrier transistors is based on different scribes with various gate lengths and various widths. The gate length and the nanowire width can be varied from 10µm down to 20nm (for the gate), and from 10µm down to 15nm (for the width). Examples of device drawn in the existing mask set are represented in Fig. 1a,b,c.

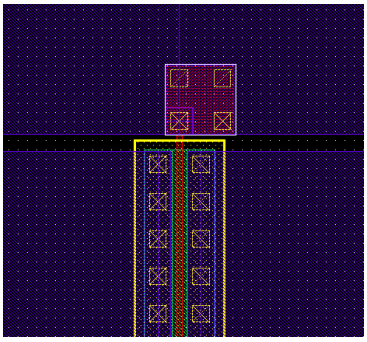


Fig. 1a: Future VBT MOSFET transistor with wide width (10µm)

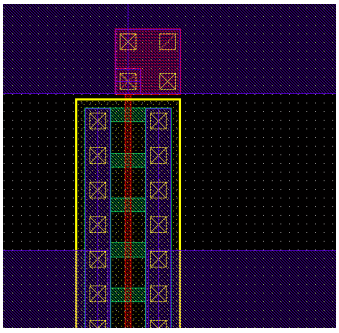


Fig. 1b: Array of future VBT MOSFET transistors with small width (~15nm after trimming and etching)

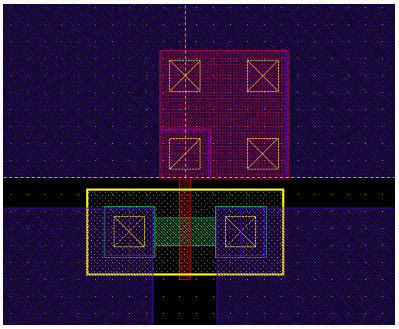
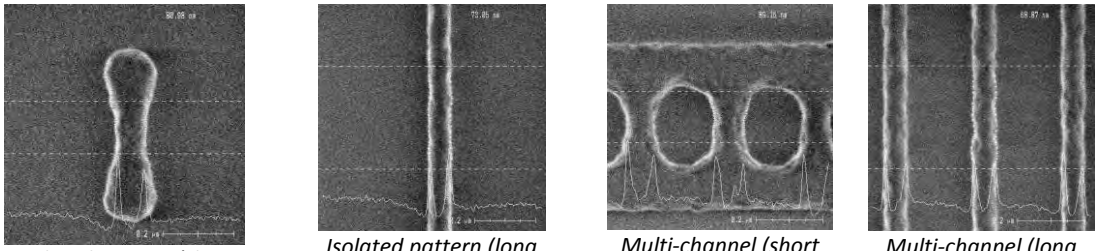


Fig. 1c: Future VBT MOSFET transistor with small width (~15nm after trimming and etching)

II. PROCESS DESCRIPTION

Silicon-on-Insulator (SOI) structures with silicon layers of 12 nm in thickness are used. The key for the fabrication of variable barrier tunneling MOSFET transistors is the formation and the control of both constrictions at the edges of the gate. The silicon layer is patterned to create the silicon nanowires and wide devices by using a mesa isolation technique. To do that, the active stack used is consisted of a 12nm undoped Si, 2.5nm SiO_2 dielectric layer and an organic bottom anti-reflective coating (BARC) layer of around 24nm patterned using 193nm ArF resist. The thickness of the photoresist is around 160nm. The active zone (i.e. nanowire feature) is carried out using the trimmed resist/BARC as a mask. Obviously, the final linewidth of nanowires is determined mainly by the amount of trimmed resist. The investigated structures after the photolithography are shown in Fig. 2. They comprised isolated lines (NW) and arrays of lines with long and short dimensions. The arrays of lines with long dimensions are used to extract the capacitance and the carrier mobility. The smallest devices (Lg) are used to investigate electrical performances as for example DIBL, subthreshold slope, $I_{DS}(V_{GS})$, and $I_{DS}(V_{DS})$ characteristics, etc. All the critical

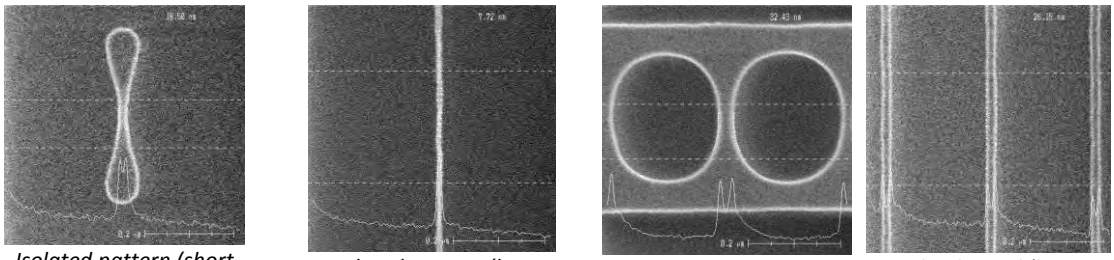
dimension (CD) measurements (after photolithography and after active patterning) are done using in-line field-emission-scanning electron microscope (SEM).



Isolated pattern (short channel) *Isolated pattern (long channel)* *Multi-channel (short dimension)* *Multi-channel (long dimension)*

Figure 2: SEM pictures of the devices observed on various chips of the 300mm wafers after the photo-lithography. Long and short isolated devices with long and short arrays of devices (x100 fingers)

The linewidth before etching is around 80nm. After etching, the reduction of the silicon nanowire width induces by the trimming is targeted to 65 nm in order to have nanowire width of around 15nm. Due to the dispersions induce by the photolithography, the NW width after etching is expected to vary between 10nm and 20nm. In Fig. 3, the same pattern that in Fig. 2 are presented after the etching (active patterning).



Isolated pattern (short channel) *Isolated pattern (long channel)* *Multi-channel (short dimension)* *Multi-channel (long dimension)*

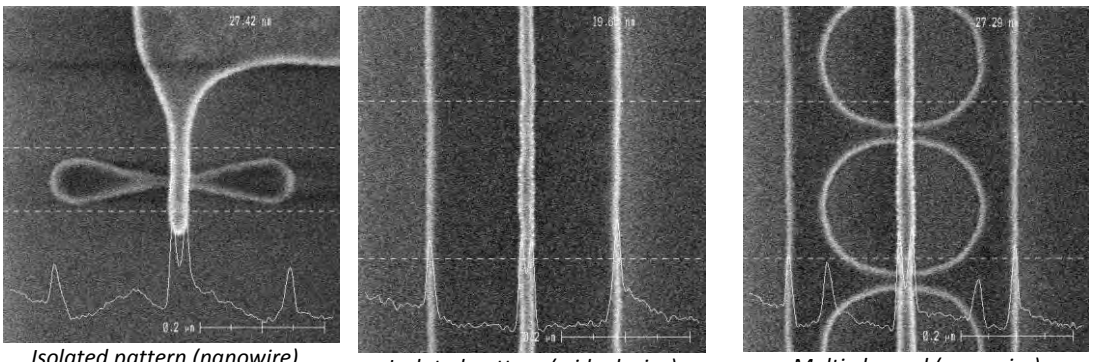
Figure 3: SEM pictures of the devices observed on various chips of the 300mm wafers after the active patterning. Long and short isolated devices with long and short arrays of devices (x100 fingers)

The gate stack used is composed of high-κ/metal gate. 2.3nm chemical vapour deposition (CVD) HfSiON with 5nm ALD TiN and Poly-Silicon (50nm) layers are deposited. This corresponds to an equivalent oxide thickness (EOT) of around 1.2nm. As for the active patterning, 193nm lithography tool is used with a resist trimming in order to address gate lengths down to 20nm. Two ways are investigated to create the both constrictions.

First approach: The both constrictions are fabricated after the gate etching. A over-etch of the silicon film is done in order to reduce the thickness. Then, we propose to

do a deposition of thin spacer (SiN nitride) to create the barrier between the source-drain and the channel. After the thin spacer etching, an epitaxial undoped silicon growth is realized to recover the barrier and to form the both constrictions. Afterwards, a nitride spacer thickness of around 15nm will be formed on the silicon source-drain. Then, low parasitic resistance will be realized by epitaxial doped silicon growth on the source-drain (ΔT_{SI}=18nm).

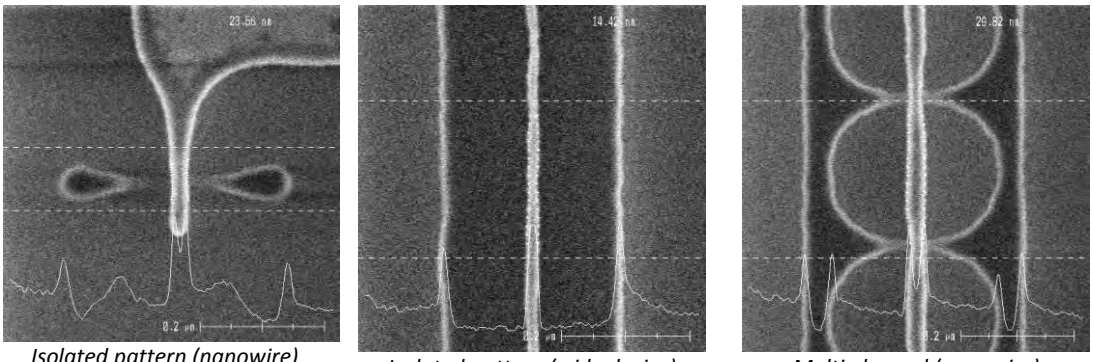
In Fig. 4, we present the first results obtained after the over-etch of the silicon film.



Isolated pattern (nanowire) *Isolated pattern (wide device)* *Multi-channel (nanowire)*

Figure 4: SEM pictures of the devices observed on various chips of the 300mm wafers after the over-etch of the Si film. Long and short isolated devices with short arrays of devices (x100 fingers)

In the Fig. 4, the nanowire width was around 30nm before the over-etch. For the smallest dimension (sub-20nm for the width), the results are shown in Fig. 5.



Isolated pattern (nanowire) *Isolated pattern (wide device)* *Multi-channel (nanowire)*

Figure 5: SEM pictures of the devices observed on various chips of the 300mm wafers after the over-etch of the Si film. Long and short isolated devices with short arrays of devices (x100 fingers)

We can clearly observed that for wide device, the over-etch of the silicon film is correctly done. However, in the case of nanowire, the over-etch (which can be characterized by an oxidation) remove the Si wire on both side of the gate. The control of this over-etch is currently in progress. The next steps will be the following: A thin spacer deposition, etching of the spacer, source/drain epitaxy to create the

constrictions. The formation of both constrictions will be characterized by using TEM image after the source/drain epitaxy.

Second approach: In the second approach, the over-etch is done just after the first spacer deposition. A over-etch of the silicon film is done in order to reduce the thickness. As previously, we propose to do a deposition of thin spacer (SiN) to create the barrier between the source-drain and the channel. After the thin spacer etching, an epitaxial undoped silicon growth will be realized to recover the barrier and to form the both constrictions. Afterwards, a nitride spacer thickness of around 15nm will be formed on the silicon source-drain. Then, low parasitic resistance will be realized by epitaxial doped silicon growth on the source-drain (ΔT_{SI}=18nm). Then, a second spacer will be deposited and etched before the source-drain doping. In Fig. 6, we show the result obtained after the over-etch of the Si film.

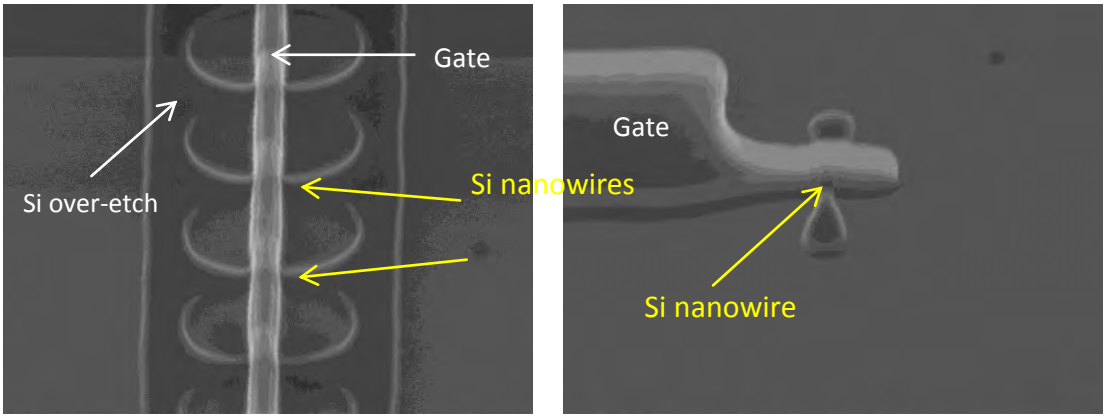
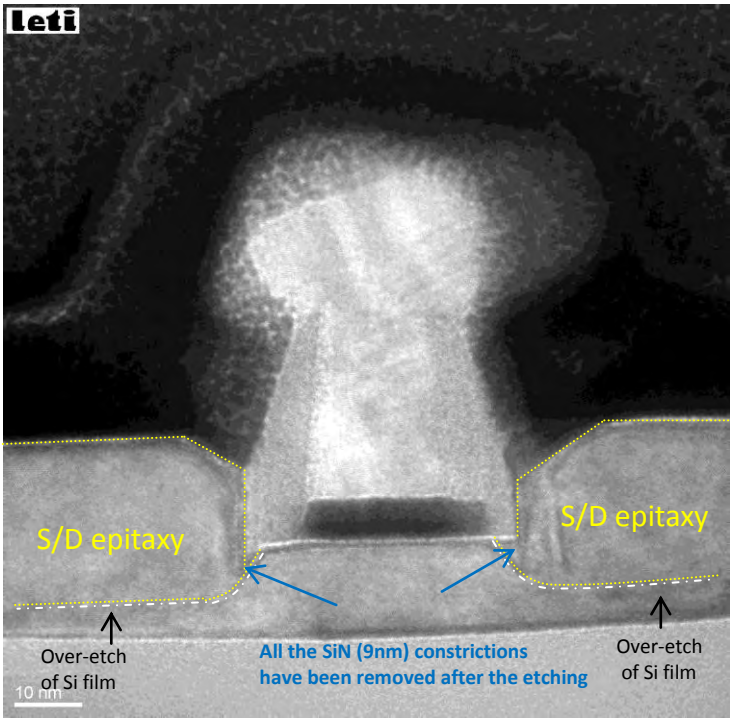


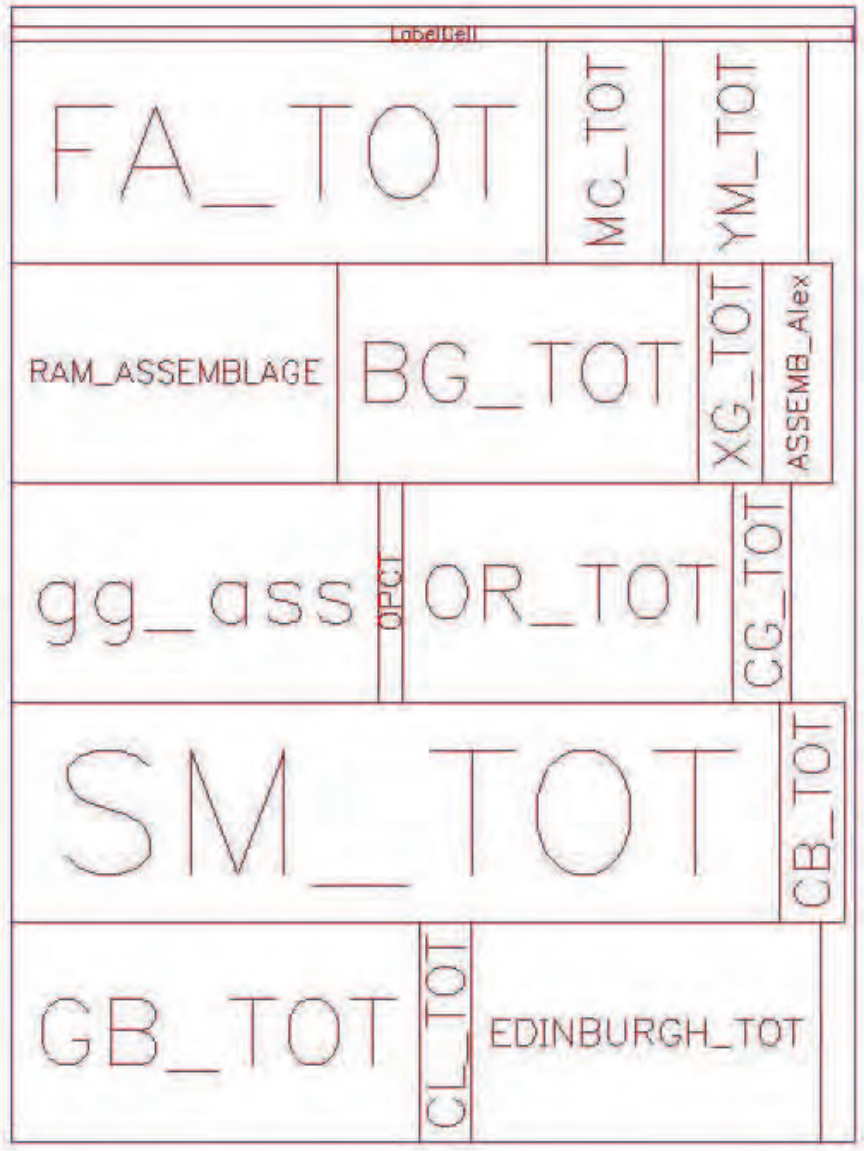
Figure 6: SEM pictures of the devices observed on various chips of the 300mm wafers after the over-etch of the Si film.

In Figure 7, a TEM image shows the result after the source-drain epitaxy. Here, the thin spacer of around 9nm has been deposited to create the both constrictions. After the etching and the various cleaning performed before the epitaxial growth (to recover the barrier), the constrictions have been fully removed. Then, new thicknesses must be tested in order to keep around 2-3nm of SiN after etching and cleaning. New tests are in progress.


Leti
S/D epitaxy
S/D epitaxy
Over-etch
of Si film
All the SiN (9nm) constrictions
have been removed after the etching
Over-etch
of Si film
10 nm

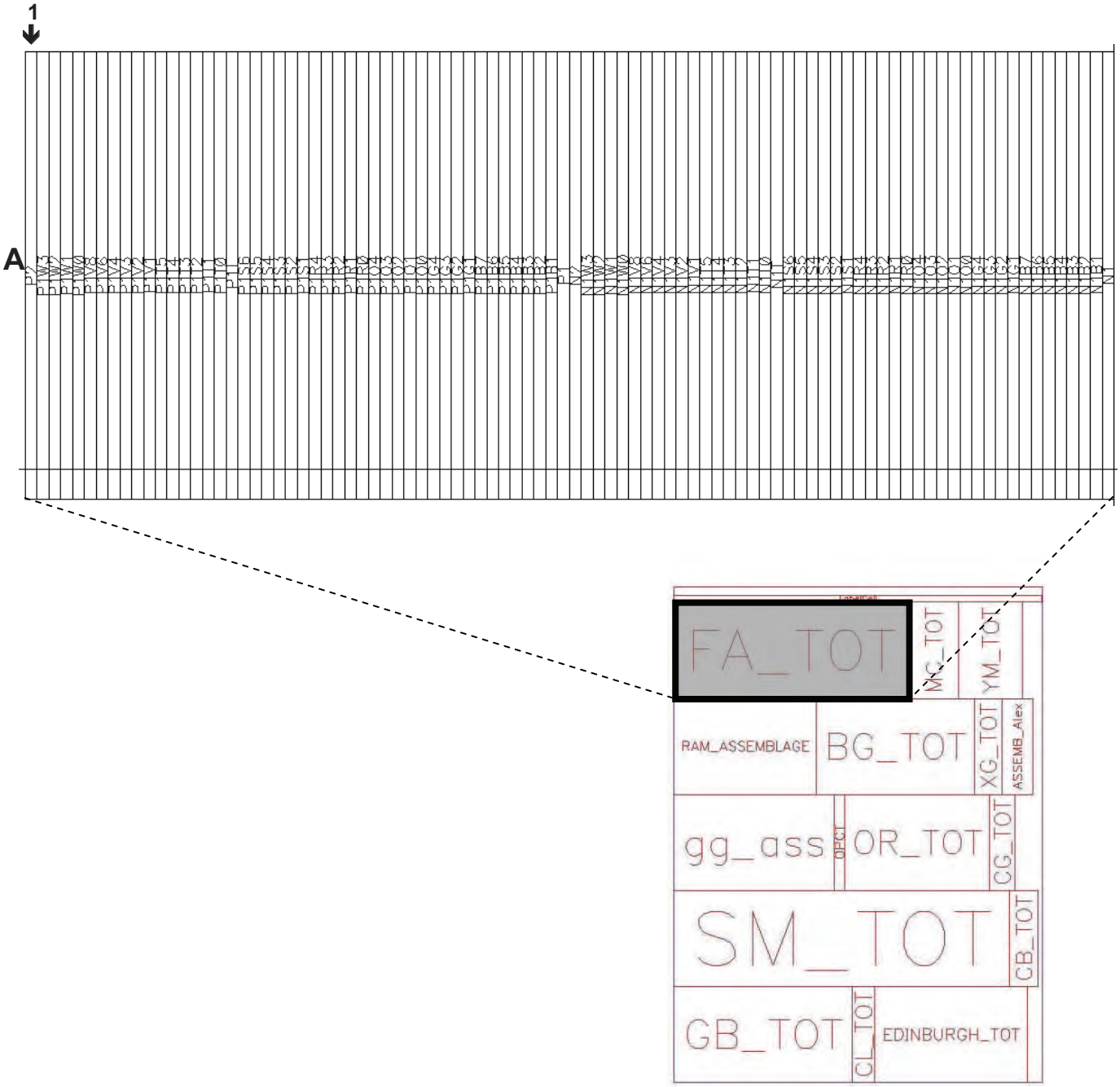
MUST RETICLE DESCRIPTION

Block view



FA_TOT: Fully Depleted SOI transistors
MC_TOT: Capacitance modules
YM_TOT: Front End Modules
RAM_ASSEMBLAGE: small SRAM cells
BG_TOT: NAND, NOR and TEM modules
XG_TOT: Body contacted devices
ASSEMB_Alex: 16 bit adder
Gg_ass: ESD and Mismatch modules
OPCT: OPC model
OR_TOT: Varactor and RF modules
CG_TOT:
SM_TOT: Back End Modules
CB_TOT: ESD and analog Modules
GB_TOT: ESD and Mismatch modules
CL_TOT: MOS capacitors
EDINBURGH_TOT: Double patterning

Fully Depleted Devices



MUST RETICLE DESCRIPTION

Scribe name	Coordinates	Responsible
N1, P1		F. ANDRIEU

Brief description of the scribe

Standard isolated N and pMOS with various gate lengths at W=10µm.

Device list

#	*Device type **	*Parameters*
1	Standard Nmos or Pmos	W=10µm, L=30nm, Orientation=0°, 1 channel
2	Standard Nmos or Pmos	W=10µm, L=40nm, Orientation=0°, 1 channel
3	Standard Nmos or Pmos	W=10µm, L=50nm, Orientation=0°, 1 channel
4	Standard Nmos or Pmos	W=10µm, L=60nm, Orientation=0°, 1 channel
5	Standard Nmos or Pmos	W=10µm, L=70nm, Orientation=0°, 1 channel
6	Standard Nmos or Pmos	W=10µm, L=80nm, Orientation=0°, 1 channel
7	Standard Nmos or Pmos	W=10µm, L=100nm, Orientation=0°, 1 channel

*: as defined in the DRM for transistors and gated diodes

Scribe pads structure

☑ Standard (22 pads) ☐ No pads ☑ Other choice (user defined)

Testing levels

☐ Active ☐ Poly1/Poly2 ☑ Metal 1 ☑ Metal 2

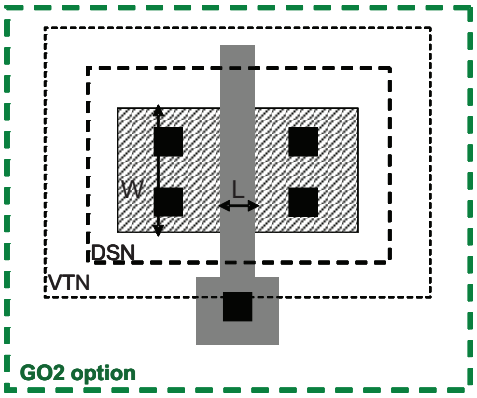
Number of module spaces reserved for the scribe

Above pads line 0 Below pads line 0

Pads assignment

Pad	*Connection*	*Pad*	*Connection*
1	Source of device 1	12	Gate of device 4
2	Drain of device 1	13	Source of device 5
3	Gate of device 1	14	Drain of device 5
4	Source of device 2	15	Gate of device 5
5	Drain of device 2	16	Source of device 6
6	Gate of device 2	17	Drain of device 6
7	Source of device 3	18	Gate of device 6
8	Drain of device 3	19	Source of device 7
9	Gate of device 3	20	Drain of device 7
10	Source of device 4	21	Gate of device 7
11	Drain of device 4	22	

Device description



Drawing of nMOSFET

MUST RETICLE DESCRIPTION

Scribe name	Coordinates	Responsible
N1T, P1T		F. ANDRIEU

Brief description of the scribe

Standard isolated N and pMOS with various gate lengths at W=80nm.

Device list

#	*Device type **	*Parameters*
1	Standard Nmos or Pmos	W=80nm, L=30nm, Orientation=0°, 1 channel
2	Standard Nmos or Pmos	W=80nm, L=40nm, Orientation=0°, 1 channel
3	Standard Nmos or Pmos	W=80nm, L=50nm, Orientation=0°, 1 channel
4	Standard Nmos or Pmos	W=80nm, L=60nm, Orientation=0°, 1 channel
5	Standard Nmos or Pmos	W=80nm, L=70nm, Orientation=0°, 1 channel
6	Standard Nmos or Pmos	W=80nm, L=80nm, Orientation=0°, 1 channel
7	Standard Nmos or Pmos	W=80nm, L=100nm, Orientation=0°, 1 channel

*: as defined in the DRM for transistors and gated diodes

Scribe pads structure

☑ Standard (22 pads) ☐ No pads ☐ Other choice (user defined)

Testing levels

☐ Active ☐ Poly1/Poly2 ☑ Metal 1 ☑ Metal 2

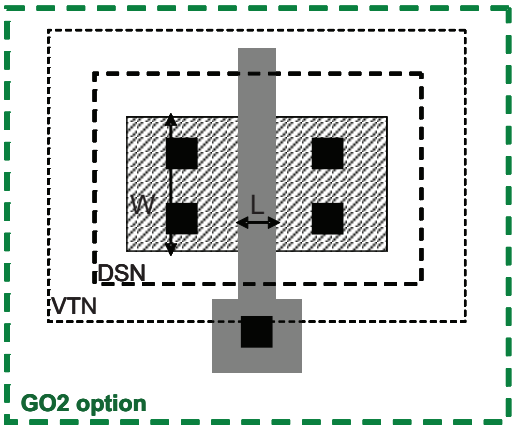
Number of module spaces reserved for the scribe

Above pads line 0 Below pads line 0

Pads assignment

Pad	*Connection*	*Pad*	*Connection*
1	Source of device 1	12	Gate of device 4
2	Drain of device 1	13	Source of device 5
3	Gate of device 1	14	Drain of device 5
4	Source of device 2	15	Gate of device 5
5	Drain of device 2	16	Source of device 6
6	Gate of device 2	17	Drain of device 6
7	Source of device 3	18	Gate of device 6
8	Drain of device 3	19	Source of device 7
9	Gate of device 3	20	Drain of device 7
10	Source of device 4	21	Gate of device 7
11	Drain of device 4	22	

Device description



Drawing of nMOSFET

MUST RETICLE DESCRIPTION

Scribe name	Coordinates	Responsible
N1W0, P1W0		F. ANDRIEU

Brief description of the scribe

Standard isolated multi-fin N and pMOS with various gate widths at L=30nm.

Device list

#	*Device type **	*Parameters*
1	Standard Nmos or Pmos	W=0.08µm, L=30nm, Orientation=0°, 50 channel
2	Standard Nmos or Pmos	W=0.1µm, L=30nm, Orientation=0°, 50 channel
3	Standard Nmos or Pmos	W=0.25µm, L=30nm, Orientation=0°, 50 channel
4	Standard Nmos or Pmos	W=0.35µm, L=30nm, Orientation=0°, 50 channel
5	Standard Nmos or Pmos	W=0.5µm, L=30nm, Orientation=0°, 50 channel
6	Standard Nmos or Pmos	W=1µm, L=30nm, Orientation=0°, 50 channel
7		

*: as defined in the DRM for transistors and gated diodes

Scribe pads structure

☑ Standard (22 pads) ☐ No pads ☐ Other choice (user defined)

Testing levels

☐ Active ☐ Poly1/Poly2 ☑ Metal 1 ☑ Metal 2

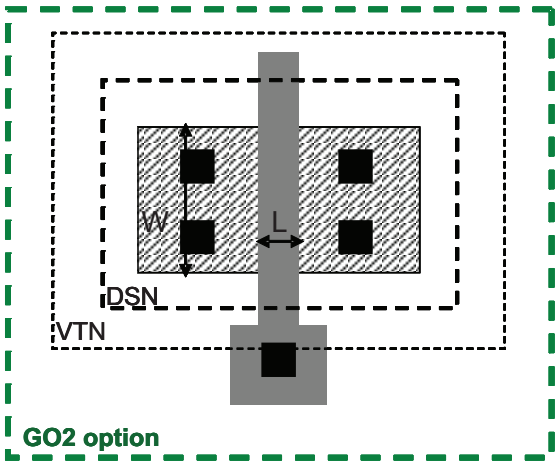
Number of module spaces reserved for the scribe

Above pads line 0 Below pads line 0

Pads assignment

Pad	*Connection*	*Pad*	*Connection*
1	Source of device 1	12	Gate of device 4
2	Drain of device 1	13	Source of device 5
3	Gate of device 1	14	Drain of device 5
4	Source of device 2	15	Gate of device 5
5	Drain of device 2	16	Source of device 6
6	Gate of device 2	17	Drain of device 6
7	Source of device 3	18	Gate of device 6
8	Drain of device 3	19	
9	Gate of device 3	20	
10	Source of device 4	21	
11	Drain of device 4	22	

Device description



Drawing of nMOSFET

MUST RETICLE DESCRIPTION

Scribe name	Coordinates	Responsible
N1W1, P1W1		F. ANDRIEU

Brief description of the scribe

Standard isolated multi-fin N and pMOS with various gate widths at L=50nm.

Device list

#	*Device type **	*Parameters*
1	Standard Nmos or Pmos	W=0.08µm, L=50nm, Orientation=0°, 50 channel
2	Standard Nmos or Pmos	W=0.1µm, L=50nm, Orientation=0°, 50 channel
3	Standard Nmos or Pmos	W=0.25µm, L=50nm, Orientation=0°, 50 channel
4	Standard Nmos or Pmos	W=0.35µm, L=50nm, Orientation=0°, 50 channel
5	Standard Nmos or Pmos	W=0.5µm, L=50nm, Orientation=0°, 50 channel
6	Standard Nmos or Pmos	W=1µm, L=50nm, Orientation=0°, 50 channel
7		

*: as defined in the DRM for transistors and gated diodes

Scribe pads structure

☑ Standard (22 pads) ☐ No pads ☐ Other choice (user defined)

Testing levels

☐ Active ☐ Poly1/Poly2 ☑ Metal 1 ☑ Metal 2

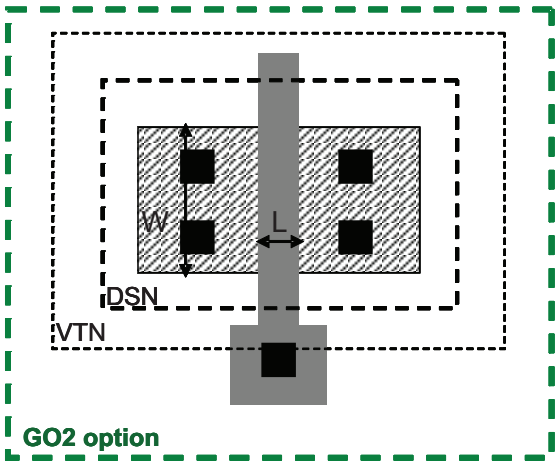
Number of module spaces reserved for the scribe

Above pads line 0 Below pads line 0

Pads assignment

Pad	*Connection*	*Pad*	*Connection*
1	Source of device 1	12	Gate of device 4
2	Drain of device 1	13	Source of device 5
3	Gate of device 1	14	Drain of device 5
4	Source of device 2	15	Gate of device 5
5	Drain of device 2	16	Source of device 6
6	Gate of device 2	17	Drain of device 6
7	Source of device 3	18	Gate of device 6
8	Drain of device 3		
9	Gate of device 3		
10	Source of device 4		
11	Drain of device 4		

Device description



Drawing of nMOSFET

MUST RETICLE DESCRIPTION

Scribe name	Coordinates	Responsible
N1W2, P1W2		F. ANDRIEU

Brief description of the scribe

Standard isolated multi-fin N and pMOS with various gate widths at L=100nm.

Device list

#	*Device type **	*Parameters*
1	Standard Nmos or Pmos	W=0.08µm, L=100nm, Orientation=0°, 50 channel
2	Standard Nmos or Pmos	W=0.1µm, L=100nm, Orientation=0°, 50 channel
3	Standard Nmos or Pmos	W=0.25µm, L=100nm, Orientation=0°, 50 channel
4	Standard Nmos or Pmos	W=0.35µm, L=100nm, Orientation=0°, 50 channel
5	Standard Nmos or Pmos	W=0.5µm, L=100nm, Orientation=0°, 50 channel
6	Standard Nmos or Pmos	W=1µm, L=100nm, Orientation=0°, 50 channel
7		

*: as defined in the DRM for transistors and gated diodes

Scribe pads structure

☑ Standard (22 pads) ☐ No pads ☐ Other choice (user defined)

Testing levels

☐ Active ☐ Poly1/Poly2 ☑ Metal 1 ☑ Metal 2

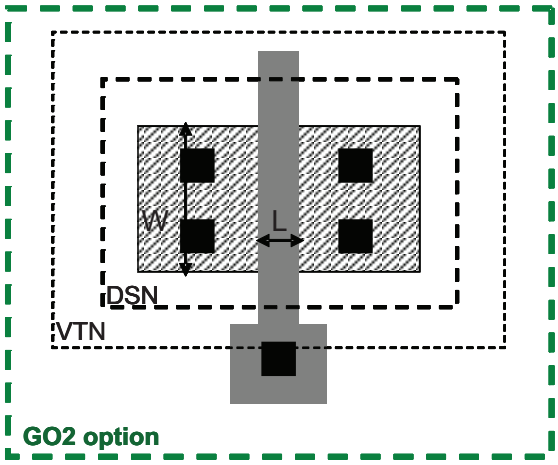
Number of module spaces reserved for the scribe

Above pads line 0 Below pads line 0

Pads assignment

Pad	*Connection*	*Pad*	*Connection*
1	Source of device 1	12	Gate of device 4
2	Drain of device 1	13	Source of device 5
3	Gate of device 1	14	Drain of device 5
4	Source of device 2	15	Gate of device 5
5	Drain of device 2	16	Source of device 6
6	Gate of device 2	17	Drain of device 6
7	Source of device 3	18	Gate of device 6
8	Drain of device 3	22	Common Source
9	Gate of device 3		
10	Source of device 4		
11	Drain of device 4		

Device description



Drawing of nMOSFET

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Tel : 33 – 04 38 78 30 51 – Fax : 33 – 04 38 78 30 34 – brigitte.gaillard@cea.fr

MUST RETICLE DESCRIPTION

Scribe name	Coordinates	Responsible
N1W3, P1W3		F. ANDRIEU

Brief description of the scribe

Standard isolated multi-fin N and pMOS with various gate widths at L=10µm.

Device list

#	*Device type **	*Parameters*
1	Standard Nmos or Pmos	W=0.08µm, L=10µm, Orientation=0°, 50 channel
2	Standard Nmos or Pmos	W=0.1µm, L=10µm, Orientation=0°, 50 channel
3	Standard Nmos or Pmos	W=0.25µm, L=10µm, Orientation=0°, 50 channel
4	Standard Nmos or Pmos	W=0.35µm, L=10µm, Orientation=0°, 50 channel
5	Standard Nmos or Pmos	W=0.5µm, L=10µm, Orientation=0°, 50 channel
6	Standard Nmos or Pmos	W=1µm, L=10µm, Orientation=0°, 50 channel
7		

*: as defined in the DRM for transistors and gated diodes

Scribe pads structure

☑ Standard (22 pads) ☐ No pads ☐ Other choice (user defined)

Testing levels

☐ Active ☐ Poly1/Poly2 ☑ Metal 1 ☐ Metal 2

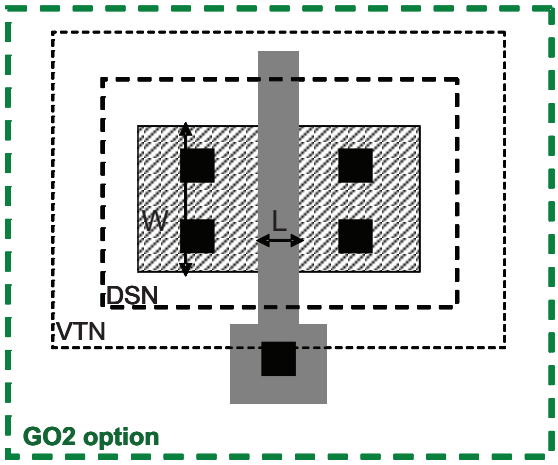
Number of module spaces reserved for the scribe

Above pads line 0 Below pads line 0

Pads assignment

Pad	*Connection*	*Pad*	*Connection*
1	Source of device 1	12	Gate of device 4
2	Drain of device 1	13	Source of device 5
3	Gate of device 1	14	Drain of device 5
4	Source of device 2	15	Gate of device 5
5	Drain of device 2	16	Source of device 6
6	Gate of device 2	17	Drain of device 6
7	Source of device 3	18	Gate of device 6
8	Drain of device 3	22	
9	Gate of device 3		
10	Source of device 4		
11	Drain of device 4		

Device description



Drawing of nMOSFET

MUST RETICLE DESCRIPTION

Scribe name	Coordinates	Responsible
N1G3, P1G3		F. ANDRIEU

Brief description of the scribe

GO2 Isolated standard nMOS or pMOS with various gate lengths at W=10µm.

Device list

#	*Device type **	*Parameters*
1	Standard GO2 Nmos or Pmos	W=10µm, L=0.15µm, Orientation=0°, 1 channel
2	Standard GO2 Nmos or Pmos	W=10µm, L=0.25µm, Orientation=0°, 1 channel
3	Standard GO2 Nmos or Pmos	W=10µm, L=0.35µm, Orientation=0°, 1 channel
4	Standard GO2 Nmos or Pmos	W=10µm, L=0.5µm, Orientation=0°, 1 channel
5	Standard GO2 Nmos or Pmos	W=10µm, L=0.75µm, Orientation=0°, 1 channel
6	Standard GO2 Nmos or Pmos	W=10µm, L=1µm, Orientation=0°, 1 channel
7	Standard GO2 Nmos or Pmos	W=10µm, L=10µm, Orientation=0°, 1 channel

*: as defined in the DRM for transistors and gated diodes

Scribe pads structure

☑ Standard (22 pads) ☐ No pads ☐ Other choice (user defined)

Testing levels

☐ Active ☐ Poly1/Poly2 ☑ Metal 1 ☐ Metal 2

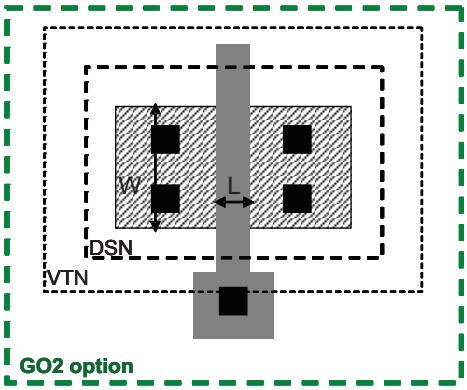
Number of module spaces reserved for the scribe

Above pads line 0 Below pads line 0

Pads assignment

Pad	*Connection*	*Pad*	*Connection*
1	Source of device 1	12	Gate of device 4
2	Drain of device 1	13	Source of device 5
3	Gate of device 1	14	Drain of device 5
4	Source of device 2	15	Gate of device 5
5	Drain of device 2	16	Source of device 6
6	Gate of device 2	17	Drain of device 6
7	Source of device 3	18	Gate of device 6
8	Drain of device 3	19	Source of device 7
9	Gate of device 3	20	Drain of device 7
10	Source of device 4	21	Gate of device 7
11	Drain of device 4	22	

Device description



Drawing of nMOSFET

Milestone 2.4: First run of gated resistors delivered to partners

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Nanowire (NW) and Tri-gated Complementary Metal Oxide Semiconductor (CMOS) technology appear as an attractive option to overcome standard CMOS bulk technology limits in terms of scaling, performances and power consumption. The electrostatic control over the channel is indeed improved in NWs, leading to a significant reduction of short channel effects and thus leakage currents in the OFF state. Based on existing expertise in fabrication of FD-SOI nanowire devices, we develop in this work a fabrication route for n-channel and p-channel *junctionless* nanowire MOSFET transistors. Existing mask set is used, with the exception of the active area level which is redrawn. The FD-SOI route is adapted in order to target *junctionless* NW with width varying from $10\text{nm} \leq W \leq 20\text{nm}$, silicon thickness T_{SOI}=10nm and with a gate length $L_G < 30\text{nm}$.

I. INTRODUCTION

This work demonstrates *junctionless* transistors fully compatible with standard trigate fabrication process, and a single high-κ/metal gate stack. In particular, we demonstrate V_T tuning capabilities with a mid-gap metal gate, by using ion implanted thin SOI channel. We investigate the structure scalability down to 20nm and we evaluate transport and noise properties of *junctionless* nanowire transistors.

II. PROCESS DESCRIPTION

Silicon-on-Insulator (SOI) structures with silicon layers of 10 nm in thickness are used. The key for the fabrication of *junctionless* gated resistor is the formation of a semiconductor layer that is thin and narrow enough to allow full depletion of carriers when the device is turned off. Then, the silicon layer is thinned down to 10nm. The semiconductor also needs to be heavily doped to allow for a reasonable amount of current flow when the device is turned on. The implant energies and doses are chosen (from process simulation – Athena Silvaco) to yield uniform doping concentration ranging from $5x10^{18}$ cm^{-3} up to $5x10^{19}$ cm^{-3}. Then, the silicon layer is patterned to create the silicon nanowires by a mesa isolation technique. The active stack used in this work is consisted of a 10nm doped Si, 2.5nm SiO_2 dielectric layer and an organic bottom anti-reflective coating (BARC) layer of around 24nm patterned using 193nm ArF resist. The BARC opening is done using CF_4 chemistry. This chemistry is used in order to ensure vertical resist/BARC profile and correct linewidth roughness. Then, the BARC/resist trimming process is performed just before the main etch to selectively pattern the silicon on the buried oxide. Trimming resist is performed to achieve nanowire structures as small as 15nm in width using the HBr/O_2 plasma. In order to smooth the resist patterns and then reduce the linewidth roughness, a curing step will be performed just before the trimming.

II. RESULTS

In order to know the dimensions of the *junctionless* nanowires, different scribes are measured: scribes N1T and N1W3. The N1T scribe is used to extract the Ion-Ioff plot, the DIBL, the sub-threshold slope, the threshold voltage, (etc.) for different gate lengths. The scribe N1W3 is used in order to extract capacitance and carrier mobility. The dimensions for the different patterned wafers are summarized below.

		N1T-1	N1T-2	N1T-3	N1T-4	N1T-5	N1T-6	N1T-7	N1W3-1	N1W3-2	N1W3-3	N1W3-4	N1W3-5	N1W3-6
P01	H (µm)	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01
	W Min (µm)	0,015	0,015	0,015	0,015	0,015	0,015	0,015	0,008	0,028	0,178	0,27	0,428	0,928
	W Mean (µm)	0,019	0,019	0,019	0,019	0,019	0,019	0,019	0,01	0,03	0,18	0,27	0,43	0,93
	W Max (µm)	0,022	0,022	0,022	0,022	0,022	0,022	0,022	0,015	0,035	0,185	0,27	0,435	0,935
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P02	H (µm)	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01
	W Min (µm)	0,021	0,021	0,021	0,021	0,021	0,021	0,021	0,017	0,037	0,187	0,287	0,437	0,937
	W Mean (µm)	0,025	0,025	0,025	0,025	0,025	0,025	0,025	0,02	0,04	0,19	0,29	0,44	0,94
	W Max (µm)	0,029	0,029	0,029	0,029	0,029	0,029	0,029	0,022	0,042	0,192	0,292	0,442	0,942
	Lg (µm)	0,025	0,035	0,045	0,055	0,065	0,075	0,095	10	10	10	10	10	10
P03	H (µm)	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01
	W Min (µm)	0,013	0,013	0,013	0,013	0,013	0,013	0,013	0,007	0,027	0,177	0,277	0,427	0,927
	W Mean (µm)	0,017	0,017	0,017	0,017	0,017	0,017	0,017	0,008	0,028	0,178	0,278	0,428	0,928
	W Max (µm)	0,023	0,023	0,023	0,023	0,023	0,023	0,023	0,01	0,03	0,18	0,28	0,43	0,93
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P04	H (µm)	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01
	W Min (µm)	0,021	0,021	0,021	0,021	0,021	0,021	0,021	0,016	0,036	0,186	0,286	0,436	0,936
	W Mean (µm)	0,024	0,024	0,024	0,024	0,024	0,024	0,024	0,018	0,038	0,188	0,288	0,438	0,938
	W Max (µm)	0,026	0,026	0,026	0,026	0,026	0,026	0,026	0,021	0,041	0,191	0,291	0,441	0,941
	Lg (µm)	0,027	0,037	0,047	0,057	0,067	0,077	0,097	10	10	10	10	10	10
P05	H (µm)	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009
	W Min (µm)	0,022	0,022	0,022	0,022	0,022	0,022	0,022	0,009	0,029	0,179	0,279	0,429	0,929
	W Mean (µm)	0,025	0,025	0,025	0,025	0,025	0,025	0,025	0,012	0,032	0,182	0,282	0,432	0,932
	W Max (µm)	0,028	0,028	0,028	0,028	0,028	0,028	0,028	0,014	0,034	0,184	0,284	0,434	0,934
	Lg (µm)	0,018	0,028	0,038	0,048	0,058	0,068	0,088	10	10	10	10	10	10
P06	H (µm)	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009
	W Min (µm)	0,007	0,007	0,007	0,007	0,007	0,007	0,007	too small	0,018	0,168	0,268	0,418	0,918
	W Mean (µm)	0,01	0,01	0,01	0,01	0,01	0,01	0,01	too small	0,021	0,171	0,271	0,421	0,921
	W Max (µm)	0,015	0,015	0,015	0,015	0,015	0,015	0,015	too small	0,022	0,172	0,272	0,422	0,922
	Lg (µm)	0,022	0,032	0,042	0,052	0,062	0,072	0,092	10	10	10	10	10	10
P07	H (µm)	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009
	W Min (µm)	0,026	0,026	0,026	0,026	0,026	0,026	0,026	0,015	0,035	0,185	0,285	0,435	0,935
	W Mean (µm)	0,029	0,029	0,029	0,029	0,029	0,029	0,029	0,017	0,037	0,187	0,287	0,437	0,937
	W Max (µm)	0,032	0,032	0,032	0,032	0,032	0,032	0,032	0,018	0,038	0,188	0,288	0,438	0,938
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P08	H (µm)	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009
	W Min (µm)	0,008	0,008	0,008	0,008	0,008	0,008	0,008	too small	0,02	0,17	0,27	0,42	0,92
	W Mean (µm)	0,013	0,013	0,013	0,013	0,013	0,013	0,013	too small	0,022	0,172	0,272	0,422	0,922
	W Max (µm)	0,019	0,019	0,019	0,019	0,019	0,019	0,019	too small	0,024	0,174	0,274	0,424	0,924
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P09	H (µm)	0,0085	0,0085	0,0085	0,0085	0,0085	0,0085	0,0085	0,0085	0,0085	0,0085	0,0085	0,0085	0,0085
	W Min (µm)	0,021	0,021	0,021	0,021	0,021	0,021	0,021	0,01	0,03	0,18	0,28	0,43	0,93
	W Mean (µm)	0,025	0,025	0,025	0,025	0,025	0,025	0,025	0,013	0,033	0,183	0,283	0,433	0,933
	W Max (µm)	0,029	0,029	0,029	0,029	0,029	0,029	0,029	0,016	0,036	0,186	0,286	0,436	0,936
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10
P10	H (µm)	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009
	W Min (µm)	0,009	0,009	0,009	0,009	0,009	0,009	0,009	too small	0,018	0,168	0,268	0,418	0,918
	W Mean (µm)	0,013	0,013	0,013	0,013	0,013	0,013	0,013	too small	0,021	0,171	0,271	0,421	0,921
	W Max (µm)	0,015	0,015	0,015	0,015	0,015	0,015	0,015	too small	0,023	0,173	0,273	0,423	0,923
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10

P11	H (µm)	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009	0,009
	W Min (nm)	0,021	0,021	0,021	0,021	0,021	0,021	0,021	0,011	0,031	0,181	0,281	0,431	0,931
	W Mean (µm)	0,026	0,026	0,026	0,026	0,026	0,026	0,026	0,014	0,034	0,184	0,284	0,434	0,934
	W Max (nm)	0,028	0,028	0,028	0,028	0,028	0,028	0,028	0,016	0,036	0,186	0,286	0,436	0,936
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10

P12	H (µm)	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01
	W Min (µm)	0,009	0,009	0,009	0,009	0,009	0,009	0,009	too small	0,021	0,171	0,271	0,421	0,921
	W Mean (µm)	0,013	0,013	0,013	0,013	0,013	0,013	0,013	too small	0,023	0,173	0,273	0,423	0,923
	W Max (µm)	0,017	0,017	0,017	0,017	0,017	0,017	0,017	too small	0,024	0,174	0,274	0,424	0,924
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10

P13	H (µm)	0,0095	0,0095	0,0095	0,0095	0,0095	0,0095	0,0095	0,0095	0,0095	0,0095	0,0095	0,0095	0,0095
	W Min (µm)	0,024	0,024	0,024	0,024	0,024	0,024	0,024	0,008	0,028	0,178	0,278	0,428	0,928
	W Mean (µm)	0,026	0,026	0,026	0,026	0,026	0,026	0,026	0,014	0,034	0,184	0,284	0,434	0,934
	W Max (µm)	0,028	0,028	0,028	0,028	0,028	0,028	0,028	0,017	0,037	0,187	0,287	0,437	0,937
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10

P14	H (µm)	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01
	W Min (µm)	0,008	0,008	0,008	0,008	0,008	0,008	0,008	too small	0,021	0,171	0,271	0,421	0,921
	W Mean (µm)	0,013	0,013	0,013	0,013	0,013	0,013	0,013	too small	0,023	0,173	0,273	0,423	0,923
	W Max (µm)	0,016	0,016	0,016	0,016	0,016	0,016	0,016	too small	0,025	0,175	0,275	0,425	0,925
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10

P15	H (µm)	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01
	W Min (µm)	0,023	0,023	0,023	0,023	0,023	0,023	0,023	0,011	0,031	0,181	0,281	0,431	0,931
	W Mean (µm)	0,028	0,028	0,028	0,028	0,028	0,028	0,028	0,015	0,035	0,185	0,285	0,435	0,935
	W Max (µm)	0,03	0,03	0,03	0,03	0,03	0,03	0,03	0,019	0,039	0,189	0,289	0,439	0,939
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10

P16	H (µm)	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01	0,01
	W Min (µm)	0,009	0,009	0,009	0,009	0,009	0,009	0,009	too small	0,021	0,171	0,271	0,421	0,921
	W Mean (µm)	0,014	0,014	0,014	0,014	0,014	0,014	0,014	too small	0,024	0,174	0,274	0,424	0,924
	W Max (µm)	0,017	0,017	0,017	0,017	0,017	0,017	0,017	too small	0,026	0,176	0,276	0,426	0,926
	Lg (µm)	0,02	0,03	0,04	0,05	0,06	0,07	0,09	10	10	10	10	10	10

This is the doping targeted for the wafers:

#P01: NMOS ($10^{19}cm^{-3}$)
#P02: PMOS ($10^{19}cm^{-3}$)
#P03: NMOS ($5\times10^{18}cm^{-3}$)
#P04: PMOS ($5\times10^{18}cm^{-3}$)
#P05: NMOS ($10^{19}cm^{-3}$)
#P06: NMOS ($10^{19}cm^{-3}$)
#P07: NMOS ($2\times10^{19}cm^{-3}$)
#P08: NMOS ($2\times10^{19}cm^{-3}$)
#P09: NMOS ($4\text{-}5\times10^{19}cm^{-3}$)
#P10: NMOS ($4\text{-}5\times10^{19}cm^{-3}$)
#P11: PMOS ($10^{19}cm^{-3}$)
#P12: PMOS ($10^{19}cm^{-3}$)
#P13: PMOS ($2\times10^{19}cm^{-3}$)
#P14: PMOS ($2\times10^{19}cm^{-3}$)
#P15: PMOS ($4\text{-}5\times10^{19}cm^{-3}$)
#P16: PMOS ($4\text{-}5\times10^{19}cm^{-3}$)

All the critical dimension (CD) measurements (after photolithography and after active patterning) are done using in-line field-emission-scanning electron microscope (SEM). The gate stack is composed of high-κ/metal gate. 2.3nm chemical vapour deposition (CVD) HfSiON with 5nm ALD TiN and Poly-Silicon (50nm) layers are deposited. This corresponds to an equivalent oxide thickness (EOT) of around 1.2nm. A HRTEM picture of the nanowire cross-section has been performed in order to reveal the good conformal gate stack deposition surrounding the nanowire and to evaluate the nanowire width. Fig. 1 shows a cross-sectional TEM micrograph of a conventional triple-gate silicon nanowire with high-k/metal gate stack (isolated devices).

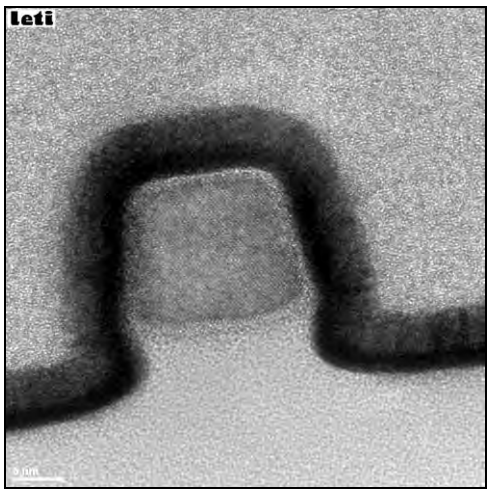

Figure 1: TEM cross-section showing a 14nm×14nm Trigate silicon nanowire with 2.3nm HfSiON/5nm TiN gate stack.

The measured I_{DS}-V_{GS} (Fig. 2) characteristics for N/P *junctionless* trigate with L=30nm, show well-behaved characteristics with DIBL lower than 30mV/V for NMOS. A good electrostatic integrity for NW is verified.

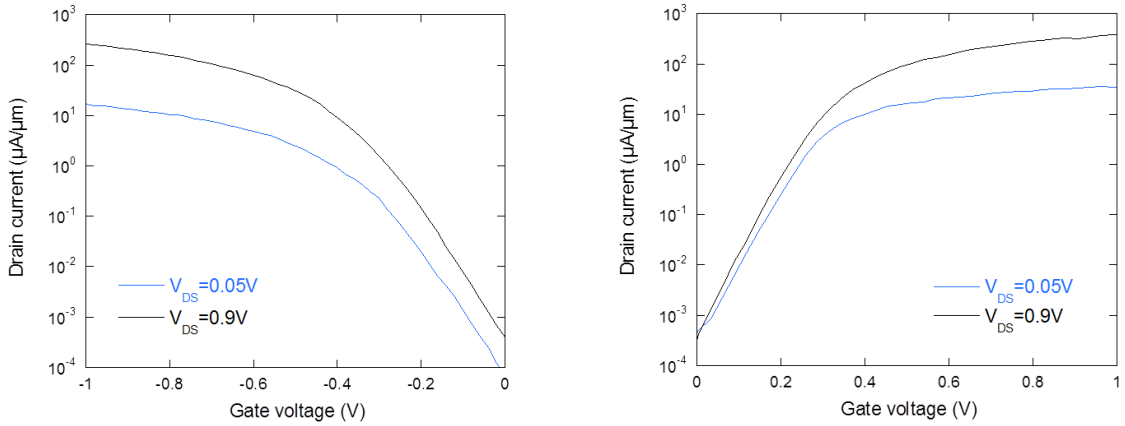

Figure 2: I_{DS}-V_{GS} characteristics for PMOS (a) (Ion=206 µA/µm @ V_{GS}=V_{DS}=-0.9V Ioff=0.38nA/µm @ V_{GS}=0V and V_{DS}=0.9V SS=75mV/dec) and for NMOS (b) (Ion=280 µA/µm @ V_{GS}=V_{DS}=0.9V Ioff=0.36nA/µm @ V_{GS}=0V and V_{DS}=0.9V SS=60mV/dec).

Figure 3 shows the I_{DS}-V_{GS} characteristics for NMOS *junctionless* trigate with L=100nm. Various doping are used.

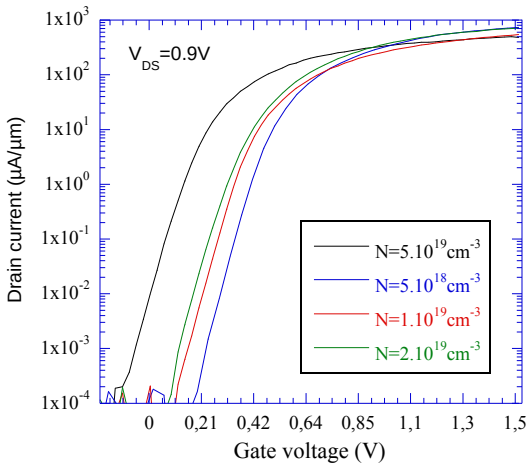

Figure 3: I_{DS}-V_{GS} characteristics for NMOS extracted at V_{DS}=0.9V for junction trigate nanowire (W~18nm) and channel doping varying from $5\times10^{19}cm^{-3}$ down to $5\times10^{19}cm^{-3}$. Lg=100nm.

The subthreshold slope and DIBL are shown in figure 4 and 5.

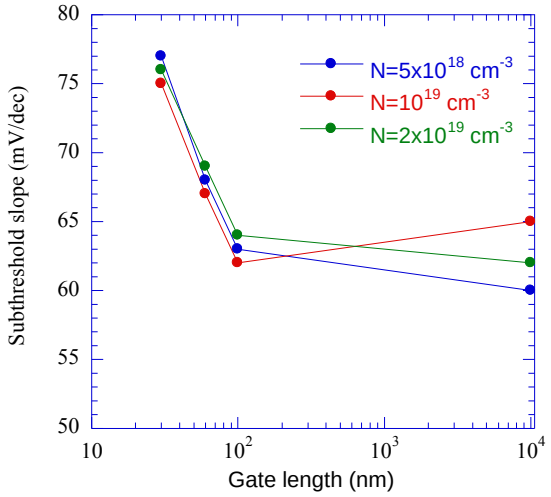

Figure 4: Subthreshold slope (SS) as a function of the gate length for *junctionless* Trigate-NW (NMOSFET)

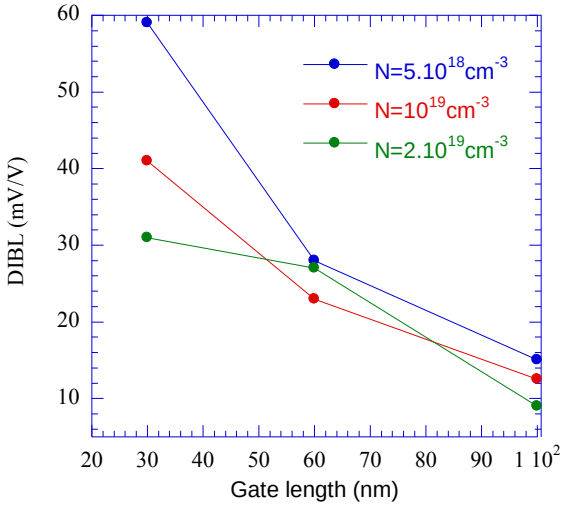

Figure 5: DIBL as a function of the gate length for *junctionless* Trigate-NW (NMOSFET)

By taking into consideration the better electrostatic control on the channel for junctionless Trigate NW, SS and DIBL are strongly reduced for the smallest gate lengths. The DIBL is improved when the channel doping is increased. Short channel effects (SCE) immunity is clearly evidenced.

III. FIRST WAFER DELIVERED TO PARTNERS

First wafer has been send to partners (IMEP) in order to characterize noise in junctionless trigate devices. Figure 6 shows the noise measurement. The noise measurement follows carrier fluctuations model and reveals trap density levels comparable to wide planar

device. The degraded subthreshold slope observed on PMOS probably comes from this higher trap density.

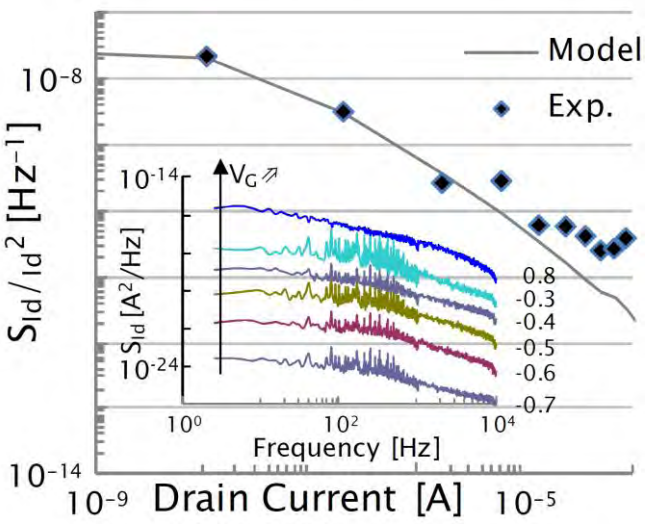

Figure 6: Fit of noise spectrum with trapping model. Lg=40nm, W=10µm. Inset: noise level versus frequency.

IV. CONCLUSION

The first junctionless trigated nanowires have been fabricated and characterized. The On-current of measured junctionless transistors seems to be mainly limited by a lower mobility compared to the inversion-mode devices. However, interesting features are their tunable threshold voltage, low noise with control trap density and good scalability.

Project Technical Report

Project: EU FP7 SQWIRE
Reporting period: 2010-09-01 – 2011-08-31

Work Package 2

Contributions from Soitec.

Progress

Soitec has worked on the improvement of the thickness uniformity of 300 SOI wafers with a silicon film thickness of less than 20 nm.

During first 12 month of the Project major efforts have been dedicated to the development of 300 mm wafers with a thin top layer of Si (< 20 nm) and with the BOX thickness < 30 nm. The focus, in close collaboration with LETI, was on the tight thickness control. The figures below for the wafers with BOX = 25 nm illustrate the progress made by Soitec on this path.

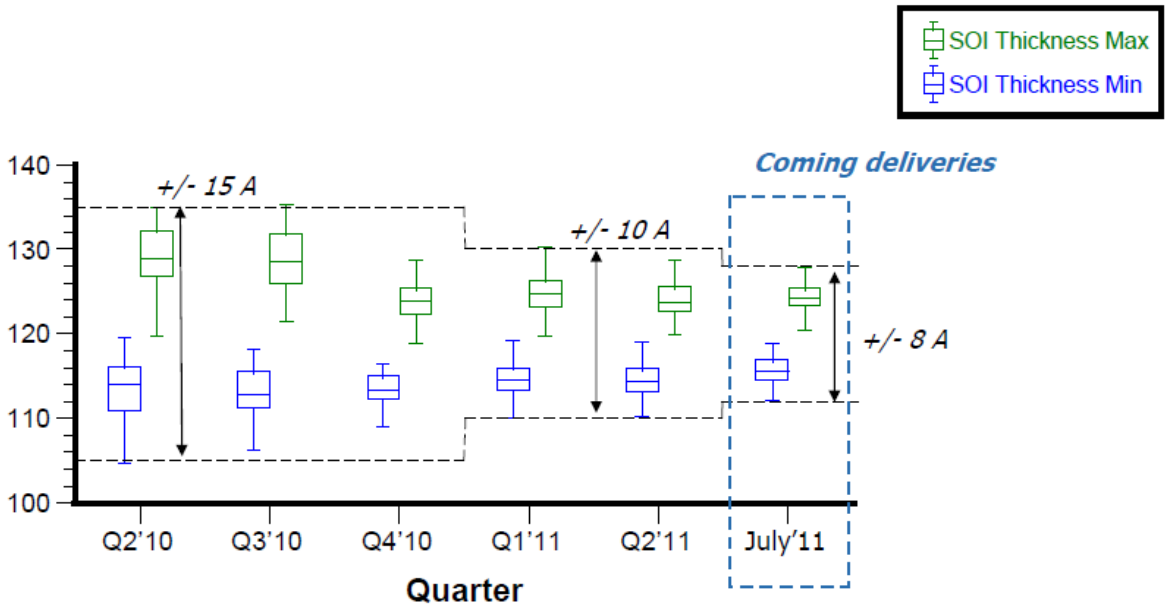

Figure 1: UTBOX25 update: Total SOI thickness variation.

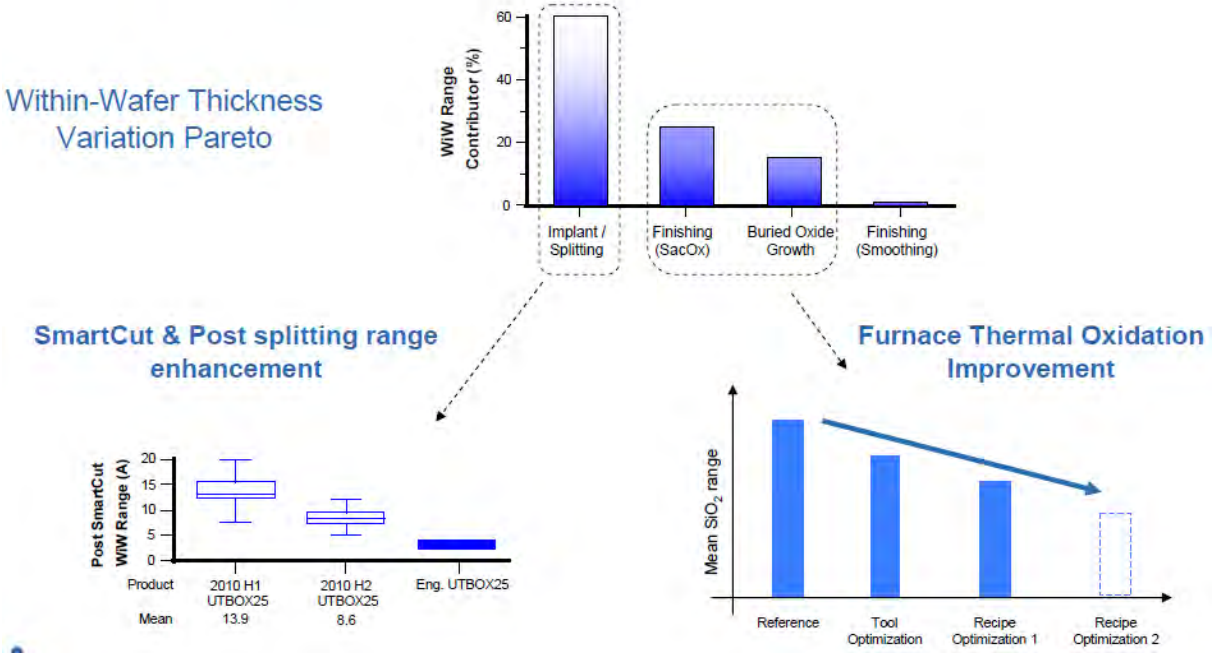

Figure 2: UTBOX25 SOI Thickness control improvement.

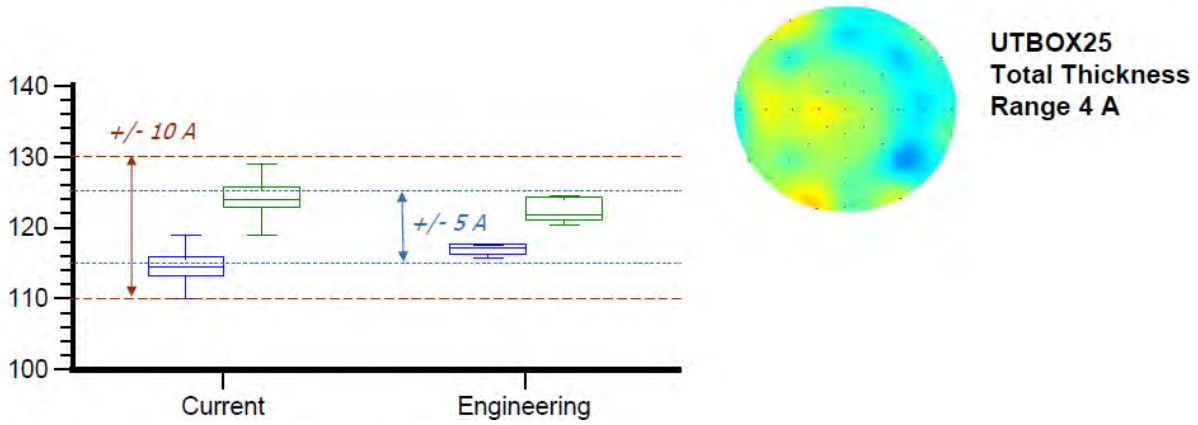

Figure 3: UTBOX25 SOI thickness control demonstration.

Before the start of SQWIRE project Soitec WP2 partner LETI has already established a nanowire transistor fabrication process flow for the SOI wafers with the BOX thickness of 145 nm. Therefore the first lot of 12 wafers delivered to LETI for the device fabrication in December 2010 has had top Si thickness of 12 nm and BOX thickness of 145 nm. A thinning of these wafers to 10 nm has been done at LETI clean room during fabrication of junctionless devices. The thickness of the top Si layer has been verified by XTEM and spectroscopic ellipsometry. A delivery of the second batch of 24 wafers to LETI is scheduled in the first week of October 2011.

Summary

A path to ± 2 Å variation for thickness control has been identified and will be implemented before end of 2011. The work to improve the total thickness variation of the top Si layer will continue.

Industrial Exploitation of Project Results/ Information Sharing

The following paper was published in the beginning of May 2011:

W. Schwarzenbach, X. Cauchy, O. Bonnin, N. Daval, C. Aulnette, C. Girard, B.-Y. Nguyen & C. Maleville “Ultra-thin film SOI/BOX substrate development, its application and readiness”, ECS Transactions, 35 (5) 239-245 (2011)The representative publications at

Laboratoire d'électronique et de technologie de l'information
Direction de la recherche technologique
Département NaNoTec

RAPPORT TECHNIQUE
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Deliverable 2.2: SQWIRE – Silicon Quantum Wire Transistors Fabrication Process Specification for *junctionless* MOSFET

Projet / Project: SQWIRE N/Réf : D2NT/10.615/SB

	Nom / Fonction – Name / Function	*Date*	*Visa*
Auteur(s) : Author(s)	*Sylvain Barraud* *Tél : 04-38-78-98-45*	*November 23th, 2010*	
Approbateur : Assentor	*Olivier Faynot*	*November 23th, 2010*	

Diffusion :

Archivage GED / Filing ☐ Fiche GED

Abstract

Nanowire (NW) and Tri-gated Complementary Metal Oxide Semiconductor (CMOS) technology appear as an attractive option to overcome standard CMOS bulk technology limits in terms of scaling, performances and power consumption [1-3]. The electrostatic control over the channel is indeed improved in NWs, leading to a significant reduction of short channel effects [4] and thus leakage currents in the OFF state.

Based on existing expertise in fabrication of FD-SOI nanowire devices, we will develop a fabrication route for n-channel and p-channel *junctionless* nanowire MOSFET transistor. Existing mask set will be used, with the exception of the active area level which will have to be redrawn. The FD-SOI route will be adapted in order to target *junctionless* NW with width varying from $10nm \leq W \leq 20nm$, silicon thickness T_{SOI}=10nm and with a gate length $L_G < 30nm$.

Those original devices have demonstrated near-ideal subthreshold slope, extremely low leakage current and less degradation of mobility with gate voltage and temperature than conventional transistors [5].

SQWIRE

INSTITUT CARNOT CEA LETI

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I. INTRODUCTION

The silicon nanowire field-effect transistor is one of the promising candidates for future ultra-scaled CMOS technology. It offers the best gate electrostatic control on short-channel-effects. The formation of ultra-shallow junctions is a limiting factor to scale and puts severe constraints on the processing thermal budget. Ultra-short-time annealing techniques are being employed to eliminate thermal diffusion of the source and drain doping impurities, but even the lateral impurity spread due to ion implantation itself is starting to cause problems. In addition to the difficulty of forming ultra-sharp junctions, random impurity fluctuations from source and drain dopants scattered in the channel region cause variability problems.

Here, a new type of transistor is investigated in which there are no junctions and no doping concentration gradients. These devices have full CMOS functionality and are made using Tri-gated silicon nanowires. Those original devices have demonstrated near-ideal subthreshold slope, extremely low leakage current and less degradation of mobility with gate voltage and temperature than conventional transistors [5].

The objective of this task (D2.2) is to propose an integration scheme and fabrication process specifications for *junctionless* Tri-gated MOSFET transistors on 300 mm wafers based on an adapted route from FD-SOI MOSFET devices developed at CEA-Leti.
First of all, the integration strategy used for the elaboration of *junctionless* tri-gated nanowire transistor is presented.

II. JUNCTIONLESS TRANSISTORS

The main difference between conventional and junctionless MOSFET transistors is that the channel doping is similar to the source-drain doping.

II.1. NANOWIRE ELABORATION ON 300 MM WAFERS FROM DUV193NM LITHOGRAPHY

Silicon-on-Insulator (SOI) structures with silicon layers of 12 nm in thickness are used. The key for the fabrication of junctionless gated resistor is the formation of a semiconductor layer that is

thin and narrow enough to allow full depletion of carriers when the device is turned off [7]. Then, **the silicon layer will be thinned down to 10nm**. The semiconductor also needs to be heavily doped to allow for a reasonable amount of current flow when the device is turned on. The implant energies and doses will be chosen (from process simulation – Athena Silvaco) to yield uniform **doping concentration ranging from $5x10^{18}$ cm^{-3} up to $5x10^{19}$ cm^{-3}**. Then, the silicon layer will be patterned to create the silicon nanowires by a mesa isolation technique. The active stack used in this work will be consisted of a 10nm doped Si, 2.5nm SiO_2 dielectric layer and an organic bottom anti-reflective coating (BARC) layer of around 24nm patterned using 193nm ArF resist. The thickness of the photoresist is around 160nm. The active zone (i.e. nanowire feature) will be carried out using the trimmed resist/BARC as a mask. Obviously, the final linewidth of nanowires will be determined mainly by the amount of trimmed resist.

The good electrostatic control being based on low dimensions of nanowire width (or diameter), shorter wavelengths are required for lithography. As a result, an alternative method to *e-beam* lithography is proposed in this study to achieve sub-15nm nanowire width in order to lower the manufacturing cost and shorten the development time.

Today's most advanced lithography uses 193nm wave-length for the production of integrated circuits devices. Following the same philosophy than for the gate patterning, we proposed to develop an approach based on resist trimming by dry plasma etching to elaborate our silicon nanowires. This approach has the advantage of reducing the dimensions without increasing the complexity of the lithography requirements. A schematic of the process flow of this trimming method is summarized in Fig. 1. First of all, HBr plasma curing process was performed in order to harden the 193nm ArF resist for better etching resistance. Then, the BARC opening is done using CF_4 chemistry. This chemistry will be used in order to ensure vertical resist/BARC profile and correct linewidth roughness [6]. Moreover, this sequence consuming a lot of photoresist, the thin thickness of the BARC layer is well suited to minimize the resist budget during the process. Then, the BARC/resist trimming process is performed just before the main etch to selectively pattern the silicon on the buried oxide. Trimming resist is performed to achieve nanowire

structures as small as **15nm in width** using the HBr/O_2 plasma. In order to smooth the resist patterns and then reduce the linewidth roughness, a curing step will be performed just before the trimming.

The investigated structures after the photolithography are shown in Fig. 2. They comprised isolated lines (NW) and arrays of lines with long and short dimensions. The arrays of lines with long dimensions will be used to extract the capacitance and the carrier mobility.
All the critical dimension (CD) measurements (after photolithography and after active patterning) will be done using in-line field-emission-scanning electron microscope (SEM).
The linewidth before etching –referred to as developed inspection critical dimension- is around 80nm. After etching, the reduction of the silicon nanowire width induces by the trimming is targeted to 65 nm in order to have nanowire width of around 15nm. Due to the dispersions induce by the photolithography, the NW width after etching is expected to vary between 10nm and 20nm.

I.2. GATE STACK DEPOSITION AND CHANNEL LENGTH

For the first run, the gate stack used will be composed of high-κ/metal gate. 2.3nm chemical vapour deposition (CVD) HfSiON with 5nm CVD TiN and Poly-Silicon (50nm) layers will be deposited. This corresponds to an equivalent oxide thickness (**EOT) of around 1.1nm**.

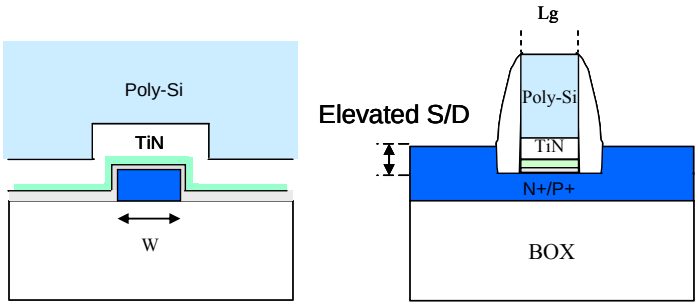
A HRTEM picture of the nanowire cross-section will be performed in order to reveal the good conformal gate stack deposition surrounding the nanowire and to evaluate the nanowire width. Fig. 3 shows a cross-sectional TEM micrograph of a conventional triple-gate silicon nanowire with high-k/metal gate stack (isolated devices).

As for the active patterning, 193nm lithography tool will be used with a resist trimming in order to address **gate lengths down to 25nm**. Firt results obtained on regular Tri-gated nanowire are shown in Fig. 4. Afterwards, a nitride spacer thickness of around 20nm will be formed on the

silicon source-drain. Then, low parasitic resistance will be realized by **epitaxial doped silicon growth on the source-drain (ΔT_{SI}=18nm)**. A schematic process flow is presented in Fig. 5.

For the second run, additional gate stack composed of SiO_2 (2-3nm)/Poly-Si will be processed to compare with high-κ/metal gate stack.

Finally, the main process specifications for the fabrication of junctionless MOSFET are the following:



Width W:	10nm ≤ W ≤ 20nm
Gate length L_g:	20nm ≤ L_g ≤ 10µm
Doping N^+/P^+:	$5\times10^{18}cm^{-3} \leq N \leq 5\times10^{19}cm^{-3}$
Silicon thickness	T_{SOI}=10nm
Gate stack:	0.8nm SiO_2 / 2.3nm HfSiON / 5nm TiN / 50nm Poly-Si
CD spacer:	20nm
Elevated source/drain:	18nm

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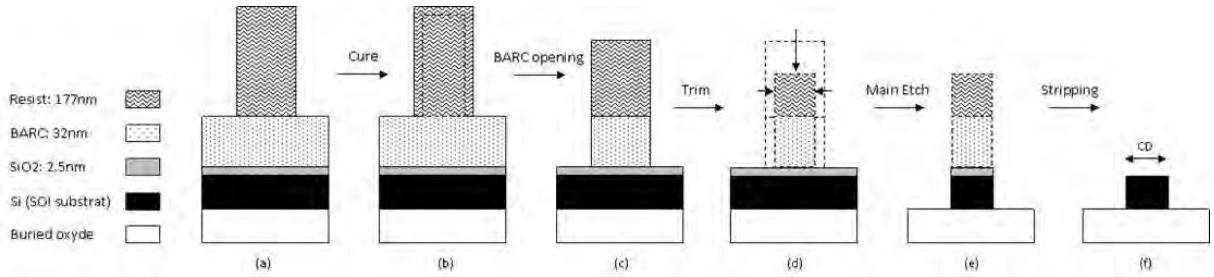

Figure 1: Schematic of the process flow for patterning the silicon nanowire

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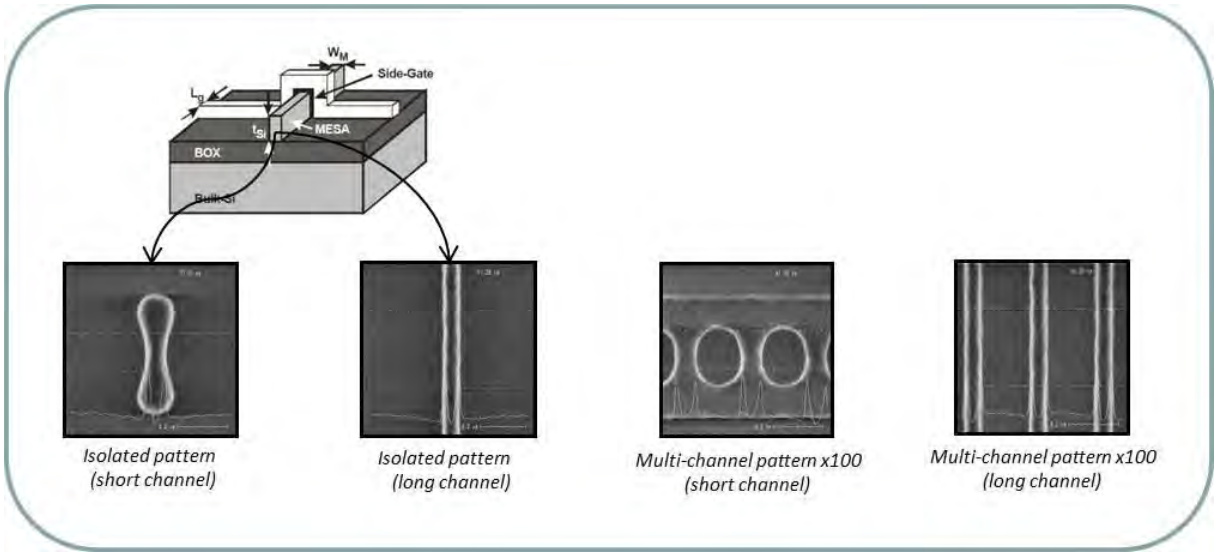

Figure 2: SEM pictures of the devices observed on various chips of the 300mm wafers after the photo-lithography. Long and short isolated devices with long and short arrays of devices (x100 fingers)

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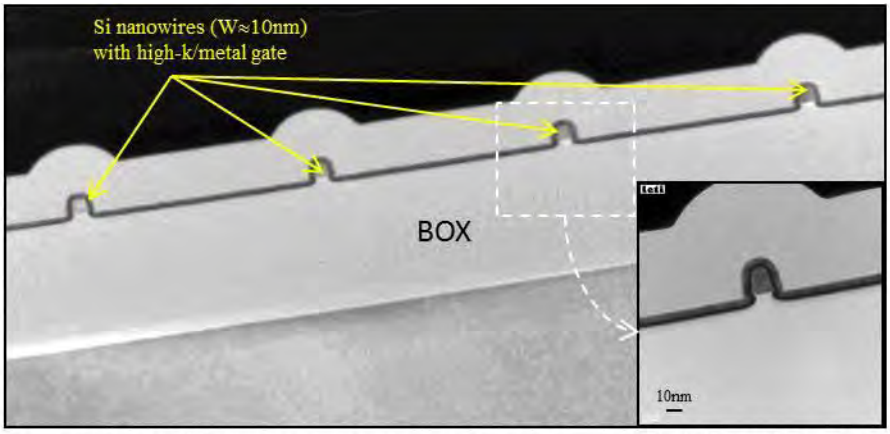

Cross-sectional TEM micrograph of triple-gate silicon nanowire with high-k/metal gate stack

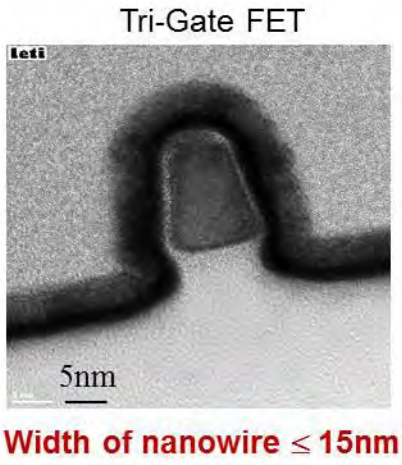

Figure 3: Cross-sectional TEM micrograph of a conventional triple-gate silicon nanowire with high-κ/metal gate stack

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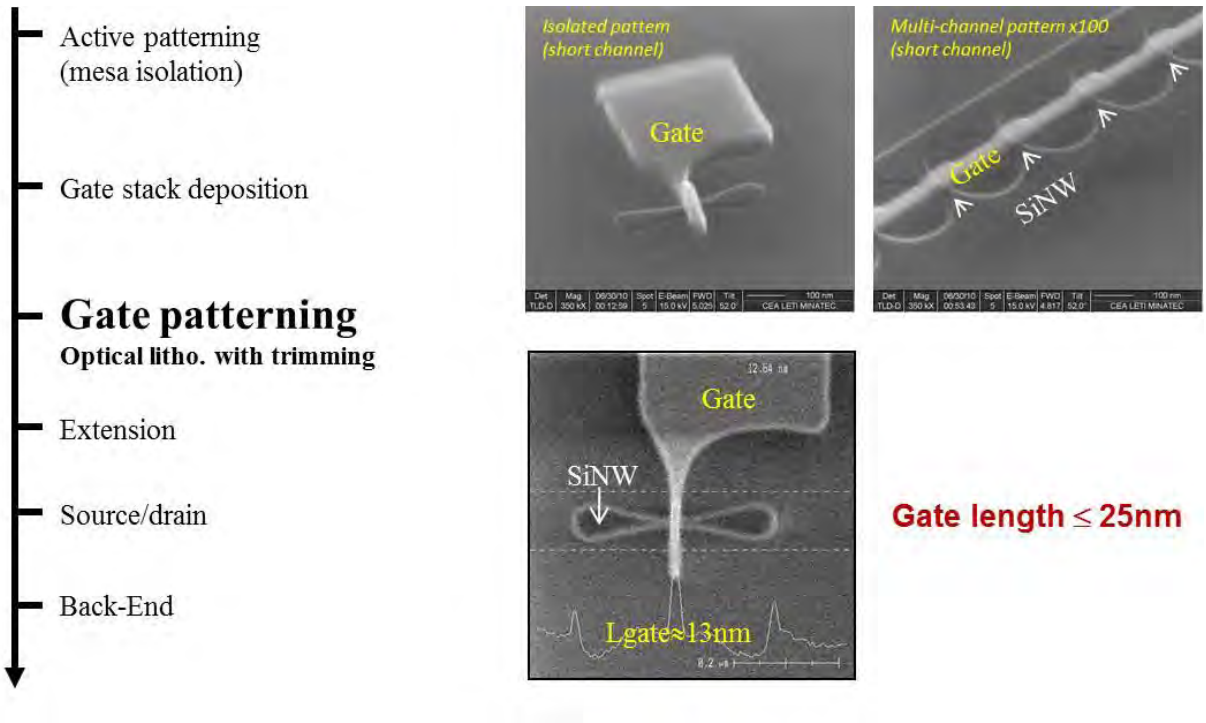

Figure 4: SEM picture of the gate after etching and trimming on regular Tri-gated nanowire transistors. Gate lengths below 25nm are obtained.

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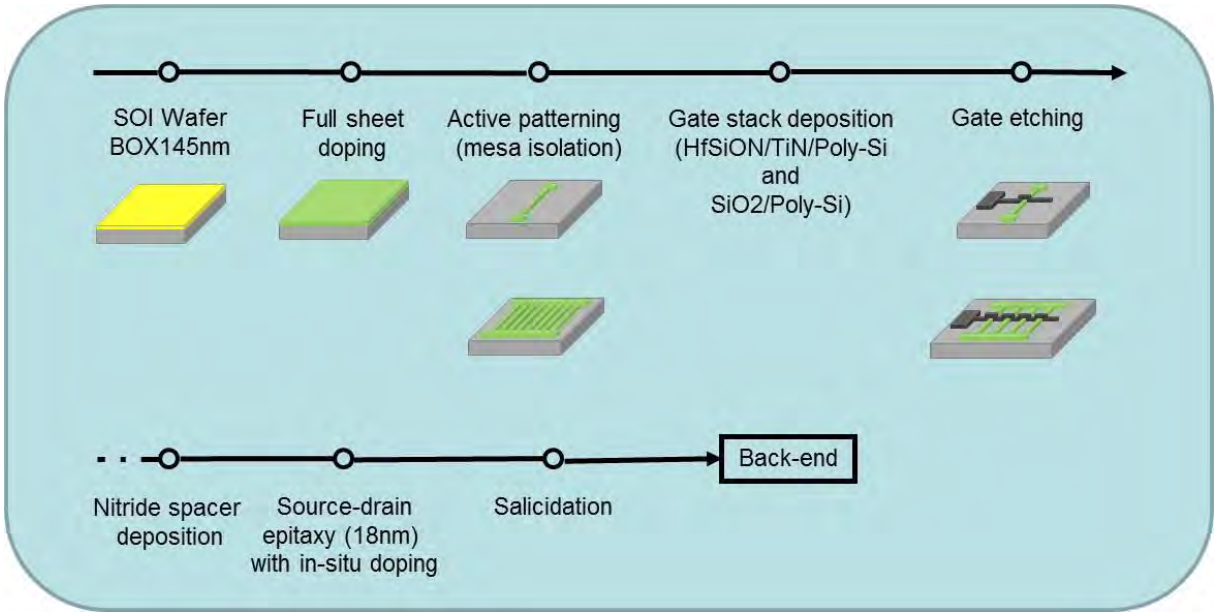

Figure 5: Process Flow chart for the fabrication of *junctionless* nanowire MOSFET devices

Deliverable 2.3: Process Specification for Variable Barrier Transistors

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Nanowire (NW) and Tri-gated Complementary Metal Oxide Semiconductor (CMOS) technology appear as an attractive option to overcome standard CMOS bulk technology limits in terms of scaling, performances and power consumption [1-3]. The electrostatic control over the channel is indeed improved in NWs, leading to a significant reduction of short channel effects [4] and thus leakage currents in the OFF state. Based on existing expertise in fabrication of FD-SOI nanowire devices, we will develop a fabrication route for n-channel and p-channel *Variable Barrier* nanowire transistor. We propose the fabrication of tri-gate nanowire transistors that include soft tunnel barriers which should strongly reduce source-to-drain tunneling and could even, in theory, achieve sub 60 mV/dec subthreshold slopes.

Existing mask set will be used, with the exception of the active area level which will have to be redrawn. The FD-SOI route will be adapted in order to target NW with width varying from $10nm \leq W \leq 20nm$, silicon thickness T_{SOI}=10nm and with a gate length $L_G < 30nm$.

I. INTRODUCTION

Steep subthreshold-slope or small subthreshold-swing devices are of great interest and significance in light of increasing subthreshold leakage current, which constitutes a major concern not only for power dissipation of digital integrated circuits but also for their energy efficiency. With the downscaling of MOSFETs devices, the phenomenon of subthreshold leakage becomes more significant because of short-channel effects and increasing parameter variations [5], as well as strong coupling between temperature and subthreshold leakage current [6]. In conventional MOSFET architectures, the lower limit for the subthreshold slope (*SS*) is $ln(10)\times kT/q$ or ≈60mV/dec at a temperature of 300K. Specifically, it is observed that most of CMOS-based transistors have subthreshold slope higher than 60mV/dec at room temperature for the shorter gate length. It is to note that among these MOSFET devices, the silicon nanowire field-effect transistor is one of the promising candidates for future ultra-scaled CMOS technology because it offers the best gate electrostatic control on short-channel-effects and then the lower subthreshold leakage current. Nevertheless, achieving steeper subthreshold slope transistors remains a key concern for further CMOS downscaling. Indeed, this increase in subthreshold swing as gate length is decreased marks a significant fundamental limitation of conventional FETs. Among the new generations of sub-kT/q transistors, Tunnel-FET devices appears as a promising device due to subthreshold swing smaller than 60 mV/dec and thus low OFF current [7-8]. However, it has also lower ON currents and higher threshold voltages compared with MOSFETs.

In this work, a new type of transistor is investigated. We propose the possibility of achieving sub-*kT/q* subthreshold slope by using a "boosted" CMOS transistor, modified to comprise tunnel barriers near the gate edges. The improvement in subthreshold slope results from a combination of relative motion between channel and tunnel barriers that modulates resonant tunneling states created by the longitudinal (transport direction) confinement in the different potential wells created between the different barriers.

The objective of this task (D2.3) is to propose an integration scheme for the fabrication of n-channel and p-channel *variable barrier transistors* on 300 mm wafers based on an adapted route from Tri-gated nanowire MOSFET devices developed at

CEA-Leti. The only difference being the formation of constrictions in the nanowire at the edges of the gate as illustrated in Fig. 1.

Existing mask sets will be used, with the exception of the active area level which will have to be redrawn. Particular emphasis will be placed on the control and reproducibility of the width of the nanowires as well as both constrictions.

II. OPERATING OF VARIABLE BARRIER TUNNELING TRANSISTOR: A THEORETICAL POINT OF VIEW

Recently, A. Afzalian *et al*. from Tyndall-UCC have demonstrated (using simulations) that the formation of soft tunnel barriers near the source/drain junctions can yield an improvement of subthreshold slope and even break the 60 mV/decade barrier [9-12]. This technique yields perfectly symmetrical MOS transistors.

This novel devices has been investigated using a fast coupled mode-space self-consistent 3D NEGF quantum simulator based on a effective mass Hamiltonian including a non-parabolic correction for the transport. A schematic representation of the simulated rectangular Gate-All-Around nanowire (with constrictions) is represented in Fig. 1.

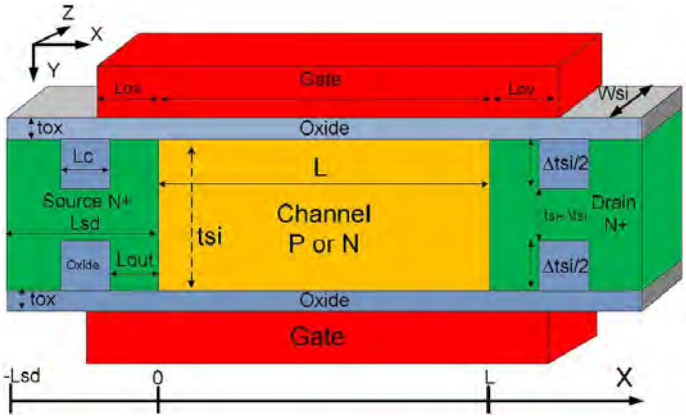


Figure 1: Rectangular GAA SOI nanowire with constrictions. T_{Si}=W=2nm, $L_{channel}$=10nm, L_{sd}=5nm. Data from Ref. [10].

In Fig. 2, the drain current and the s*ubthreshold slope (versus V_{GS})* of devices including tunnel barriers (TBs) with different parameters and different values of *Lout* and *Lov* are shown and compared to those of an identical classical "reference" nanowire transistor without barrier (Tref). Different regimes can be found:

1) The tunnel barrier transistor (TBT) characteristics are identical for a given V_{GS} range to those of Tref (*i.e.* for TBT with *Lout*=1nm and *Lov*=0 and V_{GS}<0.1V).

2) The TBT current is reduced and the *subthreshold slope* can be i) identical, ii) improved and below the *kT/q* limit of 60mV/dec, or iii) degraded. In Fig. 2.A, it is also shown the current ratio, *IR,* as a function of V_{GS} which is a convenient way to assess the impact of subthreshold slope variations on the current.

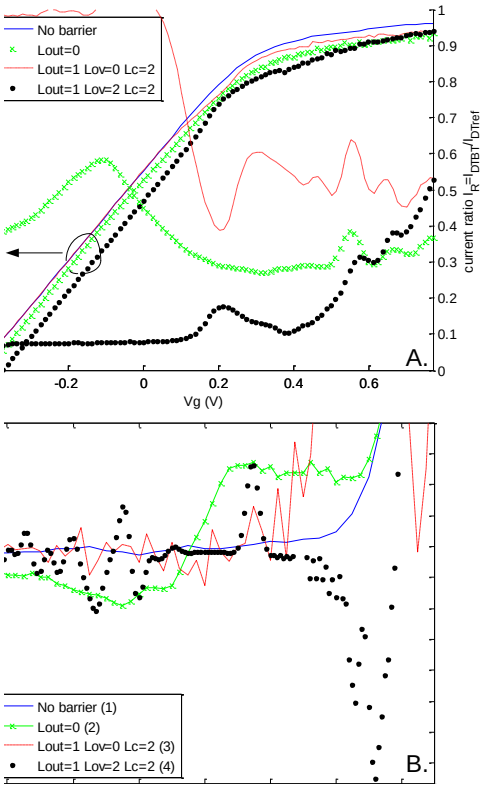


Figure 2: $I_{DS}(V_{GS})$ and $SS(V_{GS})$ curves of the nanowire without (1) and with constrictions with Lout=0, and Lc=1nm TB_S=0.26eV, TB_D=0.46eV (2), L_{out}=1nm, L_C=2nm, TB_S=0.2eV, TB_D=0.36eV L_{ov}=0 (3) and same as (3) but L_{ov}=2nm (4). Vd=1V. L=10nm. Data from Ref. [10]

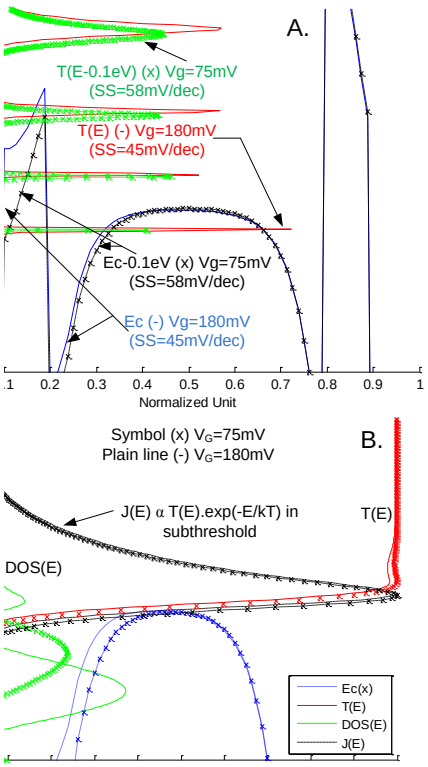


Figure 3: E_C vs. normalized x, and T (non normalized) vs. energy at V_{GS}=75 and 180mV (the curves for V_{GS}=75mV have been shifted down in energy by 102mV for comparison) for A) TBT with Lout=1 and Lov=2nm and B) Tref. In this case, the normalized spectral current density, J(E) is also shown. Data from Ref. [10]

Fig. 3.A shows the conduction band (E_C) and the transmission (T) of the TBT with *Lout*=1nm and *Lov*=2nm at V_{GS}=0.075V, where *SS* is 58mV/dec and at V_{GS}=0.18V where SS=45mV/dec (Fig. 2).

Fig. 3.B shows the same quantity for "standard" nanowire transistor (without barrier). The transmission of the device with constrictions is quite different from that without constrictions and shows very sharp peaks. This is the signature of resonant tunneling

states. When the height of the TBs become typically comparable to that of the channel barrier, they can induce resonant energy states in the quantum wells formed between tunnel-channel and/or tunnel-tunnel barriers. This decreases the current, compared to the reference transistor. In addition, it is explained in [10] that the TBs can locally move differently than the top of the channel barrier through 3D electrostatics effects at the gate edges and mixed influence between gate/source and gate/drain voltages (Fig. 3.A). A change in the relative shape of the wells with V_{GS} (*i.e.* a non translational invariant movement) can induce modifications in energy levels and their broadening (γ) which influence the density of state (DOS), transmission, current, and subthreshold slope. A reduction of *SS* below *kT/q* can be observed by this mean even if the transparency of the TBs decreases relatively compared to the channel barrier because the electron concentration is increasing faster than the Fermi-Dirac distribution of carriers with energy due to the strong non-linear change of DOS (and therefore transmission) with V_{GS}. As a result, one can achieve a lower tunneling probability when the device is turned off than when it is turned on. This increase of barrier transparency with gate voltage makes it possible to improve the subthreshold slope and even to drive it below 60 mV/decade.

This process modification (the local formation of local constrictions) can be applied to "regular" (i.e. *npn*) nanowire transistors. In the next section, the process specifications for variable barrier tunneling are described.

III. PROCESS SPECIFICATION FOR VARIABLE BARRIER TUNNELING TRANSISTOR

The main difference between conventional and variable barrier tunneling MOSFET transistors is the formation of constrictions at the edges of the gate.

III.1. NANOWIRE ELABORATION ON 300 MM WAFERS FROM DUV193NM LITHOGRAPHY

Silicon-on-Insulator (SOI) structures with silicon layers of 12 nm in thickness are used. The key for the fabrication of variable barrier tunneling MOSFET transistors is the formation and the control of both constrictions at the edges of the gate. The silicon layer will be patterned to create the silicon nanowires by a mesa isolation technique. The active stack used in this work will be consisted of a 10nm undoped Si, 2.5nm

SiO_2 dielectric layer and an organic bottom anti-reflective coating (BARC) layer of around 24nm patterned using 193nm ArF resist. The thickness of the photoresist is around 160nm. The active zone (i.e. nanowire feature) will be carried out using the trimmed resist/BARC as a mask. Obviously, the final linewidth of nanowires will be determined mainly by the amount of trimmed resist.

The good electrostatic control being based on low dimensions of nanowire width (or diameter), shorter wavelengths are required for lithography. As a result, an alternative method to *e-beam* lithography is proposed in this study to achieve sub-15nm nanowire width in order to lower the manufacturing cost and shorten the development time.
Today's most advanced lithography uses 193nm wave-length for the production of integrated circuits devices. Following the same philosophy than for the gate patterning, we proposed to develop an approach based on resist trimming by dry plasma etching to elaborate our silicon nanowires. This approach has the advantage of reducing the dimensions without increasing the complexity of the lithography requirements. A schematic of the process flow of this trimming method is summarized in Fig. 4.

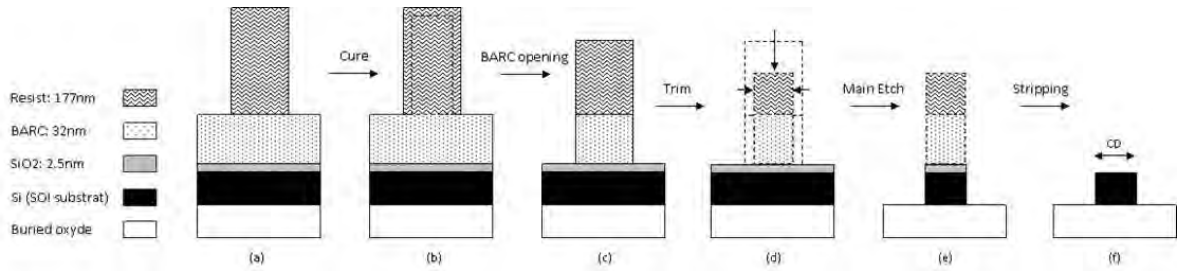


Figure 4: Schematic of the process flow for patterning the silicon nanowire

First of all, HBr plasma curing process was performed in order to harden the 193nm ArF resist for better etching resistance. Then, the BARC opening is done using CF_4 chemistry. This chemistry will be used in order to ensure vertical resist/BARC profile and correct linewidth roughness [13]. Moreover, this sequence consuming a lot of photoresist, the thin thickness of the BARC layer is well suited to minimize the resist budget during the process. Then, the BARC/resist trimming process is performed just before the main etch to selectively pattern the silicon on the buried oxide. Trimming resist is performed to achieve nanowire structures as small as **15nm in width** using the HBr/O_2 plasma. In order to smooth the resist patterns and then reduce the linewidth roughness, a curing step will be performed just before the trimming.

The investigated structures after the photolithography are shown in Fig. 5. They comprised isolated lines (NW) and arrays of lines with long and short dimensions. The arrays of lines with long dimensions will be used to extract the capacitance and the carrier mobility.

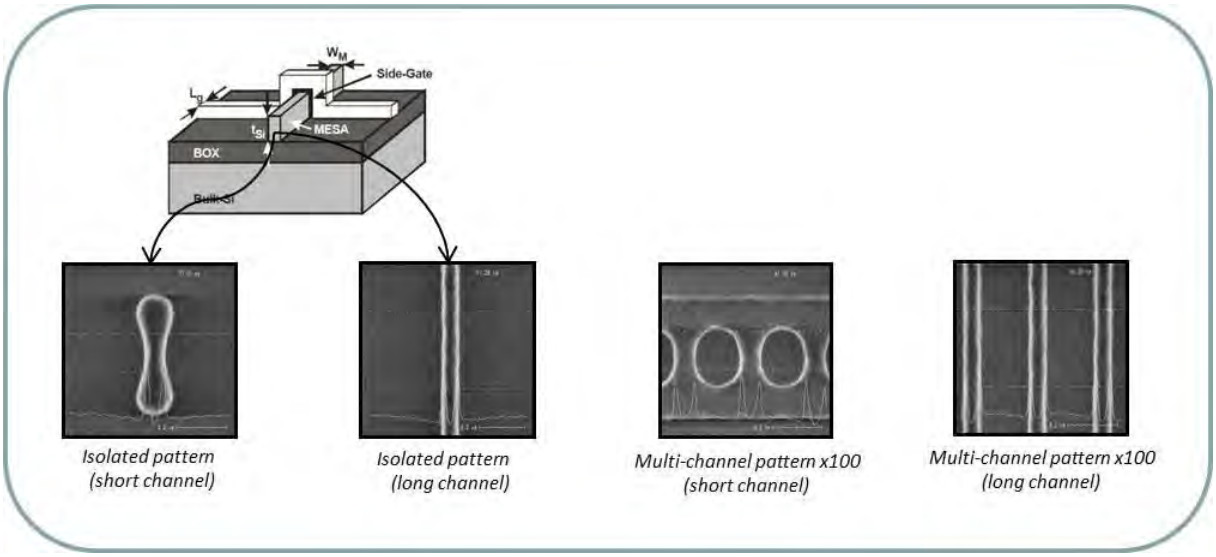


Figure 5: SEM pictures of the devices observed on various chips of the 300mm wafers after the photo-lithography. Long and short isolated devices with long and short arrays of devices (x100 fingers)

All the critical dimension (CD) measurements (after photolithography and after active patterning) will be done using in-line field-emission-scanning electron microscope (SEM).

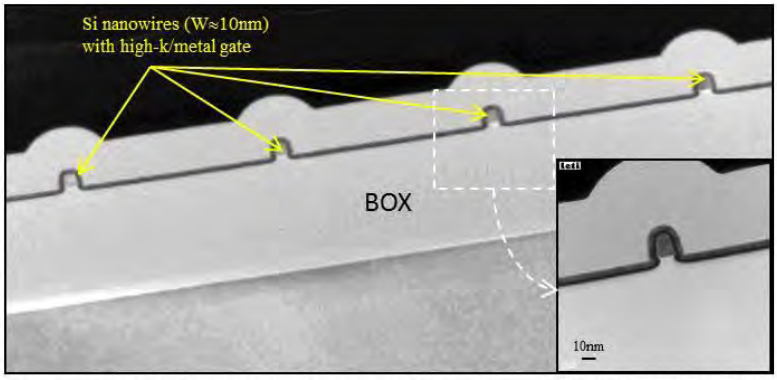
The linewidth before etching –referred to as developed inspection critical dimension- is around 80nm. After etching, the reduction of the silicon nanowire width induces by the trimming is targeted to 65 nm in order to have nanowire width of around 15nm. Due to the dispersions induce by the photolithography, the NW width after etching is expected to vary between 10nm and 20nm.

III.2. GATE STACK DEPOSITION AND CHANNEL LENGTH

The gate stack used will be composed of high-κ/metal gate. 2.3nm chemical vapour deposition (CVD) HfSiON with 5nm CVD TiN and Poly-Silicon (50nm) layers will be deposited. This corresponds to an equivalent oxide thickness (**EOT) of around 1.1nm**.

A HRTEM picture of the nanowire cross-section will be performed in order to reveal the good conformal gate stack deposition surrounding the nanowire and to evaluate

the nanowire width. Fig. 6 shows a cross-sectional TEM micrograph of a conventional triple-gate silicon nanowire with high-κ/metal gate stack (isolated devices).



Cross-sectional TEM micrograph of triple-gate silicon nanowire with high-k/metal gate stack

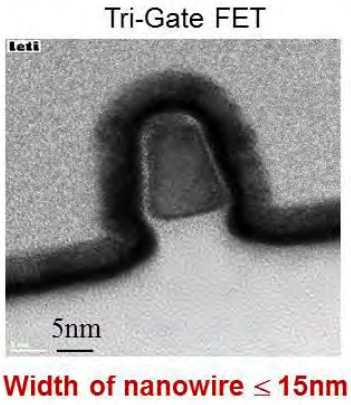


Figure 6: Cross-sectional TEM micrograph of a conventional triple-gate silicon nanowire with high-κ/metal gate stack

As for the active patterning, 193nm lithography tool will be used with a resist trimming in order to address **gate lengths down to 20nm**. First results obtained on regular Tri-gated nanowire are shown in Fig. 7.

III.3. FORMATION OF CONSTRICTIONS AT THE EDGES OF THE GATE

The both constrictions are fabricated after the gate etching (Fig. 8). A over-etch of the silicon film will be done in order to reduce the thickness. Then, we propose to do a deposition of thin spacer (nitride) to create the barrier between the source-drain and the channel. After the thin spacer etching, an epitaxial undoped silicon growth will be realized to recover the barrier and to form the both constrictions. Afterwards, a nitride spacer thickness of around 20nm will be formed on the silicon source-drain. Then, low parasitic resistance will be realized by **epitaxial doped silicon growth on the**

source-drain (ΔT_{SI}=18nm). Then, a second spacer will be deposited and etched before the source-drain doping.

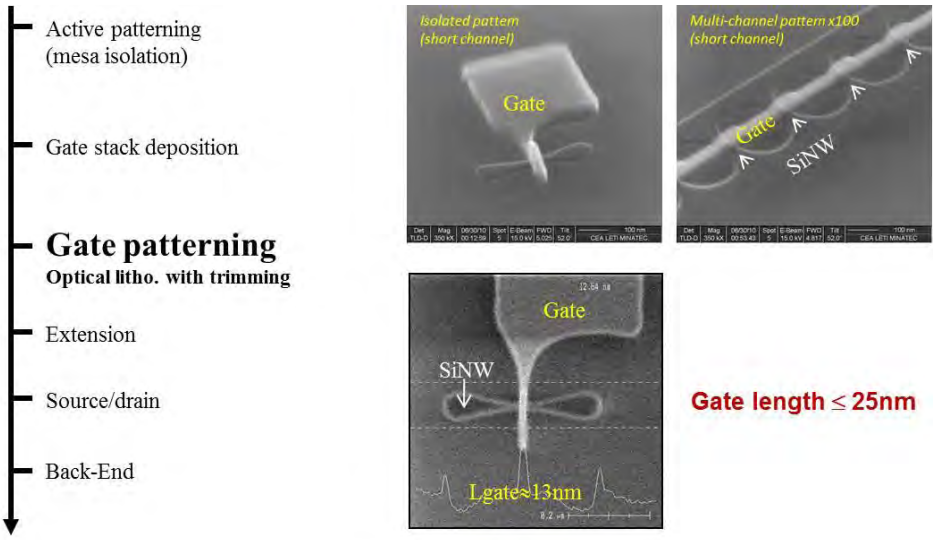


Figure 7: SEM picture of the gate after etching and trimming on regular Tri-gated nanowire transistors. Gate lengths below 25nm are obtained.

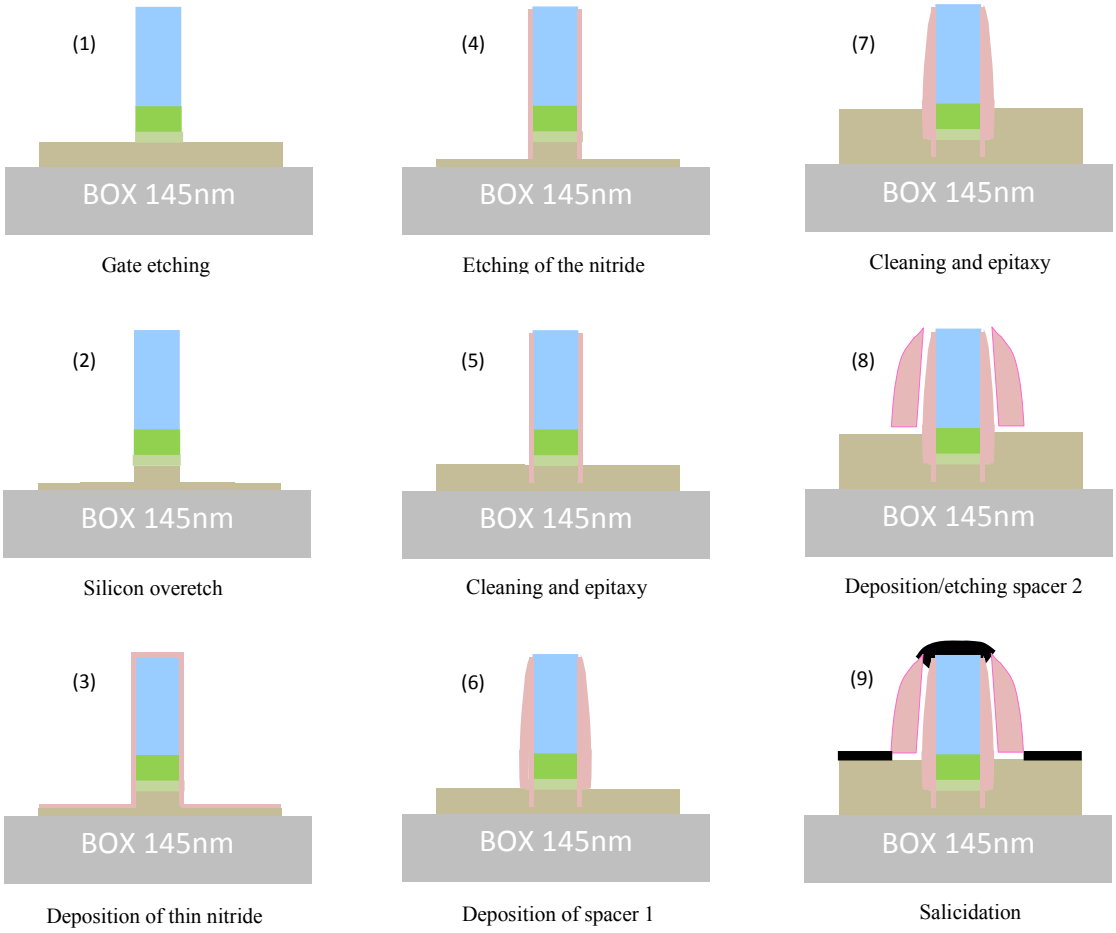
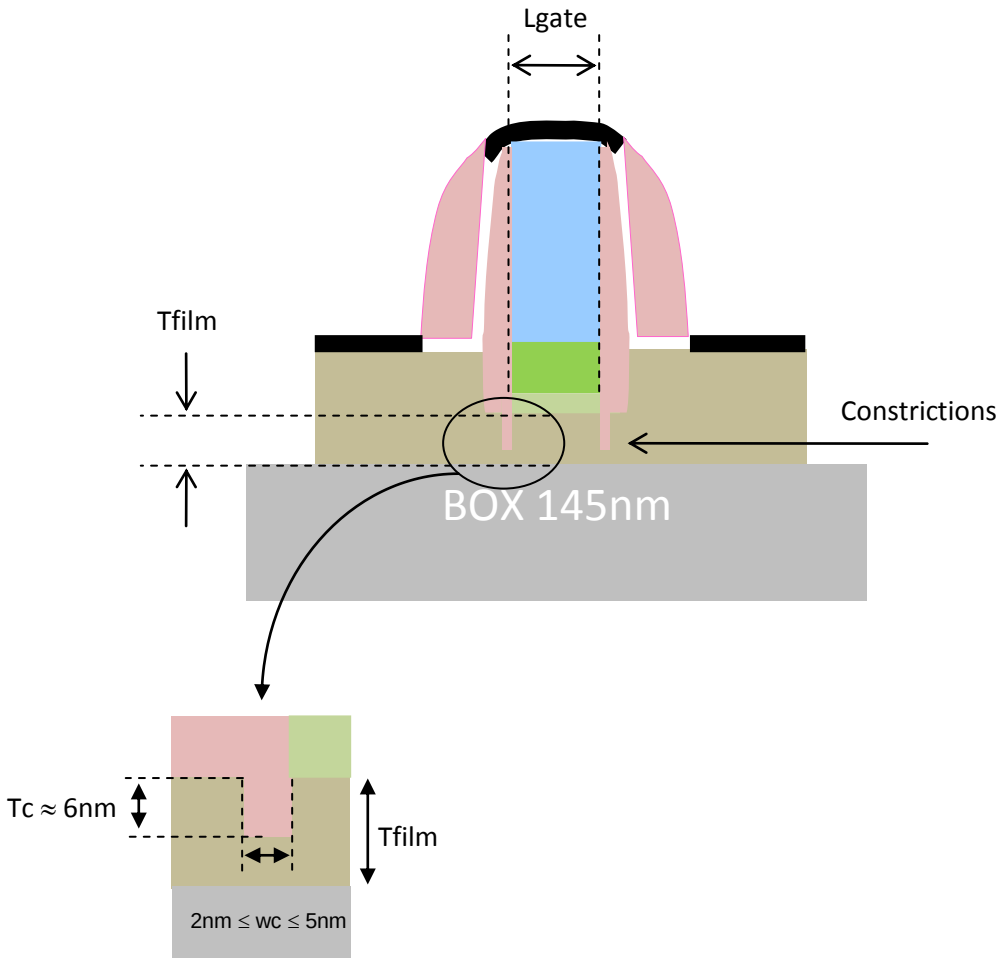


Figure 8: Simplified flow-chart for the fabrication of variable barrier tunnelling transistors.

Different splits on the thin nitride spacer will be done in order to obtain after etching a constriction of width varying from 5nm down to 2nm. Finally, the main process specifications for the fabrication of junctionless MOSFET are the following:



Width of nanowire W:	10nm ≤ W ≤ 20nm
Gate length L_g:	20nm ≤ L_g ≤ 10µm
Silicon thickness	T_{film}=12nm
Gate stack:	0.8nm SiO_2 / 2.3nm HfSiON / 5nm TiN / 50nm Poly-Si
CD spacer:	20nm
Elevated source/drain:	18nm
Width of constrictions:	2nm ≤ wc ≤ 5nm
Thickness of constrictions:	Tc≈6nm

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Deliverable 4.1: Guidelines on admissible electrical parameter variation for Gated Resistors

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28 February 2011

Abbreviation list

AM : accumulation-mode

D: Drain

FDSOI: fully depleted SOI

GAA: Gate-All-Around

IM: inversion-mode

LER: line-edge-roughness

L_g: gate length

RDF: random dopant fluctuation

S: Source

SCE: short channel effects

SiNW: Si nanowire

SOI : Silicon-On-Insulator

T_{ox}: oxide thickness

t_{Si}: nanowire thickness

V_t: threshold voltage

WF: work function

W_{Si}: nanowire width

Abstract

As a potential replacement of conventional MOSFETs, it is very important to understand the effect of process variations on the electrical characteristics of junctionless transistors. In this report, we are going to present the different sources of variability expected on a junctionless transistor based on previous publications on the competing devices.

Introduction

With the scaling of conventional transistors there is a deterioration of the gate control to the channel. As an alternative, new device structures like multiple gate MOSFETs and fully depleted SOI devices have emerged. However, one of the main challenges in building such devices in CMOS technology is the formation of ultra sharp and shallow source/drain (S/D) junctions to suppress short channel effects (SCE). The junctionless transistor has been reported to avoid this problem [1,2], as the doping concentration is uniform across the S, D and channel regions. However, the Si channel needs to be heavily doped to get reasonable high current when the transistor is on. Therefore, it can be expected that a large threshold voltage variation due to random dopant fluctuation and the variation of the nanowire dimensions might result in the junctionless transistors.

Discussion

The main sources of Si nanowire performance variability are schematically summarized in Fig. 1 and listed as follows:

- Channel random dopant fluctuation (RDF)
- Nanowire channel line-edge-roughness (LER)
- Nanowire width (W_{Si})
- Nanowire thickness (t_{Si})
- Metal-gate work-function (WF)
- Gate oxide thickness (t_{ox})
- Gate length (L_g)

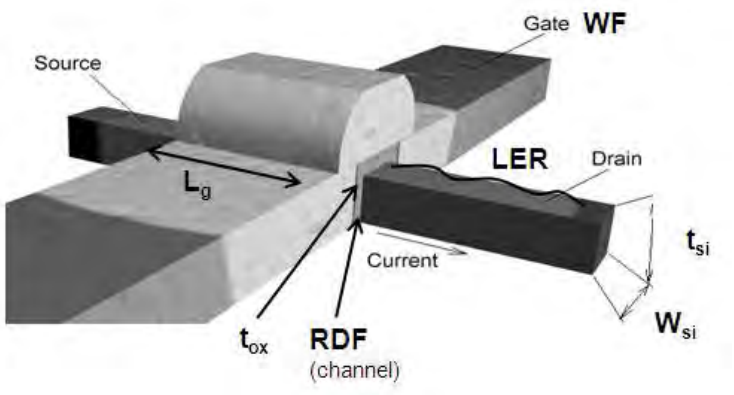

Fig1. Schematic view of a SiNW and its variability sources.

There are very few papers that have reported on the variation sources for Si nanowires [3]. Zhuge et al have experimentally characterized the variability in Gate-All-Around (GAA) Si nanowire (SiNW) transistors and concluded that the main sources of variation are the NW size (radius, R) and gate work-function (WF) variations (see Fig2).

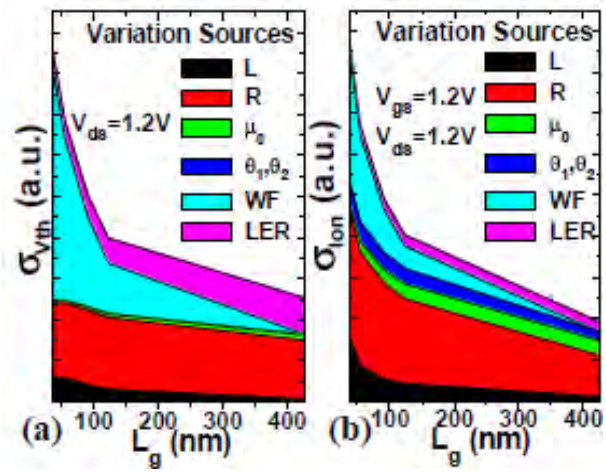

Fig2. Contributions of different fluctuation sources in SiNW transistors to (a) threshold voltage (Vt) and (b) drive current (Ion) variations [3].

In this case Zhuge et al were studying an inversion-mode (IM) nanowire transistor, with a S-channel-D doping of n+-p-n+ and no channel implantation. On the contrary, the junctionless transistor is an accumulation mode nanowire transistor, with a uniform S-channel-D doping of n+-n+-n+, with a heavily doped channel. This means that the variability sources are going to differ between them, as we are going to discuss next.

Channel random dopant fluctuations (RDF)

Traditionally channel doping has been used for adjusting the threshold voltage in conventional planar MOSFET transistors. At very small gate lengths, the number of dopant atoms in the channel has decreased significantly (as seen in Fig3, [4]), which is quite difficult to control during the fabrication process. Therefore, the random dopant fluctuation in the channel has become probably the major source of variation in conventional scaled MOS transistors in the last technology nodes. For example, for the 45nm technology node RDF corresponds to around 60% of the total sigmaV_t [5].

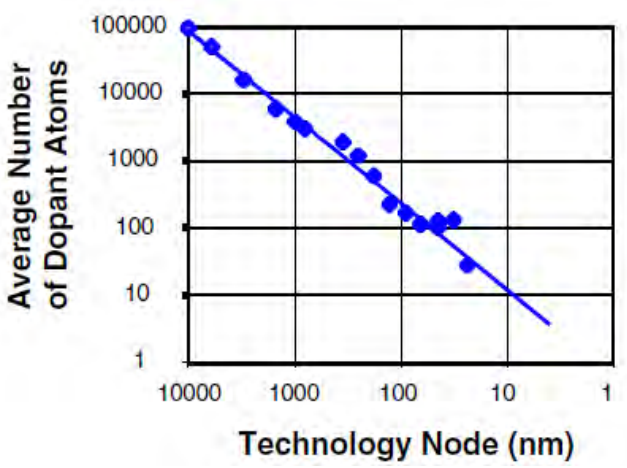

Fig3. Average number of dopant atoms in the channel by technology node [4].

In the case of the inversion mode SiNW transistor, the channel is nearly intrinsic and the Vt is adjusted with the selection of an appropriate metal gate material and thus, it is not affected by RDF. However, in the junctionless transistor the SiNW needs to be heavily doped to allow for a high drive current when the device is on [1]. The statistical variation of the dopants in the channel causes a threshold voltage variation (σV_t) that becomes significant for channel dopings above 1E18cm^{-3} as shown in Fig4 [6]. For example, if the nanowire dimensions are W_{Si}=10nm, T_{Si}=10nm and L_g=20nm, the number of doping atoms in the channel would be 10 to 100 for the doping concentrations to be used in this project (5E18 - 5E19 cm^{-3}) [7].

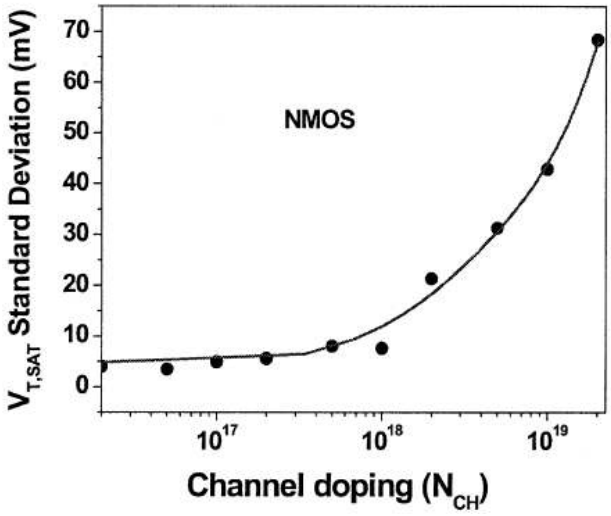

Fig4. NMOS Vt variation with channel doping due to RDF [6].

Nanowire width/thickness

The origin of the Vt variation with the nanowire size has been attributed in many papers to the quantum confinement effects in the nanowire channel at small dimensions [8, 9]. When the channel width fluctuates, the degree of the quantum confinement effects varies, resulting in the Vt fluctuation.

Choi et al [10] has experimentally looked at this effect in GAA junctionless transistors and their results showed a large Vt variation with nanowire width in the case of junctionless transistors due to the highly doped channel. In contrast, for an inversion mode transistor, the Vt variation is not as large because the desired Vt can be obtained by changing the metal gate WF, while maintaining a nearly intrinsic channel.

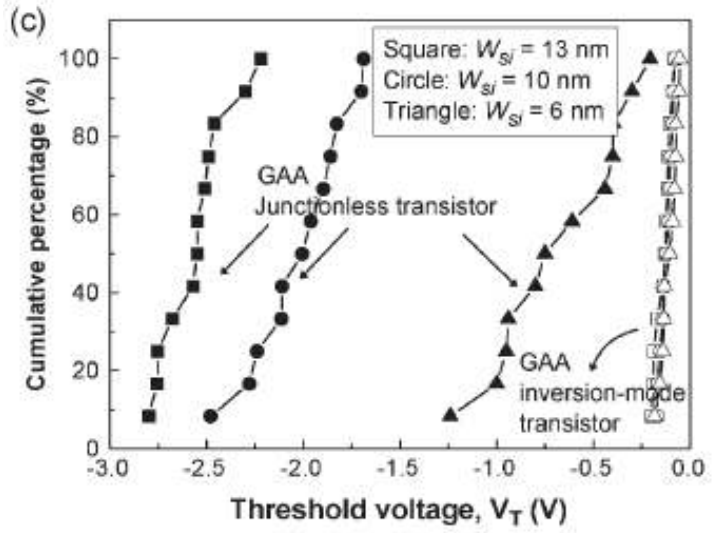

Fig5. Experimental cumulative distribution of V_t in GAA inversion-mode and junctionless transistors [10].

The junctionless transistors in the SQWIRE project are going to be patterned using 193nm photolithography and a new resist trimming method developed by CEA-LETI as described in the deliverable 2.2. Considering the variation on the Si layer from the SOI substrates and the dispersion induced by the photolithography, the nanowire width is expected to vary between 10 and 20nm.

Metal gate work function

For the fabrication of the junctionless devices a high-k/metal gate process is going to be used with a TiN metal gate. This gate metal is composed of grains with a diameter of >10nm (as shown in Fig6, [11]). These grains have different crystal orientation and

grain size resulting in a WF variation, which increases as the gate area scales and becomes comparable to the metal grain size. For undoped FinFETs and inversion-mode SiNW transistors the WF variation has been reported to be the dominant source of the Vt variation at small gate lengths [3,11] and needs to be looked into detail in the case of junctionless transistors. The TiN grain size increases with deposition temperature [12], therefore, it is critical the control of this process step during the nanowire fabrication.

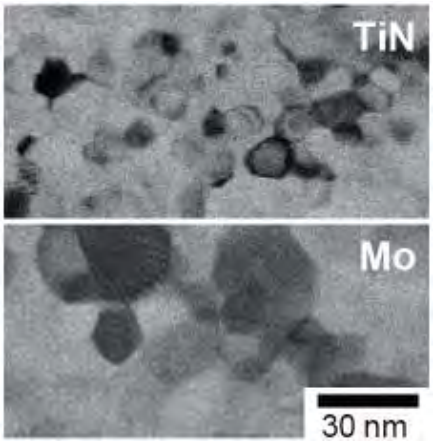

Fig6. TEM of TiN and Mo metal gates [11].

Other sources of variability

The contribution from line-edge-roughness (LER), gate length and gate oxide thickness to the V_t variability has been reported to be very small and are not going to be considered in this project [3,9].

Variation study

In the literature the conventional way of reporting the random variation in the transistor characteristics is using the Pelgrom plot (σV_t versus $1/\sqrt{(LW)}$). Its slope A_{VT} is an indicator of V_t fluctuation and it can be used to compare different device structures. In task T4.3 IPLS will perform a statistical variability analysis on the junctionless transistors and a comparison with previously reported results for conventional high-k/metal gate planar devices (as example, Intel 45nm technology A_{VT} is 2.4 mV·um as seen in Fig7, [5]), FinFETs (as example, 3 mV·um, [11]) and FDSOI. In addition, TEM will be used to get a statistical value of the nanowire

dimensions. The correlation of these results with the threshold voltage variation will help us to determine the contribution of the different variability sources.

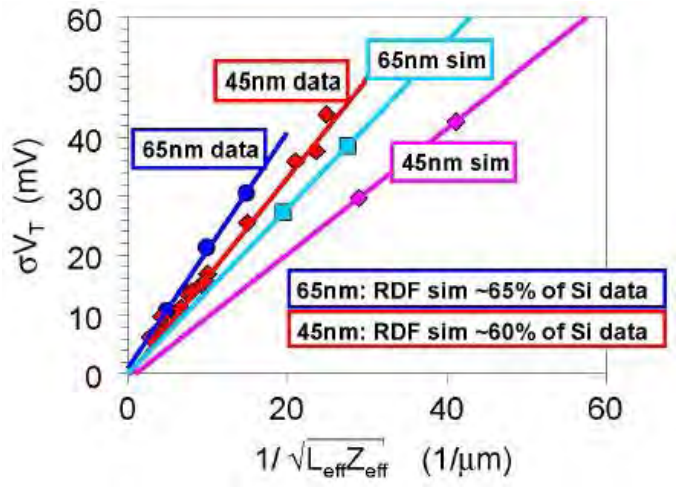

Fig7. Intel 65nm and 45nm technology Vt variation [5].

Conclusions

The main variation sources in junctionless transistors are expected to be RDF, nanowire dimensions and metal gate WF variations. In order to minimize their impact, a close process control during the device fabrication is needed, especially during the photolithography and metal gate deposition steps. An extensive variability study will be performed in task T4.3 to determine their contribution on the V_t variation of the junctionless transistor.

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Deliverable 4.2: TEM cross sections on prototyped Gated Resistors

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21 June 2011

Abbreviation list

D: drain

FIB: focused ion-beam

HRTEM: high resolution TEM

S: source

SEM: scanning electron microscopy

SOI : Silicon-On-Insulator

TEM: transmission electron microscopy

Abstract

IPLS has performed the TEM cross sections on prototype devices made at TNI-UCC. This is going to help us to develop a protocol for the nanovisualisation of the nanowires to accurately measure their thickness and width, which will feed back to task 3.2.

Sample experiment

The prototype samples delivered to IPLS consist of a half 4-inch SOI wafer with 7 fields containing 198 devices each. These devices are junctionless transistors with

single or multiple fingers and different gate lengths and nanowire dimensions. The gate oxide is 10 nm thick, covered by a 50 nm polysilicon gate.

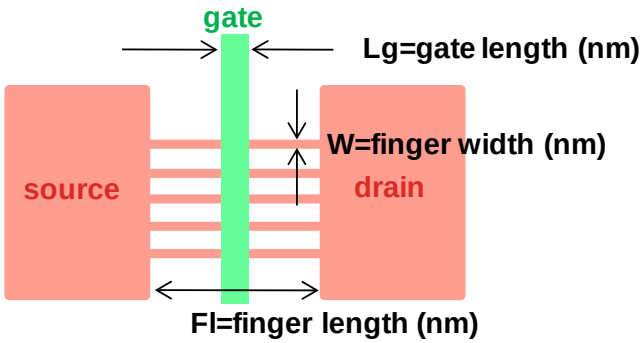


Fig. 1 Top-down of the devices with critical dimensions.

TEM characterization

For the analysis of nanowires with TEM the sample preparation is very critical in order to obtain excellent analysis results. This is done using an in-situ lift out technique on a dual-beam FEI Strata 400 focused ion-beam (FIB). The lift-out procedure consists on locating the area of interest using the FIB microscope capabilities. Then a layer of FIB-deposited Pt is placed over the area of interest to prevent milling or surface damaging. Using a large beam current two trenches are created on either side of the Pt strap. A smaller beam current is used to thin the central part between the trenches and three cuts are made to frame the area of interest. The omniprobe is inserted and positioned on the membrane and is pasted to it by depositing Pt. Then the membrane is lifted and brought to a premounted grid where is pasted. At this point, the omniprobe can be cut from the sample. Finally, once the sample is seated on the grid, it is thinned to a thickness of approx 100nm suitable for TEM imaging.

The transmission electron microscopy (TEM) analysis was performed on a FEI Technai G20 LaB6 operating at an accelerating voltage of 200 kV.

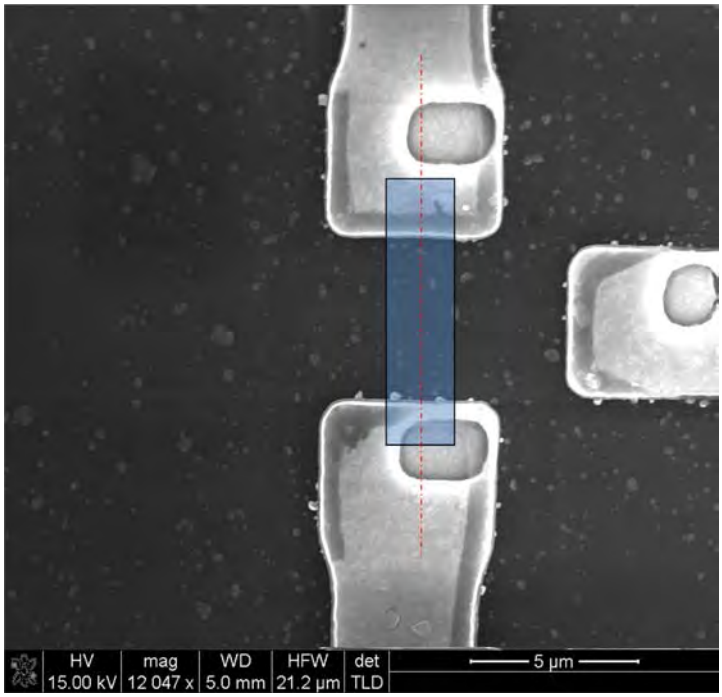


Fig. 2 Top down SEM overview with Pt location and section direction.

Results and discussion

The first TEM analysis was done on a wide single nanowire transistor along the nanowire length in order to check the Silicon thickness, the effective gate length and quantify the gate undercut.

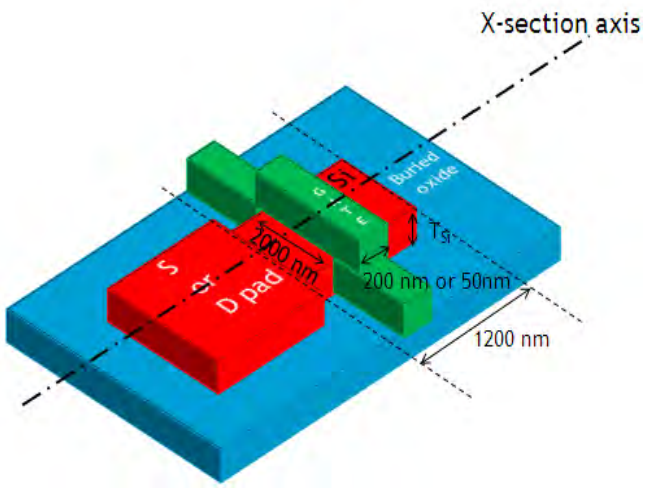


Fig. 3 Schematic of the nanowire transistor structure used for the first TEM analysis and the cross section axis.

In Fig. 4 it can be seen that the gate hasn't been fully etched, still remaining around 8nm of polysilicon. Tyndall is currently running a few test to optimise the gate etch sequence (breakthrough and softlanding times).

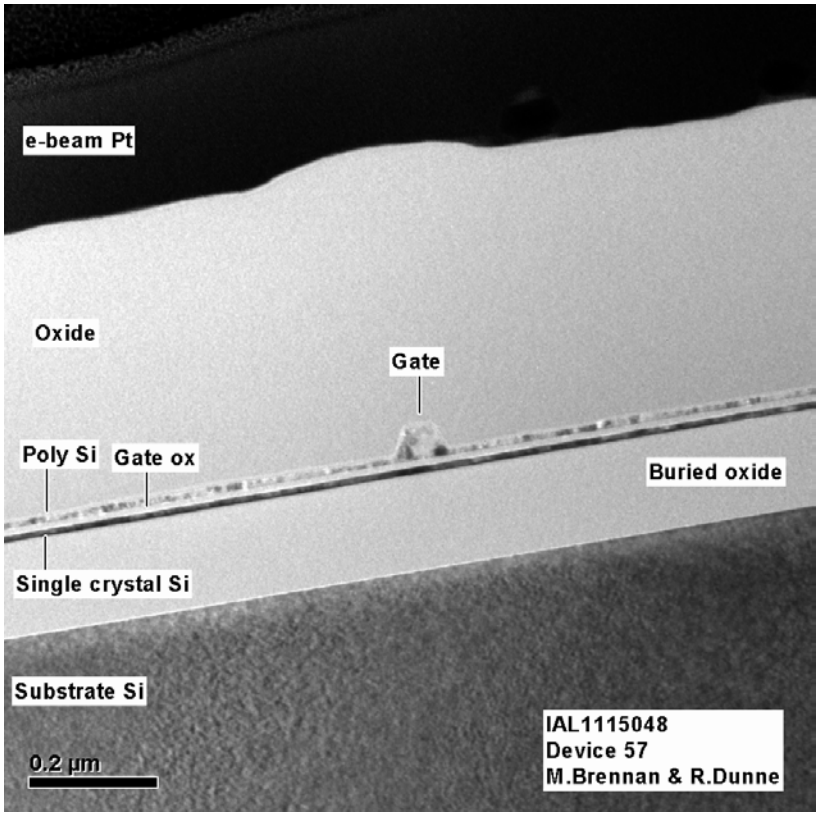


Fig. 4 TEM cross section along the nanowire showing the incomplete etching of the polysilicon gate.

The nominal gate length for the 2 devices analysed was 50 and 200nm. The resulted gates as shown in Fig 5 have a length at the base of 80 and 223nm respectively, which corresponds to 30 and 23 nm differences between the layout and the printed length respectively. The poly gate is also not showing a straight vertical profile, with a significant sidewall inclination, which would suggest an excessive polymerizing gas flow during the dry etch.

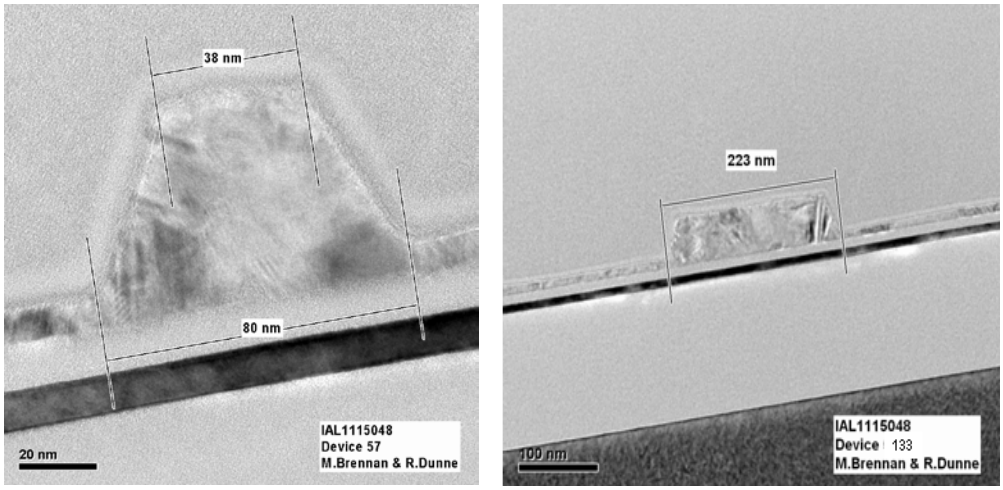


Fig. 5 HRTEM of the polysilicon gate showing the effective gate length measurements.

The second TEM analysis was done on a multiple finger transistor and cutting along the gate to measure the nanowire dimensions (Fig. 6). The structure analysed consists of 20 fingers which are 50nm wide with an expected Si thickness between 5 and 10 nm.

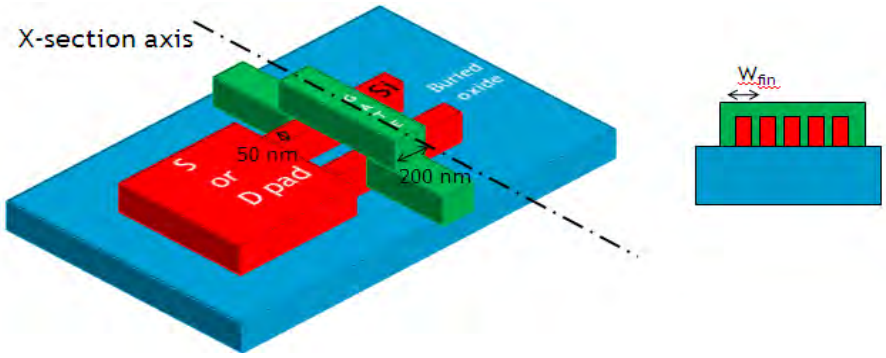


Fig. 6 Schematic of the nanowire transistor structure used for the second TEM analysis and the cross section axis.

Fig 7 shows the TEM cross section of 3 consecutive fingers. They have a dog bone type of shape (thinner in the middle), a width of 40nm and a Si thickness between 4.8 and 6.5 nm (Fig 8). The width of the rest of nanowires in the structure hasn't been measured but it was consistently uniform across the structure.

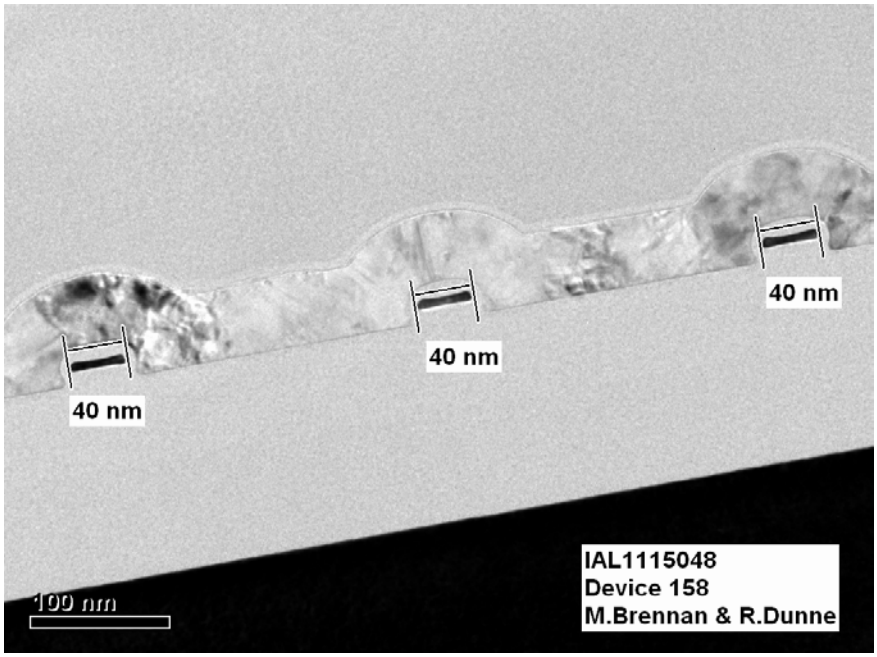


Fig. 7 TEM cross section along the gate showing 3 adjacent nanowires.

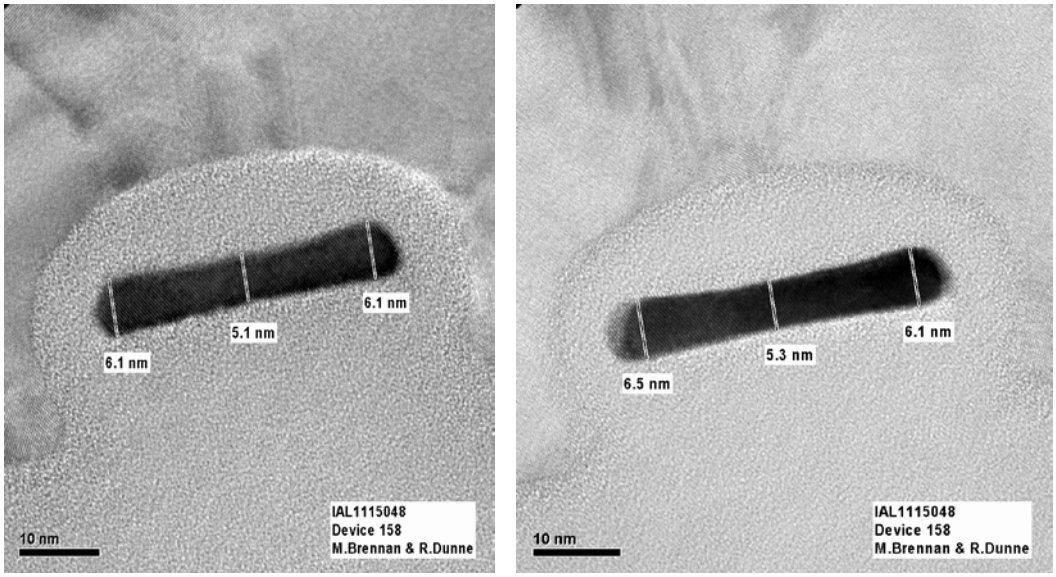


Fig. 8 HRTEM image showing the nanowire Si thickness for 2 adjacent fingers.

The polysilicon gate thickness is around 48 nm and the gate oxide thickness varies from 5.7 nm (at the edge, where is thinner) to 10.5 nm (at the centre, where is thicker) as seen in Fig 9.

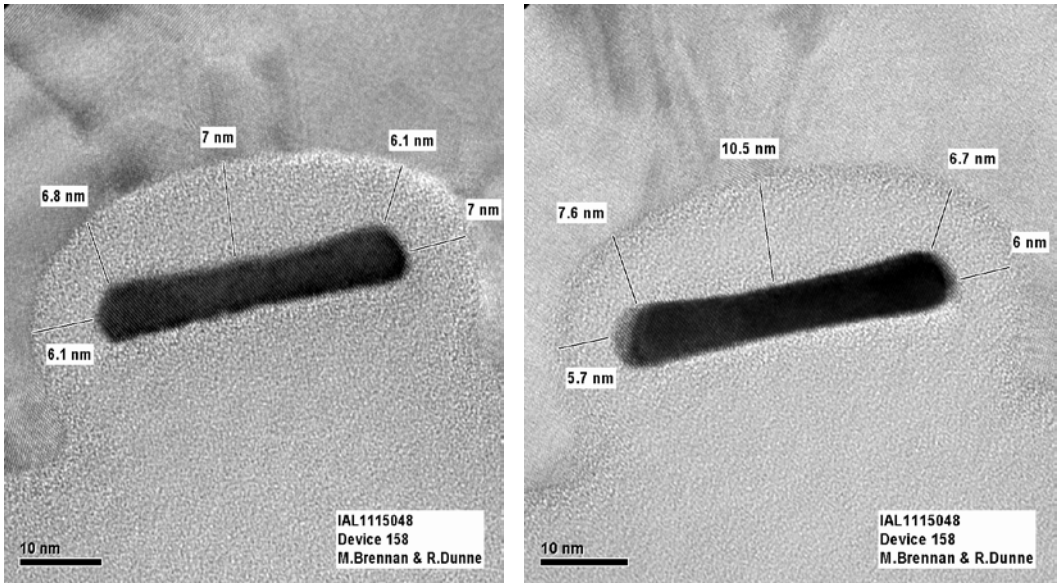


Fig. 9 HRTEM image showing the gate oxide thickness measurements.

Conclusions

In conclusion, TEM has proof to be an excellent analysis technique to accurately measure the thickness and width of the nanowires and assess the influence of processing on the nanowire geometry and quality.

Quarterly report WP1 : MAGWEL

Author: Wim Schoenmaker

Date: May 18, 2011

Introduction

MAGWEL' role in Swire consists of making the 3D quantum simulation tools that are (and were) developed at Tyndall and IMEC easily usable by intregration of these tools in the MAGWEL device simulation environment. During the first phase of the project, the emphasis has been on defining and designing the graphical user interface (GUI) that should realize this goal. A major design concern is robustness against erronous settings of input variables. An overview of the design decisions to address this issue is given below:

- Device loading
- Input variables
- Solution flow
- Excitation settings
- Results collection

After having identified these cathegories in the simulation flow, a design of the graphical user interface has been set up. During the reporting period, the design has been implemented and extensively tested. We can conclude the the GUI is now fully operational and robust against faulty inputs.

Technical aspects

The GUI design is based on the Document Object Model (DOM) approach. For that purpose a schema file is written that determines the hierarchical structure of the data as well as sets bounds on the allowable values that the data can have. The schema file determines which information the user can supply for performing the simulation. For example, the various solution modes of the NEGF solver of Tyndall are listed in the schema file as:

```
<xs:simpleType>
  <xs:restriction base="nonEmptyString">
        <xs:enumeration value="uncoupledModeSpace" />
        <xs:enumeration value="coupledModeSpace" />
        <xs:enumeration value="fastUncoupledModeSpace" />
        <xs:enumeration value="fastCoupledModeSpace" />
  </xs:restriction>
</xs:simpleType>
```

Once that the schema file is in place, the user data must be stored in a ASCII (readable) file. For that purpose the UML/XML modeling language is used. In particular, the selected user data for above model is found in the fragment :

<tyndallQuantumTransportModel>

<method>fastUncoupledModeSpace</method>

</tyndallQuantumTransportModel>

of the ASCII input file. (Here the option " fastUncoupledModeSpace" was selected. Of course, remembering this syntax literally while composing the input file is not feasable. However, combining the Xercess software with the QT GUI development tools, it is possible to generate a true graphical user interface, such that the user only has to select from a drop-down menu (or other buttons) to activate his/her choice.

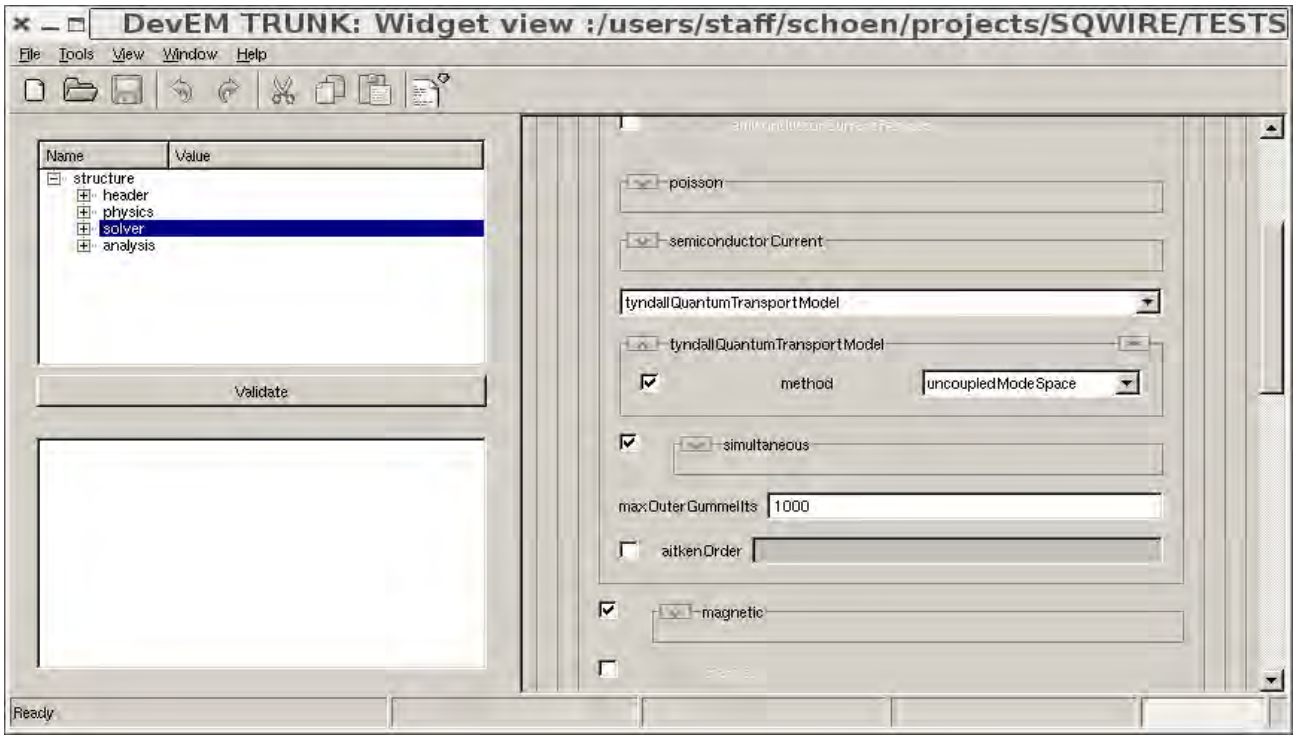


Fig.1 The appearance of the GUI for selecting the desire solution method for the NEGF approach.

Finally, after having loaded the data in the GUI environment as well saved in an xml file, it is needed to communicate this information the the compute kernel, which is in general a different library. For that purpose we have chosen a C++ object oriented architecture. Dedicated C++ parsers have been written to extract the information and to 3rd party software. The appropriate header files need to be passed:

```
static const int UNCOUPLEDMODESPACE = 1;
static const int COUPLEDMODESPACE = 2;
static const int FASTUNCOUPLEDMODESPACE = 3;
static const int FASTCOUPLEDMODESPACE = 4;
int getMethod() const;
static int getMethod(const std::string &methodName);
std::string getMethodName() const;
```

Summary : The design and development of the GUI is completed by the end of this reporting period.

Quarterly report WP4 : MAGWEL

Author: Wim Schoenmaker

Date: June 2, 2011

Introduction

MAGWEL' role in Swire consists of making the 3D quantum simulation tools that are (and were) developed at Tyndall and IMEC easily usable by intregration of these tools in the MAGWEL device simulation environment. During the first phase of the project, the emphasis has been on defining and designing the graphical user interface (GUI) that should realize this goal. A major design concern is robustness against erronous settings of input variables. An overview of the design decisions to address this issue is given below:

- Device loading
- Input variables
- Solution flow
- Excitation settings
- Results collection

After having identified these cathegories in the simulation flow, a design of the graphical user interface has been set up. During the reporting period, the design has been implemented and extensively tested. We can conclude the the GUI is now fully operational and robust against faulty inputs.

Technical Aspects

Whereas in the reporting of WP1 we have described the effort to deal with the code access from a user's perspective, in this part (WP4) we will address the code integration from a operational perspective. The challenge is to achieve sufficient computational speed combined with the flexible set up that is provided to the user by the GUI. In particular, this means that the non-equilibrium Green function formalism (NEGF) that was developed at Tyndall must be implemented in the source code environment of MAGWEL. This work is presently ongoing. We can report here on a number of technical issues that have been encountered.
The first question that needs to be answered is at which location the quentum transport modules should be activated. Since the MAGWEL software deals primarily with the drift-diffusion model, we may use the outcome of the drift-diffusion model as an initial guess for the quantum transport computation. This will be our strategy. At zero bias we determine carrier densities and potentials from a drift-diffusion simulation. These results will serve as a starting point for iterating to the NEGF solution. A second question concern variable scaling. Numerical techniques demand that the floating number ranges are pre-set in such a way that rounding errors are minimized. This demand leads to variable scaling prescriptions that transform all terms in the equation set in the numerical range close to 1. The scaling analysis has been completed.
A third key step is the construction of the Green function itself. This will be done inverting the Schrodinger operator on the discretized grid. This work is presently ongoing. Since the MAGWEL solver is ab-initio design to deal with magnetic fields as possible ingredients, the discretization will

account for this possibility. Finally the computation of the Green function itself requires powerful linear solvers. For this reason we have integrated some state-of-the-art linear solvers in the MAGWEL environment. In particular for linear solving we have integrated the UMFPACK library (University of Florida) and the Jacobi-Davidson eigenvalue solver (University of Utrecht).

The IMEC software for dealing with analytically based quantum transport computation has been transferred to MAGWEL. The integration of this code is less laborous as the Tyndall code since it is written is Fortran. By composing a series of wrappers (C++ interfaces) around it, we are able to realize the integration.

Quarterly report of WP2: Device fabrication (SOITEC/TNI-UCC/CEA-LETI)

T2.1 - Fabrication of high-uniformity Silicon-on-Insulator (SOI) wafers (SOITEC)

SOITEC is currently able to produce SOI wafers with a silicon film thickness (t_{Si}) of 20nm and a thickness variation of less than 1 nm (σ_t = 0.35 nm). SOITEC provided the first 12 SOI wafers with 300 mm diameter for the fabrication of nanowire gated resistors and nanowire variable barrier transistors. The silicon film thickness was 12 nm and the BOX (buried oxide) thickness 145 nm.

SOITEC has continued to work on the improvement of the thickness uniformity of 300 SOI wafers with a silicon film thickness of less than 20nm and with the target for thickness variation of less than 1 nm. A path to ± 2 Å variation for Wafer to Wafer thickness, control has been identified and will be implemented before end of 2011. The work to improve within the wafer uniformity is on going.

The following paper was published in the beginning of May 2011:

W. Schwarzenbach, X. Cauchy, O. Bonnin, N. Daval, C. Aulnette, C. Girard, B.-Y. Nguyen & C. Maleville "Ultra-thin film SOI/BOX substrate development, its application and readiness", ECS Transactions, 35 (5) 239-245 (2011)

T2.2 – Design and Fabrication of nanowire Gated resistors (CEA-LETI, TNI-UCC)

Based on simulation results provided by TNI-UCC (doping and sizing of the nanowire), CEA-LETI has developed a new route for the fabrication of nanowire gated resistors. SOI structures with silicon layers of 12 nm in thickness are used. Then, the silicon layer has been thinned down to 10nm. The semiconductor also needs to be heavily doped to allow for a

reasonable amount of current flow when the device is turned on. The implant energies and doses have been chosen (from process simulation – Athena Silvaco) to yield uniform doping concentration ranging from $5x10^{18}$ cm^{-3} up to $5x10^{19}$ cm^{-3}. Then, the silicon layer is patterned to create the silicon nanowires by a mesa isolation technique. The active stack used in this work is consisted of a 10nm doped Si, 2.5nm SiO_2 dielectric layer and an organic bottom anti-reflective coating (BARC) layer of around 24nm patterned using 193nm ArF resist. The thickness of the photoresist is around 160nm. The active zone (i.e. nanowire feature) is carried out using the trimmed resist/BARC as a mask.

The good electrostatic control being based on low dimensions of nanowire width (or diameter), shorter wavelengths are required for lithography. Today's most advanced lithography uses 193nm wave-length for the production of integrated circuits devices. Following the same philosophy than for the gate patterning, an approach based on resist trimming by dry plasma etching to elaborate our silicon nanowires has been developed. This approach has the advantage of reducing the dimensions without increasing the complexity of the lithography requirements. The main technological steps to pattern the nanowire are the following,

- First of all, HBr plasma curing process was performed in order to harden the 193nm ArF resist for a better etching resistance.
- Then, the BARC opening is done using CF_4 chemistry. This chemistry will be used in order to ensure vertical resist/BARC profile and correct linewidth roughness. Moreover, this sequence consuming a lot of photoresist, the thin thickness of the BARC layer is well suited to minimize the resist budget during the process.
- Then, the BARC/resist trimming process is performed just before the main etch to selectively pattern the silicon on the buried oxide. Trimming resist is performed to achieve nanowire structures as small as 15nm in width using the HBr/O_2 plasma. In order to smooth the resist patterns and then reduce the linewidth roughness, a curing step is performed just before the trimming.

The investigated structures after the photolithography are isolated lines (NW) and arrays of lines with long and short dimensions. The arrays of lines with long dimensions are used to extract the capacitance and the carrier mobility.

All the critical dimension (CD) measurements (after photolithography and after active patterning) are done using in-line field-emission-scanning electron microscope (SEM). Due to

the dispersions induce by the photolithography, the NW width after etching varies between 10nm and 20nm.

For the first run, the gate stack used is composed of high-κ/metal gate. 2.3nm chemical vapour deposition (CVD) HfSiON with 5nm ALD TiN and Poly-Silicon (50nm) layers are deposited. This corresponds to an equivalent oxide thickness (EOT) of around 1.1nm.
As for the active patterning, 193nm lithography tool has been used with a resist trimming in order to address gate lengths down to 25nm. Afterwards, a nitride spacer thickness of around 20nm is formed on the silicon source-drain. Then, low parasitic resistance are realized by epitaxial doped silicon growth on the source-drain (ΔT_{SI}=18nm).

This work led to the publication of one deliverable (D2.2) in November 2010.

Moreover, many exchanges have taken place with IPLS, and a first processed wafer has been send to Intel to test their tester and probecard.

First *junctionless* nanowire transistors have been electrically characterized in order to extract I_{on}-I_{off} plot, threshold voltage, subthreshold slope, and DIBL. Wafers have been delivered to INPG-IMEP in order to do additional measurements for a deeper understanding of electrical performances of *junctionless* nanowire transistors.

T2.3 – Design and Fabrication of nanowire Variable-Barrier transistors (CEA-LETI, TNI-UCC)

Based on simulation results provided by TNI-UCC (nanowire and constriction sizing), CEA-LETI has developed a new route for the fabrication of tri-gate nanowire transistors including soft tunnel barriers which should strongly reduce source-to-drain tunneling and could even, in theory, achieve sub 60 mV/dec subthreshold slopes.
As for nanowire gated resistors, existing mask sets has been used, with the exception of the active area level which have been redrawn. Particular emphasis is placed on the control and reproducibility of the width of the nanowires as well as both constrictions.
The same process as for the gated resistors has been used to pattern the nanowire:

- HBr plasma curing process was performed in order to harden the 193nm ArF resist for better etching resistance.
- BARC opening is done using CF_4 chemistry in order to ensure vertical resist/BARC profile and correct linewidth roughness.

- BARC/resist trimming process is performed just before the main etch to selectively pattern the silicon on the buried oxide. Trimming resist is performed to achieve nanowire structures as small as 15nm in width using the HBr/O_2 plasma. In order to smooth the resist patterns and then reduce the linewidth roughness, a curing step is performed just before the trimming.

The main difference between conventional and variable barrier tunneling MOSFET transistors is the formation of constrictions at the edges of the gate.

The both constrictions are fabricated after the gate etching. A over-etch of the silicon film is done in order to reduce the thickness. Then, a deposition of thin spacer (nitride) is done to create the barrier between the source-drain and the channel. After the thin spacer etching, an epitaxial undoped silicon growth is realized to recover the barrier and to form the both constrictions. Afterwards, a nitride spacer thickness of around 20nm is formed on the silicon source-drain. Then, low parasitic resistance are realized by epitaxial doped silicon growth on the source-drain (ΔT_{SI}=18nm). Then, a second spacer is deposited and etched before the source-drain doping.

Different splits on the thin nitride spacer will be done in order to obtain after etching a constriction of width varying from 5nm down to 2nm.

This work led to the publication of one deliverable (D2.3) in February 2011.

WP3: Advanced Characterization and Test (WP Leader: IMEP/INPG)

The objectives of WP3 are i) the development of shared protocols for standard die-level electrical testing and parameter extraction, ii) the development of shared protocols for nanometrology of SOI substrates and fabricated devices and iii) the correlation of metrology data and electrical test parameters for feedback to simulation and fabrication workpackages.

In the last period, Junctionless transistors delivered by Tyndall have been tested at IMEP/INPG. Noise measurements have been carried out on the devices. It was found that the junctionless transistors have a 1/f noise similar to what is found in the best inversion-mode MOSFETs, and much less noise than in transistors with high-k dielectric gate oxide.[1]

Junctionless transistors have been measured at Tyndall and the following properties have been observed:

- The random telegraph noise (RTN) is much lower in junctionless transistors than in inversion-mode or accumulation-mode transistors. This is due to bulk transport instead of transport in surface channels.[2,3]
- A technique to extract mobility in junctionless transistors has been poroposed. It also allows one to measure the flatband voltage in those devices.[4]
- A model to explain the good output conductance (high Early voltage) in junctionless transistors has been derived.[5,6]
- Low-temperature (cryogenic) measurements reveal that junctionless transistors show conductance oscillation at higher temperature and higher drain voltage than inversion-mode devices of same dimensions, because the carriers are confined within a bulk channel that has a smaller diameter than the cross-section of the device.[7]

LETI/CEA has developed measurement protocols for die-level electrical testing and parameter extraction on 300mm wafers for the electrical characterization of first junctionless nanowire transistors fabricated in WP2. Basic electrical parameters have been extracted on both N- and P-type junctionless nanowire devices: I_{ds}-V_{gs} characteristics (at low and high drain voltage V_{ds}), the subthreshold slope, the DIBL (drain induced barrier lowering), the transconductance, the threshold voltage, I_{on}-I_{off} plots, etc.
The previous electrical parameters have been extracted for gate length varying from Lg=30nm up to 10µm on both Trigate nanowire and planar junctionless MOSFET devices. First results show that high-k/metal gate stack provides an excellent symmetry between the threshold voltage of N- and P-MOSFET with values close to 0.5V for Si film doping between 5×10^{18} cm^{-3} and 10^{19} cm^{-3}. This results clearly

demonstrate the feasibility of trigate silicon nanowire with junctionless configuration by using high-k/metal gate stack.

First wafer has been delivered to IMEP/INPG in order to perform advanced characterization.

IMEP/INPG has started the detailed static electrical characterization, low temperature and low frequency noise studies on n and p type junctionless transistors from LETI/CEA.

Soitec continues to develop UV/optical and Atomic Force Microscopy film thickness and roughness measurements in house. After the development of the corresponding techniques and protocols at CEA-LETI and IPLS a technical benchmarking will be performed.

[1] "Low-frequency noise in junctionless multigate transistors", Doyoung Jang, Jae Woo Lee, Chi-Woo Lee, Jean-Pierre Colinge, Laurent Montès, Jung Il Lee, Gyu Tae Kim, and Gérard Ghibaudo, Appl. Phys. Lett. Vol. 98, p. 133502 (2011) doi:10.1063/1.3569724

[2] "Comparative Study of Random Telegraph Noise in Junctionless and Inversion-Mode MuGFETs", A.N. Nazarov, C.W. Lee, A. Kranti, I. Ferain, R. Yan, N. Dehdashti Akhavan, P. Razavi, R. Yu, J.P. Colinge, ECS Transactions, Vol. 35, No. 5, pp. 73-78 (2011)

[3] "Random telegraph-signal noise in junctionless transistors", A. N. Nazarov, I. Ferain, N. Dehdashti Akhavan, P. Razavi, R. Yu, J. P. Colinge, Applied Physics Letters, Vol. 98, p. 092111 1-3 (2011)

[4] "Extraction of Channel Mobility in Nanowire MOSFETs Using Id(Vg) Characteristics and Random Telegraph Noise Amplitude", A.N. Nazarov, C.W. Lee, A. Kranti, I. Ferain, R. Yan, N. Dehdashti Akhavan, P. Razavi, R. Yu, J-P. Colinge, Proceedings of Ultimate Integration on Silicon Conference (ULIS), pp. 107-109 (2011)

[5] "The roles of electric field and the density of carriers in the improved output conductance of junctionless nanowire transistors", R.T. Doria, M.A. Pavanello, R.D. Trevisoli, M. Souza, C.W. Lee, I. Ferain,, N. Dehdashti Akhavan, R. Yan, R. Yu, A. Kranti, J.P. Colinge, ECS Transactions, Vol. 35, No. 5, pp. 283-288 (2011)

[6] "Extraction of flat-band voltage and parasitic resistance in junctionless MuGFETs", A.N. Nazarov, C.W. Lee, A. Kranti, I. Ferain, R. Yan, N. Dehdashti Akhavan, P. Razavi, R. Yu, JP Colinge, Proceedings of EUROSOI 2011, VII Workshop of the Thematic Network on Silicon On Insulator Technology, Devices and Circuits, pp. 53-54 (2011)

[7] "Low-temperature conductance oscillations in junctionless nanowire transistors", Jong-Tae Park, Jin Young Kim, Chi-Woo Lee, Jean-Pierre Colinge, Applied Physics Letters Vol. 97, pp. 172101/1-2 (2010); doi:10.1063/1.3506899

SQWIRE

WP4 Activity report for Q3

Period covered: 1-3-2011 to 31-5-2011

Date of preparation: 31-5-2011

Start date of project: 3-9-2010 **Duration:** 3 years

Coordinating person: Prof. Jean-Pierre Colinge

WP4: Potential for manufacturability (WP Leader: IPLS)

WP4: summary

The main objective of this work package is to evaluate the control and reproducibility of device parameters (such as threshold voltage and drive current) as a function of the thickness and width of the nanowires. The statistical variability of the devices will be studied through simulations and by using mass-production characterisation tools on the LETI wafers. TEM observations will be also performed on a statistically-relevant number of Gated Resistors to correlate actual device thickness and width to measured electrical characteristics.

Summary of WP4 deliverables status

Deliverable	Month	Description	Owner	Status
D4.1	6	Guidelines on admissible electrical parameter variation for Gated Resistors	IPLS	Completed. Summary delivered Feb'11
D4.2	10	TEM cross sections on prototype Gated Resistors	IPLS	Completed. Preliminary summary included in Q2'11 Activity report.
D4.3	19	Measured parameter variations for Gated Resistors with correlations to TEM observations	IPLS	Will start in Sept'11 once received LETI wafers.
D4.4	35	Manufacturability of the SQWIRE architecture based on parameter variation studies	Magwel	

Key:

	completed
	in progress

Task 4.1 Technology-aware design and specifications (IPLS)

The guidelines on admissible electrical parameter variation for junctionless transistors and the main variability sources are detailed in the D4.1 report (Feb'11).

In summary, the main variation sources in junctionless transistors are expected to be random dopant fluctuations (RDF), nanowire dimensions and metal gate work-function (WF) variations. In order to minimize their impact, a close process control during the device fabrication is needed, especially during the photolithography and metal gate deposition steps. An extensive variability study will be performed in task T4.3 to determine their contribution on the threshold voltage variation of the junctionless transistor.

Task 4.2 Statistical variability: simulations (TNI-UCC, IMEP/INPG)

An alarming paper was recently published in IEEE EDL 32(2), pp. 125-127 (2011).

That paper reports huge variations in threshold voltage in junctionless transistors (see

below). The results of this paper are basically correct, but the thickness of the gate oxide is 13 nm (*i.e.* larger than the thickness/width of the silicon nanowire itself.)

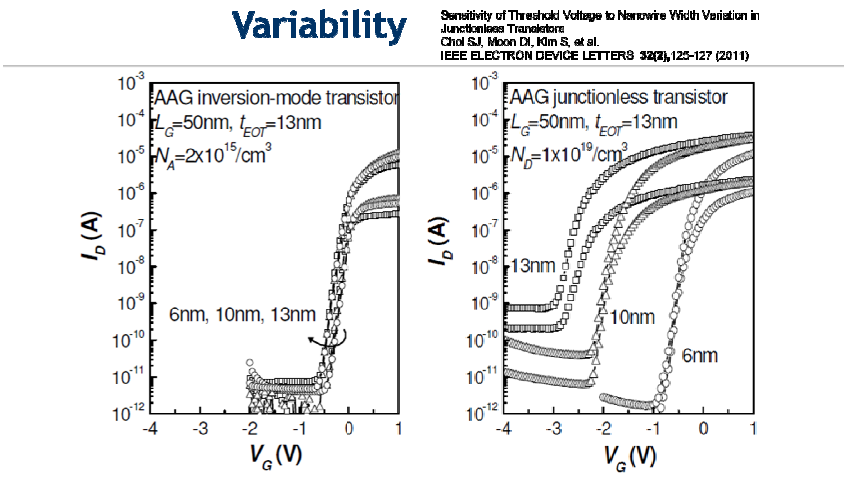
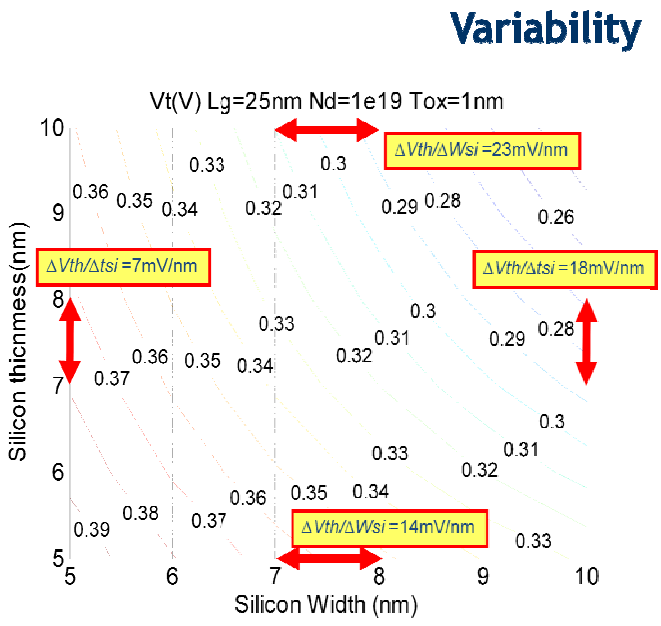
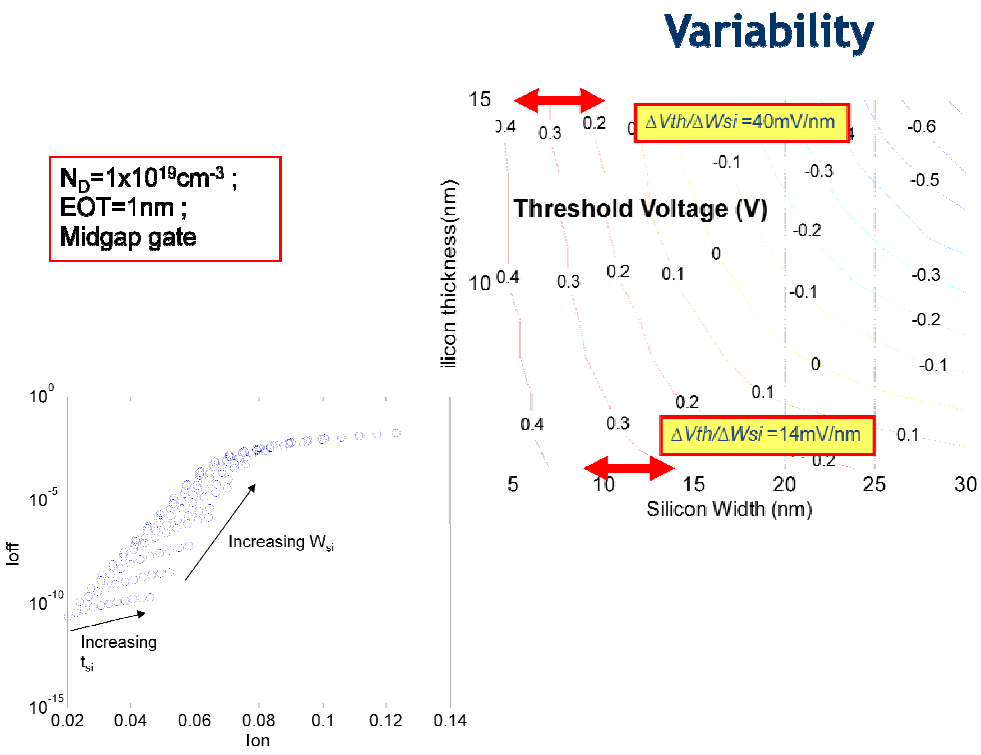


Fig. 3. Experimental I_D-V_G characteristics of inversion-mode transistors (a) and junctionless transistors (b) with various t_{si} values (6 nm, 10 nm, and 13 nm) at V_D of 0.05 V and 1 V. The doping concentration of each device is shown in the inset of graph.

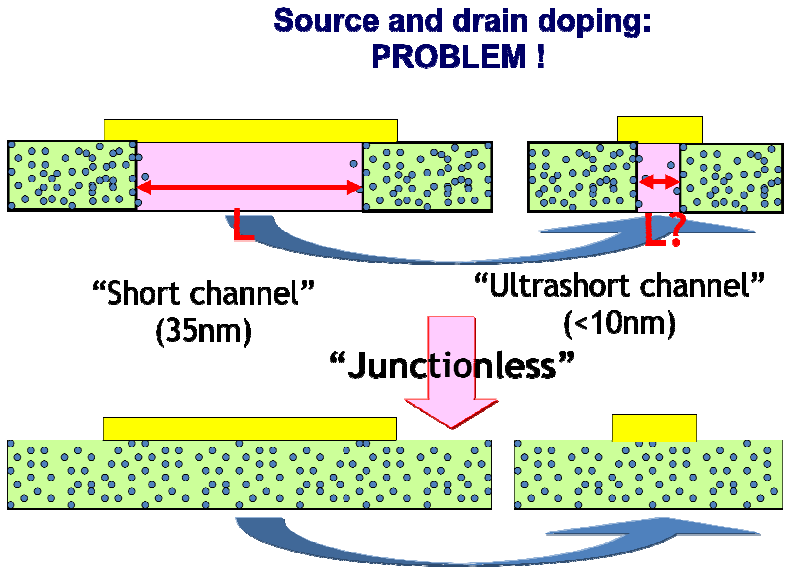
TNI_UCC has simulated the variation of threshold voltage in junctionless transistors for a more reasonable gate oxide thickness (1 nm). The results are found in the graphs below. A midgap gate material is used in both graphs. The SOITEC wafers have a thickness uniformity of 0.5 nm. Using a silicon thickness of 7nm and a width of 10nm with a variation of 10% (*i.e.* 1nm), we can expect a threshold voltage variation of 20 mV across a wafer.



For Lg=10nm $\Delta Vth/\Delta Wsi$ =14mV/nm



An important point that is often neglected is the variation of threshold voltage due to the imperfect sharpness of source and drain junctions: a few dopant atoms from the source and drain can be found a few nanometers from source or drain, in the channel region (see drawing below). This causes variations of effective channel length as well as a variation of the effective doping concentration in the channel. This problem does not exist in junctionless transistors.



This effect has been reported in an article published in the Japanese Journal of Applied Physics in 2010 (see below). Variations of threshold voltage as large as 80 mV have been predicted for a simple source/drain doping atom having diffused in the channel, depending on the position of the atom.

Japanese Journal of Applied Physics 49 (2010) 104301 **REGULAR PAPER**

Effect of Source/Drain Doping Gradient on Threshold Voltage Variation in Double-Gate Fin Field Effect Transistors as Determined by Discrete Random Doping

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Received December 30, 2009; accepted July 7, 2010; published online October 20, 2010

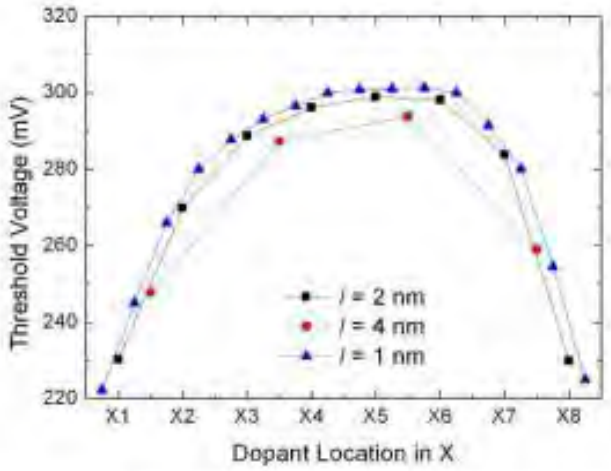
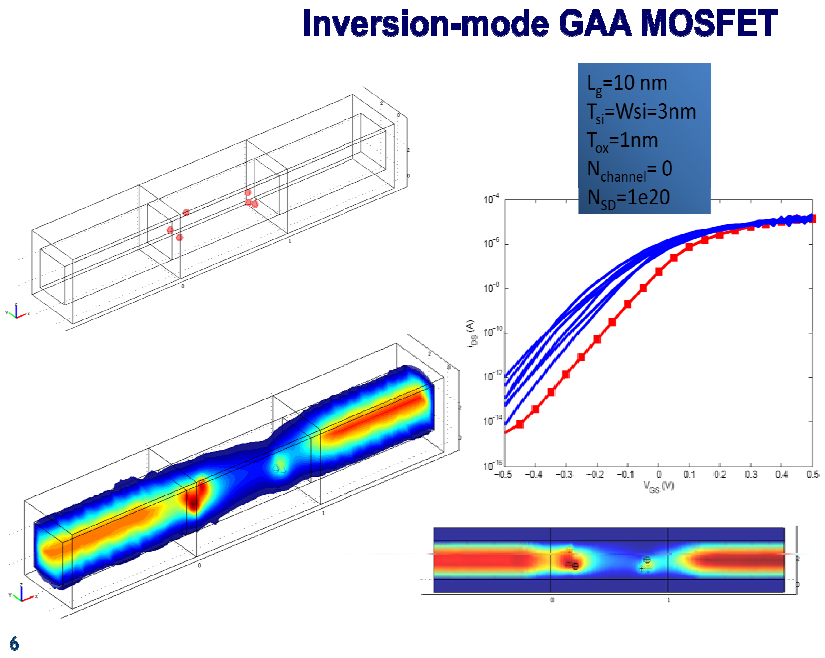


Fig. 8. (Color online) Threshold voltage variation due to a single impurity dopant located in the center of the channel at respective X's for l's of 1, 2, and 4 nm.

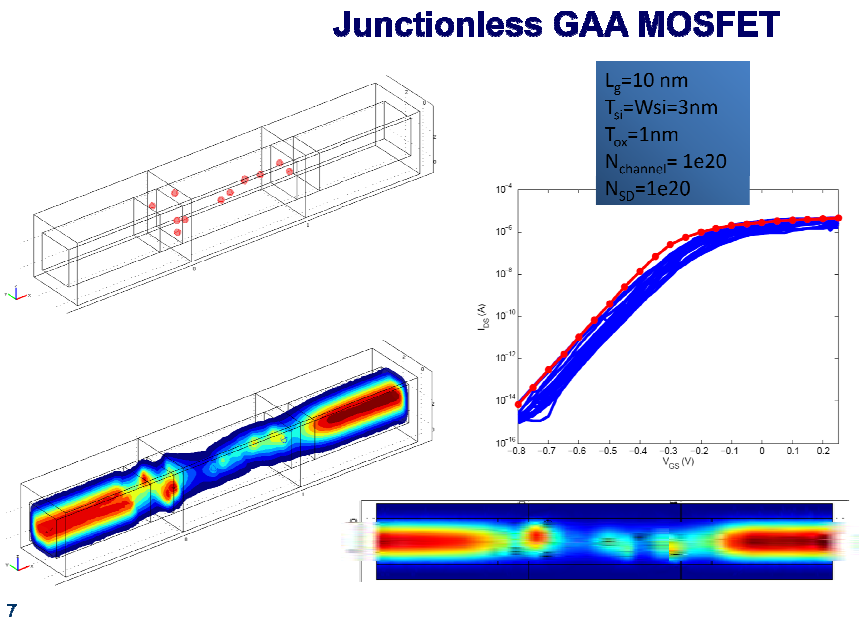
We have investigated this problem using the Poisson/NGEF simulator developed at Tyndall (and being implemented in the Magwel software).

We have simulated a gate-all-around (GAA) inversion-mode nanowire transistor with undoped channel, in which 3 doping atoms have diffused randomly from the source and from the drain into the channel, at a distance up to 2 nm. The gate length is 10 nm. The graphs below show (counter-clockwise, starting at the top left): an example of doping atoms from source and drain in the channel; the electron concentration in the device (3D); the electron concentration in the device (2D cut plane); the resulting

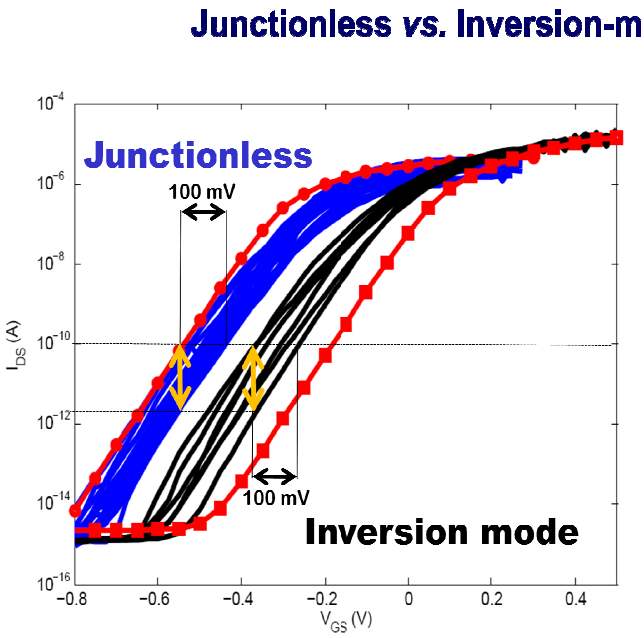
$I_D(V_G)$ curves at V_D=50 mV. The red curve is calculated in the absence of any diffusion of source and drain impurities in the channel; the blue curves correspond to different random positioning distributions of the 6 (3 + 3) dopant atoms from the source and drain in the channel.



We have also simulated a gate-all-around (GAA) junctionless nanowire transistor with a doping concentration of 10^{20} cm^{-3}, in which the channel doping atoms are placed randomly. The gate length is 10 nm. The graphs below show (counter-clockwise, starting at the top left): an example of doping atoms from source and drain in the channel; the electron concentration in the device (3D); the electron concentration in the device (2D cut plane); the resulting $I_D(V_G)$ curves at V_D=50 mV. The red curve is calculated by replacing the discrete doping atoms by a "uniform" charge concentration of 10^{20} cm^{-3}; the blue curves correspond to different random positioning distributions of the dopant atoms in the channel.



Comparing the simulation results between the inversion-mode and the junctionless transistor (below), we come to the conclusion that the variation of V_{TH} and I_{ON} is smaller in the IM devices, but the variations of subthreshold slope and I_{OFF} are smaller in the junctionless transistors.



IMEP/INPG will look to the analytical modelling of JLT variability during the second year.

Task 4.3 Statistical variability: nanometrology and electrical test (IPLS)

IPLS has performed the TEM cross sections on prototype devices made at TNI-UCC. This is going to help us to develop a protocol for the nanovisualisation of the nanowires to accurately measure their thickness and width, which will feed back to task 3.2.

The prototype samples delivered to IPLS consist of a half 4-inch SOI wafer with 7 fields containing 198 devices each. These devices are junctionless transistors with single or multiple fingers and different gate lengths and nanowire dimensions. The gate oxide is 10 nm thick, covered by a 50 nm polysilicon gate.

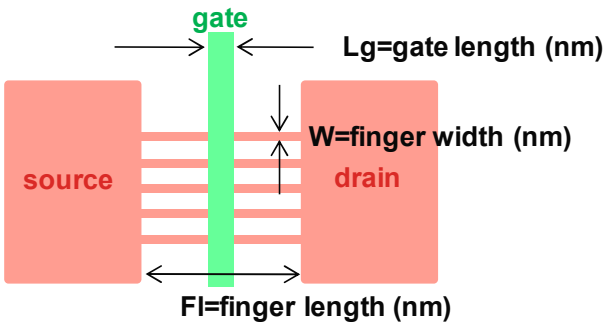


Fig. 4.3.1 Top-down of the devices with critical dimensions.

The first TEM analysis was done on a wide single nanowire transistor along the nanowire length in order to check the Silicon thickness, the effective gate length and quantify the gate undercut.

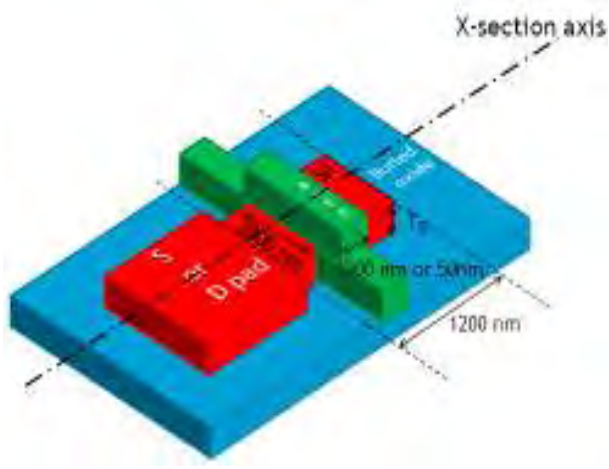


Fig. 4.3.2 Schematic of the nanowire transistor structure used for the first TEM analysis and the cross section axis.

In Fig. 4.3.3 it can be seen that the gate hasn't been fully etched, still remaining around 8nm of polysilicon. Tyndall is currently running a few test to optimise the gate etch sequence (breakthrough and softlanding times).

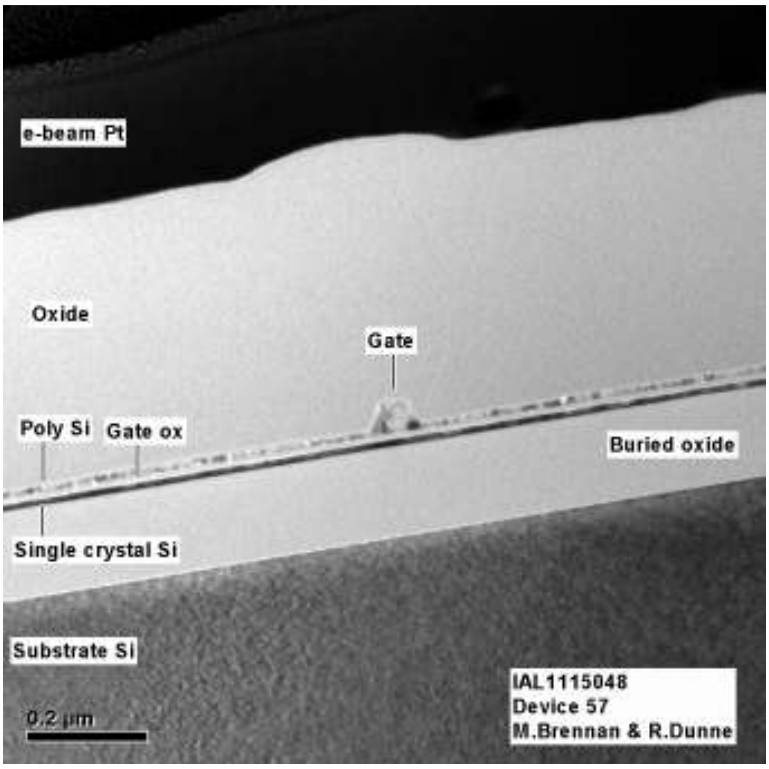


Fig. 4.3.3 TEM cross section along the nanowire showing the incomplete etching of the polysilicon gate.

The nominal gate length for the 2 devices analysed was 50 and 200nm. The resulted gates as shown in Fig 4.3.4 have a length at the base of 80 and 223nm respectively, which corresponds to 30 and 23 nm differences between the layout and the printed length respectively. The poly gate is also not showing a straight vertical profile, with a significant sidewall inclination, which would suggest an excessive polymerizing gas flow during the dry etch.

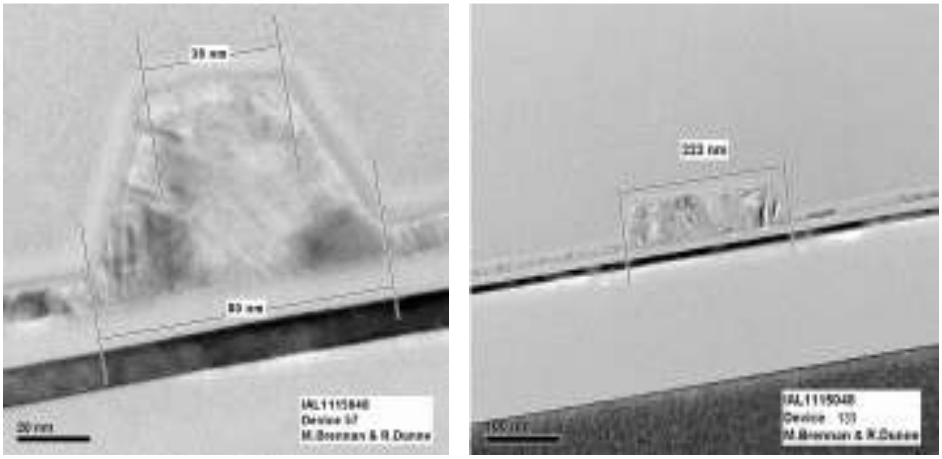


Fig. 4.3.4 HRTEM of the polysilicon gate showing the effective gate length measurements.

The second TEM analysis was done on a multiple finger transistor and cutting along the gate to measure the nanowire dimensions (Fig. 4.3.5). The structure analysed consists of 20 fingers which are 50nm wide with an expected Si thickness between 5 and 10 nm.

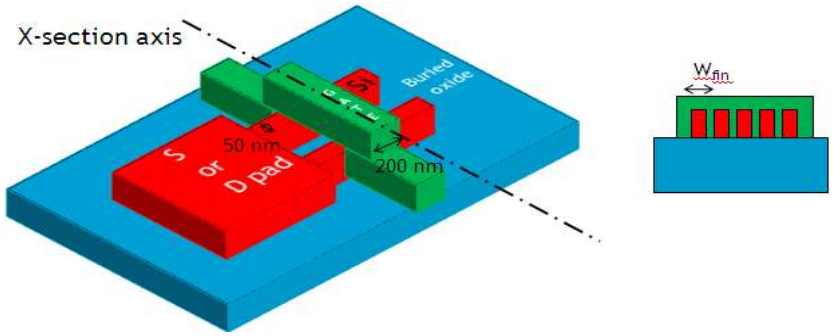


Fig. 4.3.5 Schematic of the nanowire transistor structure used for the second TEM analysis and the cross section axis.

Fig 4.3.6 shows the TEM cross section of 3 consecutive fingers. They have a dog bone type of shape (thinner in the middle), a width of 40nm and a Si thickness between 4.8 and 6.5 nm (Fig 4.3.7). The width of the rest of nanowires in the structure hasn't been measured but it was consistently uniform across the structure.

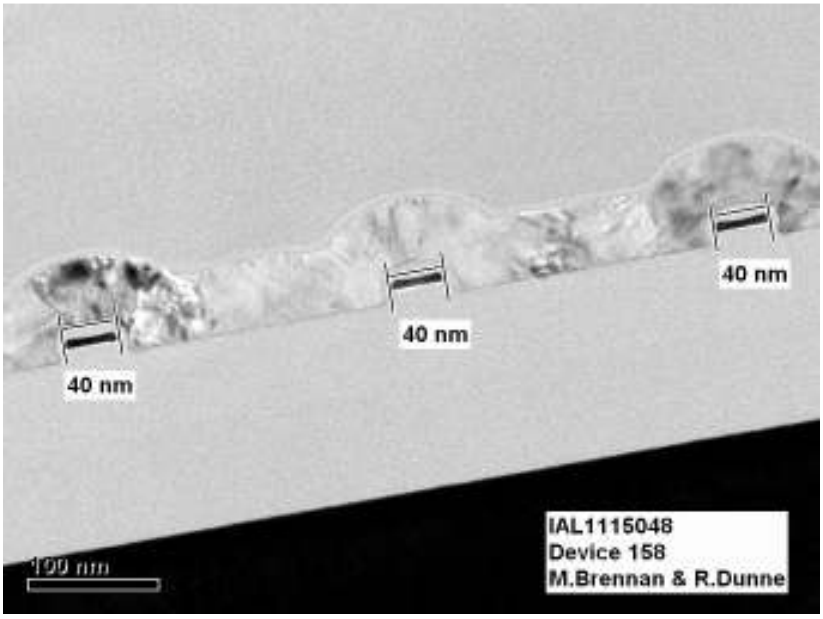


Fig. 4.3.6 TEM cross section along the gate showing 3 adjacent nanowires.

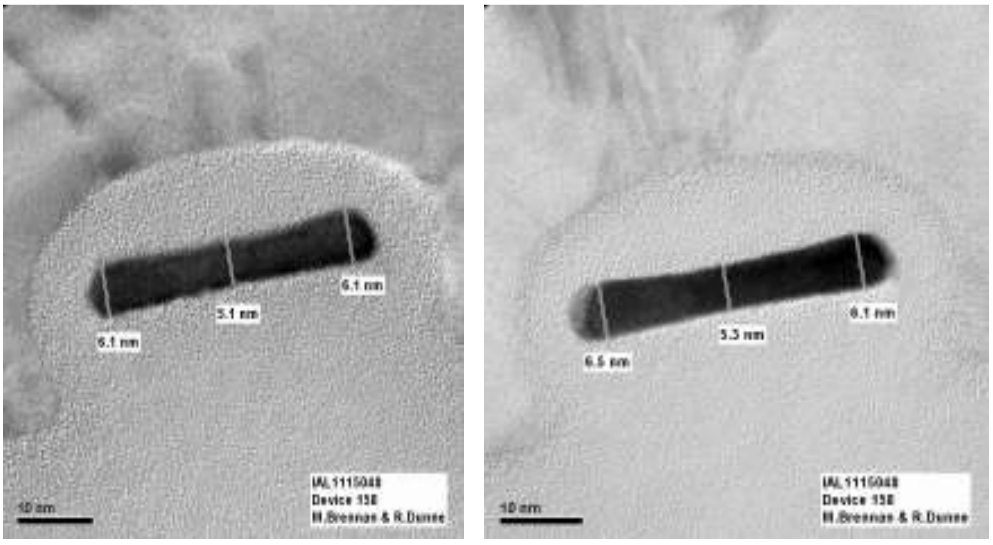


Fig. 4.3.7 HRTEM image showing the nanowire Si thickness for 2 adjacent fingers.

The polysilicon gate thickness is around 48 nm and the gate oxide thickness varies from 5.7 nm (at the edge, where is thinner) to 10.5 nm (at the centre, where is thicker) as seen in Fig 4.3.8.

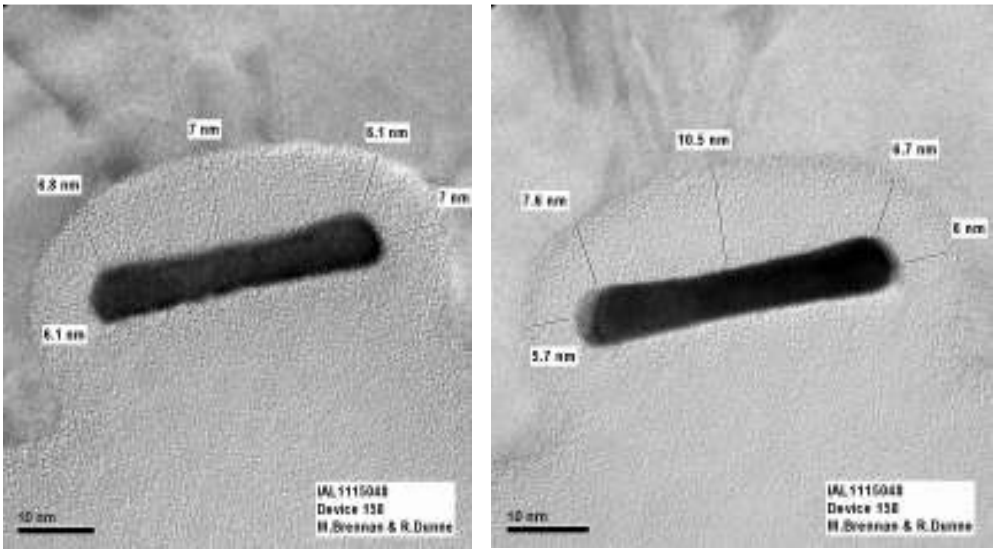


Fig. 4.3.8 HRTEM image showing the gate oxide thickness measurements.

Task 4.4 Integration of simulation tools (Magwel)

MAGWEL' role in SQWIRE consists of making the 3D quantum simulation tools that are (and were) developed at Tyndall and IMEC easily usable by integration of these tools in the MAGWEL device simulation environment. During the first phase of the project, the emphasis has been on defining and designing the graphical user interface (GUI) that should realize this goal. A major design concern is robustness against erroneous settings of input variables. An overview of the design decisions to address this issue is given below:

- Device loading
- Input variables
- Solution flow
- Excitation settings
- Results collection

After having identified these categories in the simulation flow, a design of the graphical user interface has been set up. During the reporting period, the design has been implemented and extensively tested. We can conclude the GUI is now fully operational and robust against faulty inputs.

Technical Aspects

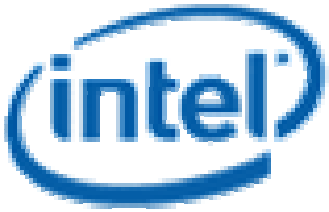
Whereas in the reporting of WP1 we have described the effort to deal with the code access from a user's perspective, in this part (WP4) we will address the code integration from an operational perspective. The challenge is to achieve sufficient computational speed combined with the flexible set up that is provided to the user by the GUI. In particular, this means that the non-equilibrium Green function formalism (NEGF) that was developed at Tyndall must be implemented in the source code environment of MAGWEL. This work is presently ongoing. We can report here on a number of technical issues that have been encountered.

The first question that needs to be answered is at which location the quantum transport modules should be activated. Since the MAGWEL software deals primarily with the drift-diffusion model, we may use the outcome of the drift-diffusion model as an initial guess for the quantum transport computation. This will be our strategy. At zero bias we determine carrier densities and potentials from a drift-diffusion simulation. These results will serve as a starting point for iterating to the NEGF solution. A second question concern variable scaling. Numerical techniques demand that the floating number ranges are pre-set in such a way that rounding errors are minimized. This demand leads to variable scaling prescriptions that transform all terms in the equation set in the numerical range close to 1. The scaling analysis has been completed.

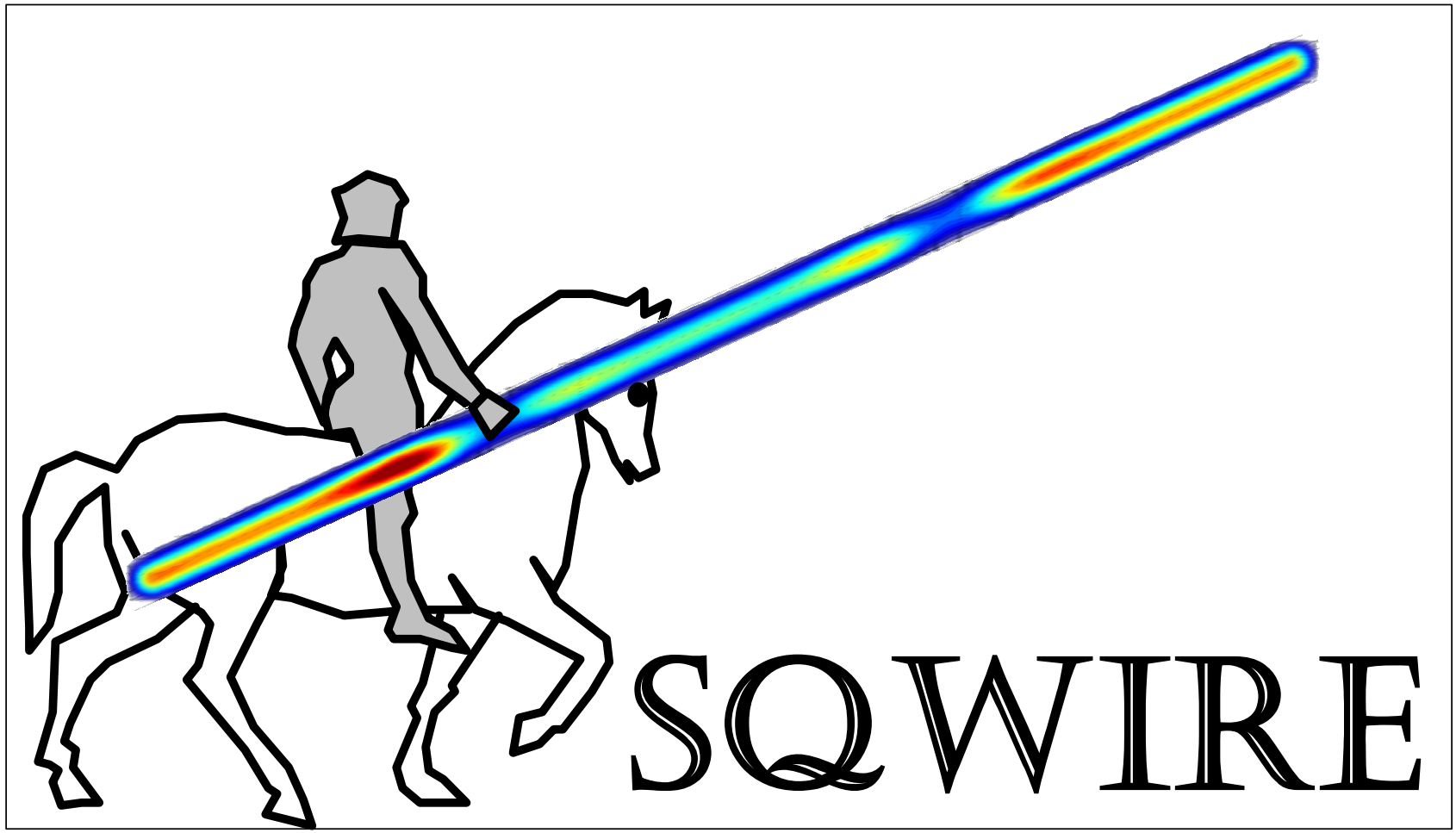
A third key step is the construction of the Green function itself. This will be done inverting the Schrodinger operator on the discretized grid. This work is presently ongoing. Since the MAGWEL solver is ab-initio design to deal with magnetic fields as possible ingredients, the discretization will account for this possibility. Finally the computation of the Green function itself requires powerful linear solvers. For this reason we have integrated some state-of-the-art linear solvers in the MAGWEL environment. In particular for linear solving we have integrated the UMFPACK library (University of Florida) and the Jacobi-Davidson eigenvalue solver (University of Utrecht).

The IMEC software for dealing with analytically based quantum transport computation has been transferred to MAGWEL. The integration of this code is less laborious as the Tyndall code since it is written in Fortran. By composing a series of wrappers (C++ interfaces) around it, we are able to realize the integration.

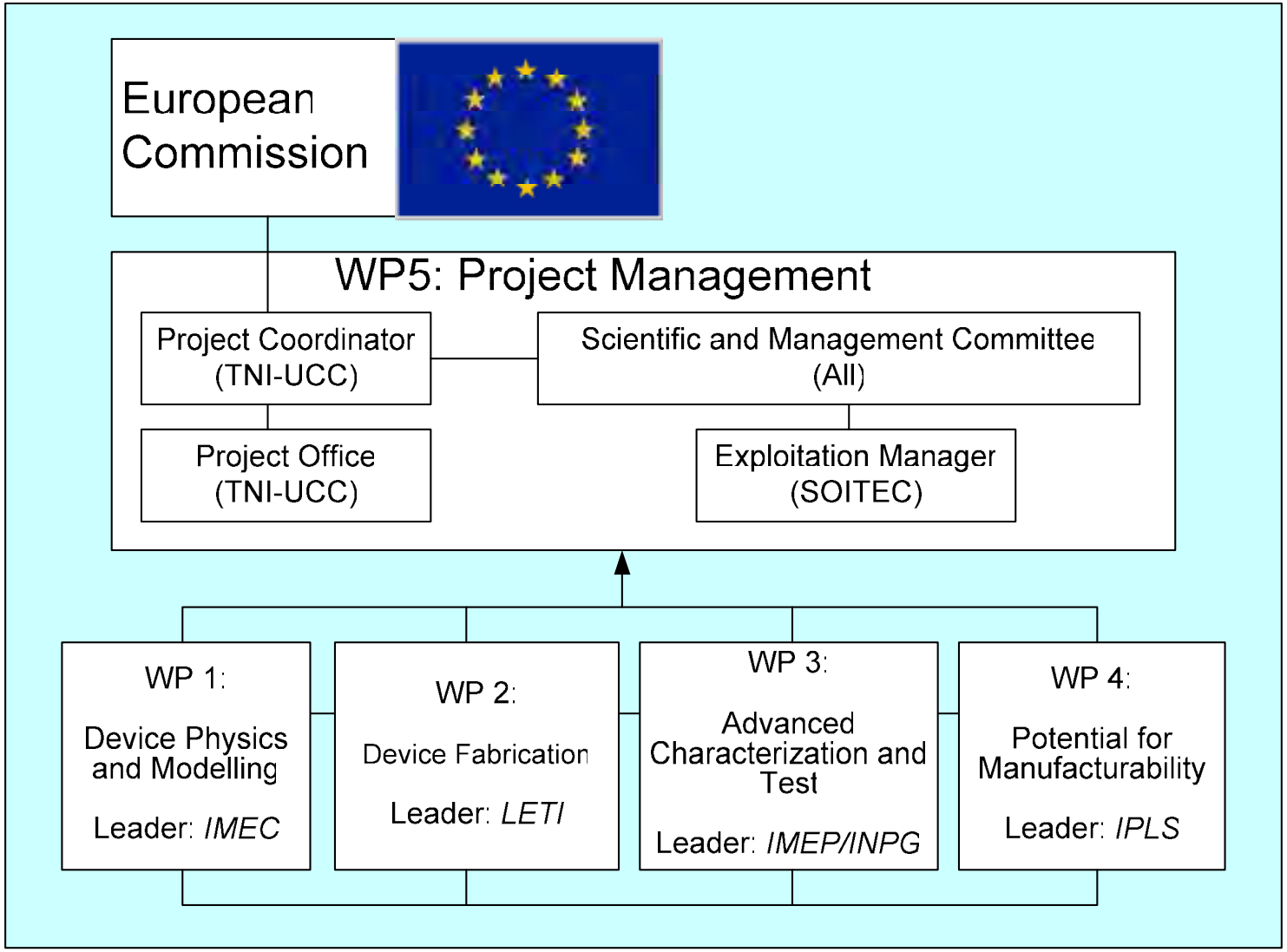
SQWIRE: Silicon Quantum Wire Transistors



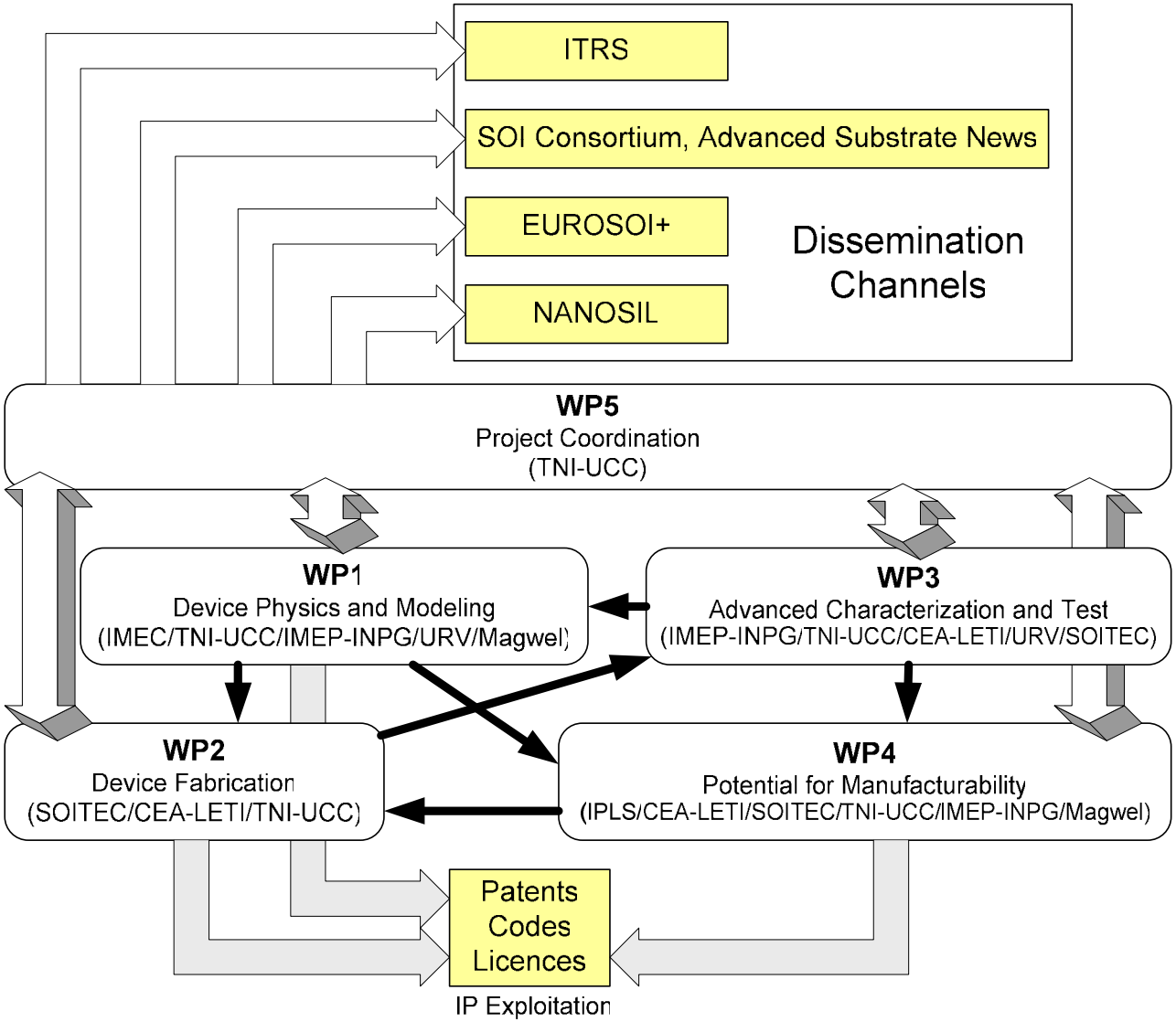
SQWIRE Logo Contest



Management Structure



PERT Diagram



Milestones and Deliverables

SQWIRE	1. Tyndall-UCC-SR	1. Tyndall-UCC-NT	1. Tyndall-UCC-ET	2. IPLS	3. CEA-LETI	4. IMEP/INPG	5. IMEC	6. URV	7. SOITEC	8. MAGWEL	Totals	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12
WP1 Device Physics and Modelling	**8**			**0**	**0**	**21**	**22.5**	**42**	**0**	**8**	**101.5**												
T1.1 3D quantum simulations			6			21				4	**31.0**					D1.1					D1.4		
T1.2 Carrier transport modelling							22.5			4	**26.5**							D1.2					
T1.3 Compact model of gated resistor	2							42			**44.0**										D1.3		
WP2 Device Fabrication	**22**			**0**	**41**	**0**	**0**	**0**	**12**	**0**	**75.0**												
T2.1 Fabrication of high-uniformity SOI wafers					21				12		**33.0**				M2.1	D2.1							
T2.2 Design & fab. of nanowire Gated Resistors	8				20						**28.0**	D2.2	M2.2		M2.4				M2.5				
T2.3 Design & fab. of nanowire Variable-Barrier Transistors	14										**14.0**		D2.3	M2.3			M2.6				M2.7		
WP3 Advanced Electrical Characterisation & Nanometrology	**31**			**2.5**	**12.5**	**27**	**0**	**0**	**0**	**0**	**73.0**												
T3.1 Electrical testing	9	3		1.5	3.5	4					**21.0**					D3.1	D3.3	M3.2					
T3.2 Nanometrology				1	9						**10.0**					D3.2		D3.4					
T3.3 Advanced Electrical Characterisation		19				23					**42.0**					M3.1		D3.5					D3.6
WP4 Potential for Manufacturability	**20**			**12**	**7**	**6**	**8**	**12**	**0**	**28**	**93.0**												
T4.1 Technology-aware design and specification				2	4			2			**8.0**		D4.1										
T4.2 Statistical variability: Simulations	7					4					**11.0**												
T4.3 Statistical variability: Nanometrology and electrical test		3		10	3						**16.0**				D4.2			D4.3					
T4.4 Integration of simulation tools			10			2	8	10		28	**58.0**												D4.4
WP5 Innovation & Project Management	**7**			**5.5**	**3**	**1**	**0**	**2**	**0**	**0**	**18.5**												
T5.1 Project Website and dissemination activities	2			4.0							**6.0**	D5.1											
T5.2 Identification, protection and exploitation of IP	1				1						**2.0**						D5.4						
T5.3 Meetings	1										**1.0**												
T5.4 Reports & cost statements	3			1.5	2	1		2			**9.5**				D5.2		D5.3		D5.5				D5.6
Total Effort (Person Months)	**88**			**20**	**63.5**	**55**	**30.5**	**56**	**12**	**36**	**361.0**												

Work Packages

Work package No	Work package title	Type of activity	Lead participant No	Person-months	Start month	End month
WP1	Device Physics and Modelling	RTD	5	106.0	1	36
WP2	Device Fabrication	RTD	3	78.0	1	27
WP3	Advanced Characterisation and Test	RTD	4	74.5	1	36
WP4	Potential for Manufacturability	RTD	2	95.0	1	36
WP5	Project Coordination	RTD	1	18.5	1	36
	TOTAL			372.0		

Milestones and Deliverables

SQWIRE	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12
WP1 Device Physics and Modelling												
T1.1 3D quantum simulations					D1.1					D1.4		
T1.2 Carrier transport modelling							D1.2					
T1.3 Compact model of gated resistor										D1.3		
WP2 Device Fabrication												
T2.1 Fabrication of high-uniformity SOI wafers				M2.1	D2.1							
T2.2 Design & fab. of nanowire Gated Resistors	D2.2	M2.2		M2.4				M2.5				
T2.3 Design & fab. of nanowire Variable-Barrier Transistors		D2.3	M2.3			M2.6				M2.7		
WP3 Advanced Electrical Characterisation & Nanometrology												
T3.1 Electrical testing					D3.1	D3.3	M3.2					
T3.2 Nanometrology					D3.2		D3.4					
T3.3 Advanced Electrical Characterisation					M3.1		D3.5					D3.6
WP4 Potential for Manufacturability												
T4.1 Technology-aware design and specification		D4.1										
T4.2 Statistical variability: Simulations												
T4.3 Statistical variability: Nanometrology and electrical test				D4.2			D4.3					
T4.4 Integration of simulation tools												D4.4
WP5 Innovation & Project Management												
T5.1 Project Website and dissemination activities	D5.1											
T5.2 Identification, protection and exploitation of IP						D5.4						
T5.3 Meetings												
T5.4 Reports & cost statements				D5.2		D5.3		D5.5				D5.6
Total Effort (Person Months)												

Deliverables - 1

Del. No.	Deliverable name	WP No.	Owner	Nature	Dissem. Level	Deliv. Date (proj. month)
D5.1	Project website, including "Consortium-only" area.	5	TNI-UCC	O	CO/PU	1
D2.2	Fabrication Process Specification for Gated Resistors	2	CEA-LETI	R	CO	3
D2.3	Fabrication Process Specification for Variable Barrier Transistors	2	CEA-LETI	R	CO	6
D4.1	Guidelines on admissible electrical parameter variation for Gated Resistors (IPLS, month 6).	4	IPLS	R	CO	6
D4.2	TEM cross sections on prototype Gated Resistors (IPLS, month 10).	4	IPLS	R	CO/PU	10
D5.2	Month 12 report		TNI-UCC	R	CO/PU	12
D3.1	Die-level electrical test protocol for Gated Resistors	3	IMEP/INPG	R	PU	13
D2.1	300 mm diameter SOI wafers with with t_{Si} = 10 nm and variation < 0.35 nm	2	SOITEC	R		14
D1.1	3D quantum simulation	1	TNI-UCC	R	PU	15
D3.2	Nanometrology protocol for Gated Resistors.	3	CEA-LETI	R	CO	15
D3.3	Gated Resistors: Nanometrology and electrical characteristics.	3	TNI-UCC	R	CO/PU	17
D5.3	Mid-term report, including first financial report		TNI-UCC	R	CO/PU	18
D5.4	Intellectual Property Audit & Workshop		SOITEC	O	CO	18

Deliverables - 2

D3.4	Nanometrology protocol for Variable Barrier Transistors.	3	CEA-LETI	R	CO	19
D4.3	Measured parameter variations for Gated Resistors, with correlation to TEM observations.	4	IPLS	R	CO/PU	19
D1.2	Carrier transport modelling	1	IMEC	R	PU	21
D3.5	Variable Barrier Transistors: Nanometrology and electrical characteristics.	3	TNI-UCC	R	CO/PU	21
D5.5	Month 24 report		TNI-UCC		CO/PU	24
D1.3	Compact model of gated resistor	1	URV	R	CO/PU	28
D1.4	User's guide for quantum simulator	1	Magwel	R	PU	30
D3.6	Detailed electrical characterisation of GR and VBT devices.	3	IMEP/INPG	R	CO/PU	35
D4.4	Manufacturability of the SQWIRE architecture based on parameter variation studies.	4	Magwel	R	CO	35
D5.6	Final report, incl. financial report and Plan for Use & Dissemination of Knowledge		TNI-UCC	R	CO/PU	36

Milestones

Mil. No.	Milestone name	WP(s) No.	Expected Date (Proj. Month)	Means of Verification
M2.2	Existing mask set adapted for Gated Resistor design	2	10	First Test Wafers
M2.3	Existing mask set adapted for Variable Barrier Transistor design	2	12	First Test Wafers
M2.1	First 300 mm wafers with 10 nm SOI thickness delivered to CEA-LETI.	2	12	TEM
M2.4	1st run of Gated Resistors delivered to partners	2,3,4	12	
M3.1	Preliminary nanometrology and electrical test data fed back to CEA-LETI as initial inputs for adjustment of process conditions for 2nd Gated Resistor fabrication run.	2,3	15	
M2.6	1st run of VBT delivered to partners	2,3	16	
M3.2	Preliminary nanometrology and electrical test data fed back to CEA-LETI as initial inputs for adjustment of process conditions for 2nd Variable Barrier Transistor fabrication run.	2,3	19	
M2.5	2nd run of Gated Resistors delivered to partners	2,3	24	
M2.7	2nd run of VBT delivered to partners	2,3	28	

Work Package 1: Device Physics and Modelling

WP Leader: IMEC

3D quantum simulations (TNI-UCC, IMEP/INPG, IMEC, Magwel**)**

Building on exisiting research capabilities in nanoscale device simulators, TNI-UCC will develop three-dimensional simulators that combine Poisson and Schrödinger solvers, *i.e.* Non-Equilibrium Green's Functions. These are essential for prediction of the electronic properties of nanowire devices with critical dimensions below 10 nm. Existing commercially available simulators cannot handle quantum effects such as tunneling, which are essential for the simulation of the novel Variable Barrier Transistor devices with sub-60 mV subthreshold slope, which will developed within SQWIRE. The software code developed at TNI-UCC will be benchmarked against existing IMEP/INPG and IMEC simulators.

The Non-Equilibrium Green's Function formalism will be implemented in the Magwel commercial simulation package, targeting development of a software tool with a state-of-the art Graphical User Interface (GUI) that can handle quantum effects. The implementation will include:

- Definition of the design flow
- Integration of the software components into a modular library
- Optimization of kernels to enable ultra-efficient dimensioning of the device architectures.

Results will be compared with the outputs from Task 2.2 (below) and correlated with the experimental metrology and electrical test data from WP3 and WP4 to identify and quantify the factors influencing charge transport in sub-10 nm devices. These data will serve as important inputs to the compact model which will be developed by URV (T1.3, below).

Carrier transport modelling (IMEC, Magwel**)**

Existing simulation tools employ the accepted effective-mass approximation. However, carrier transport in nanowires differs from that in bulk silicon: the energy gap, energy-momentum (*E-k*) relationships and effective masses depend on the device cross-section geometry and the crystalline orientation of the channel. Further, the degree of ballisticity and the carrier reflection coefficient at the drain also depend on the device geometry. It is important to understand these effects and their influence on device performance.

In parallel to Task 2.1, IMEC will develop models for carrier transport in nanowire devices using appropriate energy-momentum relationships and effective mass tensors. Results will be iteratively fed back into Task 2.1 and into WP3 and WP4 as described above.

Compact model of gated resistor (URV, TNI-UCC**)**

If the Gated Resistor is to become a successful successor to current CMOS devices, the need will arise for a compact model of it for use in circuit simulators. We will develop such a compact model, based on the expertise developed at URV in the field of nanowire and accumulation-mode transistor modelling. The compact model will be validated by comparison with 3D quantum simulations (T1.1 & T1.2) and, after parameter extraction, with the measurements carried out in WP3. Electrical parameters extracted from both simulated and fabricated Gated Resistors will be gathered by TNI-UCC and supplied to URV for calibration and benchmarking of their model. These data will be complemented by "fine-tuning" measurements done at URV. Using Verilog-A, the compact model will be implemented and tested in circuit simulators.

Work Package 2: Device Fabrication

WP Leader: LETI

Fabrication of high-uniformity SOI wafers (SOITEC)

Initial simulation work has shown that the control of device parameters such as threshold voltage and current drive of Gated Resistors are strongly dependent on the thickness of the silicon layer used to fabricate the nanowires/nanoribbons. SOITEC is currently able to produce SOI wafers with a silicon film thickness (t_{Si}) of 20 nm and a thickness variation of less than 1 nm ($\sigma\_ t_{Si} = 0.35$ nm). Within SQWIRE, SOITEC will push the limits of this control towards the single atom level in order to produce 300 mm diameter SOI wafers with $t_{Si} = 10$ nm and a thickness variation of less than 0.35 nm ($\sigma\_ t_{Si} = 0.15$ nm).

Design and fabrication of nanowire Gated Resistors (CEA-LETI, TNI-UCC**)**

Based on existing expertise in fabrication of SOI nanowire devices, LETI will develop fabrication routes for *n*-channel and *p*-channel nanowire Gated Resistors. Existing mask sets will be used, with the exception of the active area level which will have to be redrawn. Particular emphasis will be placed on the control and reproducibility of the width of the nanowires. Devices with sub-22 nm gate length will be fabricated. Initial process parameter specifications will be based on inputs from TNI-UCC, arising from simulations and prototype fabrication of long-channel (1 μm) Gated Resistors.

The first run of Gated Resistor devices fabricated by LETI will employ 300 mm diameter SOI wafers from SOITEC with a silicon film thickness (t_{Si}) of 20 nm. Silicon thinning processes will developed to reduce the film thickness to 10 nm by oxidation and oxide stripping. The second run will employ SOITEC 300-mm SOI wafers $t_{Si} = 10$ nm. Silicon thinning processes will developed to reduce the film thickness to 10 nm by oxidation and oxide stripping.

Design and fabrication of nanowire Variable-Barrier Transistors (CEA-LETI, TNI-UCC**)**

The fabrication process for Variable-Barrier Transistors is similar to that of regular transistors, the only difference being the formation of constrictions in the nanowire at the edges of the gate. Classical *npn* and *pnp* transistors will be fabricated, as well as Gated Resistors with constrictions. LETI will develop fabrication routes for *n*-channel and *p*-channel nanowire Variable-Barrier Transistors. Existing mask sets will be used, with the exception of the active area level which will have to be redrawn. Particular emphasis will be placed on the control and reproducibility of the width of the nanowires and the control of the constrictions at the edges of the gate. Initial process parameter specifications will be based on TNI-UCC's VBT simulation results.

Work Package 3: Advanced Electrical Characterisation and Nanometrology

WP Leader: IMEP

Electrical testing (IMEP/INPG, TNI-UCC, CEA-LETI, URV**)**
IMEP/INPG, in collaboration with TNI-UCC, CEA-LETI and URV, will develop agreed protocols for die-level electrical testing and parameter extraction (subthreshold slope, threshold voltage, on- and off-currents, device stability etc.). Initial measurements will be performed on prototype Gated Resistor devices fabricated at TNI-UCC, which will be delivered to the other partners at the beginning of the project.
SQWIRE will aim at achieving subthreshold slopes of 60 mV/decade and to demonstrate values as low as 56 mV/decade in VBTs. The leakage current of a device being exponentially dependent on the subthreshold slope, any improvement of the subthreshold slope, even modest, translates into substantial energy savings at the circuit level. For example, in a MOS device with a threshold voltage of 0.3V, an improvement of the subthreshold slope from 60 to 57 or 56 mV/decade brings about a reduction of leakage current by 45% and 55%, respectively (assuming room temperature operation).
Nanometrology (CEA-LETI, SOITEC, IPLS**)**
The nanoscale devices fabricated within the SQWIRE project will, however, require advanced physical and electrical characterisation. Protocols for nanovisualisation (Focused Ion Beam sectioning and Transmission Electron Microscopy, UV/optical and Atomic Force Microscopy film thickness and roughness measurements) will be developed by CEA-LETI and IPLS to accurately measure the thickness and width of the nanowires and assess the influence of processing on nanowire geometry and constriction formation. SOITEC will also employ these techniques to characterise the (atomic-scale) thickness uniformity of the SOI wafers used as starting material. Results will be fed back to both fabrication and simulation WPs.
Advanced Electrical Characterisation (IMEP/INPG, TNI-UCC**)**
Because of the emergence of quantum effects that affect the carrier transport in devices with the dimensions under consideration, sophisticated electrical characterisation techniques such as low-temperature characterisation and magneto-transport measurements will be performed by IMEP and TNI-UCC in order to extract parameters such as mobility and ballisticity. The measured parameters will be fed into the device models and simulators developed in WP1. In addition, IMEP/INPG will investigate interfaces effects using current Deep-level Transient Spectroscopy, (trans)conductance techniques and low-frequency noise measurements.

Work Package 4: Potential for Manufacturability

WP Leader: IPLS

Technology-aware design and specification (IPLS, CEA-LETI, SOITEC**)**
The fabrication process of Gated Resistors is simpler than that of regular transistors because there are neither junctions nor doping gradients. However, the control and reproducibility of device parameters such as threshold voltage and current drive will be a function of the thickness and width of the nanowires/nanoribbons. The compatibility between CMOS design requirements and variability issues in Gated Resistors will be addressed. A study will be carried out to position the Gated Resistor vs. competing devices in the ITRS roadmap.

Statistical variability: Simulations (TNI-UCC, IMEP/INPG**)**
The performances of the Gated Resistors and Variable-barrier transistors will be estimated by simulation in order to develop technology-aware design and specifications. The statistical variability of the devices will be studied through simulations by TNI-UCC and IMEP/INPG. The variation of parameters such as silicon film thickness, nanowire width, gate oxide thickness and doping concentration will affect electrical parameters such as threshold voltage, on and off current. These simulations require to design a large matrix of parameter variations and will be carried out using classical simulation tools (Atlas/Athena) for the gated resistors. For the VBT, where quantum tunnelling plays a crucial role, the quantum simulation tools developed at TNI-UCC and IMEP/INPG will be used.

Statistical variability: Nanometrology and electrical test (IPLS, CEA-LETI**)**
IPLS will perform TEM cross section observations on a statistically-relevant number of *n*-type and *p*-type Gated Resistor devices to correlate actual device thickness and width to measured electrical characteristics. IPLS will also study the statistical parameter variability using mass-production electrical characterisation tools on the LETI wafers. These statistical results will establish the industrial viability of Gated Resistors as successors to classical CMOS devices. Initially the TEM cross sections will be made on prototype devices made at TNI-UCC, and then on LETI-fabricated devices. Tight control of electrical parameters will require atomic-level accuracy for the silicon film thickness and the width of the nanowires. Experimental correlation tables between measured nanowire dimensions and electrical parameters such as threshold voltage will be employed to determine optimum processing windows.

Integration of simulation tools (Magwel, TNI-UCC, IMEP/INPG, IMEC**)**
The Non-Equilibrium Green Function formalism implemented in 3D simulators at TNI-UCC and IMEP/INPG, as well as the effective mass, mobility and scattering models developed at IMEC will be fed to Magwel to give it the possibility of integrating them in an industry-relevant output format that will generate value for the semiconductor industry in Europe and globally.

Work Package 5: Innovation and Project Management

WP Leader: Tyndall

Project website and dissemination activities

The project website will be established by the coordinator to publicise the goals of the project, introduce the consortium and disseminate progress to the wider scientific community, industry and the public. The website will have both public and "consortium-only" sections. The "consortium only" section will include a central repository of all relevant project documentation (including reports, minutes of meetings, drafts of publications awaiting pre-submission approval)

Identification, protection and exploitation of intellectual property

Intellectual property created within SQWIRE will be carefully identified and protected to the benefit of Europe. The protection of IP is a key issue. Nonetheless, this objective is closely related to the dissemination of knowledge and mechanisms will be implemented to ensure a sensitive balance between exploitation and dissemination. IP will be reviewed at all project technical meetings and a specific IP audit and exploitation seminar will be organised at month 18 by the co-ordinator and the exploitation manager. Specific exploitation strategies (e.g., licensing) will be established to ensure efficient exploitation of project results.

Meetings

The kick-off meeting will be organised to ensure a smooth and timely start to the project activities. In the course of the project, regular technical and management meetings will be held to monitor progress and review, update and, if necessary, modify the work flow of the project. In addition to face-to-face meetings, (either full-consortium and task-specific), telephone/video conference calls will be held regularly (every 1-2 months) to coordinate activities. The minutes and results of these real and virtual meetings will be available to the partners on the project website (see T5.1).

Reports & cost statements

The co-ordinator, together with the workpackage leaders and the partners, will ensure timely delivery of all reports (both periodic and deliverable reports) and cost statements. All partners will ensure that proper technical records, timesheets etc. are maintained to meet best practice in project management. TNI-UCC and CEA-LETI will furnish audit certificates as required.

From left to right:
Jean-Pierre Colinge (Tyndall), Wim Schoenmaker (Magwel), Geoff Walsh (Intel),
Bart Soree (IMEC), Jean-Baptiste Milon (Tyndall), Benjamin Iniguez (URV),
Sylvain Barraud (CEA-LETI), Olga Varona (Intel), Bernie Capraro (Intel), Aidan Quinn (Tyndall),
Konstantin Bourdelle (SOITEC).

Not on this picture:
Isabelle Ferain (Tyndall), Marco Pala (INPG), Ahn-Phuan Tuam (IMEC), Gerard Ghibaudo (INPG),
Vesselin Dontchev (EC), Georgios Fagas (Tyndall), Michel Hordies (EC).

SQWIRE

Minutes of the Six-Month Consortium Meeting

March 14th 2011

Authorised By: J.-P. Colinge

Confidentiality Status:
For the Attention of
Sylvain Barraud, Konstantin Bourdelle, Giorgos Fagas, Isabelle Ferain, Benjamin Iniguez, Jean-Baptiste Milon, Marco Pala, A.-T. Pham, Aidan Quinn, Pedram Razavi, Wim Schoenmaker, Bart Sorée, Olga Varona, Geoffrey Walsh.

Date (last revision): March 29th 2011

Attendees:

Jean-Pierre Colinge, Isabelle Ferain, Giorgos Fagas, Aidan Quinn, Pedram Razavi, Jean-Baptiste Milon	Tyndall National Institute
Konstantin Bourdelle	SOITEC
Olga Varona, Geoffrey Walsh	INTEL
Benjamin Iniguez	Universitat Rovira I Virgili (URV)
Wim Schoenmaker	MAGWEL
Marco Pala	INPG-LAHC
Bart Sorée, A.-T. Pham	IMEC
Sylvain Barraud	CEA-LETI

TYNDALL

- Jean-Pierre Colinge presented the general progress and accomplishments for the first 6 months of the project. All deliverables/milestones have been met in time. Recent results on Random Telegraph Noise (RTN) signals in Junctionless (JL) SOI FETs as well as some results from low-temperature measurements were presented. As could be expected, the bulk transport of JL devices gives rise to much less RTN than in surface-channel, inversion-mode devices.
- Giorgos Fargas presented some results of simulations using different constriction dimensions for Variable Barrier Transistors (VBT) and their impact on drive current and oscillations (low and room temperatures). A question was raised regarding the dimensions at which self-consistency Poisson/Schrödinger is required. JP suggested that self-consistency is needed for VBT with cross-sections below 10nm (or large biases). Details on the trip of G. Fagas and P. Razavi to Magwel were given; the goal of the trip was to start to integrate the Tyndall quantum models in Magwel's software. Some conversion of Matlab algorithms into C++ need to take place.
- **Action item for Tyndall:** organize and provide a date for a conference call at the end of June

CEA-LETI

- Silicon nanowire structures on SOI with a CD down to 10-15nm after etching have been demonstrated (nanowire width). Gate lengths down to 20nm have been obtained too. This will allow CEA-LETI to deliver JL SOI FETs with width and lengths series in the micrometer down to the nanometre range. Next process steps include the formation of nitride spacers and optimization of subsequent implants for raised source/drains. The first JL run is expected to be delivered in August 2011.

Action item for CEA-LETI: provide a detailed description of the widths/lengths considered in the layout (both on layout and after patterning). The goal is twofold: provide TNI and IMEP-LAHC a better understanding of

the structures that will be characterised; provide INTEL a sufficient number of similar devices for building statistics and variability studies. In addition a description of the split conditions (implant doses, etc.) has also been requested during the meeting.

MAGWEL

Wim Schoenmaker presented the progress of MAGWEL in the implementation of Tyndall and IMEC codes in their software. Attention was drawn on the fact that the Lorentz force effect has also been implemented in MAGWEL's software. A draft version of the GUI design was presented. A description of future work was also provided: completion of the parser, distribution for review, re-implementation of the solver components and the implementation of a wrapper around IMEC f90's code. Two deadlines agreed with MAGWEL on the software implementation:

End of April: MAGWEL to complete GUI for input variables of Tyndall software

End of June: MAGWEL to provide C++ code for the set up and solution of Eq. 12 of "A Three-Dimensional quantum simulation of Silicon nanowire transistors with the effective mass approximation", J. Wang, E. Polizzi, M. Lundstrom, J. Appl. Phys. 96, pp2192-2203 (2004).

IMEP-LAHC

Marco Pala presented some preliminary study of the carrier mobility in long-gate JL FETs following a split-CV experiment. Some concerns were raised regarding the meaning of the mobility vs. Q plot where Q is described as a depletion charge. Can the CV-split technique be used in the case of JL devices where there is NO depletion charge in ON state? JP stressed the importance of clarifying how the charge is defined in mobility studies. It was also requested to clarify what the drain bias was considered for the measurements.

IMEC

A.-T. Pham gave a presentation entitled ‘Quantum simulations of electrostatics in Si cylindrical nanowire pinch-off nFETs and pFETs with a homogeneous channel including strain and arbitrary crystallographic orientations’ (cf. ULIS proceedings).

SOITEC

Konstantin Bourdelle provided an overview of SOITEC’s products portfolio and specified which SOI wafers were provided to CEA-LETI for JL SOI FETs processing.

INTEL

Olga Varona presented a literature survey on short transistors variability. Some concerns were raised regarding CVD TiN for metal gates and local non-uniformities (orientation, composition) on the electrical properties of short-channel transistors. Note that this concern is not limited to JL devices but is applicable to all types of transistors.

It was also requested that more than 150 devices (same split condition, same dimensions) be available/wafer in order to build reliable statistics. This

condition should be fulfilled as Sylvain specified that about 250 chips/wafers are available.

JP pointed out that JL devices present a larger variability (as compared to inversion mode FETs) from a width standpoint but JL FETs are less prone to variability from an effective channel length standpoint.

URV

Benjamin Iñiguez presented his team's recent work on compact modelling. The mixed case accumulation/depletion is still under investigation. Although some simulation data involving quantum effects were requested by Benjamin, JP didn't recommend having those included as the compact modelling activity addresses JL FETs with cross-sections of 10x10 nm.

Concluding remark:

JP to provide an update on the project's website status in the coming weeks.

Next conference call:

Wednesday the 8th of June 2011

- **9.00** am – Cork-Ireland
- **10.00** am –Belgium-France-Spain
- **5.00** pm - Taiwan

MINUTES OF THE 9-MONTH CONFERENCE CALL (WEDNESDAY THE 8TH OF JUNE 2011)

Participants

1. **Tyndall National Institute, University College Cork (Tyndall-UCC):**

Giorgos Fagas, Nema Dedahsti, Jean-Baptise Milon, Pedram Razavi, Isabelle Ferain

2. **Intel Performance Learning Solutions Limited (IPLS):**

Olga Verona, Geoffrey Walsh

3. **Commissariat à l'Energie Atomique et aux Energies Alternatives (CEA):**

Sylvain Barraud

4. **Institut Polytechnique de Grenoble (IMEP-LAHC):**

Gérard Ghibaudo

5. **InterUniversitair Micro-Electronica Centrum vzw (IMEC)**:

Bart Sorée, Anton Pham

6. **Universitat Rovira I Virgili (URV):**

Benjamin Iñiguez

7. **Silicon On Insulator Technologies SA (SOITEC):**

Konstantin Bourdelle

8. **Magwel nv**:

Wim Schoenmaker

NB: Each summary below follows the order of the talks during the conference call

1. Presentation given by Isabelle Ferain (Tyndall-UCC)

- The list of next milestones and deliverables was reviewed. The next deliverable (due by the end of June) is a report on the TEM analysis of prototype gated resistors carried out by Intel. This report has been delivered on the 22nd of June 2011.
- The variability of JNT's threshold voltage as a function of its geometries has been addressed through device simulations. It was demonstrated that for narrow (silicon width below 15nm) and small (silicon thickness below 5nm) junctionless nanowire transitors (JNTs), the threshold voltage dependence on the width is limited and as small as 14mV/nm.
- Variations of the drive current I_{on} as a function of the source/drain doping gradient have also been addressed through device simulations. Discrete dopants were introduced randomly around the source and drain regions. Such dopants are defined as charges with a finite dimension (0.25nm). Provided that the JNT geometries are small enough (T_{Si}=3nm, L_g=10nm T_{ox}=1nm), it was demonstrated that JNT and inversion mode FETs exhibit similar I_{on} variations (over the same gate bias range) for a given S/D doping gradient.

2. Presentation by Bart Sorée (IMEC)

- A comparison, from a charge density perspective, between n-type Pinch-off FETs (circular JNT) and inversion mode FETs was presented. The comparison is carried out at L_g=16nm, with the same oxide thickness and work function difference (gate-channel) in both cases. The electron scattering that is considered takes into account the ionized impurity scattering, acoustic and optical phonon scattering and roughness scattering. An impurity averaging method is included which accounts for dopant fluctuation (10 dopants max.). Evidence of bulk transport in POFETs and surface transport in

inversion mode FETs was highlighted, with that difference in transport mode being caused to different charge density distributions.

- Future simulation work includes: 1. the definition, within the k.p theory, of scattering matrix elements dedicated to POFETs; 2. Implementation of quantum transport simulations based on a sub-band decomposition method within the k.p theory.

3. Presentation given by Gérard Ghibaudo (IMEP-LAHC)

- The first wafer with JNT was delivered by CEA-LETI in May. A preliminary electrical characterisation of these JNT was conducted at IMEP. The doping level in these JNT is in the order of 1e19/cm$^{3.}$ The thickness of the devices under measurement is 10nm (SOI layer) and their effective fin width is 20nm (80nm after photolithography).
- So far, the electrical characterisation involved measurements over a range of temperature from RT to 350°C. The effects of the JNT geometries (fin widths other than 20nm) haven't been investigated yet, noise measurements are on-going and a consistent set of data is expected by the end of June.
- Over the last couple of months, the modelling activity has been focused on the calibration of a discrete dopant model. The screening of ionized impurity scattering is taken into account by introducing surface roughness.

4. Presentation given by Wim Schoenmaker (MAGWEL)

- A presentation of the GUI implemented in Magwel's software solution was presented. From this interface, the user can select which methodology (*solver*) needs to be followed and what needs to be simulated (*analysis*). The options selected through the *solver* and *analysis* panels define the core of the *Quantum Transport Control Module*. A complete description of the *solver* and *analysis* options was delivered to the conference call participants. In the *analysis* part, for instance, the user can select which current direction and which crystal plane should be considered for quantum transport simulations.
- The software for quantum transport simulations is now ready for shipping to the partners from Tyndall National Institute. The API scripts needed for further integration within modules developed at Tyndall National Institute have been developed. This action item, defined in March, has been fully completed.
- Data is stored in an .xml format which can be easily shared among users. Geometrical data is saved in a layer based approach, and the structure and doping can be saved either as a picture or an .xml file.
- The writing of C^{++} code for solving transport equations with Green functions is on-going and will be ready by the end of June.

5. Presentation given by Benjamin Iñiguez (URV)

URV is currently working on a compact model for the long channel double-gate JNT (T_{Si}=20nm, L_g=1µm T_{ox}=1nm, silicon concentration varying from 1e19 to 5e19cm^{-3}). The short channel model can be obtained by adapting some parameters such as the threshold voltage. CAD device simulations were carried out for the reference. The model built by URV reproduces g_m data well and agrees well with CAD simulations.

6. Presentation given by Sylvain Garraud (CEA)

- The first batch of 300mm wafers with JNT is confirmed to be delivered in August 2011. A layout description will be delivered by the end of June. The latter will allow for the definition of the electrical measurements protocol. Each wafer offers the opportunity to test 250 dies, each of them

includes series of single or multiple-nanowire JNT, with a range of nanowire width from 10nm to 10µm and a silicon thickness of 10nm. The smallest gate length is 25nm after etching. Several doping concentrations have been considered, ranging from 5e18 to 5e19cm^{-3} (one doping condition/wafer). For the reference, inversion mode tri-gate FETs have also been processed. Full wafers will be delivered to INTEL for parametric testing.

- From the wafer delivered in May to IMEP, one can see that short channel (Lg=25nm) n-type JNTs exhibit ideal subthreshold slope and limited DIBL.

7. Presentation given by Konstantin Bourdelle (SOITEC)

SOITEC is currently able to deliver SOI wafers with an SOI layer as thin as 12nm and within-wafer uniformity below 1nm. SOITEC is using advanced characterisation techniques such as ellipsometry, Atomic Force Microscopy (and optical profilometry) to assess the thickness and surface roughness of these extremely thin SOI layers. By optical profilometry, a surface roughness below 0.05Å has been measured on ultra-thin SOI wafers. Such RMS roughness is expected to lead to limited V_t variations (ΔV_t below 25mV).

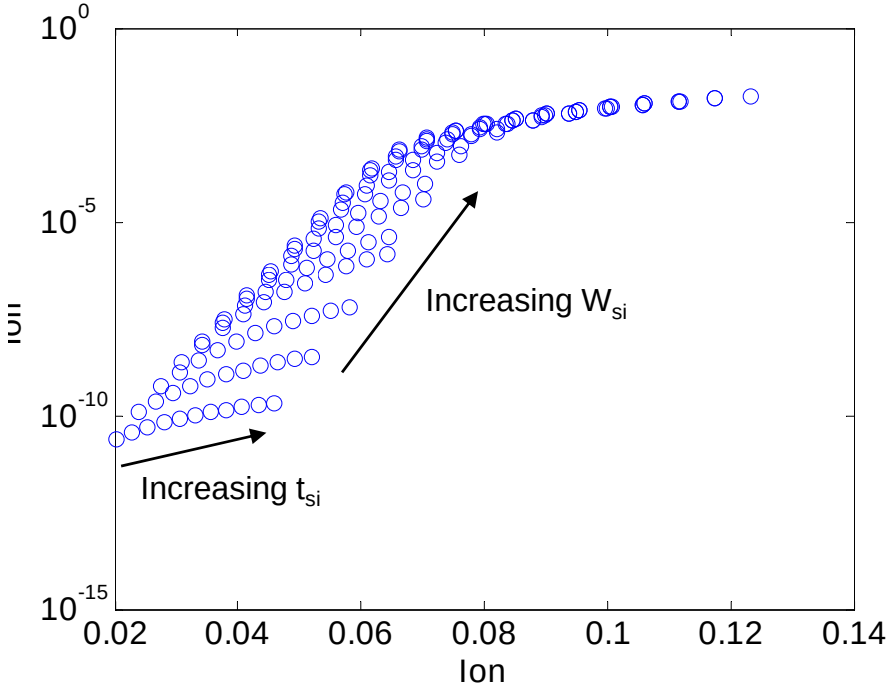
8. Presentation given by Olga Varona (IPLS)

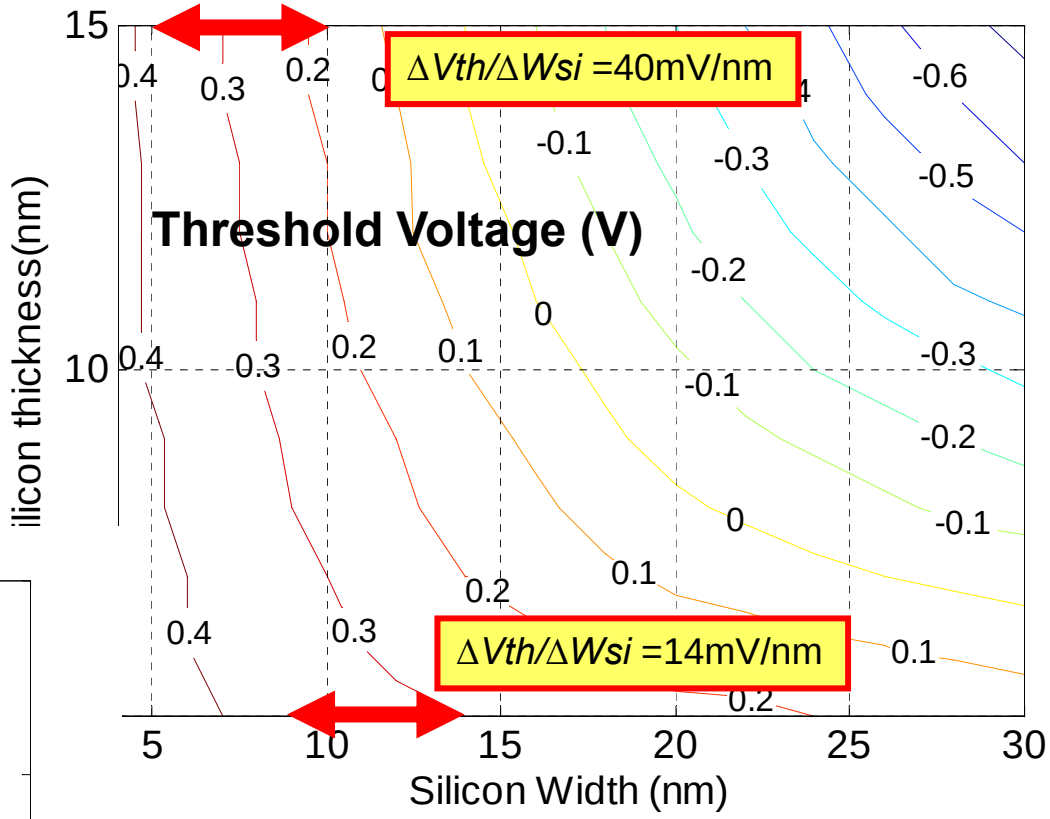
- A detailed description of a Transmission Electron Microscopy (TEM) analysis was provided. This analysis was carried out on JNT processed at Tyndall-UCC and was meant to prepare the protocol for nanometrology on the next JNT. The devices processed at Tyndall-UCC appear to have incompletely etched polysilicon gates. This process issue leads to high contact resistance as the poly-silicon is not completely removed in the contacts areas. A lateral cross-sectional TEM, from source to drain, shows that the gate profile is sloped. This effect enlarges the effective gate length after gate etching and, in turn, limits the gate length scaling. Further details on the dimensions of the constitutive elements of the JNT were also provided (gate stack dimensions, for instance)
- The definition of a protocol for electrical measurements was requested during this conference call. Following this request, another conf. call was held on 15th June which involved S. Barraud (CEA), Gérard Ghibaudo (IMEP-LAHC), Olga Varona and Geoffrey Walsh (IPLS), Aidan Quinn, Jean-Baptiste Milon and Isabelle Ferain (Tyndall-UCC). A protocol was subsequently defined (see document entitled 'Electrical Measurements - Protocol.pdf').

Next meeting will be held on Friday the 16th of September 2011 in Helsinki (Finlandia Hall).

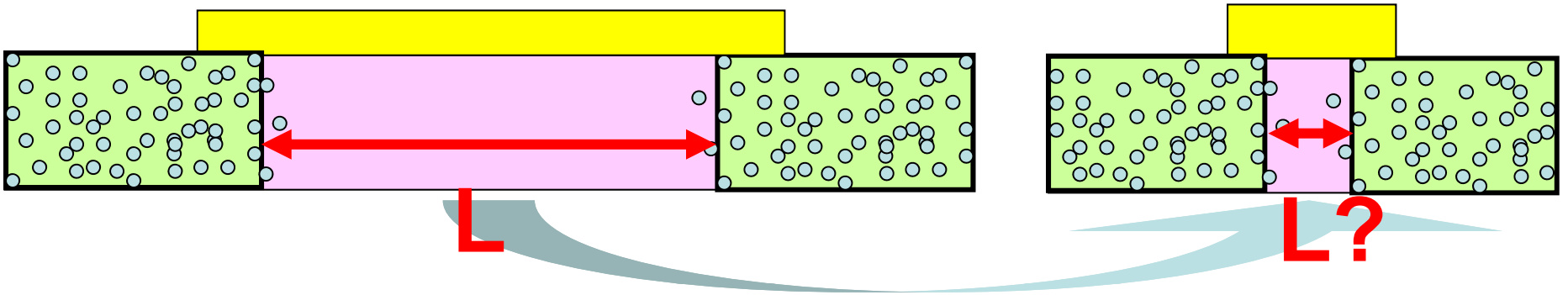
Variability

N_D=1x10^{19}cm^{-3} ;
EOT=1nm ;
Midgap gate





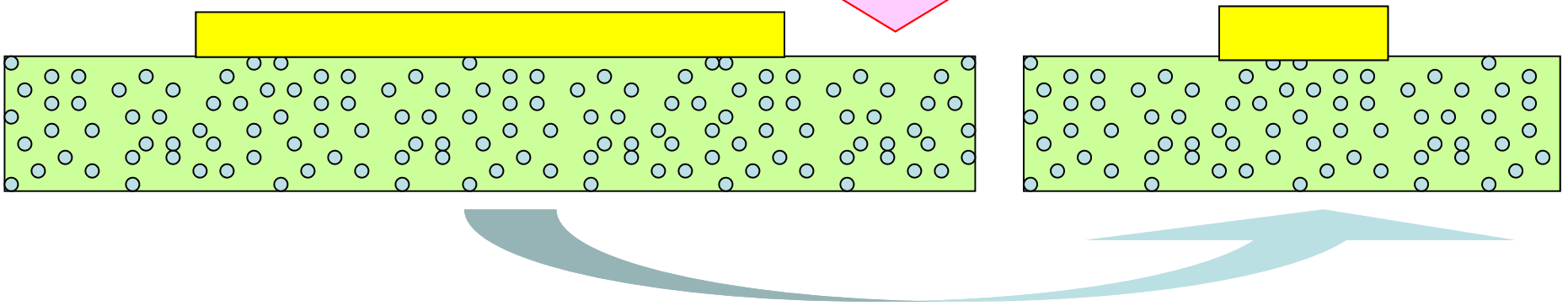
Source and drain doping: PROBLEM !



"Short channel"
(35nm)

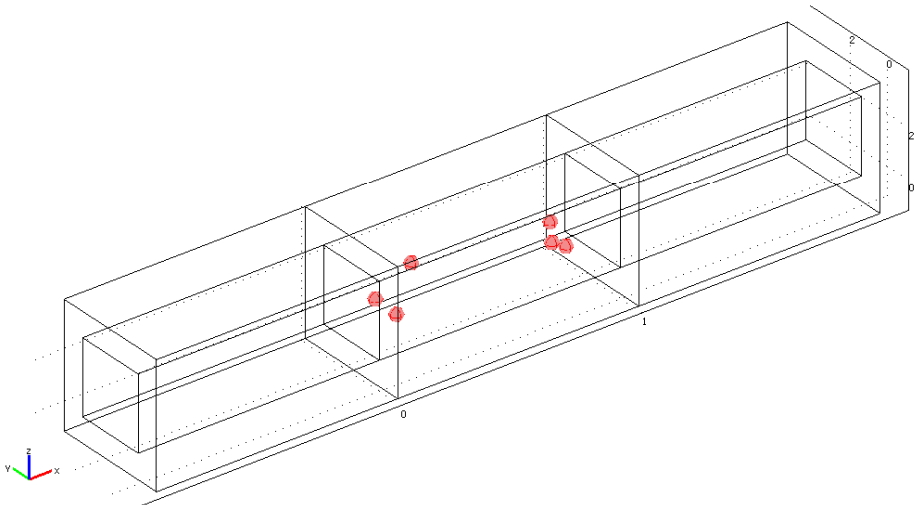
"Ultrashort channel"
(<10nm)

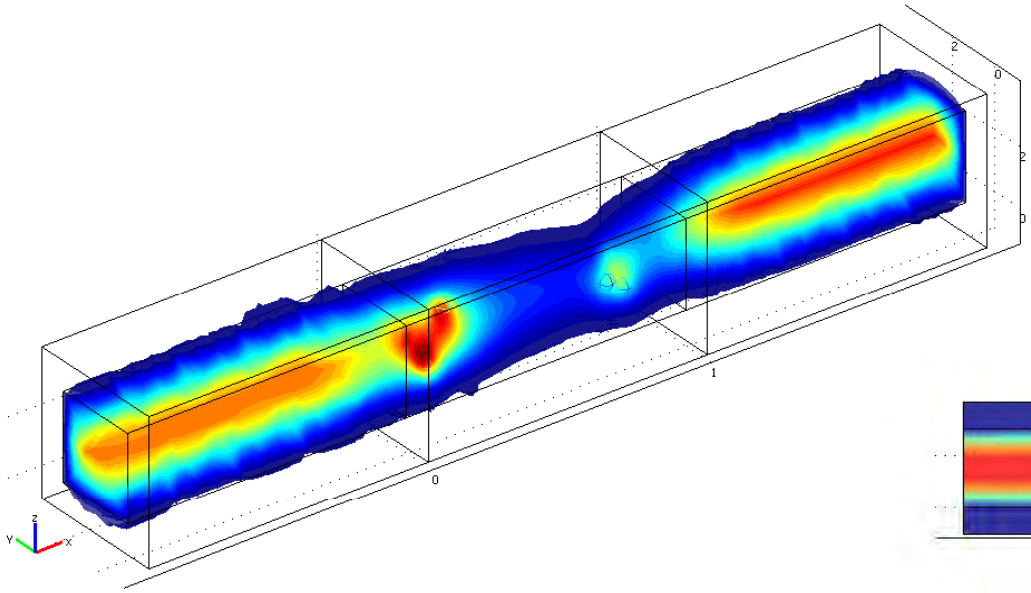
"Junctionless"



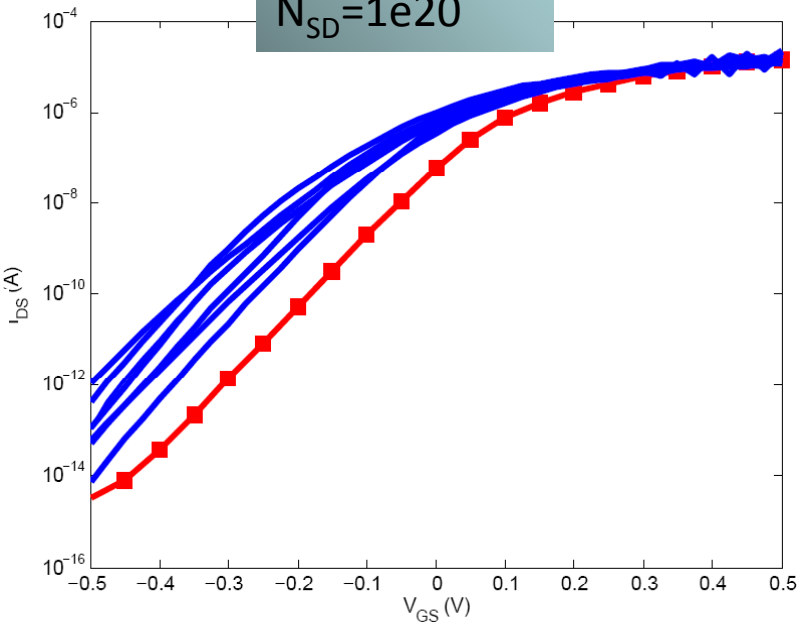
11

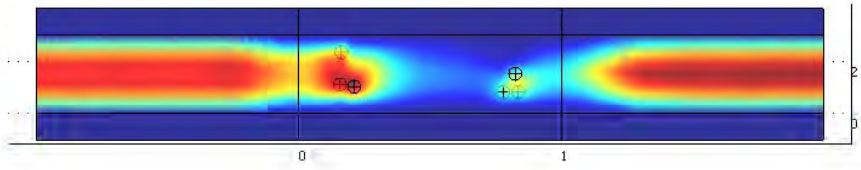
Inversion-mode GAA MOSFET





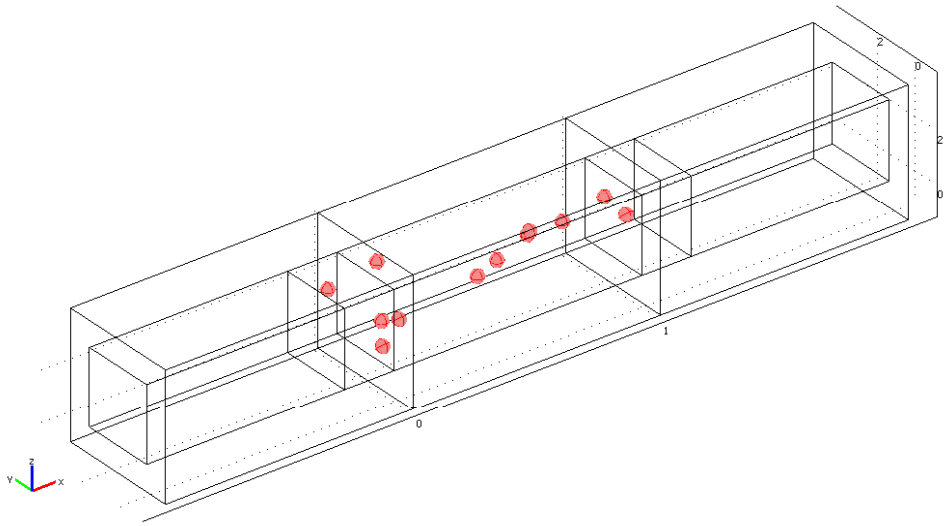
L_g=10 nm
T_{si}=Wsi=3nm
T_{ox}=1nm
$N_{channel}$= 0
N_{SD}=1e20

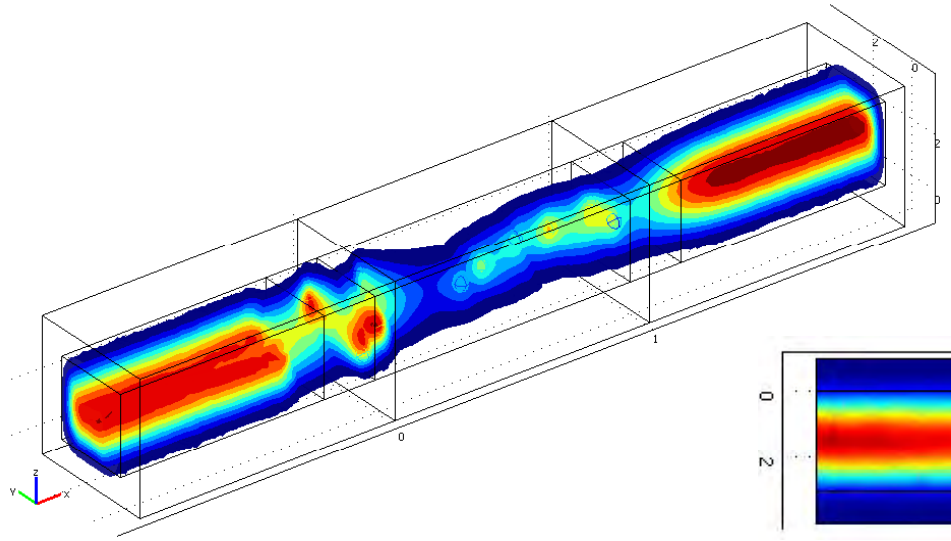


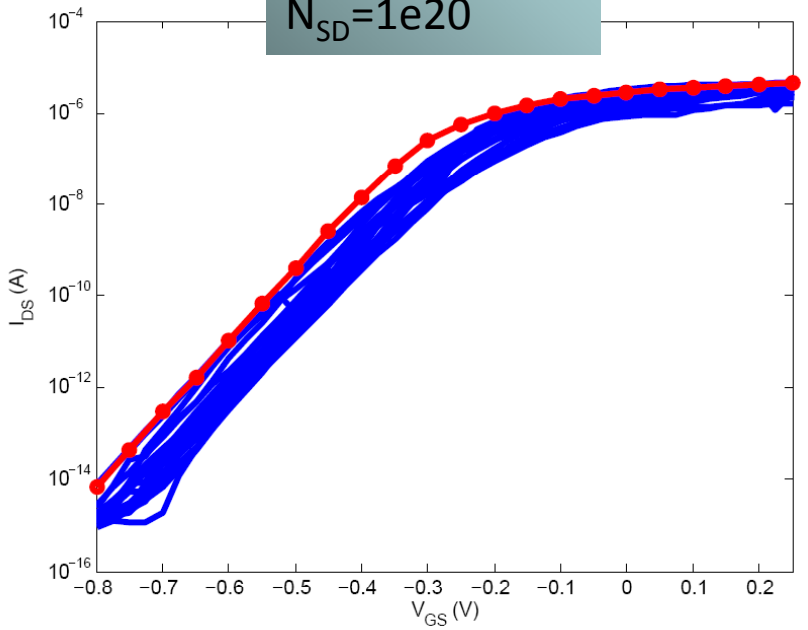


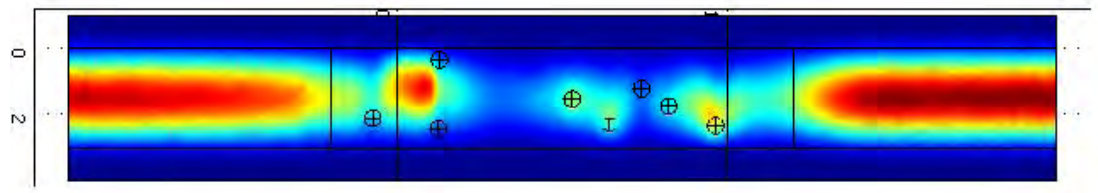
Junctionless GAA MOSFET

L_g=10 nm
T_{si}=Wsi=3nm
T_{ox}=1nm
$N_{channel}$= 1e20
N_{SD}=1e20

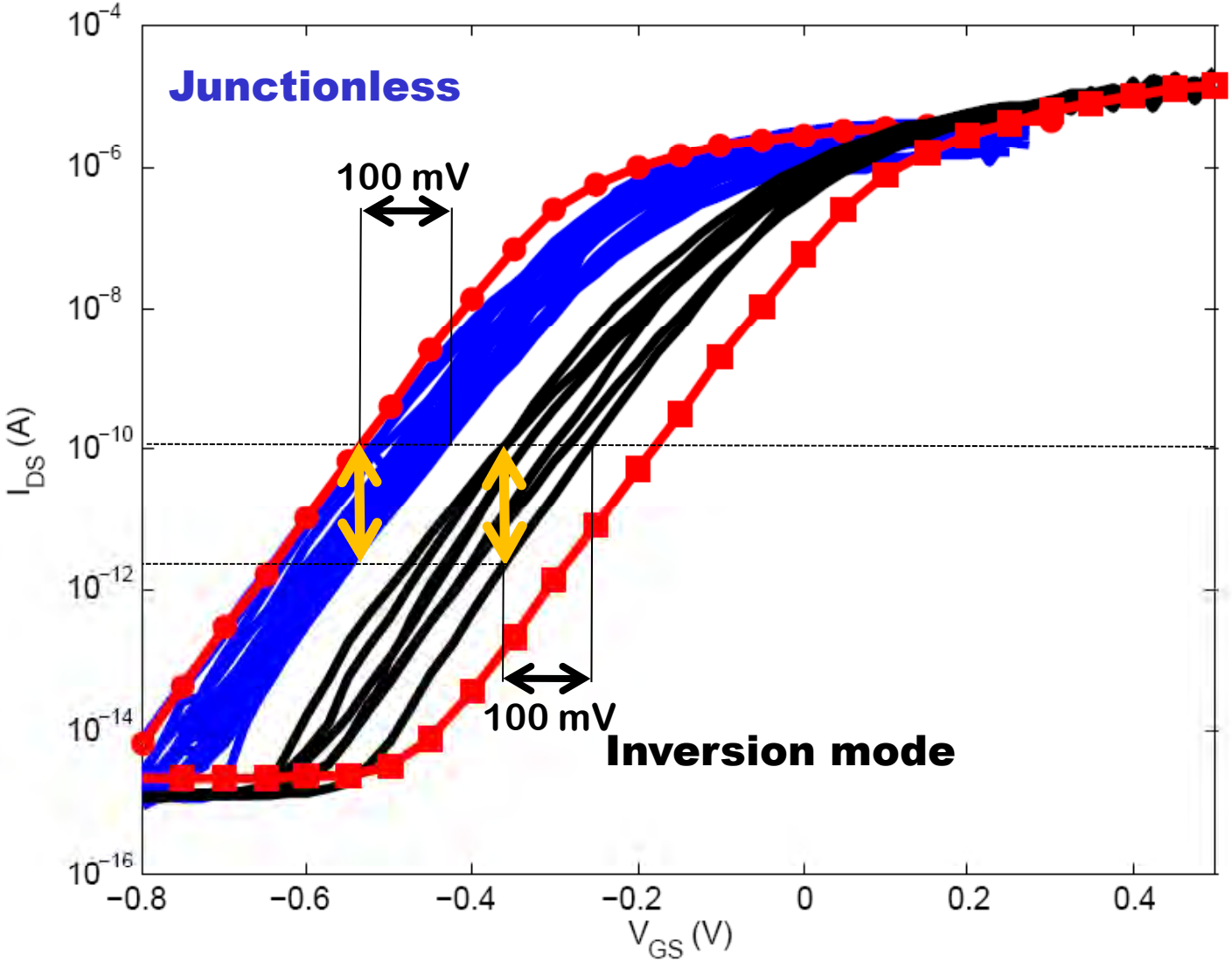




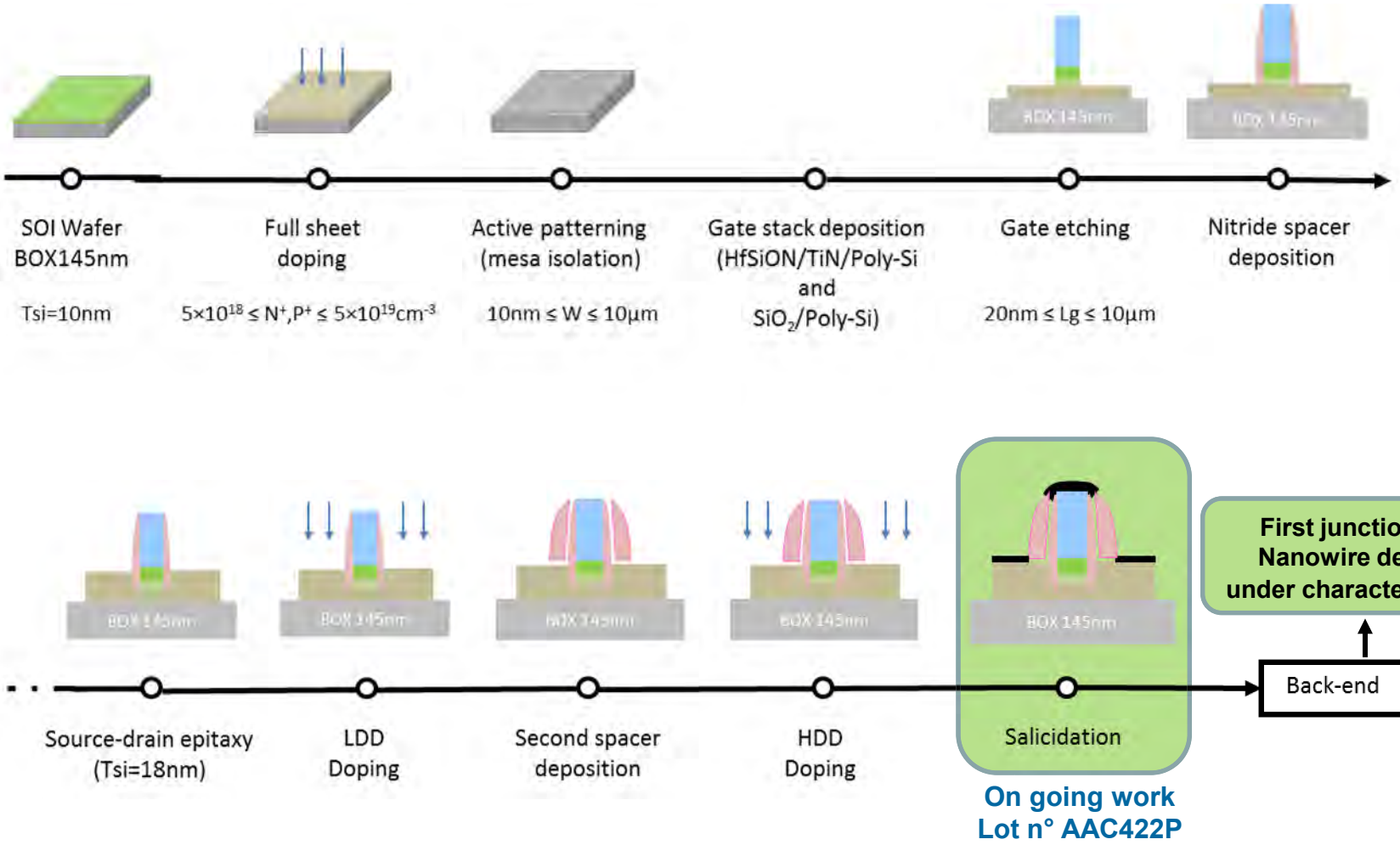




Junctionless *vs.* Inversion-mode



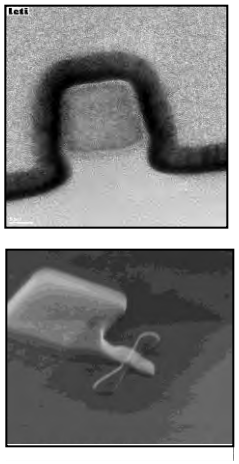
Fabrication process for junctionless NW

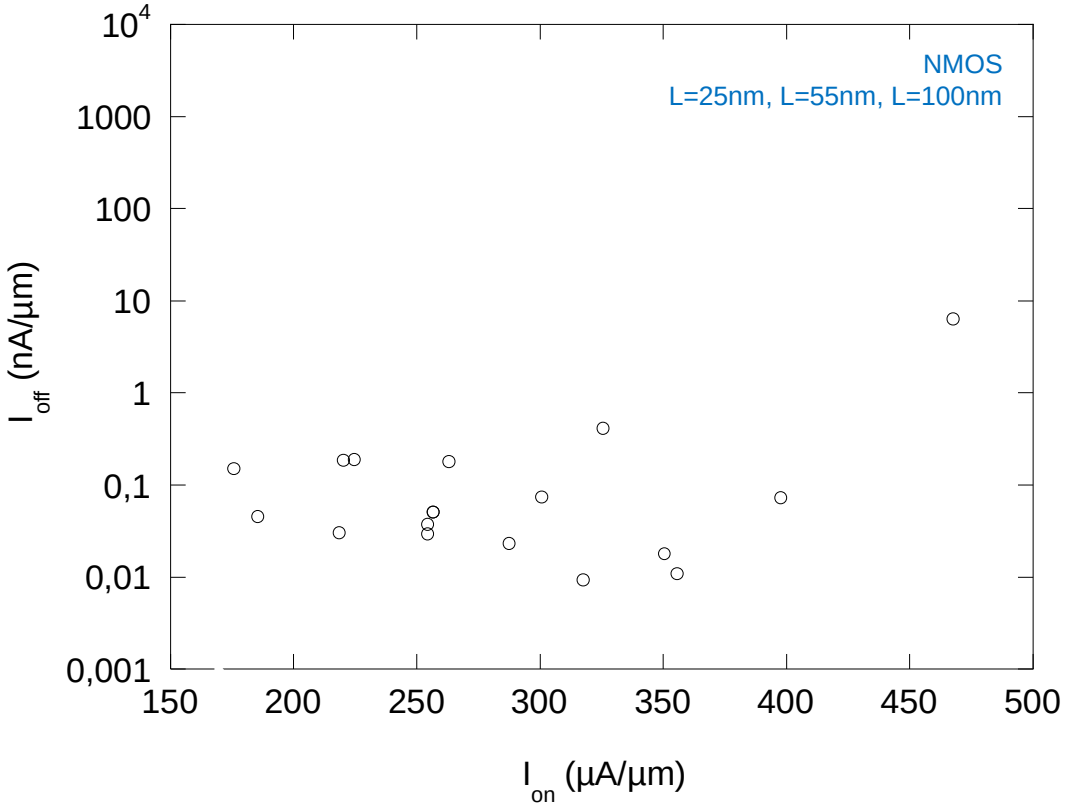


Fabrication process for junctionless NW

Ioff-Ion plot of *junctionless* nanowire transistors

Tri-gated Si nanowire
Width=20nm

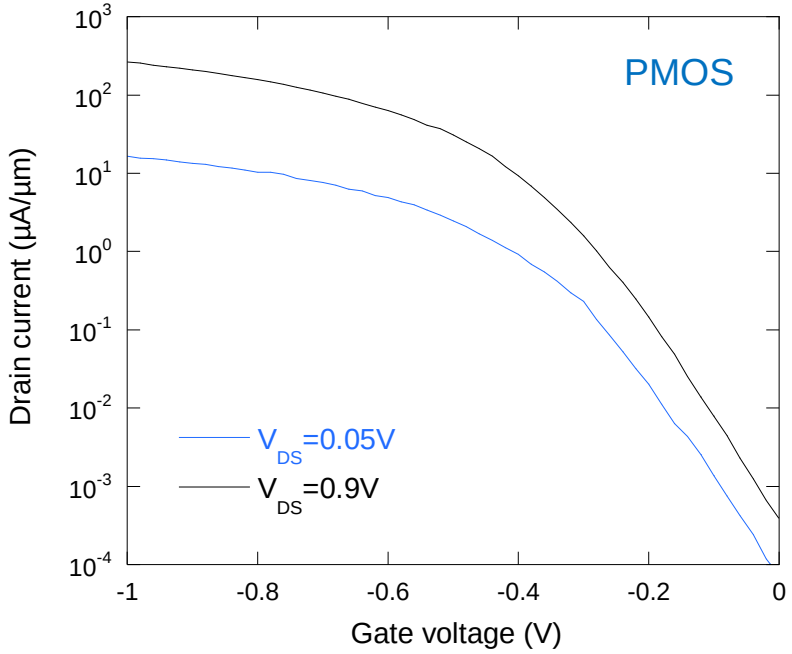




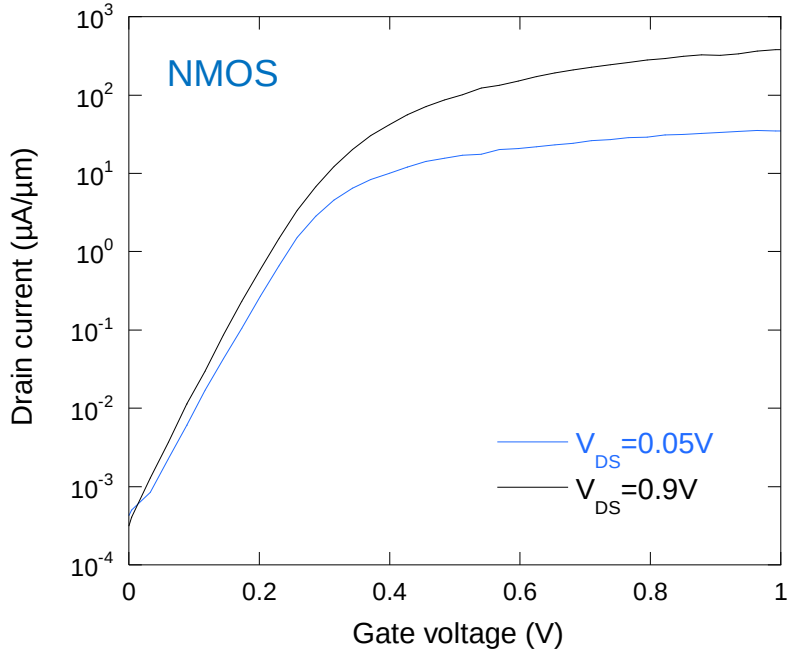
Fabrication process for junctionless NW

Current-voltage characteristics of *junctionless* nanowire transistors

L~25nm



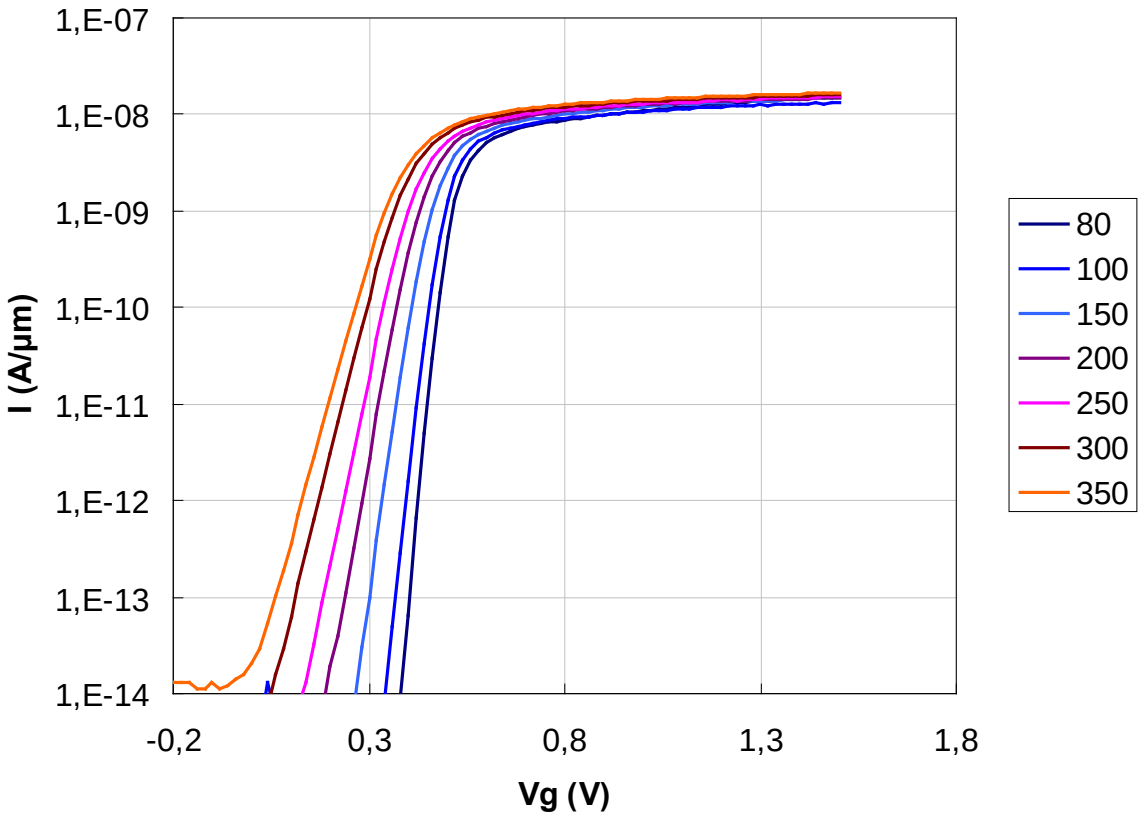
Ion=206 µA/µm @ V_{GS}=V_{DS}=-0.9V
Ioff=0.38nA/µm @ V_{GS}=0V and V_{DS}=0.9V
SS=75mV/dec



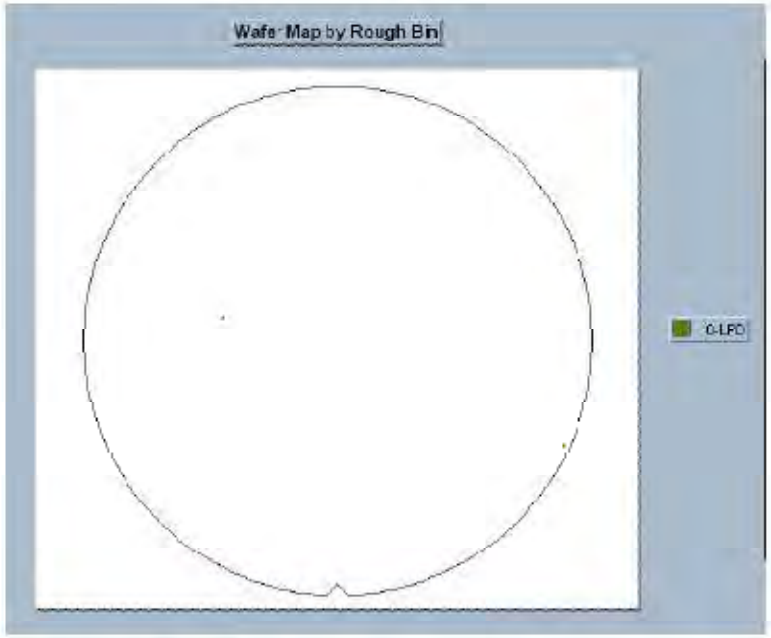
Ion=280 µA/µm @ V_{GS}=V_{DS}=0.9V
Ioff=0.36nA/µm @ V_{GS}=0V and V_{DS}=0.9V
SS=60mV/dec

WP3: Advanced electrical characterization
(D. Jeong, M. Mouis)

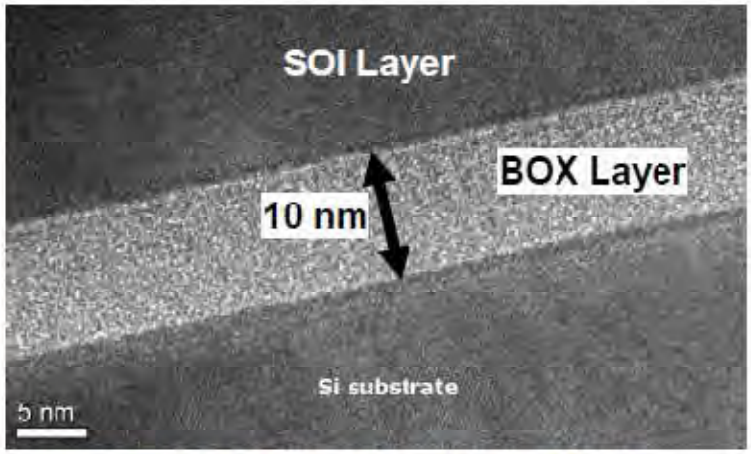
LETI JLT/FD-SOI (W=80nm), L=100nm, T variable)



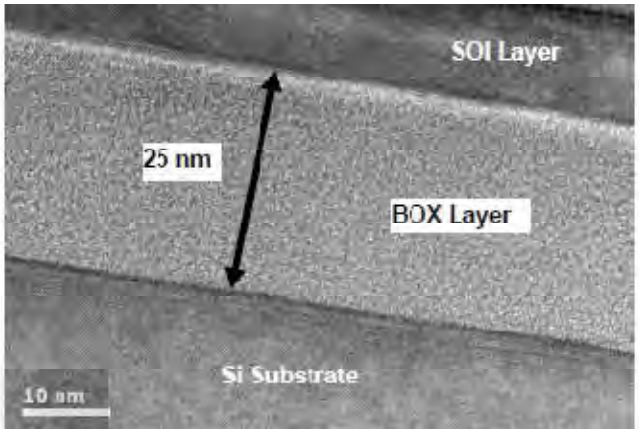
UTBB substrates



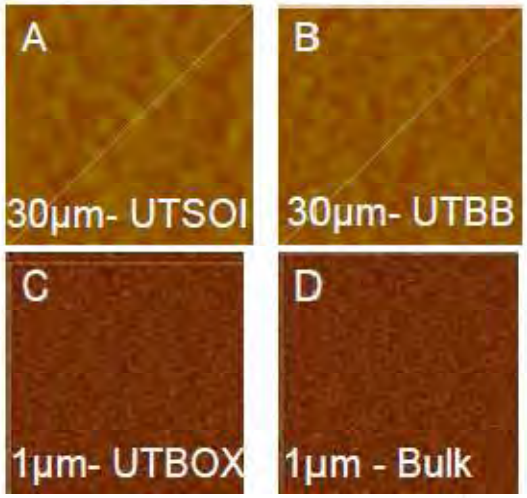
UTBOX25 defectivity map SP2
@ 90nm threshold



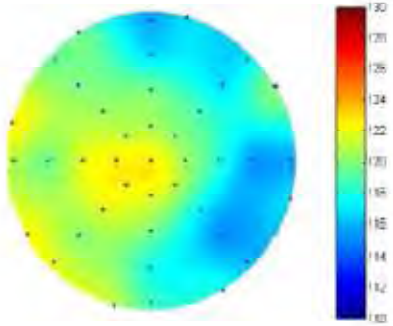
UTBOX10 & UTBOX25 TEM
cross section



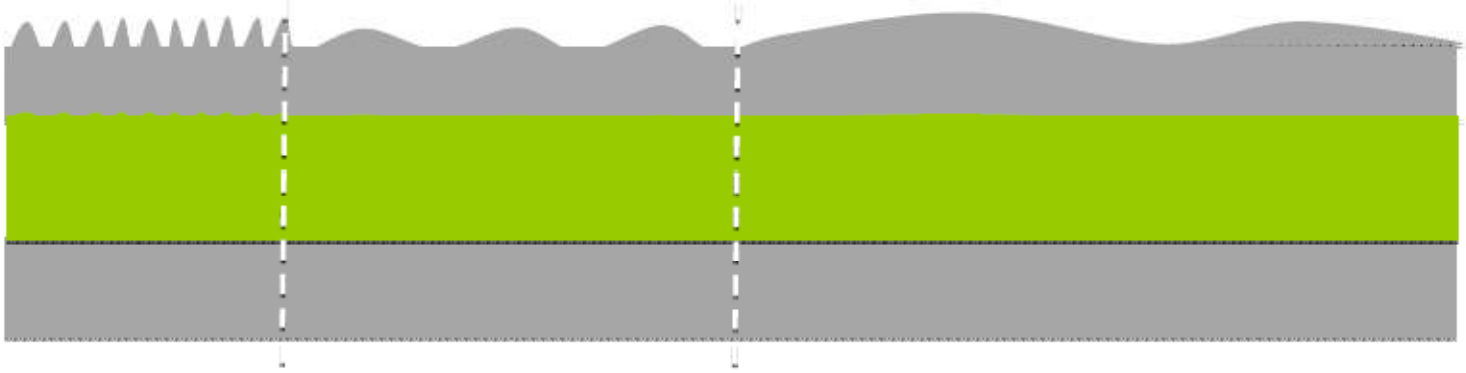
Thickness Contributions



Roughness
<2Å RMS

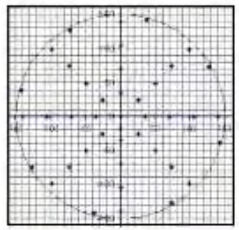


Optical Profilometer
RMS=0.05 Å
100µm scan



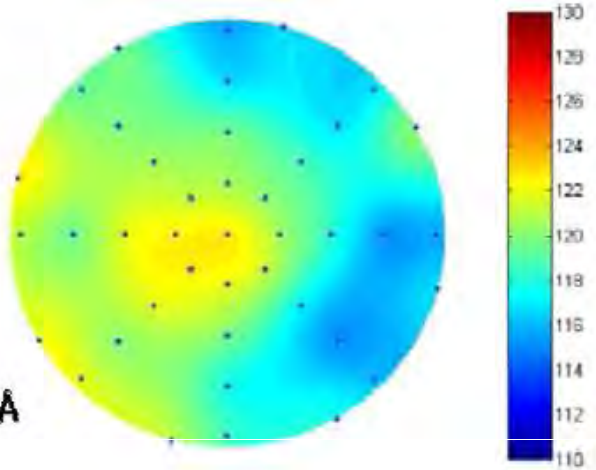
- Thickness control is ensured for all frequencies

Within-the-wafer Uniformity Performance

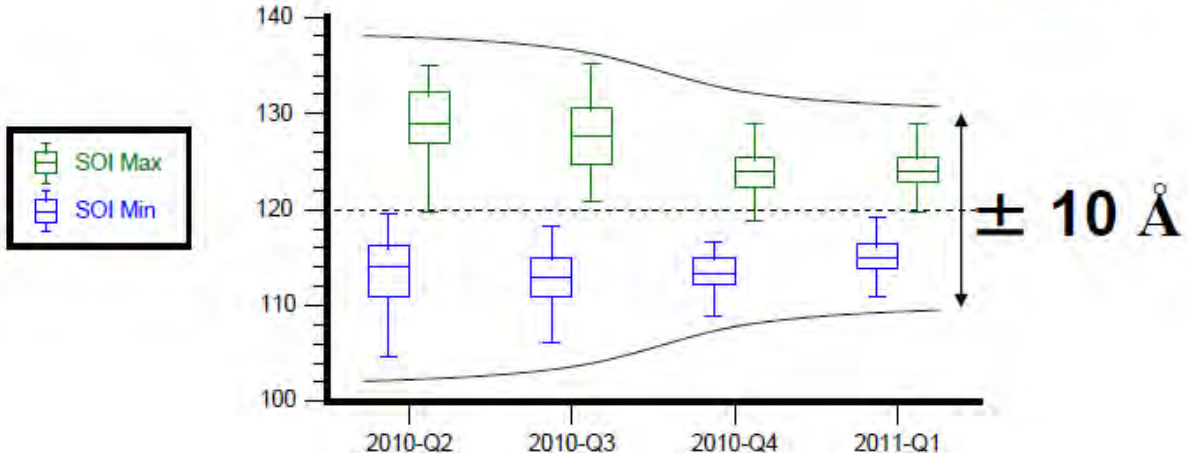


Thickness Measurement
Ellipsometry mapping

F5X Ellipsometer
41 pts – 3MM EE



Final SOI:
Mean = 120Å – Range=7.4Å



Junctionless DG MOSFET

- Analytical charge control model from 1D Poisson (with approximations) – long channel model
- Short-channel effects can be incorporated in a similar way as in accumulation-mode Single-Gate SOI MOSFETs
- Results accepted for publication in IEEE TED

Conclusions

- The model is valid for all regimes of operation
  - Deep depletion – accumulation
  - Linear – saturation

- No empirical parameters are used
- Can be improved by adding field dependent mobility and SCE

- As it happens with DG MOSFETs models, our model for junctionless DG MOSFETs can be applied to Tri-gate MOSFETs and FinFETs with adequate values of some parameters (Si layer thickness, thershold voltage, mobility).

- URV is currently working on the adaptation of this model to a junctionless cylindrical Surrounding Gate MOS structure (can be applied to nanowires)