Gant Agreement N° 257111

SQWIRE

Silicon Quantum Wire Transistors

Start date of project:	1 September 2010
Duration:	36 Months

Coordination Action
Information and Communication Technologies

Deliverable D3.3	
Gated Resistors: Nanometrology and electrical characteristics	
Due date of deliverable:	31/01/2012
Actual submission date:	01/02/2012
Organisation name of lead contractor for this deliverable:	Tyndall National Institute - UCC

Revision [ ]

Approval

WP Leader	☐	**SP Leader**	☐	**Coordinator**	☒

Partner	**Please, give a short description (1-3 sentences) of partners contribution to this deliverable**
Tyndall	Initial measurements will be performed on prototype Gated Resistor devices fabricated at TNI-UCC.
IMEP / INPG	IMEP/INPG, in collaboration with TNI-UCC, CEA-LETI and URV, will develop agreed protocols for die-level electrical testing and parameter extraction.

Project co-funded by the European Commission within the Seventh Framework Programme (2007-2012)		
Dissemination Level		
PU	Public	**x**
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission	
CO	Confidential, only for members of the consortium (including the Commission Services)	

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Introduction

CMOS Junctionless nanowire transistors (JNT) were processed by CEA-LETI. A description of the fabrication process and of inline measurement results are provided in Deliverable 3.2 (Nanometrloogy protocol for gated resistors). Among the wafers delivered to the participants, some were selected for advanced electrical characterisation.

The present document summarises the most relevant results obtained to date, including their analysis and prospects for future research work. All of the results presented below originate from experimental evidence, not from simulation work.

Temperature and bias dependence in JNTs (Contributors: Tyndall-UCC)

1. Impact of temperature on the threshold voltage in JNTs

In this section we analyze the impact of temperature on various device parameters of JNTs. Fig. 1 shows measured transfer characteristics (drain current as a function of gate voltage) of JNTs at different temperatures for of gate length (a) L=40 nm, (b) L=50 nm, and (c) L=90 nm at V_{DS} = ±0.9 V. Their effective fin width is estimated to be 22 nm. The source terminal and the substrate are grounded during electrical measurements. These curves are used to calculate the threshold voltage in saturation V_{th}, sub-threshold slope SS, leakage current, and ON/OFF current ratio. From Fig. 1, it is observed that, as the substrate temperature increases, the threshold voltage decreases and the sub-threshold slope is degraded.

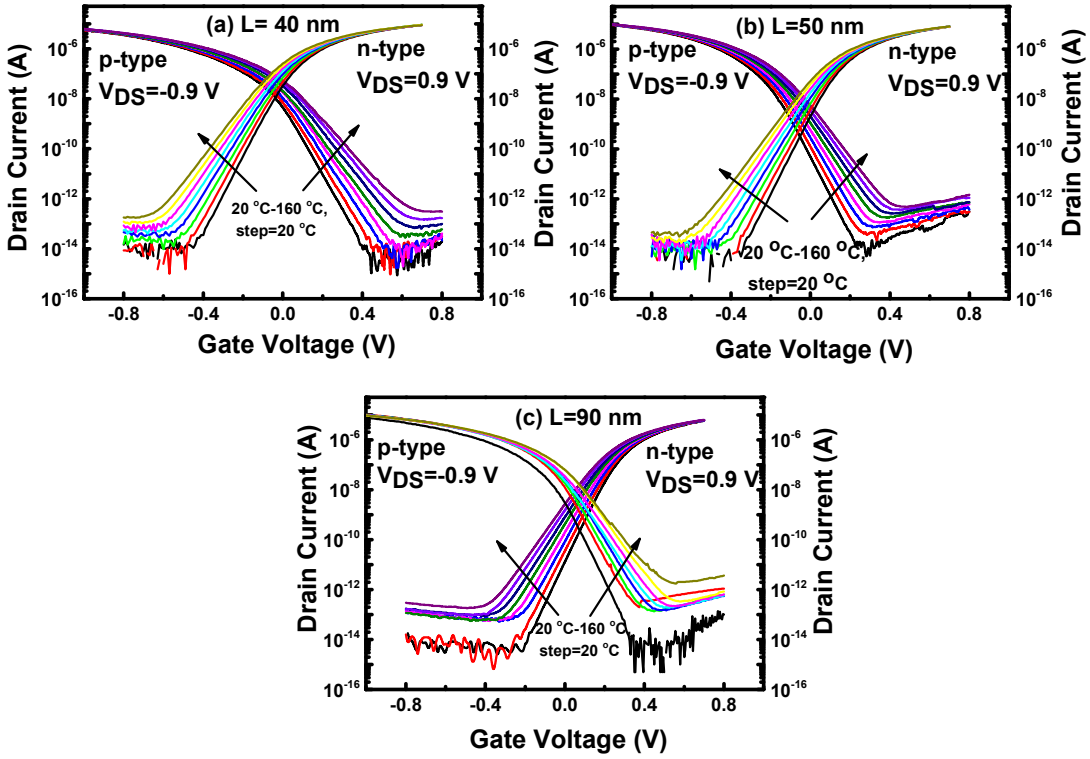

Fig. 1: Transfer characteristics (I_{DS}-V_{GS}) of JNTs at different temperatures for gate lengths (a) L=40 nm, (b) L=50 nm, and (c) L=90 nm.

The impact of temperature on threshold voltage (V_{th}) is discussed first. Figs. 2 (a) and (b) show the variation of V_{th} with temperature for p-MOS and n-MOS JNTs, respectively, for different gate lengths. The threshold voltage was calculated from the maximum derivative of transconductance. For n-MOS JNT, the expression for threshold voltage can be written as [1],

$$V_{th} = V_{FB} - \frac{qN_D}{\epsilon_{Si}}\left(\frac{A}{P}\right)^2 - \frac{qN_D A}{C_{ox}} + \frac{\Delta E_0}{q} \qquad (1)$$

Where A and P are the device cross-sectional area and gate perimeter, respectively, and ΔE_0 is the variation of the minimum energy level in the conduction band due to quantum confinement. Now the variation of threshold voltage with temperature T is

$$\frac{\partial V_{th}}{\partial T} = \frac{\partial V_{FB}}{\partial T} - \left(\frac{q}{\epsilon_{Si}}\left(\frac{A}{P}\right)^2 + \frac{qA}{C_{ox}}\right)\frac{\partial N_D}{\partial T} + \frac{1}{q}\frac{\partial \Delta E_0}{\partial T} \qquad (2)$$

- The first term depends on the Fermi potential and bandgap variations with temperature.
- The second term is only related to the variation of N_D with T.
- The third term depends on the effective mass, which is only slightly dependent on T.

The band gap is assumed to be independent of T over the temperature range under consideration (20-160 ^{o}C). The Fermi potential depends on intrinsic carrier concentration, which is a function of

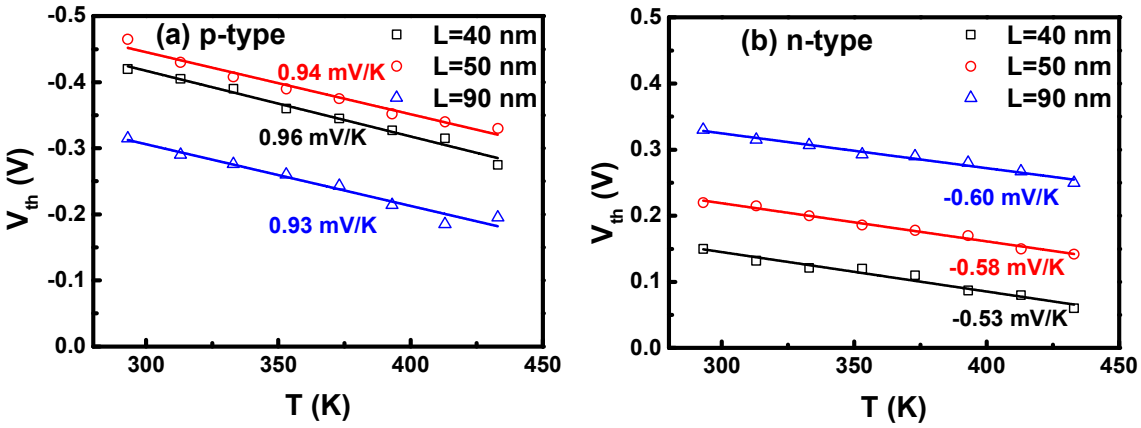

Fig. 2: Threshold voltage of JNTs: (a) p-MOS and (b) n-MOS as a function of temperature for different gate lengths.

temperature. Hence the 1st term is the dominant part of (2) since variations in the doping level N_D are not expected for these devices. The rate of change (dV_{th}/dT) of threshold voltage with temperature is around -0.60 mV/K for n-MOS and that is 0.97 mV/K for p-MOS with 40 nm gate length. The value of dV_{th}/dT is nearly independent of gate length. FDSOI MOSFETs have a smaller threshold voltage variation with temperature than bulk MOSFETs [2], due to the non-existence of temperature induced variation of the depletion zone depth. For a similar reason, the threshold voltage dependence on temperature in JNTs (entirely depleted in on-state) is less pronounced than in inversion mode multi gate devices [4].

2. Impact of temperature on the sub-threshold slope *SS* in JNTs

The SS is defined as the inverse of the slope of the log of the drain current versus gate voltage, below threshold. It has a theoretical value of $SS = (kT/q)\ln(10)$. The impact of temperature on SS along with the thermodynamic limit (at room temperature, solid black line) is presented in Fig. 3. Minor difference with the theoretical limit shows that JNTs exhibit an ideal turn ON. The sub-threshold slope measured at 300 K is 62 mV dec-1 for n-MOS and 66 mV dec-1 for p-MOS having

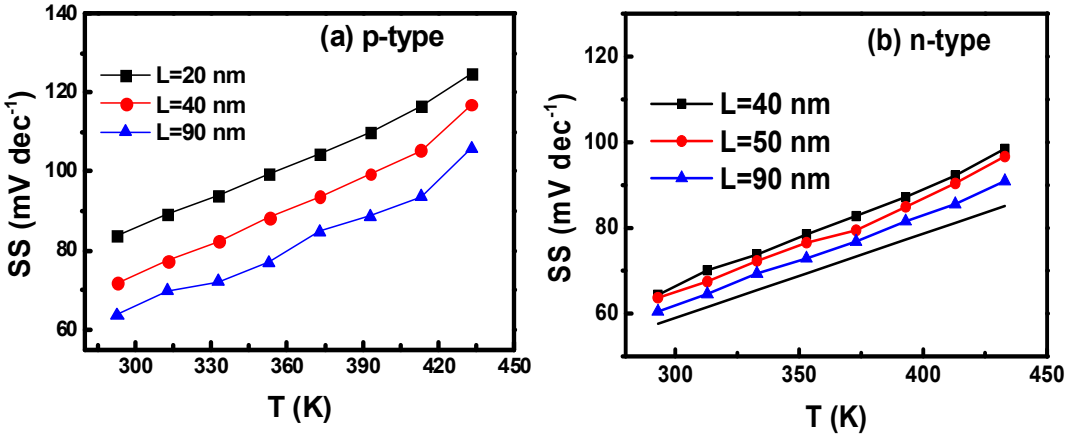

Fig. 3: Variation of sub-threshold slope (SS) with temperature of JL (a) p-MOS and (b) n-MOS for different gate length. Solid black line shows the evolution of the minimum *SS* with temperature.

a gate length of 90 nm. The SS at 300 K increases from 62 to 67 mV dec-1 for n-MOS and from 66 to 86 mV dec-1 for p-MOS as the gate length decreases from 90 nm to 40 nm. A little increase in the non-ideality above 420 K is observed for n-MOS JNTs.

3. Impact of temperature on ON and OFF currents in JNTs

Figs. 4 (a) and (b) show the measured ON current as a function of temperature for p-MOS and n-MOS JNTs, respectively. The ON current is taken at a fixed gate voltage overdrive ($GV_0 = |V_{GS} - V_{th\ (roomtemperature)}|$). Here, we used $GV_0 = 0.5$ V.

In a conventional MOSFET, the decrease of threshold voltage with temperature tends to increase drain current, while the reduction of mobility due to increasing phonon scattering with temperature tends to compensate for this increase. In JNTs, the reduction of mobility with temperature is much

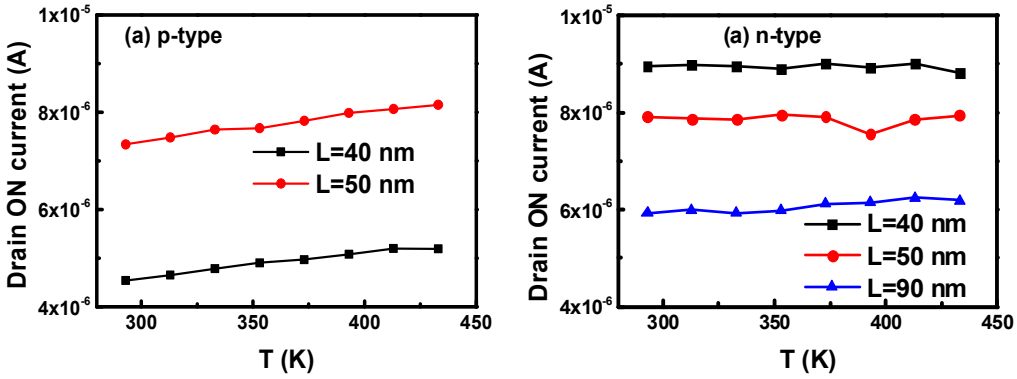

Fig. 4: Measured drain ON current of (a) p-MOS and (b) n-MOS JNTs as a function of temperature.

lower than in the other types of transistors thanks to the bulk conduction. As a result, current increases in a monotonous manner as the temperature increases. The change of drain ON current with temperature is more pronounced for p-MOS due to larger change in threshold voltage compared to p-MOS.

Figs. 5 (a) and (b) show the variation of off-leakage current with inverse absolute temperature for p-MOS and n-MOS JNTs, respectively. The off-state leakage current is extracted at a fixed gate voltage, V_{GS} =+0.6(-0.6) V for p(n)-MOS. The off–leakage current increases with temperature because of the increase of intrinsic carrier concentration. All transistors show low leakage levels (below 1 pA) up to a temperature of 160 ^{o}C thanks to the absence of junctions in JNT.

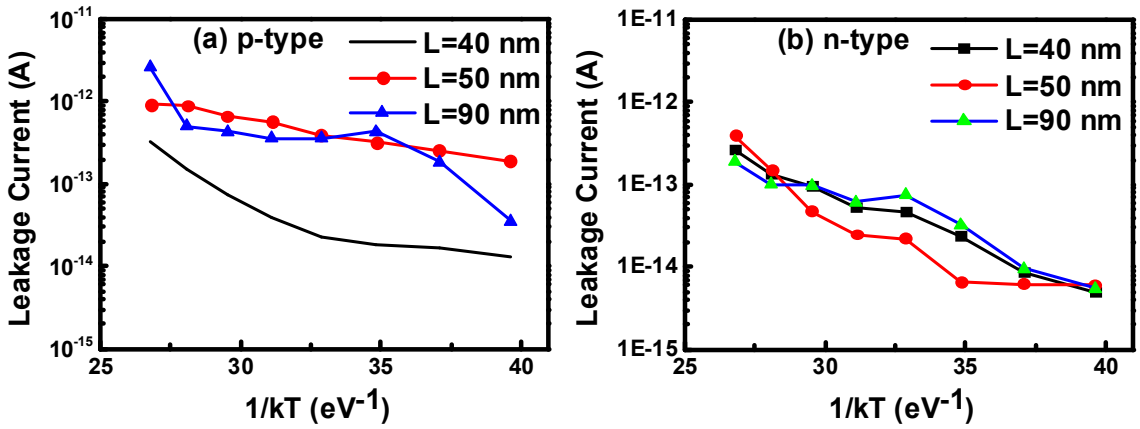

Fig. 5: Extracted drain OFF current of (a) p-MOS and (b) n-MOS JNTs as a function of inverse temperature.

Fig. 6 shows the ON/OFF current ratio of JL transistors measured at different temperatures. For all the devices the ON/OFF current ratio is higher than 10^7 A at a temperature of 160 ^{o}C. The degradation of ON/OFF current ratio at high temperature is mainly due to the increase in OFF current.

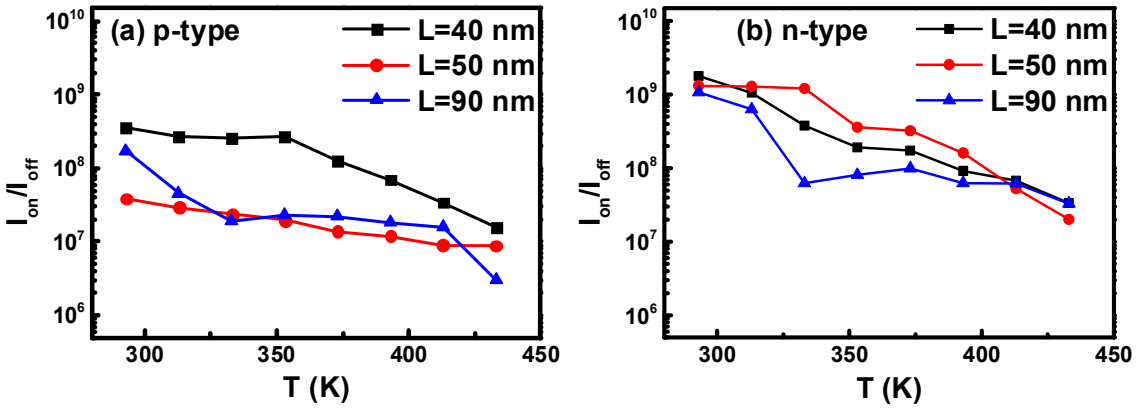

Fig. 6: Variation of ON/OFF drain current ratio with temperature for (a) p-MOS and (b) n-MOS JNTs for different gate lengths.

4. Gate Induced Drain Leakage (GIDL) in JNTs

Fig. 7 shows the measured drain current vs gate voltage in n-MOS junctionless transistor for different drain voltages. For 40 nm gate length device when a drain voltage of 1 V is applied, the sub-threshold slope of 67 mV dec^{-1} has been observed. But a sub 60 mV dec^{-1} *SS* value is observed when a3.25 V drain voltage applied. The current increase and sub-threshold reduction t higher drain voltage are attributed to impact ionization. However the off-state leakage current caused by GIDL increases with V_d. Thus we attempt to estimate the GIDL current value for JL transistor.

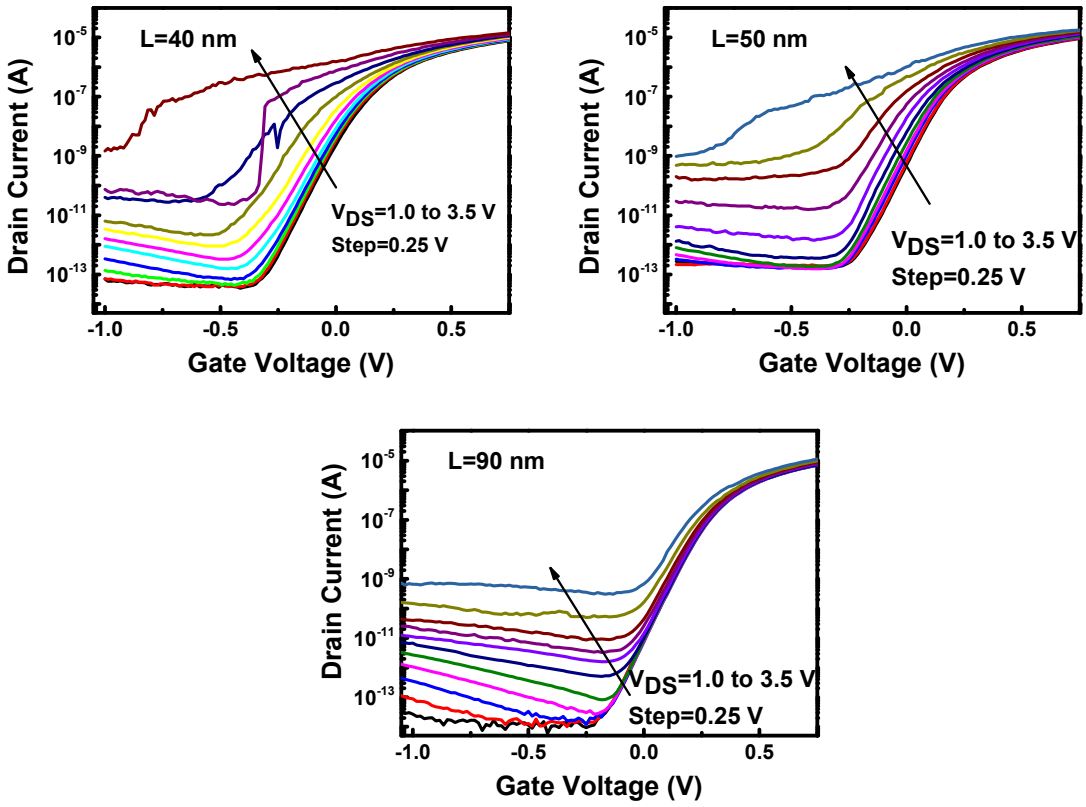

Fig. 7: Measured drain current vs gate voltage in JNTs for different drain voltages.

Fig. 8 shows the measured off-state leakage of n-MOS JL transistors for different gate length at V_{GS}=-1 V. GIDL manifests itself as an increase of drain current when a negative (positive) gate voltage is applied to the gate of an n-channel (p-channel) device. The GIDL current is caused in JNTs is attributed to band-to-defect tunnelling (BTDT) in the gate and drain overlap region.

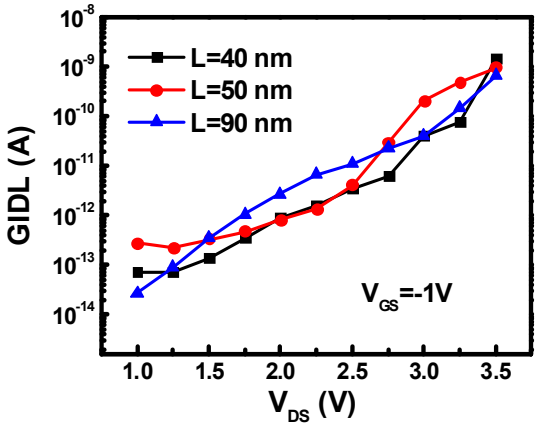

Fig. 8: Evolution of the off-state leakage current in n-MOS JNTs for different gate lengths.

In conclusion, silicon junctionless nanowire transistor is presented with temperature studies on the electrical performance. Whilst having superior transistor properties at room temperature, the junctionless nanowire transistor has managed to maintain many of these properties even as temperature is increased.

Electrical characterization and Revisited Parameter Extraction Methodology in Junctionless Transistors

(Contributors: D.-Y. Jeon, S. J. Park, M. Mouis, and G. Ghibaudo (collaboration with LETI-Grenoble))

1. Introduction

Recently, much attention has been focused on the JNT as a possible candidate for the continuation of Moore's law [5]. Although JNT operation is governed by field-effects, the use of a doped channel, with the same doping type as in the source and drain, raises specific features compared to standard inversion mode MOSFETs. Thus, the methodologies used to extract physically-grounded electrical parameters must be revisited. This is the aim of this paper.

2. Devices under test and experiment

JNT devices with high-k/metal gate stack were fabricated at CEA-LETI on (100) SOI wafers with 145 nm thick BOX and Si body thinned down to 10 nm. The channel implant was performed on non-patterned wafers with a phosphorus doping targeted at $10^{19}/cm^3$. The gate consisted in an HfSiON /TiN /Poly-Silicon stack. On mask gate width W_M was ranging from 10 µm (wide planar devices) to 80 nm (nanowires). Arrays of nanowires were available making capacitance measurements possible for the smallest devices. On mask gate length L_M ranged from 10 µm down to 30 nm. Split C-V measurements were carried out using HP4294a with a 50 mV small signal at 500 kHz and substrate bias (V_{gb}) varying from -30 V to 30 V. Gate voltage will be called V_{gf}. The low frequency noise was measured with a semi-automatic system from Synergy concept (Meylan, F).

3. Results and discussion

Typical $I_d(V_{gf})$ and $g_m(V_{gf})$ characteristics were obtained for gate lengths and show good behaviour down to 30 nm (Figs 1-2).

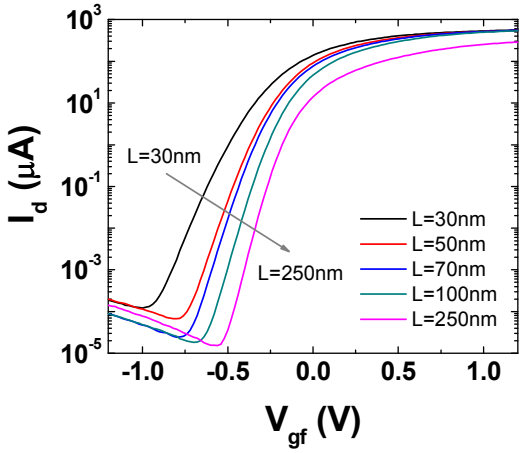

Fig.1: I_d vs V_{gf} for various gate lengths (V_d=50 mV, W=10 µm).

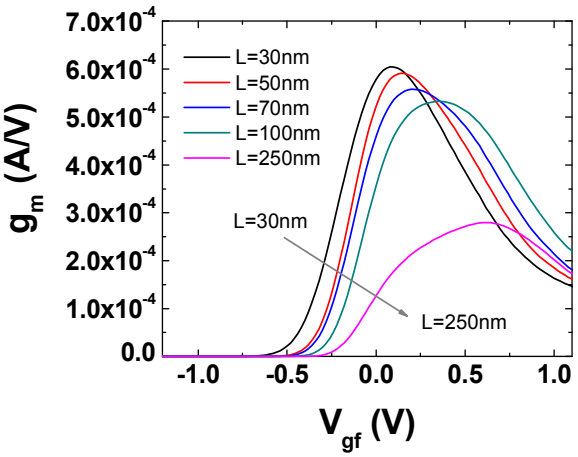

Fig.2: g_m vs V_{gf} for various gate lengths (V_d=50 mV, W=10 µm).

The corresponding $Y(V_{GS})$ functions defined as [6]:

$$Y(V_{gf}) = I_d / \sqrt{g_m} \qquad (1),$$

are plotted in Fig. 3.

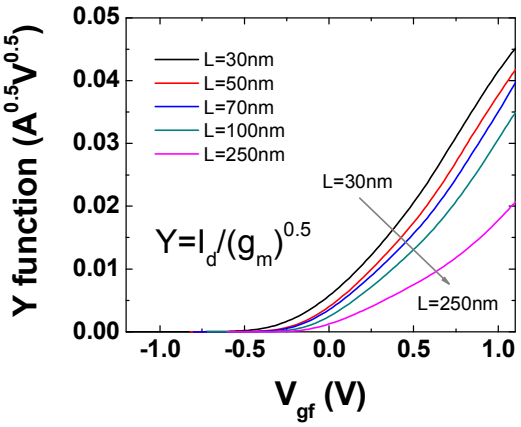

Fig.3: Y(V_{gf}) function based on the results of Figs1-2 for various gate lengths.

The threshold voltage V_{ty} extracted using Y-function in accumulation was compared with the values deduced from other methods (Fig.4) such as linear extrapolation of transfer characteristics (V_{text}), maximum derivative of transconductance (V_{tdgm}) and constant current technique (V_{tcc}). The low field electron mobility μ_0 extracted from Y-function was close to the maximum field effect mobility (μ_{femax}, deduced from the maximum g_m) for long gate lengths only, due to degradation effect by series resistance (R_{SD}) at small gate lengths (Fig.5).

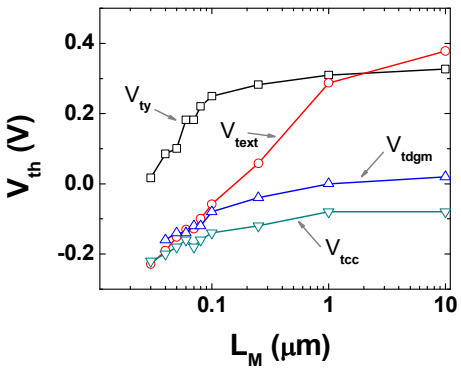

Fig.4: V_{th} vs gate lengths extracted by various methods (W=10 μm).

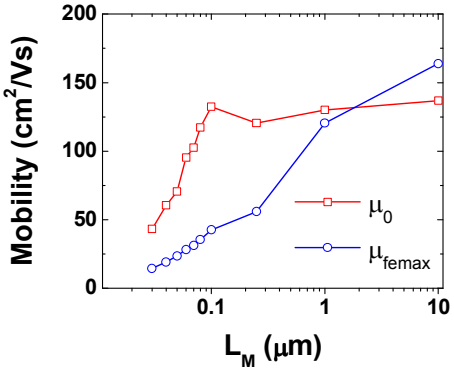

Fig.5: Variation of mobility μ_0 and μ_{femax} vs various gate lengths (W=10 μm).

The R_{SD} (≈660 Ω·cm) extracted from first-order attenuation factor as shown in Fig. 6 is consistent with the value (≈1050 Ω·cm, in inset of Fig.7) obtained from transfer length method (TLM).

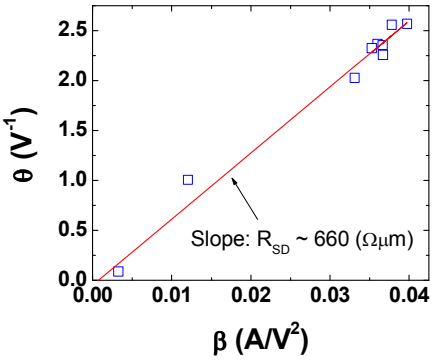

Fig.6: Extraction of R_{SD} and first-order attenuation factor values (W=10 μm).

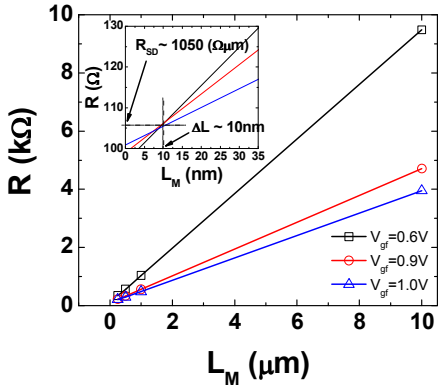

Fig.7: Channel resistance R vs gate length for extraction of R_{SD} and ΔL.

The channel length and width reduction, ΔL and ΔW, of JNT were extracted from the linear relationship between the gate-to-channel capacitance (C_{gc}) and effective channel dimensions (W and L) in Fig. 7. ΔL and ΔW can also be deduced by TLM method (Fig. 8) and the linearity between I_d vs W_M (Fig. 9).

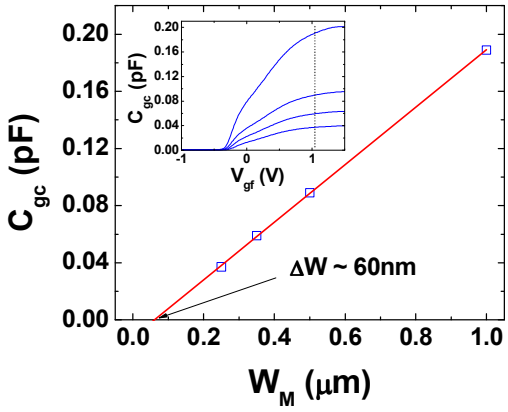

Fig.7: C_{gc} (gate to channel) vs gate width for extraction of ΔW.

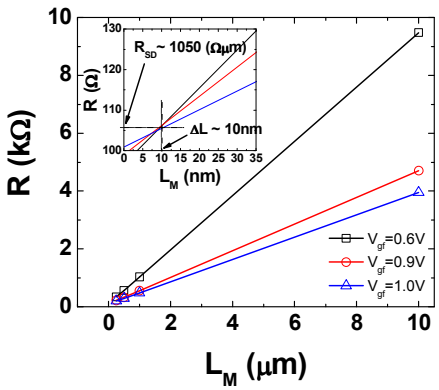

Fig.8: Channel resistance R vs gate length for extraction of R_{SD} and ΔL.

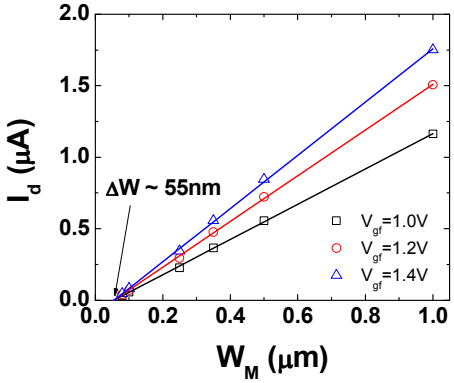

Fig.9: I_d vs gate width for extraction of ΔW.

The drain induced barrier lowering (DIBL) vs length as shown in Fig. 11 was calculated by saturation drain current sensitivity to drain voltage normalized to its sensitivity to gate voltage in subthreshold, near flat-band and accumulation regions from data of Fig. 10 [6]. Note the strong increase of DIBL with gate voltage due to worse saturation behaviour of JNT in accumulation.

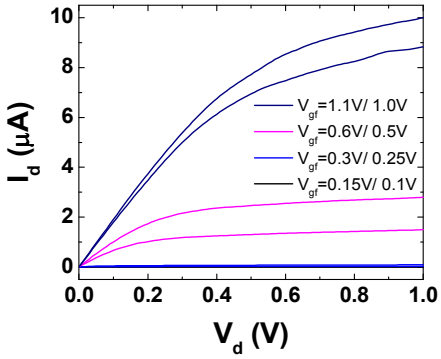

Fig.10: I_d vs V_d for various values of V_{gf} for extraction of DIBL (W_{eff}:23 nm, L_{eff}:35 nm).

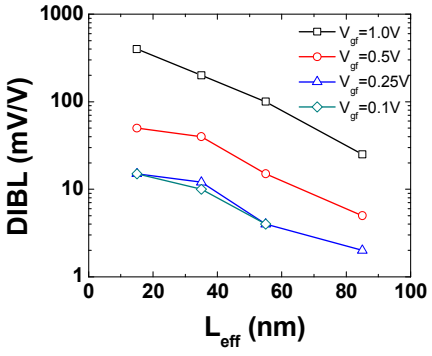

Fig.11: DIBL variation with L_{eff} extracted from fig.10.

Threshold (V_{th}) and flat-band voltage ($V_{fb} \approx 0.24$ V) of JNT were determined through peaks of derivative of $C_{gc}(V_{gf})$ for various V_{gb} varied from -30 V to 30 V as shown in Fig. 12 and compared to the results from derivative of $g_m(V_{gf})$. Effective mobility in Fig. 13 could be distinguished as dominated by bulk conduction (left-hand side) or accumulation (right-hand side), with $V_{fb} \approx 0.24$ V separating the two regimes. Channel doping concentration was extracted from two methods, namely sheet carrier density (n_s) at V_{fb} and Maserjian's doping function (Figs 14-15) [7,8]. Doping concentrations deduced from these two methods were close to each other ($\approx 3.5\times10^{18}$/cm^3 and $\approx 6\times10^{18}$/cm^3, respectively). They were also comparable to the targeted doping level (1.0×10^{19}/cm^3).

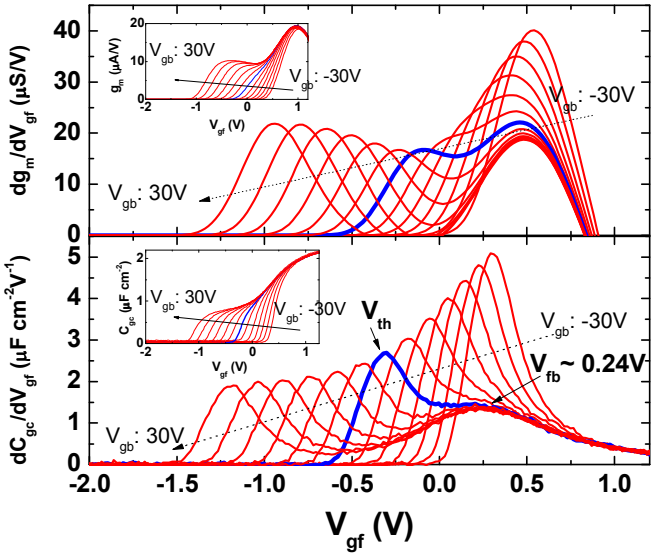

Fig.12: Derivative of $C_{gc}(V_{gf})$ and $g_m(V_{gf})$ for various values of substrate bias V_{gb} (Freq.:500 kHz, W=L=10 μm).

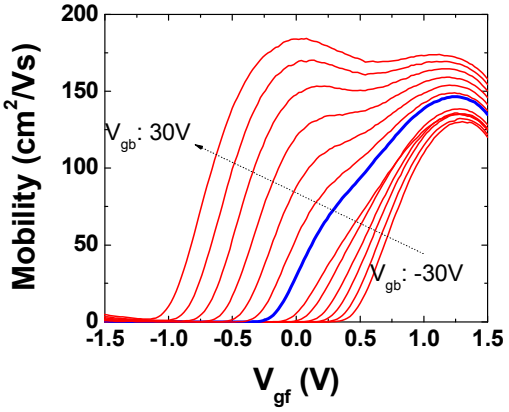

Fig.13: Effective mobility vs V_{gf} with V_{gb} ranging from -30 V to 30 V as a parameter (W=L=10 μm).

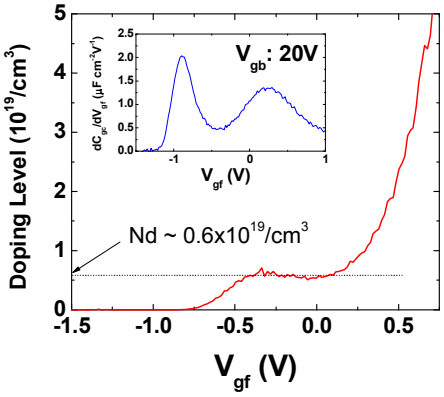

Fig. 14: Variation of extracted doping level vs V_{gf} as obtained using Maserjian's function.

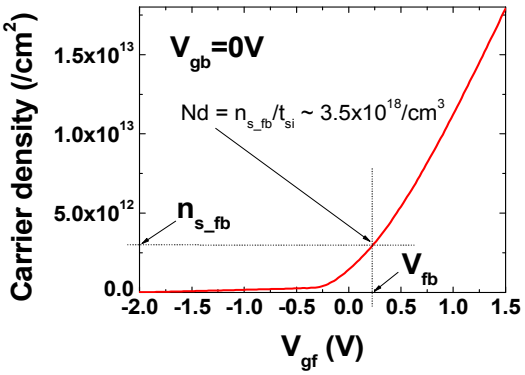

Fig.15: $n_s(V_{gf})$ characteristics as obtained by $C_{gc}(V_{gf})$ integration from fig.12.

The quality of the silicon-gate dielectric interface was evaluated using LF noise measurements. Figure 16 shows typical 1/f noise spectra obtained on large JNT for various gate voltages varying from subthreshold to accumulation regions. Figure 17 gives the variations of the normalized drain current noise with drain current in log-log scale to allow for LF noise source diagnostic. The LF noise in JNT is very explained by the carrier number fluctuation model (dash line in Fig. 17) [9]:

$$\frac{S_{Id}}{I_d^{\,2}} = S_{Vfb} \cdot \left(1 + \alpha_C \mu_{eff} C_{ox} \frac{I_d}{g_m}\right)^2 \cdot \left(\frac{g_m}{I_d}\right)^2 \qquad (2)$$

where S_{Vfb} is the flat-band voltage power spectrum (V^2/Hz), α_C the Coulomb scattering parameter which is relevant to mobility fluctuations (Vs/C), μ_{eff} the effective mobility (cm^2/Vs) and C_{ox} the oxide capacitance per unit area (F/cm^2). The S_{Vfb} arises from tunneling process at the oxide interface:

$$S_{Vfb} = \frac{q^2 k_B T \lambda N_t}{f W L C_{ox}^{\,2}} \qquad (3)$$

where q is the electronic charge, k_B the Boltzmann constant, T the temperature (K), λ the oxide tunneling length (cm), N_t the volume oxide trap density ($cm^{-3}eV^{-1}$) and W the total channel width. In this case, the oxide trap density Nt was found around $7x10^{17}/eVcm^3$, in good agreement with data obtained on inversion mode devices of same dielectric/metalgate stack, confirming the good quality of such JNT devices.

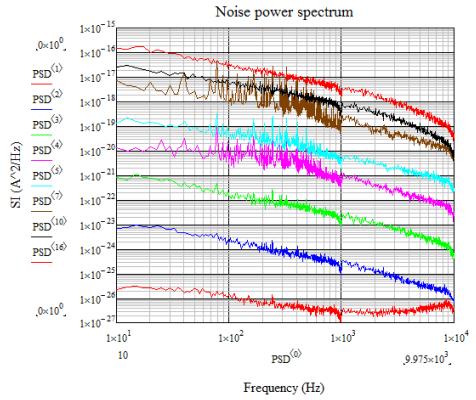

Fig.16: Spectra of drain current PSD obtained on W=10µm and L=60nm JNT device for various gate voltage from subthreshold to accumulation regions (Vd=50mV).

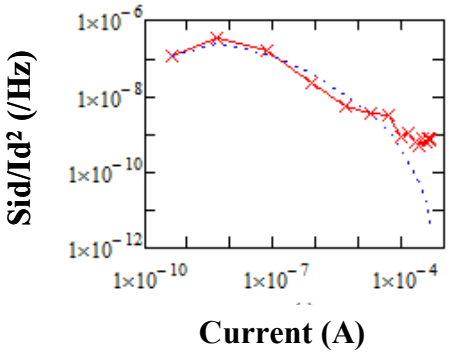

Fig. 17: Experimental (symbols) and modelled (dash line) normalized drain current noise variations with drain current measured at 10Hz (Vd=50mV).

The electrical parameters of junctionless transistors were extracted by I-V and C-V characterization based on methodologies which were revisited from those used for inversion transistors. The extracted parameters such as V_{th}, V_{fb}, DIBL, mobility and doping level show the specificities of JNTs.

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