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BASTION

Board and SoC Test Instrumentation for Ageing and No Failure Found

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Thematic Priority: Information and Communication Technologies

Improvements of test coverage metrics (Deliverable D1.3)

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Notices

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This document is intended to fulfill the contractual obligations of the BASTION project concerning deliverable D1.3 described in contract 619871.

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Executive Summary

This document represents the BASTION research results in the area of test coverage metrics (Task 1.4 – Improvement of test coverage metrics).

Based on the conclusion of D1.1, the most important contributor to NFF was narrowed down to insufficient coverage; whereas intermittent and timing faults were confirmed to be challenging issues, due to lack of respective test techniques or test coverage metrics.

The BASTION partners identified test coverage improvements and related methods and tools, that should contribute to the BASTION mission: reducing NFF.

List of Abbreviations

AOI	- Automated Optical Inspection
AXI	- Automated X-ray Inspection
BERT	- Bit Error Rate Testing
BIST	- Built-in Self-Test
BST	- Boundary Scan Test
BTI	- Bias Temperature Instability
CM	- Contract manufacturer
CMOS	- Complementary Metal-Oxide Semiconductor
CRC	- Cyclic Redundancy Check
dB	- Decibel
DPM	- Defects Per Million
DPMO	- Defects Per Million Opportunities
DPU	- Defect per Unit
DUT	- Design under Test
EI	- Embedded Instrument
EM	- Electro Migration
EMS	- Enhanced Manufacturing Services
FAM	- Subset of PCOLA/SOQ/FAM
FET	- Field Effect Transistor
FMEA	- Failure Mode and Effect Analysis
FPGA	- Field Programmable Gate Array
FP7	- European Union's 7th Framework Program
FPT	- Flying Probe Test
FPY	- First Pass Yield
FT	- Functional Test
HCI	- Hot Carrier Injection
IC	- Integrated Circuit
ICT	- In-Circuit Test
IPC	- Institute for Printed Circuits
Iddt	- Transient power-current
Iddq	- Quiescent power current
INEMI	- International Electronic Manufacturing Initiative
IRF	- Intermittent Resistive Fault
IST	- Information Society Technologies
IVF	- Intermittent Vulnerability Factor
JTAG	- Joint Test Action Group

MPS	- (Coverage metrics based on) Material, Placement & Solder
MTRF	Marginal TRF's - can lead to sporadic failures of electronic products in field.
NBTI	- Negative Bias Temperature Instability
NDF	- No Defect Found
NFF	- No Fault Found, No Failure Found
NMOS	- n-type Metal Oxide Semiconductor
NTF	- No Trouble Found
OBD	- Oxide Breakdown
PCOLA/SOQ	- (Coverage metrics based on) Presence, Correct, Orientation, Live, Alignment/Short, Open & Quality
PCOLA/SOQ/FAM	- (Coverage metrics based on) Presence, Correct, Orientation, Live, Alignment/Short, Open & Quality, Feature, At-Speed, Measurement
PCOLA	- Subset of PCOLA/SOQ
PCBA	- Printed Circuit Board Assembly
PMOS	- p-type Metal Oxide Semiconductor
PPM	- Part Per Million
PPVS	- (Coverage metrics based on) Presence, Polarity, Value & Solder
PVT	- Process, Voltage, Temperature
RO	- Ring Oscillator
SoC	- System on Chip
SOQ	- Subset of PCOLA/SOQ
SBD	- Soft Breakdown
SPQL	- Shipped Product Quality Level
TDDB	- Time Dependent Dielectric Breakdown
TRF	- Timing-Related Faults
TSV	- Through Silicon Via
URL	- Uniform Resource Locator
UUT	- Unit Under Test
VTH, V_{th0}	- Threshold Voltage

Table of Contents

1 Introduction

This document relies on the state-of-the-art as defined in D1.1 - Report on the NFF and ageing fault study - for defects, fault model, test coverage, production model and escape rate. D1.1 provides information relating to test coverage and how it is linked with NFF.

The insufficient/unknown test coverage has been identified as a key contributor to NFF. The cumulative fault coverage achieved by the combination of board-level test techniques reveals duplicated tests, but more importantly, reduces the missing test coverage.

It was also observed that were limitations in the state-of-the-art industrial best practices for traceability data analysis and DPMO tracking. This gives space for improvement in NFF case analysis.

Cooperation with the BASTION partners helps to identify subjects where the coverage metrics can be significantly improved. In BASTION we are focusing on the following types of faults:

- Aging and wear-out at IC and board level
  - IC and board-level intermittent resistive faults (IRF);
  - IC-level aging faults mainly due to NBTI but also HCI.
- Timing-related faults (TRF) at board level and signal integrity issues in high-speed links (board/system level)
  - transition delays (pin-level and connection-level);
  - bit slips and bit errors;
  - crosstalk.

This deliverable has the following structure. Section 2 addresses the coverage of timing related faults (TRF), or performance-related issues, e.g. delay faults, crosstalk, signal integrity, interconnection quality, communication link integrity, etc. State-of-the-art test methods for these fault classes (such as conventional BERT or at-speed test) do not provide proof of good or sufficient fault coverage.

The in-field monitoring test coverage resulting from hardware and software monitors including intermittent resistive faults (IRF) is addressed in Section 3 followed by the description test coverage representation format allowing to formally describe the test coverage and use it in software like QuadDPMO (see Section 4). Section 5 presents the test coverage analysis based on real DPM, which is followed by Section 6, which focuses on the cross-analysis of defects detected, versus the defects covered.

Finally, conclusions and discussion on relevant KPIs are also provided.

2 Board-Level Timing-Related Fault Modeling

Like the snake biting its tail, the test techniques and respective equipment (the head of the snake) are developed, based on the manufacturing defect universe (the tail), while target defect classes are expert-defined and based majorly on the ability of test equipment to test them. This fact creates a certain deadlock in thinking: to see the gap in the coverage we need to break the snake-circle and take a step outside the defect universe. To put it simply: 100% test coverage of known defect categories does not guarantee that defects unknown today are also well-covered.

Board-level testing of Printed Circuit Board Assemblies (PCBA) is characterized by a great diversity of, sometimes, incompatible or overlapping approaches to fault modeling. This, mixed with explicit defect enumeration and expert experience, collectively contributes to product test strategy development, as well as test coverage (as opposed to fault coverage) assessment.

Marginal faults at board level form the risk group located in the "grey zone". Their detection requires either special environmental conditions (e.g. vibration, temperature, humidity, electromagnetic interference) or fine-tuned test application and measurement techniques. Typical examples of these faults or observed effects are: intermittent faults, delay faults, crosstalk, low signal-noise ratio, soft errors, etc.

Although systematic test methods for some of them do exist, their quality and contribution to the overall combined PCBA test coverage often remains unquantified. The common practice is to categorize *defects*, not faults, where defect categories are often equipment vendor-driven [3], or defined by testability analysis tool vendors, e.g.[4], [18], [19].The studies on systematic board-level abstract *fault modeling* available in the literature are mainly related solely to JTAG/Boundary Scan (JTAG/BST) test techniques, e.g. [1], [2], [7], [8], [17].

An action group called iNEMI collected a mixture of faults and defects into a system of categories known as PCOLA/SOQ/FAM [5]. These categories are chosen based either on real physical defects (e.g. misplaced component) caused by the manufacturing process, or on capabilities of particular test techniques to detect faults (e.g. at-speed test).

In the context of board level test in BASTION, we have studied intermittent resistive faults (IRFs, as discussed in D1.1 and D2.1), delay faults on interconnects as well as outliers in a group of signals on a high-speed synchronous bus, such as a DDR4 interface.

The importance of testing for IRFs, as well as for any intermittent faults especially in mission-critical systems, is widely accepted and remains an important research topic today. The importance of testing for delays and other timing-related faults (TRF) has been thoroughly analyzed in D1.1, by pointing out a gap in the state-of-the-art test coverage metrics used in practice for PCBA test quality assessment.

Although the value of at-speed test is increasingly evident today, a systematic approach to quantify the quality of such a test, in terms of test coverage, is still missing. This section describes the attempt to propose an easy-to-implement, interconnect-level fault model extension targeting delay faults. The simple extension is based on static fault models, widely adopted in JTAG/BST. As a result, several proposed types of delay fault models, described in Section 2.2, could be easily integrated into test coverage assessment tools. This contribution specifically addresses the BASTION KPI on identification of at least 2 new fault classes contributing to NFF. With regard to this KPI we, first, indicated the current issues of testing for the class of board-level delay

faults (see D1.1 for details). Secondly, we have formulated two new types of delay faults that can be enumerated on board level and that may correspond to a number of structural defects or quality issues like excessive solder voids or large ground void, solder rejection, “head in pillow”, caves in microvias, excessive roughness of trace surface, etc. which are otherwise hard-to-test without involving X-Ray equipment due to marginal influence on functionality.

2.1 *Issues in board level TRF test*

The electronic manufacturing industry has entered a new age, where *static* structural test technologies like JTAG/BST and In-Circuit Test (ICT) start quickly losing their efficiency, in terms of fault coverage, while there is currently no existing systematic alternative to replace them. For instance, a vast majority (86%) of the test engineers often encounter problems when testing SRAM/DRAM or Flash memories [6] using JTAG/BST.

As a result, *at-speed* test techniques, mainly ad-hoc but capable to detect *timing/dynamic* faults, are being developed today and introduced into the manufacturing process. They target timing-related defects or dynamic faults (e.g. bad terminations, resulting in transition faults, delays, crosstalk, switching noise or other AC domain effects) that manifest themselves only at high signal frequencies.

Architectural modifications, enabling at-speed test application mechanisms [7], [8], have also been proposed in the past for JTAG/BST. However, with the lack of standard support, these methods didn’t find any practical applications.

Traditionally, the Functional test (FT) [9] and interconnect Built-in Self-Test (BIST) [10] are the final resort in hunting for timing-related faults (TRF). Although, being costly in development the FT, unlike the BIST, does not require any modifications to the system, and is therefore often used along with the Application Test as the end-of-the-line technique, to ensure the high quality of the delivered product. Unfortunately, the FT typically does not produce measurable coverage of structural faults (including TRFs) and is not suitable for debug and diagnosis. As a result, the portion of tested TRFs out of the complete fault universe remains unknown.

The latter fact keeps the industry to focus on available test strategies, based on enumerated structural faults, and drives development of new structural test techniques aimed at solving problems of TRF detection and diagnosis. The leading companies are adopting recently emerging high-speed, or at-speed, test techniques, based on the automated (re-)configuration or programming of on-board programmable devices like FPGAs (referred to as FPGA-centric [11-12] or FPGA-controlled [13] test) and processors (referred to as processor-emulation [14], processor-centric [15] or processor-controlled [16] test).

Together with relevant test coverage metrics, these test techniques promise good timing fault coverage. *However, if adequate test metrics are missing, the coverage is incidental because generating good-quality test stimuli becomes difficult.*

As it has been already pointed out, FT does not guarantee complete TRF coverage, because the structural coverage of FT is normally unknown. Traditional structural tests are normally low speed tests, hence leaving no chance to cover TRFs. Advanced test methods are good in terms of capabilities but require dedicated metrics (enumerated fault classes) to be used, which are missing.

2.1.1 Where is the TRF coverage today?

When BASTION project started, PCOLA/SOQ/FAM [5] was the most comprehensive system to assess test quality and combined test coverage, achieved by a collection of test techniques. It classifies defects into a set of categories and provides quasi-quantitative metrics of defect coverage for each category.

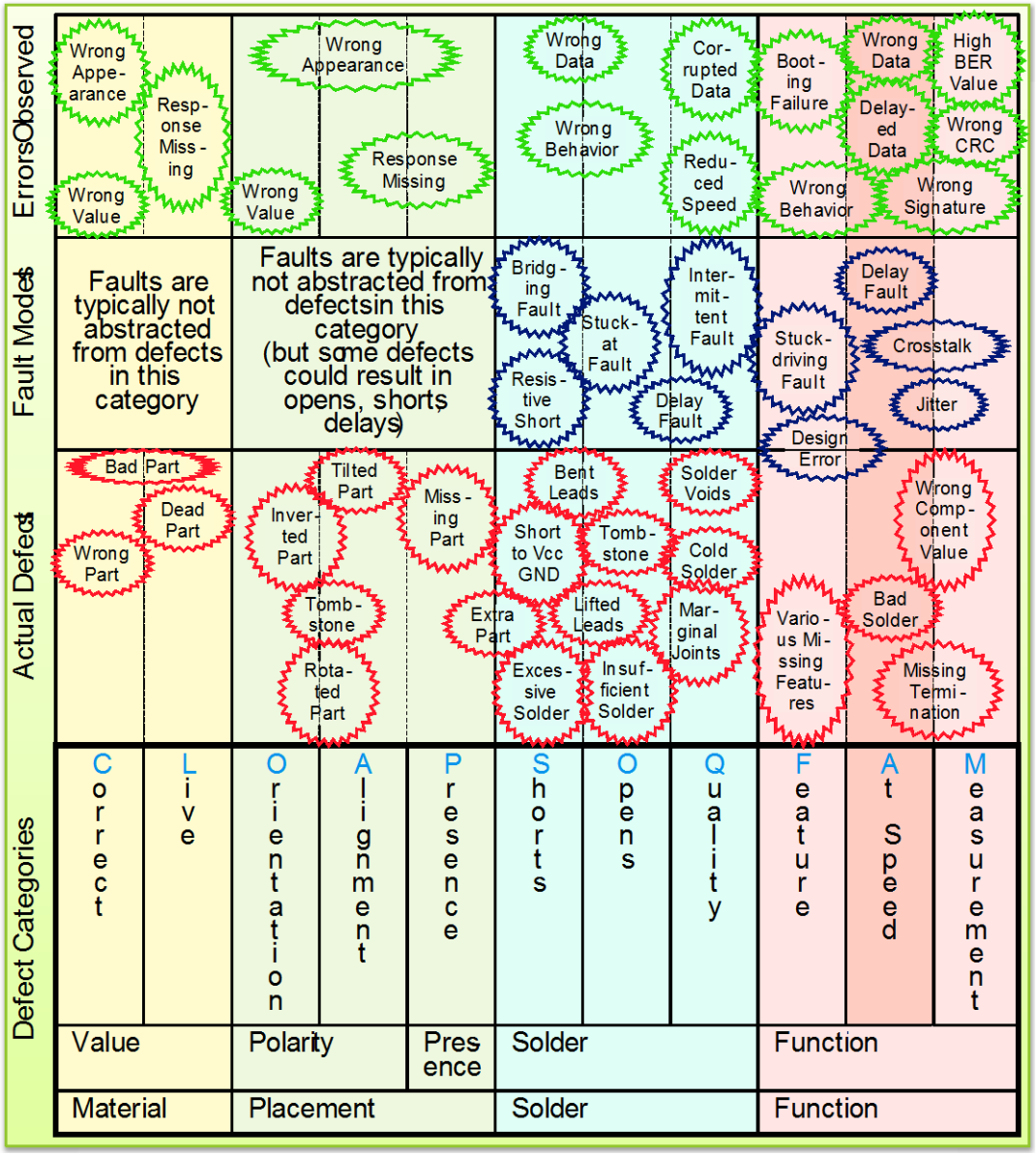

Table 1: Relationship between Defects, Faults, Errors and PCOLA/SOQ/FAM

Table 1 summarizes the relationship between PCOLA/SOQ/FAM [5], PPVS [18], and MPS [17] systems. It also lists examples of possible defects falling into each category. PCOLA and SOQ categories, and the respective defect universe, are well defined, providing a clear link between particular defects, faults, test coverage and test techniques. The defects of PCOLA section are directly testable by respective techniques. For example, the Presence and Orientation can be directly checked by the AOI and the value (Correct + Live) can be measured by the FPT. The SOQ category is well addressed by BST, whereas instead of SOQ, fine-grain fault models are widely

used in practice such as pin-level opens, stuck-at faults, bad driver faults, net-level shorts, etc. to both expand the SOQ category and abstract particular defects. Moreover, testing for faults instead of defect categories, would allow test compaction, and diagnosis that is more precise.

Before, pointing out serious shortcomings of the PCOLA/SOQ/FAM approach with respect of TRF (which is also part of D1.1) we provide some details on the way the test coverage has to be calculated, which is quite an ad-hoc and leaves some dangerous ambiguity in measuring the quality of test.

The PCOLA/SOQ test coverage methodology suggests assigning 0-value for missing coverage under specific categories per component, net or pin. Value 1 will be assigned in case of full coverage, while an intermediate value (e.g. 0.5) corresponds to partial coverage. The rules of assigning intermediate value depends on the category and might even be expert-driven (pen and paper method).

Although being rather straightforward for PCOLA/SOQ, the metrics are rather ambiguous for the FAM part. First of all, the list of features in the 'Feature' category is not systematically enumerated but it is rather expert-defined. In the context of the current paper, it is important to point out that the 'A' category (At-Speed Test) does not address the question "what was tested at-speed and how?" According to the current methodology it is enough to know that test stimuli can be applied at-speed in order to declare the part is fully at-speed tested, or even assign an abstract 0.75-value knowing that the majority of pins are tested.

The following important questions remain unanswered: Was it a test for both the raising and the falling transitions or just one of them? Was the crosstalk addressed? Was the jitter also measured? In fact, the current methodology suggests that; if there is a functional test running on the in-system processor, then, with certain generalization, all pins of the processor can be marked as at-speed tested (i.e. 1-value for all). Such approach is good for test coverage prediction. It is less effective at the production, as it reflects the testability, rather than the real achieved fault coverage.

It is important to point out that each defect category embraces a collection of defects that could be represented by a set of fault models. In fact one fault model can represent several defects. For example, a delay fault (transition is late to arrive) can be observed due to presence of any one of the defects: major solder voids, missing termination, wrong value of an in-line serial resistor, parametric variations or environmental conditions.

Expansion of abstract defect categories in the FAM section, by defining fine-grain truly quantitative fault coverage based on enumerated faults, would allow better control over the quality of tests, as well as over the potential test escapes caused by TRFs. Such expansion is proposed in the next section.

2.2 *Interconnect-Level Delay Faults*

The at-speed defect category is actually a way to measure the quality of tests (primarily functional test) that target defects affecting signal integrity. For example; bad termination, incorrect serial resistor value, cracks or voids in soldering – all of them essentially belonging to other defect categories, e.g. Correct, Live, Presence, Open, Quality. Hence, the At-Speed category reflects an alternative way to test for these defects. In other words, the approach considers the effect observed (delayed data, wrong

data) and the way of test application as opposed to the defect category. Therefore, an abstract fault model, collectively representing these defects, has to be the primary target of respective tests. Faults like delay faults, crosstalk, jitter are typical examples.

When adopting a new fault model, it has to be taken into account both the adequacy of addressing a particular class of defect and the ease of implementation of the model in the industrial environment. Therefore it is required to narrow down the general notion of delays to the task in hand.

A novel approach is proposed, based on typical pin-level and net-level *static* fault models, typical for JTAG/BS test. The modeling concept is simply extended towards delay faults and double-pattern based tests.

	Type of Fault	Dynamic behavior	Static domain equivalent	IC-level fault equivalent	Test patterns
Pin-level	Pin delay fault	Slow to rise Slow to fall	Stuck-at 1 Stuck-at 0	Transition delay faults	0-1 pair on every pin 1-0 pair on every pin
Connection-level	Pin-to-pin delay fault	Slow to rise Slow to fall	Open fault	Path-delay fault	0-1 & 1-0 pair on all driver-receiver pairs on the same net
Net-level	Crosstalk errors	Glitch, Delay	Short between nets	Crosstalk	MAF tests (Maximum Aggressor Fault model)

Table 2: Novel timing fault modeling under the "A" category in PCOLA/SOQ/FAM

The new approach to timing fault enumeration, test and diagnosis, is summarized in **Table 2**. Three levels of delay faults are formulated: a) isolated delay associated with a single pin; b) cumulative delay on a connection between any two pins; c) a delay or signal distortion on a complete net (e.g. due to bad termination or a crosstalk).

The *pin-level delay* fault model is the simplest and the defect universe is relatively small. It is good to address isolated problems, like bad soldering on one pin. If the delay fault affects several segments of the net, or is related to a bad serial resistor, then it is not any longer enough to consider it as an isolated fault, it is required to ensure transition propagation along the whole path from the driver to receiver along the net. If a net has several drivers and several receivers then *pin-to-pin delay* fault model requires that each pair of pins has to be tested separately. The fault universe in this case will be larger, but the chance to detect subtle delays is increased. The Pin-to-pin delay fault universe is a superset of the pin-level delay fault universe. Hence, the test set generated for the former model will be guaranteed to also cover all pin delays.

The net-level fault model targets crosstalk between any two or more nets and in fact this concept is not new, but needs to be added to the test strategy.

An important limitation of the proposed fault model is related to the test methodology used to apply test patterns. If the source of patterns in the sending IC and the target in the receiving IC are not equivalent to the ones used during normal operation, then either

an additional delay or a shorter path could be observed during test. This fact highlights an important conclusion: that the best way to perform At-Speed tests for delay faults, is to run it during functional test by applying proper test stimuli, i.e. both rising and falling transitions according to the pin-to-pin delay fault model. Using a special test configuration may result in false alarms (over-testing) or test escapes.

2.2.1 Practical Considerations

The pin is considered fully tested if all requirements are satisfied as discussed below.

2.2.1.1 Pin Delay Fault

For the **driving pin**, the full coverage is achieved if both items below are true:

- Raising transition (01) is driven at-speed and sensed *at least once* at the receiver side on any other pin (not via the internal loop-back);
- Falling transition (10) is driven at-speed and sensed *at least once* at the receiver side on any other pin (not via the internal loop-back);

For the **receiving pin**, the full coverage is achieved if both items below are true:

- Raising transition (01), which was driven at-speed from any other pin (not via the internal loop-back) is sensed *at least once*;
- Falling transition (10), which was driven at-speed from any other pin (not via the internal loop-back) is sensed *at least once*;

For the **bi-directional pin**, the full coverage is achieved if all four conditions (two for the driver and two for receiver) are *all true*.

The test coverage figure can be calculated in three stages for the driver or receiver: where 0% corresponds to no transitions generated; 50% is achieved if one either rising or falling transition was exercised; and 100% is assigned for the fully covered pin. In case of bi-directional pin, the granularity is finer: falling/rising driven and falling/rising sensed. Instead of coverage percentage, a concept of full vs. partial coverage can be used per pin.

2.2.1.2 Pin-to-Pin Delay Fault

For the **driving pin**, the full coverage is achieved if both items below are true:

- Raising transition (01) is driven at-speed and sensed *at each receiver* on the same net (also via the internal loop-back);
- Falling transition (10) is driven at-speed and sensed *at each receiver* on the same net (also via the internal loop-back);

For the **receiving pin**, the full coverage is achieved if both items below are true:

- Raising transitions (01), which was consequently driven at-speed once at a time from *every other pin* on the same net (also via the internal loop-back) is sensed;
- Falling transition (10), which was consequently driven at-speed once at a time from *every other pin* on the same net (also via the internal loop-back) is sensed;

For the **bi-directional pin**, the full coverage is achieved if all four conditions (two for the driver and two for receiver) are all true.

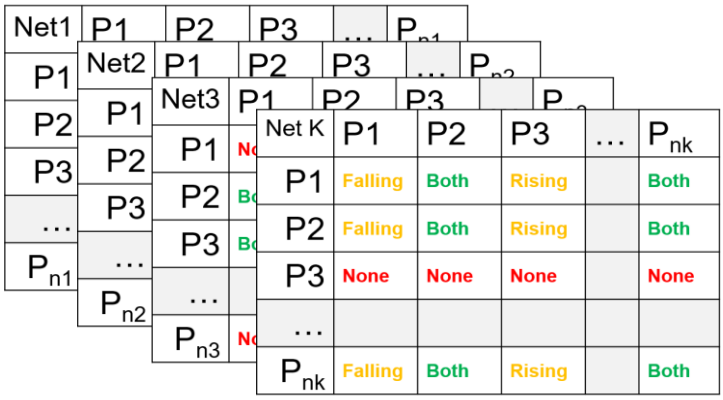

Figure 1: Pin-to-Pin Delay Fault Coverage tables for the board (all relevant nets)

2.2.2 Examples for the Pin-to-Pin Delay Fault

Example 1: net *N1* has 4 bi-directional pins, i.e. 4 drivers and 4 receivers, each can potentially drive and receive simultaneously. Test stimuli have been prepared so, that when pin *P1* drives at-speed, only two other nets can sense. The fault coverage for raising pin-to-pin fault at *P1* in this case will be 50%, because 2 out of 4 pins can only sense. The same coverage will be achieved for the falling pin-to-pin fault at *P1*. Cumulatively, this gives **50% pin-to-pin driving fault coverage** at *P1*. When pin *P1* reads at-speed, it can read rising transition from all other pins on the same net except for itself and it can read the falling transition from two other pins. That produces raising pin-to-pin fault coverage of 75% and falling pin-to-pin fault coverage of 50% at *P1*. Cumulatively, this gives **62.5% pin-to-pin sensing fault coverage** at *P1*.

The **total pin-to-pin fault coverage** at *P1* can be characterized by the average between sensing and falling transitions but it is recommended to keep them separately per pin.

The same principle should be used to calculate fault coverage at the other three pins *P2*, *P3*, *P4* on net *N1*.

Example 2: Five bidir pins on a single net with given test stimuli (see Table 3) result in cumulative TRF coverage of 52%.

Drivers → Receivers↓	P1	P2	P3	P4	P5	Receiver Coverage	
P1	Falling	Both	Both	None	Both	F: 4/5 R: 3/5	70%
P2	None	None	None	None	None	F: 0/5 R: 0/5	0%
P3	Falling	Both	Both	None	Both	F: 4/5 R: 3/5	70%
P4	Falling	Both	Both	None	Both	F: 4/5 R: 3/5	70%
P5	Falling	Both	Both	None	Both	F: 4/5 R: 3/5	70%
Driver Coverage	F: 4/5 R: 0/5	F: 4/5 R: 4/5	F: 4/5 R: 4/5	F: 0/5 R: 0/5	F: 4/5 R: 4/5	FD: 16/25 (64%) RD: 12/25 (48%) FR: 16/25 (64%) RR: 12/25 (48%)	
	40%	80%	80%	0%	80%		

Table 3: Insufficient stimuli on a 5-port net

Example 3: Different pins on a single net (three bidir, one input, one output). The same stimuli as in example 2 will produce cumulative TRF coverage of 87.5% (higher!). Raising transition on P1 has to be added to achieve 100% TRF coverage.

Drivers → Receivers↓		P1 bidir	P2 output	P3 bidir	P4 input	P5 bidir	Receiver Coverage	
bidir	P1	Falling	Both	Both	N/A	Both	F: 4/4 R: 3/4	87.5%
output	P2	N/A	N/A	N/A	N/A	N/A	F: 0/0 R: 0/0	N/A
bidir	P3	Falling	Both	Both	N/A	Both	F: 4/4 R: 3/4	87.5%
input	P4	Falling	Both	Both	N/A	Both	F: 4/4 R: 3/4	87.5%
bidir	P5	Falling	Both	Both	N/A	Both	F: 4/4 R: 3/4	87.5%
Driver Coverage		F: 4/4 R: 0/4	F: 4/4 R: 4/4	F: 4/4 R: 4/4	F: 0/0 R: 0/0	F: 4/4 R: 4/4	FD: 16/16 (100%) RD: 12/16 (75%) FR: 16/16 (100%) RR: 12/16 (75%)	
		50%	100%	100%	N/A	100%		

Table 4: Same stimuli, better coverage

3 Test coverage for Monitors

Hardware monitor is an embedded measurement system which follows one or more parameters (e.g.: voltage, current, frequency, temperature). These reveal the health of an electronic component, board or system.

It is usually activated after the product delivery, in order to ensure health monitoring during the product life cycles.

From the test coverage point of view, a monitor is similar to the test of a functional block, with no drive point and one or several sense points. The classic way of measuring functional coverage should be applied or adapted to monitors.

The defect categories which are tracked by the monitors fit with the BASTION research program. This section is studying how to qualify the test coverage as produced by the monitor. The monitor test coverage contributes to the overall test coverage and by reducing the escape rates, it minimizes the NFF phenomenon.

3.1 *Defects which should be detected by a monitor*

University of Twente focused on two fault categories in NFF: ageing and intermittent faults.

In deliverable D1.1, emphasis was placed on the investigation of ageing faults, resulting from NBTI (and HCI). Several health monitors (error-detection circuits and embedded instruments) have been investigated and some have been designed. To compute fault coverage it is first required to introduce the health monitoring here again.

In nanometer CMOS technologies, ageing effects tend to increase the threshold-voltage of single MOS transistors in time and therefore, reduce the drain current. The consequence is performance reduction for analogue/mixed-signal IPs.

An existing solution, for measuring the degraded performance, is to use an embedded-instrument (EI). These on-chip EIs are supposed to test basic physical parameters like voltages, currents, temperatures, as well as performance parameters of analogue/mixed-signal IPs.

In BASTION, a threshold-voltage measurement EI for MOSFETs was designed. It can measure the threshold-voltage of a MOS transistor, periodically and extract the change in threshold-voltage, caused by aging effects.

The threshold-voltage (V_{th0}) cannot be measured directly. Normally, it is extrapolated from the drain current measurement, at various gate and drain voltages with compact models. V_{th0} shift, caused by ageing, can be measured by comparing the difference in V_{th0} between a reference transistor and the DUT aged transistor.

Experimental results show that the proposed EI can characterize V_{th0} shift, with 3mV accuracy. It can be concluded that this EI can detect all BTI and HCI aging faults in a transistor. This results in full fault coverage for these kinds of faults.

The second category of faults is the intermittent resistive faults (IRFs) [20]. These have been discussed in deliverables D1.1 and D2.1. Several IRF detection sensors have been investigated and published, by the University of Twente, to detect IRFs at board and chip level [21], [22].

In [21], an enhanced version of IEEE standard 1149.4 was suggested, to allow online monitoring of IRFs in boards. To calculate fault coverage of this monitor, it should be considered that IRFs are characterized by their active time (pulse width) and range of

resistance changes. The proposed monitor can detect all pulses larger than 0.49 ns and with a resistance larger than 1kΩ. Providing that IRFs are in the resistance range [0.1kΩ-200kΩ] and the timing range [100ps-∞], then the fault coverage of the monitor is better than 99%.

To detect IRFs in chip level, an on-chip monitor has been proposed in deliverable D2.1 and published in [22]. The simulation-based experiment shows that the proposed monitor can detect all faults with a resistance larger than 70kΩ and active time longer than 0.6 ns. Providing IRFs are in range, [0.1kΩ-200kΩ] and [100ps-∞], then the fault coverage of the proposed monitor is 65%.

In order to calculate the fault coverage of this monitor, with regard to IRFs on boards, a UART on a FPGA has been implemented, with the capability of the proposed monitor, in IRFs detection. Experimentation included the injection of various real hardware faults [23]. The results show that the monitor can detect faults larger than 0.5kΩ and 1uS. Therefore, if IRFs that occur on boards are in the range of [0.1kΩ-200kΩ] and [100ps-∞] then the fault coverage will be roughly 98%.

4 Test Coverage Description file

In order to consider Section 2 (on at-speed-defects), and Section 3 (on monitoring coverage), a suitable method is needed to describe the test coverage produced by any given test step.

In order to design a flexible open solution, the Test Coverage Description file was designed as an XML database. The W3C standard helps to import, query, transform and export. It should contribute to a rapid adoption by the BASTION partners and the overall electronics industry.

Each BASTION tool is subject to generate a coverage report, which describes the contribution to higher test coverage and the contribution to lower escape rates resulting in less NFF.

```
<?xml version="1.0" encoding = "ISO-8859-1"?>
<!--XML-Data generated by TestWay (http://www.aster-
technologies.com)-->
<TestCoverage version="1.0" date="19-APR-2016 10:22">
    <Tools name="xxx" version="xx" vendor="yy"/>
    <Board name="xxxx" version="xx" partnumber="xxx"/>
    <TestList>
        <Test name="Testonica">
            <Target object="PinPair" name="U1-2,U3-2">
                <Defect fault="AtSpeed" category="Function"
class="Dynamic" efficiency="100%"/>
                <Defect fault="@0" efficiency="100%"/>
            </Target>
            <Target object="PinPair" name="U1-3,U3-3">
                <Defect fault="AtSpeed" category="Function"
class="Dynamic" efficiency="0%" comment="Unstable"/>
                <Defect fault="@0" efficiency="100%"/>
            </Target>
            <Target object="Part" name="U1">
                <Defect fault="Live" efficiency="50%"/>
            </Target>
            <Target object="Net" name="1N513">
                <Defect fault="AtSpeed" efficiency="100%"/>
            </Target>
        </Test>
        <Test name="Aging Monitor">
            <Target object="block"
name="EDIF20,aging_monitor.edn">
                <Defect fault="Live" efficiency="95%"/>
            </Target>
        </Test>
    </TestList>
</TestCoverage>
```

Figure 5: Test Coverage Description – XML format

The ASTER TestWay Coverage analyzer will import each report and show the contribution to reducing the escape rate. For the BASTION Demonstrator, ASTER

expects enough Test Coverage reports from all the software/hardware tools (monitors, new test instruments, new test methods...) to highlight their benefits.

The test coverage includes the test tool descriptor, the board descriptor and the test list. A test list is built around a list of tests, which target different objects: pin, part, net, pin-pairs (short, at-speed defects), or a schematic/layout block (linked with a formal netlist). Each test has certain efficiencies, for defect categories, which are listed in D1.1 - 4.3.2 - New class of board faults. New defect classes can be added in each of the defect categories as required.

5 Test Coverage analysis driven by real DPM

The majority of electronic industrial partners trust that test coverage is the key contributor for providing a better yield. A deeper analysis demonstrates that the reality is slightly different.

5.1 *Coverage by facets & test efficiency*

Each test technique brings, by the mechanism of stimulation and measurement, a certain ability to detect defects. This coverage spectrum is represented by various facets (MPS [17], PPVS [18], PCOLA/SOQ [3]).

These coverage facets can be used for a set of testers, distributed on the production line. For each facet, there is a defect category, which should be detected by the set of testers.

Combination of all these facets is needed to obtain a number representing the ability to capture the defects and therefore the test efficiency. The ASTER model is based on a coverage balanced by the defects opportunities.

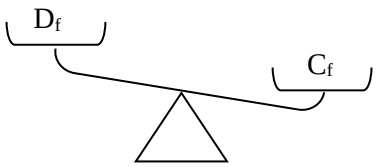

Figure 6: Balance between defects and coverage

For each category of defects (D_f, $f \in \{M, P, S\}$), we associate the corresponding coverage (C_f, $f \in \{ M, P, S\}$).

$$\text{Coverage} = \frac{\Sigma D_M \times C_M + \Sigma D_P \times C_P + \Sigma D_S \times C_S}{\Sigma D_M + \Sigma D_P + \Sigma D_S}$$

Figure 7: Weighted Coverage = Test efficiency

This formula is easily extended for new classes of defects. It also shows that DPM has a similar importance to the measurement of the test efficiency.

5.2 *QuadDPMO: True Defect Opportunities*

Both DPM and DPMO are used for determining the overall quality of the UUT, produced from the sample quantity inspected. DPM is a measure of manufacturing throughput (how many bad parts slip through the manufacturing process). DPMO is a measure of performance (how many times a manufacturing defect class occurs). DPMO is an indicator of which manufacturing process is in need of improvement.

Six Sigma is a scientific methodology that strives to achieve perfect quality. Whilst Lean Manufacturing focuses on waste reduction, Six Sigma strives to reduce waste and:

- Understand and reduce product or process variation
- Improve performance (improve the mean)
- Improve customer satisfaction

Sigma is a measure of process variability, or spread. The higher the sigma level, the fewer defects the process creates (refer to Table 8). Six sigma experts use DPMO values to determine the process sigma level.

Sigma level without 1.5 σ shift	DPMO without 1.5 σ shift	Sigma level with 1.5 σ shift	DPMO with 1.5 σ shift
1.0	317,311	1.0	697,672
1.5	133,614	1.5	501,350
2.0	45.500	2.0	308,770
2.5	12,419	2.5	158,687
3.0	2,700	3.0	66,811
3.5	465.35	3.5	22,750
4.0	63.37	4.0	6,210
4.5	6.8	4.5	1,350
5,0	0.574	5,0	232.67
5,5	0.038	5,5	31.69
6.0	**0.002**	**6;0**	**3.40**

Table 8: DPMO to Sigma level conversion

DPM levels are commonly used to monitor the quality of a UUT in production and determine the quality levels on the production line. Since DPMO is inversely proportional to the defects per unit (DPU), the DPMO can be manipulated by changing the DPU. This is possible because defect opportunities per unit are defined by users, prior to making the DPMO calculation.

For this reason, a link to NFFs at board-level is suspected. Within the scope of the BASTION research program, a new concept is being developed by ASTER, to analyze the NFF phenomenon using a software tool. The QuadDPMO algorithm application is under development to:

- Collect & understand, in-real time, the DPMO,
- Group defect labels and root causes, by defect class,
- Compute long term, medium term and short term DPMO metrics,
- Investigate common areas of occurrence for each defect class.

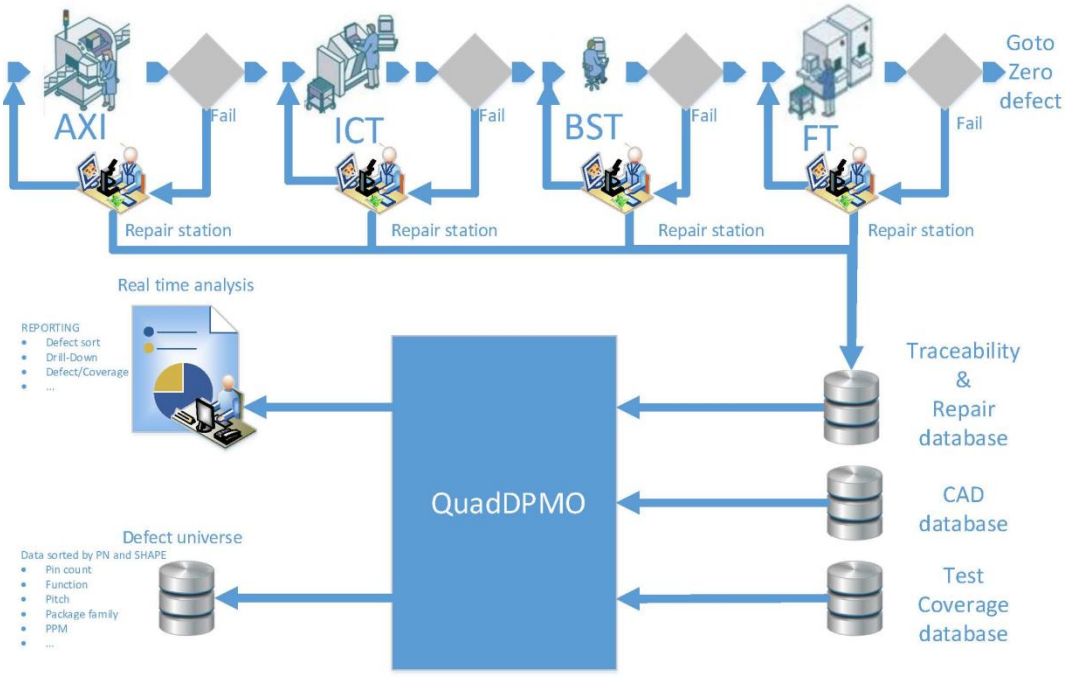

Figure 9: QuadDPMO synopsis.

QuadDPMO produces many reports where test data can be analyzed by site, period of time, test station, batch ID and product ID. It gives access to detailed reports where the defect family, defect code or defect label, can be sorted by various attributes, such as: pin count, pitch, mounting technology, mounting side, JEDEC shape, manufacturer, component function, board complexity, board type…

The chart (pie or bar graph) color code is automatically transferred to the layout, or schematic views, in order to verify that the defect occurrence is linked with a physical or logical location (functional block).

5.3 *Using real DPM in order to measure test efficiency*

As the QuadDPMO database includes CAD Data, test coverage metrics as well as test & repair information, it is possible to extract the real DPM per component population.

With the experiments that have been completed, the defect database represents more than 100,000 defects, which has identified two clear problems.

1. The DPM attached to a defect category/component is a pretty small population. From the statistical point of view, this population is too small to be considered as representative.
2. Even if the population is large enough, a new design may, use a new component, which is unknown in the QuadDPMO database and subsequently the defect probability will be unknown.

In order to overcome the two difficulties, a population hierachy has been created, which should provide a DPM number that is as precise as possible.

Defect category	Ideal group	Alternate1	Alternate2
Material	PartNumber	PartNumber	Function, pin count & package family
Placement	PartNumber	Shape	Function, pin count & package family
Solder	PartNumber	Shape	Function, pin count & package family
Function	PartNumber	PartNumber	Function, pin count & package family

Table 10: DPM grouping selection

Initially, the population grouping is by PartNumber. If the resulting population is not large, another grouping possibility should be evaluated (see Alternate1 and Alternate2 selection columns in Table 10: DPM grouping selection).

From processing this data, a DPM table is produced which highlights the amount of PPM per defect category. The PPM information can be imported by the test coverage tools in order to measure the deviation between the theoretical defect rates and the real defects, extracted from the traceability & repair database.

There are two strategic benefits:

1. If the theoretical defect rate is higher than the real DPM, test coverage has been developed to detect defects that do not occur, or only rarely. This provides an opportunity to optimize the test strategy, by focusing only on the most probable defects. This optimization could be static (done one time for the overall board production), or dynamic (adjusted in real time by disabling some tests when the DPM is decreasing). The dynamic mode can facilitate an increased throughput,

when a test becomes a bottleneck of the production line. Alternatively, specific test lines could be selected based on their capability to detect certain defects, thereby tuning the test line to the product being manufactured.
This capability could be expanded to allow OEM companies to select an EMS company, based on their process capability as reflected by their DPM figures.

2. If the real DPM is higher than the theoretical defect rate, it means better test coverage is required on this component, in order to prevent a higher escape rate, which, in turn, contributes to the NFF phenomenon.

In Europe, the board manufacturing is mainly high-mix low-volume; QuadDPMO must overcome some unexpected situations.

- When the production starts on a new lot, the first set of boards is used to tune the production line and may contain an abnormal amount of defects. This phenomenon should be neutralized in the DPM computation by ignoring the first number of boards which are produced when a new lot is launched.
- As the number of boards produced might be low, some part numbers might appear a limited amount of times. This inhibits an accurate DPM computation. In order to overcome this issue, QuadDPMO exports several sets of DPM, based on a different key (PartNumber, shape, pin count/pitch/function). Due to the small database used for experimentation, DPM is exported for Material, Placement and Solder. When the population is lower than a certain limit, instead of the DPM, QuadDPMO exports "NA" for Not Applicable. The Figure **11**: TestWay strategy file – load DPM from QuadDPMO, highlights the priority order for the DPM usage.

The TestWay QuadDPMO.ts has been designed as follow:

```
!    Load DPM per priority:
!    1. Default value per pin count/pitch/function
!    2. Per shape
!    3. Per partnumber
!
!    "Na" means "Not Applicable". It is not loaded.
Requirements:
     Call file VISAROOT:aPinCnt.csv
     Call file VISAROOT:aShape.csv
     Call file VISAROOT:aPartNumber.csv
```

Figure 11: TestWay strategy file – load DPM from QuadDPMO

5.4 *Case study*

Based on the QuadDPMO database collected in T1.1, experimental results are as follows:

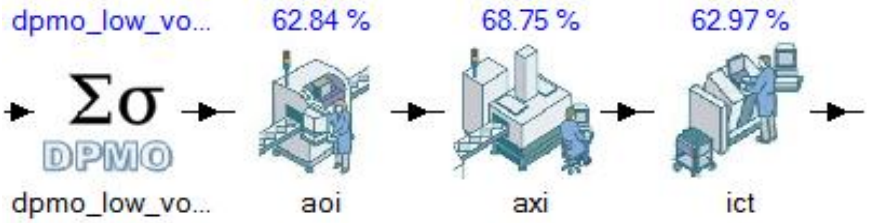

Figure 12: Test Coverage with standard DPM

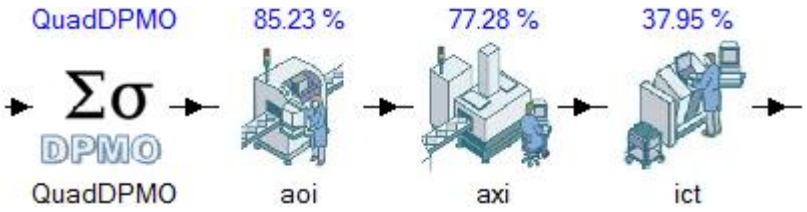

Figure 13: Test Coverage with real DPM

The inspection, AOI and AXI, target the defects which occur more often. Then the weighted test coverage increases whereas ICT is just the reverse and the test coverage is reduced.

Complementary research has been launched, with the test coverage matrix, in order to understand the link between DPM and test coverage.

6 Test Coverage Matrix

6.1 *Defects covered vs. detected*

ASTER has designed an innovative test coverage matrix, to classify defect occurrences against test coverage. A typical managerial report is created, where in one page, all critical information is presented: “Convert data to information” since information is used to make decisions.

There are 4 cases detailed in Figure **14**: Innovative TestWay Coverage Matrix:

- Faults which have been detected and are subject to be covered: This number shows the effective test coverage which is used. The difference between this number and total test coverage highlights the test coverage which has been produced but never used due to “no defect” occurrence. It opens the opportunity for cost savings with a test development driven by defects that really occur.
- Faults which have not been detected and are not covered. It is the typical definition of Insufficient Coverage.
- Faults which are detected in contradiction with the coverage: the test coverage is clearly under estimated. The coverage report generated by the test equipment must be updated to reflect the true test efficiency.

- Faults are not detected and are supposed to be covered: the test coverage is over estimated. This contributes to increased escape rates and NFF.

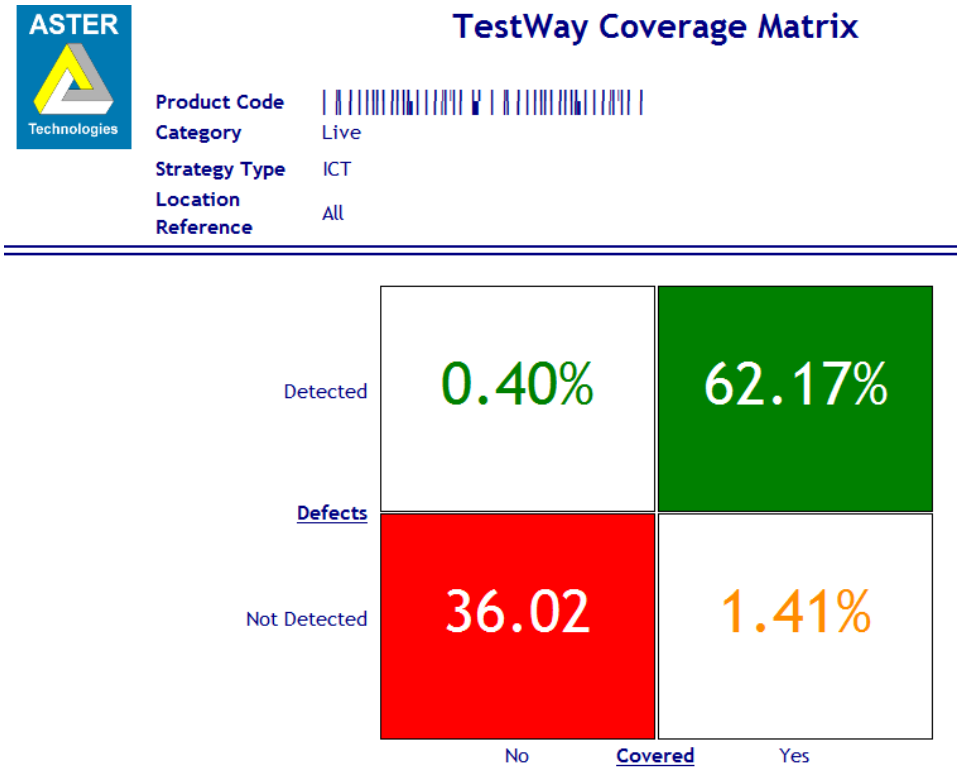

Figure 14: Innovative TestWay Coverage Matrix

6.2 *Coverage matrix variation*

Depending on the purpose of the analysis, different variants of the coverage matrix have been identified.

Each inspection or test equipment is able to detect a set of defects.

'Not detected' is initially unknown because it has not been established if the defect has never occurred or if it has been not detected due to insufficient test coverage.

The variants of the coverage matrix have been designed to explore the 3 objectives.

6.2.1 Incremental contribution

As the inspection and test are executed in line, the previous test steps are unknown or should be ignored: Figure **15**: Coverage Matrix – Incremental contribution If we are evaluating strategy B, the following test helps to identify the population of "Not detected" defects (c, C, n, N). If a test fails in the subsequent test, strategy C or N, QuadDPMO considers that the defect was already on the board and should have been addressed by the test strategy B.

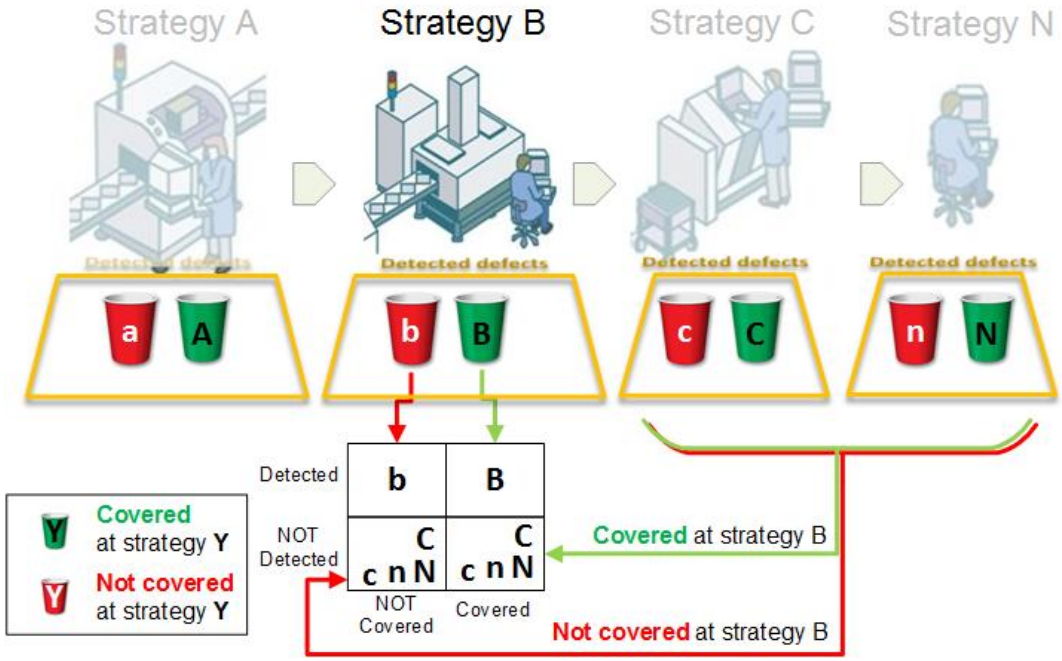

Figure 15: Coverage Matrix – Incremental contribution

6.2.2 Contribution to total

In order to evaluate the contribution of one test step in the complete test line, QuadDPMO considers the overall population of defects (a, A, c, C, n, N) which has been detected by, at least, one test strategy.

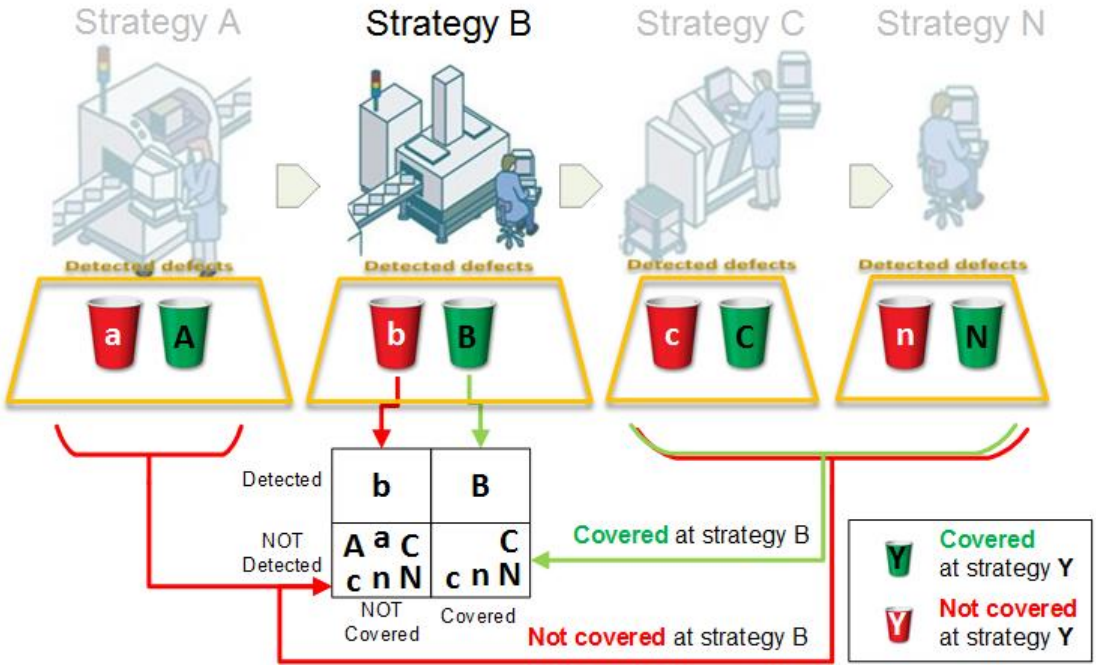

Figure 16: Coverage Matrix –Contribution on total

6.2.3 Unique contribution

The overlapping test coverage through the complete test line, gives the impression that a strategy is contributing to a higher coverage, where most of the defects could be detected by a combination of test strategies or another test strategy .

Coverage Matrix-Unique contribution is looking at the defects that should be detected exclusively by the strategy B and not detected by any other strategy.

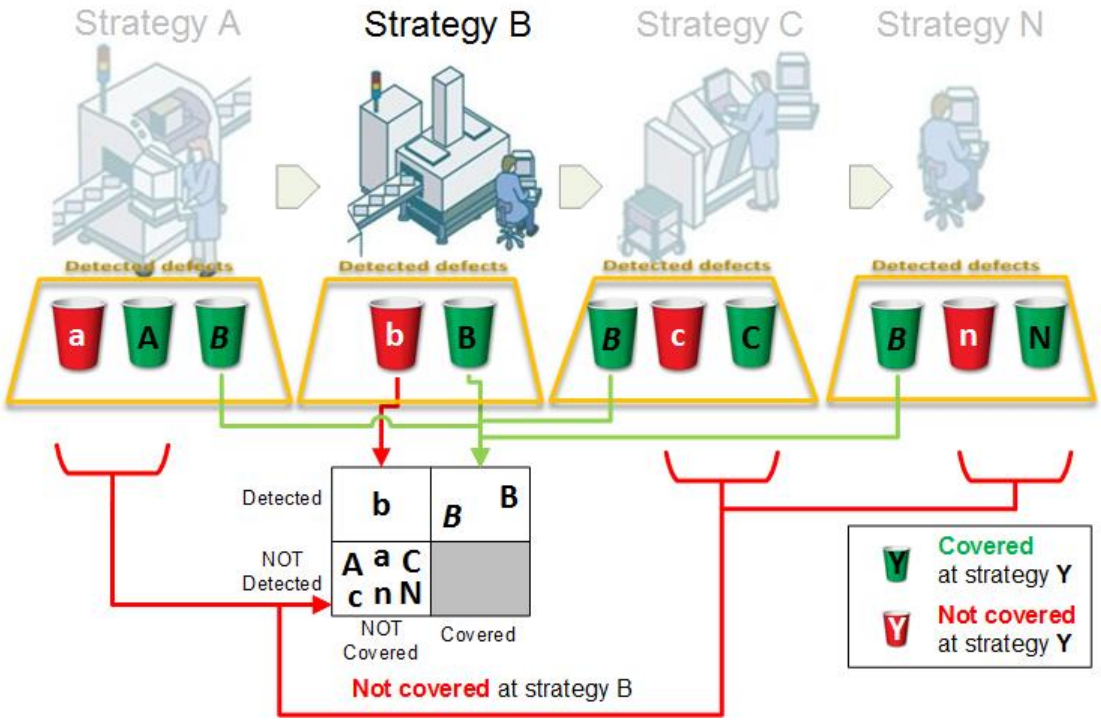

Figure 17: Coverage Matrix –Unique Contribution

6.3 *Case studies*

The QuadDPMO database has been compiled based on production data from various industrial partners. See D1.1 for complementary information.
A data sample reflecting one million boards should contribute to more precise results from the statistical point of view. The QuadDPMO data set is large enough to see how the new coverage metrics should be used to identify issues at AOI, AXI, ICT and FCT. To report the coverage, 1663 boards have been used that produce 3186 defects in total on the test line.

6.3.1 Study: Incremental Contribution

Figure 18: Incremental Contribution per test strategy

The first matrix (displayed on the top left in Figure 18) summarizes the AOI results, showing that 53.4% - 6.85% + 46.59% - of the overall defects are captured from the first inspection strategy.
28.96% of test coverage has never been used as the defect has never occurred.

The second matrix (top right) summarizing the AXI results shows that 95.05% - 9.94% + 85.11% - of the defects (including the one from AOI) are caught.

The third matrix (bottom right) summarizing the ICT results shows that 99.01% - 40.59% + 58.42% - of the remaining defects are caught.

The last matrix (bottom left) summarizing the FCT results shows that the last known defect is caught.

6.3.2 Study: Test Contribution per defect class

PCOLA/SOQ defect models were used in order to analyze the test contribution of each strategy.
The defect universe for components includes:

- Presence (the component is present)
- Correctness (it is the correct component)
- Orientation (if the component is polarized, it is not rotated. For a QFP or BGA, the component is not rotated by 90, 180 or 270 degrees)
- Live (the component is basically alive - not a full functional qualification)
- Alignment (the component is properly centered, free of skews or small rotations)

The defect universe for component pins includes:

- Shorts (unwanted continuity to other nearby connection points)
- Opens (lack of continuity between component and the intended board connection)
- Quality (free of malformation, excess or inadequate solder, cold solder voids, etc.)

6.3.2.1 Presence

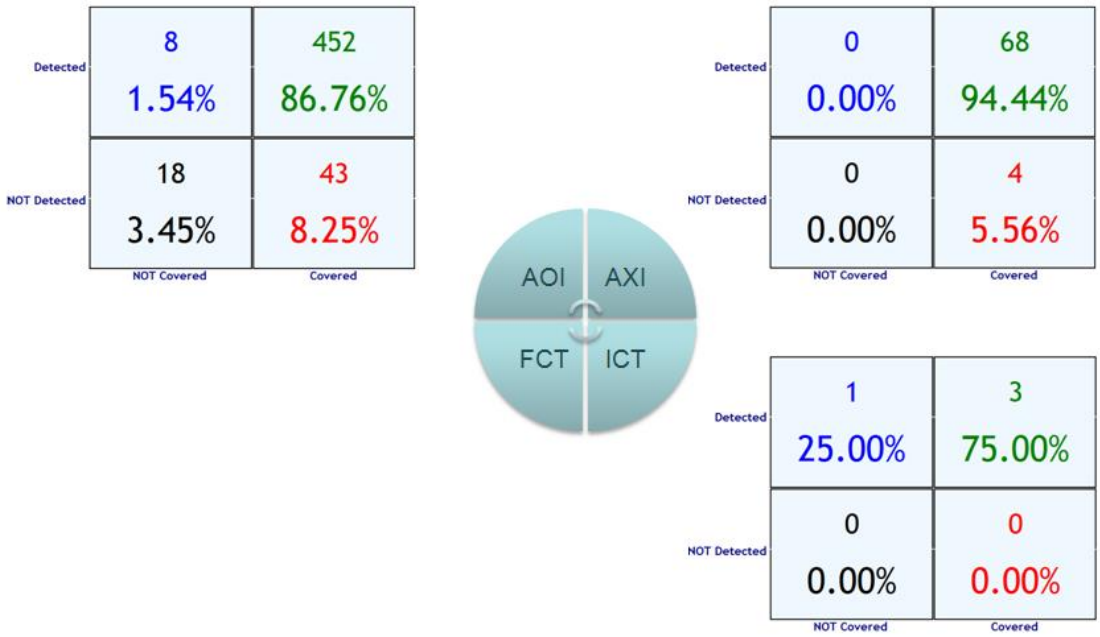

Figure 19: Test Contribution per defect class (Presence)

The inspection technique catches most of the "Presence" defects, but it was noticed that 4 defects are still detected at In-Circuit Test.

6.3.3 Correctness

Figure 20: Test Contribution per defect class (Correctness)

"Correctness" is checked by OCR applied at AOI. With small packages, it is highly probable that the component reference will not be written on the component body or be unreadable.

6.3.4 Orientation

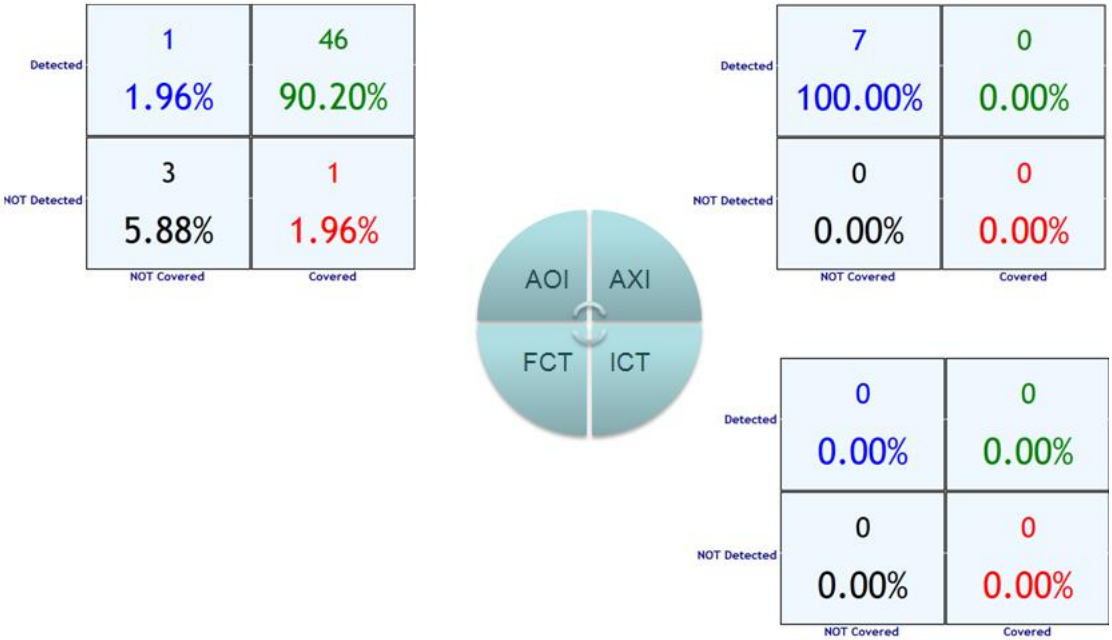

Figure 21: Test Contribution per defect class (Orientation)

Even if AOI is the easiest way to catch orientation issues, AXI is better for polarized capacitors (notice the 7 escapes that result from AOI).

6.3.5 Live

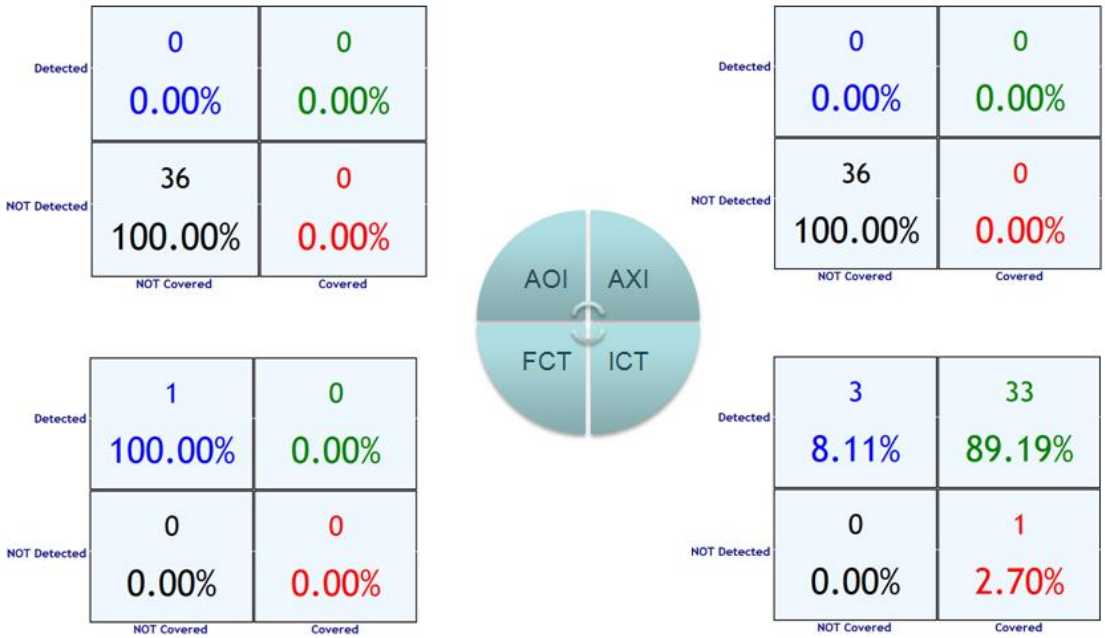

Figure 22: Test Contribution per defect class (Live)

The ICT and FCT are good in component validation. As the QuadDPMO database is built including some avionics product, it is likely that the qualifying components (High SPQL for Avionics) considerably reduce the level of "Live" defects.

6.3.6 Alignment

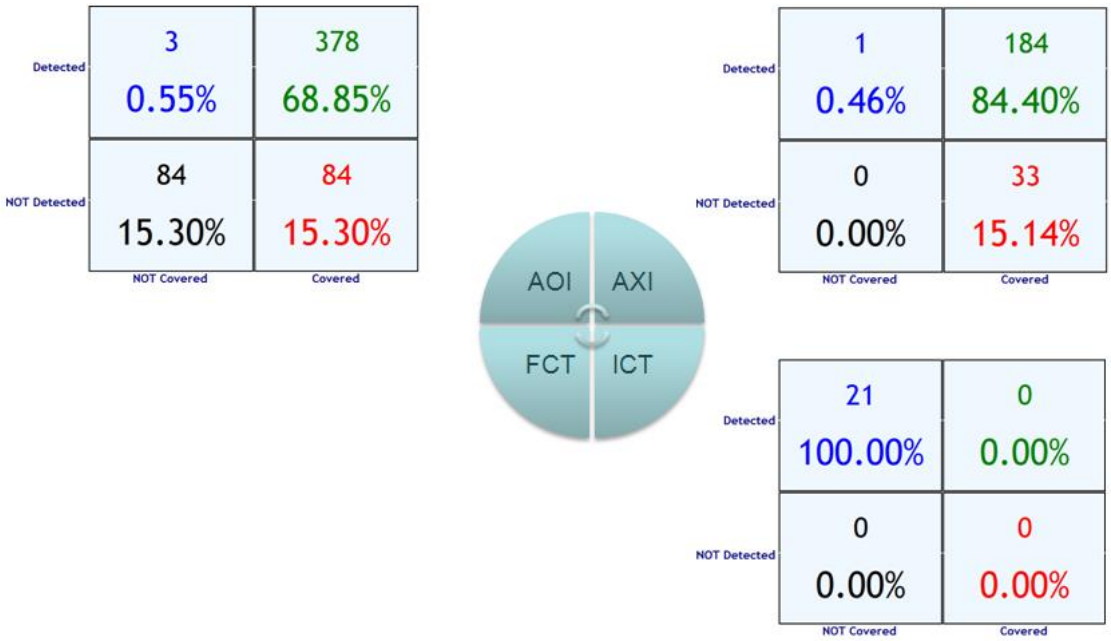

Figure 23: Test Contribution per defect class (Alignment)

"Alignment" is the typical type of defect which is targeted by inspection. Still, it was noticed that 21 defects of this type were detected at In-Circuit test. After investigation, it is electrical short circuits caused by misaligned components. During the repair process, the fault has been re-qualified as a "misaligned" defect (as the root cause). From the test coverage point of view, ICT is not capable to catch such defects and so the 21 defects (see Figure 23) appear in Detected/Not Covered.

6.3.7 Short

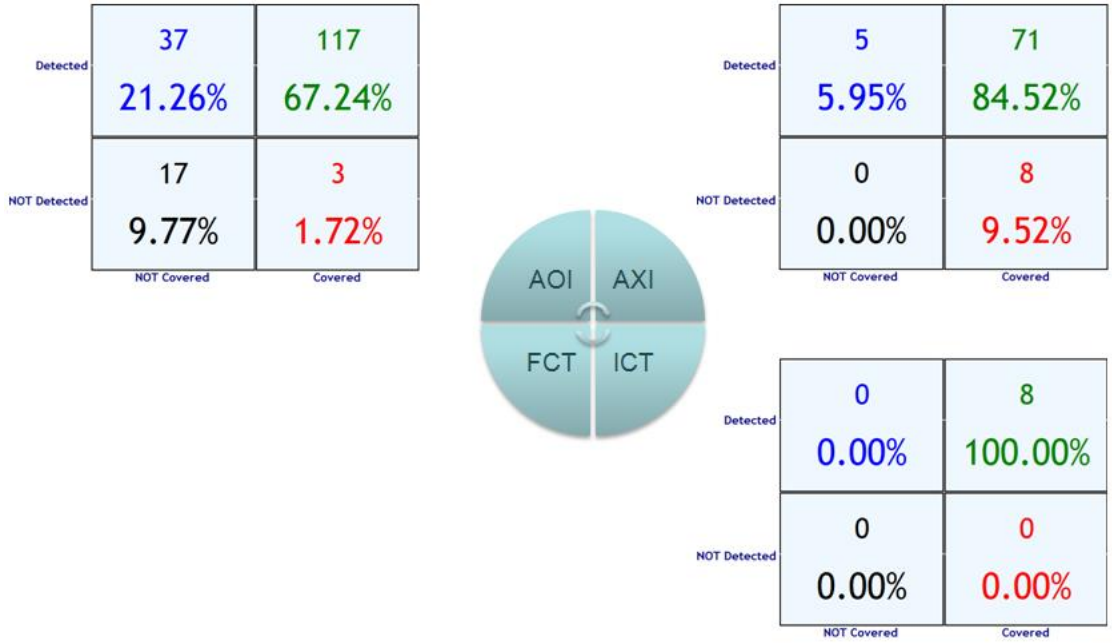

Figure 24**: Test Contribution per defect class (Short)**

AOI and AXI were unable to capture all possible "Short" defects, as the inspection is done pin-to-pin and so other short circuits like trace-to-trace, via-to-trace or via-to-pin cannot be detected.

6.3.8 Open

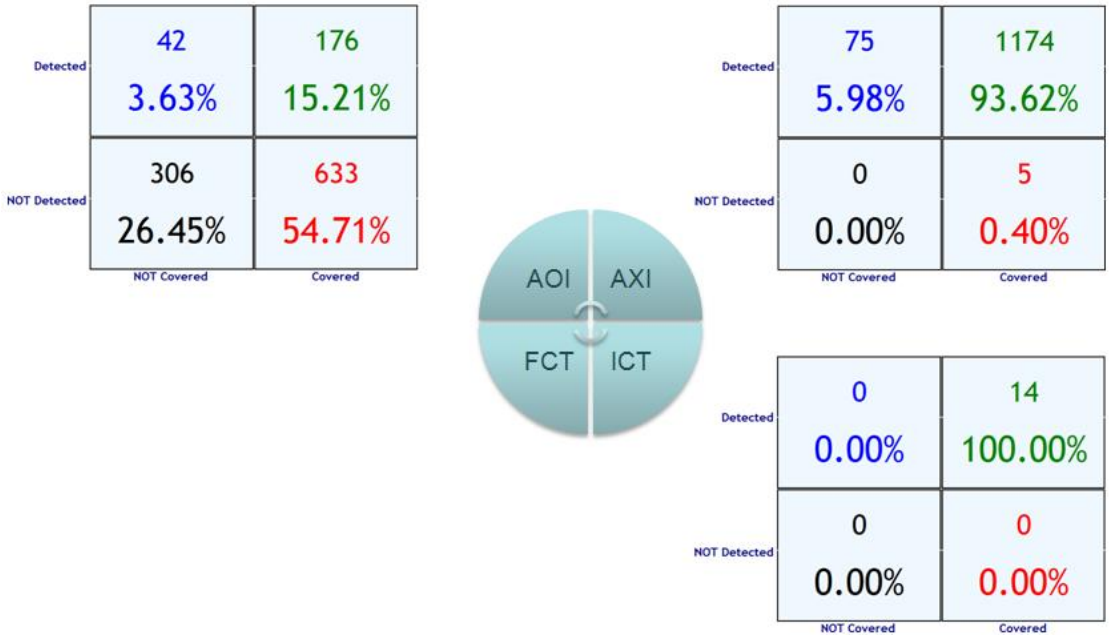

Figure 25**: Test Contribution per defect class (Open)**

AXI proves to be the best contributor to catch "Open" defects, even if the electrical test has a low level contribution with 14 defects detected, some of these defects are critical from the FMEA risk analysis.

6.3.9 Quality

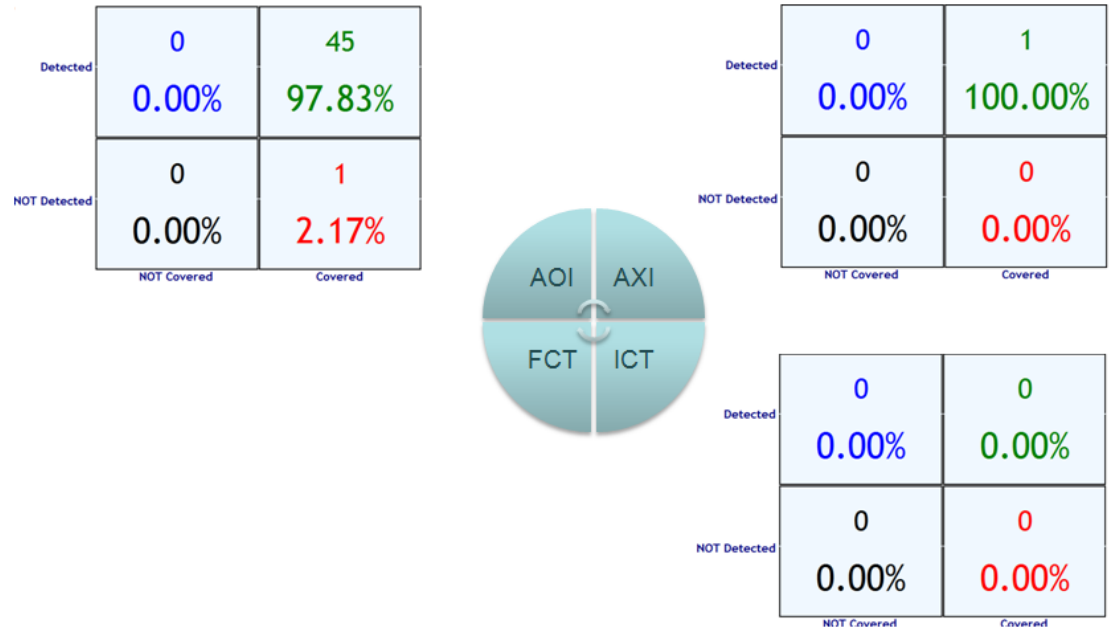

Figure 26**: Test Contribution per defect class (Quality)**

"Quality" is the typical type of defect which is targeted by inspection. Most of the defects are captured by AOI, because it is looking at the shape of the solder joints. One defect is detected by AXI due to voids (undetectable by AOI).

6.3.10 Defect universe

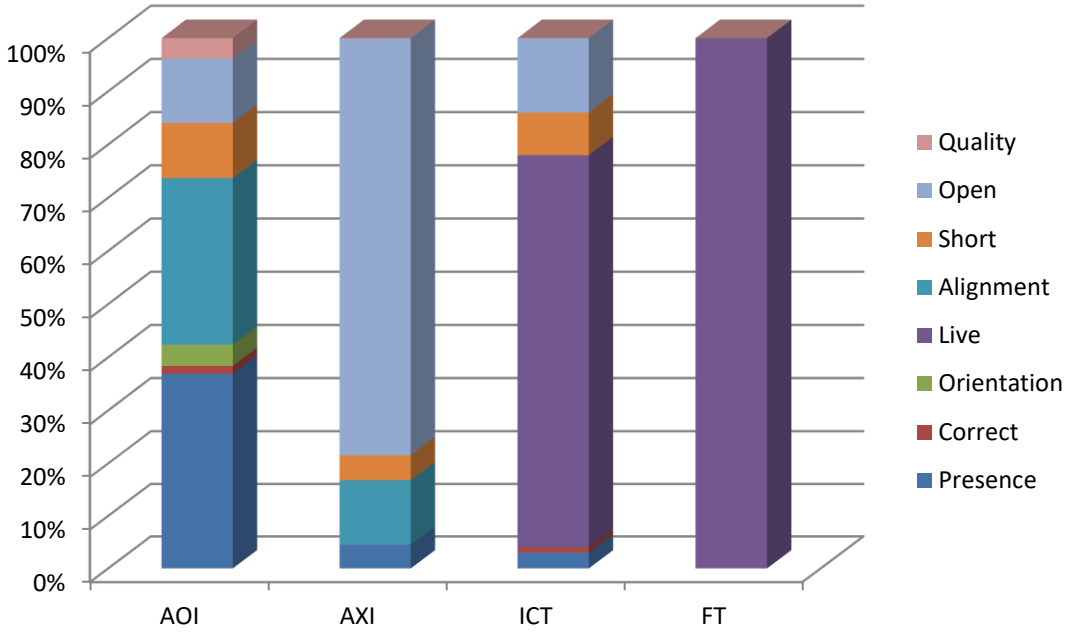

Figure 27: Defect distribution

The Figure **27**: Defect distribution, highlights that the “Presence”, “Alignment”, “Quality” and “Open” are targeted more by inspection techniques: AOI and AXI, whereas the ICT is targeting “Live”. It also contributes to complementary “Open” and “Short” detection. The FT is contributing almost exclusively to validate the function and therefore the “Live” defects.

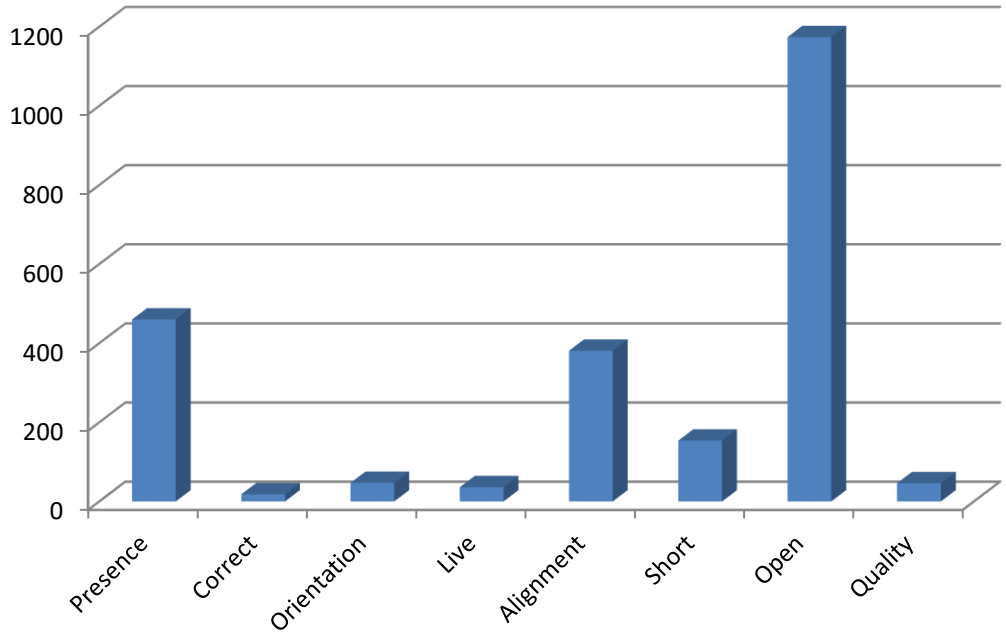

Figure 28: Defect Universe

The Figure **28**: Defect Universe, highlights that the majority of defects are due to manufacturing processes. It is perfectly logical as in a double reflow soldering process, the "Open" category is the main contributor. The solder paste is reduced as much as possible to avoid micro-balls of solder rolling on the bare board (risk of short) and insufficient solder is prone to create "Open" defects.

The QuadDPMO database includes an important proportion of avionics products. These modify the perception of the "Live" defect rates. In the avionics industry, all components benefit from a higher level of test and a better SPQL.

7 Conclusions

Based on the D1.1 conclusion, the most important contributor to NFF was narrowed down to insufficient coverage; whereas intermittent resistive and timing related faults were confirmed to be challenging issues due to lack of respective test techniques or test coverage metrics. Ageing is the second largest contributor, as stress testing is not yet widely used by board assembly companies. Lack of communication between the design and manufacturing departments has a measurable influence on the final product quality. There is no systematic strategy to test timing faults at board level to enable estimation of the quality of test in terms of fault coverage.

QuadDPMO is built around a centralized and open architecture database, for providing traceability of any PCB. It allows accurate retrieval of data and conversion to meaningful information. This information can be used to fine tune the product life-cycle.
Improving product yields does not simply mean better product quality at a lower cost, but also acquiring a deeper understanding of the whole manufacturing process by making full use of manufacturing information. This can lead to improved product reliability, prevention of re-occurring defects, improved future product designs and increased competitiveness. Processes must be monitored before they can be controlled, which often means collecting data from a number of incompatible sources.

Two major BASTION KPIs have been addressed in this deliverable with the new coverage metrics:

1. Identification of at least 2 new fault classes contributing to NFF
2. Reducing test escapes and impact of NFF at least by the factor of 2.

KPI – Identification of at least 2 new fault classes contributing to NFF

This KPI is addressed by two new fault classes (or special sub-classes) proposed in frames of BASTION:

1. Board-level Timing Related Faults (TRF) including *pin-level* and *connection-level* transition faults modelled at interconnect between components. These particular types of faults have never been considered in literature. They have not been known to the industry either. However, these sub-types of a more general delay fault model allow fine-grain grading of at-speed test techniques and test patterns used at board-level test.

2. IC-level Intermittent Resistive Faults have been demonstrated in frames of BASTION to be a real existing class of defects developing as a result of wear out and hence they need to be tested during the product lifetime.

KPI - Reducing test escapes and impact of NFF at least by the factor of 2

Test escapes at IC level are mainly caught during board-level test. For board-level, the defects which are detected during integration or system-level test should have only two following sources:

1. The defect appears on the board during the integration. The board test is not able to detect the defect, due to lack of coverage (*Slip*), wrong coverage metrics, or a defect universe misaligned with the industrial reality.
2. The defect occurs later, after board test (aging or damage) and/or is intermittent.

The BASTION contribution in terms of new coverage metrics deeply contributes to reducing NFF:

- Not implemented test step: the survey (D1.1 – Figure 26 – Test line) demonstrates that all suppliers are not using all the spectrum of available inspection or test strategies. Some of these test strategies are unique contributors as they are the only station capable to catch this category of defects.
    - The Figure 17: Coverage Matrix –Unique Contribution – is a key tool to understand how a test line must be designed to cover the whole defect spectrum.
    - The stress test is not widely used, as revealed by the survey ((D1.1 – Figure 26 – Test line)). Outside of the industrial partners which fulfilled the survey AXI or SPI are not yet widely adopted. QuadDPMO, has highlighted the defects which are detected by these inspection & test approaches. When some tests are missing, it is prone to deep contribution to NFF.
- Missing test techniques - NFF is also due to defects which are “unclassified” or not specifically targeted by a test instrument. The “at-speed” or “ageing” defects are good examples. The production lines of the BASTION industrial partners do not include any instruments to qualify faults as a root cause of “at-speed” or “ageing”. So the analytics don’t show any of these defects in the statistical table or charts. But they do exist in the proportion which is unknown prior to implementation of the new instruments or new coverage metrics.

The innovations and tools resulting from the BASTION research program provide a measurable performance. The production model (D1.1 – Figure 20) explicitly shows the escape rate. By measuring the DPMO and measuring & increasing the coverage (new instruments and coverage metrics), BASTION can reduce significantly the NFF, even if it must be admitted that it cannot be proven that this methodology results in exactly a factor of 2 or more. This aspect will be addressed by the BASTION demonstrator.

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