FP7-ICT-2013-11-619871

BASTION

Board and SoC Test Instrumentation for Ageing and No Failure Found

Instrument: Collaborative Project
Thematic Priority: Information and Communication Technologies

Demonstration plan
(Deliverable D6.1)

Due date of deliverable: June 30, 2015
Actual submission date: September 10, 2015

Start date of project: January 1, 2014 Duration: Three years

Organisation name of lead contractor for this deliverable: Testonica Lab

Revision 1.9

Project co-funded by the European Commission within the Seventh Framework Programme (2014-2016)		
Dissemination Level		
PU	Public	☒
PP	Restricted to other programme participants (including the Commission Services)	☐
RE	Restricted to a group specified by the consortium (including the Commission Services)	☐
CO	Confidential, only for members of the consortium (including the Commission Services)	☐

Notices

For information, please contact Artur Jutman, e-mail: artur@testonica.com

This document is intended to fulfil the contractual obligations of the BASTION project concerning deliverable D6.1 described in contract 619871.

© Copyright BASTION 2015. All rights reserved.

Table of Revisions

Version	Date	Description and reason	Author	Affected sections
1.0	June 8, 2015	Structure created	A. Jutman	Contents
1.1	June 15, 2015	Intro and summary sections	A. Jutman	Contents
1.2	June 19, 2015	Update of Chapter 3 sections, integration of inputs from partners	C. Lotz, E. Larsson, M. Sonza-Reorda, R. Krenz-Baath, P. Engelke, A. Jutman	All sections in Chapter 3
1.3	June 23, 2015	Sections 3.2 and 3.8	J. Raik	3.2, 3.8, References
1.4	June 26, 2015	Section 3.9	A. Jutman	Contents
1.5	July 3, 2015	Update and extension of demonstration use case descriptions in Chapter 3	E. Larsson, A. Jutman, P. Engelke	Chapter 3
1.6	July 30, 2015	Update of demonstration scenarios	A. Jutman	Chapter 3
1.7	August 17, 2015	Update of Introduction and platform description	A. Jutman	Chapters 1 and 2
1.8	August 21, 2015	Important updates in all parts of the document	A. Jutman, E. Larsson	All sections
1.8b	August 26, 2015	Pictures in Section 2 updated	A. Jutman	Chapter 2, Section 3.7
1.8c	Sept 4, 2015	Chapters 2 and 3 swapped	A. Jutman	Chapters 2 and 3
1.9	Sept 9, 2015	Document review and minor updates in all parts of the document	A. Jutman, E. Larsson	All sections

Author, Beneficiary

Artur Jutman, Testonica Lab
Christophe Lotz, ASTER Technologies
Piet Engelke, Infineon
Jaan Raik, TU Tallinn
Erik Larsson, University of Lund
Matteo Sonza-Reorda, Politechnico di Torino
Rene Krenz-Baath, HSHL

Executive Summary

This document presents the Demonstration Plan that embraces all RTD activities of BASTION, i.e. work packages WP1, WP2, WP3, WP4. First, the common demonstration platform is described, which is based around a complex board that will represent the test case (system under test) used throughout the whole project for demonstration purposes. Then, the demonstration experiments to be performed are described, thus giving inputs for the development of prototype tools implementing important BASTION techniques. Based on experimentation targets, a set of specifications required by the partners to guarantee an easy usage of their tools in an integrated manner is also presented.

List of Abbreviations

AOI - Automated Optical Inspection
ASIC - Application-Specific Integrated Circuit
AXI - Automated X-ray Inspection
BERT - Bit Error Rate Testing
BBIST - Board BIST
BIST - Built-In Self-Test
BOM - Bill of Material
BSDL - Boundary-Scan Description Language
BST - Boundary-Scan Test
CAD - Computer Aided Design (also EDA)
CMOS - Complementary Metal-Oxide Semiconductor
CPU - Central Processing Unit, also Processor
DDR - Double Data Rate
DPM - Defects Per Million
DPMO - Defects Per Million Opportunities
DRAM - Dynamic RAM
DRC - Design Rule Check
EDA - Electronic Design Automation (also CAD)
EMS - Enhanced Manufacturing Services
FIFO - First In, First Out (data buffer)
FMC - FPGA Mezzanine Connectors
FPGA - Field Programmable Gate Array
FP7 - European Union's 7th Framework Program
FPT - Flying Probe Test
FPY - First Pass Yield
FT - Functional Test
HDMI - High-Definition Multimedia Interface

HW	- Hardware
IBIS	- Input Output Buffer Information Specification
IC	- Integrated Circuit
ICL	- Instrument Connectivity Language
ICT	- In-Circuit Test
IIC	- Inter-Integrated Circuit, also I^2C
IJTAG	- Internal JTAG, a short name for IEEE 1687 standard and infrastructure collectively
IP	- Intellectual Property (hardware module in FPGA or SoC)
IST	- Information Society Technologies
JTAG	- Joint Test Action Group; also Boundary Scan; often used as a short name of the IEEE 1149.1 standard and respective infrastructure including test access port and header on the board;
MPS	- (Coverage metrics based on) Material, Placement & Solder
NBTI	- Negative Bias Temperature Instability
NFF	- No Fault Found or No Failure Found (also NTF)
NoC	- Network-on-Chip
NTF	- No Trouble Found (also NFF)
OTG	- USB On-The-Go
PCOLA/SOQ	- (Coverage metrics based on) Presence, Correct, Orientation, Live, Alignment/Short, Open & Quality
PCBA	- Printed Circuit Board Assembly
PCI	- Peripheral Component Interconnect
PCIe	- PCI Express
PDL	- Procedural Description Language
PMOS	- p-type Metal Oxide Semiconductor
POST	- Power-On Self-Test
PPVS	- (Coverage metrics based on) Presence, Polarity, Value & Solder
PVT	- Process, Voltage, Temperature
RAM	- Random-Access Memory
RTD	- Research and Technological Development
SBST	- Software-Based Self-Test
SIB	- Segment Insertion Bit
SMA	- SubMiniature version A (connector)
SoC	- System on Chip
SODIM	- Small Outline Dual In-Line Memory
SFP+	- Enhanced Small Form-Factor Pluggable (transceiver)
SVF	- Serial Vector Format
SW	- Software
TDR	- Test Data Register

UART	- Universal Asynchronous Receiver/Transmitter
USB	- Universal Serial Bus
UUT	- Unit Under Test
VHDL	- VHSIC Hardware Description Language
VHSIC	- Very High Speed Integrated Circuit

Table of Contents

1 Introduction

1.1 Purpose of the Demonstration Activities

The overall goal of WP6 is to evaluate and demonstrate key achievements made by BASTION partners throughout the project. More specifically, the WP aims at:

- Identify a test case to be used throughout the whole project, combining the activities at core, IC and PCBA level and thus demonstrate the achievements that can be reached by the partners, as well as the experiments to be done on it and the output results to be gathered;
- Collect and report all the output data gathered by different partners in the final experiments performed within the WPs according to the plan in the previous item;
- Develop a plan for allowing the combined usage of tools developed within the project, so that they can be used in an integrated manner (See Chapter 3 of this deliverable);
- Put together a set of demonstrations with corresponding data that can be exploited by WP5 in order to better disseminate the results and achievements produced by the project.

This report (D6.1) describes foreseen demonstration experiments to be performed, thus giving inputs for the development of corresponding prototype tools implementing the main novel techniques of WP1, WP2, WP3, and WP4.

1.2 Structure of the document

This document presents the Demonstration Plan that embraces all RTD activities of BASTION, i.e. work packages WP1, WP2, WP3 and WP4. This document is organized as follows.

Individual demonstration experiments to be performed are described in Chapter 2. These experiments are giving inputs for the development of prototype tools and implementing major BASTION techniques. Also presented is a set of specifications based on experimentation targets, required by the partners to guarantee an easy integration and usage of their tools. The common demonstration platform is described in Chapter 3. The demonstration platform can be seen as the test case itself (the system under test) used for demonstration purposes throughout the whole project. The selection of demonstration platform and its architecture is based on the requirements and needs of individual demonstration setups given in Chapter 2. Chapter 4 concludes the report.

2 Individual demonstration plans and setups

This section lists individual experiments, which are foreseen as of now. In the course of the project, we might add a few more demonstration scenarios to the list. The individual experimental setup descriptions are supplied with the following information:

- Related WP;
- Partners;
- Background information and demonstration objective (if applicable);
- Brief, description of experiments;
- Particular minimum requirements towards the demo platform (if any);
- Setup: expected customization of demo platform or additional components (if needed);

The individual demonstration scenarios are collectively driving the choice of common demonstration platform described in Chapter 3.

2.1 Testability Metrics and Tools

Related WP: WP1
Partners: ASTER, TL
Experiments and demonstrations:
Test Coverage metrics, as defined by BASTION research program, should be demonstrated on the BASTION demonstration board. Test coverage analysis will be performed for AOI, AXI, BST, FPT and ICT.
When new test instruments are designed by the project partners, ASTER will define a universal test coverage format that helps to formerly describe the test coverage. TestWay Express will be able to import such reports and visualize the test coverage on components and pins (traffic light color coding: green=well tested, orange=partially tested, red=not tested). Example: coverage of timing-related faults between the processor on the demo board and DDR3.
All analyzing/reporting features of QuadDPMO will be able to run on the "shadow" traceability & repair data, CAD data and test coverage data as analyzed by TestWay Express. The demonstrator will become an excellent "sales" tool, to demonstrate the concept to new customers, without compromising the Non Disclosure Agreement, signed with the BASTION industrial partners.
The experimental data set will be the result of the following workflow:

- collect the CAD data (netlist and BOM) of the demonstration board;
- process the CAD data as a TestWay Express project:
    - Board viewer managing layout, schematic and virtual schematic views;
    - Component modelization: BSDL, IBIS, test models;
    - Probe placement;
    - Default DPMO figures;
- From the QuadDPMO database, built from data collected from the industrial partners, ASTER identified a board with similar complexity and will create a shadow database, linked with demo board data. This database will be used as realistic example.

Requirements for the demonstration platform:

- JTAG port to JTAG device;

- Parallel accesses for external JTAG resources;
- DRAM clusters;

2.2 Concurrent Fault Monitors

Related WP: WP2
Partners: TUT, TL
Experiments and demonstrations:

TUT has developed a new tool framework [3] for automating design of fault monitors. The framework allows formal qualification of fault monitors as well as automated minimization of the respective area overhead. As a case study, the framework, together with the underlying methodology, will be demonstrated on a fault tolerant router design. A 5-port 2D Network on Chip (NoC) router will be implemented consisting of a datapath and a control part. The datapath will be composed of input buffers (implemented as FIFOs), one for each input port, a crossbar switch and an output buffer for each output port. The control part will contain routing units, arbiters and FIFO control.

Using the monitor design framework, a set of monitors for the router will be synthesized with a goal to achieve high-fault-coverage, low-area, low-latency fault monitors. The Concurrent Fault Monitor demonstration will be linked to the IEEE 1687 based fault management fault management demonstrator by including, error reporting on top of the fault detection to be demonstrated by fault injection.

Requirements for the demonstration platform:

- FPGA area for the ~30 kgate (logic NAND equivalents) router design, which includes the fault monitors and fault injection framework.

2.3 Experiments and measurements on silicon

Related WP: WP3
Partners: IFAG, UT, TL
Background:
Monitors that detect faults caused by CMOS-ageing can be embedded deeply within an IC. The information collected by such monitors can be exploited for in-field testing. This, however, may require enhanced controllability, and observability of chip-embedded instruments. Using a suitable combination of the IEEE 1149.1 and 1687 standards, deeply embedded ageing monitors can be made accessible from the outside of the IC.
An ageing monitor, which is embedded on a test-chip in 40 nm technology, was developed by Infineon and the TU München as part of the project RELY [6] from the CATRENE-program. The monitor proposed in [7] employs in-situ timing measurement to evaluate the effect of stress conditions and to track device aging. This test-chip offers a unique opportunity to demonstrate how a chip-embedded ageing monitor can be made easily controllable from the common demonstration platform via an IJTAG network.
Experiments and demonstrations:
The focus of this evaluation is on the integration of a chip-embedded instrument, and on the required infrastructure. Integrating a test-chip in the platform is a challenging task which involves the risk that the test-chip's functionality will be limited.
Objective:

- Get access to a measurement instrument for device aging which is implemented on a test chip in silicon (40 nm technology).

- Integrate this test chip into the common demonstration platform.
- Demonstrate that the measurement instrument can be connected to an IJTAG network, and that it can be controlled via that network.
- The data produced by the measurement instrument can be processed further, e.g. by higher system-levels of the demonstrator.

Requirements for the demonstration platform:

- Interface with the test chip according to its mechanical and electrical specifications (e.g. provide nominal/stressed V_{DD}, and V_{SS})
- Provide a connection between the FPGA and the I/O pins of the test chip.
- Drive the connection between the FPGA and the RELY test chip.
- Implement a state-machine operating the measurement instrument on the test chip.
- Implement registers to control that state-machine (start measurement, read measured values, etc.).
- Connect these control registers to the IJTAG network.

2.4 Verify test time calculation on a real IEEE 1687 network

Related WP: WP2
Partners: HSHL, ULUND
Objective: Verify test time calculation from our methods on a real IEEE 1687 network
Background: HSHL and ULUND are jointly developing EDA methods to optimize access time for IEEE 1687 networks. The demonstrator will be used to demonstrate that the developed methods work on a real design.
Requirements for the demonstration platform:

- An FPGA with an IEEE 1687 network. The IEEE 1687 network is created with EDA tools such as the ones from Testonica or Mentor Graphics.

2.5 Test IEEE 1687 network for HW defects

Related WP: WP3
Partners: PDT, ULUND
Objective: Check an IEEE 1687 network for eventual HW defects in the network itself.
Background: Defects may affect the IEEE 1687 network itself. PDT and ULUND are jointly developing EDA tools for testing and diagnosing IEEE 1687 networks. The methods in the developed tools are to be validated.
Requirements for the demonstration platform:

- An FPGA with an IEEE 1687 network with capability to inject faults. The IEEE 1687 network is created with EDA tools such as the ones from Testonica or Mentor Graphics.
- A dedicated TDR, which is not included in the IEEE 1687 network itself can be used to inject permanent faults. The faults that are to be injected are: stuck at, slow-to-raise, slow-to-fall, fast-to-raise, fast-to-fall. Most important is the capability to insert stuck-at faults. The defects should impact flip-flops in the TDRs, the ScanMuxes and the SIBs.

2.6 Validation of IEEE 1687 infrastructure

Related WP: WP2
Partners: TL, TUT, HSHL

Background: Complex reconfigurable scan architectures capable for the accommodation of hundreds of instruments normally include multiple levels of multiplexing logic that results in a large variety of different possible network configurations. Normally, an EDA tool is used for the final integration of the IJTAG network and generating the corresponding ICL file. Since IJTAG is expected to be used beyond IC test: for board test and in the field, silicon vendors seek an opportunity to make sure that third-party tools will support the particular IJTAG implementation in the chip and that the ICL file really corresponds to the silicon. The source of problem could be a human factor, e.g. manual correction of the IJTAG network or ICL/silicon version mismatch. History shows numerous problematic examples from a similar earlier standard IEEE 1149.1 where BSDL files were either not matching the silicon or the silicon was violating the standard. Industry needs to avoid this sort of problem today and looks for an effective solution.
Experiments and demonstrations:
We plan to demonstrate various validation scenarios including standard compliance, design rule check (DRC), and mismatch between ICL and the silicon. The main emphasis will be made on the latter aspect, as this is the main focus in BASTION (T2.4). FPGA will mimic the silicon. We will implement the instrumentation network with fault injection capability, whereas faults will be mainly design errors.
Requirements for the demonstration platform:

- Fault injection in scan chains is needed;
- Flexibility of reconfiguration (FPGA);
- JTAG port;
- IJTAG control tools such as the one from TL;
- Mid-size FPGA.

2.7 IEEE 1687 based fault management

Related WP: WP3
Partners: TL
Objective: Demonstrate the key features of the IJTAG based fault management infrastructure; localize failing resources/modules (injected faults).
Experiments and demonstrations: a many-core demonstration system under test will be implemented on FPGA (could be based on the NoC router design with monitors from section 2.2) including resource-specific embedded instruments. A fault-management infrastructure will be added to the system that includes a dedicated IEEE 1687 network with emergency signaling, instrument manager and health map. Faults will be injected and the complete fault management system will be demonstrated in action (including fault detection, localization, and classification).
Requirements for the demonstration platform:

- Fault injection in resources;
- JTAG port;
- IJTAG control tools such as the one from TL;
- Large FPGA is needed;

2.8 Aging Mitigation Techniques

Related WP: WP4
Partners: TUT
Experiments and demonstrations:

In BASTION, we propose a novel NBTI mitigation approach by rejuvenation of nanoscale logic at NBTI-critical paths with dedicated stimuli sequences. The method

is based on fast hierarchical NBTI-critical paths identification at the gate-level and rejuvenation stimuli generation using an Evolutionary Algorithm. The rejuvenation stimuli is targeted to be applied as execution overhead at pre-calculated periods of time to drive to the recovery phase the pMOS transistors that are the most significant for the NBTI-induced path delay. The proposed approach aims at extending the reliable lifetime of nanoelectronics.

Evolutionary Computation has been used by the Computer Aided Design community for years, also involving it for the tasks of automatic test-pattern generation. In BASTION, we exploit a general-purpose evolutionary toolkit called µGP [4] and find a suitable fitness function using an open source hardware analysis framework zamiaCAD [5]. The advantage of such flow is its ability and flexibility in solving the dependencies of impacts by individual gates to the most critical NBTI-induced path delay using the evolutionary optimization process.

Requirements for the demonstration platform:

- a software tool demonstrator running on a PC with Java virtual machine.

2.9 Instrument-assisted in-field functional test of uProcessors and Board BIST

Related WP: WP4
Partners: PDT, TL
Experiments and demonstrations:
A combined demonstrator of WP4 methods for in-field *Power-On Self-Test* (POST) including the *Board BIST* (BBIST) framework and related *Software-Based Self-Test* (SBST) methodology will be developed.
The BBIST instrument IP is a special FPGA design intended to test on-board components and interconnections during the board boot-up process, i.e., to carry out *Power-On Self-Test* (POST) test procedures on PCBA. BBIST will provide a framework to host and manage test techniques like Boundary Scan, Embedded Instrumentation, and SBST. Important part of the demonstrator will be devoted to instrument-assisted SBST of microprocessors. BBIST will handle the following aspects of SBST as storing the test program test program, how to trigger the processor to execute it, how to retrieve and check the produced results.

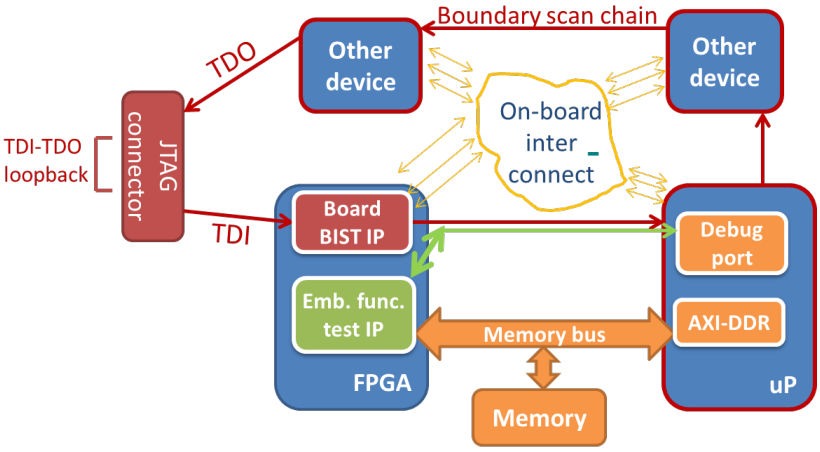

Figure 1: Combining Board BIST and SBST in a single demonstration setup

Example of demonstration flow could be:

- The FPGA is programmed to implement a suitable instrument;
- The Trace facility is programmed and activated (through the Debug Access Port);
- The Test Program is launched;
- The Trace buffer is downloaded (through the Debug Access Port or the Trace Port Interface Unit) and checked;
- An error signal is possibly triggered if a mismatch is found.

Requirements for the demonstration platform:

- Mid-size FPGA and a microprocessor core with debug trace port.
- Demo board needs a JTAG port.
- FPGA and CPU core need to be connected.
- CPU can be either a hard macro IP (like e.g. Xilinx ZYNQ SoC) of a softcore IP.

3 The Common Demonstration Platform

The main target of the demonstration work package is twofold: to demonstrate key achievements and to allow combined usage of tools and complementary techniques. Therefore a due effort has been spent by the BASTION consortium on defining a common vision towards the demonstration platform and studying technical feasibility of this target. Finally, based on individual experimental scenarios and requirements collected from partners, it has become clear that the majority of techniques could be integrated around an FPGA development platform. Of course, none of the available FPGA boards comes with a ready-made necessary ecosystem, but in combination with tools of BASTION industrial partners, primarily ASTER and TL, an FPGA development platform can become the cornerstone of the BASTION demonstration strategy.

A typical FPGA development board represents an example of high-end electronics, featuring both passive and active components, some analog part and quite complex digital part including modern IC packages being mounted on a many-layer PCB. Hence it is a good example of challenging object under test both in terms of test coverage metrics and the quality of test (WP1).

Since FPGA has a programmable interface between the standard JTAG port and the internal reconfigurable logic, the FPGA itself is a very good platform for IEEE 1687 infrastructure implementation and related experiments. This represents a real-life object for IJTAG control tools and respective controller providing interface between the runtime and the hardware. The experimental software will be running on the industrial IJTAG runtime adapted for BASTION needs, while the IJTAG networks can be easily reprogrammed implementing different scenarios (e.g. for various optimizations) as well as fault injection fulfilling the needs of WP2.

The challenge of physical defect injection and integration with ASICs is more difficult because it is based on intrusive methods. Still, the latter is accomplishable using interface (plug-in) cards (e.g. the one with RELY chip to be provided by IFAG). That would allow various demonstration scenarios including fault management (WP3).

An FPGA itself is a good flexible platform to host embedded instruments, both for inward and outward testing (WP4). The former is used in BASTION in connection with functional test of processors, while the latter is an example of high-performance test instrumentation for advanced board test (targeting new fault classes).

In the following, we describe the general structure of the common demonstrator and give an example of an available FPGA development board that was identified to be suitable for BASTION demonstration purposes. Still some tools (e.g. for ageing effect mitigation) have no benefit from the FPGA platform and shall be demonstrated separately.

3.1 Overall Structure of the Common Demo Platform

Figure 2 shows the overall composition of the common demonstration platform and its main components detailed in the following sub-sections of Section 3.1. The platform will be put together from the following main components, whereas each one has its important role in individual demonstration scenarios:

- Off-the-shelf FPGA demonstration/development kit (to be purchased);
- Plug-in card (to be developed) with RELY chip provided by IFAG;
- Testability and coverage assessment tools provided by ASTER;
- JTAG bus controller HW and basic SW tools will be provided by TL (industrial JTAG system);
- IJTAG support tools developed by TL and adapted for BASTION purposes;
- CPU core either as a hard macro (part of FPGA SoC) or as a softcore to be placed inside FPGA;
- Individual experiment-specific tools developed by partners;
- Individual experiment-specific FPGA images prepared by partners;
- Set of configuration and script files (PDL, ICL, SVF, etc.) prepared by partners;
- Board/system netlist and other CAD data.

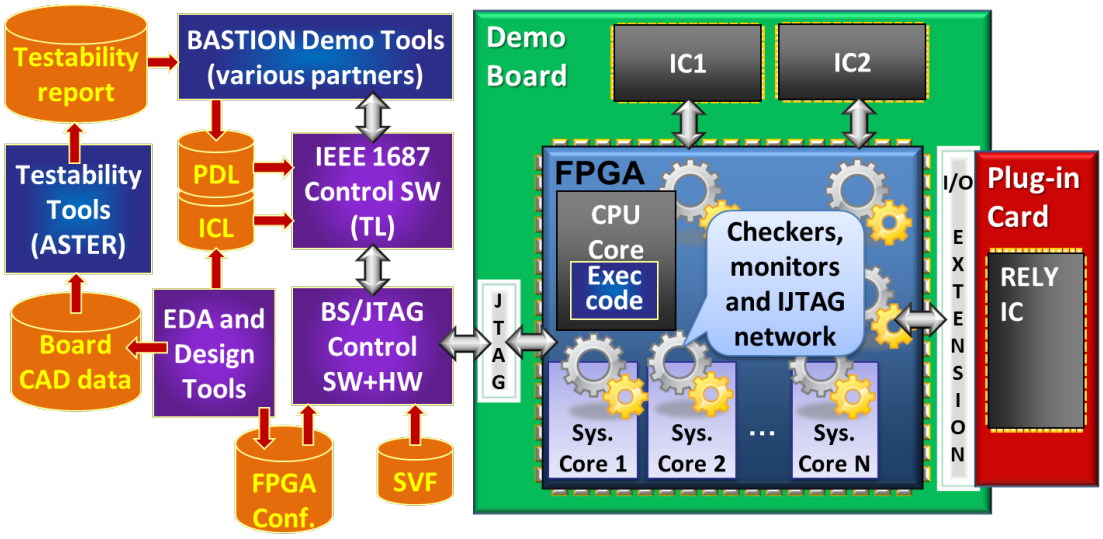

Figure 2: Common Demonstration Platform

3.1.1 FPGA device

The FPGA device will become the cornerstone of the demonstration ecosystem playing the role of SoC/ASIC, yet providing a flexible reconfigurable hardware for various experimental configurations and fault injection. The FPGA will

- host a multi-core system with embedded instrumentation and fault monitors for implementing fault-management and on-line test scenarios;
- contain a re-configurable IJTAG network for several experiments including fault injection, validation, optimization of the IJTAG itself as well as for fault management;

- be used in connection with microprocessor for instrument-assisted functional test scenarios;
- contain high-performance instruments for advanced board test (new fault models) as well as for implementing board BIST/POST scenarios;

3.1.2 On-board components

An advanced FPGA demonstration board features high-performance electronics, like gigabit links (e.g. PCIe), DDR memories, bus controllers, etc. These devices will represent a challenging system under test both for new testability metrics and tools as well as for advanced test instrumentation. Defect injection can be also done right on the board itself by destroying the integrity of selected structural elements of the system.

3.1.3 Plug-in cards

We plan to develop a plug-in card for the IFAG-s experimental IC. The IC could then be attached to the main board and connected to FPGA ports. FPGA will be used to control the IC and perform different experiments.

3.1.4 Test runtime software

Dedicated software that communicates with the FPGA via the JTAG port will be provided by TL and extended to support IEEE 1687 protocol/procedures and respective formats (ICL and PDL). This runtime will enable (e.g. by using respective PDLs) experiments with fault injection and diagnosis in IJTAG infrastructure as well as its validation. All other scenarios involving FPGA will be also run using this SW.

3.1.5 JTAG interface

The JTAG interface is the major access bus foreseen for IEEE 1687. TL will provide necessary hardware and a software platform that supports the JTAG protocol. The JTAG interface will be used as a basis for the Test runtime.

3.1.6 FPGA configurations

Separate FPGA configurations (bit-streams/images) will, in general, be necessary in distinctive demonstration set ups. FPGA configurations will be prepared in advanced and stored in a form of image files at the demo platform. TL's JTAG software will be used to download these images to the FPGA before each demo experiment.

Different FPGA configurations could be used even in a single demonstration scenario, for instance, to implement various architectures of IEEE 1687 IJTAG infrastructure or IP cores in SoC for proof-of-concept or optimization purposes.

3.1.7 Experiment-specific tools

Most of experiments involving the FPGA are expected to be run either based on PDL scripts (in case of IJTAG), or SVF, or based directly on the Test runtime (e.g. for board BIST/POST scenarios and high-performance instruments for advanced board test). Each case will be considered separately and a suitable solution developed.

The final integration of the common demonstration platform will be led by TL, because it possesses a large part of the basic SW and HW tools needed to run the system.

In addition, ASTER will give full access rights to the TestWay Express demo packages, as well as data sets relating to the BASTION demo project, to all partners. The BASTION demo project is used for viewing, analyzing and reporting BASTION results on layout, schematics and virtual schematics data.

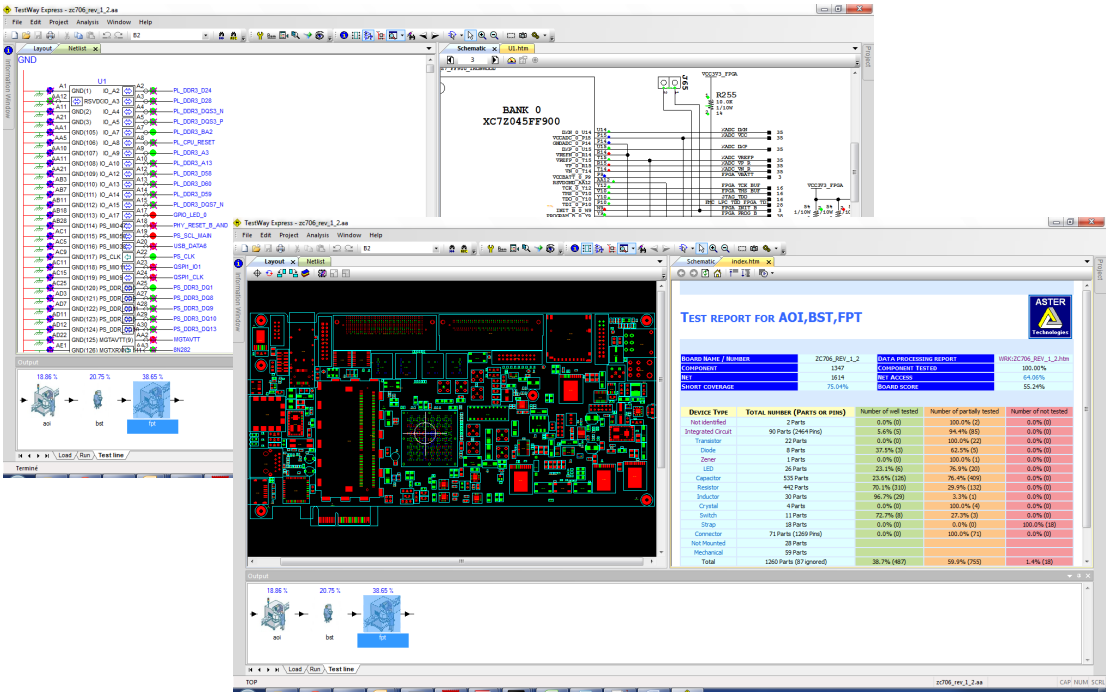

Figure 3*:* Screenshots of TestWay Express

3.2 Off-the-shelf HW fulfilling the requirements

The requirements of the demonstration hardware, listed in Section 2, allow us to identify, under individual experiments, several available boards to be used as the basis of the common demonstration platform.

Here is an example of such a board: Xilinx Zynq-7000 All Programmable SoC ZC706 Evaluation Kit [8]. The extract from the information leaflet reads: “The ZC706 Evaluation Kit includes all the basic components of hardware, design tools, IP, and pre-verified reference designs, including a targeted design. This enables a complete embedded processing platform and transceiver based designs including PCIe. The included reference designs and industry-standard FPGA Mezzanine Connectors (FMC), allow scaling and customization with daughter cards.”

The board represents an example of a modern complex high-performance system, suitable e.g. for such applications as high-definition video streaming for HDMI-based display applications and for development of networking applications with 10-100-1000 Mbps Ethernet (RGMII).

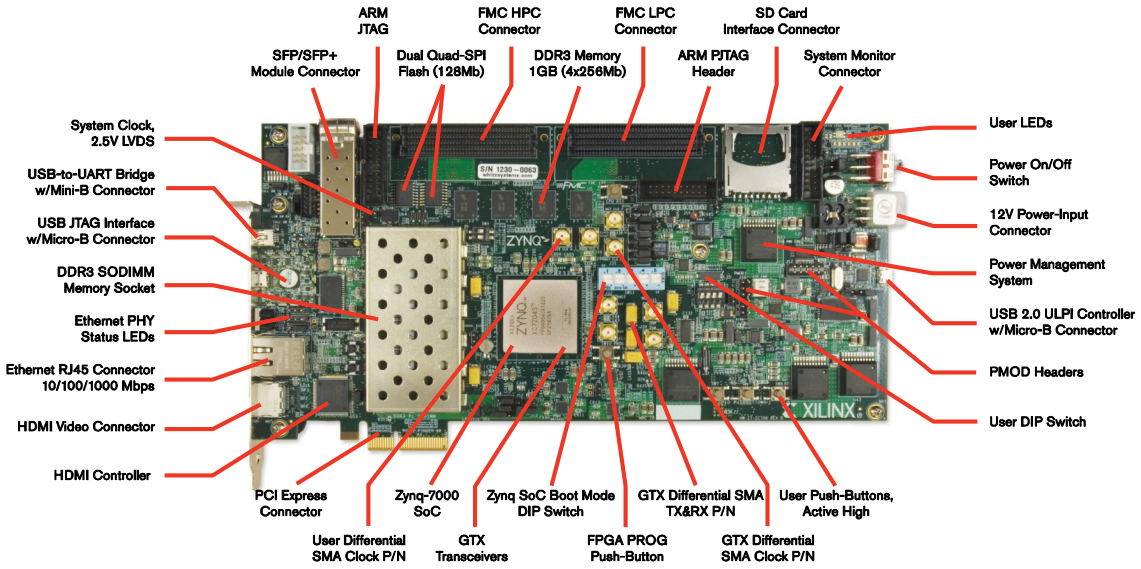

Figure 4*:* Xilinx Zynq-7000 All Programmable SoC ZC706 Evaluation Kit

3.2.1 Key Features & Benefits of ZC706 Board

- Optimized for quickly prototyping embedded applications using **Zynq-7000 SoCs including FPGA and ARM Cortex A9 processor**
- Hardware, design tools, IP, and pre-verified reference designs
- Demonstrates an embedded design, targeting video pipeline
- Advanced memory interface with:
- 1GB DDR3 Component Memory **(DRAM cluster)**
- 1GB DDR3 SODIM Memory **(DRAM cluster)**
- Enabling serial connectivity with PCIe Gen2x4, SFP+ and SMA Pairs, USB OTG, UART, IIC
- Supports embedded processing with Dual ARM Cortex-A9 core processors
- **Expand I/O with the FPGA Mezzanine Card (FMC) interface**
- **JTAG port and respective connector**

4 Summary

BASTION will offer new tools and technologies to the electronics industry, including improved test coverage and DPMO estimation tools, at-speed test instrumentation and IEEE 1687 solutions for fault management, hierarchical and in-system test as well as high-performance board-level test. This document presented a plan towards demonstration of the key results and technologies expected to be produced by the BASTION consortium. We described both the list of planned demonstration experiments and the description of the common demonstration platform to be used across the BASTION project.

5 References

[1] *Big Trouble with "No Trouble Found" Returns,* Accenture Report, 2008, Available at: http://www.accenture.com/SiteCollectionDocuments/PDF/Accenture_Returns_Repairs.pdf

[2] *Embedded Instrumentation: Its Importance and Adoption in the Test & Measurement Marketplace: A Frost & Sullivan White Paper*, Frost & Sullivan, 2009. Available at: www.frost.com/prod/servlet/cio/201638885

[3] Pietro Saltarelli, Behrad Niazmand, Ranganathan Hariharan, Jaan Raik, Gert Jervan, Thomas Hollstein. Automated Minimization of Concurrent Online Checkers for Networks-on-Chip, *Proceedings of the 10th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC 2015)*, Bremen, 2015.

[4] E. Sanchez; M. Schillaci; G. Squillero, *Evolutionary Optimization: the µGP toolkit*, Springer, ISBN: 978-0-387-09426-7, 2011

[5] zamiaCAD framework web page, [http://zamiaCAD.sf.net]

[6] RELY - Design for RELIABILITY of SoCs for Applications like Transportation, Medical, and Industrial Automation, http://www.rely-project.eu/

[7] N. Pour Aryan, G. Georgakos, D. Schmitt-Landsiedel, "Reliability Monitoring of Digital Circuits by in situ Timing Measurement " in 23rd International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2013.

[8] Xilinx Zynq-7000 All Programmable SoC ZC706 Evaluation Kit [http://www.xilinx.com/products/boards-and-kits/ek-z7-zc706-g.html]