SEVENTH FRAMEWORK PROGRAMME
THEME [ICT-1-3.1]
Next-Generation Nanoelectronics Components and Electronics Integration

Deliverable Report

Work Package 2 – IC buffers' innovative modelling approach

Deliverable D2.2- Report collecting the results on the validation of the new parametric models. Two test-cases models extracted by simulation.

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WP2 leader:	Igor Stievano
WP2 leader organization:	Politecnico di Torino
Project coordinator:	Antonio Girardi
Project coordinator organization:	Numonyx Italy Srl

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Content

1. Introduction

This document summarizes the activity carried out within the Task 2.2 "Model validation on identified test-case:" of WP2:

General description of the task*: The feasibility of the proposed modified modeling technique is applied to the characterization of the same test devices used in WP1. The accuracy of models generated from the simulation of the detailed-transistor-level descriptions of devices is assessed.*

The partners that are mainly involved in this part of the activity are NUMONYX, POLITO and IT. Once the most suitable model structure for the digital buffers have been derived and implemented in different commercial EDA tools in the first part of the activity (see the Task 2.1 and the related Milestones M2.1, M2.2 and deliverable D2.1), **the accuracy and the efficiency of the proposed enhanced model have been assessed.**

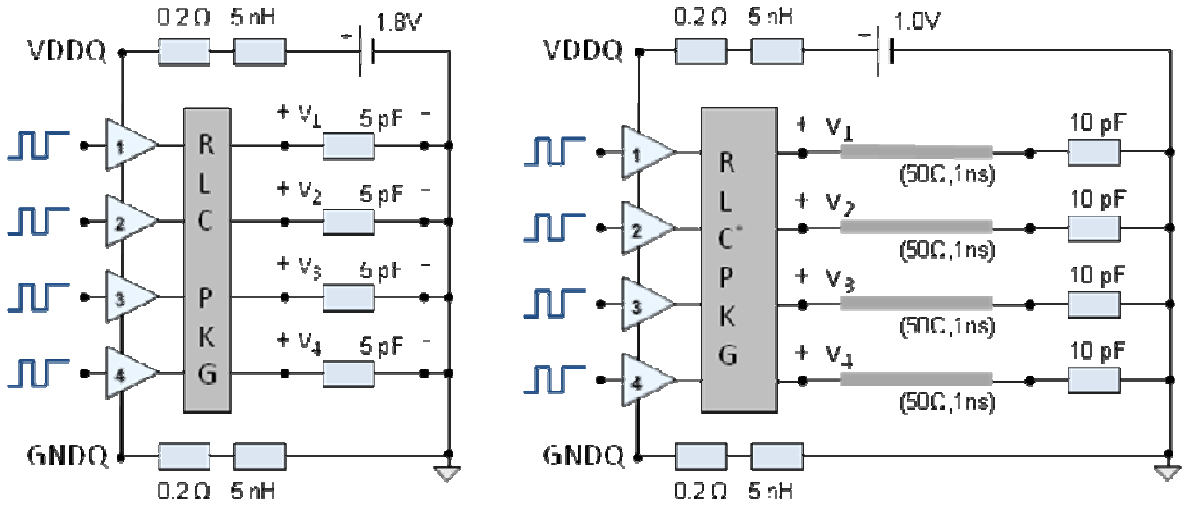
2. Validation strategy

In order to validate the enhanced buffer models developed in the first part of the activity of WP2 (see Task 2.1), a large and systematic set of simulation tests have been carried out to assess both the accuracy and the efficiency of the buffer models. The models have been estimated from the detailed transistor-level descriptions of two example devices. The two devices considered in the study and defined by Numonyx are a 512Mb NOR Flash memory in 90nm technology and a DDR external third parties device, in 70nm technology. Hereafter, the two test devices are labeled as "first test case" and "second test case", respectively. An extra test case (the so called "third test case") has been also included in the study. The latter test case is a new test chip designed by Numonyx in 90nm technology, with a Low Power DDR interface for I/O buffers and a clock frequency of 166MHz. It is worth noting that the latter test case has been considered as an additional chip that were not required in the original MOCHA work plan. It has been included to stress the proposed methodology as well as to possibly contribute to the inclusion of a larger number of devices of interest. The additional efforts that are going to be spent for this alternate example will allow the reseachers involved in this activity to tune the proposed model structures and modeling methodology.

All the simulation tests carried out in the validation phase are based on the realistic structures shown in Fig. 1, where several drivers supplied by a common power and ground structure switch on either lumped or distributed loads. The two structures of Fig. 1 are representative for the case of short (a) or long (b) interconnecting paths. All the devices are connected to the same lumped equivalent of the power supply net (here represented by a simple RL equivalent, where the value of the inductance has been tuned to allow for the large fluctuation of the supply voltage values and thus to stress the different models considered in the comparison). Additional tests based on the simplification of the structures of Fig. 1 or their modification, e.g., the structures obtained by increasing the number of devices, were also considered. The results however, are not shown in this report since the same results on both accuracy and efficiency were found. In the different tests, the simultaneous switching of the devices that produce the same "010101…" bit sequence is considered since it has been verified that this was the most representative test stressing the model accuracy. On the second and third test cases (i.e. the DDR devices) a longer pseudo random binary sequence has been considered to allow the computation of the eye diagrams.

In this study, three models are considered: the detailed transistor-level description of the devices; the standard IBIS models [1,2] and the proposed enhanced Mpilog models (all the details on the model

structure, and on the parameters estimation are collected in the deliverable report D2.1). The waveforms obtained from the simulation of the two structures of Fig. 1 and the transistor-level models of devices are assumed as the reference waveforms hereafter. The accuracy of the IBIS and Mpilog models has been assessed by comparing the functional responses of the port voltage of the different drivers (e.g. the voltage v_1) and the power supply fluctuations of the nodes VDDQ and GNDQ. On the other hand, the efficiency has been quantified by computing the CPU time of the transient simulation of the test cases of Fig. 1. All the simulations have been carried out by means of the ELDO tool, i,e,, the SPICE-based simulation tool of Mentor Graphics.



(a) (b)

Fig. 1. Realistic test cases considered for the validation of the proposed enhanced models of the I/O ports. The values of elements composing the lumped RLC equivalents of the package structures are: R=200mΩ, L=10nH, C=0.5pF.

3. Results for the first test case

This Section summarizes the results on the accuracy and the efficiency of the proposed enhanced models of the first test case considered in the study.

Figures 2 and 3 collect a selection of the port voltage responses obtained by simulating the test cases of Fig. 1. From the previous Figures (and in particular form Fig. 2), it is worth noting that the proposed Mpilog models provide improved accuracy for both the functional signals like the output port voltage v_1 and the power supply fluctuations. The same comparison highlights that the IBIS models overestimate the under/over-shoots observed in the reference responses of the device and introduce large timing errors of the port voltage (e.g., see v_1) computed during the state transition events. Furthermore, the IBIS prediction of the supply voltage fluctuations like the V(VDDQ) of Fig. 3 incorporate spurious and faster dynamics. On the other hand, some minor changes of the Mpilog model structure are going to be considered to further improve the quality of the prediction of the curves of Fig. 2. As an example, the effects of small changes of the model structure will be considered to possibly improve the prediction of the damped oscillations of the functional voltage responses. This will be carried out by the separate characterization of the power and ground pins.

Table I collects the information on the CPU time required to simulate the test structure of Fig. 1 (a) for the generation of the curves of Fig. 2 via ELDO simulation and the different models involved in the comparison. From the data of Table I, it is clear that either the IBIS and the Mpilog models

provide a large improvement on the speed-up of the simulation of realistic structures. Even if IBIS models are faster than the Mpilog ones, the two models can be simulated in some tens of seconds w.r.t the quite long simulation time required by the reference-transistor level models of the devices. The differences between the simulation times of IBIS and Mpilog models do not to certainly limit the application of Mpilog models for large and real simulation tests.

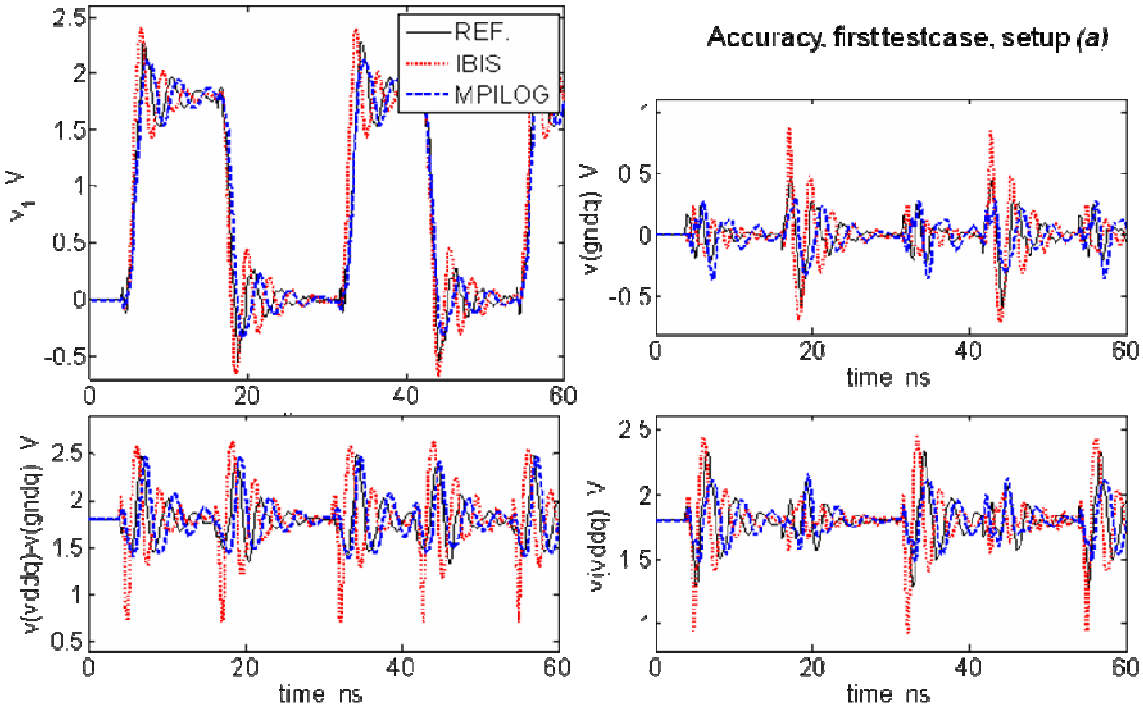


Fig. 2. Comparison between the reference responses of the example buffer of the first testcase and the predicted responses computed by means of the ELDO implementation of the IBIS and of the proposed MPILOG models for the setup *(a)* of Fig. 1 (see text for details).

In order to provide quantitative results on the accuracy of the models involved in the comparison, Table II collects the information of the timing errors introduced by the models, of the maximum errors of the fluctuations of the power and ground signals and of the standard deviation of the same error. The timing errors are computed as the maximum timing difference of the up and the down transition events of the reference transistor-level models and of the Mpilog and IBIS models (the switching events are computed at the voltage crossing of the 0.9V-threshold of the voltage v1).

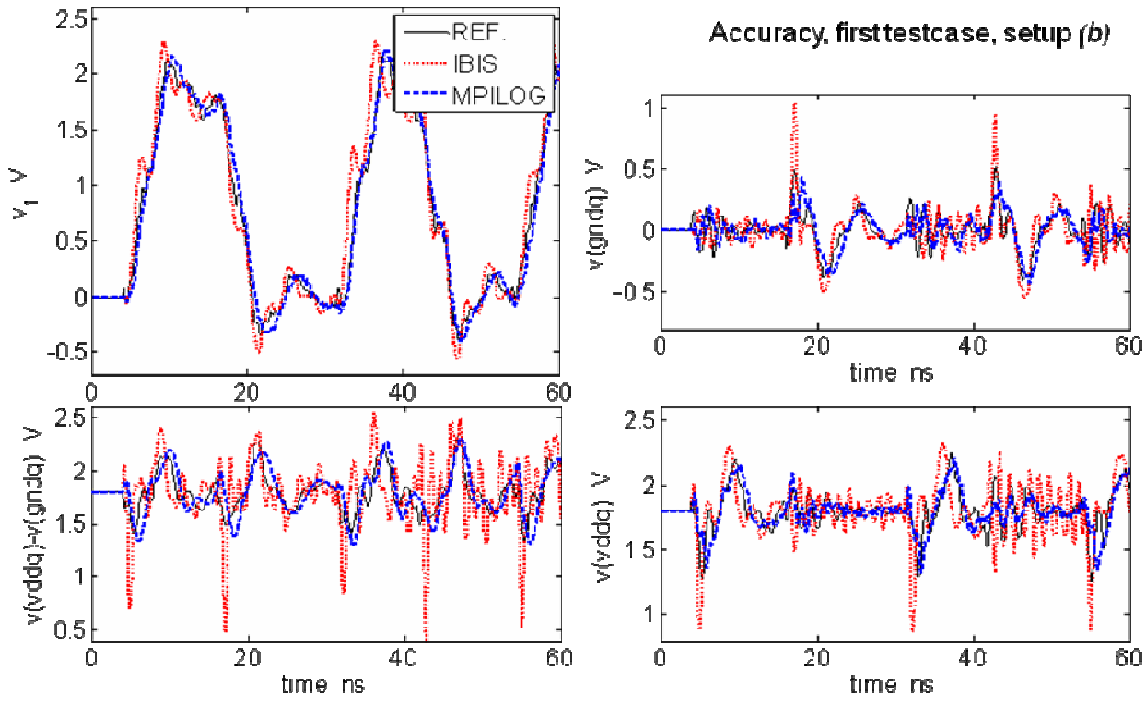


Fig. 3. Comparison between the reference responses of the example buffer of the first testcase and the predicted responses computed by means of the ELDO implementation of the IBIS and of the proposed MPILOG models for the setup *(b)* of Fig. 1 (see text for details).

Table I. Efficiency of the different models used to generate the curves of Fig. 2.

	CPU time	Speed up
Reference	773 s	
IBIS	13 s	59x
MPILOG	31 s	25x

Table II. Quantitative results based on the data processing of the responses of Fig. 2 and Fig. 3.

	Setup (a), first test case		Setup (b), first test case	
	Max timing error on $v_1(t)$ (low-to-high event)	Max timing error on $v_1(t)$ (high-to-low event)	Max timing error on $v_2(t)$ (low-to-high event)	Max timing error on $v_2(t)$ (high-to-low event)
IBIS	550 ps	180 ps	1 ns	700 ps
MPILOG	100 ps	400 ps	100 ps	750 ps
	Max relative error of vddq(ref.)-vddq(model)	Max relative error of gndq(ref.)-gndq(model)	Max relative error of vddq(ref.)-vddq(model)	Max relative error of gndq(ref.)-gndq(model)
IBIS	43 %	29 %	37 %	26 %
MPILOG	18 %	25 %	21 %	20 %
	Standard deviation of vddq(ref.)-vddq(model)	Standard deviation of gndq(ref.)-gndq(model)	Standard deviation of vddq(ref.)-vddq(model)	Standard deviation of gndq(ref.)-gndq(model)
IBIS	218 mV	165 mV	324 mV	338 mV
MPILOG	121 mV	100 mV	86 mV	86 mV

4. Results for the second test case

This Section summarizes the results on the accuracy and the efficiency of the proposed enhanced models of the alternate second test case considered in the study.

As already done for the first test, Figures 4 and 5 collect the same selection of the port voltage responses obtained by simulating the two test cases of Fig. 1. The previous figures confirm the improved accuracy of the Mpilog models for both the functional signals and for the power supply fluctuations, thus demonstrating that the model enhancements of WP2 have been completely accomplished. It is worth noting that for this second test case, the accuracy of the enhanced Mpilog models is very good and that the predicted responses reproduce the reference responses of the devices very well; the timing errors introduced by the models is negligible and the accuracy of the prediction of under/over-shoots is excellent.

For this second test case, the same efficiency (and consequently the speed-up introduced by the different models) of Table I is confirmed.

As briefly outlined in the introduction, in order to quantify the maximum errors in the predicted waveforms, the eye diagrams derived from both the output port voltage $v_1(t)$ of the setup (a) of Fig. 1 and the far end voltage response of the same driver in the setup (b) of Fig. 1 have been generated. For the eye generation, a longer bit stream defined by a 128 long pseudo random binary sequence is considered. Figure 6 and Fig. 7 show the eyes for the two simulation setups and the three models considered in the study, i.e., the reference transistor-level model, the IBIS models and the proposed enhanced model. To better quantify the accuracy of the IBIS and of the Mpilog models, Table IV collect the eye openings and errors in predicting the reference eye opening obtained by means of the transistor-level models, thus highlighting the enhancements introduced by the Mpilog models.

Finally, as already done, for the first test case, Table III collects the same quantitative results on the accuracy of the models of this alternate example.

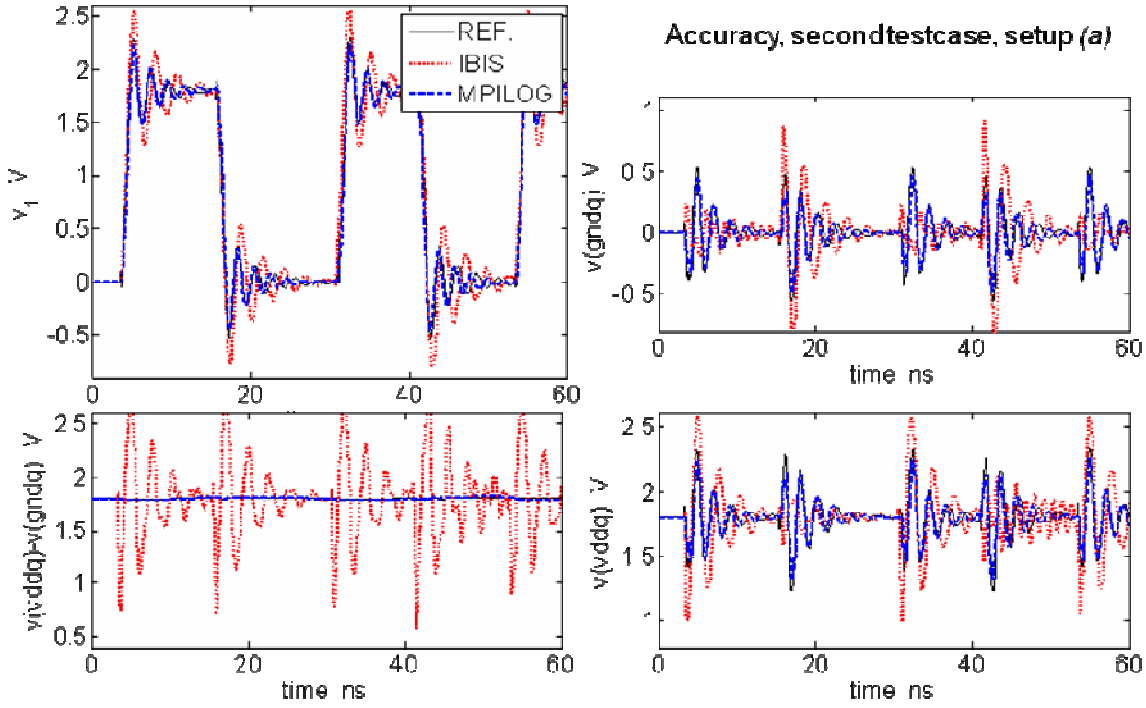


Fig. 4. Comparison between the reference responses of the example buffer of the second testcase and the predicted responses computed by means of the ELDO implementation of the IBIS and of the proposed MPILOG models for the setup *(a)* of Fig. 1 (see text for details).

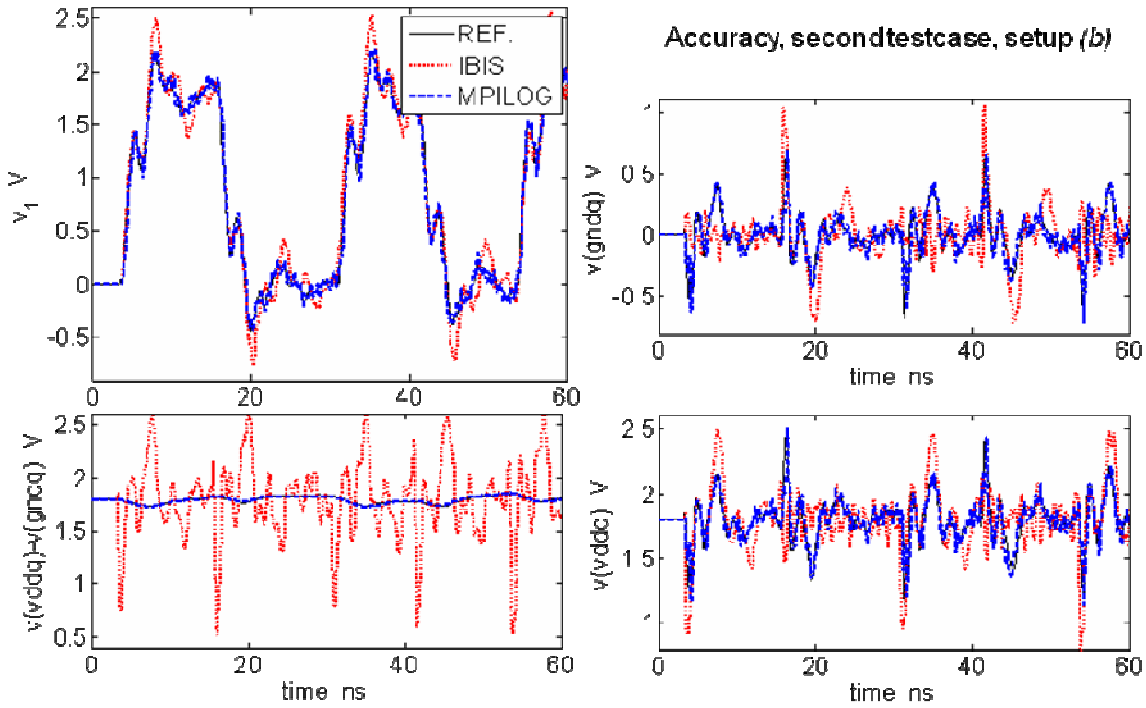


Fig. 5. Comparison between the reference responses of the example buffer of the second testcase and the predicted responses computed by means of the ELDO implementation of the IBIS and of the proposed MPILOG models for the setup *(b)* of Fig. 1 (see text for details).

Table III. Quantitative results based on the data processing of the responses of Fig. 4 and Fig. 5.

	Setup (a), second test case		Setup (b), second test case	
	Max timing error on $v_1(t)$ (low-to-high event)	Max timing error on $v_1(t)$ (high-to-low event)	Max timing error on $v_1(t)$ (low-to-high event)	Max timing error on $v_1(t)$ (high-to-low event)
IBIS	300 ps	80 ps	700 ps	200 ps
MPI_OG	60pc	100pc	600 ps	100 ps
	Max relative error of vddq(ref.)-vddq(model)	Max relative error of gndq(ref.)-gndq(model)	Max relative error of vddq(ref.)-vddq(mode.)	Max relative error of gndq(ref.)-gndq(model)
IBIS	47 %	38 %	71 %	50 %
MPI_OG	14 %	14 %	32 %	31 %
	Standard deviation of vddq(ref.)-vddq(model)	Standard deviation of gndq(ref.)-gndq(model)	Standard deviation of vddq(ref.)-vddq(mode.)	Standard deviation of gndq(ref.)-gndq(model)
IBIS	195 mV	170 mV	302 mV	250 mV
MPI_OG	99 mV	110 mV	103 mV	103 mV

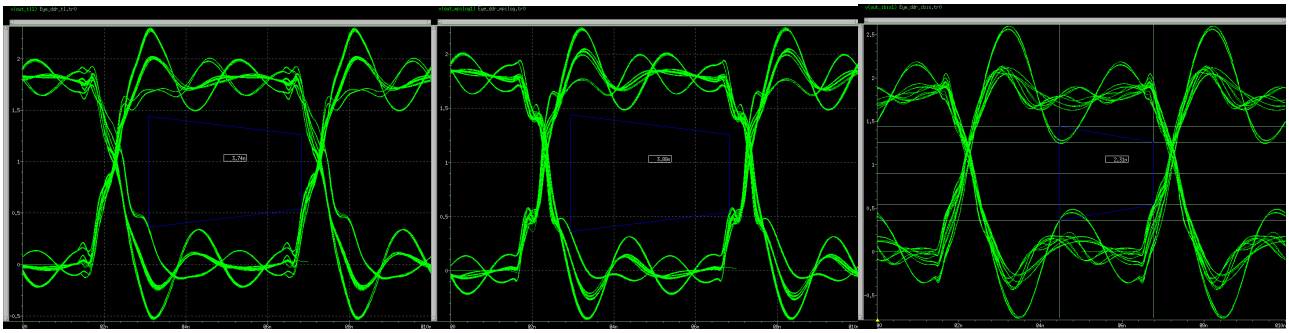


Fig. 6. Eye diagrams arising from the voltage signal v1(t) of the simulation setup (a) and for the second test case. Left: reference transistor level model; middle: Mpilog model; right: Ibis model.

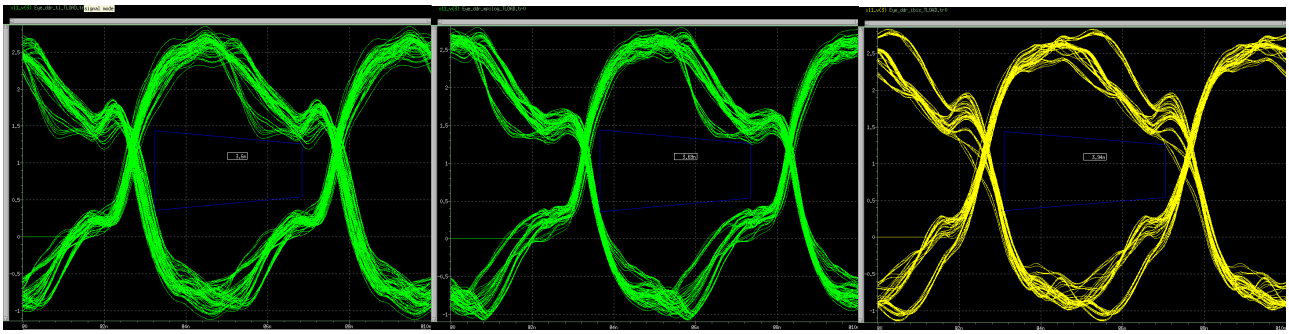


Fig. 7. Eye diagrams arising from the far end voltage response of the first driver in the simulation setup (b) and for the second test case. Left: reference transistor level model; middle: Mpilog model; right: Ibis model.

Table IV. Eye opening for the eye diagrams of Fig. 6 and 7

	Setup (a), second test case		Setup (b), second test case	
	Eye opening	Error	Eye opening	Error
Reference (trans. level)	73.8%	-	72%	-
IBIS	46.2 %	38.3 %	78.8 %	9.5 %
MPILOG	77.6 %	3.75 %	73.8 %	2.5 %

5. Results for the third test case

As already done for the first two test cases, the same set of simulations has been carried out to assess the accuracy of the proposed models for this additional chip. As an example, Fig. 8 and Fig. 9 show the eye diagrams derived from both the output port voltage $v_1(t)$ of the setup (a) of Fig. 1 and the far end voltage response of the same driver in the setup (b) of Fig. 1. Also for this test case, a longer bit stream defined by a 128-long pseudo random binary sequence is used as the input of the drivers in Fig. 1. Table V collects the results on the IBIS and of the Mpilog models in predicting the eye opening, thus confirming the enhanced accuracy of the proposed models.

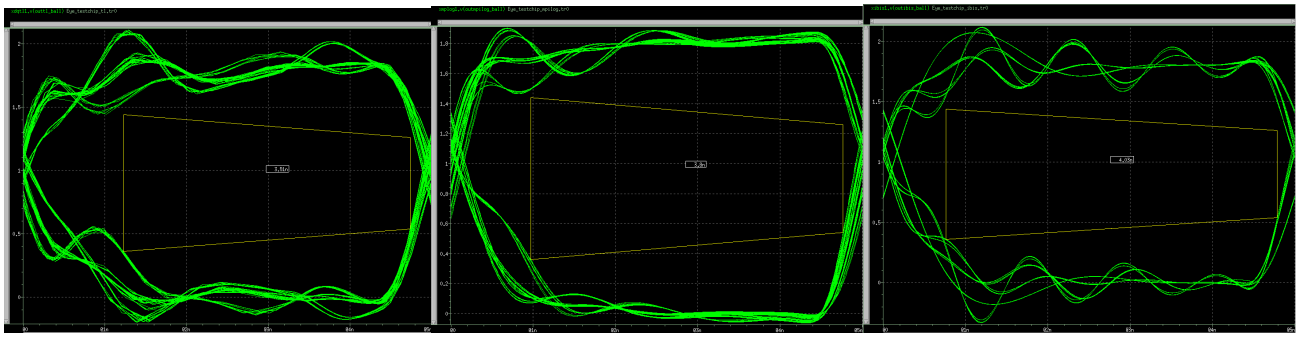


Fig. 8. Eye diagrams arising from the voltage signal v1(t) of the simulation setup (a) and for the third test case. Left: reference transistor level model; middle: Mpilog model; right: Ibis model.

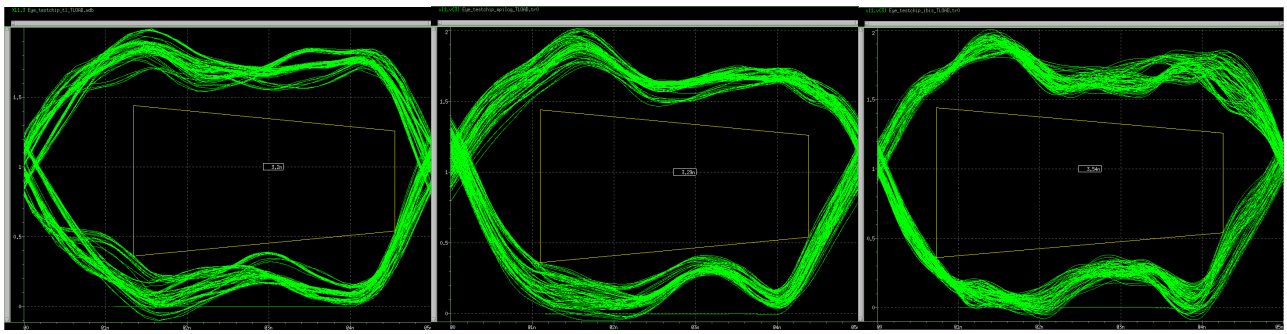


Fig. 9. Eye diagrams arising from the far end voltage response of the first driver in the simulation setup (b) and for the third test case. Left: reference transistor level model; middle: Mpilog model; right: Ibis model.

Table V. Eye opening for the eye diagrams of Fig. 8 and 9

	Setup (a), second test case		Setup (b), second test case	
	Eye opening	Error	Eye opening	Error
Reference (trans. level)	70.2%	-	64%	-
IBIS	80.6 %	14.8 %	70.8 %	10.6 %
MPILOG	76 %	5.3 %	65.8 %	2.8 %

References

[1] I/O Buffer Information Specification (IBIS) Ver. 5.0, on the web at http://www.eigroup.org/ibis/ibis.htm, Aug. 2008.

[2] P. Pulici, A. Girardi, G. P. Vanalli, R. Izzi, G. Bernardi, G. Ripamonti, A. G. M. Strollo, G. Campardo, "A Modified IBIS Model Aimed at Signal Integrity Analysis of Systems in Packag,e" IEEE Trans. On Circuits and Systems, Vol. 55, No. 7, Aug. 2008.