SEVENTH FRAMEWORK PROGRAMME
THEME [ICT-1-3.1]
Next-Generation Nanoelectronics Components and Electronics Integration

Deliverable Report

Work Package 3 – SiP design and verification EDA platform

Deliverable D3.4 - Functionality description of SiP Platform including validation report, for purpose of dissemination to be published & presented at conferences

Contract no.:	216732
Project acronym:	MOCHA
Project full title:	MOdelling and CHAracterization for SiP Signal and Power Integrity Analysis
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Report responsible partner:	CADENCE and AGILENT
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Dissemination level:	PU
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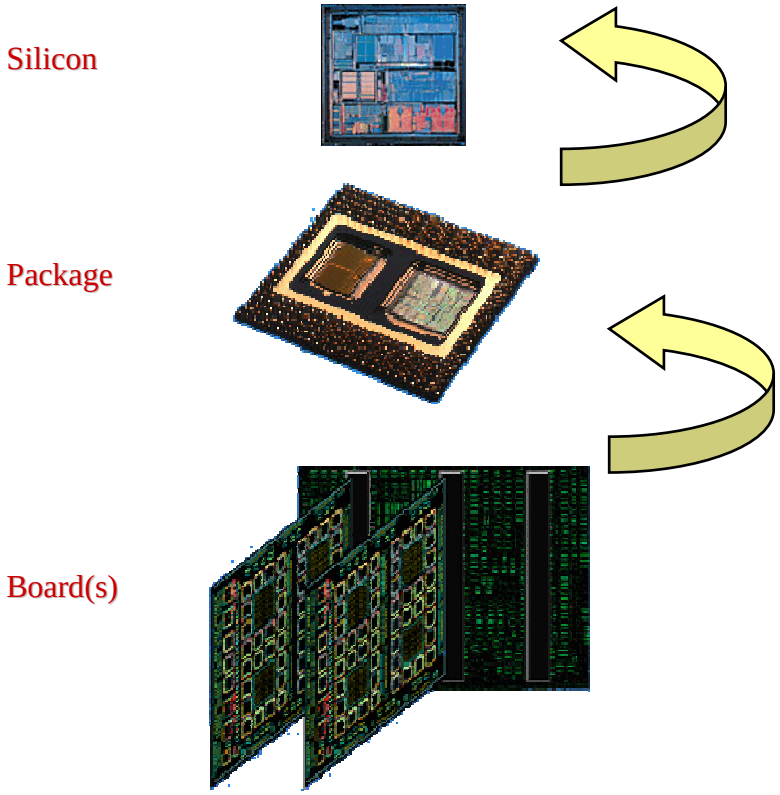
WP3 leader organization:	Cadence
Project coordinator:	Antonio Girardi
Project coordinator organization:	Numonyx Italy Srl

Revision: 1.0

Contents

1. Introduction

Power Integrity (PI) as a concept was introduced several years ago to describe the design goals and methodologies of power delivery network on a system that includes chips, packages, and boards. Unlike signal integrity (SI) analysis, power integrity analyzes phenomena on power delivery paths from battery to active devices through boards and packages.

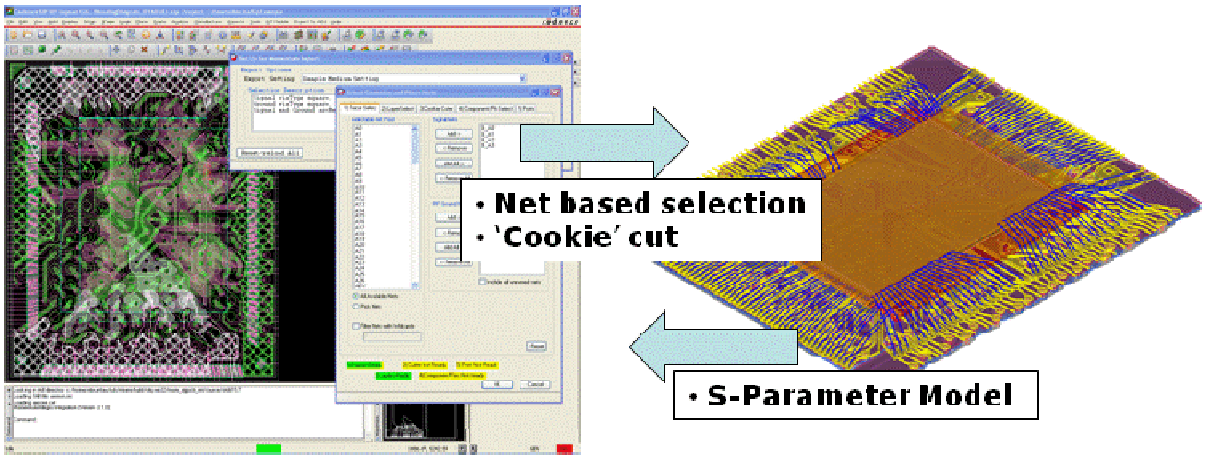


Taking this idea to the next level is to provide a combined methodology for PCB, IC package and IC design, while addressing IO as well as core power delivery. Next to such a framework, the essential piece to this is the development and integration of a 3D EM field solver that is able to generate electrical models for passive SiP interconnect with special focus on the kind of large structures that power and ground nets usually are built of. Such a tool has been implemented by Agilent and Cadence, while receiving feedback and validation results from Numonyx and MC2.

2. 3D EM Tool Development and Integration

2.1 Introduction

This part summarizes the activities carried out as part of Task 3.1 “3D EM tool development and integration” of WP3.



The work of Task 3.1 can be split in 3 main activities.

The first is the development of the "EM front-end module". The objective of this is to address the need of extraction and transfer of the necessary design data available in the Cadence SiP platform into the 3D EM simulator.

The second are the enhancements to the 3D EM field solver needed to handle typical SiP designs.

Third, to finalize the integration in the SiP platform, there is the back-annotation of the EM S-parameter model back to the SiP platform.
The validation of the 3D EM tool is subject of Deliverable 4.3. Only some representative results are shown here.

Finally, we summarize the EM model generation work done in support of Task 3.5 "EDA platform validation and model correlation on a complete system (IC+PKG+PCB).

The partners that have been mainly involved in this activity are CADENCE and AGILENT. NUMONYX and MC2 are involved for the validation of the EM field solver and the SiP platform.

In the following, a detailed description of the different activities is given.

2.2 EM front-end module

A net driven selection and export to the 3D EM simulation environment is available from the SiP Layout Platform through the front end module created in the context of this task.

The flow through the front end tool is as follows:

1. Choose a set of export rules optimizes for the EM simulation at hand (define new rule sets if needed)
2. Select the nets of interest based on the distinction between:
   - RF Signal Nets which are the actual nets of interest
   - RF Ground Nets that have significant impact on the behavior of these RF Signal Nets
3. Limit the layer stack to a subset of drawing layers, add ref. plane definitions, and define solder ball properties.
4. The cutter feature allows to limit the simulation to the area define by the signals of interest.
5. Select the components and component pins connect to the selected nets that need to be considered for the EM simulation.

6. Next build the ports for EM simulation automatically using the defined pin list.
7. Export the design subset to the EM simulation environment.

The figures below illustrate this export operation using the example design provided by Numonyx. The setup window allows choosing the export rules for the export of design data. A set of nets that need simulation are selected in the Select Geometry window.

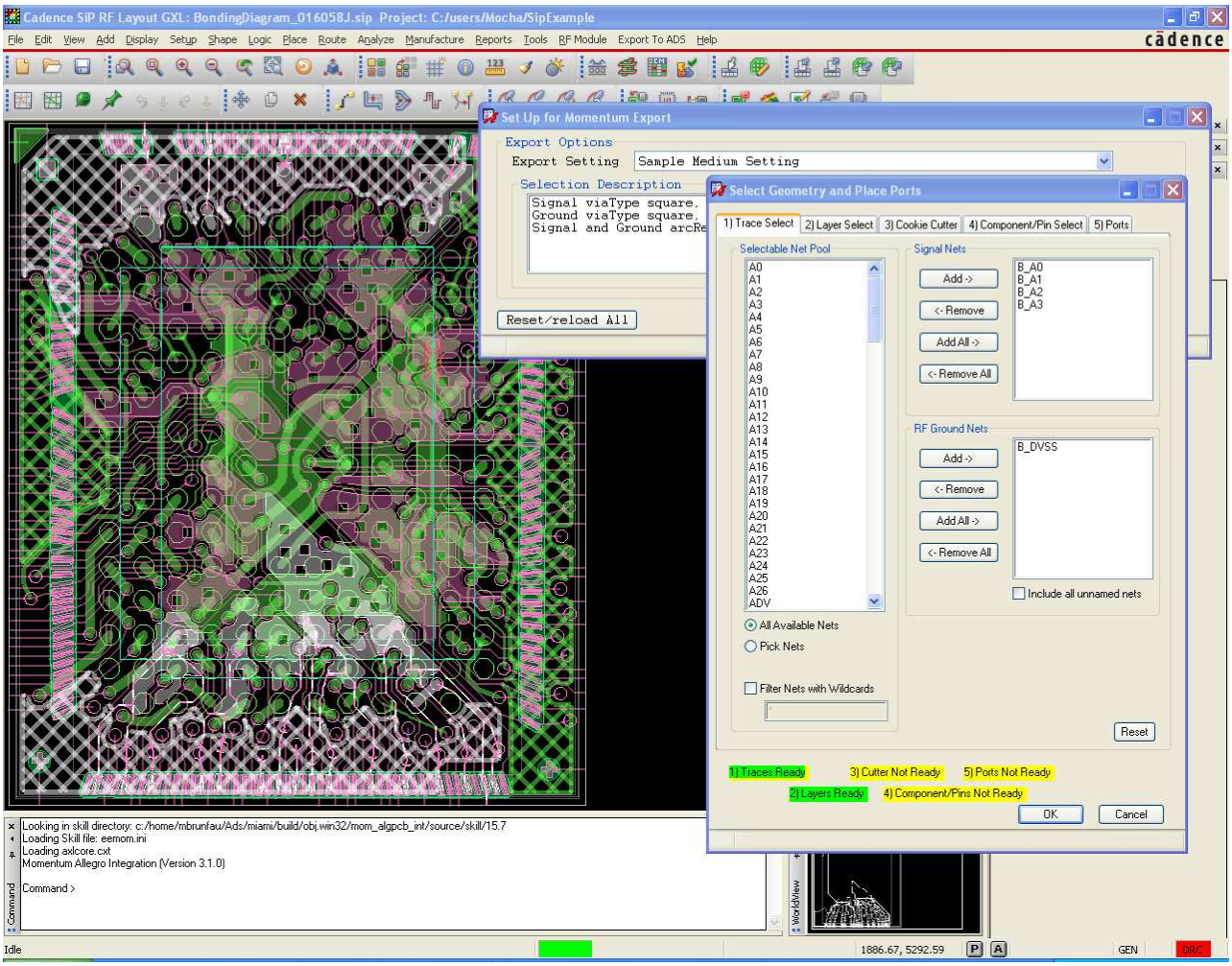


Figure 3 - Setup and selection UI of front end module

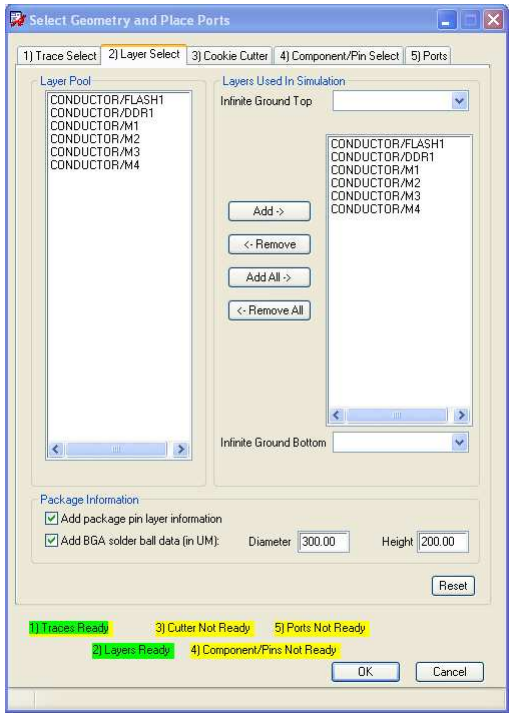


Figure 4 - Define the layer stack, reference planes and pin/solder balls

In the Layer Select tab of the selection window the user can remove certain layers from the simulation, add infinite plane reference layers and define the properties of package pins (solder balls) as these objects are not completely defined inside the Sip database.
In a third step the volume around the selected signal nets and a cutout from the ground nets is defined in the Cookie Cutter tab.

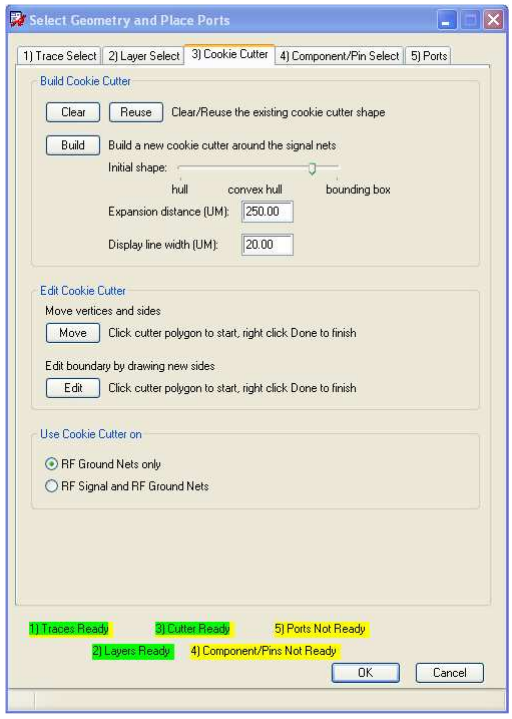


Figure 5 - Defining the cutter region

The Component/Pin selection tab now allows selecting that pins of the components that the user wants to consider in the EM simulation.

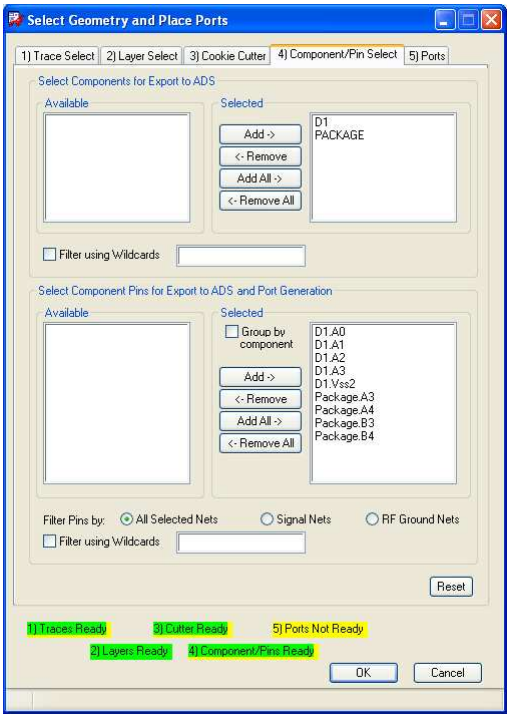


Figure 6 - Select the set of component pins for EM simulation

In a final step of the selection process the actual EM simulation ports are created automatically.

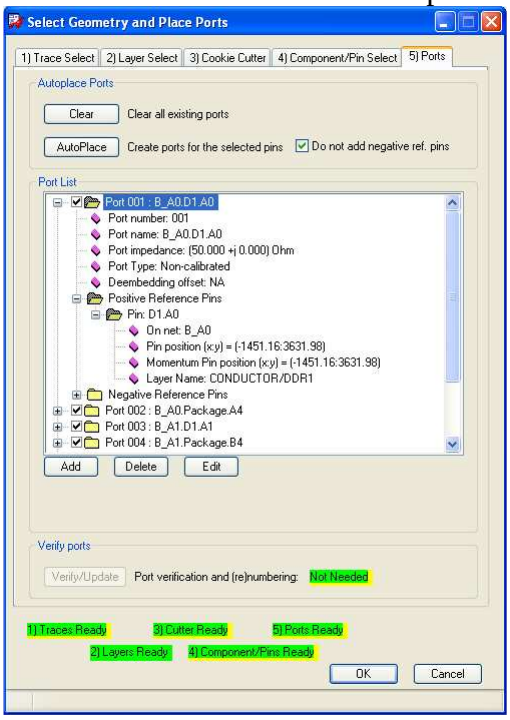


Figure 7 - Definition of the EM simulation ports based pin, component and ref. plane info

Sufficient selection information is now present to export the simulation data on the nets of interest from inside the SiP tool. The properties of bond wires, chip stacks, spacers, interposers are automatically transported to the EM simulation environment by the export command.

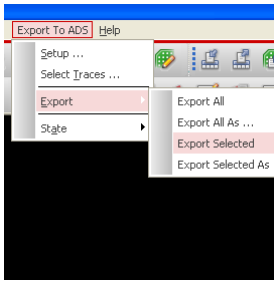


Figure 8 - Final export step extract the design data necessary to do an EM simulation

In the EM simulation environment the results of the export can be viewed.

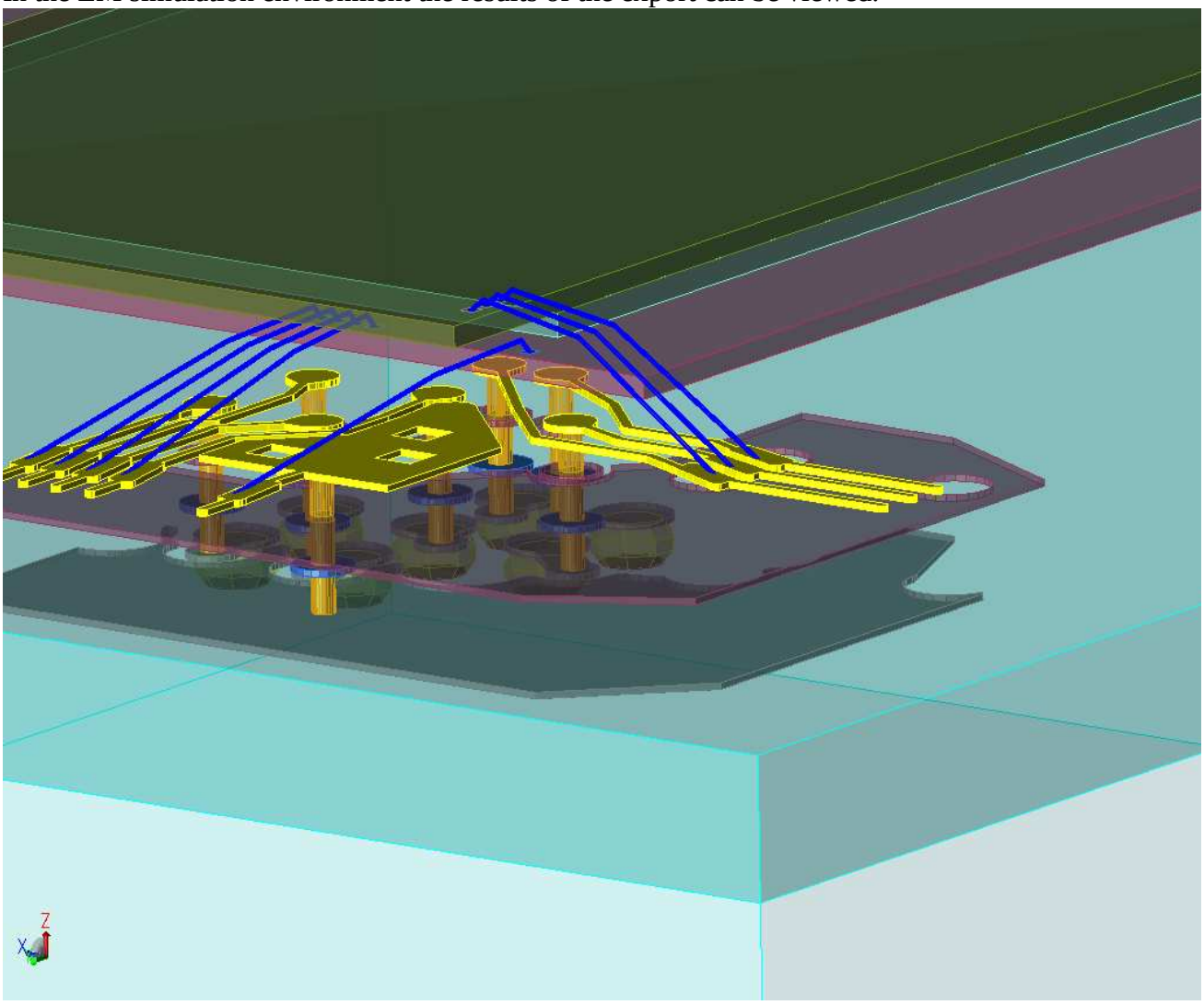


Figure 9 - Snapshot of an exported signal subset inside the EM simulation environment

2.3 3D EM field solver development

The EM field solver development work was bundled as subtask 3.1.2 “Advanced meshing and solving”. Before a layout is sent to the EM field solver, a pre-processing step is carried out. This step prepares the layout in such a way that the new layout representation, after pre-processing, is optimally tuned for efficient and accurate EM simulations. This involves two aspects: layout healing and layout simplification.

Layout healing merges points and lines in very close proximity. Its main purpose is to correct numerical issues in the layout that obstruct the creation of a high-quality conformal mesh. The figure below illustrates the types of layout problems that get corrected with layout healing. This involved eliminating small gaps in the layout, resolving misalignment of layout objects on different layers or eliminating small angle features. Problems like this really can make the EM simulation and meshing very in-efficient.

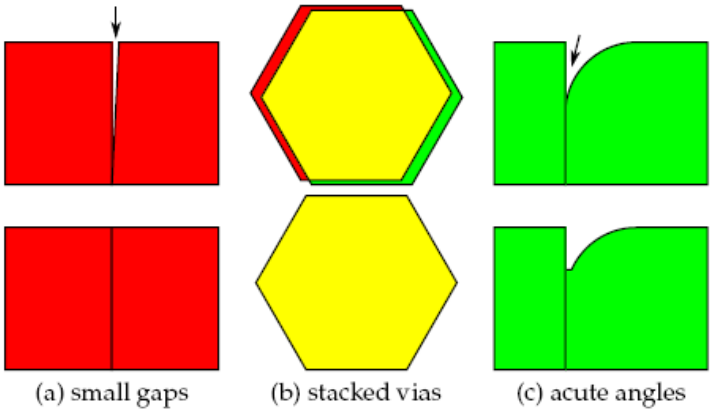


Figure 10 - Types of layout problems that get corrected with layout healing.

Layout simplification replaces polygons by nearly identical polygons with fewer vertexes. Its main purpose is making the generation of a conformal mesh containing the least edges possible. Layout simplification may also create higher quality meshes as it removes many small segments.

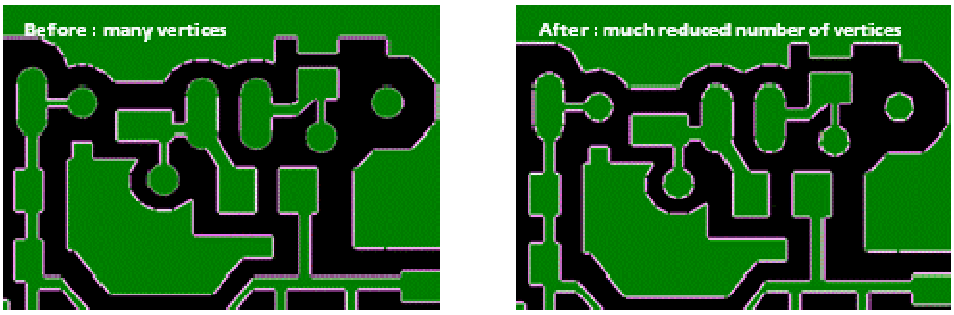


Figure 11 - The layout simplification reduces the number of vertices in the rounded artwork, typically found in board, package or SiP layouts

The pre-processed layout is than sent to the EM field solver. The solver meshes the structure so that Maxwell's equations can be solved. Within the project, the core meshing algorithms have been upgraded to make use of state-of-the-art geometrical processing approaches.

The EM field solver has been extended to account for the presence of the wire bonds. Each wire bond is passed to the solver as a sequence of 3D line segments with properties attached like radius, conductivity, net name, etc.

The mesher identifies the proper position of the wire bonds and the location of the contacts with the rest of the circuit, e.g. the package fingers or die pads. Each wire bond adds 1 additional unknown to the EM interaction matrix. This unknown allows determining the amplitude of the current which is

flowing through the wire bond. Because the wire bonds are now an integral part of the EM interaction matrix, an S-parameter model is obtained for the overall circuit.

A lumped series RL impedance is obtained as electrical model for the wire. The electrical model includes the resistance R and inductance L of the wire as calculated from the geometry and the material parameters. The model further includes the mutual inductance M between the wires and the mutual inductance with a ground plane in the substrate. The ground planes in the substrate stack are automatically taken into account so that wires that are separated by an infinite ground plane are automatically uncoupled. Skin effect (yielding a higher resistance and a lower internal inductance as frequency increases) is included when a wire material with conductivity is specified.

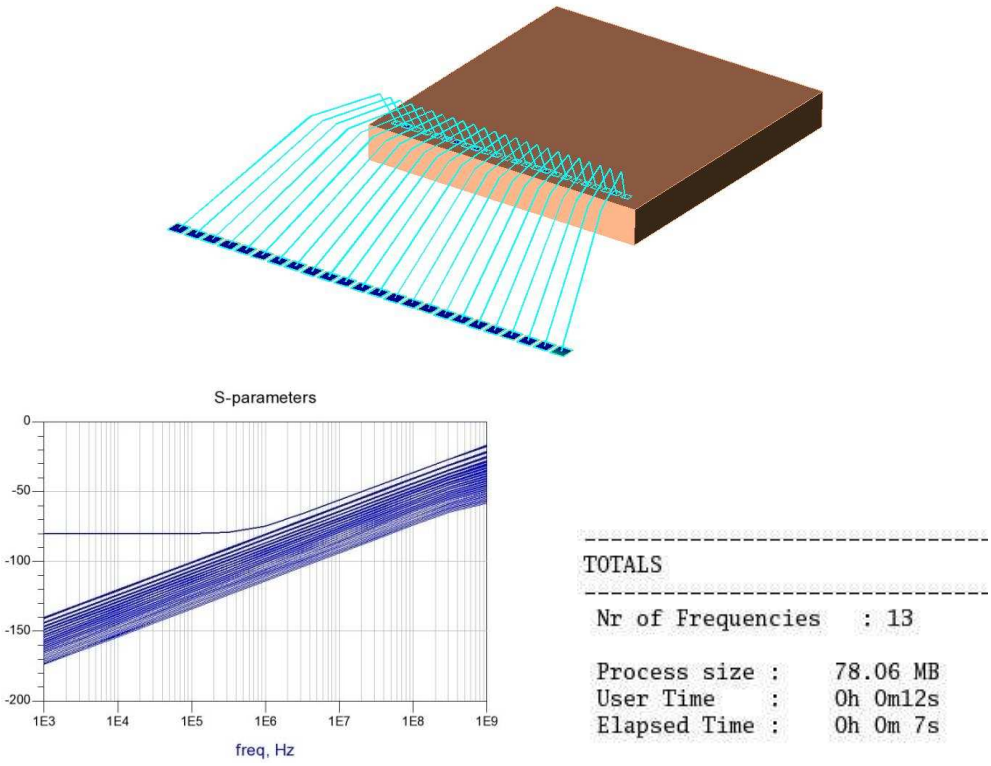


Figure 12 - Example with typical wire bond profiles from Cadence SiP environment

2.4 Finalize tool development

The EM field solver integration and validation work was bundled as subtask 3.1.3 “Finalize tool development”. With the above subtask accomplished, the entire flow can be completed. The flow encompasses the export of selected nets from the SI/PI platform to the EM field solver, the corresponding EM model generation and the back-annotation of that model to the platform so that it can be incorporated into a further analysis. The integration between the SiP Platform and the EM field solver has been tested for a BGA package of Numonyx.

The test-case used in Numonyx is a 10.5 x 13 x 1.4 mm BGA with 165 balls that contain two stacked devices: a 512Mbit Flash memory plus a 512Mbit RAM. The package substrate is composed by four metal layers. The outer layers are mainly dedicated to signals routing, the inner layers are dedicated to power and ground nets. A more detailed description can be found in the Milestone M3.8 report.

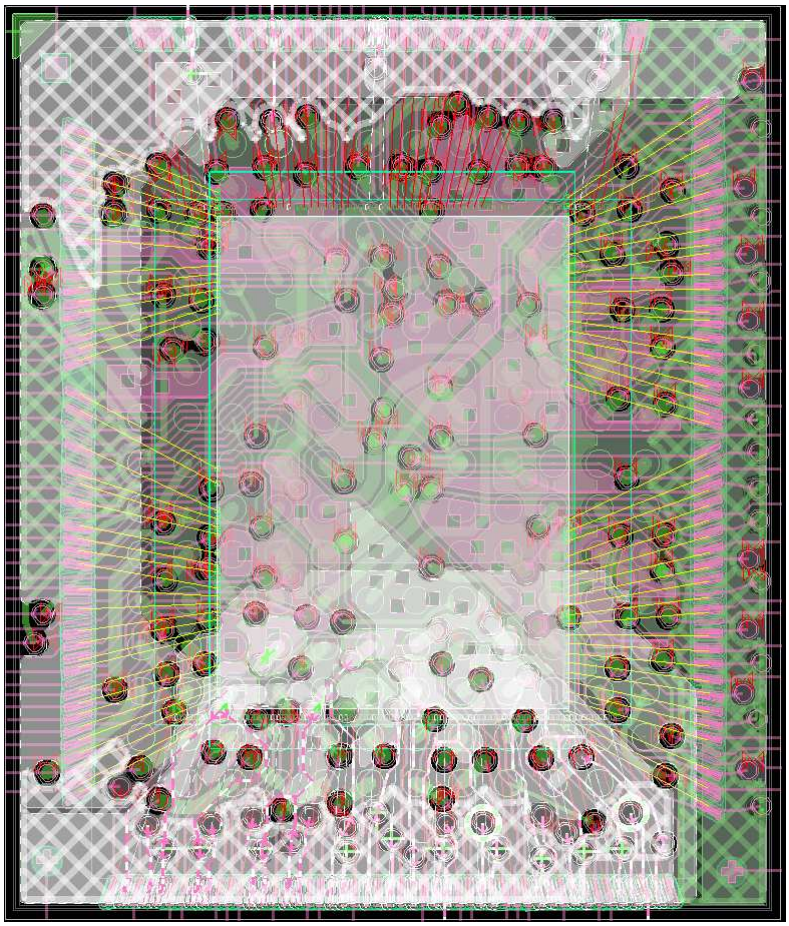


Figure 13 - BGA package

The EM field solver provides a model for the B_DVCCQ power and B_VSS ground plane which is used in the Power Integrity (PI) analysis tool in Cadence's SiP platform.
The flow starts in the SiP platform where the net selection is made of what will be exported to Agilent's EM field solver. The selection in this example is straightforward. Two nets and all associated pins will be transferred.

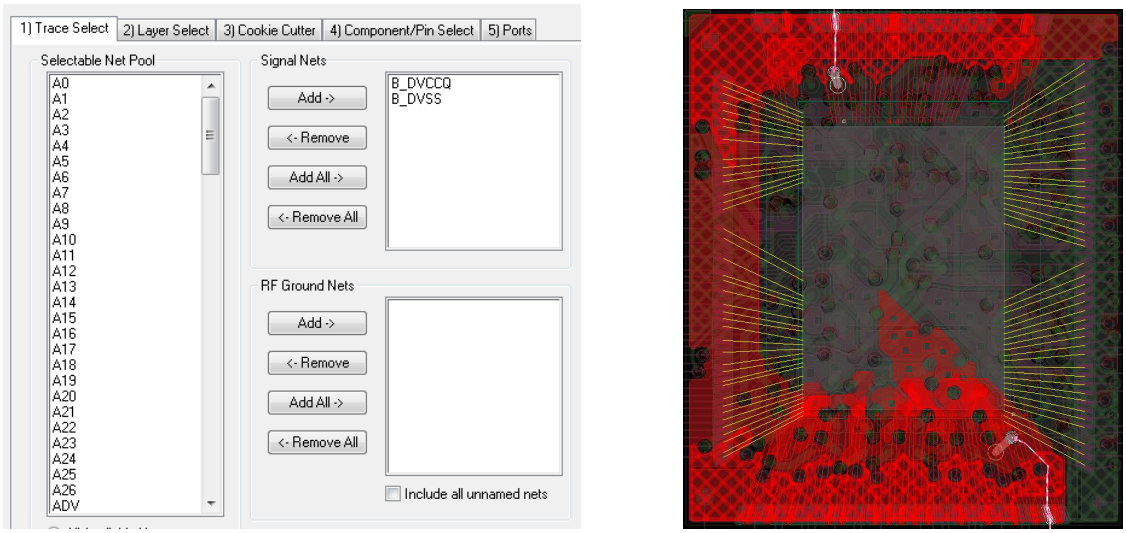


Figure 14 - Net Selection in the SiP platform

37 pins (balls and pads) are associated with this selection. A 3D view of the exported layout is shown below.

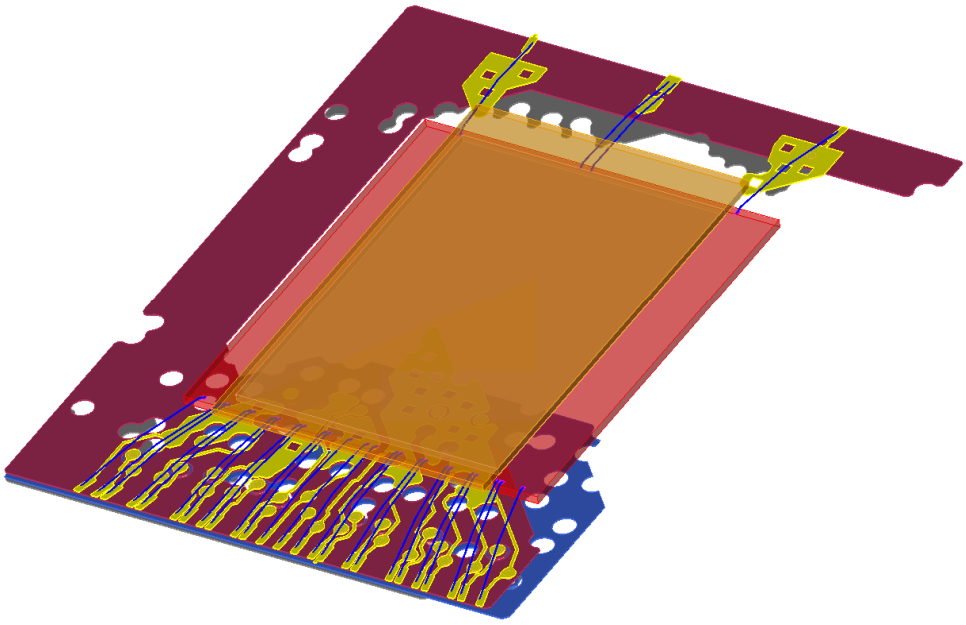


Figure 15 - 3D view of the layout simulated by the EM field solver

The EM field solver doesn't group (short) similar pins together by default as this is a low frequency approximation that is only valid when the electrical distance between the pins is small. In the model that was generated, each pin corresponds with an S-parameter port. Consequently, a 37x37 S-parameter model for this power/ground plane structure was generated, valid from DC up to 10 GHz.

This model is passed back to the SiP platform through an interconnect model file (IML).

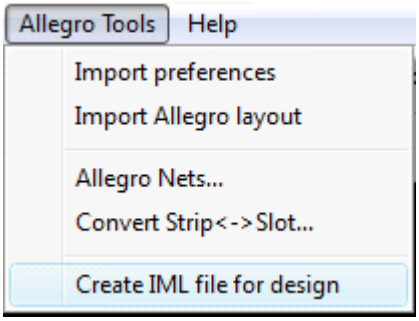


Figure 16 - Back-annotation of the EM model to the SiP platform through IML file

The figure above shows the "Allegro Tools" menu that provides the interface between the Cadence SiP (Allegro) platform and the Agilent EM simulation environment. The "Create IML file for design" item allows the users to generate an interconnect model file in an easy way. It starts from an existing EM simulation result for the current design and writes out the IML file to a user selected filename.

The IML file is using the Touchstone S-parameter file format with a type 2 S-Parameter Model File Header as supported by the Cadence SiP environment. This header format allows transferring the multi-port net results correctly from the solver to the Cadence SiP platform.

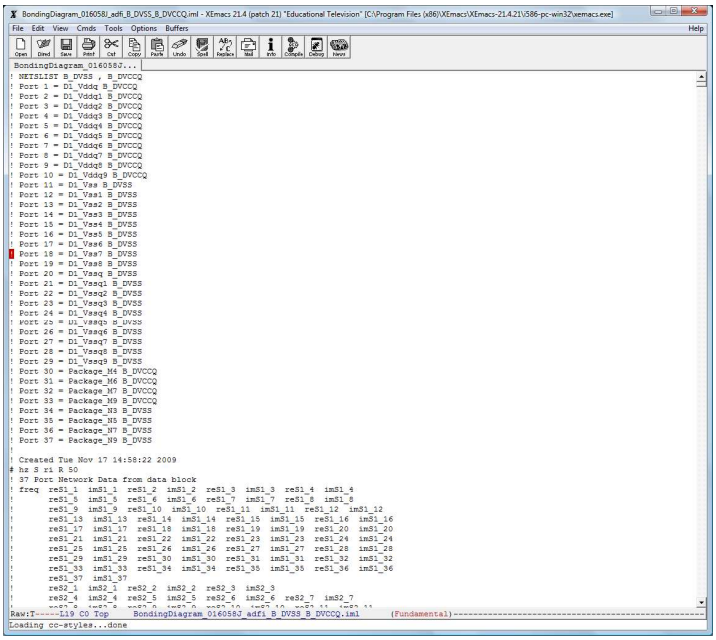


Figure 17 - IML file header

In the Cadence PI flow a model in the Cadence dml (device model language) format is required. The model needs to be a Package Device model with a subcircuit definition with nodes representing the power/ground pins. In the Cadence PI flow it's possible to select the option ¨Reuse previously extracted dml model¨ as shown in Figure 18. The referenced model file will be checked if the subcircuit definition matches to the current design database. If the database matches to the dml model, it is marked as valid model and will be used to calculate the impedance profile in frequency domain or the voltage ripple in time domain.

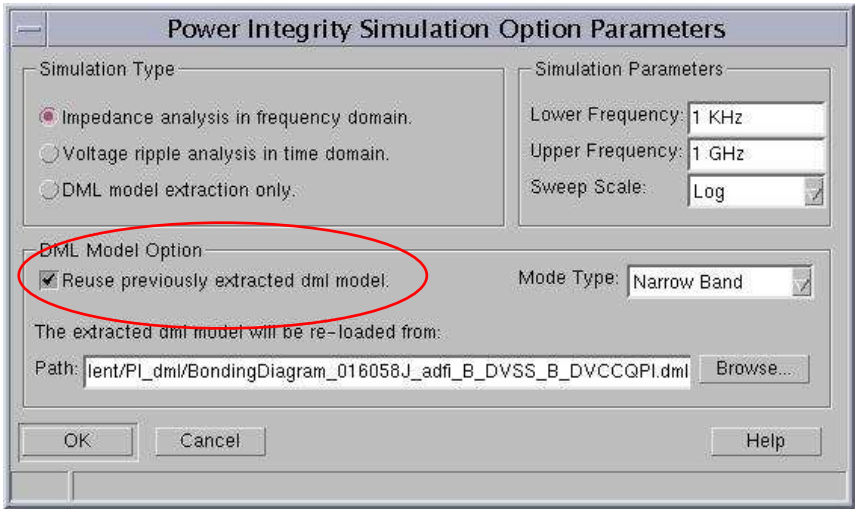


Figure 18 – Cadence PI Simulation Options Parameter form

To be able to use the iml model file provided by the EM solver in the Cadence PI flow it has to be converted to a package device dml file with the right number and order of subcircuit nodes.

The following actions describe how to convert the iml model provided by the EM solver to a valid dml model.

First step is to use the standard S-Parameter to DML converter provided with the Cadence SPB tool installation.
In a UNIX shell the command to be entered is:

ts2dml ¨modelname.iml¨

The resulting file ¨modelname.iml.dml¨ file would need to be modified to match the required format for the Cadence PI flow.
A wrapper program, written in SKILL is used to convert the ¨modelname.iml.dml¨ file into a file called ¨modelnamePI.dml¨ that has the required dml syntax and the right subcircuit calls and nodes so that the Cadence PI flow will accept this dml file as a valid dml model to calculate and display the impedance profile or voltage ripple.

In addition in the Cadence PI flow it is possible to combine ports of power and ground pins in so called port groups together. The resulting subcircuit in the dml file will have only one node of each port group defined. Although grouping of ports is only meaningful for low frequencies if ports are next to each other the wrapper program will modify the dml file in a way that the subcircuit will have only one node for each port group. The nodes of the subcircuit having nodes for each power and ground port will be mapped to the right port group node.
The following example will illustrate the mapping in more detail. The subcircuit `BondingDiagram_016058J_adfi_B_DVSS_B_DVCCQ` is defined with 5 nodes. The design has 37 B_DVCC and B_DVSS pins in total as shown with 37 nodes in the subcircuit `BondingDiagram_016058J_adfi_B_DVSS_B_DVCCQ_37Port_Data`. The 37 pins are grouped together in 5 different port groups. In the subcircuit call `XBondingDiagram_016058J_adfi_B_DVSS_B_DVCCQ_37Port` each of the 37 nodes have to be mapped to one of the 5 port group nodes. If we look at the port group PACKAGE-N3-Reference that contains the 4 B_DVSS pins at the package component (Ports 34 – 37 in Figure) the nodes 34-37 in the subcircuit call `XBondingDiagram_016058J_adfi_B_DVSS_B_DVCCQ_37Port` are all named with the port group node `PACKAGE-N3-Reference`.

```
".subckt  BondingDiagram_016058J_adfi_B_DVSS_B_DVCCQ  PACKAGE-N3-Reference  D1-
VSSQ3-2 D1-VDDQ-4 PACKAGE-M4-1 D1-VDDQ3-3

XBondingDiagram_016058J_adfi_B_DVSS_B_DVCCQ_37Port D1-VDDQ-4 D1-VDDQ3-3 D1-VDDQ3-
3 D1-VDDQ3-3 D1-VDDQ3-3 D1-VDDQ3-3 D1-VDDQ3-3 D1-VDDQ3-3 D1-VDDQ3-3 D1-VDDQ3-3
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PACKAGE-M4-1 PACKAGE-M4-1 PACKAGE-N3-Reference PACKAGE-N3-Reference PACKAGE-N3-
Reference                                          PACKAGE-N3-Reference
BondingDiagram_016058J_adfi_B_DVSS_B_DVCCQ_37Port_Data

.subckt BondingDiagram_016058J_adfi_B_DVSS_B_DVCCQ_37Port_Data 1 2 3 4 5 6 7 8 9
10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36
37
```

Which of the port group ports have to be used in the subcircuit call and in which sequence can be read out of the design database.

If no port groups were used in the design the wrapper would also create a valid dml model file without the need to map nodes.

Another option in the Cadence PI flow is to add ¨Virtual Capacitors¨ to the design as seen in Figure . These capacitors would be placed and connected to the power ground nets and would need to be included into the extracted netlist having ports or nodes in the model file.
This feature would allow making feasibility studies, which capacitor would have to be placed at which location to finally get an acceptable impedance profile or maximum voltage ripple.

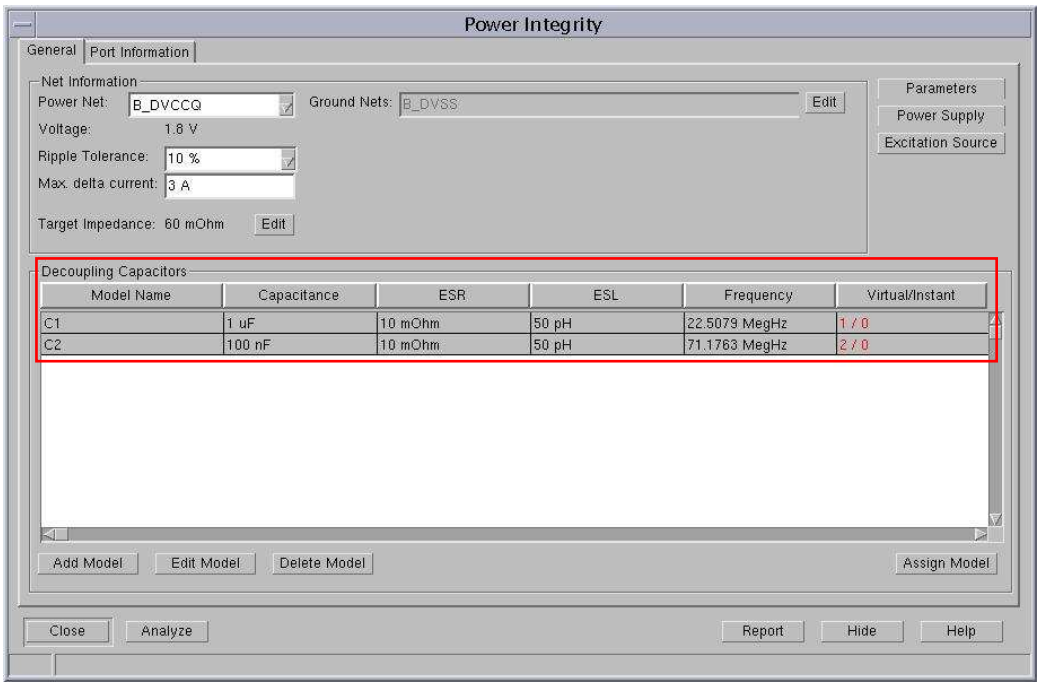


Figure 19 – Virtual Decoupling Capacitors

Currently these virtual capacitors won't be passed to the EM solver and therefor aren't included in the model subcircuit of the EM solver model. That's why a design with virtual capacitors can't be used in a flow with the EM solver from Agilent. Users would have to delete the virtual decoupling capacitors before using the wrapper program.
It may be considered in a next step to include any ¨Virtual Capacitors¨ in the design in the EM solver extraction as well.

2.5EM field solver validation

As a result of WP4, Task 4.2, MC2 delivered a detailed report about the measurements that were carried out in support of the validation of the EM field solver. Time domain measurements (TDR/TDT) have been carried by MC2. Agilent generated EM models for the structures and compared TDR/TDT circuit simulations with the measurements.

Overall, a good to excellent agreement was obtained, what validates the solver development work of WP3. The validation did not lead to specific enhancements of the EM field solver; however it allowed illustrating the importance of a proper setup of the EM simulation. We refer to D4.3 for further details on this activity.

Highlights and key learning's from this activity are listed below.

- A proper description of the substrate stack is crucial. For example, modeling the package cannot be done in isolation from the board it is mounted on. The PCB substrate is needed to properly model the signal's transition into the package.
- Conductor traces can be modeled more efficiently as 2D sheets but this introduces a significant error (10-20%) on the characteristic impedance and propagation factor for typical trace dimensions found in today's boards and packages. 3D modeling is required!
- The EM front-end allows a selective transfer of nets to the field solver. Special care must be taken to include (enough of) the nets that will carry the return path current. Leaving the latter out of the selection will change the current's return path and consequently the resulting model.
- Understanding the port definition for the EM solver is crucial to interpret and use the resulting EM model in a circuit simulator. The voltage at a specific trace port, provided by the circuit simulator, is relative to the absolute (circuit simulator) ground. The EM port definition requires a proper specification of where that reference is present in the physical layout. The reference will often be located at a nearby power or ground net. The return path current will flow back to the source through this reference.
- The mesh created by the EM field solver must be adequate to model the current and charge distribution. Coarse meshing of the power/ground planes allows speeding up the EM simulations but it reduces the accuracy of modeling the return path current. At higher frequencies, the latter tends to concentrate under the signal trace. The 'overlap extraction' and 'layer precedence' features turn out to be very important for an accurate but still efficient modeling.

Some representative validation results are shown below. A dedicated board has been designed and processed by MC2-technologies. This board has simple shapes in order to enable and simplify without ambiguity the simulations results achieved by Agilent technologies. A second SiP test sample provided by Numonyx and processed by ST Microelectronics embeds passive interconnect patterns typically used in SiP package systems. Time domain measurements (TDR/TDT) have been carried by MC2-technologies.

The dedicated test board contains 10 mm long GSGSG lines with variable spacing.

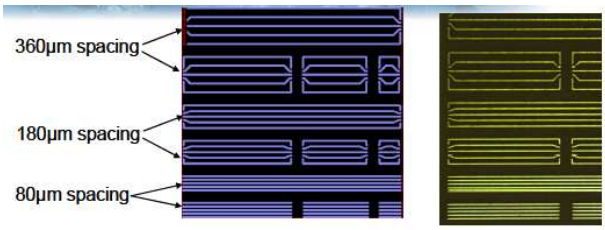


Figure 20 – GSGSG Lines on Dedicated Test Board

With the GSGSG probes, 4-port TDR/TDT measurements were done. The figures below illustrate the good match between measurements and simulations.

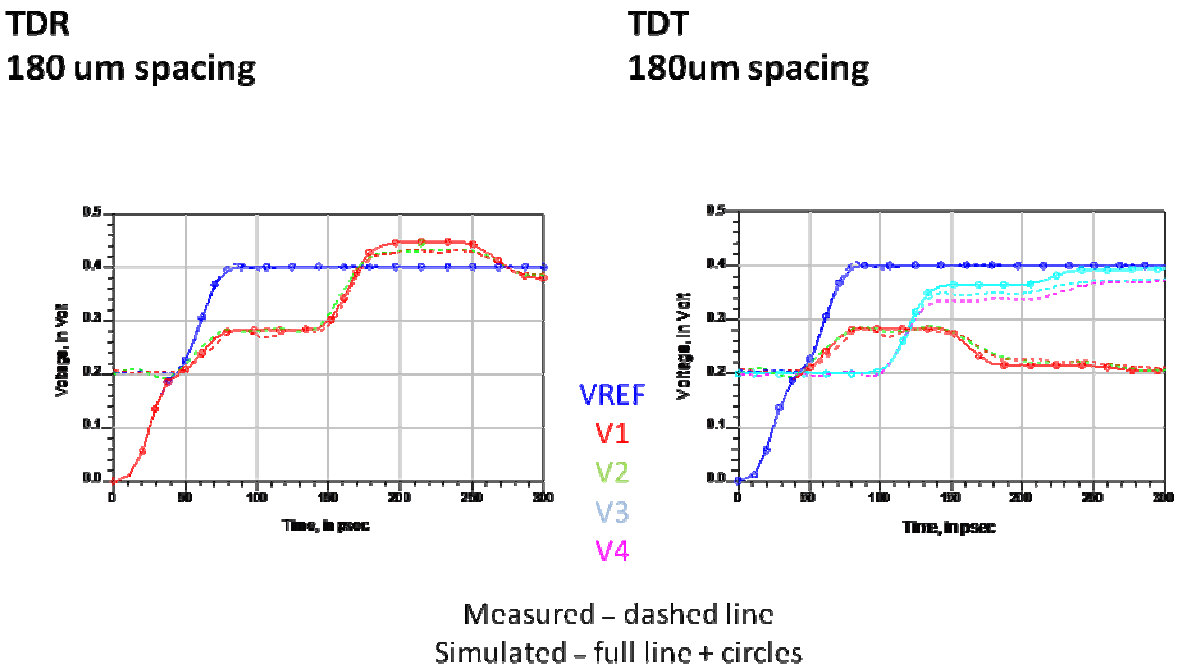


Figure 21 –TDR/TDT results

Another dedicated test board structure investigates the coupling between lines at one side of the board with a meander line at the back side of the board.

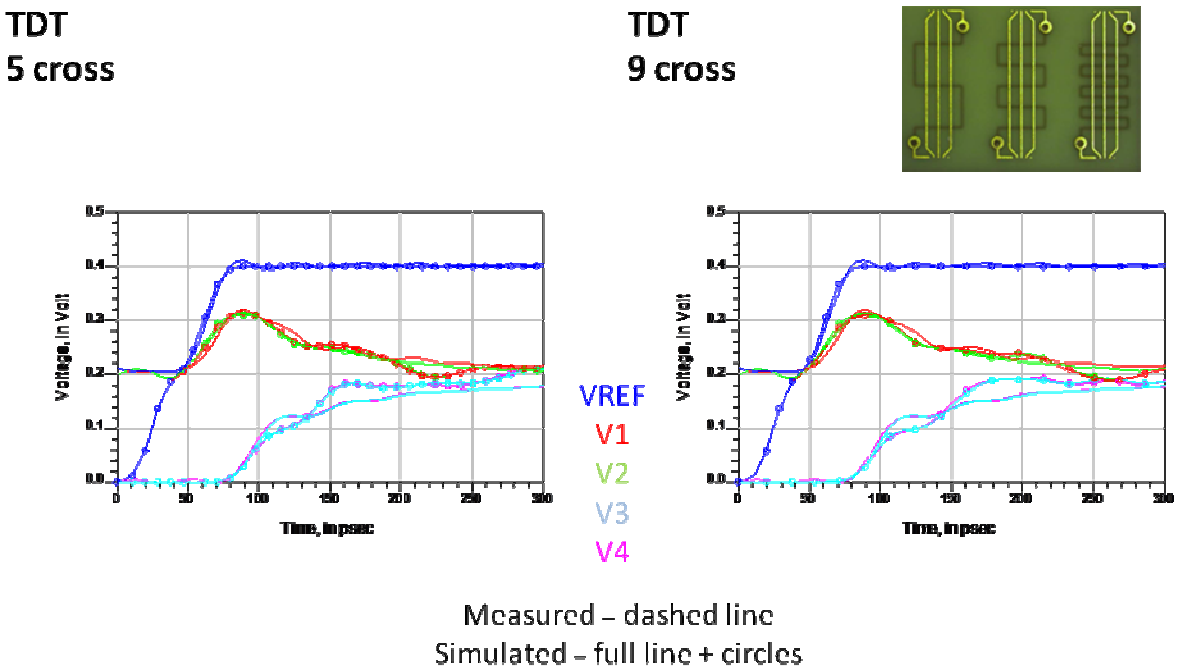


Figure 22 – Meander lines: layout and TDT results

The test sample provided by Numonyx embeds passive interconnect patterns typically used in SiP package systems. Only passives structures are present with lines, via holes, bumps and wire bonds.

All the lines are interconnected with a ground plane above the lines (the grey square) through wire bonds. 16 connections were selected to be the subject of the study.

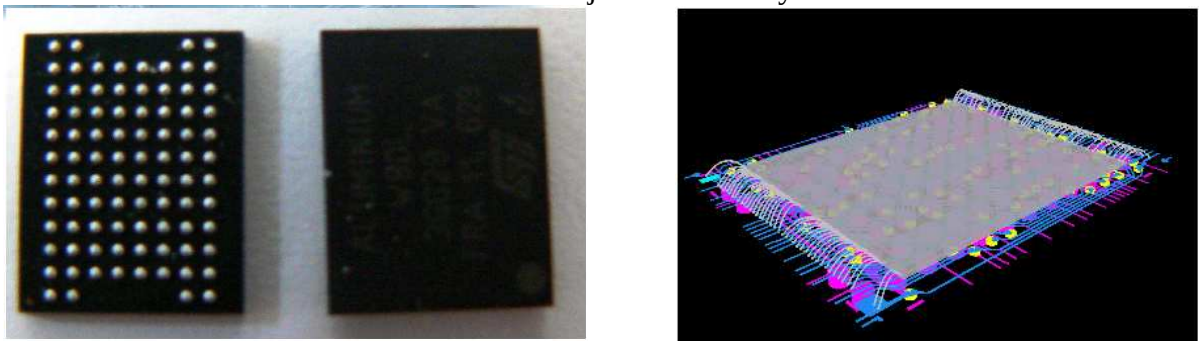


Figure 23 – SiP Test Sample

The complete design, including all the nets, was simulated as a whole. This ensures that the coupling effects with all neighbor nets are taken into account.

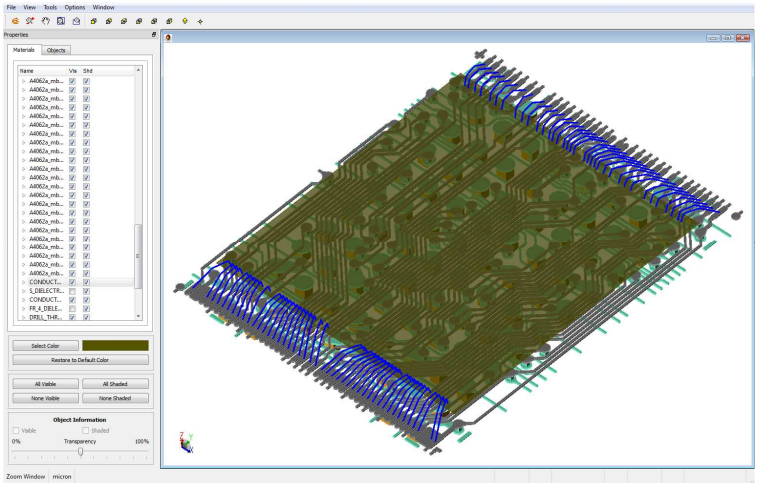


Figure 24 – 3D Visualization of the Simulated Package

A representative result of the comparison between TDR/TDT measurements and simulations for two connectors (2 and 15) is shown below

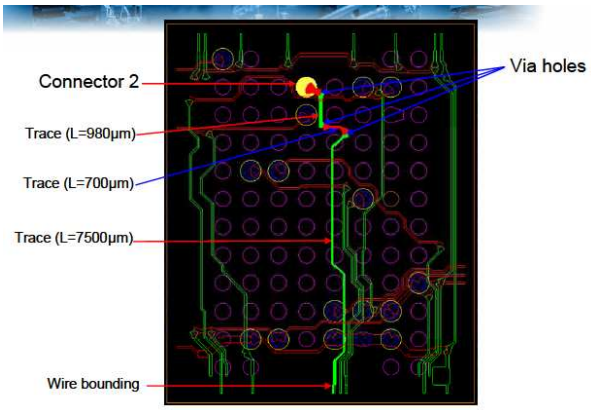


Figure 25 – Connector 2

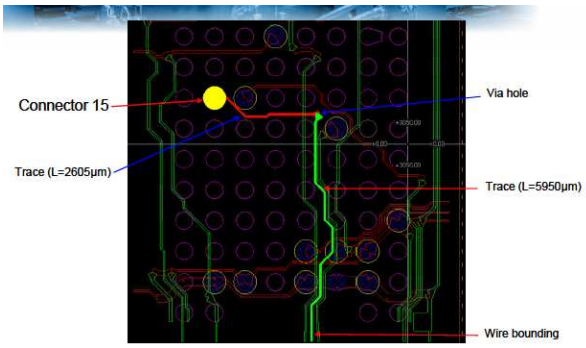


Figure 26 – Connector 15

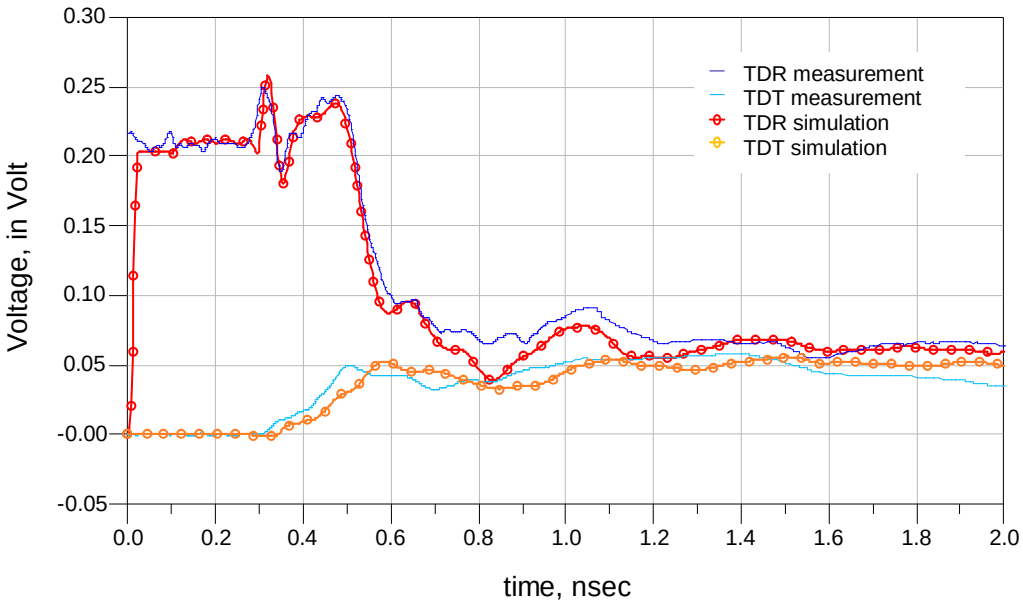


Figure 27 – TDR/TDT Simulation and Measurement from Connector 2 to Connector 15

2.6EM model generation for final platform validation

For the final validation of the complete signal integrity platform several EM simulation models have been created with the Agilent 3D EM solver:

1. model of the entire Numonyx SiP design;
2. models for the signals of interest and the supply system of the memory module board that was used to mount the SiP package during the measurements;
3. model of VDDQF supply net on the main measurement board.

For the creation of the SiP model we could use the developed EDA platform directly. For the two measurement boards, this was not the case. We needed to start from Gerber files exported by another EDA tool what complicated the EM model extraction setup significantly.

2.6.1EM model generation for the memory SiP design

The complete Numonyx SiP design BondingDiagram_016058J was exported from the Cadence SiP layout platform into the Agilent 3D EM solver to construct a full S-parameter model of this physical structure through the export UI.

This BGA package design uses a 4 layer substrate and contains a NOR and a DDR device stacked on top of each other. It has 165 external package pins (solder balls) and the 164 die pads of the chips are connected with 164 bonding wires to the package bonding fingers. The 3D EM simulation includes this entire structure in a single 329 port simulation.

Based on the EM solver validation experiments reported in M4.5, we defined a physical cross-section with an additional perfect ground layer and FR-4 dielectric layer below the actual package solder balls just like the layer structure used by the upper layers in the memory module PCB. This is needed to accurately model the behavior of the mounted BGA on a PCB. A 3D visualization of the simulated structure is shown in Figure 2828. Graphical representation of the substrate cross-section of the simulated SiP design is shown in Figure 299.

The EM simulation of this SiP structure really requires the full featured 3D EM solver developed in the Mocha project context. The layout simplification and mesh generation technology are crucial to minimize the complexity of the simulation. The need for the native integration of the bondwire capability is obvious given the 164 bonding wires in the design. The final method of moments based 3D EM simulation had the following simulation statistics:

1. Simulation for model from DC to 10GHz
2. Layout preprocessing and meshing take less than 10 minutes
3. EM system size of 222387 unknowns
4. The simulation converges after 77 automatically chosen frequencies from the adaptive frequency selection algorithm
5. Process size of the EM solve process is 40293.88 MB
6. Total simulation time was 165.5 hours on an 16-core Linux machine
    a. 10 hours was needed for the first frequency point
    b. 2 hours for each new frequency point that followed
7. Completed EM model requires over 600 MB and proves difficult to handle for circuit simulation due this large size.

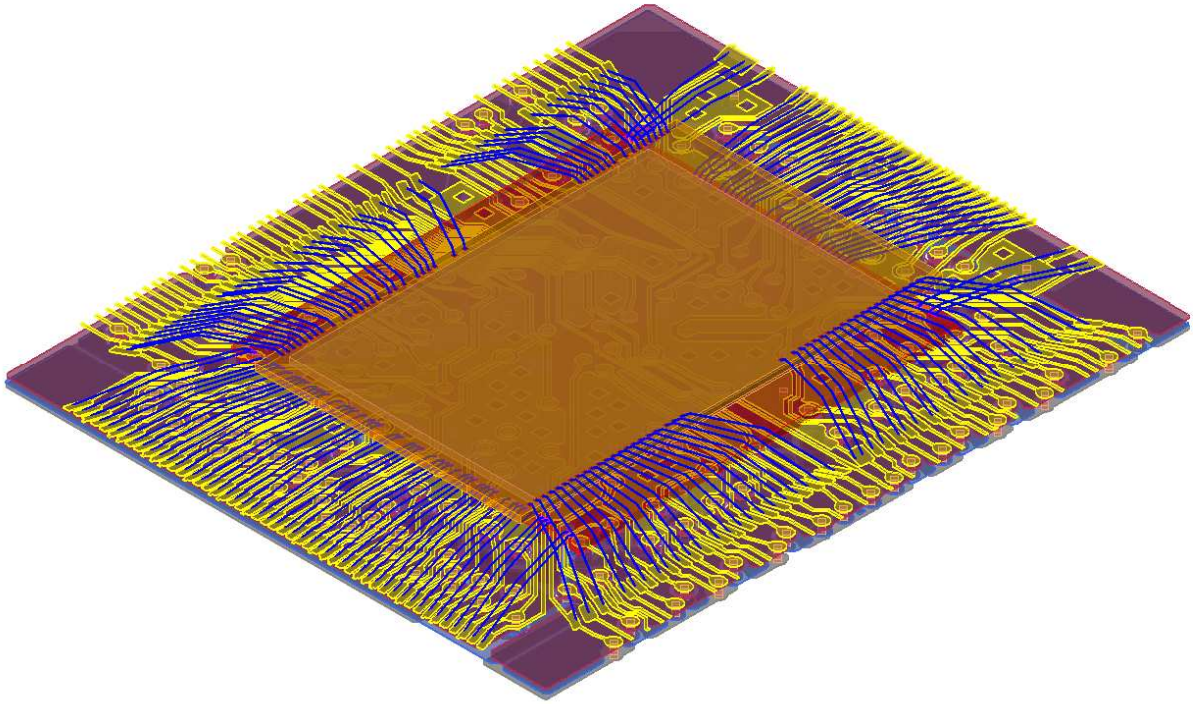


Figure 28 - Visualization of the simulated SiP BGA design with the stacked NOR and DDR device

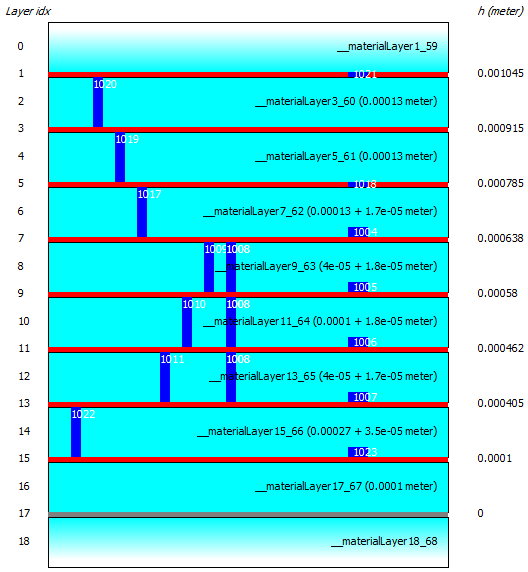


Figure 29 - Cross section definition of the SiP substrate used in EM simulation

From this overall EM model, two sub-models have been derived for use in the simulation test benches in the Cadence SiP simulation platform. One model for each packaged die, limited to the nets of interest for the switching behavior: the data, the strobe, the clock nets and the supply nets of these chips. The overall S-parameter model was re-sampled for the ports associated with these nets at a discrete set of frequencies while the other pins remained open. These models were exported in iml files for use in the Cadence SiP platform.

- For the DDR device the exported iml model contains the nets: B_CLK, B_CLK_N, B_DQ[0-15], B_DLQS, B_ULQS, B_DVCC, B_DVCCQ, B_DVSS.
- For the NOR device the exported iml model contains the nets: WAIT, FCLK, DQ[0-15], VCCQ, F1VCC, VSS.

A complication during the model extraction for the Cadence SiP platform was the selection of discrete sampling frequencies. These frequencies need to be selected sufficiently dense to allow the transient simulator to create the transfer functions and remain sparse enough to keep the size sufficiently small. We found that a sequence of: DC, 20 samples per decade from1MHz to 1GHz and a linear spacing of 0.1GHz up to 10GHz worked well with the Cadence Spectre simulator for the SiP models. Ideally the EM simulator should be guided by the circuit simulator for the frequencies it needs.

2.6.2EM model generation for the memory module board design

This piggy back board used for mounting the SiP design during measurements is the first of the two boards that we need EM models for in order to compare the measurements with simulations. The design measures 90 mm x 110 mm and has 18 metallization layers. The design of the board is constructed in such a way that the data and control signals for the NOR and DDR devices are on 5 separate impedance controlled stripline layers with a ground layer placed above and below. All supply nets have been assigned to individual metal layers which combined with the many decoupling capacitors provide a low impedance supply system for the SiP module under test. The outer layers of the board are the mounting layers for the surface mount devices. All pads there have very short connections from the mounting pads to the inner interconnect layers. Non-used area on the outer layers is filled metal attached to the B_VSS net.

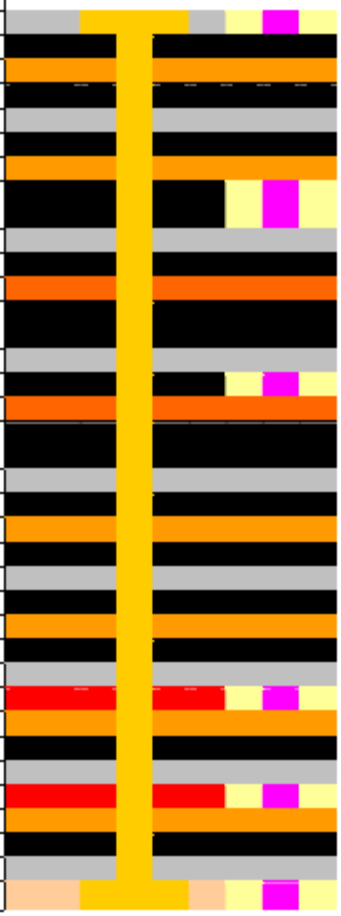
The combination of the size of the board, the number of metal layers and the 843 pins make a complete full-wave EM simulation of this board up to 10 GHz impossible to realize with a reasonable amount of resources. We expect such a simulation to need hundreds of simulation frequencies in the EM simulator to converge and that the resulting model grows into tens of gigabytes of S-parameter data.

We decided, given the quality of the supply system and the stripline architecture for all the other nets to create three EM models of parts of the design. One for the signal nets of interest of the DDR device, one for the signal nets of interest for the NOR device and one lower frequency model for the entire supply system. For the signal nets models of the designs we assumed an ideal supply system around the signal traces, while the supply system model ignored all the signal nets in the system and used a reduced pin count for supply and ground pins on the various connectors.

Unfortunately this test board has not been designed in the Cadence Allegro platform and the lack of a high quality link for importing the structures of interest in the 3D EM simulation environment was a major handicap in creating the EM models. The import and EM simulation setup task which typically takes less than an hour with the infrastructure designed in the Mocha project between the Cadence SiP (Allegro Layout) platform and the Agilent 3D EM simulator changed for this board into a very slow and tedious manual process taking many days of layout manipulation. For this board we needed to start from the Gerber files used for the board fabrication which are not generated with further manipulation in an EDA tool mind. This created lots of problems with the type and complexity of the polygons that the EM tool received after import. Many hours of layout editing in Agilent's ADS platform where needed to create the structures that were viable for EM simulation. Gerber files also don't maintain the device and netlist information and an ad-hoc importer combining the pick and place files and test pin netlist in IPC-D-356A format was created to translate this data from the

manufacturing info into an ADS layout design. Finally the cross-section definition of the board structure needed manual translation and a lot of manual verification to avoid setup errors.

Thickness (um)	Signal types	Layers	Controlled Impedance
35	Pad , signals, ground	1	
100			
17,5	B_VDDQ	2	
100			
17,5	B_VDD	3	
50			
17,5	B_VSS	4	
200			
17,5	LPDDRAM signal	5	55 and 100 ohm
200			
17,5	B_VSS	6	
200			
17,5	LPDDRAM signal	7	55 and 100 ohm
200			
17,5	B_VSS	8	
200			
17,5	LPDDRAM signal	9	55 and 100 ohm
200			
17,5	B_VSS	10	
100			
17,5	VDDQF	11	
90			
17,5	VDDF	12	
100			
17,5	VSS	13	
200			
17,5	NOR signal	14	55 ohm
200			
17,5	B_VSS	15	
200			
17,5	NOR signal	16	55 ohm
200			
17,5	B_VSS	17	
100			
35	Pad , signals, ground	18	
2990			



Through hole diamater : 250um
Pad outer layer and inner layer : 400um
Er = 4,4 preper
Er = 4,4 FR4
Total thickness : about 3mm

Figure 30 - Board cross-section of memory module test board

Figure 31 shows a 3D visualization of the DDR signal nets B_DQ[0-15], B_K, B_NK, B_LDQM, B_LDQS, B_UDQM, B_UDQS with 65 pins which have been simulated with the 3D EM simulator between DC and 10 GHz.
This simulation resulted in an EM system with a size of 24727 unknowns and required 64 adaptively selected frequencies before the simulation converged. Layout preprocessing and meshing took less than 1 minute. The first frequency point was solved after 42 minutes and every following frequency point requires 7.5 minutes. The entire simulation finished in 8 hours 25minutes using 2 GB of memory on a 16-core Linux machine. A densely sampled iml S-parameter file of 86MB was passed back to the Cadence SiP platform for further circuit level simulation.

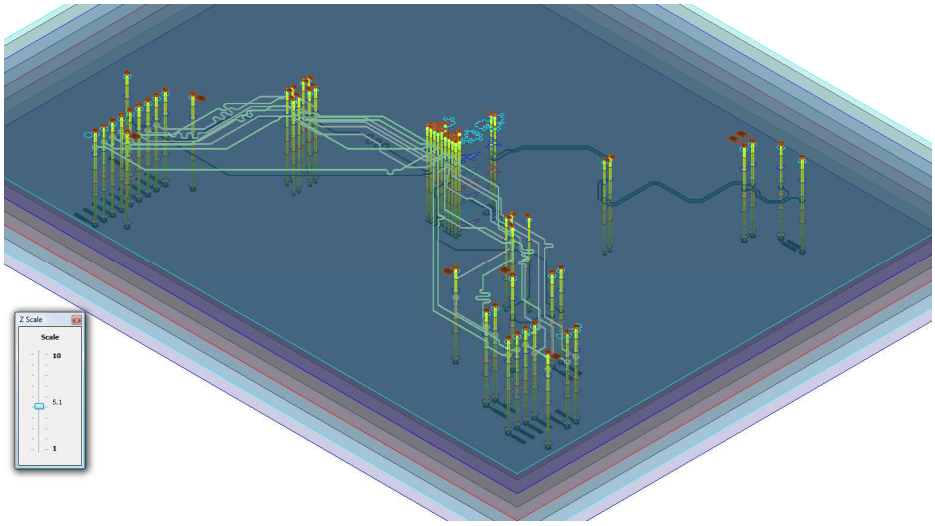


Figure 31 - 3D visualization of the DDR signal nets used for 3D EM simulation

Figure 32 shows a 3D visualization of the NOR signal nets DQ[0-15], KF, WAITF with a total of 55 pins which have been simulated with the 3D EM simulator between DC and 10 GHz. The simulation size was 23116 unknowns and converged after 51 adaptively selected frequencies. The first frequency point is available after 16 minutes and every following frequency point requires 4.5 minutes. The simulation finishes after 3 hours 26 minutes and needs 1.8 GB of memory on a 16-core Linux machine. A densely sampled iml S-parameter file of 56MB was passed back to the Cadence SiP platform for circuit level simulations.

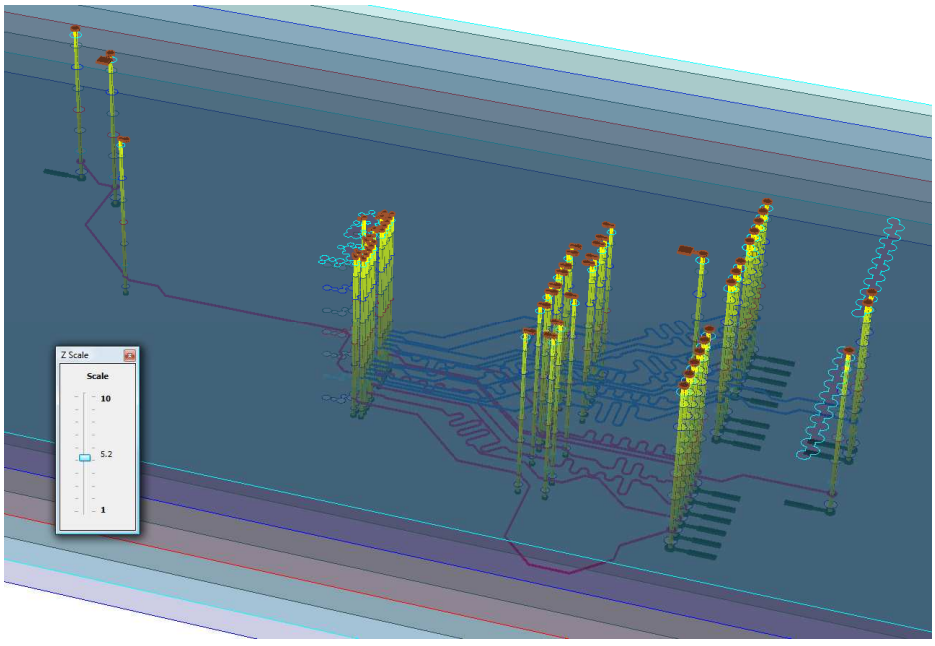


Figure 32 - 3D visualization of the NOR device signal nets used for 3D EM simulation

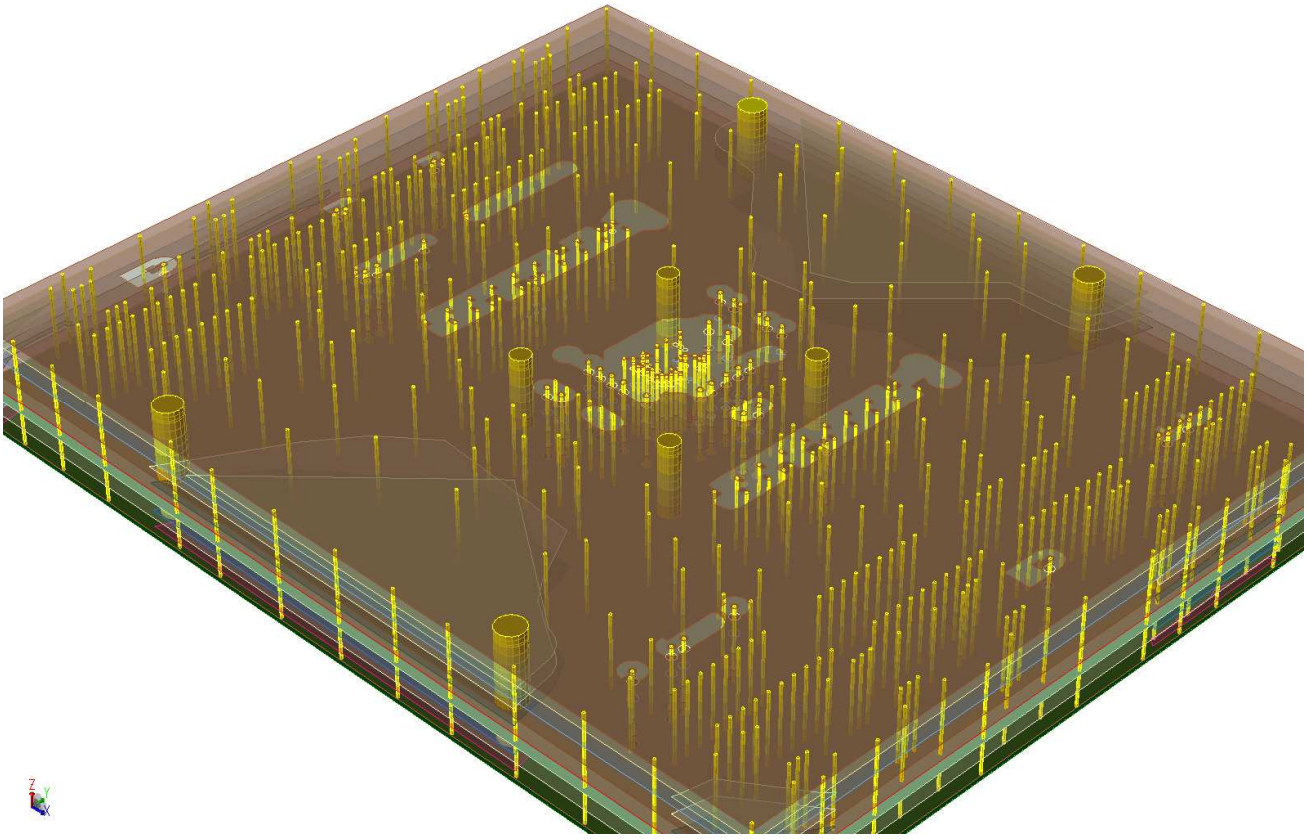


Figure 33 - 3D visualization of simplified supply structure of memory module board

The generation of an EM model for the board supply system is an order of magnitude more complicated. Without simplification and port grouping we need to create a single model with 477 pins for the nets B_VSS, B_VDDQ, B_VDD, VSS, VDDF and VDDQF formed by 13 finite plane structures littered with holes for the 833 through hole vias of the board of which 534 vias on supply nets. This complexity is not realistic for the 3D EM solver we have currently available. Therefore we simplified the port structure by grouping the B_VSS on the QT connectors in groups of 3 or 4 and keeping only a minimal number of other pins on the remaining devices. This reduced the number of pins to 169. Furthermore we removed all non-supply nets and closed all via holes in the finite planes without a supply via going through to reduce the mesh complexity. We modeled all the supply vias by a lumped model and the finite planes as planar sheets without edge mesh. Figure 3333 shows this simplified layout with just the supply shapes and supply vias remaining.

Even with these simplifications, the simulation remains challenging. Not only because of the problem size. In addition to that, the dynamics in the system are high because the decoupling capacitors cannot be included in the EM simulation. Only the latest development version of the EM solver, available at the time of this validation task, is capable to run a sweep between DC and 1GHz for about 25 frequencies of this design. The simulation system to solve has 140108 unknowns and it takes 11 hours to get to the first point and 1hour 20 minutes for the next frequencies on a 16-core Linux machine. The simulation needs 25 GB of memory. Although 25 frequency samples are not sufficient to provide a converged, fine resolution frequency model capturing all the resonances, this model was used as a first approximation for the board supply system.

The EM model does not include any of the decoupling capacitors on the board yet. To create a complete supply model, we performed an additional circuit level simulation with the decoupling capacitors attached to include them into the supply system model. The resulting simulation model has 127 pins and was sampled at every 50 MHz from DC to 1GHz. The resulting iml S-parameter model was provided for use in the Cadence SiP analysis platform.

Later in the validation process, we discovered that this supply model is not sufficiently dense sampled when going to DC. Figure 3434 illustrates clearly how at least one half turn in the S parameter plane is missing between the DC point and the 50 MHz for S11 of connector J23 pin A1. Many other S-parameters show similar sample issues and the available interpolation techniques don't have enough information to fill the missing data. We also ran into an issue on the high frequency side for transient simulations in the SiP platform. Here a physically consistent extension of the data is not easy to produce and brings the circuit simulator in problems.

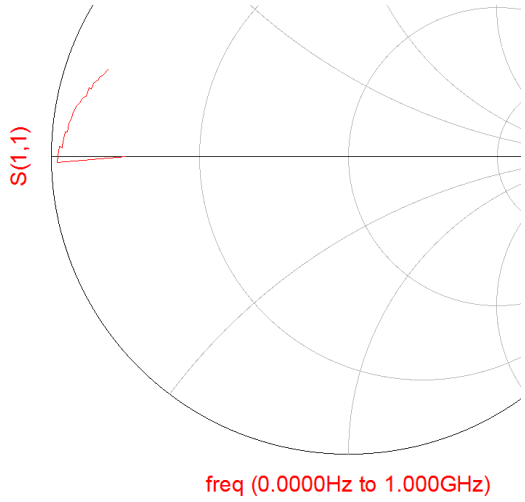


Figure 34 - S11 of connector J23 pin A1 of net B_VDDQ illustrates the missing low frequency sample problem

2.6.3EM model generation for the main test board design

The main test board for the SiP testing is again an 18 layer PCB board with impedance controlled striplines for all signal traces related to the SiP modele. This board is equipped with a large control FPGA and connectors for measurement and for mounting the memory module board with the SiP. This main board has a size of 120 mm x 150 mm and a complicated interconnect structure with nearly 3200 pins. We decided to perform simulations for this board with circuit level models for the stripline interconnections and assume the supply system was close to ideal. The only exception was the VDDQF supply net for the NOR device. This supply net is routed on the top and bottom layers of the main board as just one single trace without decoupling capacitors and we suspected EM related issues with this net. To verify we created an EM model for this trace between DC and 5GHz in a simplified board structure. We extracted the trace with a cookie cut of the top and bottom layer from the board and ignored all other nets. The inner layers 2 and 17 are both ground planes for net VSS which are considered ideal and are used as reference for the VDDQF supply trace ports.

A 3D visualization of this structure is shown in Figure 3535. The EM simulation indeed revealed a rather complicated behavior for this net. The simulation with 10434 unknowns needed 105 adaptive frequency points to converge. The simulation finished after 1hour 33 minutes on a 16-core Linux machine.

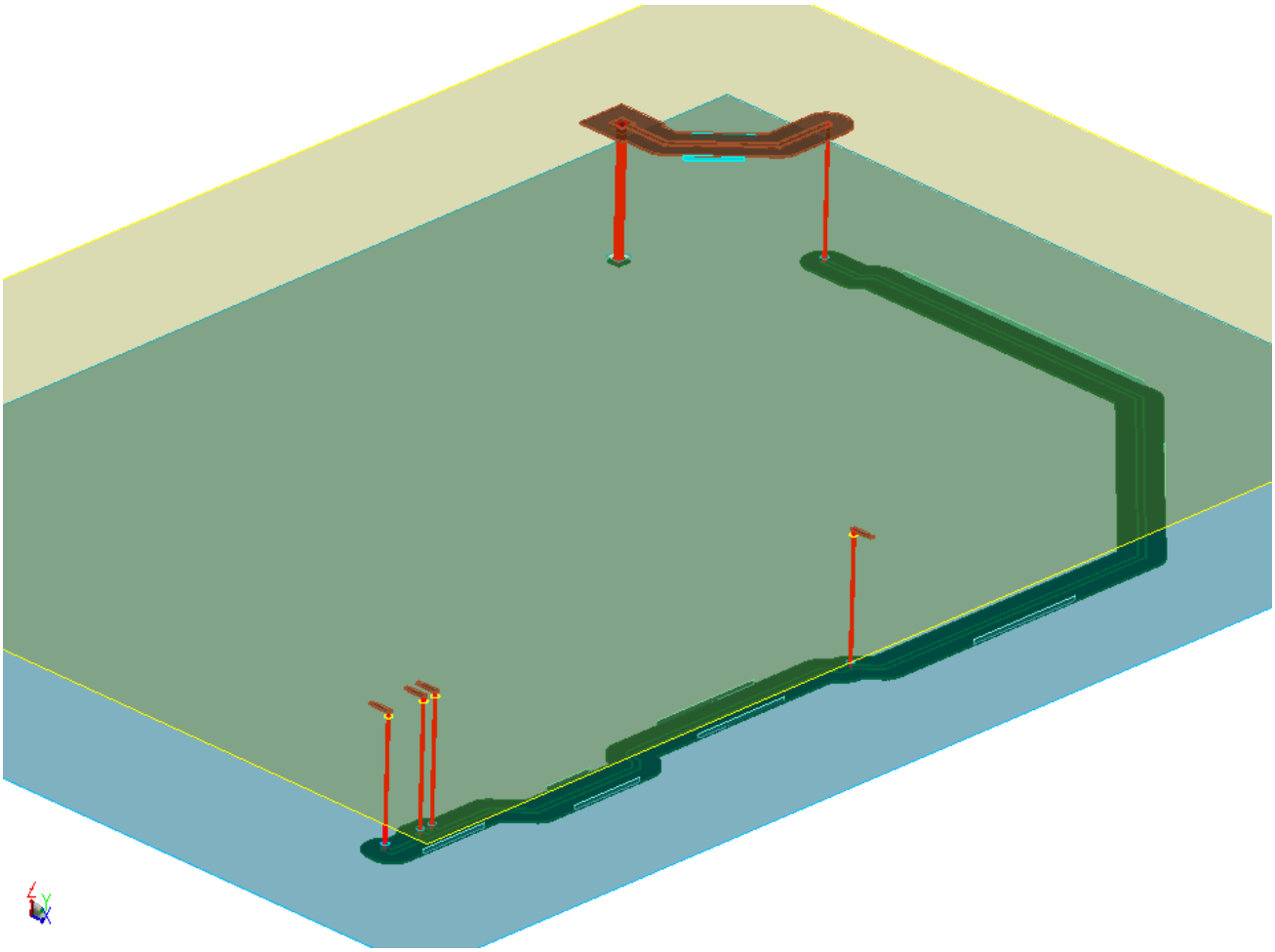


Figure 35 - simplified 3D view of the VDDQF net for EM simulation

Figure 3636 illustrates the complexity of the behavior of the VDDQF supply trace rather nicely. The start near -8 dB is due to the 5 port model with the pins of the net terminated at 50 Ohm. We see and the overall behavior of a transmission line with loss but with a large number of surplus resonances.

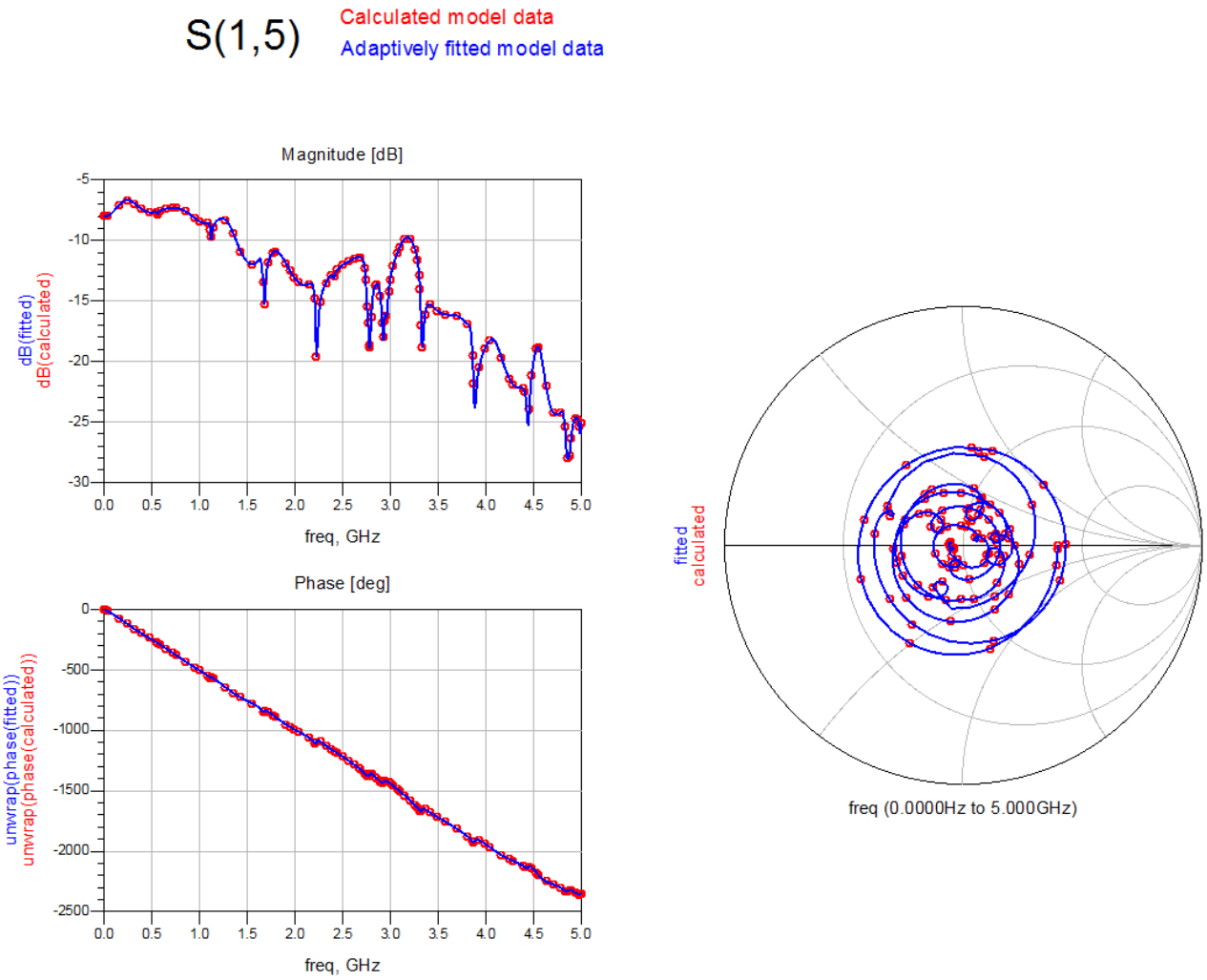


Figure 36 - S-parameter plot from the voltage regulator pin and the most distant pin of VDDQF from DC and 5 GHz

2.7Hand-off between Agilent and Cadence

2.7.1 Formats for the Model File Header

The supported header formats are S-Parameter, Spice and DML (Cadence propriatary device model language) Model Files.

- **S-Param**

  Two different header types are supported for S-Param files:

  1.

```
! ---------- Net List ----------
! NET062
! NET068
! ---------- Port List ----------
! Port 1 = U8-2
! Port 2 = U6-2
! Port 3 = U7-2
! Port 4 = U10-2
! ------------------------------
! GNDNET NET014
! NETSLIST NET029, NET012
```

```
! PCELLSLIST U1, U4, U6
```

2.

```
! GNDNET NET014
! NETSLIST NET029, NET019
! PCELLSLIST U3, U4
! Port 1 = U3_1 NET029
! Port 2 = U1_2 NET019
! Port 3 = U4_1 NET019
! Port 4 = U6_2 NET029
```

In the first header type, the ports and nets are not bound to each other. So an implicit binding is assumed. All nets and ports are traversed sequentially and first net is assumed to be connected to first 2 ports, second net is assumed to be connected to next 2 ports and so on. The last net is assumed to be connected to all the remaining ports.

In the second header type, the nets and ports are specifically bound to each other. No implicit assumptions are made in this case and only the explicit binding specified in the header is honored.

GNDNET, NETSLIST and PCELLSLIST are solver specific optional parmeters. GNDNET specifies the net to which all the ground pins in the model should be connected. NETSLIST is a comma separated list of nets which should be deleted from the schematic when the model gets assigned. PCELLSLIST is a comma separated list of refdes of PCELLS which should be deleted from the schematic when the model gets assigned.

- **Spice**

```
* GNDNET NET014
* NETSLIST TN-35
* PCELLSLIST U1, U3
* net TN-35
* port I2 'U1-11'
* port O2 'U2-7'
* net TN-33
* port I3 'U1-12'
* port O3 'U2-6'
```

In this header a net is specified on one line with the net keyword and all ports connected to this net are specified on the following lines with the port keyword. There is no implicit assumption in Spice headers. Everuthing has to be specified explicitly in the given format.

GNDNET, PCELLSLIST and NETSLIST have same meaning and format as in case of S-Param headers.

- **DML**

```
("2net.dml"
 (PackagedDevice
  (2net
   (ESpice ".subckt 2net P1_A10 D1_43 P1_A11 D1_44
* ------------------------------
* net SIG_D1.43_TO_P1.A10
* port O214 = P1-A10
* port I214 = D1-43
* net SIG_D1.44_TO_P1.A11
* port O215 = P1-A11
* port I215 = D1-44
```

```
* GNDNET net6
* NETSLIST TN-35
* PCELLSLIST U1, U3
") ) ) )
("9net.dml"
 (PackagedDevice
  (9net
   (ESpice ".subckt 9net P1_D8 D1_23 D1_250 P1_AC36 D1_257 P1_AB32
P1_AG31 D1_289 D1_337 P1_AI22 D1_370 P1_AJ15 D1_434 P1_AF4 P1_A10
D1_43 P1_A11 D1_44
* ------------------------------
* GNDNET net14
* PCELLSLIST U1, U3
* NETSLIST net1
* net SIG_D1.23_TO_P1.D8
* port O248 = P1-D8
* port I248 = D1-23
* net SIG_D1.250_TO_P1.AC36
* port I82 = D1-250
* port O82 = P1-AC36
* net SIG_D1.257_TO_P1.AB32
* port I87 = D1-257
* port O87 = P1-AB32
* net SIG_D1.289_TO_P1.AG31
* port O111 = P1-AG31
* port I111 = D1-289
* net SIG_D1.337_TO_P1.AI22
* port I169 = D1-337
* port O169 = P1-AI22
* net SIG_D1.370_TO_P1.AJ15
* port I238 = D1-370
* port O238 = P1-AJ15
* net SIG_D1.434_TO_P1.AF4
* port I361 = D1-434
* port O361 = P1-AF4
* net SIG_D1.43_TO_P1.A10
* port O214 = P1-A10
* port I214 = D1-43
* net SIG_D1.44_TO_P1.A11
* port O215 = P1-A11
* port I215 = D1-44
* ------------------------------
") ) ) )
```

A DML file is a collection of Spice Models. The format of each model in a DML file is same as that of a model in a Spice file. The only difference is in the way the parentheses are used to bundle multiple models together.

Model Backannotation Mechanism

With the circuit extraction performed in the Agilent environment, Package PI will not invoke user selected field solver to extract equivalent circuit for selected power nets and coupled ground nets, wirebond, bump and ball pins, vias, fanout of decaps, and so on. The equivalent circuit extracted needs be stored as DML or/and Spice format in PI working directory by default. User can also change it to store in another location for later use. S-parameter format can also be supported. It should be pointed out that the center frequency of narrow band modeling is set in the Frequency field of parameter form in Figure 37.

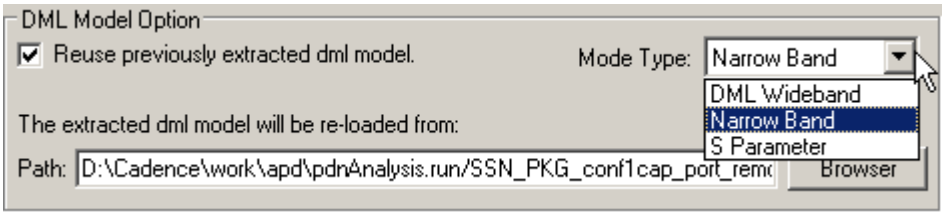


Figure 37: Confirmation Report for the Reuse Option

Now Package PI will concentrate to connect equivalent circuit with various elements, such as VRM models, board and chip power supply circuits, decap models, die current profiles and sink excitations into a whole TLSim circuit. The ESpice circuit used for TLSim simulation will be also exported and saved in power integrity working directory pdnAnalysis.run.
Once the TLSim circuit is build correctly, Package PI will pass it to TLSim engine for time-domain or frequency-domain simulation, and output the result as SigWave waveform. The target impedance value and voltage ripple will be also displayed with analysis result in SigWave for reference. If the provide equivalent circuit does not match the power network selected, an error message will be given (Figure 38).

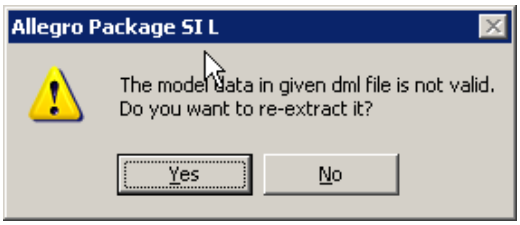


Figure 38: Confirmation Report for the Reuse Option

3User Interface

3.1 Menu

The package PI flow can be invoked via the following menu item:
Analyze➔Power Integrity…
The main window for package PI solution is invoked as Figure 39:

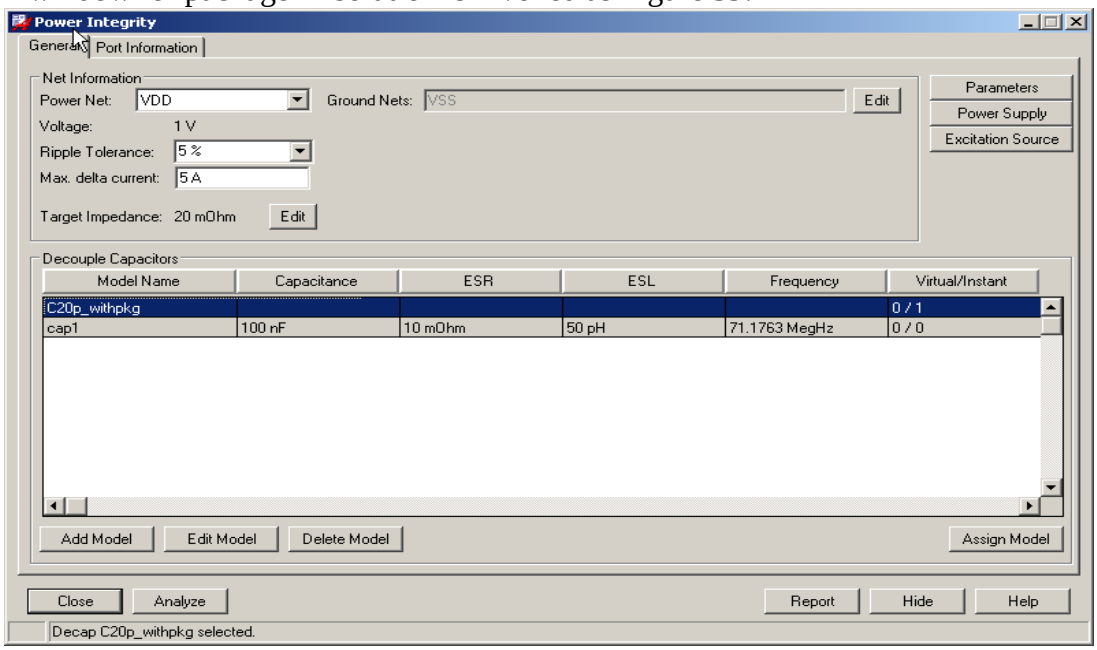


Figure 39: Package PI Main Window

Parameters Invoke dialog to set up common parameters for field solver and 3-D modeling.
Power Supply Invoke dialog to edit VRM and board power supply subcircuit for co-design.
Excitation Source Invoke dialog to manage and edit all excitation sources used in design.
Analyze Perform time or frequency-domain analysis for selected power net.
Assign Model Perform the signal model assignments.
Report Review and export decoupling capacitors used in design for selected or all power nets.
Hide Hide main form manually. PI will hide and restore main form automatically for various operations.
Close Close the form and quit PI flow.

3.2 Power/Ground Net Information

As the first step, user should configure the power and ground net information for analysis. It is user's responsibility to identify the power and ground nets with right voltages via the following menu item before analysis: **Logic ➔ Identify DC Nets …**

In this section, user can perform actions on the following item in main window as Figure 39.

Power Net All power nets in design will be listed in drop down list, and user can select any one for later analysis.

Ground Nets By default, all ground nets associated with selected power net via decoupling capacitors will be listed here. User can click "**Edit**" button to invoke the ground net list editor form to add into or delete them from list. These ground nets will be used to identify which net a pin of decoupling capacitor connects to when it is placed into design. **Note:** The field solver should determine which nets are used as reference automatically.

Voltage Display the voltage value for selected power net.

Ripple Tolerance The maximum voltage drop or spike noise that the design can tolerate (expressed as a percentage of voltage).

Max. Delta Current The worst-case dynamic current that the power net will potentially suffer. This value will be replaced by the current (noises) from various die pins if have.

Target Impedance Display the target impedance the Package PI computed based on the supply voltage, tolerable ripple, and the worst-case dynamic current user specified. User can click "**Edit**" button to review and modify the parameters for target impedance.

3.3 Ground Net List Editor

When user places the virtual or instant decoupling capacitors into the design, he needs to specify which ground net the pin of decoupling capacitors connects to, otherwise, the direct connection to BGA or die pin will be used for simulation. By default, all ground nets associated with selected power net via existing decoupling capacitors in design will be taken into consideration automatically. User can remove items from this list or add other ground nets into this list manually.
User can review and modify the ground net list in this form as figure 40.

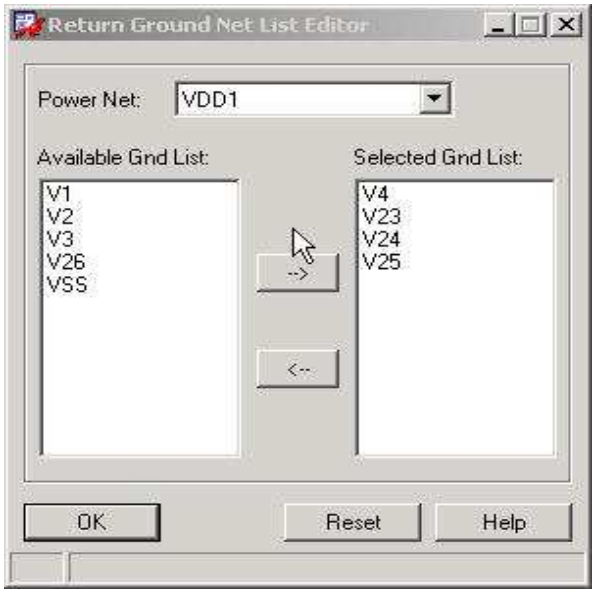


Figure 40: Ground Net List Editor Form

Here are the detail items in this form:
Power Net The power net selected for analysis.
Available Gnd List All ground nets available for selection in design. Double click this list will move the selected item into the selected list.
Selected Gnd List All ground nets selected for power net in design. Double click this list will move the selected item into the available list.
➔ Move select ground nets in available list to selected list.
➔ Remove selected ground nets from selected list.
OK Close the form.
Reset Reset to default list for selected power net. All ground nets associated with selected power net via existing decoupling capacitors in design will be taken into consideration as default automatically.

3.4 Target Impedance

The key parameter in a power deliver system is the target impedance. The power deliver network must deliver current at or near the target impedance at all frequencies from DC to the highest frequency of concern (often well into the microwave bands). The target impedance **Ztarget** is defined as the following formula:

$$Z_{target} = \frac{(\text{Power Supply Voltage}) \text{ X } (\text{Ripple Tolerance})}{\text{Dynamic Current}}$$

User can review and modify these parameters to define the target impedance curve at concerned frequency range as figure 41.

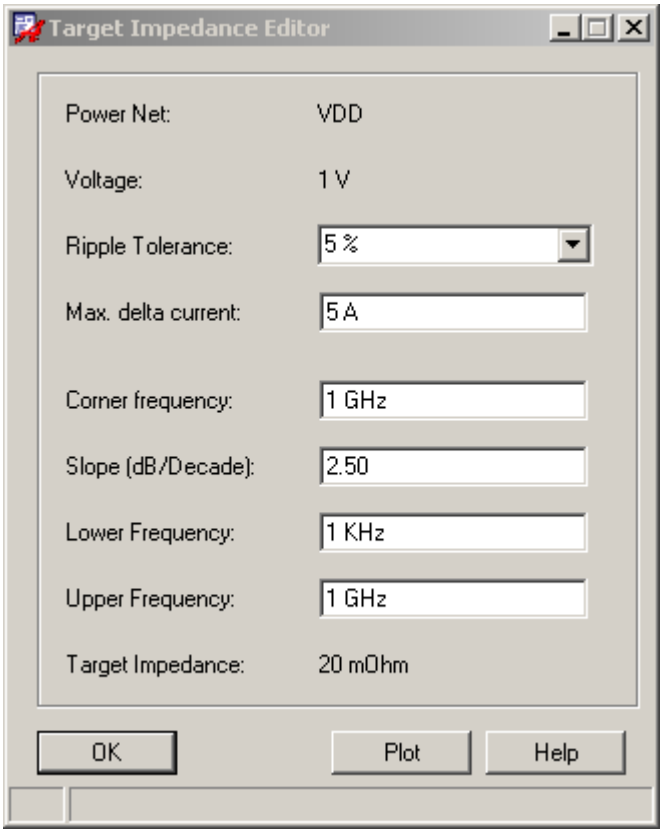


Figure 41: Target Impedance Editor Form

Here are the detail items for Target Impedance parameters:
Power Net The power net selected for analysis.
Voltage The supplied voltage from selected power net.
Ripple Tolerance The maximum voltage drop or spike noise that the design can tolerate (expressed as a percentage of voltage).
Max. Delta Current The worst-case dynamic current that the power net will potentially suffer. This value will be replaced by the current (noises) from various die pins if have.
Corner Frequency The frequency up to which the target impedance is constant.
Slope (Db/Decade) The ramp-up of target impedance after the corner frequency.
Lower Frequency The lower frequency range for analysis.
Upper Frequency The upper frequency range for analysis.
Target Impedance Display the target impedance the Package PI computed based on the supply voltage, tolerable ripple, and the worst-case dynamic current user specified.
Plot Generate a plot of the target impedance profile and display it in SigWave tool.
OK Close the form.

3.5 Power Supply

The co-design flow for power integrity is to deliver the power from VRMs to PCB Board, and then to Package and Die ultimately. VRMs act as supply points from which the power is delivered and regulated, and the PCB supply equivalent subcircuit acts as the transport line to deliver the power supply to die.

3.6 VRM Module

A voltage regulator module (VRM) converts one DC voltage to another DC voltage. The VRM uses a reference voltage and feedback loop to sense the voltage near the load, then adjusts the current accordingly.

User can create new VRM model or browser existing model from design. Before the analysis, one VRM can be provided to connect to package, but it is not required to place actual VRM in package design, Package PI will connect the VRMs to package via package pins automatically. Only in special case the users want to analyze the response from the noises only, they then can not provide VRM module and ignore it.

By default, there is no VRM provided for Package PI flow.

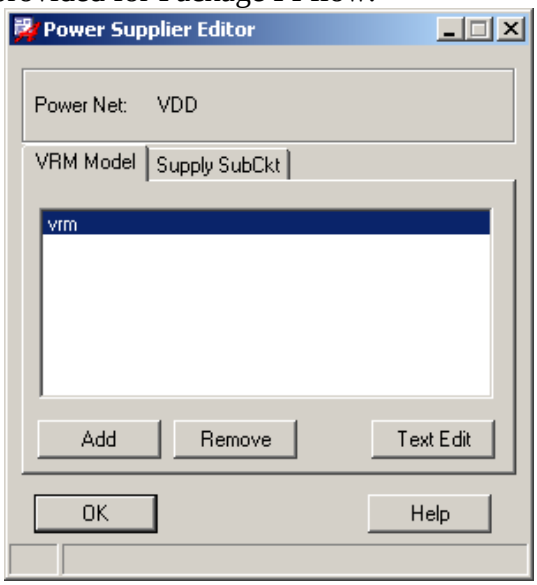


Figure 42: Power Supply VRM Model Form

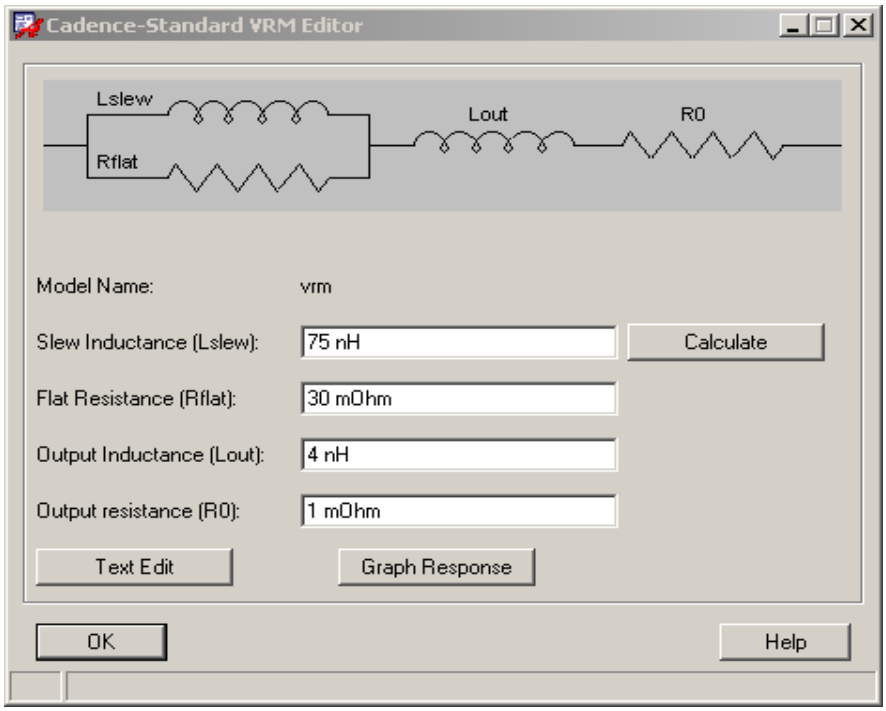


Figure 43: Power Supply VRM Module Editor Form

PI models the behavior of the VRM as a four-element SPICE model, and provides a default VRM model. Users can create new VRM models as four-element SPICE models, and also can load user-defined, multi-phase VRMs, as well as those provided by Cadence.
Here are the detail items for VRM module of power supply editor form as figure 43:
Power Supplier For net Specify the selected power net.
Voltage Specify the voltage value for power supply.
VRM Model Name All VRM models current used to supply power are listed in the list field. And the VRM model currently edited is also displayed.
Add Create a new VRM model or select an existing VRM model from standard model browser form into list.
Remove Remove a VRM from current used list.
Text Edit Bring up a text editor to edit the selected VRM model.
Graph Response See the impedance curve resulting from the configuration of the VRM. PI simulates the VRM and displays the results in SigWave.
Slew Inductance (Lslew) Rate at which the VRM can react to changes in current. For example, a VRM may take 15 microseconds to slew the current from 8- to 20- amps.
Flat Resistance (Rflat) Equivalent series resistance of the capacitor that is associated with the VRM.
Output Inductance (Lout) Cable or pin parasitic inductance of connecting the VRM to the board.
Output Resistance (R0) Sense resistance between the VRM and the load.
Calculate Bring up the VRM input inductance calculation form.

3.7 Power Supplier Subcircuit

The power supplier subcircuit acts as transportation network to deliver the power from VRM modules to package. Users can extract the power supplier subcircuit by measurement tools ot thru analysis. The VRM is concatenated with supply circuit, and then connects to package model on BGA pins. Any inconsistent nodes on board subcircuit model with package model will be shorted to other port.
The package PI provides the capabilities to concatenate the external subcircuit for board power delivery. Today, it is user's responsibility to provide such subcircuit to Package PI. Package PI will ignore it and continue if no such subcircuit available.
Notes: In future new PCB PI flow, we will provide function to extract such subcircuit for power delivery. For now, user can create one in manually, or modified the tlsim subcircuit stored in current PI simulation.
The power supplier subcircuit consists of two separate elements: the subcircuit definition itself and the pin mapping file. After the separate subcircuit file and the pin mapping file are loaded, user need to specify the mapping from package pins to subcircuit ports. PI will try to match them automatically based on the component name and pin number.

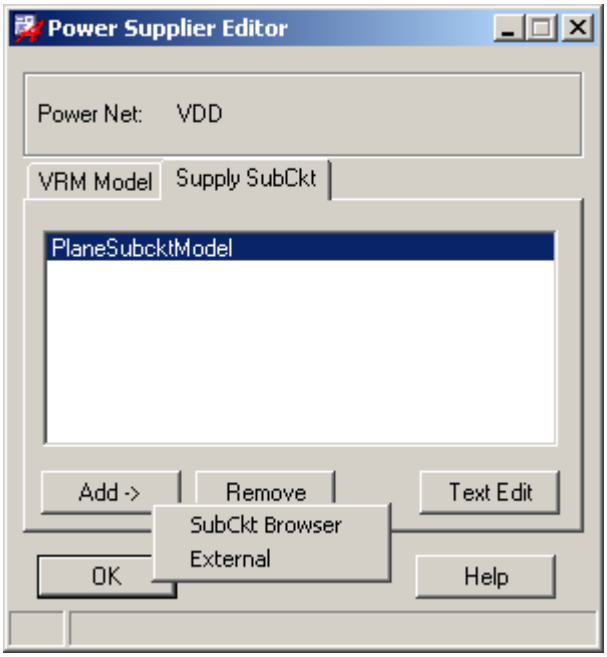


Figure 44: Power Supply Board Module Editor Form

Here are the detail items for power supplier subcircuit editor form as figure 44 by clicking "SubCkt Browser" button from Dml Model Browser. At the same time, the subcircuit can also be obtained from external file through "External" button.

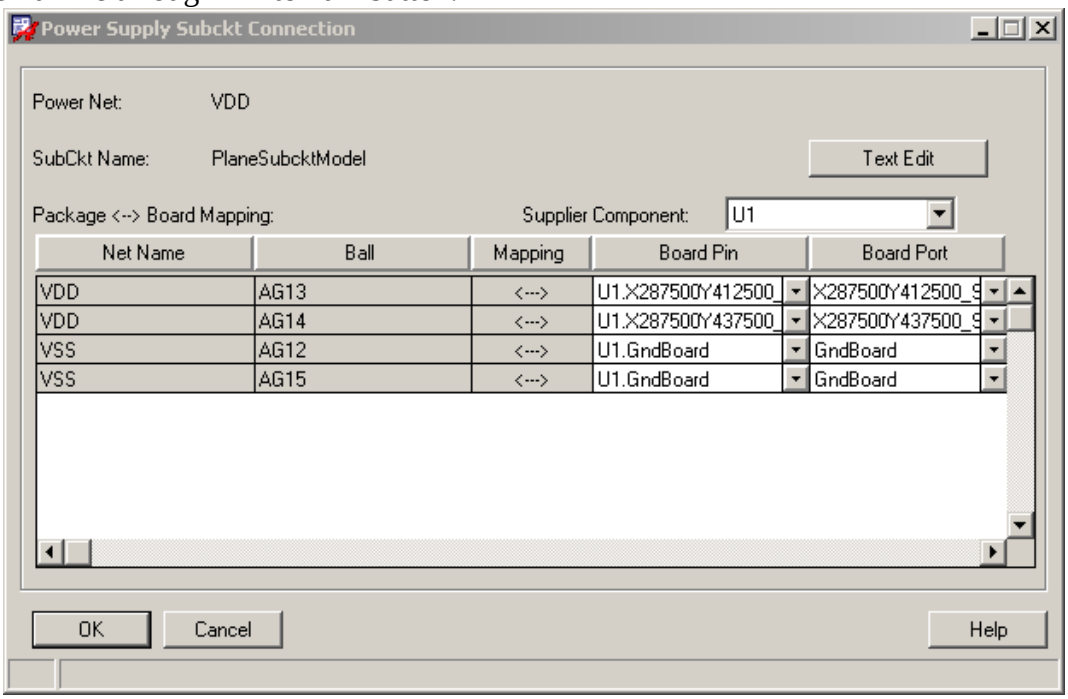


Figure 45: Power Supplier Board Subcircuit Connection Form

Power Net Specify the selected power net.
Subckt Name All available subcircuits have been loaded into current design are listed in the drop-down field. User can select one to deliver power to package for selected power net.
SubCkt Browser Load external subcircuit definition file and pin mapping file into design.
Text Edit Bring up a text editor to edit selected subcircuit.
Supplier Component Optional information to specify where the subcircuit comes from.

Package ←→ Board Mapping User can use this grid to match package pins to board pins and then to subcircuit ports.

3.8 Current Excitation/Noise Source

The co-design flow for power integrity is to sink current from boards to packages, and then to dies. The sink current acts as the excitation sources and noise sources for package power integrity impedance and voltage ripple analysis. The excitation source can be constant current, Gaussian pulse, train pulse, switching current profile for IC, or other format sources in future.
All excitation sources will be managed and edited in excitation source form as figure 46, 47 and 48. These excitation sources can be referred as die current profile and pin sink current later. Only constant, Gaussian pulse, train pulse and current profile are currently supported by PI.
Import User can import excitation sources from previously stored ASCII text file.
Export User can export all excitation sources into an ASCII text file for later use.

3.8.1Gaussian Pulse Source

All Gaussian pulse sources will be listed and editor in this form as figure 46.

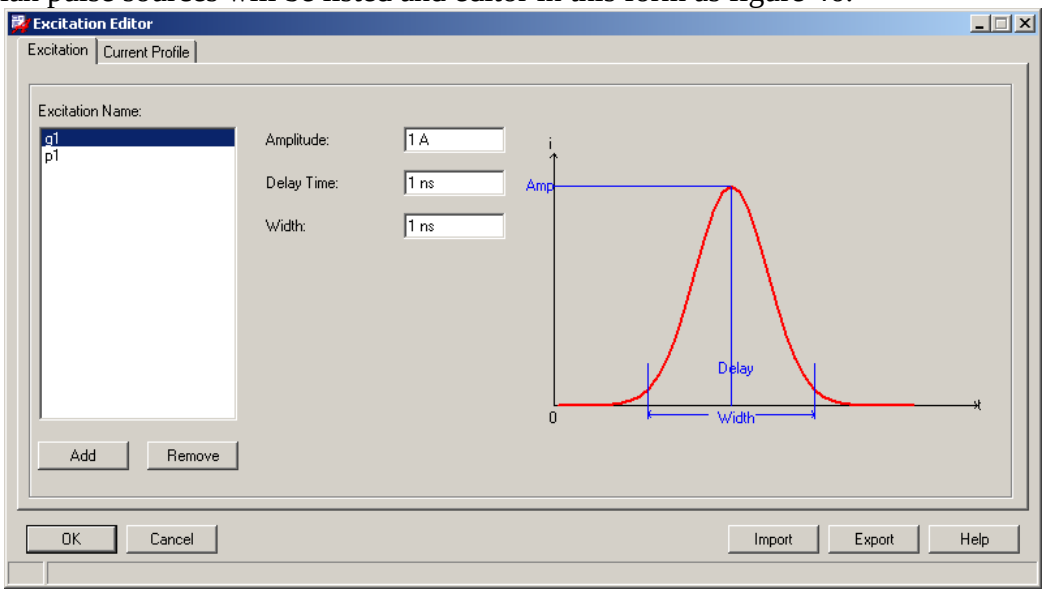


Figure 46: Gaussian Pulse Excitation Source Editor Form

Here are the detail items for Gaussian pulse excitation source editor form:
Excitation Name All available Gaussian pulse excitations are listed in the list field. And the excitation current edited is also displayed.
Add Create a new Gaussian pulse excitation and add it into the list for edition.
Remove Remove an excitation from the list.
Amplitude Gaussian pulse amplitude value.
Delay Time Gaussian pulse delay time.
Width Gaussian pulse width.
The curve for selected Gaussian pulse is also displayed with the given parameters.

3.8.2 Pulse Source

All pulse sources will be listed and editor in this form as figure 47.

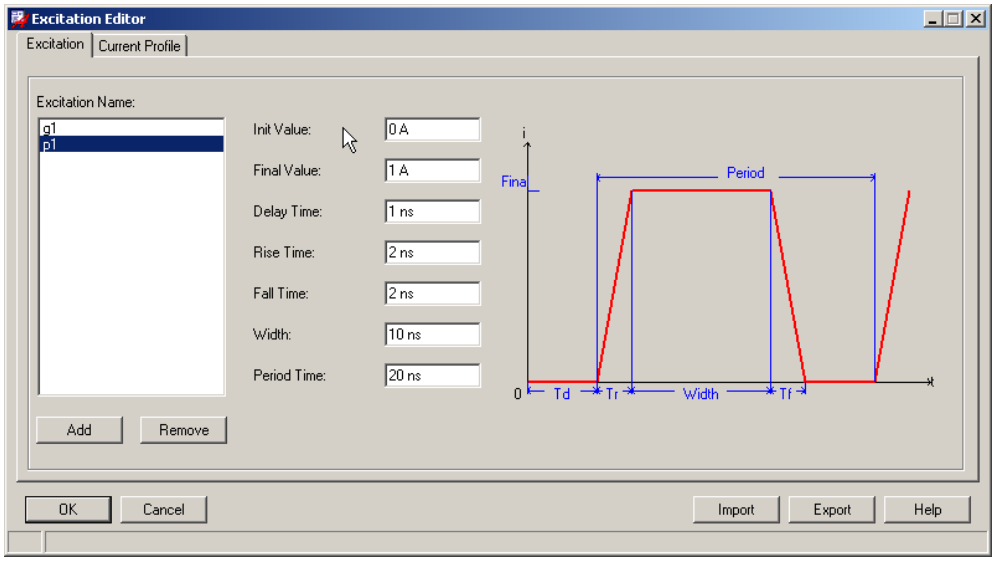


Figure 47: Pulse Excitation Source Editor Form

Here are the detail items for train pulse excitation source editor form:
Excitation Name All available pulse excitations are listed in the list field. And the excitation current edited is also displayed.
Add Create a new pulse excitation and add it into the list for edition.
Remove Remove an excitation from the list.
Init Value The initial value for pulse.
Final Value The amplitude value for pulse.
Delay Time pulse delay time.
Rise/Fall Time pulse rise/fall time.
Width pulse width.
Period pulse period time.
The curve for selected pulse is also displayed with the given parameters.

3.8.3 Import Current Profile

All current profiles from ICs will be listed and editor in this form as figure 48.

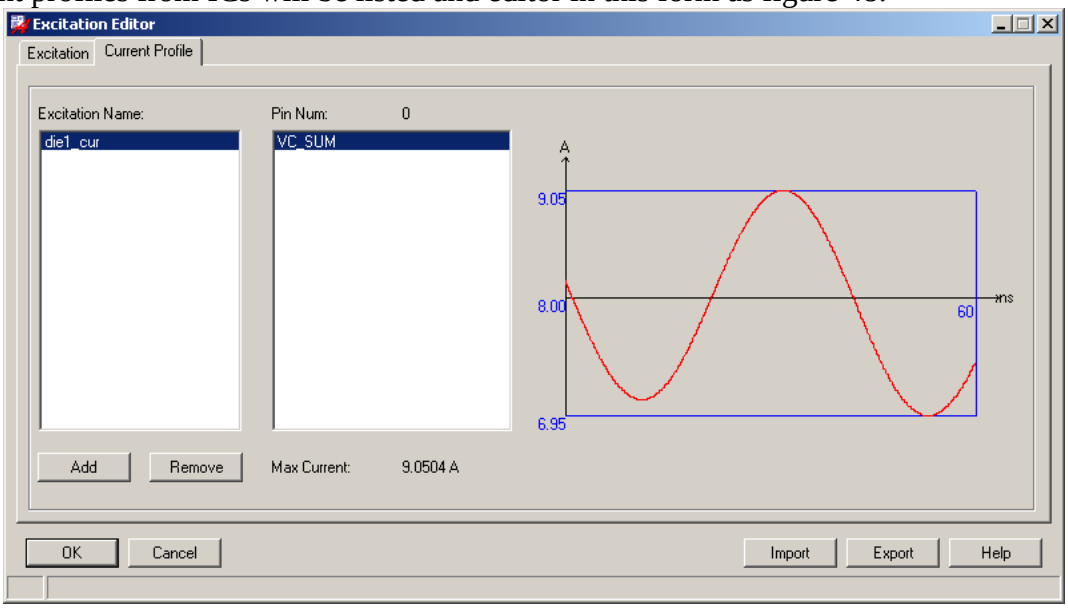


Figure 48: Switching Current Profile Excitation Source Editor Form

Here are the detail items for current profile excitation source editor form:
Excitation Name All available current profile excitations are listed in the list field. And the excitation current edited is also displayed.
Add Load a new current profile excitation from external and add it into the list for edition. This file can be derived from VoltageStorm or IC manufacturer.
Remove Remove an excitation from the list.
Pin Num Display total pin number for selected current profile.
Pin List All pins with sink current in current profile will be listed for selection. User can select pins to display the curves and their maximum current value.
Max Current The maximum current value for selected pins in all time.
The curves for all selected pins are also displayed with the given parameters.

3.9 Power and ground rail network (On-Die Information)

Before extraction and analysis, users should configure the corresponding on-die information, including the current profile, series capacitance and resistance, or subcircuit, these information normally are provided by IC manufacturer or IC simulation tool.
Here are the detail parameters user can edit as figure 49:
Filter Component name filter pattern.
Select All Select all components in the list for later operations.
Port Group Assign pin group information for selected components. Refer to the later section for more detail.
Component List All dies and package components connected to selected power net will be listed in this list.

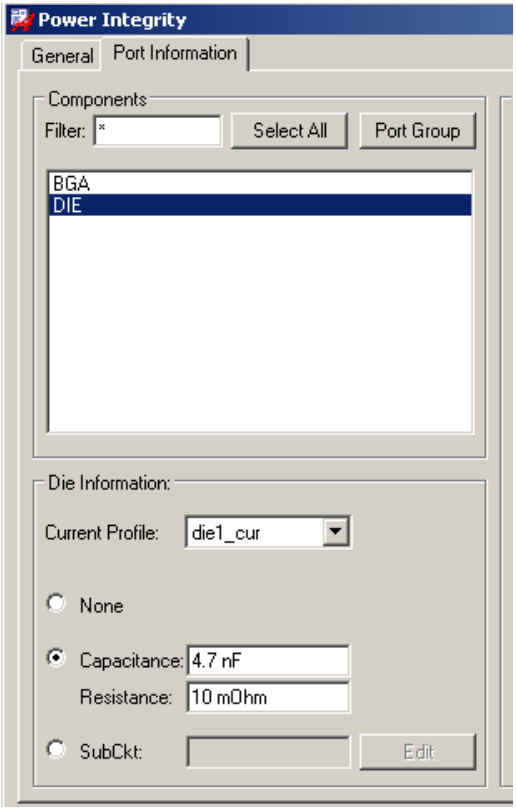


Figure 49: On-Die information

Current Profile Switching current profile from IC.

None No On-die subckt information.
Capacitance On-die seres capacitance value.
Resistance On-die series resistance value. The on-die series capacitance and resistance can acts as simplified die circuit. For more complicated user-defined subcircuit, user can import it through below field.
Subckt an ESpice chip subcircuit model. User can use this field to import more complicated user-defined subcircuit.
Edit Edit ESpice chip subcircuit model.
A Spice subcircuit model from chip can be used to model the die on selected power net. This chip subcircuit is extracted by IC manufacturer or IC analysis tools.
The chip subcircuit consists of two separate elements: the subcircuit definition itself and the pin mapping file. After the separate subcircuit file and the pin mapping file are loaded, users need to specify the mapping from die pins to chip ports. PI will try to match them automatically based on the pin, pad and port name.
Here are the detail items for chip subcircuit editor form as figure 50, which is similar to the board subcircuit connection:

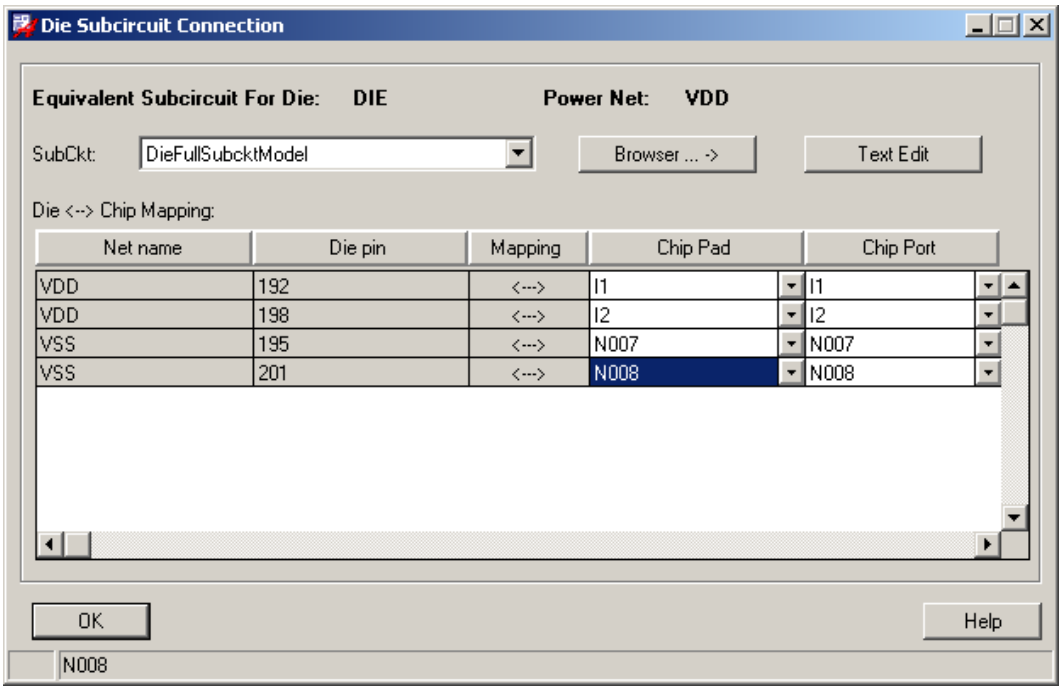


Figure 50: Chip Subcircuit Editor Form

Chip Subcircuit For Die Display the selected die.
Power Net: Display the power net name.
SubCkt The chip subcircuit name from die. All available chip subcircuits have been loaded into current design are listed in the drop-down field.
Browser…> Load external subcircuit definition file and pin mapping file into design.
Text Edit Bring up a text editor to edit selected subcircuit.
Die ←→ Chip Mapping User can use this grid to match die pins to chip pins and then to chip ports.

3.10 Port Information

Before analysis, user need to specify the package and die pin port type, excitation current and group information in figure 51. In package PI, the port type and group defined through 3-D Modeling will be overwritten by the settings in Port Group form as figure 51.

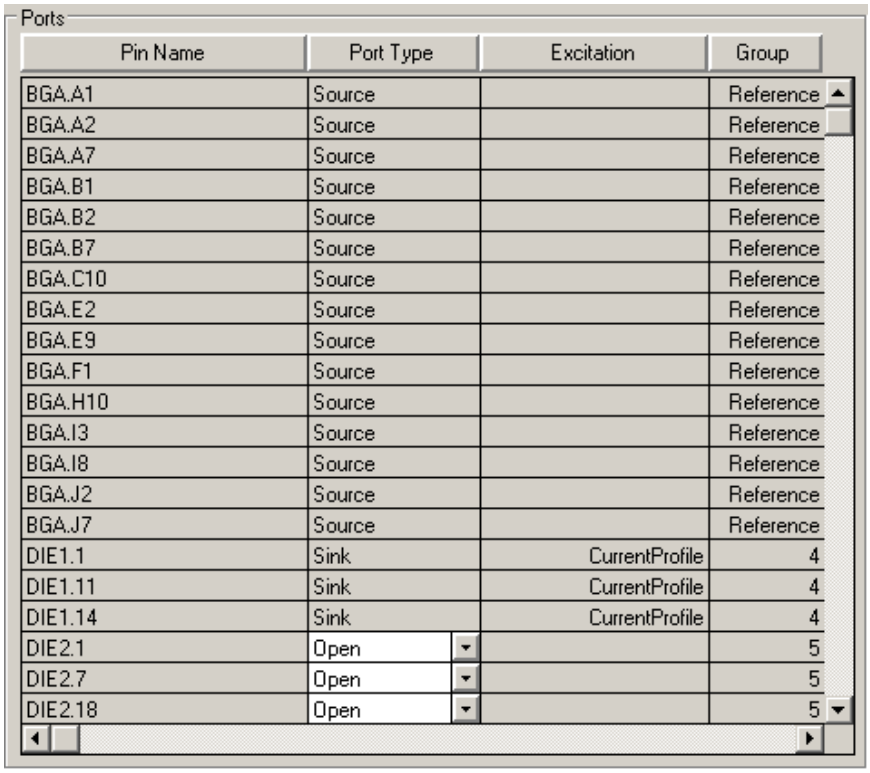


Figure 51: Assign package and die pin port information

Note: In figure 51, the status of port type field for die pins is incorrect and can be editable.
All package and die pins connected to the selected power net will be listed here. In PI, the port type for all of the BGA pins are set as Source type automatically and un-editable. If the excitation is from on-die current profile, then the port type and excitation can not be changed. If the port type is Open, then the port will not be extracted by any quasi-static solver. For example, the extracted dml model will not have the pins for DIE2 as shown in figure 51.
You can sort, search, or manipulate data in the columns of the port grid using right mouse button. The available options vary from the column header you right-click on.

3.10.1 Port type

The port types for pins can be one of open, sink and source. All package pins are forced to be source pins and user can not change it. All die pins are considered to be sink pins by default. User can change it to source if necessary, especially in SiP case, some die pins act as source to provide voltage. If the sink excitation current of sink pins are zero, then they actually acts as open type.

3.10.2 Port excitation

In additional to assign switching current profile on die, users can also specify the constant, Gaussian or train pulse excitation for each sink pin directly. If a die has been assigned with a current profile, all pins of this die can read excitation current from this die current file automatically and the excitation field will be marked as “From Component”.
All Gaussian and train pulse excitation sources are listed in drop-down list and user can select from the list or assign constant current for pins directly.
A warning message will be prompted once the total current (noise) from various die pins is exceeding the pre-defined worst-case dynamic current.

3.10.3 Import/export of port configurations

The port information including the pin name, port type, port group and excitation source can be imported and exported from external files.

3.10.4 Port Group

In order to improve the extraction and simulation performance, users need to group the sink pins and source pins on package and die as a Multi-port net. Port grouping gives user the capability of setting up a partition-based extraction by enclosing ports of source and sink pins in a specified portion of your design. This eliminates the limitation of having to extract the entire design with each pin identified. User can group the sink and source pin in below figure 52.

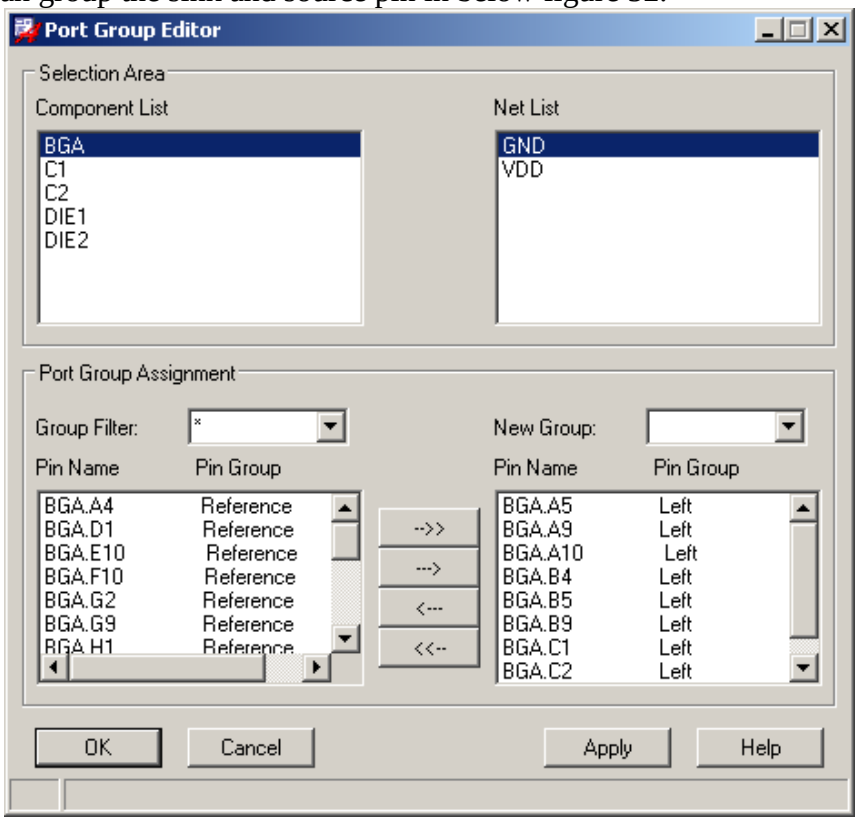


Figure 52: Sink and Source Pin Group Editor Form

Here are the detail items in this form.
Component List All pins belong to selected components in this list will be considered to be grouped.
Net List All pins connected to selected nets in this list will be considered to be grouped.
Group Filter Pin group name filter pattern on available list.
Available List All pins belong to selected components and connected to selected nets and those names match the filter pattern will be listed here for later selection and group. Double-click this list will move selected item into selected list.
Selected List All pins selected are moved from available list and listed here for new grouping. Double-click this list will remove the selected pin from this list.
New Group Assign new group name for selected pins.
All → Select all pins in available list for new group name.
← Remove pins in selected list from new group name.
→ Select pins in available list for new group name.
← **All** Remove all pins in selected list from new group name.

Apply Make pin grouping effective immediately.
OK Accept all pin grouping information and close the form.
Cancel Discard all pin grouping information and close the form.
Users can select sink and source pins in canvas directly by rectangle in mouse and then click left mouse button. All pins users selected will be moved from available list into the selected list for new grouping process.

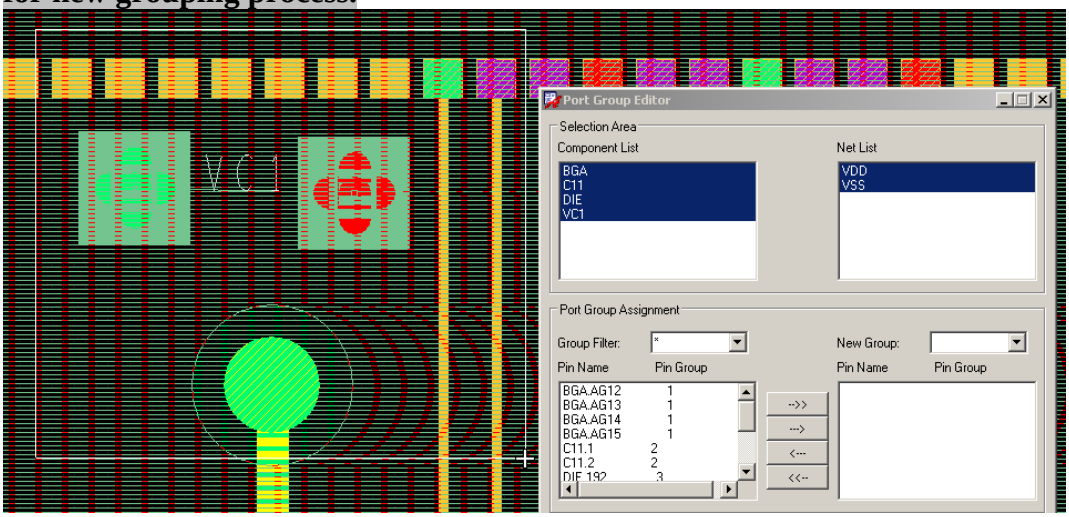


Figure 53: Port Group in Allegro Canvas

3.11 Decoupling Capacitor Information

PI accurately models the VRM, decoupling capacitors, system powers and reference nets to determine the impedance of the power delivery system, and uses SigWave to present the curves to describe the impedance as a function of frequency or voltage ripple as function of time. Any place where the power deliver system impedance or voltage ripple exceeds the target impedance or voltage ripple can be corrected by placing decoupling capacitors whose resonant frequencies effectively lower the system impedance to within the allowable target impedance or voltage ripple. What user does is to place selected decaps, change dc-net routing, re-extract model and see the impedance and voltage ripple fit.
The decoupling capacitor information contains a worksheet with corresponding parameters for analysis as figure 54.

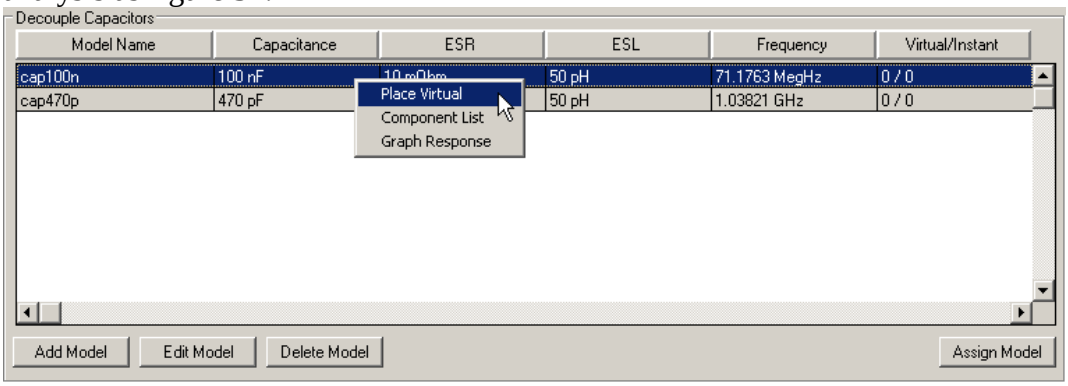


Figure 54: Decoupling Capacitor Worksheet

When you select any row in the worksheet and right-click, the context popup menu lets you choose among different operations as figure 54.
Place Virtual Place virtual decoupling capacitors with selected signal model and other parameters.
Component List Display a text report containing all device components found on a board with associated locations for selected model.

Graph Response Generate single cap response waveform.
Add Model Create new or select an existing model via model browser and add it into the worksheet.
Edit Model Edit parameters for selected model.
Delete Model Delete selected model from worksheet. All virtual and instant decoupling capacitors placed for selected power net will be removed also.
By default, there will have no decap model available for any selected power net. User need click "Add Model" button to add or browse specific decap model for selected power net

3.11.1 Decap Model Selection

User can create new decap model or browse an existing model via model browser and add it into worksheet as figure 55. User can also import models from Allegro part library directly.

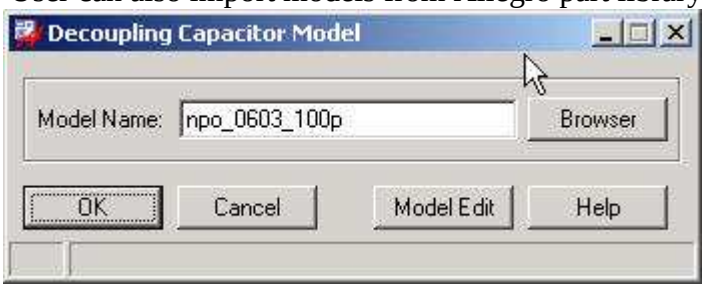


Figure 55: Decap Model Selection

Model Name The decap model name to be added into worksheet.
Browser User can click this button to invoke model browser to select an existing model. User can also import model from Allegro part library directly.
Model Edit User can invoke model editor form to change model parameters.
Cancel Discard model selection and close form.
OK accept model selection, add it into worksheet and close form.
When a new name is entered into this field and click **OK** button, a new decap model with default parameters will be created and stored into default dml model files **devices.dml**.

3.11.2 Decap Model Edit

User can edit decap model (ESpice and S-Parameter) as figure 56.

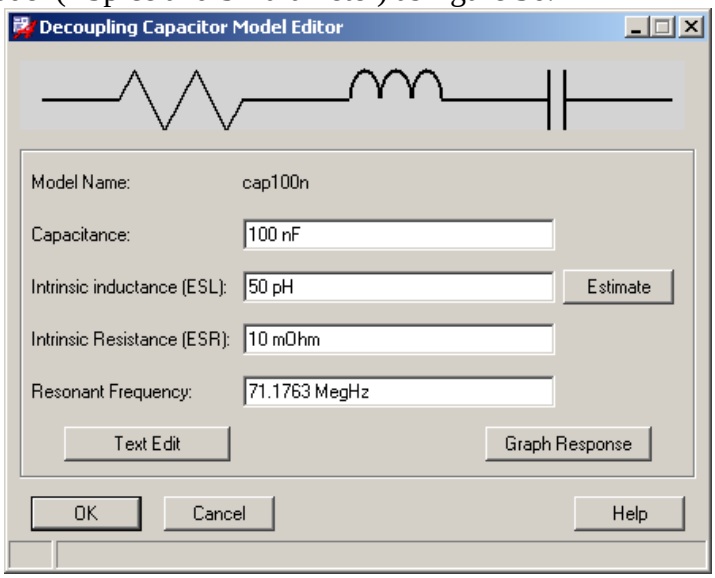


Figure 56: Decoupling Capacitor Model Edit Form

Model Name The decap model to be edited.
Capacitance The nominal capacitance value specified in the decap model. User can leave it blank or enter an estimated value if the capacitance for some complex decap model is not available, such as n-terminal and S-parameter model.
Intrinsic Inductance (ESL) Estimated intrinsic inductance of a surface mounted capacitor computed from its height parameters. Intrinsic inductance computations do not account for the capacitor's mounting characteristics. User can leave it blank or enter an estimated value if the capacitance for some complex decap model is not available, such as n-terminal and S-parameter model.
Estimate User can experiment with different capacitor thickness setting.
Intrinsic Resistance (ESR) Impedance value at resonance for decapl model. User can leave it blank or enter an estimated value if the capacitance for some complex decap model is not available, such as n-terminal and S-parameter model.
Resonant Frequency Computed resonant frequency based on capacitance and intrinsic inductance value for decap model. User can leave it blank or enter an estimated value if the capacitance for some complex decap model is not available, such as n-terminal and S-parameter model. For S-param model, the resonant frequency point can be extracted out at the lowest value for S11 or S22. It has the same frequency point for the S21/S12 for the highest value.
Graph Response Generate a single capacitor response wave and display it in SigWave.
Text Edit Edit the selected decap model via ASCII editor.
OK Accept modification and close form. The decap model will be stored in default dml files, "devices.dml".
Cancel Discard modification and close form.

3.12 Canvas Operation

PI will provide context-sensitive popup menu for user during various actions. The user can do the operations on the VDecap for decoupling capacitor and VPort for probe. User can do some operations on the pins of virtual decap and probe port in canvas on power/ground net.
Here are some menus available for various contexts:

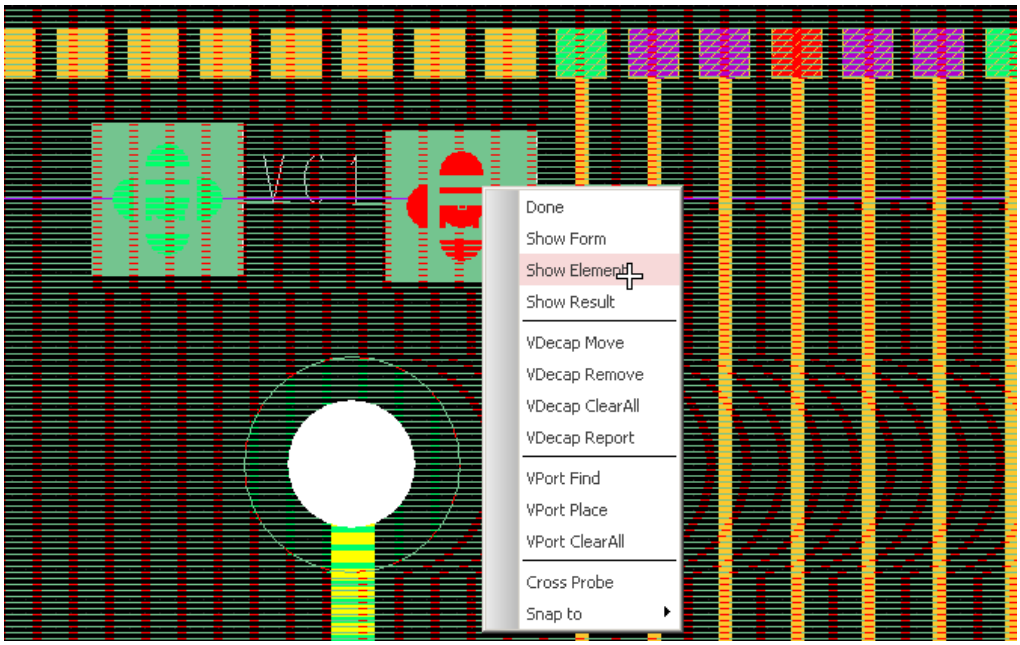


Figure 57: Menu for Right Click Button on One Vdecap in Allegro Canvas

Show Form This command can invoke the hid main form.
Show Element User can show the detail information for picked element as regular "**show element**" command.
Show Result User can show the analyzed result by opening the analyzed .sim SigWave file.
VDecap Move User can move the placed virtual decoupling capacitor to another location pin by pin.
VDecap ReMove User can delete the selected virtual decoupling capacitor.
VDecap ClearAll User can delete all of the virtual decoupling capacitors placed on the selected power net.
VDecap Report User can get the information for the selected virtual decoupling capacitor as figure 58.

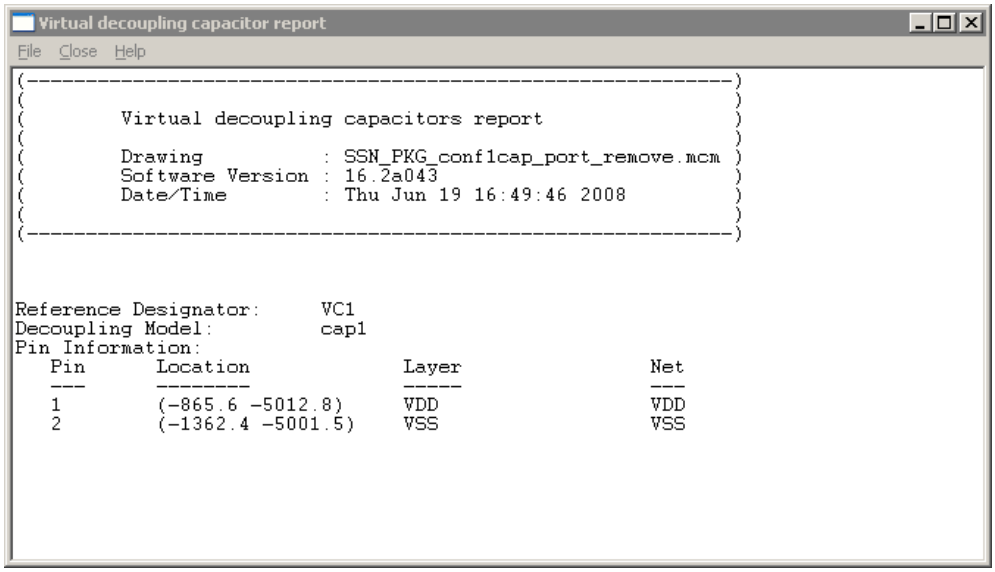


Figure 58: Vdecap Report on Allegro Canvas

User can place various probe ports in canvas directly to output voltage ripple and impedance value in specific locations. The probe port is a specified temporary component with 1-pin package but no decap model assigned. The probe port acts as test point for analysis, and will be float in tlsim subcircuit to generate output during simulation. The user needs to place the probe port before model extraction. The operation menu for one vritual probe port is as figure 59.

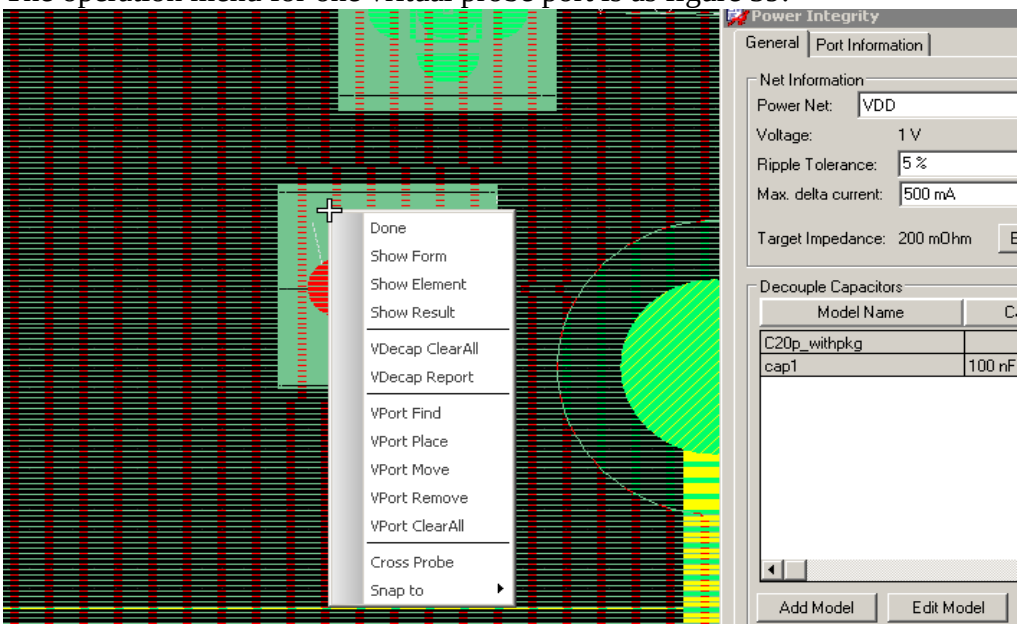


Figure 59: Menu for Right Click Button on One VPort in Allegro Canvas

Vport Place User can place one virtual probe port at any location on power/ground net.
VPort Find User can search for virtual probe port through the name and PI will zoom to the selected items and highlight then.
VPort Move User can move the placed virtual probe port to other location on power/ground net.
VPort Remove User can delete the selected virtual probe port.
VPort ClearAll User can delete all of the virtual VPorts placed on the selected power net.

3.13 Extraction and Analysis

In this section, user can now perform the voltage ripple analysis in time domain or target impedance analysis in frequency domain and check the result in SigWave.
After user has configured all corresponding parameters for field solver, optional VRMs, group various sink and source ports, and place all necessary virtual and instant decoupling capacitors into design, PI will call user-selected field solver to extract the equivalent subcircuit for selected power and reference nets, and then establish a full circuit for TLSim simulation engine in time or frequency domain, and display the analysis result in SigWave. Users can place new capacitors, refine existing capacitors, or replace the virtual capacitors into instant capacitors and then re-run the analysis for correction.

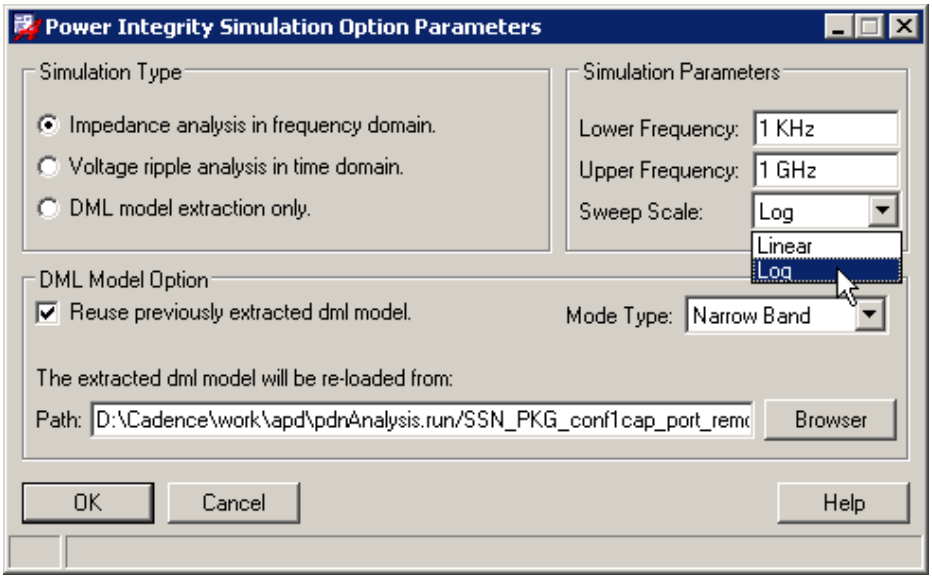


Figure 60: Simulation Parameters Options Form

User can click the **Analysis** button in main form for extraction and analysis, and the following analysis types will be prompted for user selection:

- **Impedance analysis in frequency domain**
- **Voltage ripple analysis in time domain**
- **DML model extraction only**

When user selects to **Impedance analysis in frequency domain**, Package PI will perform successive circuit build and TLSim simulation in frequency domain. The user can change the lower and upper frequency range for frequency domain simulation as figure 60. The target impedance and impedance curves of group ports will be viewed in SigWave. When option **Voltage ripple analysis in time domain** is selected, Package PI will perform successive circuit build and TLSim simulation in time domain. The user can set the duration time and resolution time for simulation and display as figure 61.

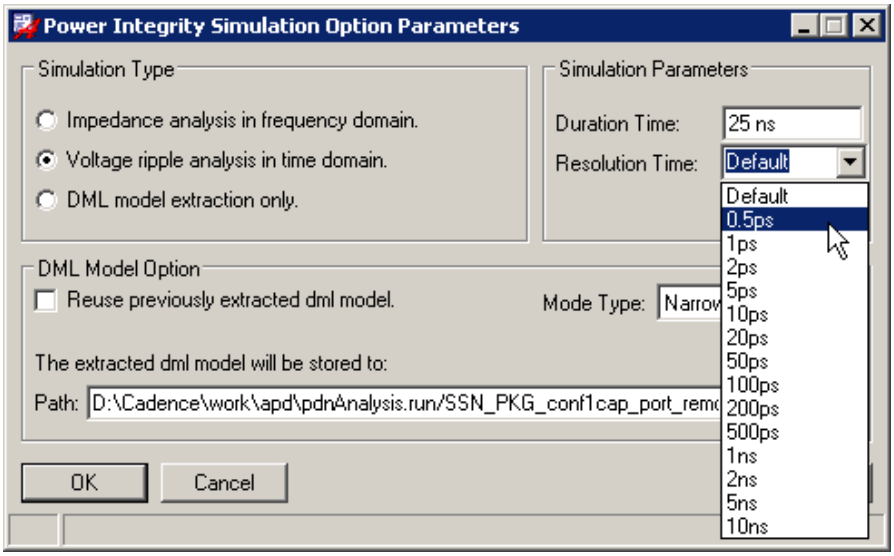


Figure 61: Voltage Ripple Analysis in Time Domain

4 SiP platform test plan

For the final validation of the complete signal integrity platform several test benches have been created using the Cadence Signal Xplorer tool SigXp.
The plan was to create one test bench for simulating the NOR signals and another for the DDR signals.
The parts and models required to build up the test benches is shown in Figure 6262.

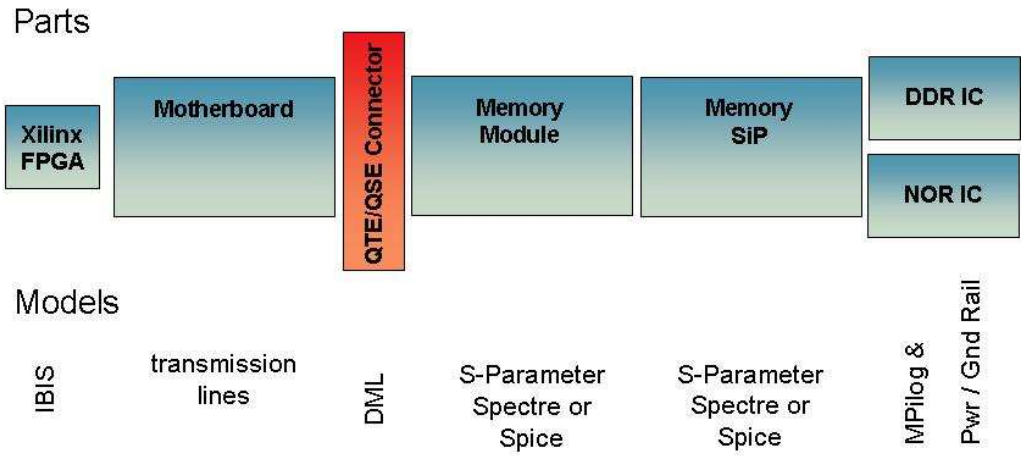


Figure 62 - Parts and models for the NOR and DDR test benches

The parts and models in detail are:

4. IBIS device model of the Xilinx Virtex5 FPGA including package model. The model was created with I/O models assigned to pins required for NOR and DDR simulations only.
5. Lossy transmission line elements and via models using standard elements provided by the Cadence SI tools. The parameters like line width and length of the transmission line elements were provided by Agilent.

6. Connector model provided by the vendor in the Cadence DML (device model language) format.
7. S-Parameter models of the Memory Module extracted by the 3D field solver from Agilent. A model for the NOR and DDR signals of interest respectively and a model of the Memory Module supply system.
8. S-Parameter models of the Memory SiP design extracted by the 3D field solver from Agilent. A model for the NOR and LPDDR signals of interest respectively including the supply system.
9. MPilog models for the DDR and NOR driver pins.
10. Power rail model representing the load for the MPilog models
11. Because the power supply net VDDQF on the motherboard was routed with narrow long traces a model for this net was extracted by the 3D field solver from Agilent too.

4.1 DDR test bench and simulation results

The DDR test bench has the same structure. FPGA I/Os on one side, transmission line and via elements modeling the main board interconnections, the Memory Module signal model in the middle and the SiP model on the other side and MPilog models for the DDR I/Os. A model for the power supply on the main board isn't required as the power is realized with plane layers. Also the Memory Module supply can be considered as nearly ideal with power ground planes and many decoupling capacitors. The DDR test bench used in simulations to get the following results is shown in Figure 63.

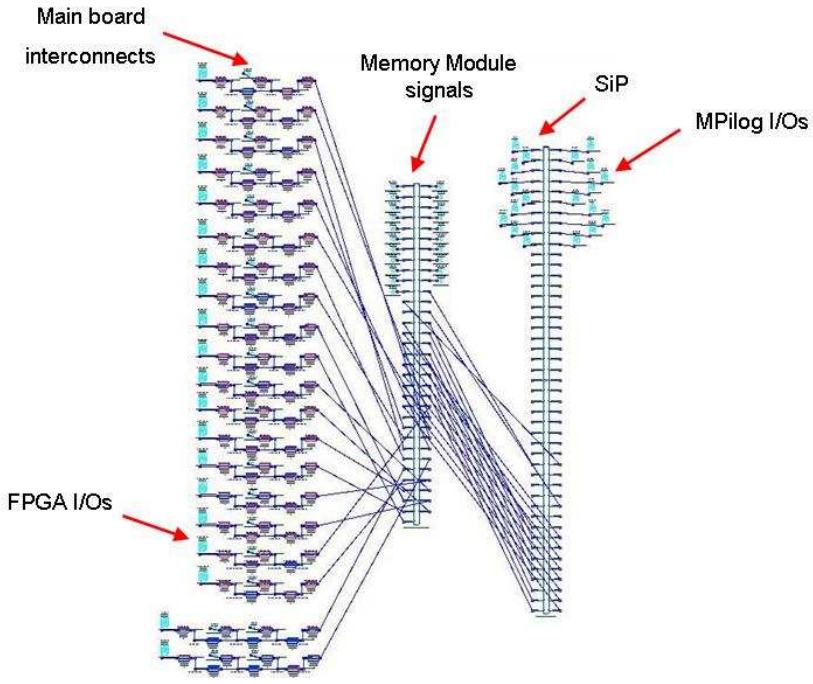


Figure 63 - DDR test bench

The first simulation vs. measurement result is a crosstalk simulation shown in figure 64. Victim net is the B_DQ3 signal in high state probed on the main board. All other B_DQ nets are switching at the same time.

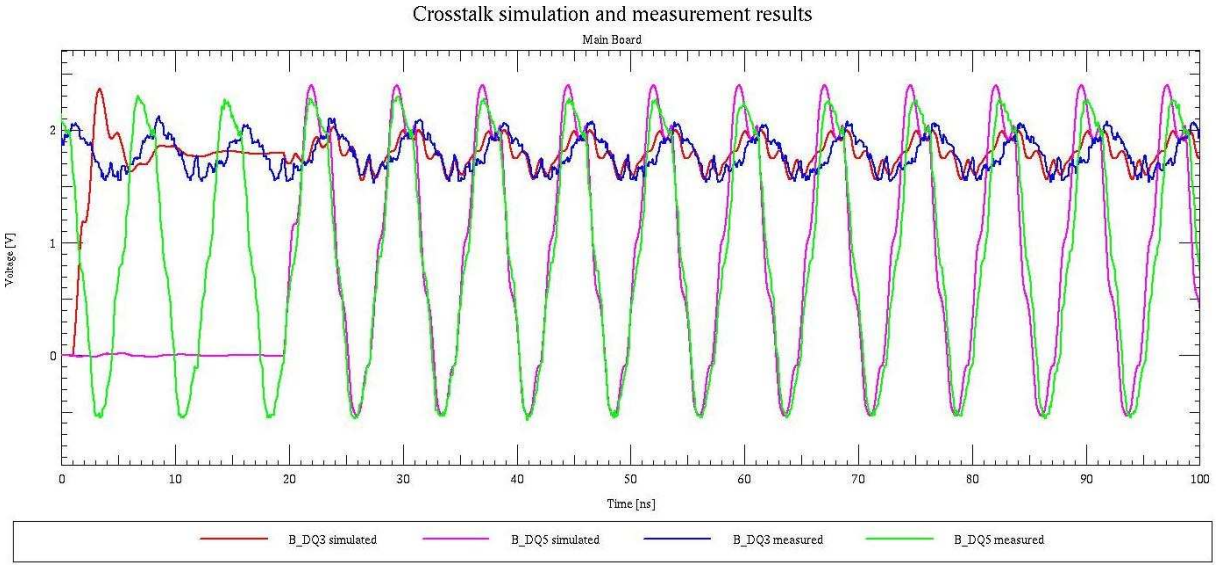


Figure 64 - Crosstalk simulation and measurement results; B_DQ3 high; all other B_DQ signals switching

Similar to the NOR test bench crosstalk result the high overshoot of the simulated signals is slightly larger than the measured one. The overshoot in low state shows a nearly perfect match between simulation and measurement. Also the crosstalk on B_DQ3 shows a very good correlation between simulation and measurement results.

The crosstalk simulation results with B_DQ3 in low state probed on the main board are shown in figure 65.

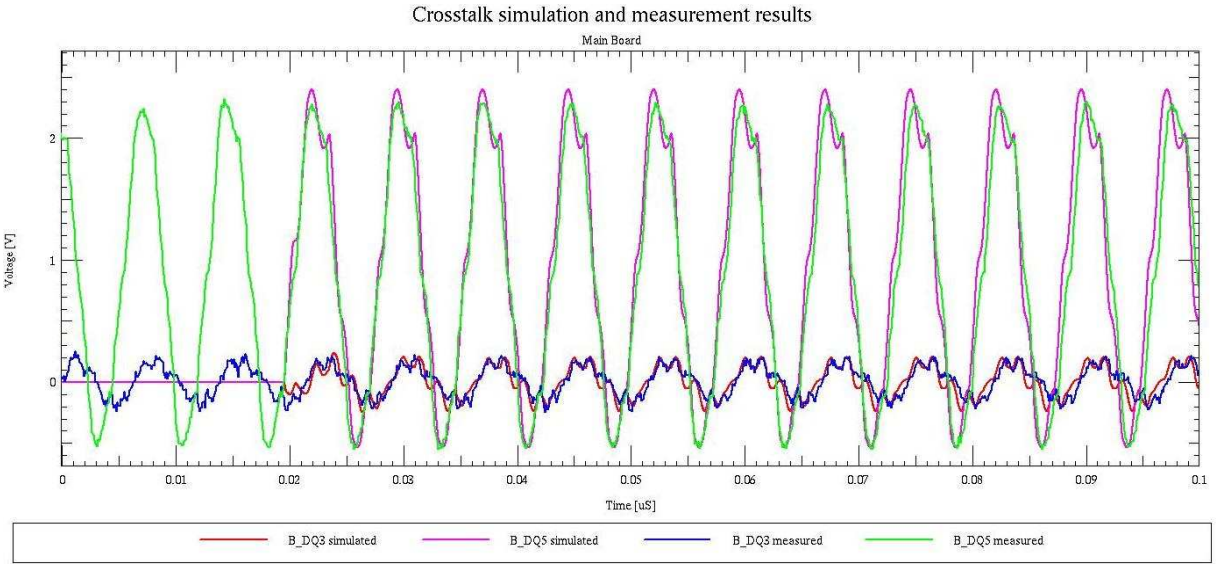


Figure 65 - Crosstalk simulation and measurement results; B_DQ3 low; all other B_DQ signals switching

The correlation between simulation and measurement is as good as described for B_DQ3 in high state.

The same simulation but with the signals probed at the Memory Module are shown in figure 66.

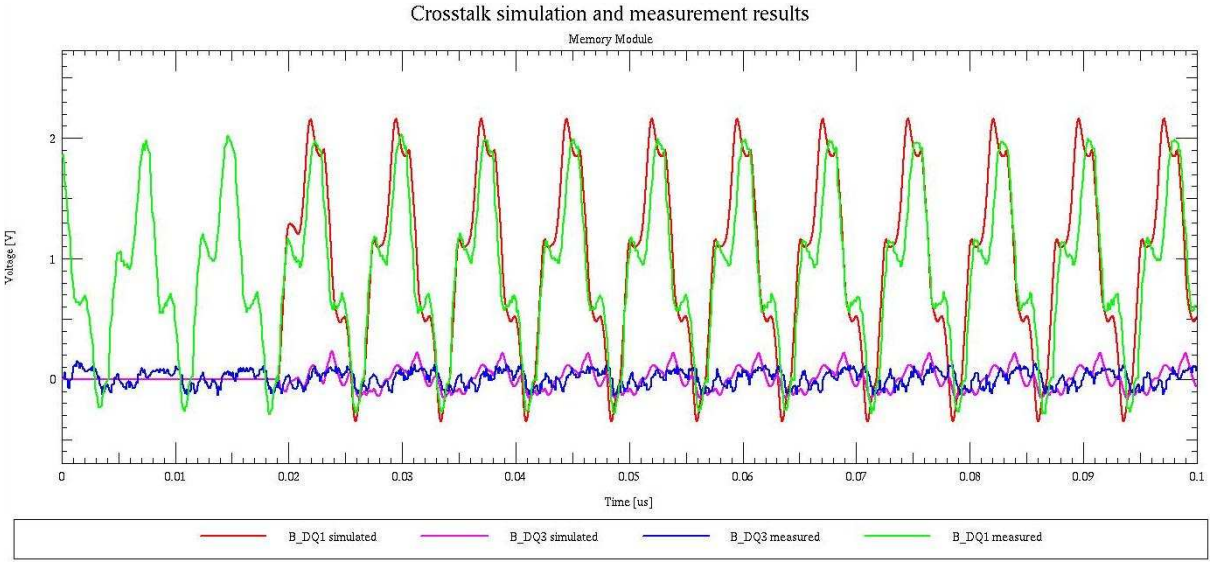


Figure 66 - Crosstalk simulation and measurement results; B_DQ3 low; all other B_DQ signals switching

The crosstalk amplitude at B_DQ3 is again matching very well between simulation and measurement. The difference of the switching signal B_DQ5 between simulation and measurement is probed on the Memory Module slightly larger. There is again a larger overshoot high of the simulated curve. The difference on the overshoot low is insignificant. Both simulation and measurement show a ringing in the rising and falling edges. The measured curve shows larger ringing.

In addition a bit pattern provided by Numonyx was simulated on the B_DQ nets to obtain eye diagrams. Theoretically for eye diagram simulations a large number of bits have to be simulated to cover a broad frequency range. Transient simulations especially on these large test cases are slow. Running the bit pattern on the DDR testcase 10ns of transient results per hour were obtained. The simulation was run several days to get the transient results covering 700ns transient time.

The simulated bit patterns from 0 to 700ns probed at the main board are shown in figure 67. The same bit pattern was applied to all B_DQ signals.

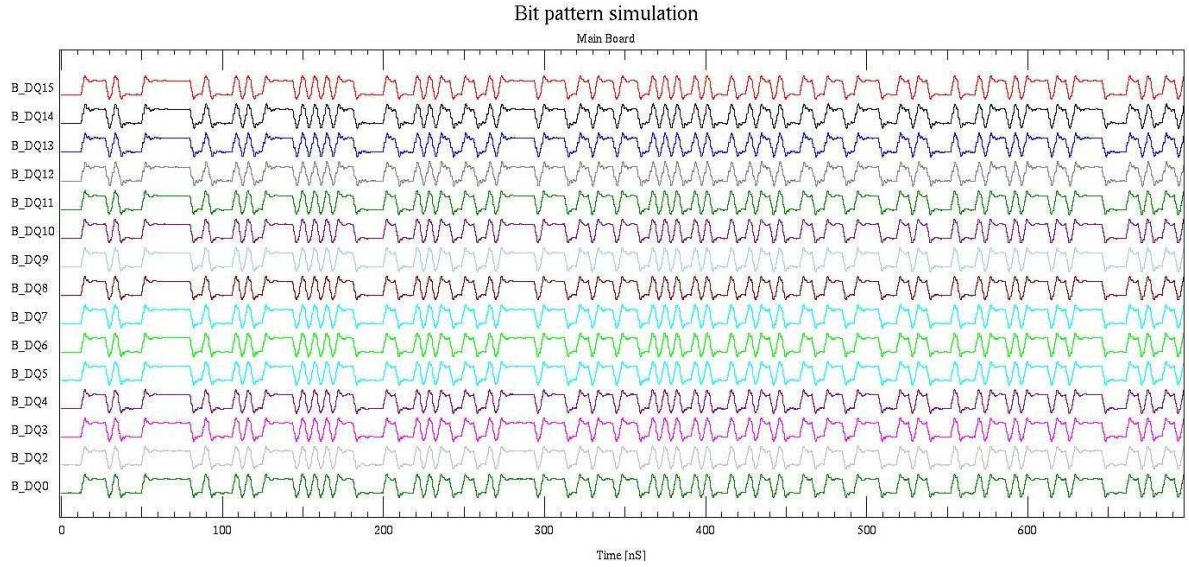


Figure 67 - Bit pattern simulated on B_DQ signals

This bit pattern simulation displayed in eye diagram mode is shown in figure 68.

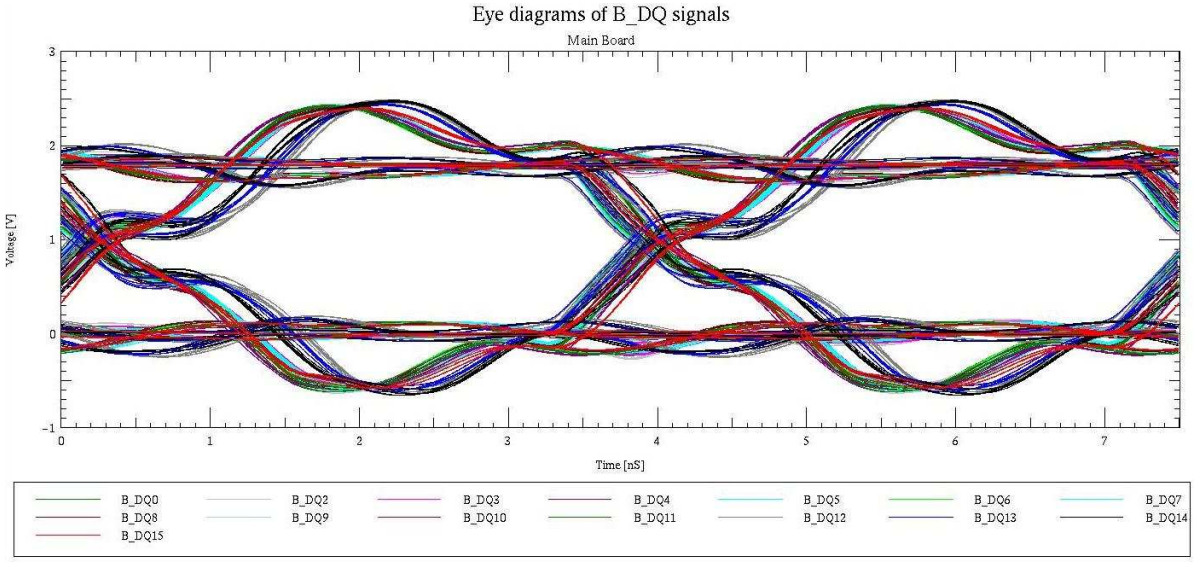


Figure 68 - Eye diagrams of B_DQ signals probed at the main board

There are other techniques like channel analysys or statistical approaches available to analyze the interconnection behavior for long bit pattern means a broad frequency range.
These analyses weren't yet performed but it should be possible to perform them on the Mocha test benches too.

4.2 Summary

Proof has been found that all relevant kinds of models could have been used in the SiP platform to create test benches, as well as to be netlisted and simulated with the Spectre simulator. Signal pathes spawning from a main board through a memory module and SiP were modeled and simulated. It was shown that the simulation results match very well to the measurements.