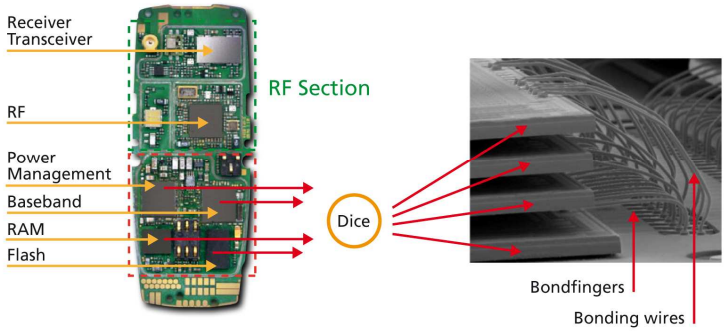
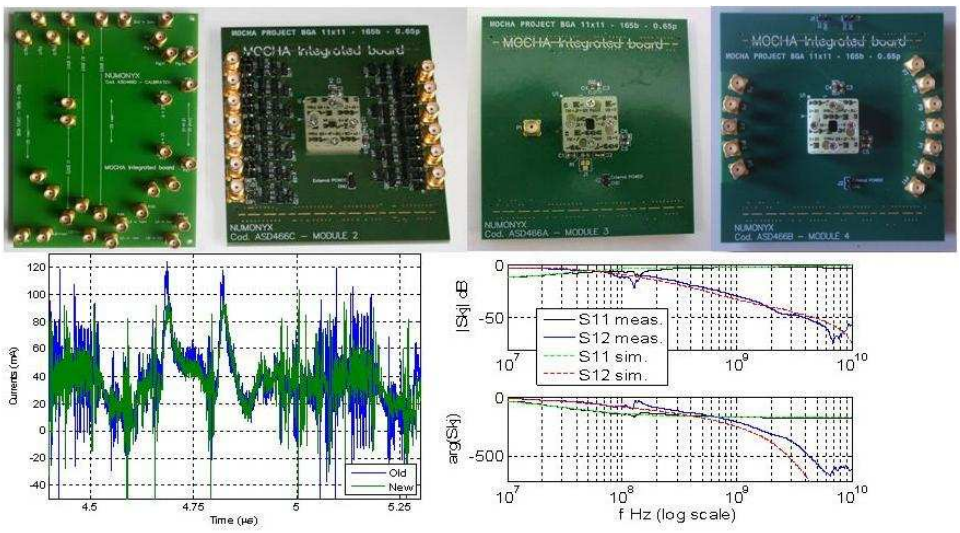
MOdelling and CHAracterization for SiP Signal and Power Integrity Analisys



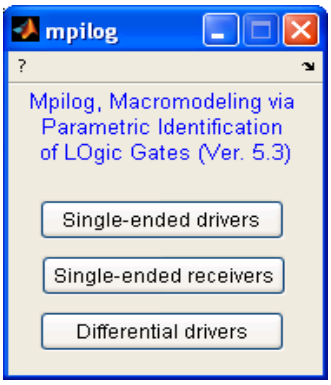
The MOCHA project work plan was organized in four major Work Packages, called as WP1, WP2, WP3 and WP4, according with the different technical fields to be addressed. However, they were not developed separately, but many interdependencies and interactions existed among the tasks of different work packages.
The main objective of WP1 was the development of a suitable modelling methodology for extracting a reliable model of IC power networks to be used for power integrity analysis. During the first year, the WP1 activities were focused on two main tasks: *"Wide-frequency-range passive power networks model"* (Task1.1) and *"Core switching activity model"* (Task1.2). The first one was devoted to the definition of the most suitable wide-frequency-range model of the IC power delivery networks, while the second one aimed at extrapolating the "switching activity" model of IC core. In summary, in the first task a cascade of lumped basic cells was defined to model the I/O power rail distribution. This model was completely validated through on wafer measurements (both unbiased and biased case) that allowed also extrapolating the model parameters. These measurements were performed on a wide frequency range (some MHz to 10GHz) for every considered test-case (internal and external memories). In the Task 1.2 the procedure for extracting by simulations the IC core switching activity current was finalized together with the design of a test board (denominated EMC-board) which, after a thorough analysis, was considered more suitable than alternative commercial solutions for the measurement of the switching current. During the second working year the activities of WP1 were focused on the: Task 1.3 (*Model Validation*) and Task 1.4 (*Characterization board design*). Within the Task 1.3 two main activities were carried out: a) use the designed EMC-board for extracting by measurement the IC core switching activity model and correlate the results with those of the simulations obtained in the Task1.2; b) perform power noise measurements on an ad-hoc application board and correlate the results with the ones obtained by a simulation test-bench that used the power integrity model finalized in Task1.1 and Task1.2. Both validation activities were carried out on the two selected test-cases (a NOR Flash memory and a LPDDR memory) with very good results that confirmed the approach used for the power integrity



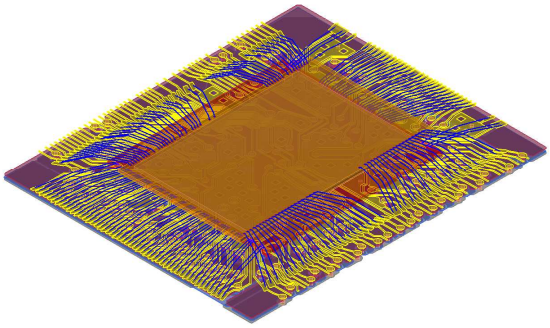
Integrated Board: on the top from left to right: Module 1, Module 2, Module 3, Module 4. On the bottom from left to right: Switching activity currents model validation, Power rail model validation.

modelling. In the Task 1.4 a characterization board which was flexible, practical and easy to use, independent (as much as possible) from the hardware specificities of each die being analyzed, was designed and manufactured. This platform, called "**Integrated Board"**, was composed of four modules, and implemented (i) the methodology defined in the Task 1.1 to measure S-parameters characteristics of the die power-rails, (ii) the circuitry to measure the die supply currents defined and validated in the Task 1.2; (iii) the circuitry necessary to perform the I/O buffer measurements that lead to the extraction of the Mπlog model; and (iv) a calibration board used for calibration purposes and to de-embed the characteristics of the test fixture structures inserted in the platform. The Integrated board is based on the MOCHA-SI mother-board, developed in the WP4 of MOCHA project. Up to 550MHz of working frequency is supported. The measurement results of Integrated Board platform were fully validated, together with the obtained models.

As regards the activity of WP2, it was devoted to the development of accurate and efficient models of digital ICs input and output buffers. The obtained models must overcome the current limitations of the existing state-of-the-art models in reproducing the behavior of recent devices with enhanced features and allowing to provide good predictions for large fluctuations of the supply voltage. Besides, they must be obtained either from simulation or from actual measurement carried out on a real board. During the first Year of the project, the research mainly focused on the selection of the most suitable model structure allowing to represent the nonlinear dynamical behaviour of the I/O buffers of a digital memory; on the procedure for the computation of model parameters from either the simulation of transistor-level models of devices and the real measurements carried out on a test board and on the implementation of model equations in different commercial EDA tools [1, 2]. Also, a systematic assessment of the accuracy and the efficiency of the proposed enhanced models obtained from the simulation of the detailed transistor-level models of the MOCHA test cases have been assessed, thus confirming the strengths of the proposed methodology. During the second Year, the activity concentrated on (i) the generation of models from real measured data, i.e., from transient voltage and current measurements carried out at the output port of a digital buffer connected to a distributed load and operating as in normal condition [2], and on (ii) the development of a set of modeling routines providing a useful tool for designers and allowing to generate device models for recent device technologies. The measurements have been carried out on the same test boards developed in WP1. A joint design of the boards has been in fact decided for optimizing the efforts and leading to a common characterization platform. The last part of the activity focused on (iii) the development of a procedure for the extraction of a selection of the characteristics of a digital buffer suggested by IBIS (Input/Output Buffer Information Specification, [3]) from the proposed enhanced models. The extraction procedure has been implemented in the Mπlog modelling tool developed during the project. The tool, that is freely available for download from the official MOCHA website http://www.mocha.polito.it, provides a step-by-step modelling procedure that guides the users to generate the models of digital devices (see the screenshot on the right). To spread the information on the MOCHA activities on WP2, the ongoing results of the second Year has been published in [2] and presented in the 2009 and 2010 European IBIS summit meetings.

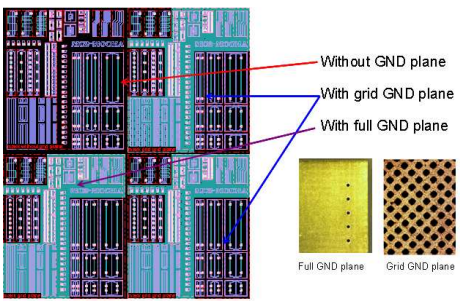


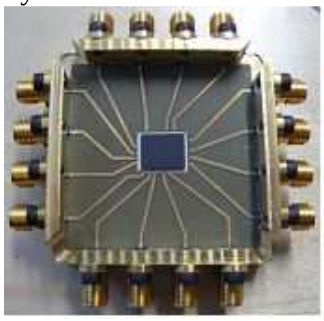
As regards the WP3, it focused on the development of two EDA tools: a 3D EM field solver by Agilent and a SiP Platform by Cadence, supporting design and verification power integrity analysis. During the first Year, Agilent mainly worked on the "EM front-end module", whose objectives were to address the need of extraction and transfer of the necessary design data available in the Cadence SiP platform into the 3D EM simulator. The second year had the following objectives: (i) the 3D EM field solver development. Its validation is part of WP4; (ii) the field solver integration in the SiP platform; (iii) the generation of the necessary EM models to validate the SiP analysis platform. In order to accomplish the first objective: the work was completed in the area of the layout pre-processing; the mesh algorithms were refined to produce efficient meshes; the EM solver technology needed to model the true 3D parts (i.e. the bond wires) was added into the solver; and an export link to back-annotate the model to the SiP platform was put in place. With these additions the second objective, the entire flow, could be completed. The flow encompasses the export of selected nets from the SI/PI platform to the EM field solver, the corresponding EM model generation and the back-annotation of that model to the platform so that it can be incorporated into a further analysis. The integration between the SiP Platform and the EM field solver was tested for a SiP BGA package of Numonyx (see the picture on the left).

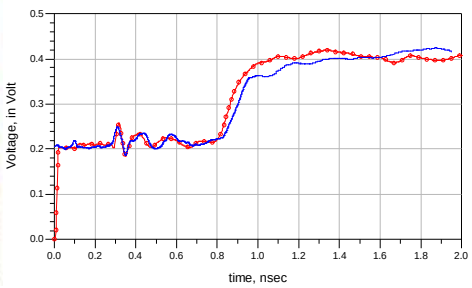


Finally, the third objective was accomplished by generating the necessary EM models to validate the SiP analysis platform. Multiple EM models were generated in support of the EDA platform validation and model correlation on a complete system (IC + PKG + PCB). An EM model was generated for the SiP design as a whole. As of Cadence's part, the first year efforts were concentrated on the development of new power integrity simulation strategies for the first half, joined by working on integrating Mpilog IO buffer model into the simulation environment. As for defining a power analysis strategy, it became quite clear that (i) both IC core as well as IO buffers need to be addressed; (ii) simulations need to be run in both time and frequency domain. While the IO buffer behavior is well understood and with Mpilog a comprehensive model is available, core power modeling requires a higher degree of abstraction due to the large number of transistors involved. The three methods research has been converging into are: (i) Measurement; (ii) Full chip static timing analysis (mostly applicable to memory only); (iii) Equivalent current source method. While the first two are obvious, the equivalent current source method abstracts core circuitry into a limited number of current sources. The reason for extending simulations commonly done in time domain into frequency domain is due to the nature of the power integrity problem itself and follows the very simple idea of defining 'good power integrity' as the actual impedance of the power delivery path for a given frequency range being equal or less the impedance profile required for delivering enough current at a maximum voltage drop over that same frequency range. While problems at very high frequencies (GHz-range and above) of the impedance profile of the power delivery path can only be fixed on the die (die capacitance and power/ground rails), lower frequency issues (several hundred MHz up to the GHz range) need to be fixed on the IC package (e.g. wire bond inductance). The second year's efforts were mostly spent on integrating the previously defined specification into the Cadence Allegro SiP design platform and to verify the system. This resulted in a prototype version of the Cadence Allegro SiP Power Integrity tool. From all that has been learned when consuming data from various inputs and performing validation and comparison with measurements, a list of enhancements and future improvements to the platform have been defined. While two test cases have been set-up for verification, the more demanding of the two (the DDR case) has been picked to correlate simulation results with measurements. Since there is a very good match between simulation results and measurements, the concept of the platform and the models has been proven.

As regards the WP4, at the beginning MC2-technologies carried out a deep bibliographic survey in order to identify the best approaches for device characterization at high frequencies. This work was aimed at validating by measurements two simulation platforms: the 3D EM solver developed by Agilent and the SiP Power Integrity tool developed by Cadence. To accomplish the first objective, two dedicated boards were designed and developed by MC2-Technologies. The first boards (picture in the left side) contained typical 3D physical structures of package and boards, while the second board (picture in the centre) allowed to carry out characterization measurements on a BGA package prototype designed and manufactured by Numonyx. These boards were probed thanks to microwave probes allowing TDR/TDT measurement with high accuracy. Agilent built up simulation test benches to produce simulation waveforms that could be directly correlated with the TDR and TDT measurement ones, obtaining a very good agreement (picture in the right side) that confirmed definitively the high accuracy of the 3D EM tool. From this validation step Agilent got a lot of learning's for further fine tuning the accuracy of 3D EM tool simulation results.



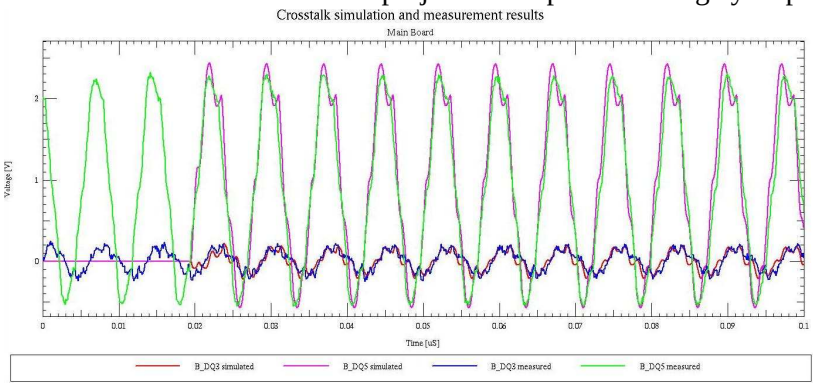




Finally a measurement platform was developed in this work package to allow the characterization of high-speed SiP devices and use the measurement results to validate the Cadence SiP Power Integrity tool. The designed board, called "**MOCHA-SI Platform"**, is a general purpose board that allows users to perform

signal integrity measurements on SiP devices up to 550MHz of working frequency. It covers the upcoming applications of memory systems, especially the ones that use LPDDR. The platform is composed of a main board (see the picture on the left) that hosts a Xilinx FPGA memory controller and a small board (i.e. the so called memory module) where the DUT is mounted. The memory module is plugged on the main board through two QTE connectors. A lot of studies through simulations and literature researchers were carried out by Numonyx and MC2-technologies to finalize the best state-of-art of design specifications. The measurements were carried out on a double stacked composed of the two test cases considered within the WP1 and WP2: the 512Mb Numonyx NOR Flash memory in 90nm technology (66MHz) and the 512Mb LPDDR third party device (133MHz). The laboratory results have shown good performances of platform and hence the quality of design was confirmed as well. Finally, as already anticipated, a set of the MOCHA-SI platform signal integrity measurement results were also used for validating the Cadence SiP Power Integrity platform. The picture below on the left shows an example of crosstalk analysis and the very good agreement achieved between simulation and measurement results.

The outcomes of the MOCHA project are expected to hugely improve the SiP design verification, reducing the time to market for every complex combination of non volatile memory, high speed volatile memory and µController. The capability to develop complex SiP solutions, ready to go in mass production, is going to become a key factor for successful semiconductor companies involved in today's memory market. Since most SiP devices are developed to address the handsets market segments (Low-end-Phone, Entry-Feature-Phone, Full-Feature-Phone and High-end/Smartphone), the MOCHA outputs will especially affect the design cycles in this area. The innovative simulation models and EDA tools as well as the measurement approaches developed and validated within the MOCHA project will be surely exploited to speed up the overall design and verification analyses, without derogating in accuracy at all.



More detailed information about the MOCHA project objectives and results, as well as papers and public deliverable reports, can be found on the public website www.mocha.polito.it.

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[2] I. S. Stievano, L. Rigazio, I. A. Maio, A. Girardi, R. Izzi, F. Vitale, T. Lessio, "Modeling of IC power supply and I/O ports from measurements," Proc. of 18th *IEEE Topical Meeting on Electrical Performance of Electronic Packaging and Systems, EPEPS*, Portland *(*Tigard), Oregon, pp. 85–88, Oct. 19–21, 2009

[3] I/O Buffer Information Specification (IBIS) Ver. 5.0, on the web at http://www.eigroup.org/ibis/ibis.htm, Aug. 2008.