Collaborative project

Small or medium-scale focused research project

THEME FP7-ICT-2009-4

Deliverable 4.2 – Realization of OTFT circuits on foil

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Coordinator contact details: Gerwin Gelinck (gerwin.gelinck@tno.nl)
TNO / Holst Centre
High tech Campus 31
PO Box 8550
5605KN Eindhoven
The Netherlands
Tel: +31 40 277 4098
Fax: +31 40 274 6400

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1	02-08-2011	Sarah Schols	First version
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3	08-08-2011	Sarah Schols	Third version sent to partners for approval
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1. Introduction

This deliverable describes the realization of circuits on foil. Two different technologies are implemented: unipolar p-type and unipolar n-type technology. The first part of this deliverable deals with the design of the different circuit building blocks. Realization of the circuitry is discussed in section 3.

2. Design of circuits on foil

Different circuit building blocks have been designed. Apart from standard building blocks, such as TFTs, invertors and ring oscillators, also larger digital and analog blocks, useful for the read/write electronics of memory arrays, have been designed.

Since the read-out electronics is preferably made with the same, or similar, technology as is used to make the memory arrays, most of the designs were made in unipolar p-type (pentacene) as well as in unipolar n-type (a-GIZO) technology.

2.1 Design of standard building blocks

Prior to the design of complex circuitry, robust technology development has been performed utilizing a basic mask set containing test structures like single transistors, inverters, ring oscillators. The layout of one cell of the used mask is depicted in Figure 1. Each cell comprises 24 repetitive structures allowing spread measurements of transistors. In the middle of the cell, small circuits are designed; more precisely zero Vgs-load and diode-connected load inverters and 5/19-stage ring oscillators.

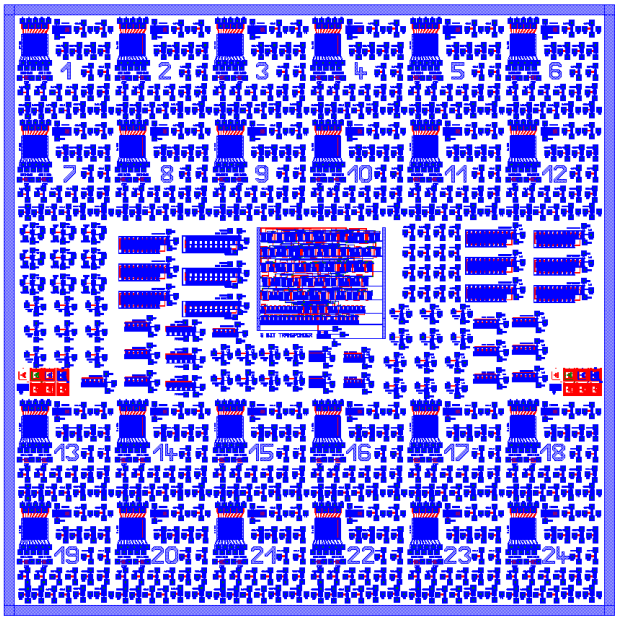

Figure 1: Test structures to evaluate both thin-film technologies

2.2 Design of digital building blocks for memory arrays

Furthermore, more complex building blocks enabling the integration towards a 96-bit, embedded memory system, have been designed. The architecture suggested in D5.1 for a 4x4 memory array (see also Figure 2) is easily upscalable to a 8x12 memory array.

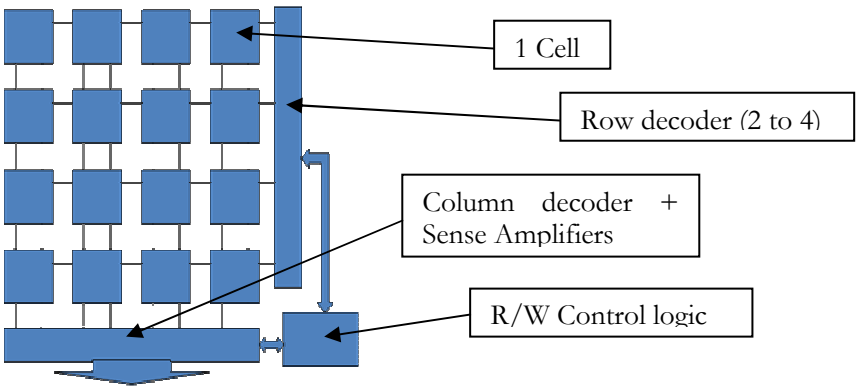

Figure 2: Block scheme of an embedded 4x4 memory with passive matrix configuration scheme

A major part in the design of organic readout circuitry is the selection of the word and column lines. Key for the word lines is that only individual word lines should be active during each part of the readout cycle. The column decoder, on the other hand, can be designed such that all 12 columns are read out simultaneously, which is advantageous for timing, but requires 12 sense amplifiers. An alternative configuration is that only 1 column is active during the readout cycle, requiring therefore only 1 sense amplifier. The latter option is most preferred for organic and metaloxide embedded memory arrays, because of the lowered risk for circuit robustness when integrating less analog building blocks.

Multiple possibilities for decoders are under investigation. A first possibility is the combination of a 4-bit binary counter and a 4-16 decoder (design shown in Figure 3). In case of the targeted matrix size, an 8x12 array, a 3-bit counter and a 3-8 decoder would be sufficient to drive the word lines. The column lines would require a 4-bit modulo-12 counter and 4-12 decoder. Another possibility for row and column decoders is the use of a so-called line driver or straight ring counter. A 10-stage and a 120-stage straight ring counter in dual-gate p-type technology and a 32-stage and 160-stage line driver in a-GIZO technology have been implemented (Figure 4).

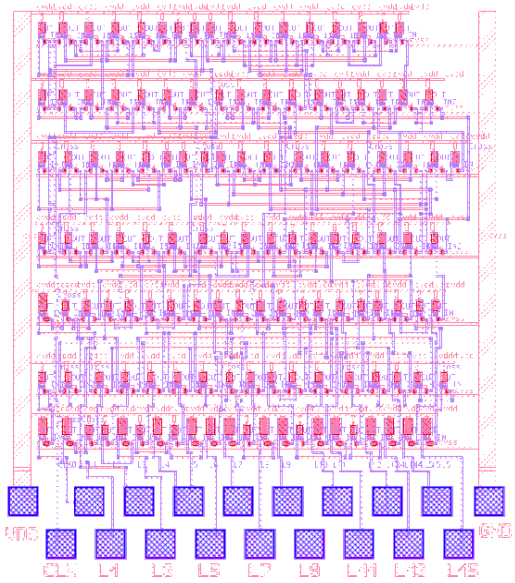

Figure 3: Implementation of a 4-bit binary counter combined with a 4-16 decoder using a-GIZO technology.

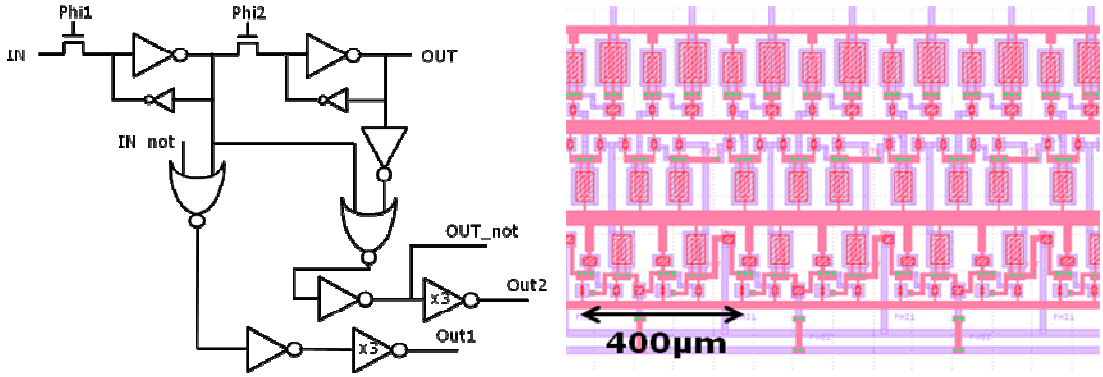

Figure 4: Implementation of a line driver using a-GIZO technology.

2.2 Design of analog building blocks for memory arrays

A sense amplifier, shown in Figure 5, was designed for the memory read-out. This sense amplifier is built with a differential amplifier strengthened with common-mode feedback, bootstrapped gain enhancement and gate-backgate connected 4-pin transistors. The output current of the memory cell is pushed through a resistor. The voltage signal over the resistor is stored on two capacitors with a delay of half a clock cycle in between both. Subsequently they are compared and the difference is amplified. In that way the differential output of the sense amplifier represents the value that was stored in the memory cell.

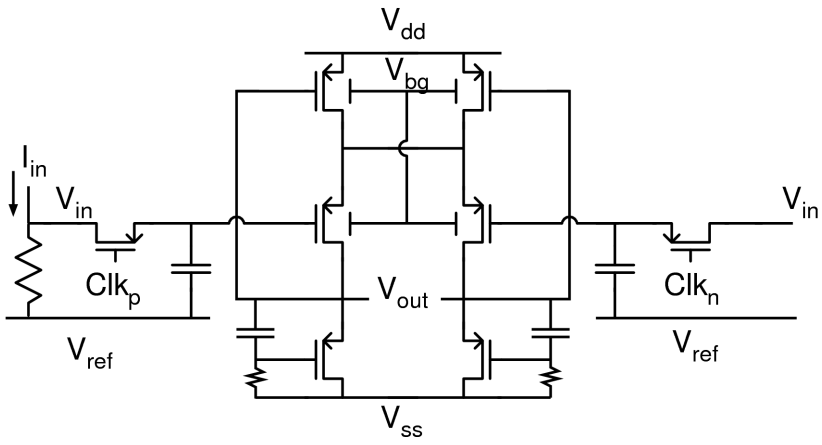

Figure 5: Schematic view of the sense amplifier for the memory read-out.

3. Realization of OTFT circuits on foil

3.1 Technology

As originally planned, we started making designs in p-type only logic circuitry. During the project, it was, however, decided that amorphous (n-type) metal oxide semiconductors merit deeper investigation and they are thought to be key to achieve the project's goals.
Therefore, many of the test structures and designs of circuit building blocks developed in MOMA to be implemented in unipolar p-type logic have recently been adapted in order to embed the ferroelectric memory devices with amorphous (n-type) metal oxide semiconductors.

3.1.1 Unipolar p-type technology (pentacene)

The unipolar p-type technology is based on pentacene as organic semiconductor. Furthermore, the cross-section of the layer stack depicts the availability of an additional gate, the back gate. The back gate is coupled much weaker to the channel than the front gate, such that it only shifts the threshold voltage. This effect is depicted in Figure 6.

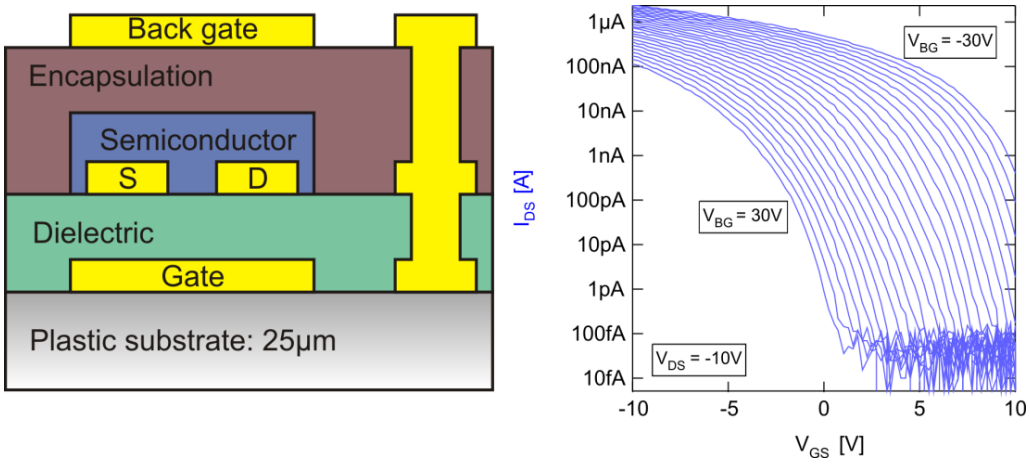

Figure 6: Cross-section of the dual-gate OTFT technology (left) and a typical measured transfer characteristic of this OTFT when using the back-gate as V_T-control gate (right). The channel width equals 140µm, the channel length 5µm.

This back gate architecture enables the possibility to design dual-V_T logic which favours in terms of robustness compared to single-V_T logic. Figure 7 shows an example of an inverter implementation using dual-gate TFTs. Increasing the back-gate voltage of the drive transistor introduces a shift of the inverters' transfer characteristic to its ideal position (half the supply voltage). This leads to an increased noise margin (>6V at a supply voltage of 20V) and therefore more robust circuitry. This digital building block topology has recently been integrated into larger circuitry, like RFID transponder chips [1] and an 8-bit organic microprocessor on foil [2].

[1] K. Myny, et al., IEEE J. of Solid-State Circuits, vol. 46, pp. 1223-1230, 2011
[2] K. Myny, et al., ISSCC 2011, pp. 322-323, San Francisco, February 20-24, 2011

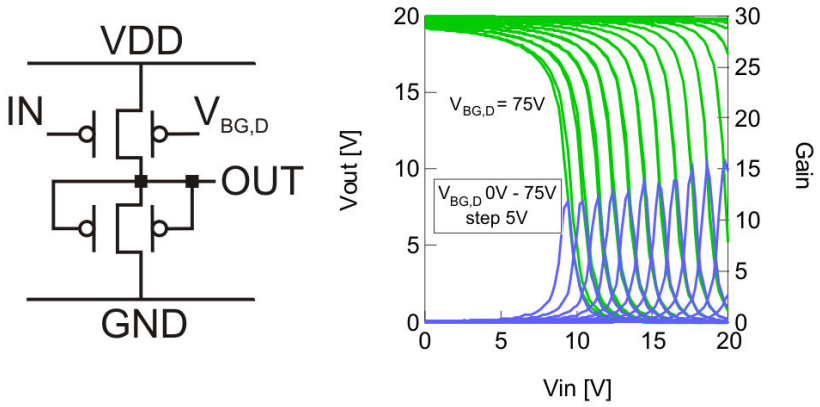

Figure 7: Architecture of the dual-gate, zero-V_{GS}-load inverter (left) and transfer curves of these inverters plotted for a supply voltage of 20V, as a function of the voltage on the V_T-control gate of the drive transistor (right).

3.1.2 Unipolar n-type technology (a-GIZO)

Many of the test structures, measurement protocols, design and addressing schemes developed in MOMA require little to no adaptation in order to embed the ferroelectric memory devices with other thin-film transistor technologies, such as amorphous silicon metal oxide transistors.

The cross-section of the proposed n-type technology is shown in Figure 8. It consists of an a-GIZO semiconductor, processed at temperatures below 150°C, which enables integration of this technology on foil. Figure 8 depicts the transfer curves of 8 a-GIZO TFTs on foil, yielding a charge carrier mobility of 9 cm^2/Vs. We have also integrated these GIZO TFTs into zero-V_{GS}-load inverters. Typical inverter measurements are shown in Figure 8 when a supply voltage of 10V is applied.

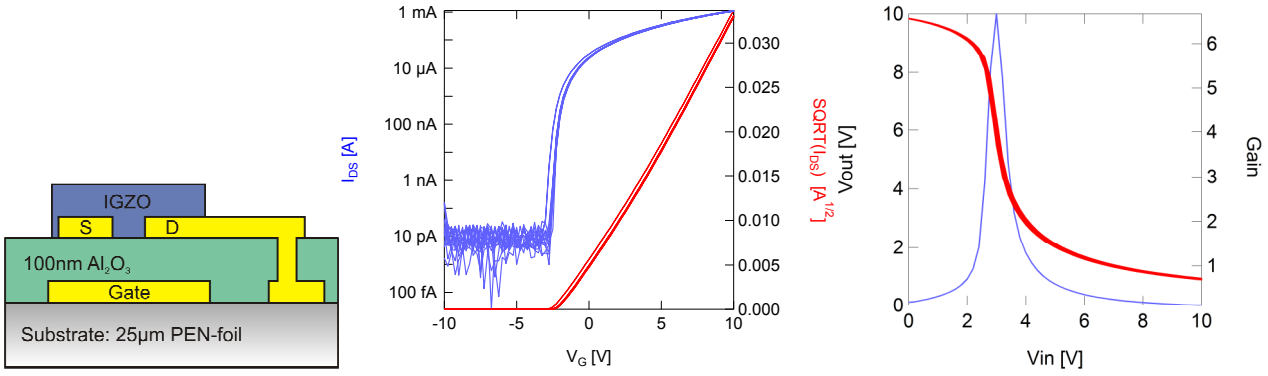

Figure 8: Cross-section of the a-GIZO TFT technology (left), 8 typical obtained transfer characteristics (middle) and 5 zero-V_{GS}-load inverters at a supply voltage of 10V (right).

3.2 Realization of analog and digital building blocks for memory arrays

Besides basic logic blocks, we have also realized and characterized some more complex building blocks related to the embedded memory architecture. Figure 9 demonstrates that straight ring counters (up to 120 stages) can be used as row and/or column decoders since the on-signal, in this case '0', returns after it rippled through all stages in the circuit. The clock for this circuit was 200Hz for a supply voltage of 20V and a back-gate voltage of 35V. Each on-time for the line is 5ms, and the signal returns after 120 stages or 600ms. In the final demonstrator design, the 120-stages will be 8 stages for the word lines and 12 stages for the column lines. The achieved frequency of 200Hz is sufficiently high to meet the specifications of the final 96-bit demonstrator.

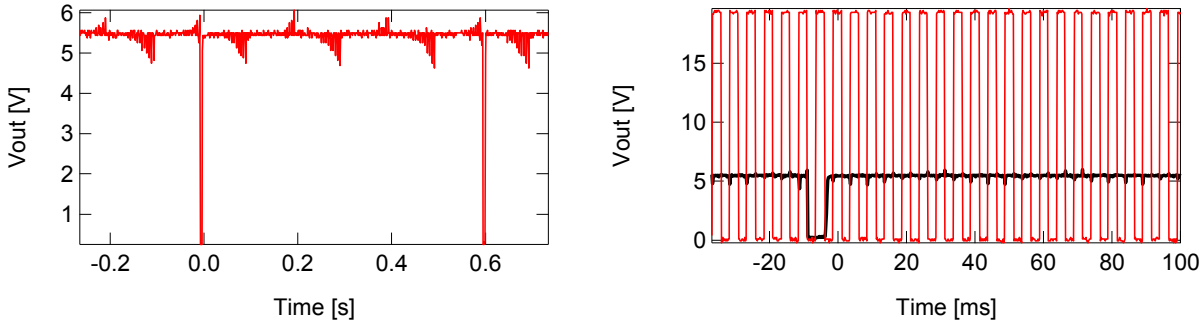

Figure 9: Obtained measurement result of a 120-stage straight ring counter for about 2 periods (left) and a zoom of 1 cycle (right).

The characterization of all realized analog and digital building blocks will be presented in D4.3 that will mostly focus on the realizations in a-GIZO technology because of the relevance of the MOMA-project.

4. Conclusions

In the current timeframe of the project, we have primary focussed on the realization of organic thin-film circuitry on foil, yielding working row decoders so far. On the other hand, due to the promising characteristics of the metal oxide semiconductors, read/write circuitry have been adapted to work in latter technology. In the next period, we will therefore mainly focus on the characterization of a-GIZO read/write circuits, targeting 96-bit embedded memories on foil.