CARBON BASED SMART SYSTEM FOR WIRELESS APPLICATION

Nano-RF

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1 ABBREVIATION / DEFINITION

CPW	Coplanar waveguide
CNT	Carbon nanotube
CNTFET	Carbon nanotube based Field effect transistor
GFET	Graphene based Field effect transistor
RF	Radio frequency

2 INTRODUCTION

Transistors made out of graphene and Carbon nano-tubes was one of the major goals of the NANO-RF project. In this report the performance of each constituent technology will be briefly reviewed. The performance of the fabricated devices will be described and the problems addressed at each step will be discussed.

In total a series of 14 fabrication runs were done within the project and both CNT and graphene FETs were realised in most of them with variations. A total of 50 samples were fabricated and measured.

3 MEASURING SETUPS

To completely characterize the fabricated FETs a series of setups were utilized. They are briefly described in the following section

3.1 LOW FREQUENCY MEASURING SYSTEM

Measurements were done at probe station using Keithley 2604B, wave generator Agilent 33500B (fmax 20MHz) and digital oscilloscope OWON MSO8202T. This setup operates in 2 modes either a DC mode were the current and voltage are directly aplied and measured by the K2604B using an automation program, or in low F mode were the DC components are applied by the K2604 but an AC component is also applied by the signal generator and the response is measured using the circuit shown below.

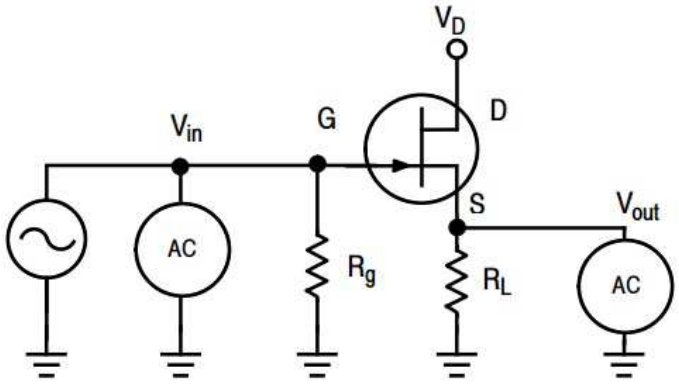


Figure 1: Schematic of the measurement circuit for low AC FET response.

Using this setup it is possible to measure DC response, and AC up to 10 MHz.

3.2 HIGH FREQUENCY MEASURING SYSTEM

Measurements were done using two systems:

1. An HP8510B VNA up to 100MHz - 20GHz
2. An Agilent MS4644 VNA up to 10MHz - 40 GHz

Both systems can bias the DUT using a K2604B and perform multiple RF performance measurements for different bias points automatically.
The resulting S-parameters were used to analyse the FET performance under high frequency operation.

4 OPTIMIZATION OF FET CONSTITUENTS (OHMICS AND DIELECTRICS)

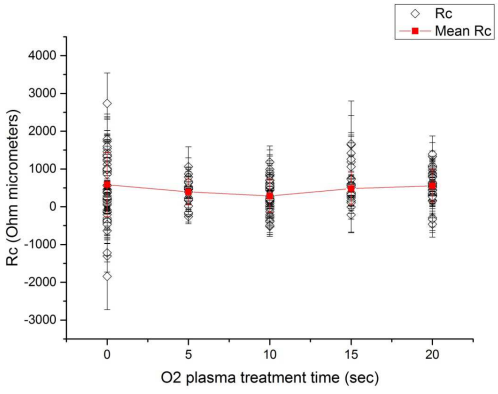
4.1 OHMIC CONTACTS

The following table summarizes the work done to optimize the ohmic contacts for Graphene FETs. All samples were CVD graphene on Silicon / SiO_2.

Sample	O_2 plasma treatment time (sec)	No annealing	Vacuum annealing (300^{O}C for 10min)	Air annealing (300^{O}C for 10min)	Forming gas (H_2/N_2) annealing (200^{O}C,300^{O}C,400^{O}C for 10min)
Sample1	*0,5,10*	√		√	
Sample2	*0,15*	√	√	√	
Sample3	*0,20*	√		√	
Sample4	*0,5,10,20*	√	√		
Sample5	*0,10,15*	√			√

Table 1: Process information for the graphene ohmic contact optimization

Each parameter was independently optimised. Initially the Oxygen plasma pretreatment time on the areas were the contacts would be deposited was investigated. The figures below show the extracted contact resistance and the sheet resistance of the material between the contacts. Differences of the Rsh are attributed to doping of the graphene – metal contact due to oxygen spieces.



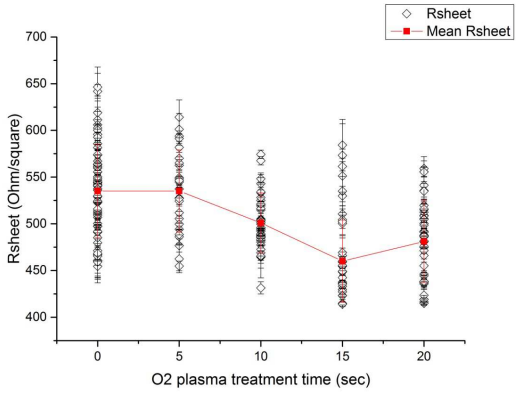


Figure 2: Contact resistance (left) and Sheet resistance (right) depending on the oxygen plasma time exposure prior to metal deposition. No annealing

The optimum plasma time exposure was 10sec and that was used to investigate the post deposition annealing as shown in the following figure. Annealing in air and vaccuum did not substantially improve the contact performance whereas forming gas annealing showed clear evidence of contact improvement.

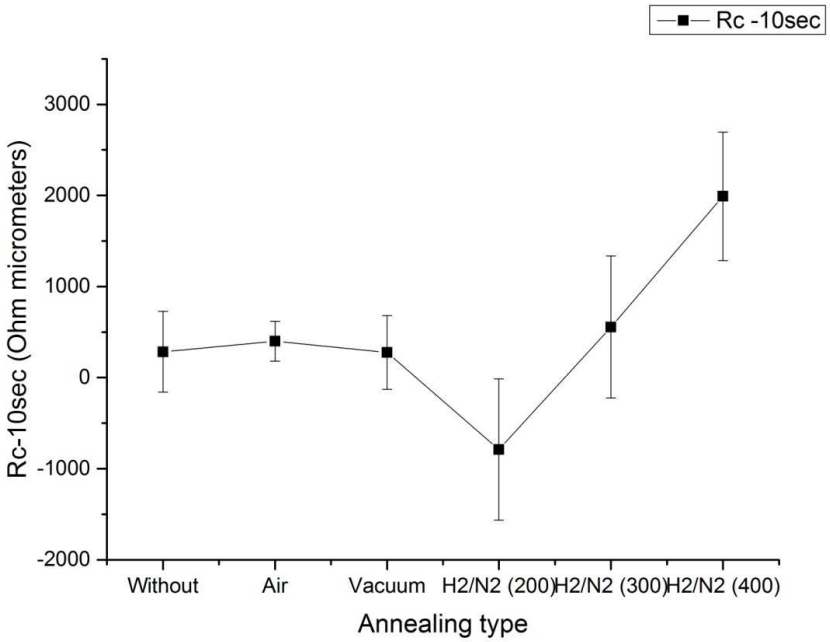


Figure 3: Contact resistance as a function of annealing ambient and temperature. The optimum results are obtained for forming gas annealing (H_2/N_2) at 200ºC. The first data point corresponds to no annealing

A more detailed view of the acquired data regarding contact resistance is shown below. The optimum annealing temperature was 200ºC.

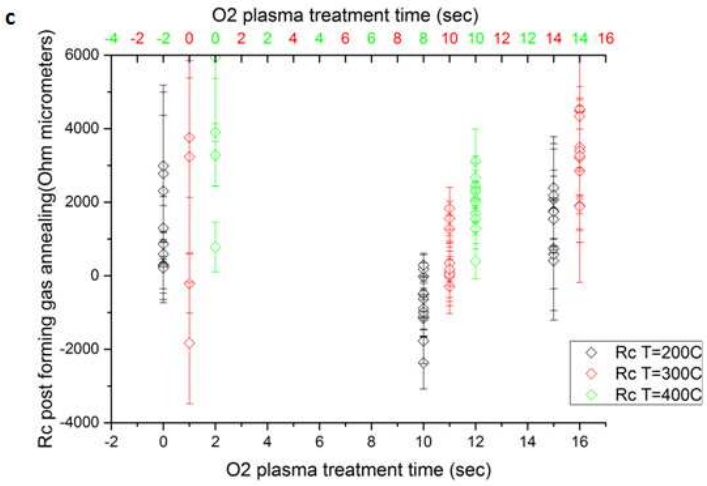


Figure 4: Contact resistance for post-forming gas annealing at 200ºC, 300ºC and 400ºC as a function of O_2 plasma treatment time. Traces corresponding to different annealing temperature have been shifted for clarity.

Sheet resistance is an indirect measure as to the quality of the remaining graphene layer (the channel) te higher resistance translates to less doped graphene which is a desired feature in FET fabrication. As can be seen the optimum values are obtained for forming gas at 200 and 300 Celsius.

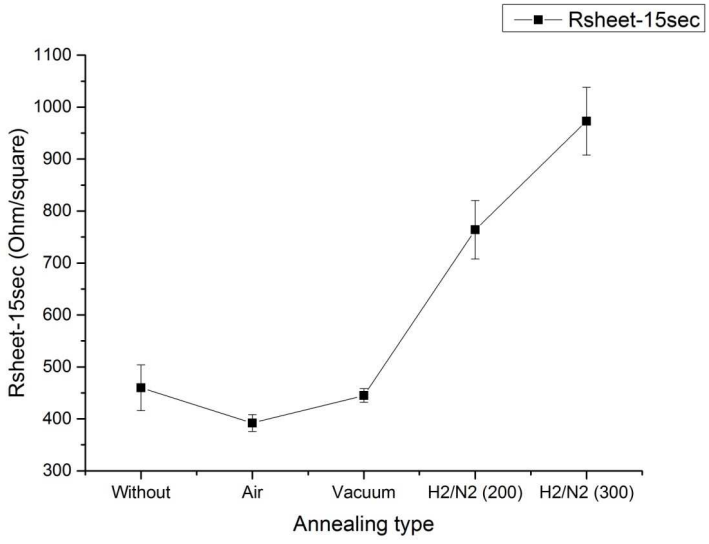


Figure 5: Mean R_{sheet} for 15sec O_2 plasma treatment time versus all thermal annealing types (in air, in vacuum, in H_2/N_2 at 200°C, 300 °C and 400 °C) respectively.

The optimization of ohmic contacts was performed in parallel with the initial fabrication runs and was incorporated into the main fabrication flow after run 6.

4.2 DIELECTRICS

4.2.1 Low-k dielectric optimization

Two type of low-k dielectrics were used at the early stages of the FET fabrication. They were mainly used as a reference to the high-k material that is described in the following section. Furthermore that choice allowed the consortium to optimize the rest of the FET process independently from the high-k dielectric development thus saving time.

Polyimide was used initially to obtain very thin layers using spin coating. Although the material exhibits very low dielectric constant and voltage breakdown it is known to produce no adverse effect on graphene and CNT mobility and is very simple to process.

Si_3N_4 deposited by plasma enhanced chemical vapour deposition (PECVD) at temperatures of 300 and 150ºC was also investigated. The technique avoid very high deposition temperatures and the deposition process was optimized using Raman to investigate the effect of deposition to graphene quality.

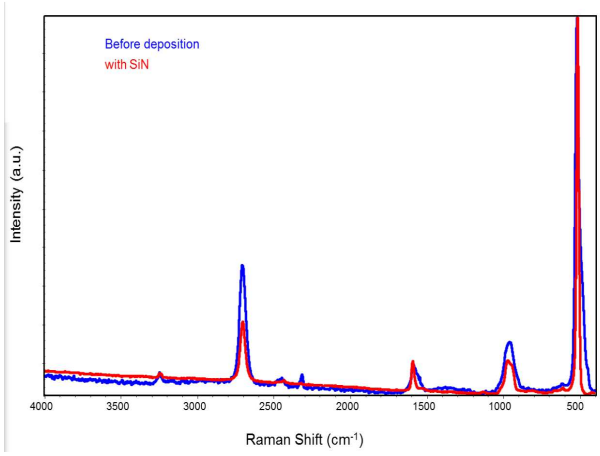


Figure 6: Raman before and after Si_3N_4 deposition by PECVD showing no adverse effect on graphene.

Overall, the low-k dielectrics were used to create graphene FETs and the gate leakage sand breakdown was measured and is shown in the following figure.

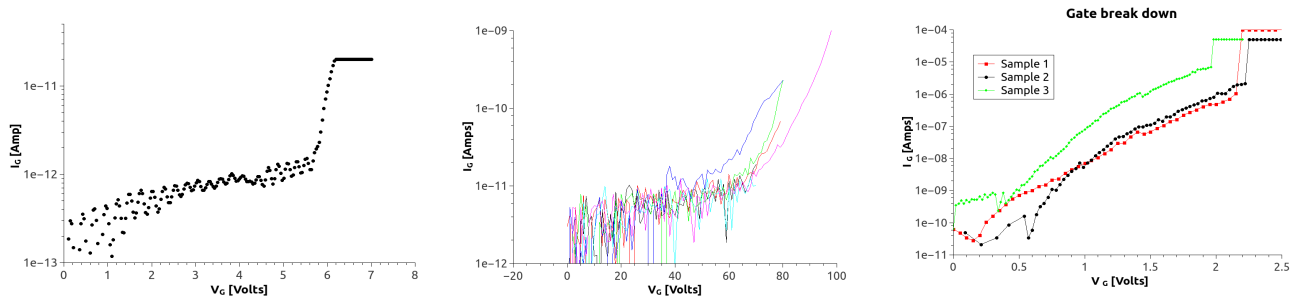


Figure 7: Leakage and breakdown behaviour of metal – dielectric – graphene structures. Left is 40nm Si_3N_4, center is 250nm polyimide and right is 40nm polyimide dielectric.

The breakdown voltage is shown in the following table.

Sample	Breakdown (Volts)	Dielectric strength
40nm Si_3N_4	*5.5*	*137.5 V/μm*
250nm Poly	*63*	*252 V/μm*
40nm Poly	*2.1*	*52 V/μm*

Table 2: Dielectric behaviour information for low-k dielectrics used in NANO-RF

It is evident that the Polyimide layer exhibits a large leakage when thinned down and a low breakdown.

4.2.2 High-k dielectric deposition optimization

Raman was used to check graphene and CNT prior and after HfO2 deposition.

process was optimized using Raman to investigate the effect of deposition to graphene quality.

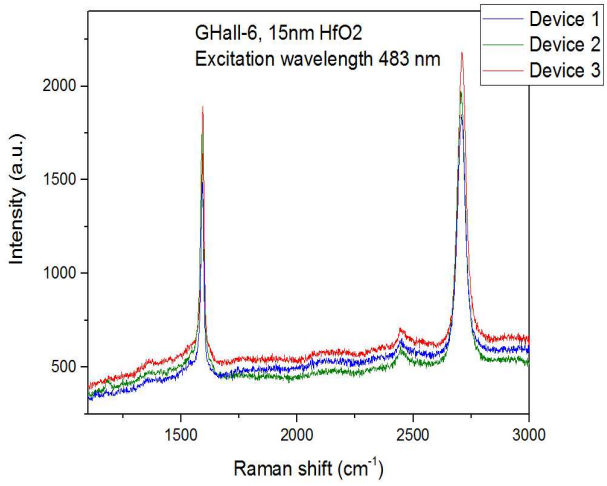


Figure 8: Raman after HfO_2 deposition on graphene.

The mobility was also measured in test structures and is shown below.

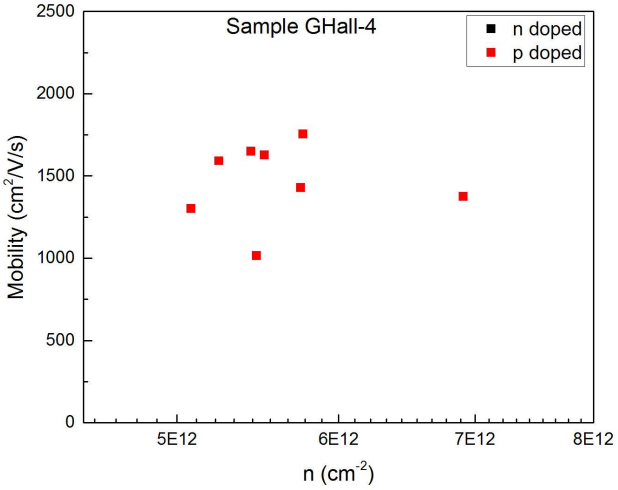


Figure 9: Plot of the charge carrier mobility μ ($cm^2/V/s$) as a function of residual carrier concentration n (cm^{-2}) for sample Ghall-4 (5nm HfO_2)

4.2.3 High-k dielectric electrical performance

Since both graphene and CNTs are prone to surface scattering, the gate dielectric is a critical issue in Fet fabrication in both technologies. ALD growth of dielectrics is not possible directly on graphene nor CNTs it is thus necessary to provide a nucleation layer. Different approaches were investigated as shown on the table below. The initial samples were used to characterize the e-gun evaporated HfO2 materials and subsequently ALD was used (samples 5-7).

Sample	HfO_2 thickness (nm)	Deposition technique
Sample 1	*10*	*e-gun evaporation*
Sample 2	*20*	*e-gun evaporation*
Sample 3	*80*	*e-gun evaporation*
Sample 4	*200*	*e-gun evaporation*
Sample 5	*7*	*e-gun evaporation +ALD*
Sample 6	*12*	*e-gun evaporation +ALD*
Sample 7	*17*	*e-gun evaporation +ALD*

Table 3: Process information for samples to study HfO_2 dielectric performance

e-gun evaporated HfO_2 suffers from structural integrity and that is evident in the electrical characteristics shown below.

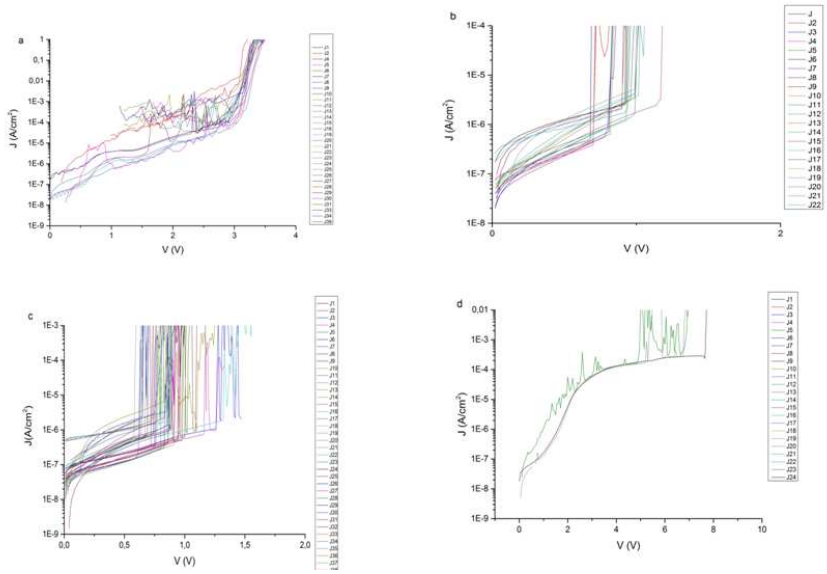


Figure 10: J-V characteristics of samples with e-gun evaporated HfO_2. a) Sample 1 with 10nm HfO_2, b) Sample 2 with 20nm HfO_2, c) Sample 3 with 80nm HfO_2 , and d) Sample 4 with 200nm HfO2.

In the above figure, the J-V characteristics of the samples with e-gun evaporated HfO_2 are illustrated. As we observe the breakdown voltage and the leakage current density for the sample with 10-nm thick HfO_2 were (2.90±0.60)V and (1.06e-6±1.02e-6)A/cm2, respectively. For the samples with 20-nm and 80-nm thick HfO2 the values of the breakdown voltage were (0.90±0.10)V and (0.83±0.17)V while the corresponding leakage currents were (1.62e-7±1.02e-7)A/cm2 and (1.32e-7±1.04e-7)A/cm2. Finally, the breakdown voltage and the leakage current density for the sample with 200-nm thick HfO_2 were (6.30±1.32)V and (1.12e-7±8.40e-8)A/cm2, respectively. The results are summarized in the following table.

HfO_2 thickness (nm)	V_{br}(V)	J_{leak}(A/cm^2)
10	(2.90±0.60)	(1.06e-6±1.02e-6)
20	(0.90±0.10)	(1.62e-7±1.02e-7)
80	(0.83±0.17)	(1.32e-7±1.04e-7)
200	(6.30±1.32)	(1.12e-7±8.40e-8)

Table 4: Summary of electrical performance of e-gun evaporated HfO_2 dielectric films

The breakdown and leakage of the layer was high as expected revealing a poor dielectric quality. The final method used was a thin (2nm) nucleation layer deposited by e-gun) followed by a thin high quality layer deposited using ALD. The following figures show the ALD deposited samples performance.

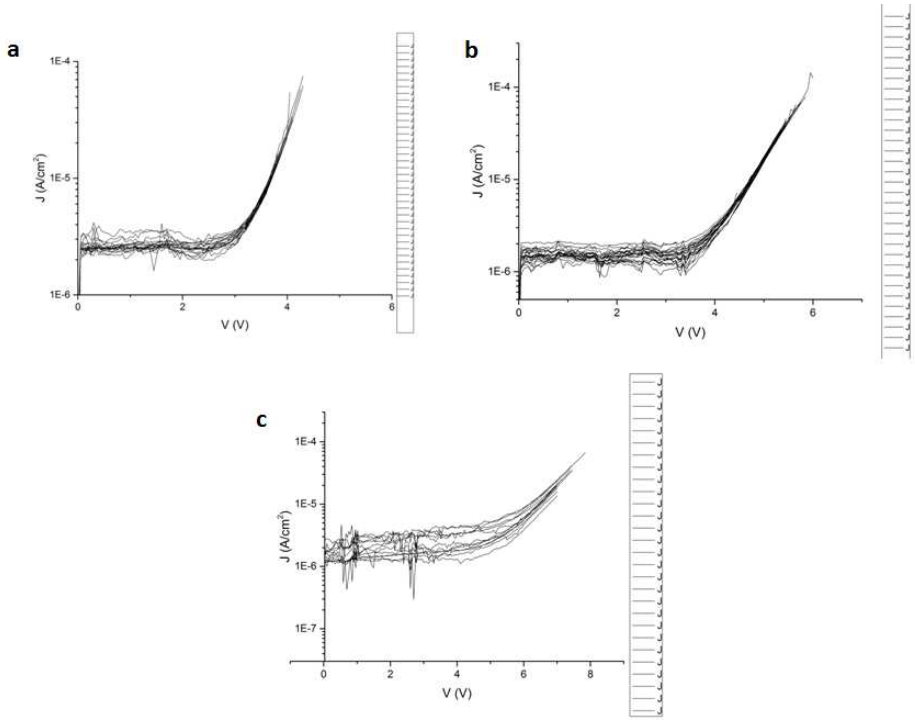


Figure 11: J-V characteristics of samples with mainly atomic layer deposited HfO2. a) Sample 5 with 7nm HfO2, b) Sample 6 with 12nm HfO2, and c) Sample 7 with 17nm HfO2.

In the above figure, the J-V characteristics of the samples with atomic layer deposited HfO2 are illustrated. As we observe the breakdown voltage and the leakage current density for the sample with 7-nm thick HfO_2 were (3.20±0.40)V and (4.15e-6±8.80e-7)A/cm2, respectively. For the samples with 12-nm and 17-nm thick HfO_2 the values of the breakdown voltage were (4.50±0.50)V and (5.70±0.40)V while the corresponding leakage currents were (1.80e-6±5.80e-7)A/cm2 and (1.40e-6±8.70e-8)A/cm2. The results are summarized in the following table.

HfO_2 thickness (nm)	V_{br}(V)	J_{leak}(A/cm^2)
7	(3.20±0.40)	(4.15e-6±8.80e-7)
12	(4.50±0.50)	(1.80e-6±5.80e-7)
17	(5.70±0.40)	(1.40e-7±8.70e-8)

Table 5: Summary of electrical performance of ALD deposited dielectric films

The following figures serves as a comparison of the electrical characteristics of the e-gun and ALD depsited dielectric layers.

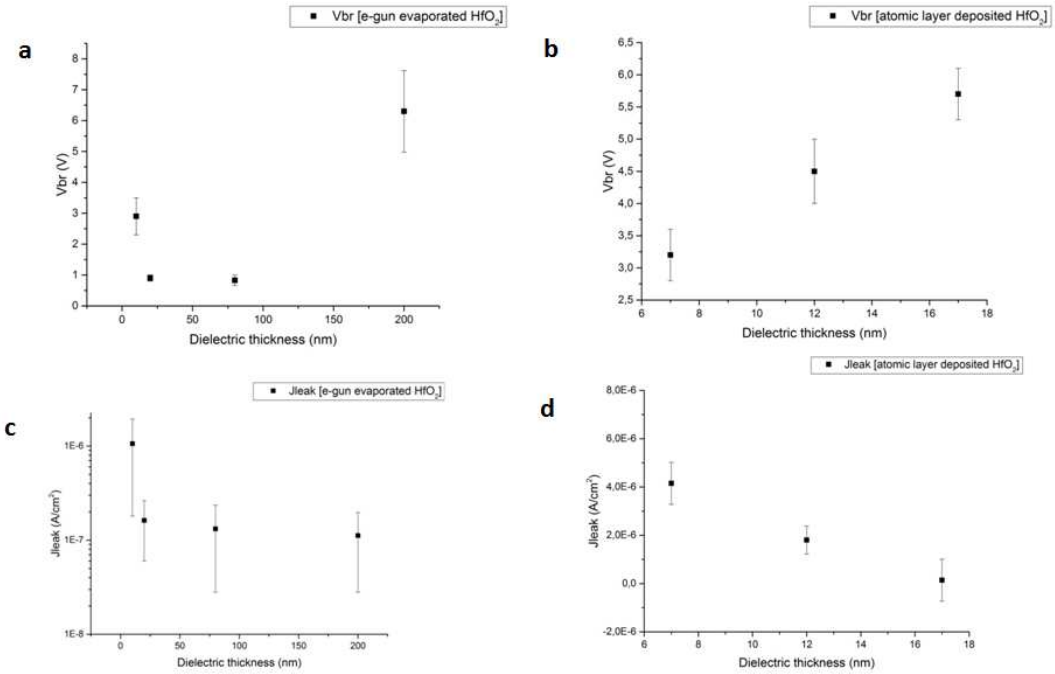


Figure 12: Breakdown voltage and leakage current density as a function of dielectric thickness. a) V_{br} vs dielectric thickness for e-gun evaporated HfO_2, b) V_{br} against dielectric thickness for atomic layer deposited HfO_2, c) J_{leak} against dielectric thickness for e-gun evaporated HfO_2 , and d) J_{leak} against dielectric thickness for atomic layer deposited HfO_2.

5 FET PERFORMANCE

5.1 PERFORMANCE OF LOW-K DIELECTRIC FETS

5.1.1 DC characterization

Initially the Polyimide FETs were measured. The specific devices have large Source Drain distance (4μm) thus exhibit large access resistance and low channel currents.

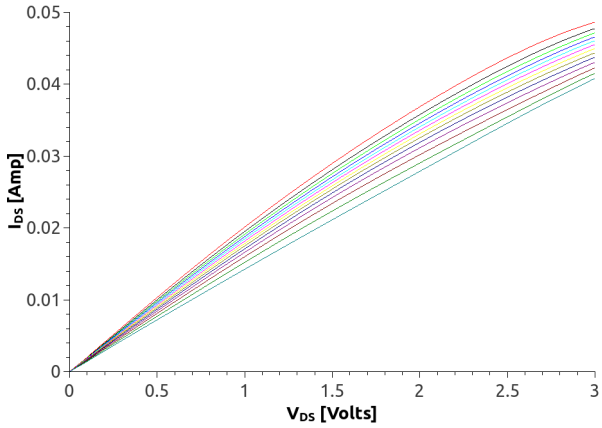


Figure 13: I_{DS} – V_{DS} sweep for various gate voltages (V_g step 5 Volts) showing the Polyimide 250nm gate dielectric performance in a graphene FET.

Although there is current control, the gate voltages required are very large due to the low-k nature of the dielectric and its large thickness.

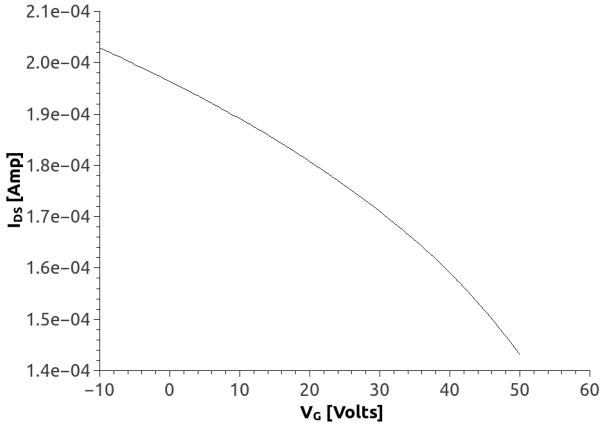


Figure 14: I_{DS} as a function of V_g (Dirac plot) at low V_{DS} showing the current control.

Attempting to reduce the polyimide dielectric thickness resulted in poor devices due toleakage of the gate dielectric. The following figures show the corresponding performance of devices with 40nm Polyimide dielectric.

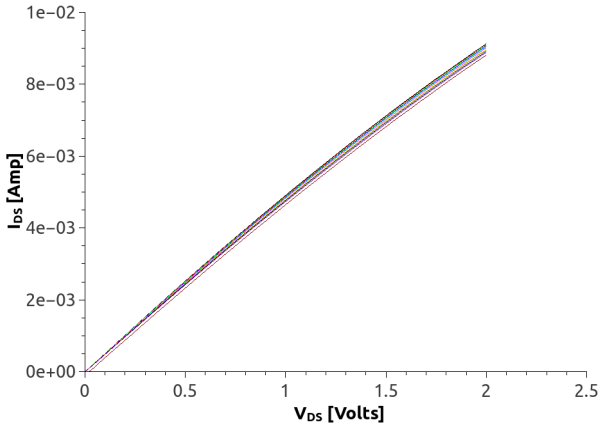


Figure 15: I_{DS} – V_{DS} sweep for various gate voltages (V_g step 0,1 Volts) showing the Polyimide 40nm gate dielectric performance in a graphene FET.

Poor current control within the limits of gate operating voltages were achieved. As shopwn below, the Dirac point is not accessible up to the gate breakdown.

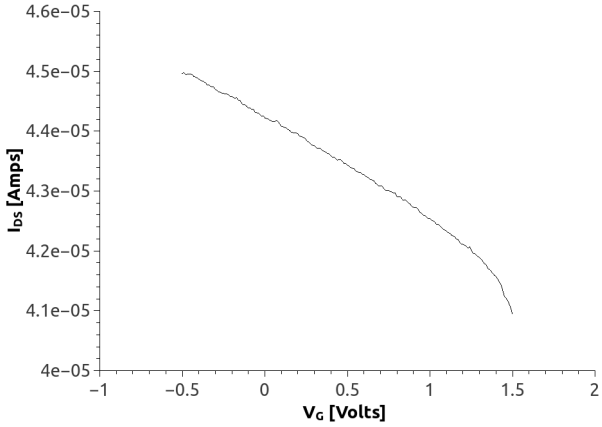


Figure 16: I_{DS} as a function of V_g (Dirac plot) at low V_{DS} showing the current control.

Finally the Si3N4 based FETs are shown below. All devices were fabricated using optically defined gates with size in the order of 1μm.

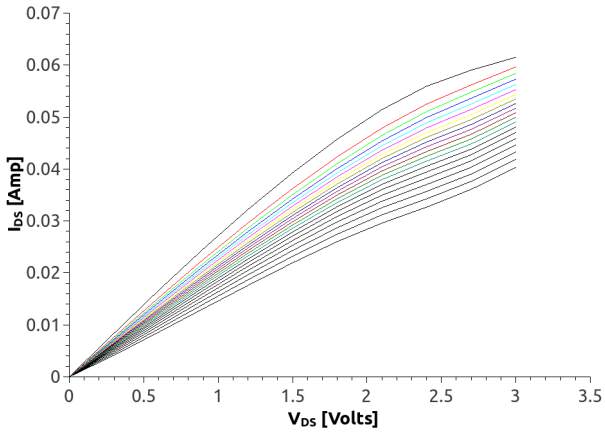


Figure 17: I_{DS} – V_{DS} sweep for various gate voltages (V_g step 0,5 Volts) showing the Si_3N_4 40nm gate dielectric performance in a graphene FET.

Good current control within the limits of gate operating voltages were achieved. The pseudo-saturation regions of the device was clearly evident showing the FET has good behavior. Access resistance is large due to large Source Drain separation (4μm). As shown in the Dirac plot below, there is marginally access to the Dirac point of the FET at voltages comparable to the breakdown.

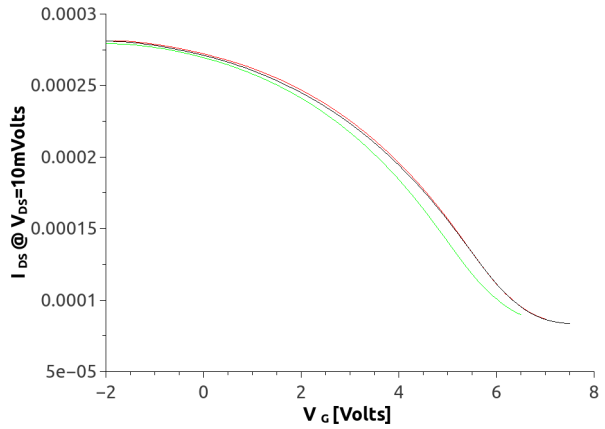


Figure 18: I_{DS} as a function of V_g (Dirac plot) at low V_{DS} showing the current control.

Finally using a new design of FETs with multiple finger topology and lower Source drain distances a new set of FETs was fabricated with Si_3N_4 gate dielectric. The gate metal work function was also tuned to improve the position of the Dirc point (closer to V_g=0).

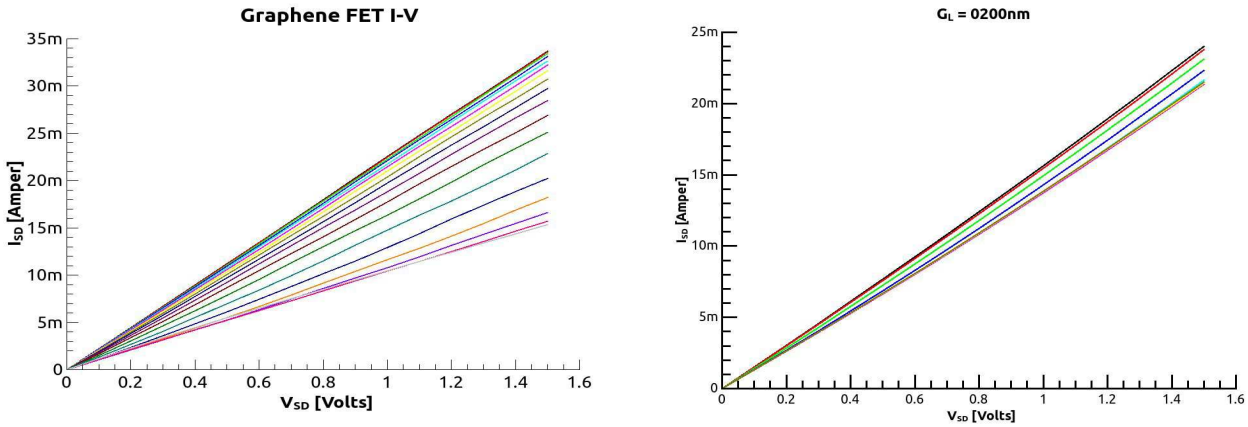


Figure 19: I_{DS} – V_{DS} sweep for various gate voltages showing the Si_3N_4 40nm gate dielectric performance in a graphene FET. The left plot corresponds to a wide (1μm) gate, the right plot shows similar devices but with a narrow (0.2μm) gate.

Good current control within the limits of gate operating voltages were achieved. The pseudo-saturation regions of the device was not evident Access resistance is much lower due to small Source Drain separation (~1μm). The loss of gate control when gate is downscaled is evident from the comparison. As shown in the Dirac plot below, there is good access to the Dirac point and both p and n type branches of the FET at voltages well below the breakdown.

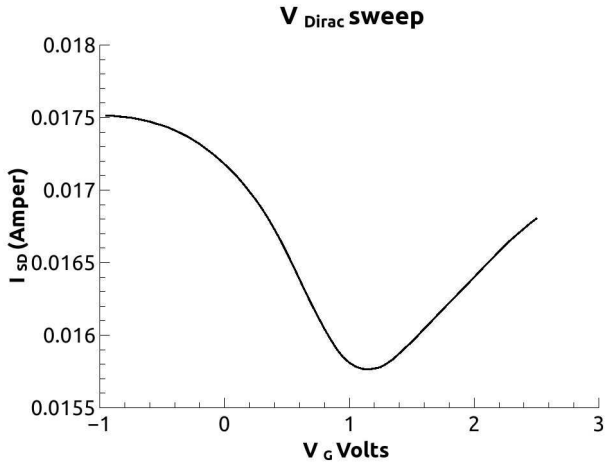


Figure 20: I_{DS} as a function of V_g (Dirac plot) at low V_{DS} showing the current control.

In the framework of that run, the first CNT FETs were also fabricated. The following figure shows the DC characteristics of a 2 finger device with 100μm wide gates (0.25μm gate length) and source drain distance 3.6μm.

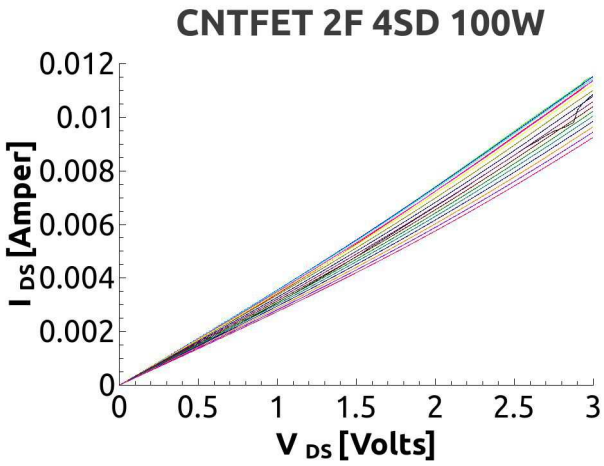


Figure 21: I_{DS} – V_{DS} sweep for various gate voltages (V_g step 0,5 Volts) showing the Si_3N_4 40nm gate dielectric performance in a graphene FET.

From the previous plot the transconductance map can be calculated showing that the gain increases for negative Vg values.

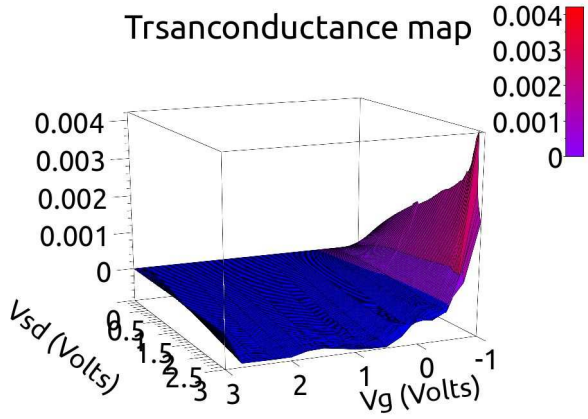


Figure 22: I_{DS} as a function of V_g (Dirac plot) at low V_{DS} showing the current control.

5.1.2 RF characterization

For the final run with Si_3N_4 RF measurements were also performed on graphene devices. In the following figures one of the best device performance is shown:

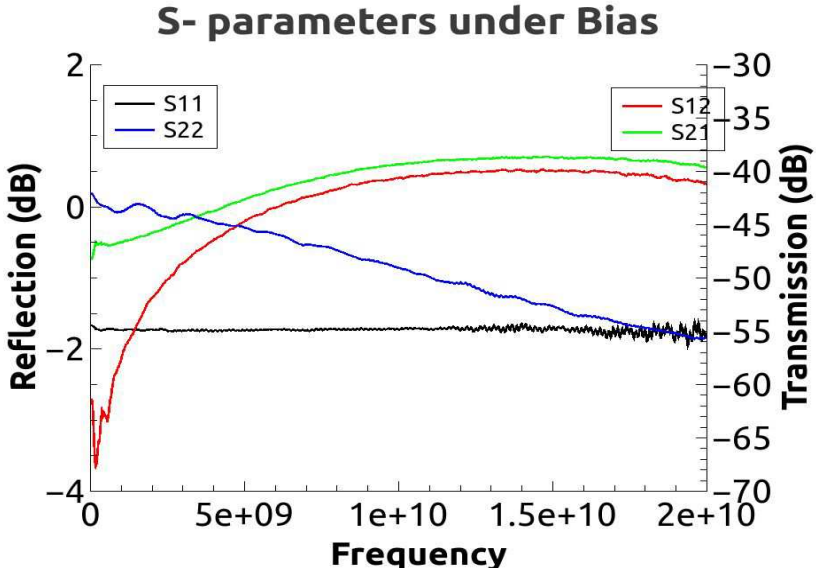


Figure 23: Non de-embedded S-parameter magnitude for a 2 finger device with gate width 100μm and Si_3N_4 gate dielectric under bias.

The transmission magnitude is still low (-38dB) however the device exhibits some amplification up to large frequencies.

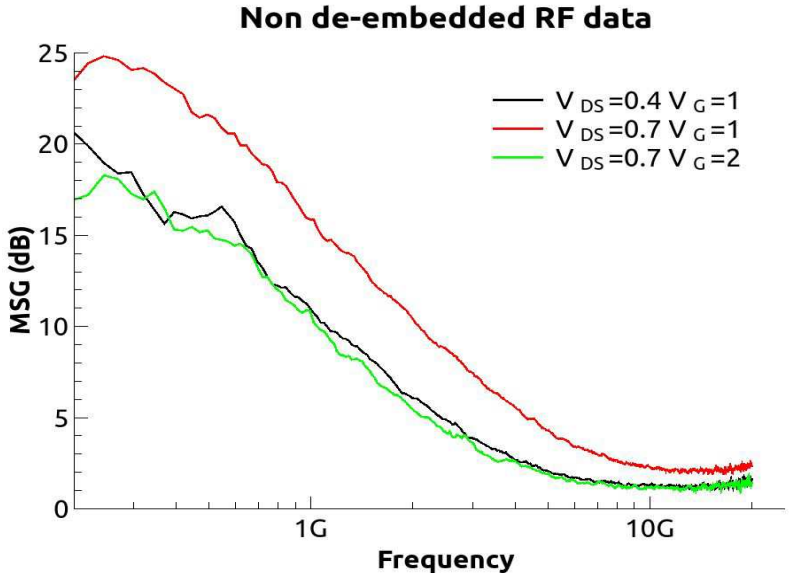


Figure 24: Embedded S21 / S12 ratio showing significant amplification up to ~5GHz.

5.2 PERFORMANCE OF HIGH-K DIELECTRIC FETS

5.2.1 DC characterization

5.2.1.1 Run 7 CNTFET

The following is a typical image of I-V characteristics of a HfO2 CNT based FET.

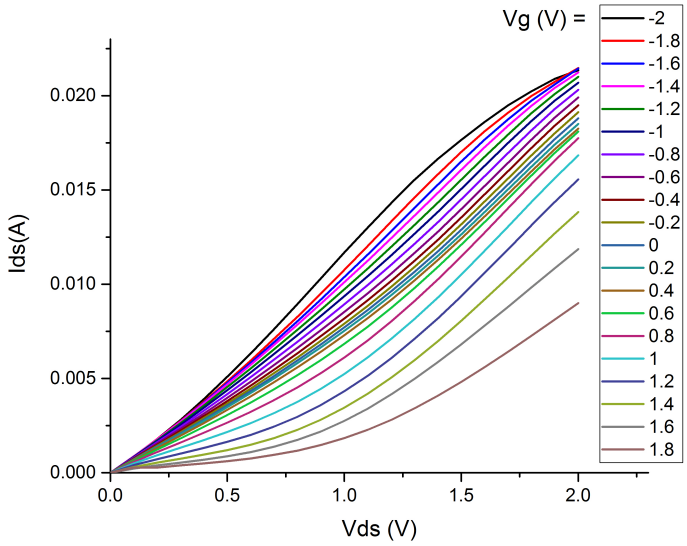


Figure 25: Typical behavior I_{SD} as a function of V_{DS} *for different* V_G *for FET 2F4SD030WB.*

Transconductance g_m was calculated from the slope of I_{SD} vs V_G at constant V_{DS}., following the formula: $g_m=dI_{DS}/V_G$.

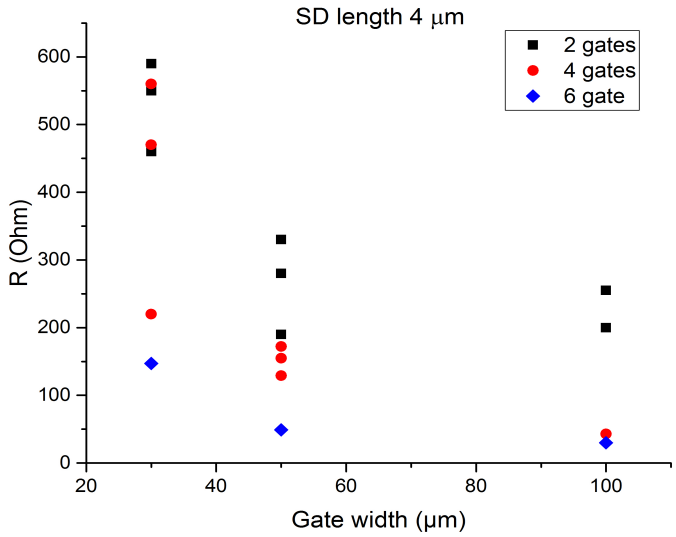


Figure 26: channel resistance as a function of gate width *for two gate (blue), four gate (green) and six gate (red) FETs.*

A large variation in attained characteristics is shown. Nevertheless it is clearly shown that long gates exhibit lower gm. This is a clear sign of gate resistance.

5.2.1.2 Run 7 GFET 609

This was the first attempt to realise Klein tunnelling inhibited graphene FETs. As shown clearly on the following image, the transconductance behaviour has drastically changes with maximum gm values at lower Vds values.

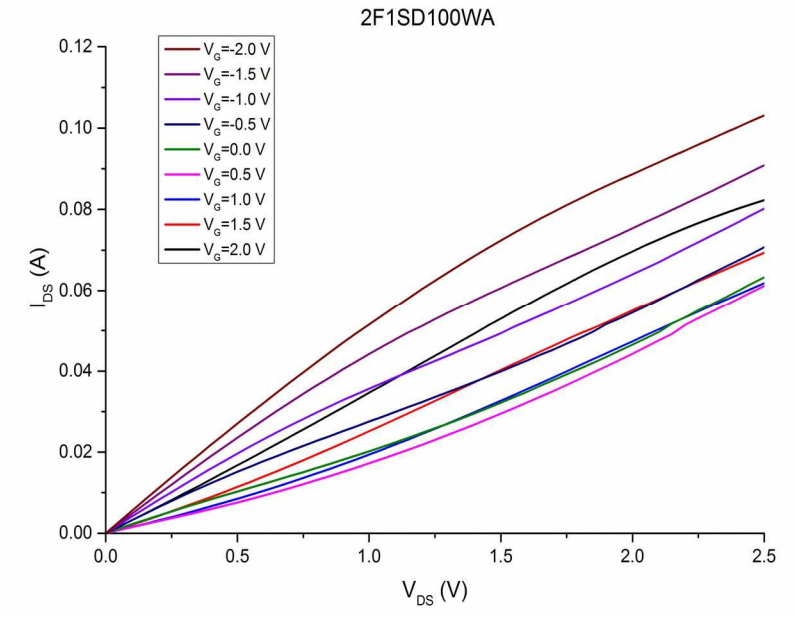


Figure 27: Typical behaviour I_{SD} as a function of V_{DS} *for different* V_G *for FET 2F1SD100WA.*

Transconductance g_m (Fig.2) was calculated from the slope of I_{SD} vs V_G at constant V_{DS}., following the formula: $g_m=dI_{DS}/V_G$.

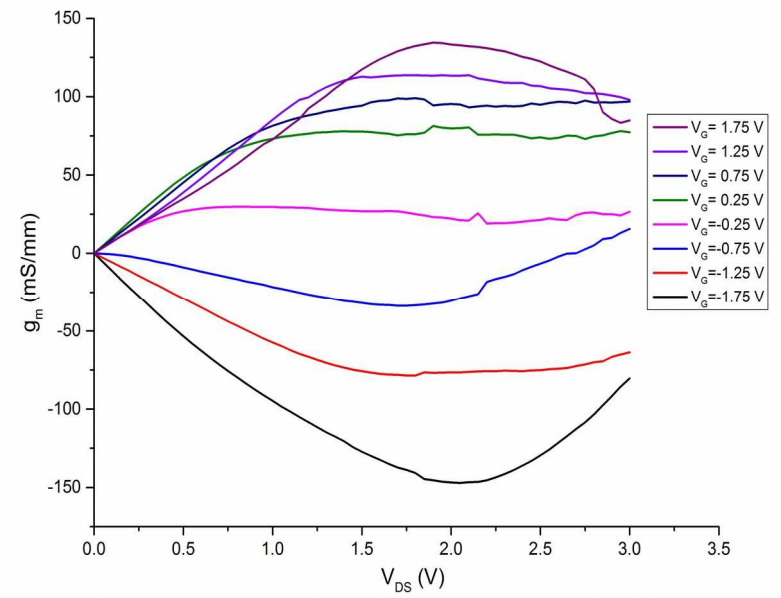


Figure 28: Transconductance g_m normalized to the channel size as a function of V_{DS} for different V_G *for 2F1SD100WA.*

5.2.1.3 Run 9 GFET 734

This run was focused at optimising source – drain distance to improve access resistance.

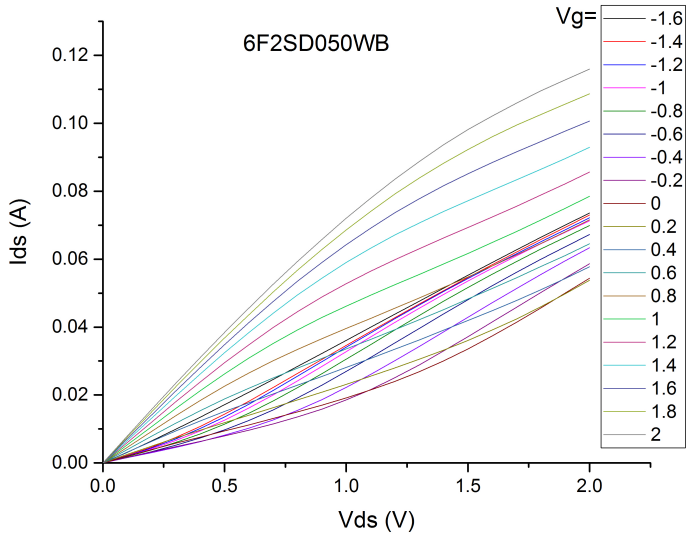


Figure 29: Typical behaviour I_{SD} as a function of V_{DS} *for different* V_G *for FET.*

Transconductance g_m (Fig.2) was calculated from the slope of I_{SD} vs V_G at constant V_{DS}., following the formula: $g_m=dI_{DS}/V_G$.

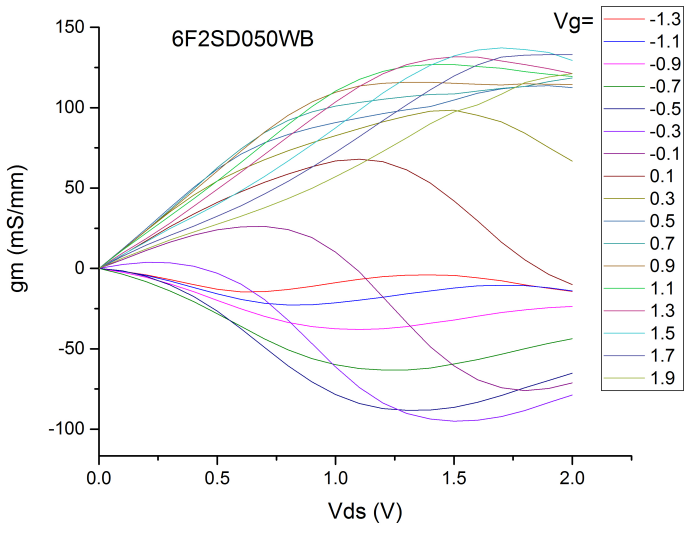


Figure 30: Transconductance g_m normalized to the channel size as a function of V_{DS} for different V_G

5.2.2 Low frequency characterization

The behaviour of the presented devices at very low frequency was characterised and is presented here.

5.2.2.1 Run 7 CNTFET

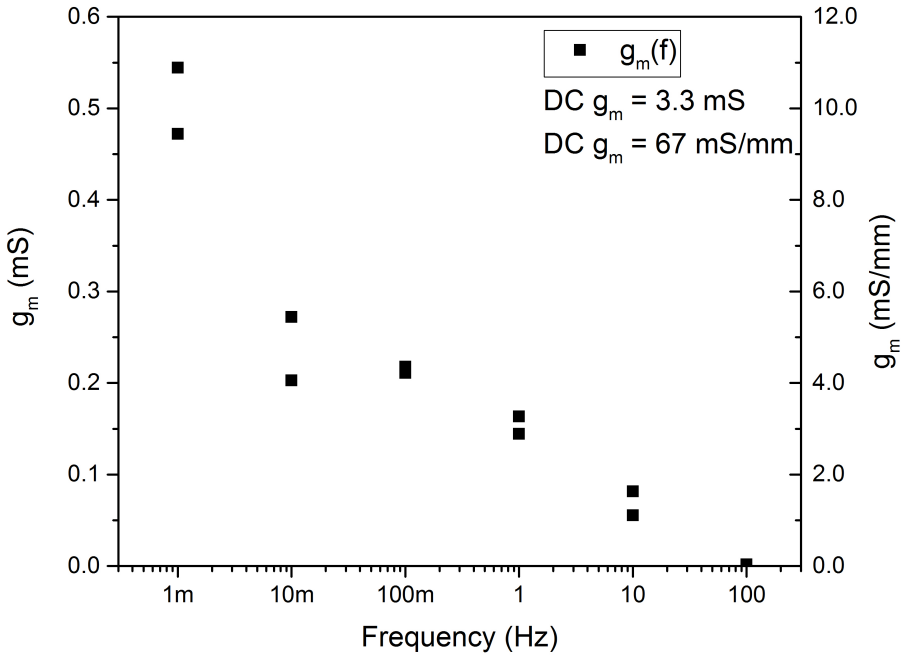


Figure 31: Transconductance g_m (left axis), normalized to *the SD width (right axis) as a function of* ΔV_{in} *frequency. Derivative value from DC measurements written for the reference. FET 6F2SD050WB.* ΔV_{in} *= 0.6Volts p-p.*

However the frequency dependence is still clear as the g_m values drastically drops even for a frequency as low as 10mHz.

Changing the R_L to improve accuracy and reducing ΔV_{in} to 60mVolts p-p leads to the measurements shown in the following figure.

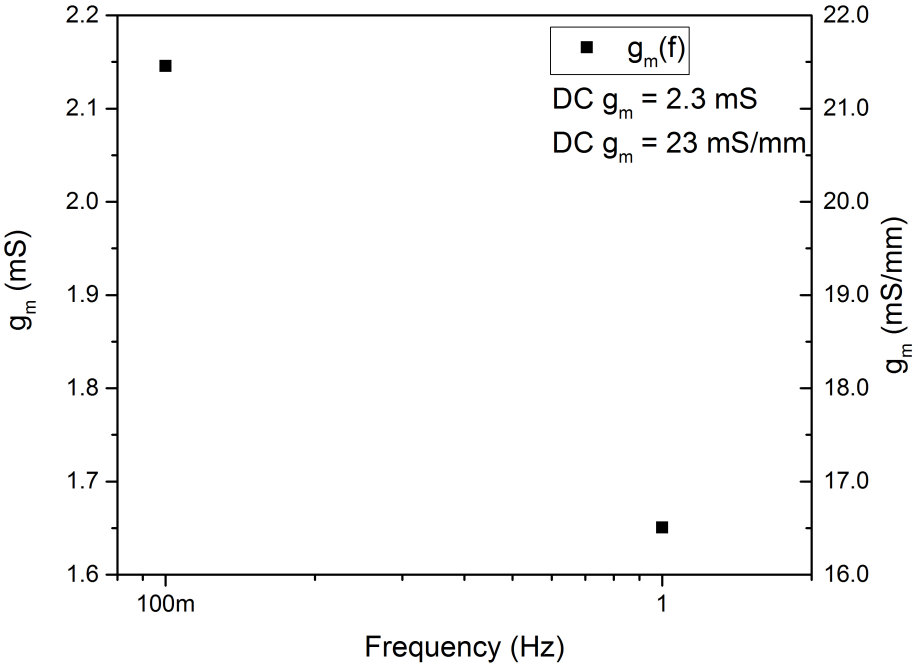


Figure 32: Transconductance g_m (left axis) and normalized g_m (right *axis) as a function of V_{in} frequency. Inset shows g_m from DC measurements written for reference. FET 2F4SD100WB.*

In order to characterize the characteristic time t_1 of the gate response, several gate charging/discharging cycles have been performed (Fig. 6) at constant Vds. From the slope of the Ids as a function of time, a characteristic time rate of the gate dielectric trapping/detrapping has been extracted. It should be noted that the discharging time is more then two times higher, than the charging time.

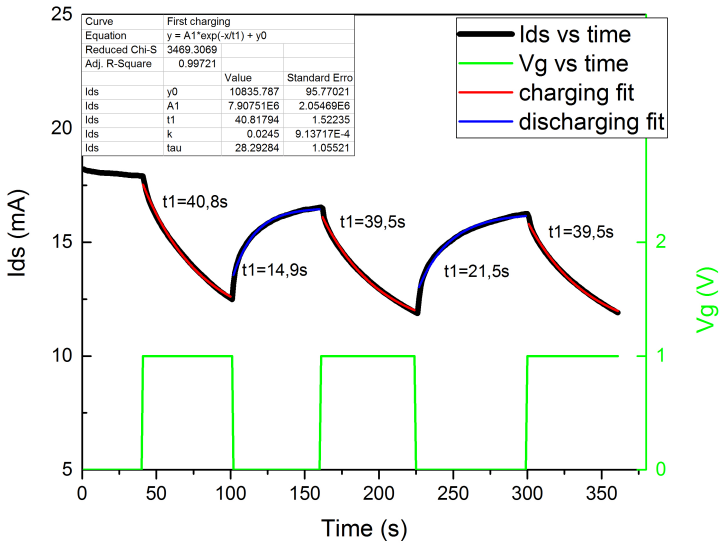


Figure 33: Drain-souse current Ids (black curve) and gate voltage Vg (green curve) versus *time. Charging and discharging slopes are fit exponentially (red and blue curves respectively) and characteristic time parameter t1 is shown near each curve. FET 2F1SD050WB bottom.*

5.2.2.2 Run 9 GFET 609

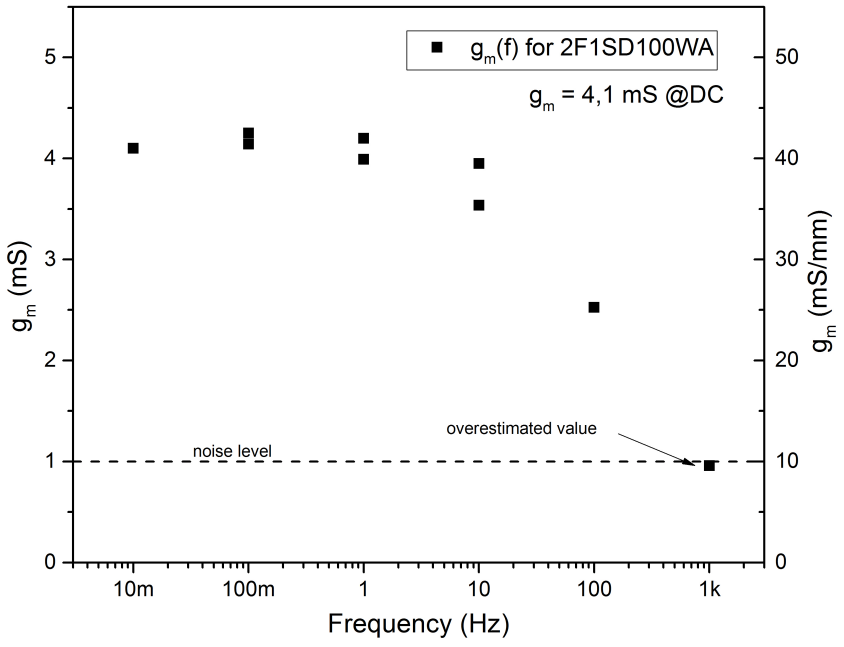


Figure 34: Transconductance g_m (left axis), normalized to *the SD width (right axis) as a function of* ΔV_{in} *frequency. Derivative value from DC measurements written for the reference. FET 2F1SD100WA.* ΔV_{in} *= 1 V + 0.1 Vpp,* V_{DS} *= 2 V.*

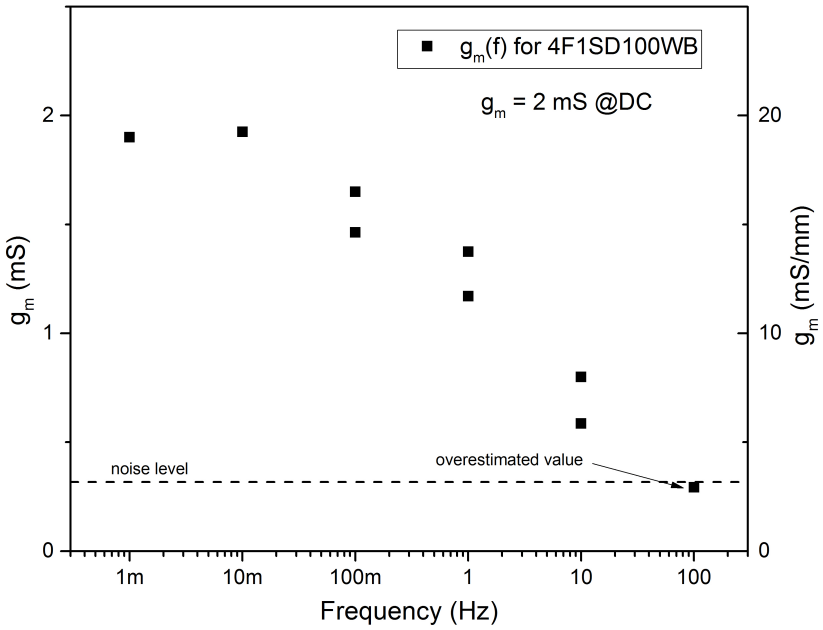


Figure 35: Transconductance g_m (left axis), normalized to *the SD width (right axis) as a function of* ΔV_{in} *frequency. Derivative value from DC measurements written for the reference. FET 4F1SD100WB.* ΔV_{in} *=1V+0.1Vpp,* V_{DS} *= 1 V.*

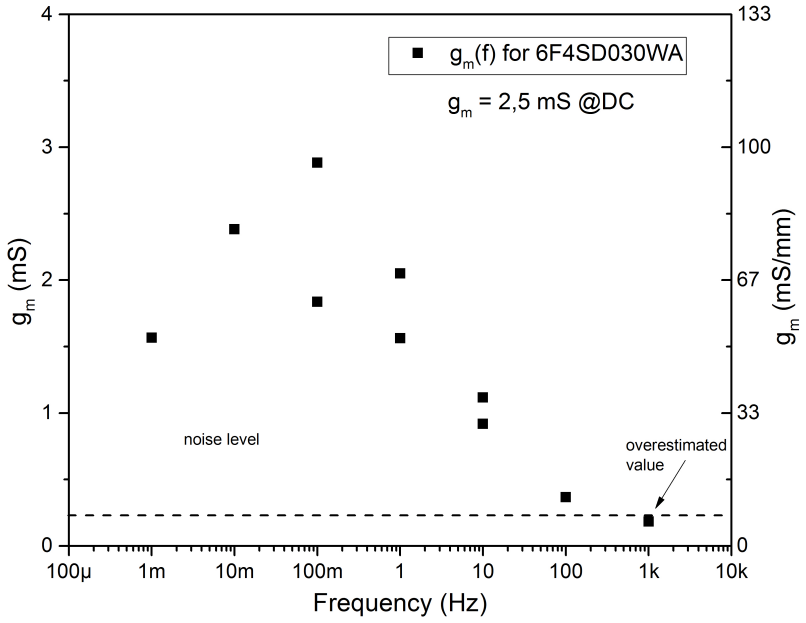


Figure 36: Transconductance g_m (left axis), normalized to *the SD width (right axis) as a function of* ΔV_{in} *frequency. Derivative value from DC measurements written for the reference. FET 6F4SD030WB.* ΔV_{in} *=1V+0.1Vpp,* V_{DS}*=2V.*

In order to characterize the characteristic time t_1 of the gate response, several gate charging/discharging cycles have been performed at constant V_{DC} = 1 V. From the slope of the Ids as a function of time a characteristic time rate of the gate dielectric trapping/detrapping has been extracted.

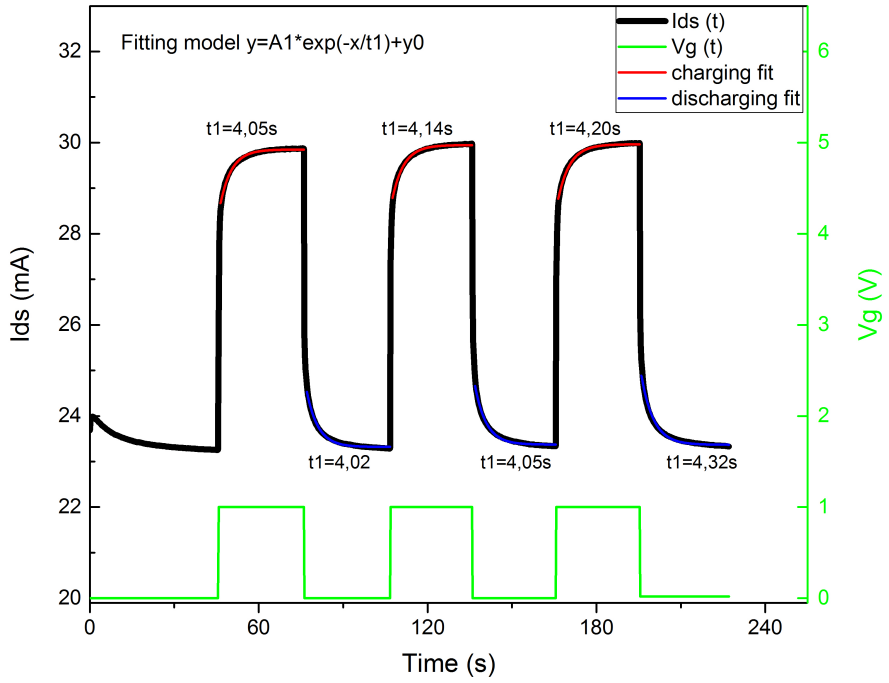


Figure 37: Drain-souse current Ids (black curve) and gate voltage Vg (green curve) versus *time. Charging and discharging slopes are fit exponentially (red and blue curves respectively) and characteristic time parameter t1 is shown near each curve. FET 4F1SD100WB, V_{DS} = 1 V.*

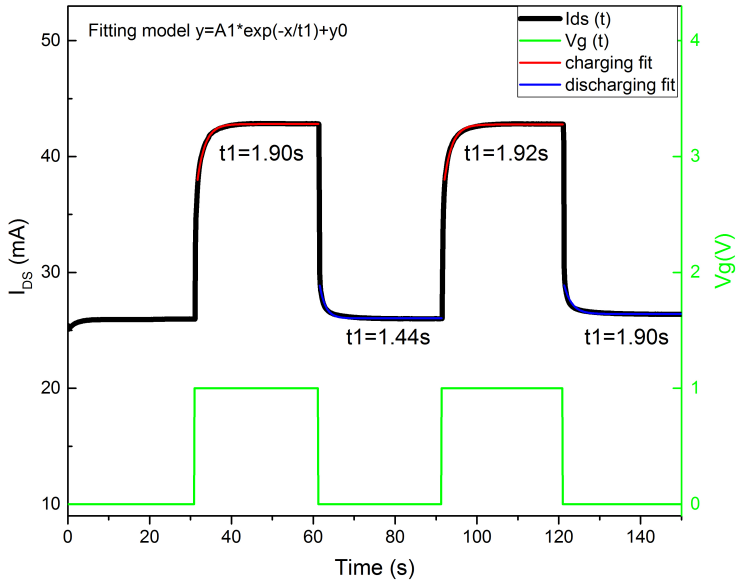


Figure 38: Drain-souse current Ids (black curve) and gate voltage Vg (green curve) versus *time. Charging and discharging slopes are fit exponentially (red and blue curves respectively) and characteristic time parameter t1 is shown near each curve. FET 6F4SD030WB, V_{DS} = 2 V.*

As evident from the above results, there has been a systematic gate lag effect in all high-k based FETs. Throughout the runs the following improvements have been incorporated into the main process flow:

1. High-k dielectrics (run 4)
2. Short source drain (run 7)
3. T-gate to improve gate resistance (run 9)
4. Optimised ohmic contacts (run 10)

The major issue that was not addressed is the gate lag evident in high-k FETs that hindered RF performance of the devices.

A brief overview of the obtained results are:

1. Graphene Gm > 120mS/mm
2. CNTFET Gm > 110mS/mm
3. Channel resistance ~Ohms in both technologies