CARBON BASED SMART SYSTEM FOR WIRELESS APPLICATION

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WORK PACKAGE 7 : Project management

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1 PROJECT OBJECTIVES AND MAJOR ACHIEVEMENTS DURING REPORTING PERIOD (T0+12 – T0+18)

According to the timetable (see Figure 1), the project objectives over the reporting period are:

- Within the framework of WP 2 'Design and simulation activities' : design and simulate all the CNTs and graphene based sub-components forming the nano T/R module to be demonstrated in WP5 comprising filters/oscillators, switches, mixers, LNAs and PAs and finally an antenna. The main technical objectives are:
  - Design and modelling of CNT and graphene based FET and then design and modeling of LNA,PA and mixer based on either CNT or graphene
  - Design and modelling of CNT switch;
  - Design and modelling of CNT filter/oscillator and graphene mixer
  - Design and modelling of CNT antenna.
  - Design and modelling of LNA based graphene
  - Design and modelling of a graphene loaded antenna.

- Within the framework of WP 3 'Fabrication activities': all the CNT and graphene based sub-modules that have been designed in the work package 2. The principal objective of this work package is to fabricate the test structures and also final components based on the results of WP2

- Within the framework of WP 4 'Test activities': the different manufactured CNT components will be tested, consisting of the following test:
  - CNT FET and graphene electrical characterization: DC to RF
  - CNT RF switch tests
  - CNT based filter/oscillator tests§ CNT based antenna tests
  - RF graphene device (LNA ,mixer, detector)
  - Calibration of basic equivalent circuit models (parameter extraction based on experimental data)

- Within the framework of WP 7 'Project Management' : to establish durable basis for the project management and monitoring all along the project duration, through the following actions:
    - Regular project and technical meetings;

As described in the following sections, all these objectives have progressed between T0+12 and T0+18.

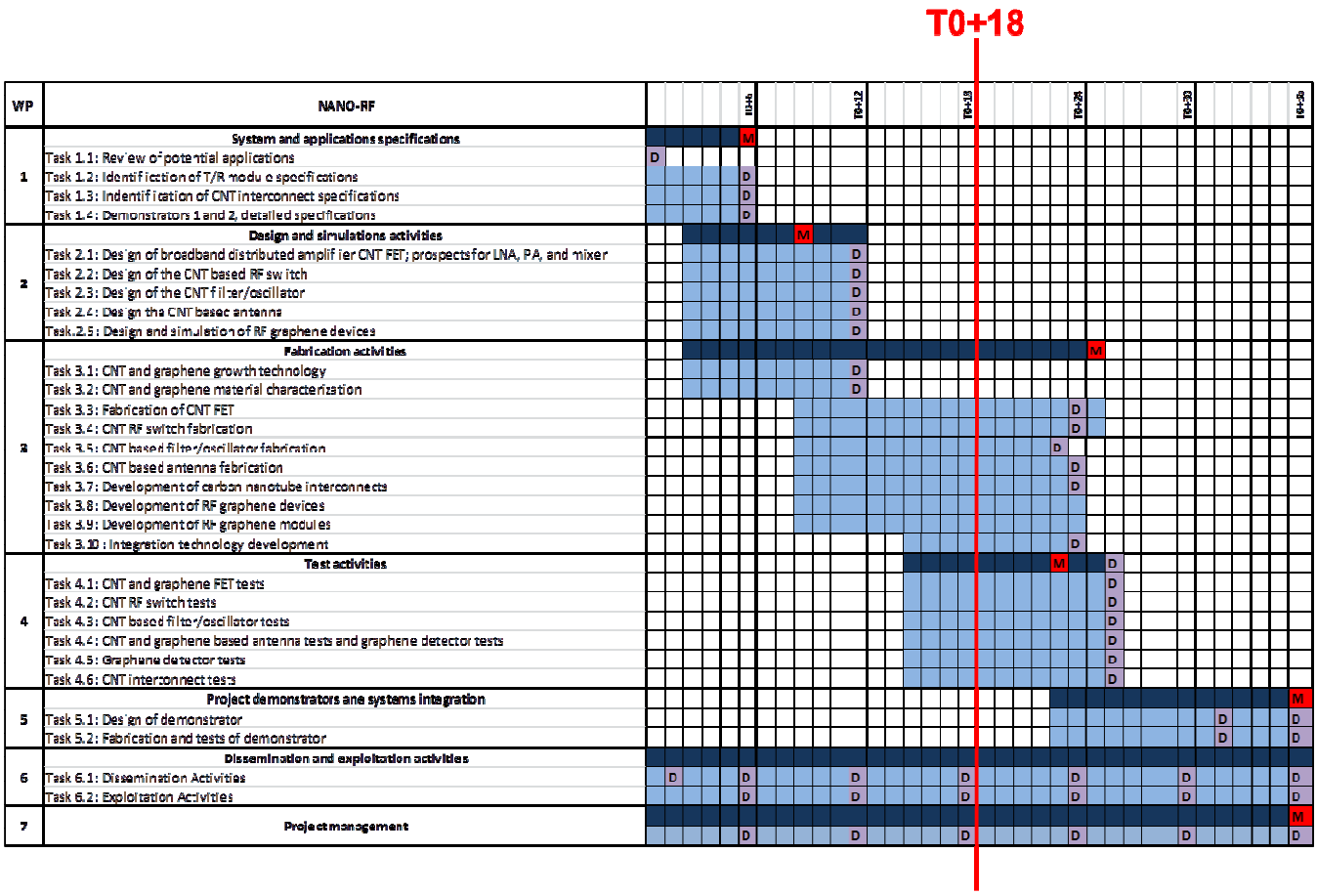


Figure 1 : NANO-RF Timetable

2 MANAGEMENT ACTIVITIES (WP7)

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
TRT	TRT, CHALMERS, FORTH, LAAS, IMT, TSA, SHT, UNIVPM, ICN, Tyndall	$T_0 – T_0+36$	D7.1 to D7.21 M7.1	-	**On-Going**

- **MEETING**

In order to ensure a correct progress and a high coherence of the collaborative project, during the reporting period, numerous meetings were organized:

- 2 project meetings, where all the partners are represented
  - 18-Month Meeting, held in Barcelona on 06th February 2014;
  - 21-Month Meeting, held in Bucharest on 27th May 2014;

- 1 technical meetings for WP 3, where only the partners involved in the given WP are represented:

- Technical Meeting, held in Brussels on 02st May 2014;

The agendas, minutes and presentations made for these meetings are downloadable on the private area of the website.

3 PROGRESS IN THE ACTIVE THECNICAL WORKPACKAGE 2

3.1 WP2 : DESIGN AND SIMULATION ACTIVITIES

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
IMT	TRT, UPMC, IMT, TSA, UNIVPM, LiU, ICN	T_0 +3 – T_0+12	D2.1 to D2.5 M2.1	T2.1 to T2.5	**On Going**

All the deliverables for WP2 are submitted at T_0+13.

Following the recommendation during the first review meeting, it was decided to do a re-modelling and re-design for all the five tasks in WP2 when feedback from WP3 and WP4 will be available. So WP2 is still on going.

3.2 WP OBJECTIVES

In this WP, we will design and simulate all the CNTs and graphene based sub-components forming the nano T/R module to be demonstrated in WP5 comprising filters/oscillators, switches, mixers, LNAs and PAs and finally an antenna. The main technical objectives are:

- Design and modeling of CNT and graphene based FET and then design and modeling of LNA, PA and mixer based on either CNT or graphene
- Design and modeling of CNT switch
- Design and modeling of CNT filter/oscillator and graphene mixer
- Design and modeling of CNT antenna
- Design and modeling of LNA based graphene
- Design and modeling of a graphene loaded antenna.

3.3 PROGRESS TOWARD OBJECTIVES : STATUS OF ACTIVES TASKS

3.3.1 Task 2.1: Design of broadband distributed amplifier CNT FET (LAAS/UNIVPM/IMT)

- **<u>Simulation of Single and multi-wall CNT FET</u>**

The multiband carrier transport (Schrödinger equation) and the electrostatic potential (Poisson equation) throughout the device are simultaneously solved by numerical iteration (Figure 2).

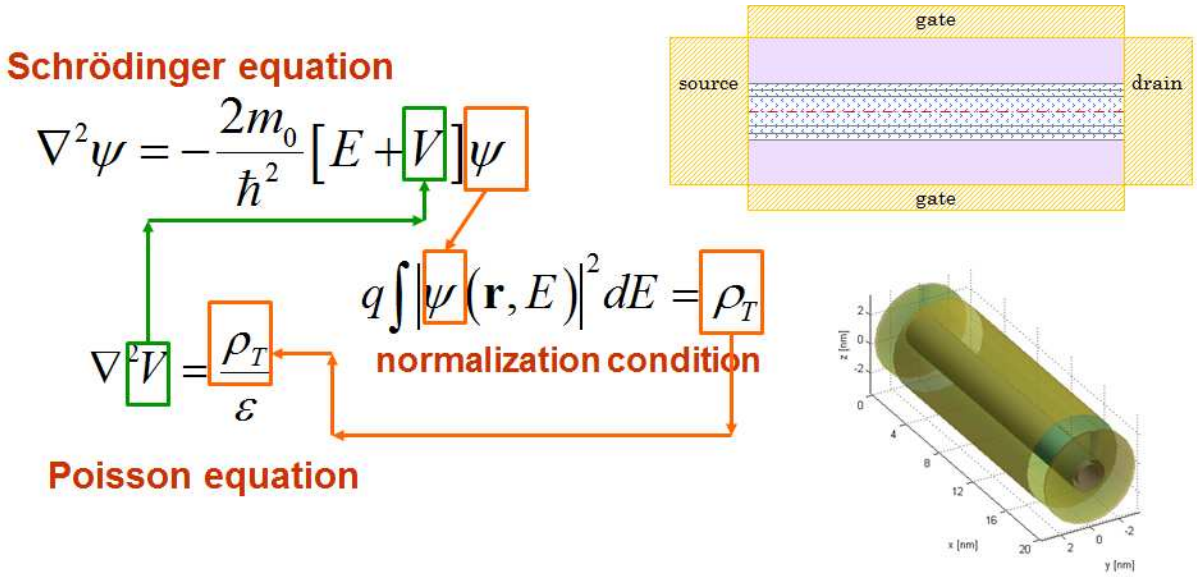


Figure 2 The solver is based on the simultaneous solution of the Schrödinger (carbon nanotube-based FETs) equation and the Poisson equation. The em field provides sources terms for the quantum transport equations, that, in turns, provides charges and currents for the em field.

The solver allows the control of geometry (channel size, gate radius), as well as quantistic parameters (number of electronic bands, transfer energies among carbon atoms, etc.), electrical parameters (applied voltages, electrical permittivity of the medium around CNT, etc.), and numerical parameters (space refinement in the CNT for Schrödinger solution, energy refinement in calculating the current and charge integrals, the number of modes in potential solution, etc.).

- **Simulation of CNT-array FET**

It is reasonable assumed that the mutual CNT interaction is almost negligible: in practice, it is possible to simulate an array by integrating the results of the individual CNT as if they were separately gated (see Figure 3).

An equivalent lumped circuit model of the CNT-FET is made available after the simulation. The following qualitative key issues stem from the quantitative analysis:

- Simulating CNT transistors of different length shows that, in the ballistic regime, the length of the CNT channel just slightly affects the I-V characteristics.
- The transconductance increases with the CNT diameter, the number of walls, and, in case of a CNT-array-FET, the number of CNTs.
- In general, the quantum capacitance of a CNT has a small impact in the unit-gain frequency of the transistor, because the electrode capacitance dominates: however, increasing the number of CNTs in a large CNT-array-FET may reduce the operation frequency-range.

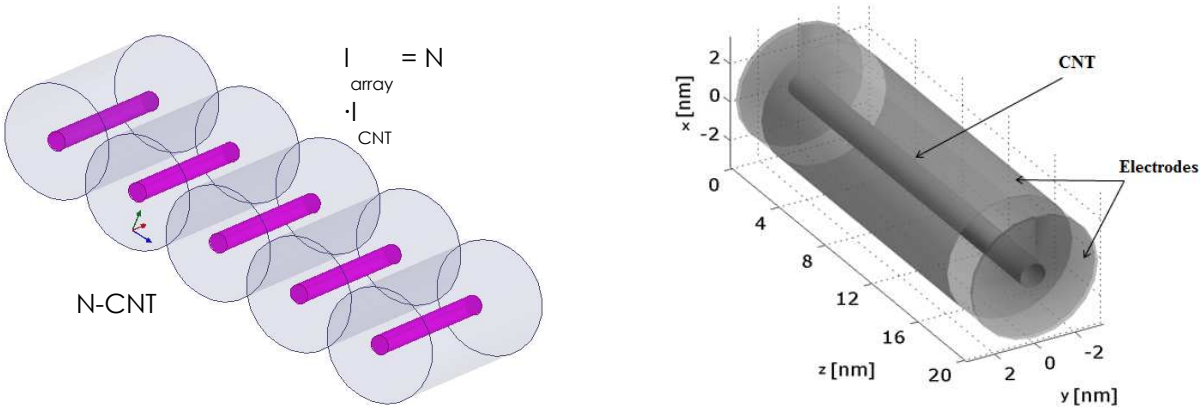


Figure 3 : CNT-FET (right), and CNT-array-FET (left).

3.3.2 Task 2.4: Design the CNT based antenna (UPMC/UNIVPM)

A considerable size reduction of integrated antenna structures may be achieved using CNTs: the resonating length of a dipole, at THz frequencies, is almost 10-100 times lower than a metallic wire antenna and the input impedance is some order of magnitudes higher. Simulations are carried out by a home-made solver based on the Method of Moment (MoM).
The radiation efficiency of a CNT antenna is much lower than that of a resonating metal dipole.
The analytical results are successfully compared with HFSS and CST simulation results.

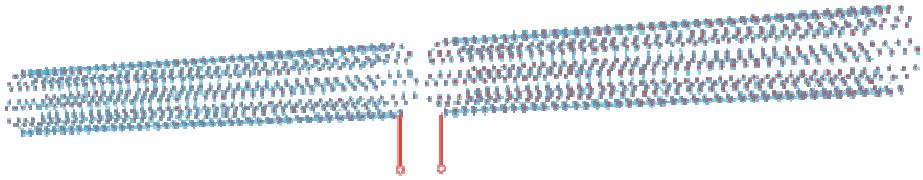


Figure 4 : A CNT wire antenna

3.3.3 Task 2.5: Design and simulation of RF graphene devices (UIMT/UNIVPM)

- **Analysis and synthesis of graphene-patch antennas**

In the microwave and mm-wave range, graphene is modeled as an equivalent surface conductivity tensor. EM simulations have been performed by using HFSS. We show that the graphene patch can act properly as an antenna, i.e. with a significant radiation efficiency (for instance > 40%), if the graphene surface sheet is equal or less than 10 Ohm, which is on the border of the values predicted theoretically; the latter condition is likely to be matched only by defect-free graphene patch and with a high uniform voltage Bias (Fermi level shifted by >1eV). The radiating element is shown here below:

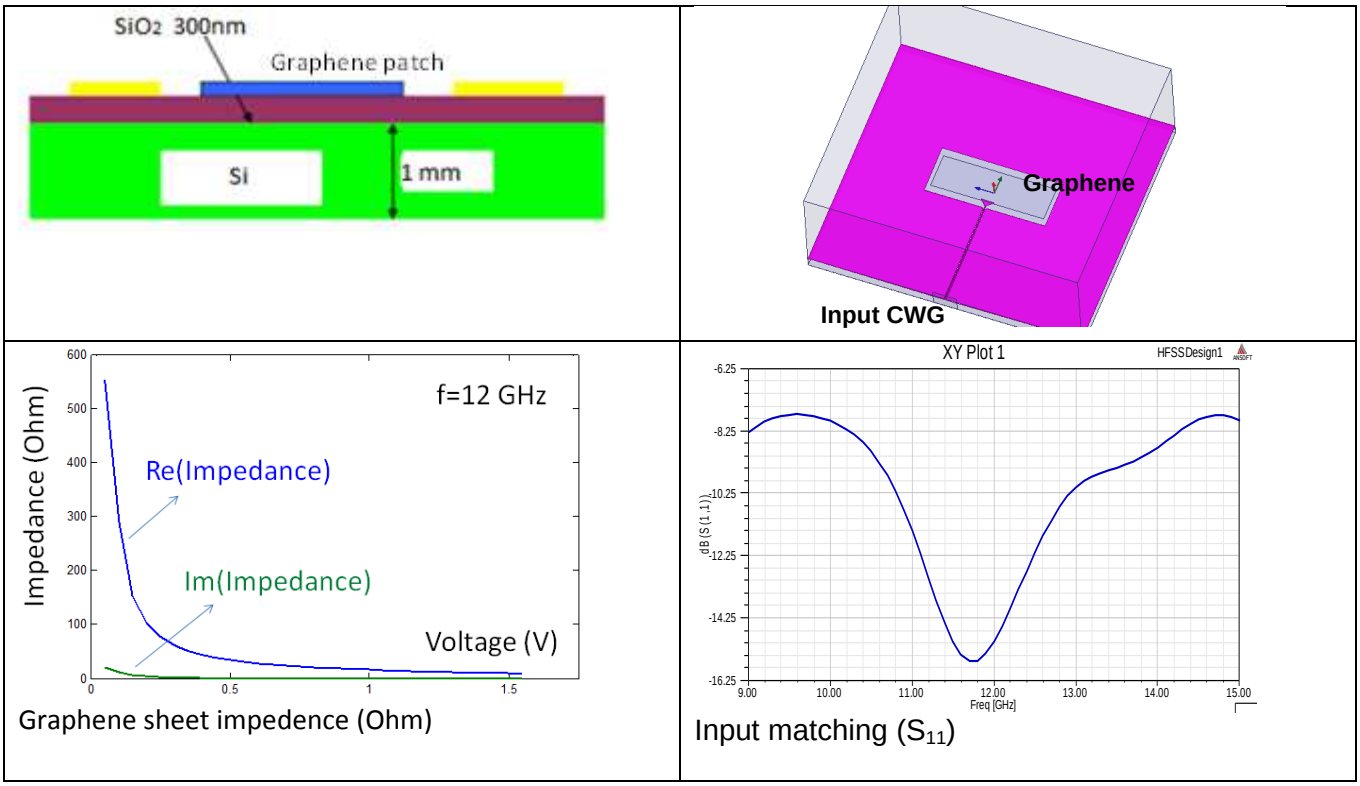


Figure 5 : Up in the figure: Graphene antenna. Down: graphene surface impedance (a), as a function of the applied voltage V, with a fixed frequency. (b). Reflection coefficient of the optimized antenna.

The predicted advantages of the proposed antenna reside in the following aspects:
i) tunability of the antenna parameters, like radiation pattern, resonant frequency, directivity, efficiency;
ii) tunability of the e.m. coupling between different radiating elements, and (then) of the array pattern of an array of graphene patches;
iii) possible reduction of the in-plane size of the patch owing to the slow wave" behavior (kinetic inductance contribution);
iv) integration: in future, a new class of high performance carbon components will be hopefully integrated in the same circuit (amplifiers, switches, mixers, attenuators, etc.).
As an alternative strategy for increasing the sheet resistance, following the literature, where a value of 30 Ohm is reported for a four-layer graphene, the use of a few layer graphene (FLG) may be, in our opinion, a potential solution to the graphene antenna. In this case the price to pay is given by the reduced tunability of the sheet resistance.

The synthesis of a broadband sub-array antenna (Figure 6), made of four radiation elements, has been carried out by properly designing a CWG feed network: this includes the synthesis of the individual components, i.e. a 90° bend and a CWG po wer divider (''T'' junction). Geometry constrains are imposed to obtain narrow-beam broadside operation: the elements spacing is lower than the e.m. wavelength in air (no grating lobes), and radiation of each element in phase (same electrical path from the input CWG port to the patches).

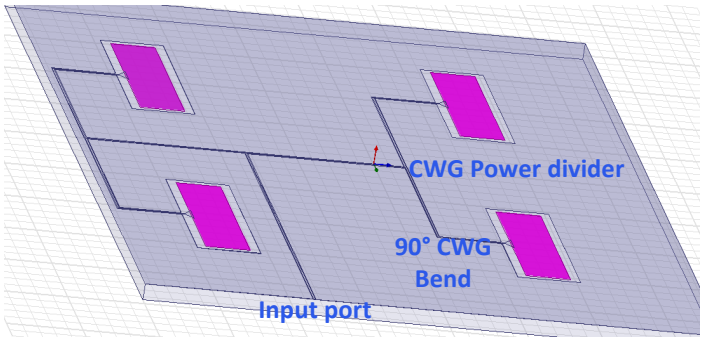


Figure 6 : Design of a 2x2 (four element) sub-array made of graphene patches.

- **Analysis of e.m. response of graphene**

A fundamental question: is it possible to tune, by means of an external voltage, the power dissipated/reflected in graphene irradiated by e.m. fields?
This is assessed by the analysis of the radiation of a real antenna, e.g. a half wavelength wire antenna, placed very close to a graphene patch (Figure 7). A rigorous Green's function approach is analytically implemented. Results show that the patch can be in fact tuned in order to provide microwave reflection, when the sheet resistance goes down to few tens Ohms, or to provide significant microwave absorption, when the graphene is not electrically Biased. Applying a magnetic Bias leads to the appearance of strong peaks of absorptions at certain Bias values.

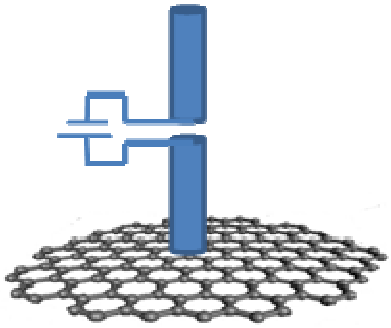
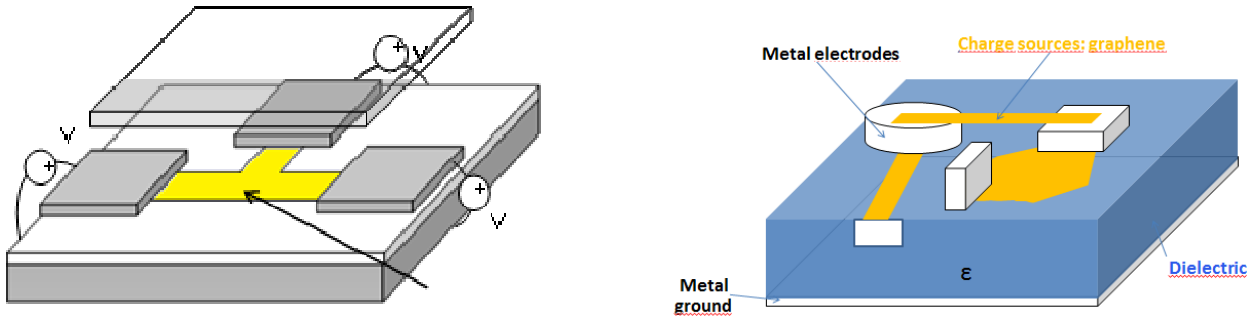


Figure 7 : Wire antenna over a graphene patch.

- **Development of a full self-consistent Dirac-Poisson simulator for i) graphene/GNR FET, ii) GNR circuits**

The quantum transport is described by the Dirac equation.



(a) (b)

Figure 8 : General GNR-FET like device (a), with, possibly, many ports for charge injection; full 3D Poisson solver: typical configuration (b).

As depicted in Figure 8(a), many branches and ports GNR-devices are simulated by our solver, with a wide variety of possible applications, e.g.: multiport GNR circuits, scattering by lattice defects, change in width in cascade GNRs, crossing GNRs, T-junctions, metal-carbon contact, field coupling among GNRs

Moreover, a novel, optimized full-3D Poisson solver has been recently developed and inserted in the main code. It is possible to deal with realistic 3D devices with high geometrical/electrical aspect ratios, involving: ground planes, metal electrodes, charge sources (graphene/CNT) etc. (Figure 8(b)). The shape of electrodes can be arbitrary, as well as the shape of (2D-3D) charge sources.

4 PROGRESS IN THE ACTIVE THECNICAL WORKPACKAGE 3

4.1 WP3 : FABRICATION ACTIVITIES

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
FORTH	TRT, CHALMERS, FORTH, LAAS, UPMC, IMT, GI, SHT, LiU, ICN, Tyndall	T_0 +3 – T_0+25	D3.1 to D3.8 M3.1	T3.1 to T3.10	**On Going**

D3.1 and D3.2 are submitted at T_0+13.

4.2 WP OBJECTIVES

In this work package we will fabricate all the CNT and graphene based sub-modules that have been designed in the previous work package. The principal objective of this work package is to fabricate the test structures and also final components based on the results of WP2. The manufacturing process in this WP will be optimized and the products will be delivered to WP4. The technical objectives for this work package are:

- To develop CNT growth technology to achieve the desired structure following results of the design activities. CNT growth must be compatible with all the substrate technology to achieve the desired RF components as specified in Work-package 1.

- To develop graphene growth techniques either based on exfoliation for proof of concept RF graphene devices and at the wafer scale for graphene circuits to be used in the sub-modules

- To set-up a pilot line for manufacturing CNT for microwave applications.

- To fully characterize the CNT that have been grown by thermal CVD or plasma enhanced CVD . The characterization of graphene via exfoliation or epitaxial growth on SiC. The goal will be to verify that physical, structural, etc. properties will be compatible with the RF functions we want to achieve.

- To fabricate the RF submodules designed in the previous work package: CNT FET (LNA, PA and mixer), the RF switch, the RF filter/oscillator and the antenna, LNA based on graphene, graphene antenna , graphene mixer and graphene detector

- To develop various technologies that will allow for the integration of the sub-modules produced within this work package to be integrated on a single Si carrier wafer.

- To supply other work packages with CNT and graphene for characterization, modeling, simulation and demonstration and to optimize CNT and graphene according to their feedbacks.

4.3 PROGRESS TOWARD OBJECTIVES : STATUS OF ACTIVES TASKS

4.3.1 Task.3.1 : CNT and graphene growth technology

There are several ways to obtain graphene material and we started to study the different graphene synthesis methods.

- **<u>Graphene CVD growth on metals (SHT/CHALMERS)</u>**

Thermal chemical vapor deposition (CVD) method was employed for fabrication of graphene. During the period reported, we have developed a bubbling transfer process to transfer graphene from catalyst to target substrate. By doing this we can greatly decrease the contaminates during the transfer process so that higher quality of graphene material can be obtained. The improved transfer process is illustrated in Figure 9.

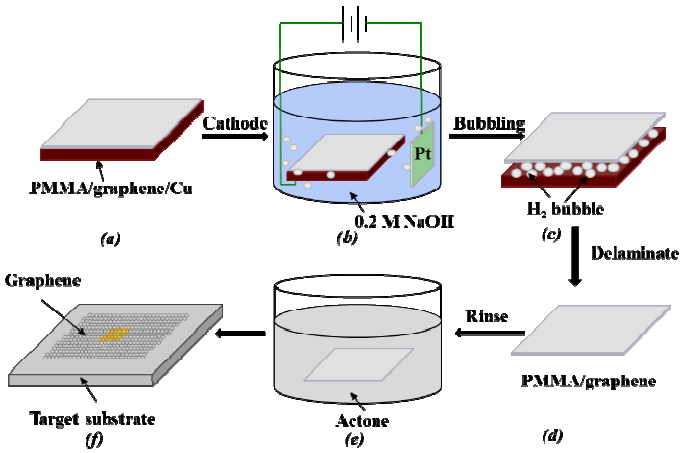


Figure 9 : Illustration of the bubbling transfer method making reuse of the Cu

Our experiment result showed good separation rate which is typical 1-2 minutes for a 12mm PMMA/graphene/Cu sample, while the traditional chemical etching method on the same area costs a few hours.

We have also measured the Raman spectrum of graphene after the transfer process. As shown in Figure 10, after the transfer process the intensity ratio of D to G peak is higher than that of before transfer process, this means there are some defects introduced after transfer, but it is possible to decrease bubbling to decease the defects which will be further investigated in the future.

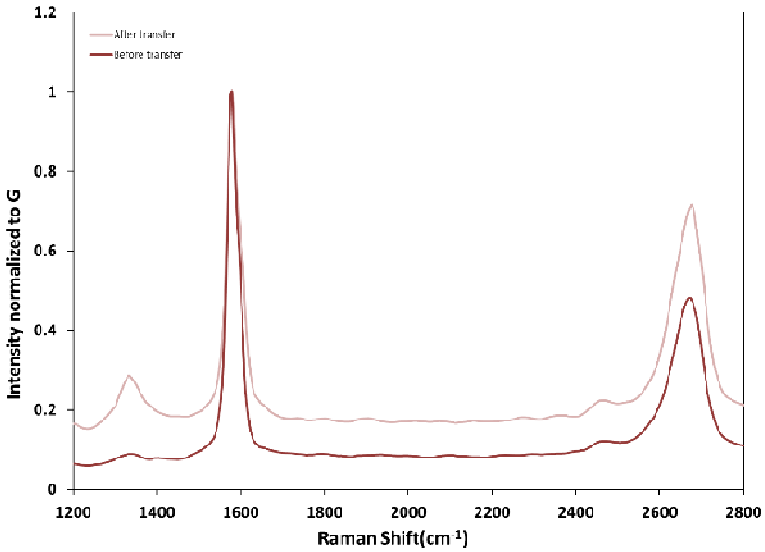


Figure 10 : Raman spectrum of as synthesized graphene after being transferred onto a Si with 300 nm SiO2 substrate

- **SiC decomposition (LiU)**

During the period reported, we have considered the following issues:

(1) Growth process and feedback characterization;
(2) Substrate polytype;
(3) Pre-growth surface preparation;
(4) Post-growth treatment;
(5) Effect of ambience conditions.

o Growth process and feedback characterization

For epitaxial graphene fabrication on SiC we use unique growth process proposed by R. Yakimova and described in a pending patent filed by the support of a previous SSF project. Key issues are not only the temperature of 2000℃ in combination with the assistance of Ar gas but also the temperature ramp up and ramp down conditions. This development has been made during the reported period which resulted in improved thickness homogeneity and most importantly it allows to controllably obtaining required thicknesses.

On Figure 11 a 2inch wafer with graphene is shown.

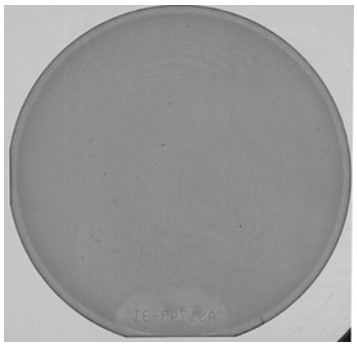


Figure 11 : 2 inch Graphene wafer

Typical LEEM image showing graphene samples with predominantly 1ML and 2MLs (as was required) are displayed in Figure 12a and Figure 12b, respectively. Furthermore we have elaborated process conditions for growth of graphene on the carbon face of SiC substrates. While graphene on Si face of SiC grows epitaxially and experiences the substrate charge transfer, graphene on the C-face does not grow epitaxially and is decoupled from the substrate. However, the lateral thickness homogeneity is inferior to the Si-face graphene and for this reason no approved applications have been demonstrated yet. Nevertheless it is of interest to elucidate the growth mechanism in order to be able to control domain size and orientation [2].

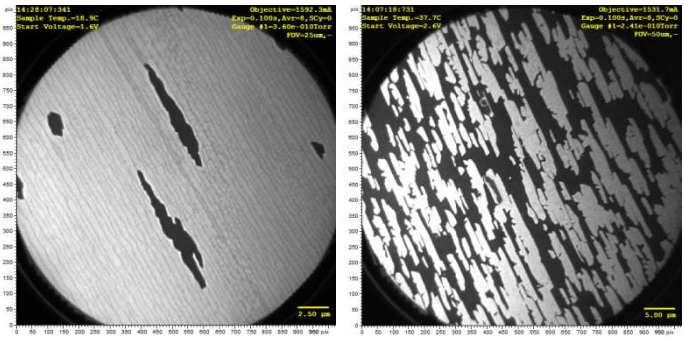


Figure 12 : LEEM images of a) 1ML graphene (white area) with islands of 2MLs (few % only); b) About 70% of the sample is covered with 2monolayers (white area).

Substrate polytype

We have shown that the self-contained phenomenon of step bunching during sublimation (thermal decomposition) of SiC substrates is a crucial factor for properties homogeneity of epitaxial graphene, e.g. monolayer thickness, carrier concentration and mobility [3, 4] because of existence of step edges. Without going into details, which can be found in Ref. [5] we will stress the main findings in this study:

Step bunching is different in three different SiC polytype – it is to a largest extent in 4H-SiC, less in 6H polytype and is minor in 3C-SiC provided the crystal is free of extended defects. From this point of view cubic (3C) SiC would be an ideal substrate for graphene growth having in mind also that there is no internal polarization in a cubic crystal, which would diminish substrate charge transfer. Figure 13 illustrates the difference in graphene thickness uniformity on different substrate polytypes. 98% of 1ML graphene on 3C substrate is a record value world wise. Graphene on 3C SiC on cm scale was studied by ellipsometry [6].

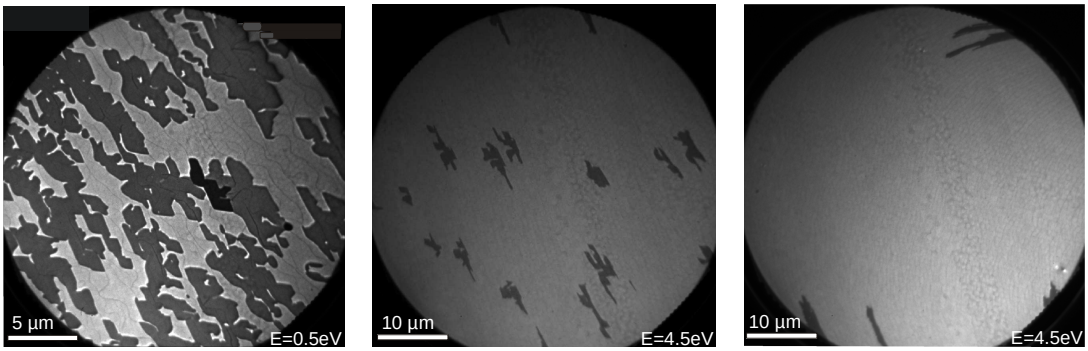


Figure 13 : LEEM images of graphene (from left to right) grown on 4H-, 6H- and 3C-SiC substrates respectively. Dark areas are patches of 2 MLs graphene while the rest is 1ML.

There are two obstacles to be overcome before we can really employ 3C substrates and that is (i) lack of commercially available substrates and (ii) lack of SI material.
It is worth noting that to date the best quality substrates in terms of low defects and resistivity required by electronic devices are of 4H-polytype. Taking this in consideration we have tuned the growth process in a way to reach good graphene thickness uniformity, as for example shown in Figure 12a.

Furthermore we have accomplished growth of 1ML graphene one 2inch 6H-SiC wafer for processing of high frequency transistors. The thickness of graphene was affected by structural defects present in the wafer (Figure 14)

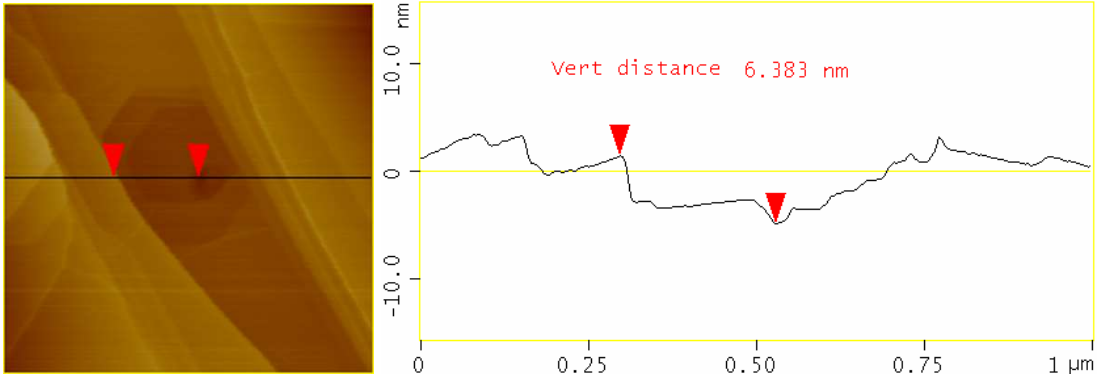


Figure 14 : AFM images of uneven surface morphology of graphene on 6H-SiC wafer and the line profile showing severe effect of a micropipe (right arrow).

Pre-growth surface preparation

Figure 15 demonstrates the effect of polishing scratches on graphene thickness. A variety of thickness may be observed. A solution of this issue is commonly approached by doing pre-growth hydrogen etching which is a standard procedure in SiC epitaxy. However the consequence is not unambiguous:

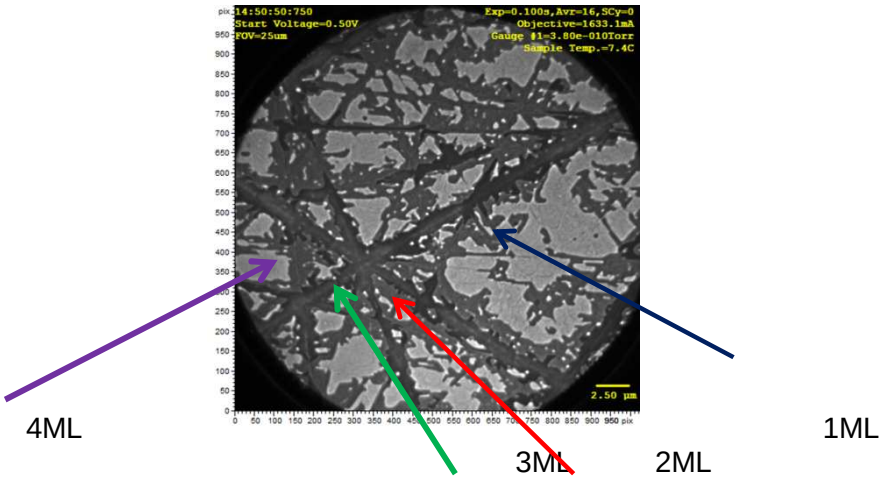


Figure 15 : A LEEM image: Remaining of polishing scratches (dark lines) after graphene growth on a 6H-SiC substrate purchased from SiCrystal and graphene with different thickness.

- Hydrogen etching is known to result in step bunching and therefore the step height during graphene formation may be increased.
- Hydrogen atoms may not be completely removed from the surface which will result in more complex graphene growth mechanism.
- This treatment requires Hydrogen gas supply which needs all safety rules to be fulfilled and brings an additional risk in the lab.

We have built up an etching module which employs sublimation etching in which no foreign agents are used. The etching can be controlled to a level of atomic steps (0.25 nm for SiC) over the whole substrate area. The setup has a capacity of etching up to 2 inch in diameter wafers and is fully compatible with the graphene growth process. We have done a series of etched samples under varying conditions in order to reach an optimized regime for atomically flat surfaces. Figure 16 depicts an optical reflectance map of graphene grown on an etched substrate. The second monolayer here is arranged along the steps and has a minor area compared to 1ML. If one compares with the image in Fig. 4, there is a significant benefit in the case of scratch elimination.

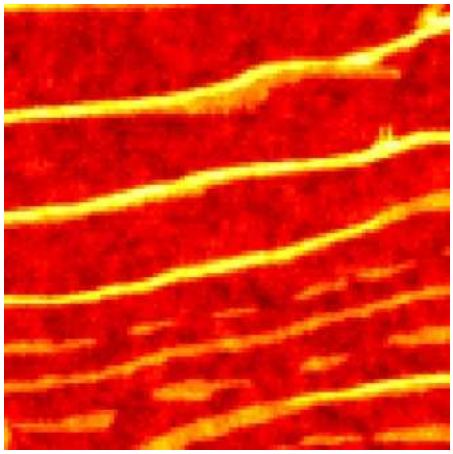


Figure 16 : Optical reflectance map of 30×30 μm with 0.3 μm step. Red colour indicates 1ML graphene, yellow- 2ML

Post-growth treatment

It is believed that hydrogen intercalation after graphene growth eliminates the buffer layer and thereafter substrate/buffer layer induced doping by decoupling the newly formed graphene layer. A proof of concept of the idea has been published in a number of articles but it is not proven yet that this is an industrially viable method. The main problem, to our understanding, is that there is no a full control over the hydrogen penetration underneath the buffer layer and large area decupling cannot be ensured. Nevertheless this is a way to understand the effect of the buffer layer on the properties of epitaxial graphene and how much the mobility can be raised and the sheet resistance decreased. This is of great interest for device makers and therefore it is our obligation to try it.

We have made several tests in different set ups. Some tests were unsuccessful because our graphene is defect free with rather low steps which makes difficult hydrogen penetration to the interface. The degree of success can be evaluated by Raman measurements which give the intensity and the FWHM of three major peaks of different relevance, i.e. 2D – the signature of graphene, G-doping and D-defects. Another evaluation is made by Hall effect measurements which yield carrier concentration and mobility. Sample G495 and G496 were processed under similar conditions. Interestingly, although graphene was grown under identical conditions the samples showed different features after intercalation. Judging from Raman spectra it seems that the intercalation was less successful on sample G496. In overall the results have shown some promises but the treatment still needs further improvement (Table 1).

Table 1 : Hall results concentration/mobility

conditions	before		after	
Sample #	concentration	mobility	concentration	mobility
G495	-1.9e13	1040	+3.0e13	1446
G496	-1.8e13	920	+7.0e13	460

It is to be noted that the initial carrier concentration is rather high what has not been measured as a typical value on micron size Hall bars. Here a Van der Pauw geometry was used. This indicates that there are a number of factors that can be taken into account in the processing chain.

Sample delivery during the period reported

3 samples 7X12 mm2; 2 samples 7x7 mm2 ; 6 samples 15x15 mm2
4 samples 15x15mm2 to Tyndall for ALD of dielectric films – 05/2014
More samples- the number and time to be decided by partners

- **Graphene ex-foliation (GI)**

Based on requirements from consortium partners, particularly Tyndall, we have concentrated on producing graphene flakes on oxidised silicon wafers (thermally grown oxide) for this period. In total, >10 mono-crystalline graphene flakes have been prepared across 5 samples (T0+12 → T0+18).

The table below contains more information about the samples (Table 2).

Sample Ref #	Substrate material	Flakes	Delivered to
S8140	High resistivity Si with 300 nm of SiO_2 (dry thermal growth)	2 monolayers, 1 mixed (mono-, bi-)	TYNDALL
S8141	High resistivity Si with 300 nm SiO_2 (dry thermal growth)	2 monolayer, 1 mixed (mono-, bi-)	TYNDALL
S8142	High resistivity Si with 300 nm of SiO_2 (dry thermal growth)	1 monolayer	TYNDALL
S8143	High resistivity Si with 300 nm of SiO_2 (dry thermal growth)	1 mixed (mono-, bi-, tri-)	TYNDALL
S8144	High resistivity Si with 300 nm of SiO_2 (dry thermal growth)	3 mixed (mono-, bi-)	TYNDALL

Table 2 : Sample fabricated during the period reported

Datasheets for the samples can be found at: http://grapheneindustries.com/datasheets/NanoRF

All the samples sent to consortium partner Tyndall were intended for high-k metal oxide growth experiments. Each flake contains homogeneous regions >20µm wide that are suitable for a range of characterization techniques.

15 additional samples are in production (>50% complete).

4.3.2 Task.3.2 CNT and graphene material characterization (UNIVPM/SHT/Tyndall)

During this reporting period Tyndall has continued to be involved in extended Raman characterisation of graphene samples supplied by three NANO-RF partners: SHT (3 samples), Graphene Industries (1 samples) and Linköping University (4 samples). It this foreseen that this activity will continue for the next reporting period T_{0+18}-T_{0+24}.

The surface analysis of three different types of CVD graphene samples transferred on SiO2/Si substrate has been done. In detail the 1st sample is an ALD HfO2 20nm-thick on top of CVD graphene transferred on SiO2/Si substrate. The 2nd sample is the reference sample and it is a CVD graphene directly transferred on SiO2/Si substrate.

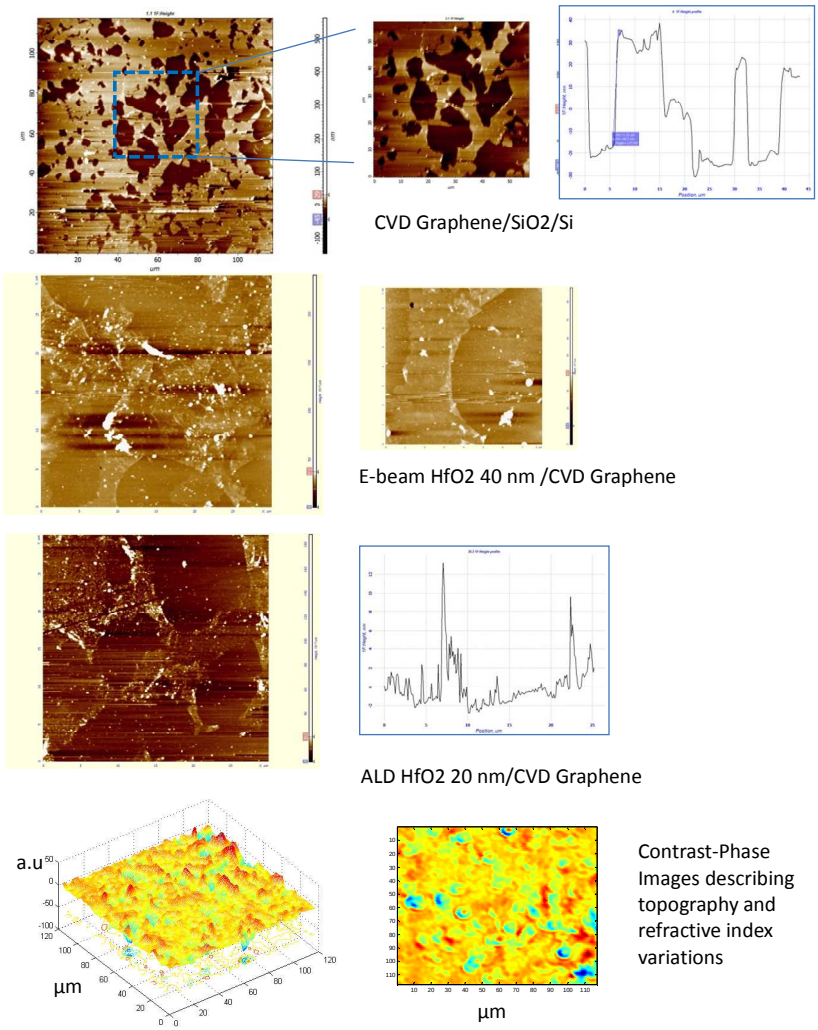


Figure 17 : Atomic Force Microscopy measurements of topography and Contrast-phase images by means of optical micro-cavity ,microsocpy

The 3rd sample has E-beam HfO2 40nm-thick on top of CVD graphene transferred on SiO2/Si substrate. The reported measurements describe a first endeavors to identify the areas where the growth of the high-k metal oxide is covering completely the graphene. The measurements were made by means of Atomic Force Microscopy and Fiber Optical Scanning Microscopy

High resolution Raman spectroscopy and Raman thermometry of graphene

FORTH has provided graphene on quartz and on polymer for Raman characterization. ICN has measured micro-Raman spectroscopy with high spectral resolution in order to evaluate the defect concentration, strain and homogeneity of the material. The spatial distribution of mono, bi- and multilayer graphene is observed in optical micrographs and analysed by the line shape of the 2D Raman mode in graphene for different position of the sample.

In addition, the previously developed and constructed Raman thermometry technique was applied to study the thermal conductivity of CVD grown graphene on a 7x7 µm Cu grid. The presence of defects and the homogeneity of graphene over a large number of grid windows was pre-characterized using high resolution scanning electron microscopy. Subsequently, the thermal conductivity of the different graphene flakes was investigated by 1-laser Raman thermometry. In order to increase the statistical

relevance, a large number of flakes was investigated by Raman spectroscopy as function of excitation power density. The results indicate large variations in the thermal conductivity for different flakes which will strongly affect the performance and lifetime of graphene based devices in the project.

4.3.3 Task.3.3 : Fabrication of CNT FET (LAAS/SHT/TRT)

A new mask containing RF optimized transistors has been designed and fabricated. The target was to optimize high frequency characteristics and study design parameters in respective fabricated devices.

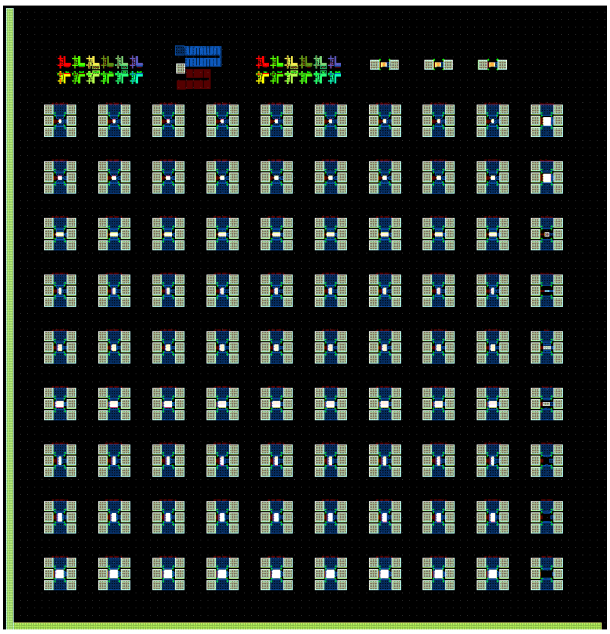


Figure 18: Image of the period of the design. Each period contains 81 RF transistors, Open and Short for de-embedding and test devices to measure gate dielectric capacitance and metal resistivity.

The design completes a parametric study of the following parameters:

1. Source – Drain distance: 4,2 and 1um with alignment marks to reduce this further by e-beam lithography
2. Gate width: 100, 050 and 30 um
3. Gate length: 1um by optical lithography and alignment marks to add submicron gates by e-beam lithography
4. Gate finger number: 2, 4 and 6 fingers (Figure 19).

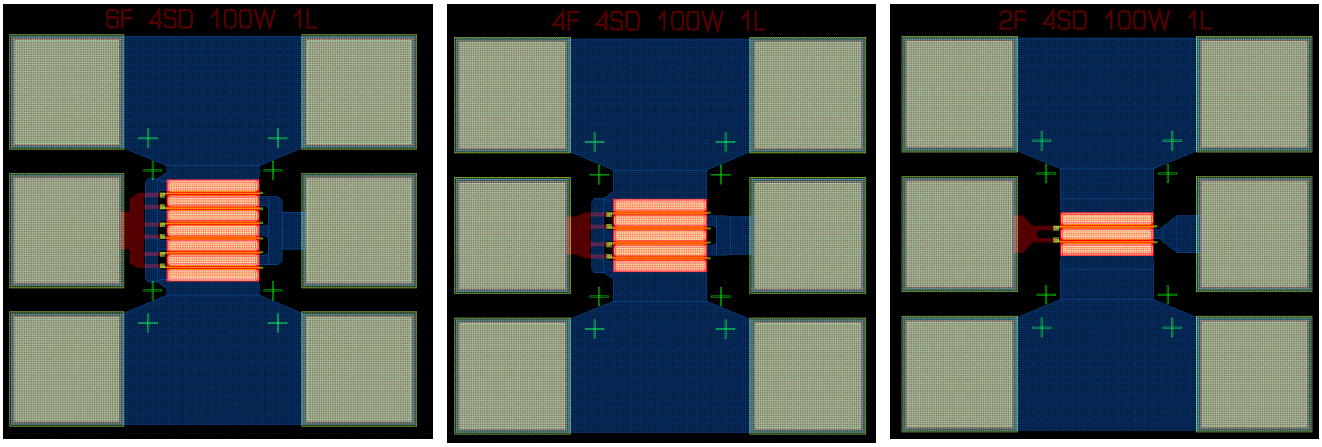


Figure 19: Transistor design with different number of source – Drain channels (6, 4 and 2 starting from left)

RF probe gate pitch was designed to be 150um compatible with the consortium measuring systems.

Furthermore, the following test devices were added:

- Open de-embedding standard
- Short de-embedding standard
- Metal meander for each metalization to measure resistance
- Gate and polyimide capacitance to calibrate capacitance per area for subsequent matching networks fabrication

In Figure 20, the devices to study gate finger number for a gate width of 100um are shown.

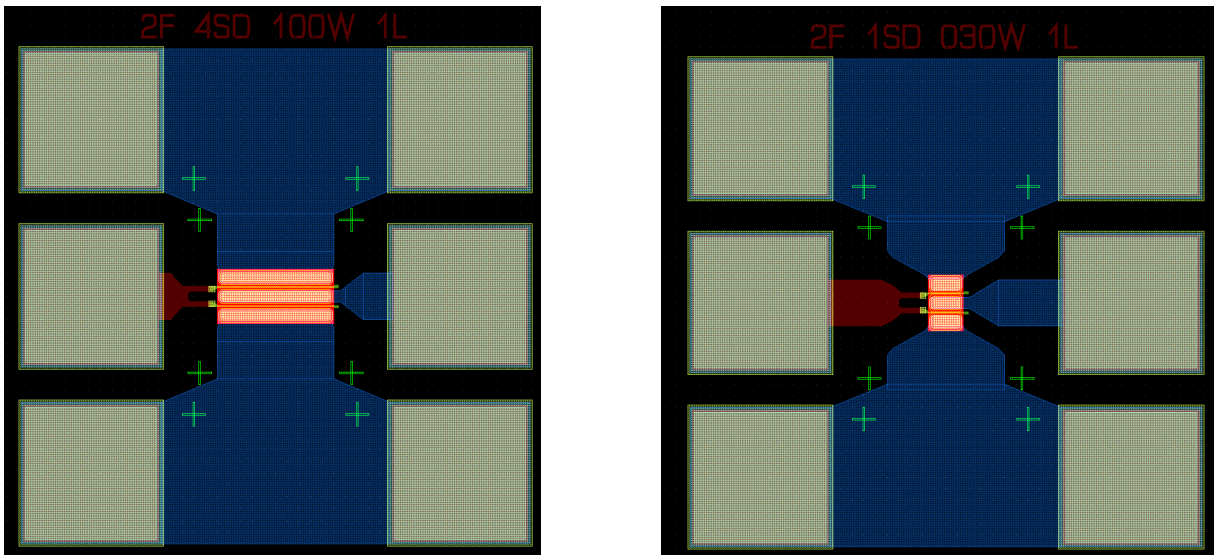


Figure 20: Transistor design with changing channel width from 100um (left) to 30um (right)

The optical lithography masks were transferred to FORTH for further device fabrication

The design described in the previous paragraph was completed using a process flow able to realize all necessary MMIC process for final circuits. In short the designed process flow is as follows:

- CNT growth/deposition
- Ohmic contacts deposition (source – drain formation)
- MESA etching (active material removal)
- Bottom metal deposition (Gate access metal, Bottom capacitor plates)
- Gate dielectric deposition and patterning (Gate dielectric, high value capacitors dielectric)
- Gate metal deposition (optical lithography and/or e-beam lithography)
- Top dielectric deposition and patterning (Gate to S-D metal isolation, low value Capacitors dielectric)
- Top metal deposition (S-D interconnection, low loss lines formation, top capacitor plates formation.

Concerning the horizontally CNTs growth, we found the mass flow controller for acetylene at low flow rate is not accurate. However, the SWCNT growth is very sensitive to the flow rate of gases and pressure in the growth chamber. So we tried to install a new flow meter MFC in the equipment with more accurate control on the feeding carbon gas. The new MFC allows a maximal flow rate of 100sccm, and solves the non-accuracy and delay problem in the growth machine. After adjusting the process parameters, higher quality of SWCNTs can be grown under the new conditions, as shown in Figure 21 and Figure 22. Different from growth using methane, when acetylene is used as carbon feedstock, the low gas concentration is usually necessary for SWCNT growth. But in our CNT CVD, the chamber pressure, which corresponds to the concentration of the carbon gas, can't be adjusted continuously. That's the reason why we need the new MFC for more accurate flow rate control. In the next stage, we will perform the growth at low pressure using the active pressure controller to maintain a continues and steady chamber pressure. Meanwhile, we are planning to install a methane line for high pressure mode growth of SWCNTs.

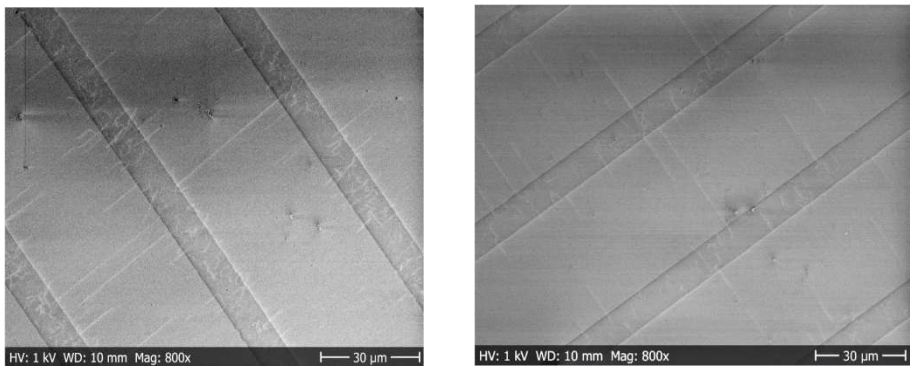


Figure 21 : Growth result with long but low density SWCNTs.

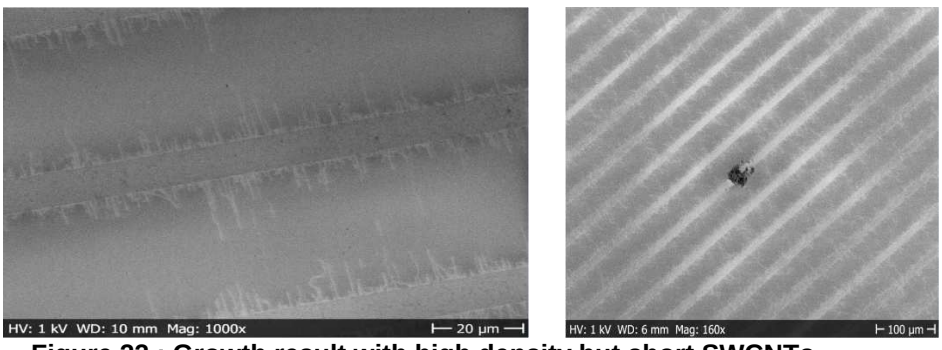


Figure 22 : Growth result with high density but short SWCNTs

4.3.4 Task.3.6 : CNT based antenna fabrication (TRT/SHT/UPMC)

The growth of CNT bundles for CNTs antenna application is performed using thermal CVD method on HR silicon wafers. Different heights of CNTs have been grown in order to study the impact of CNT height on radiation. One example of the CNT bundles grown for this purpose is depicted in Figure 23.

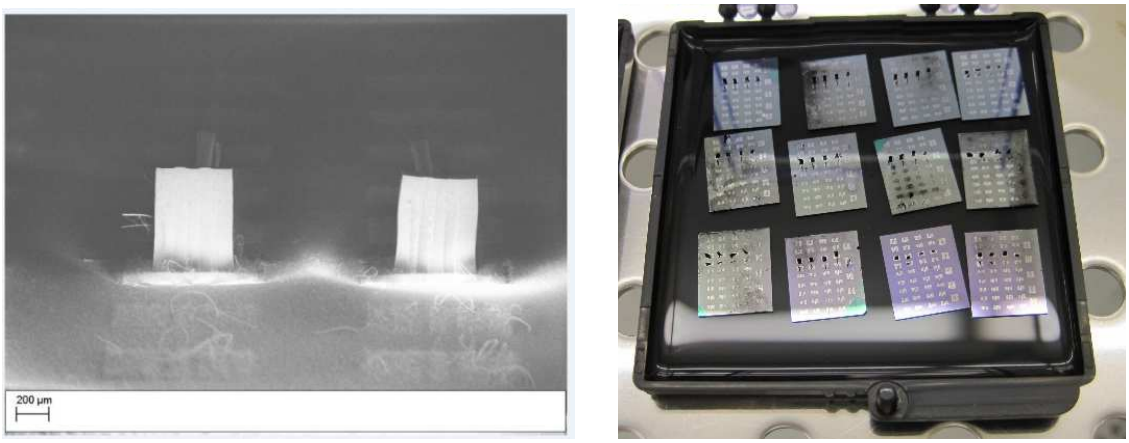


Figure 23 : Vertically aligned CNT bundles for filter application.

4.3.5 Task.3.7 : Development of carbon nanotube interconnects (SHT/CHALMERS)

In the previous period, a transfer technique was employed and the fabrication process of these CMOS process compatible CNT-filled TSVs. During the period reported, we have developed a new transfer process to improve the quality of transfer for the CNT TSV interconnects.

The improved transfer process is illustrated in Figure 24. The CNT-carrying growth substrate is aligned and inserted in the pre-DRIE-etched TSV silicon substrate using a flip-chip bonder machine (the CNTs are covered with Ti/Au layer as we explained in our previous report). After the two substrates are aligned and pressed together, a layer of BCB polymer is spin-coated onto the surface and into the vias. Then the whole sample is cured in a standard BCB curing oven at the temperature of 250 degree C for about 2.5 hours. After the BCB is cured, the bottom CNT growth silicon substrate is removed by using DRIE-etching. And the excessive BCB remained on the CNT tips is removed by plasma etching, thus exposing the CNT tips for electrical contact.

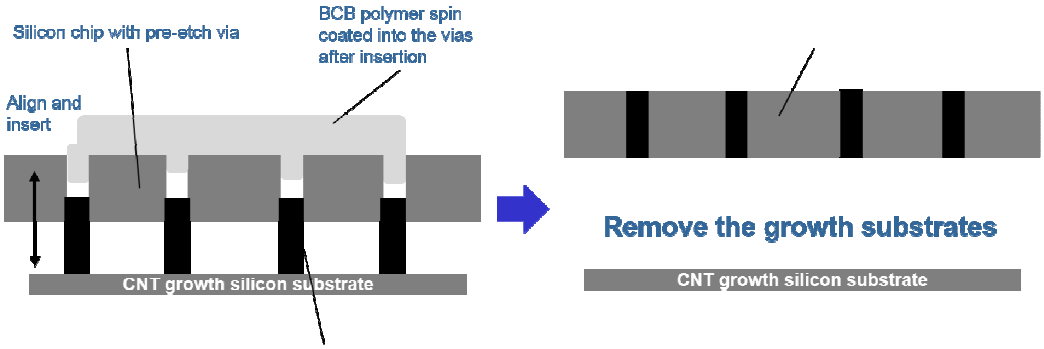


Figure 24 : Illustration of the improved transfer method making use of BCB polymer as the transfer medium, in order to improve the yield of TSV fabrication.

Our experiment result showed good transfer rate over 1mm x 1mm sized silicon chips. As shown in Figure 25, most of the CNTs got transferred into the pre-etched silicon vias. Considering this experiment is carried out manually using an old model flip-chip bonder, the yield of such a process in a fully automated manufacturing process is promising.

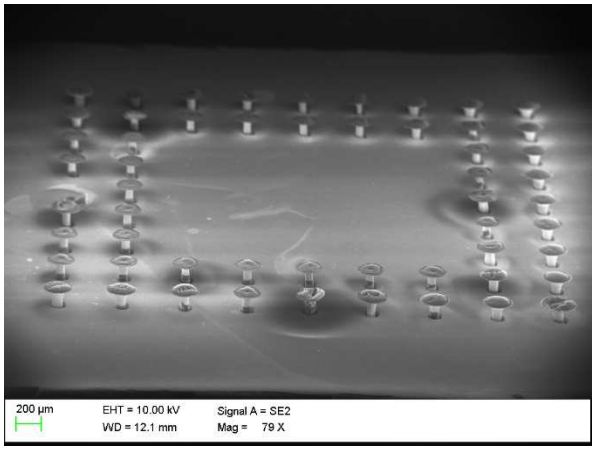


Figure 25 : Result of the new BCB transfer process on densified CNT bundles.

4.3.6 Task.3.8 : Development of RF graphene devices (FORTH/LiU/Tyndall/ICN/IMT)

- **Graphene FET fabrication**

Within the consortium, we have available several types of graphene with the possibility to compare their quality.

The table summarizes the different samples available and collaboration between partners

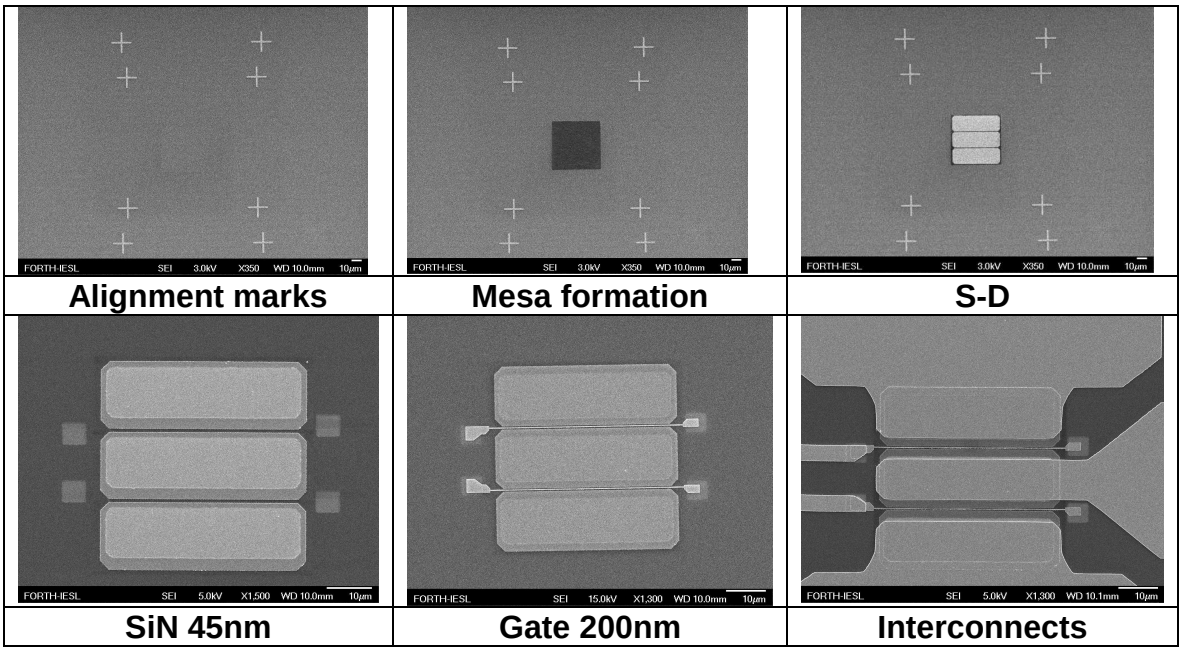
Purchased (Graphenea)	• 1x Monolayer Graphene Films on Si/SiO2 (10mm x 10mm) - Pack 4 units] • 1x Monolayer Graphene Films on PET (10 mm x 10 mm) - Pack 4 units • 1x Monolayer Graphene on Quartz (10 mm x 10 mm) - Pack 8 units • 1x Trilayer Graphene Film (1x1cm) on Si/SiO2 substrate (1.25x1.25cm)
Linköping University	G444, G445, G480, G481, G491 and G492
Tyndall	Received: 1) 3 Sample series HfO on Pt/Silicon by e-beam deposition with thickness for Breakdown and leakage measurements (3 Samples) 2) 1 Sample HfO on Pt/Silicon by ALD deposition for reference of leakage and breakdown 3) 1 Sample HfO by ALD for Gate dielectrics on GaAs temporary wafer for inverse processing (old process for RF) FORTHDENSE mask Sent: 1) 2 Silicon 4" with Pt for ALD and e-beam test depositions 2) 5 Graphene by CVD on Si/SiO2 for gate dielectric depositions 3) 1 3" GaAs (old process for RF) for HfO by ALD (returned) 4) 1/2 3" GaAs (new process for RF) for HfO by ALD
ICN	2 sample for raman thermography: SLG on quarzt and SLG on PET.

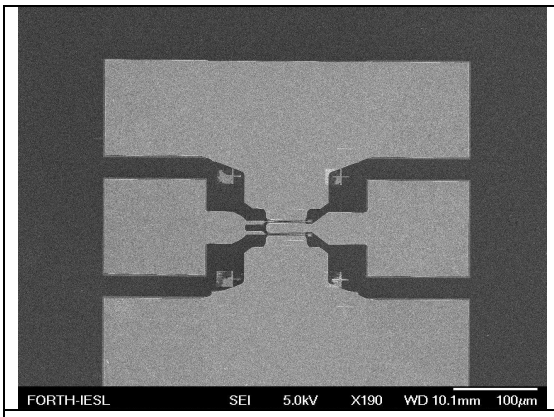
Table 3 : Sample DATA Login

3 series of transistors has been fabricated by FORTH.

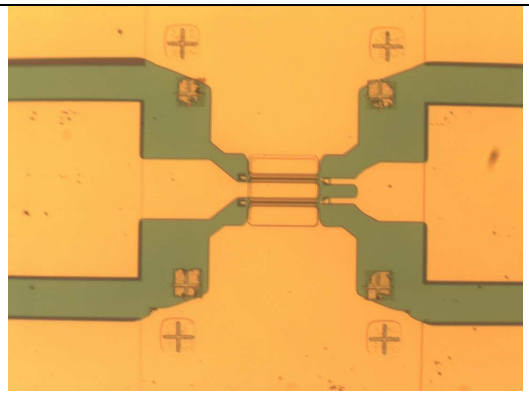
- **<u>1st series (Figure 26)</u>**

Material: SLG on SiO2 on HR-Si (Commercial).
Fabrication: Full e-beam process





Final device (SEM photo)

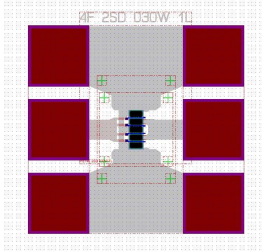


Final device (Nomarski microscope)

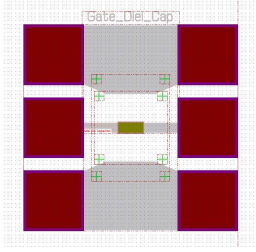
Figure 26 : Graphene FET – 1st series fabrication

- **2nd series (Figure 27)**

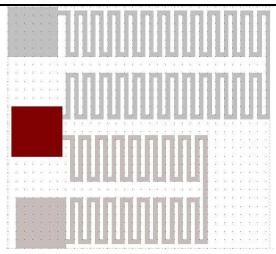
Material: SLG on SiO2 on HR-Si (Commercial).
Fabrication: New design (mix and match optical & e-beam lithography)
Masks fabricated at CNRS-LAAS.



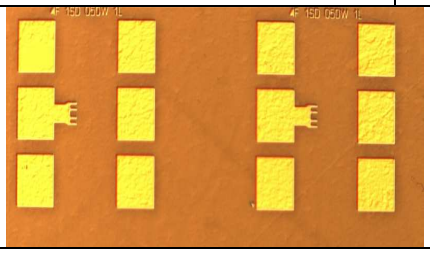
Transistor unit cell



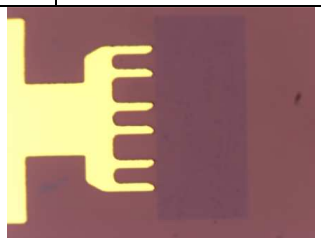
Gate dielectric capacitors



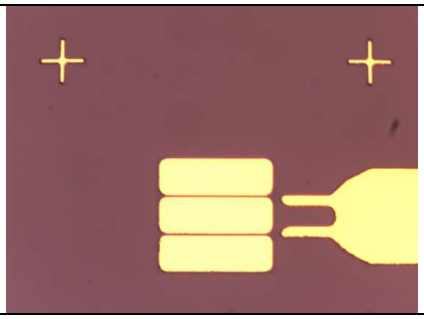
Metal resistivity



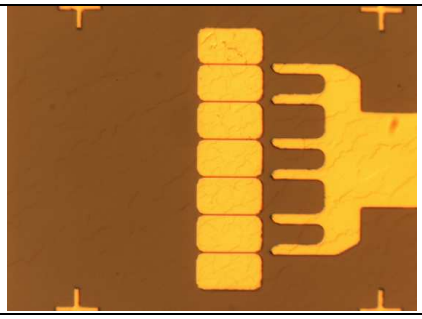
Gate interconnects



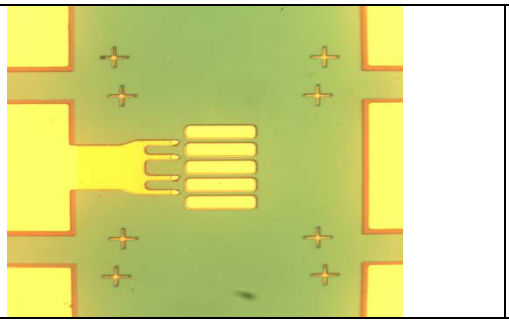
Mesa formation

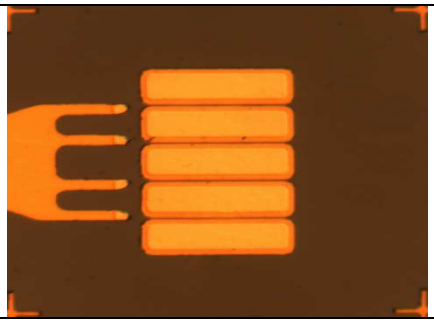


Source - Drain

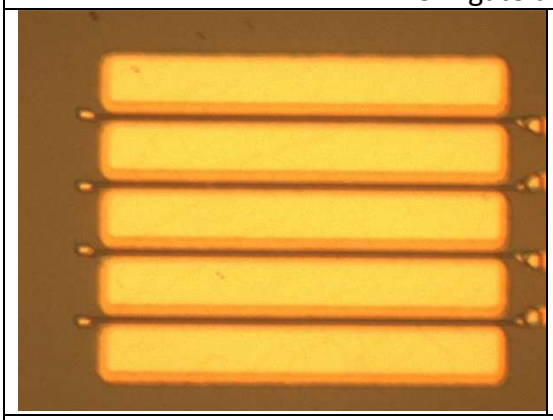


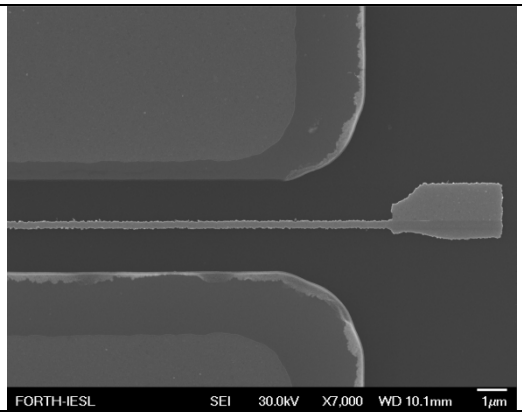
S-D multi gate transistor



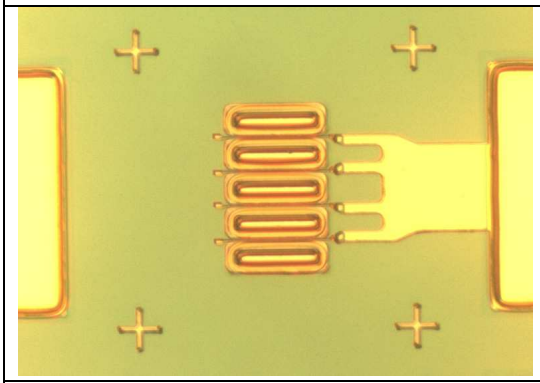


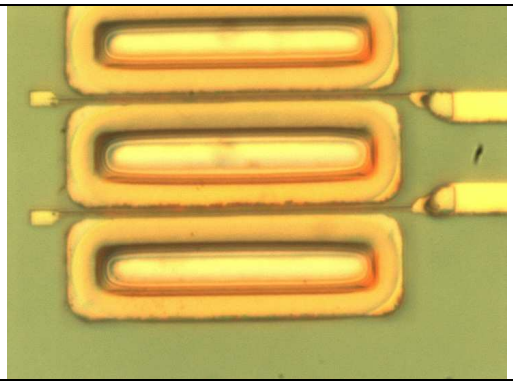
SiN gate dielectric 40nm



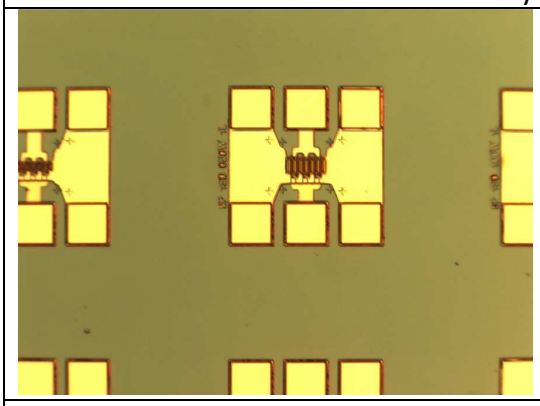


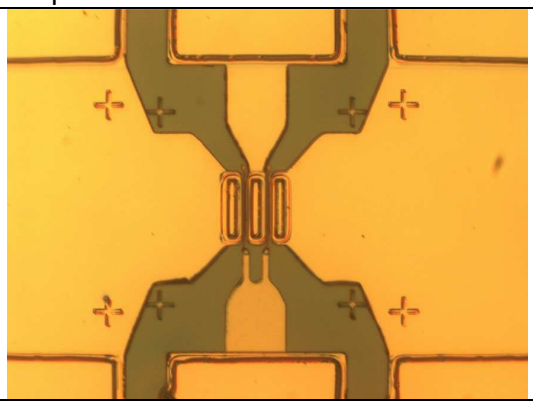
Gate 200nm





Polyimide 1µm





Interconnects | Final Device

Figure 27 : Graphene FET – 2nd series fabrication

- **3rd series**

With the new set of masks and exactly the same processing as for the 2nd series transistors were fabricated on G444 (from Linkoping).

Dielectrics (Tyndall)

Tyndall-UCC has continued his work towards developing a room temperature e-beam process for the growth of high-k metal oxides (ZrO_2 and HfO_2) suitable as gate oxides for graphene and CNT FET devices that will be developed in Task 3.3 and Task 3.8. Following the decommissioning of the Leybold Optics Lab 600 metal oxide coating system and the commission of the new coating system Leybold Optics SYRUSpro 710 Tyndall-UCC started to develop a new room temperature e-beam process for the growth of high-k metal oxides (ZrO_2 and HfO_2)

For the qualification of the new growth process, three HfO_2 thin films with nominal thickness of 4000, 2000 and 400 Å have been grown on Si substrates. The spectroscopic ellipsometry studies done in Tyndall-UCC confirm that these layers are dense and assume a high refractive index (n@632.8nm=1.98±0.02) and good thickness uniformity (see Figure 28 and Figure 29). The Auger spectroscopy study, performed by partner Thales, confirms that HfO_2 thin films assume the correct chemical stoichiometry.

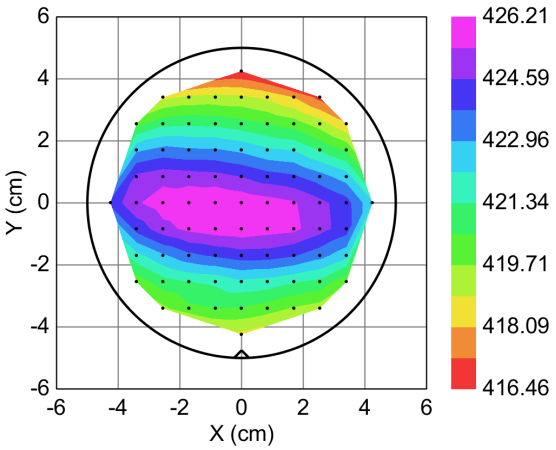


Figure 28 : HfO2 thin film thickness (400 Å-nominal thickness) uniformity over a 4-inch Si substrate (colour chart unit in Å)

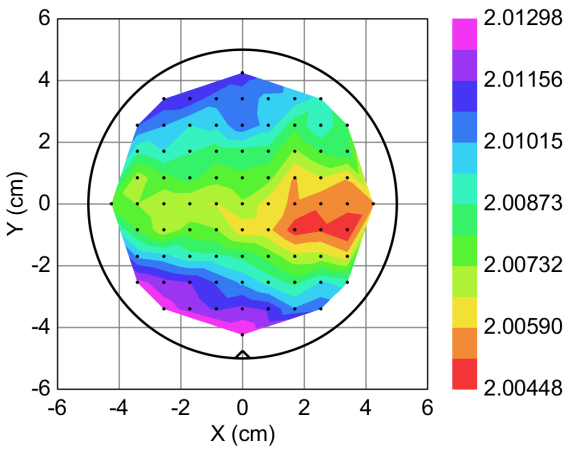


Figure 29 HfO2 thin film refractive index (400 Å-nominal thickness) uniformity over a 4-inch Si substrate (colour chart, n@632.8nm)

In addition Tyndall-UCC has started growth experiments of high-k metal oxide growth on CVD graphene (supplied by partner SHT) and exfoliated graphene (supplied by partner GI). Three samples have been sent by Tyndall-UCC to partners Thales, IMT and UNIPVM for in depth Atomic Force Microsopy and Auger spectroscopy studies and these partners will complete the work in the next period.

- **Graphene antenna fabrication (IMT)**

First step in technological manufacturing of the antenna on graphene it to pattern the graphene layer. Using a photoresist layer, the photoresist layer is pattern using first mask (Figure 30) to remain just over the area where graphene layer should remain.

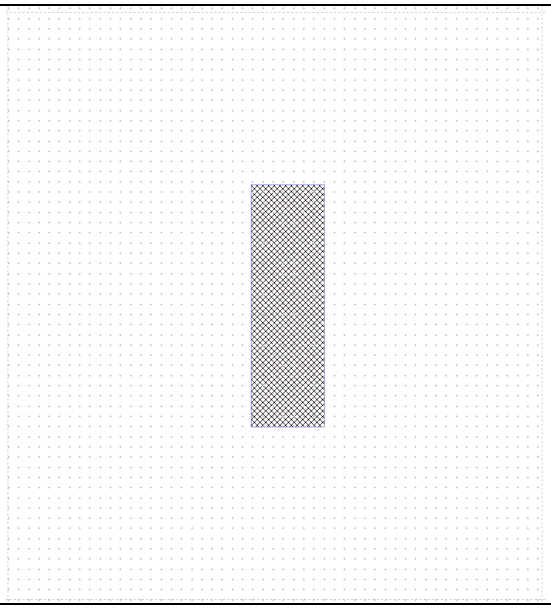


Figure 30 : Mask used for graphene layer patterning.

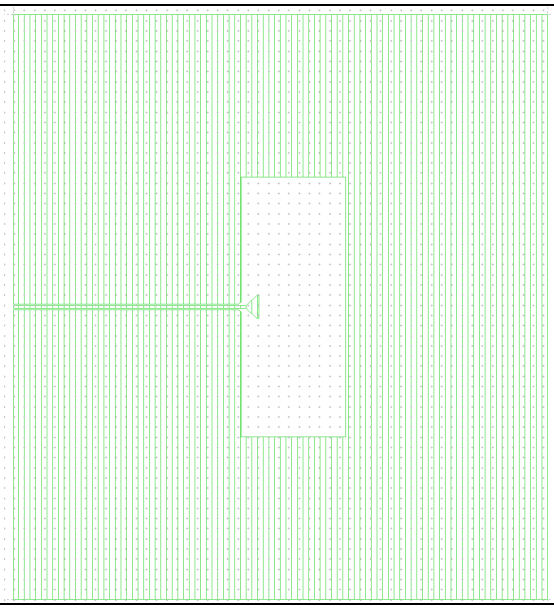


Figure 31 : Mask used for Cr/Au lift-off process.

After graphene layer etching using RIE and removing of the resist layer, the metal (Cr/Au) will be deposit. For this a lift-off process is used. The photoresist layer is pattern in this step using second mask presented in Figure 31.

A superposition of the masks used to manufacture the antennas on graphene is presented in Figure 32

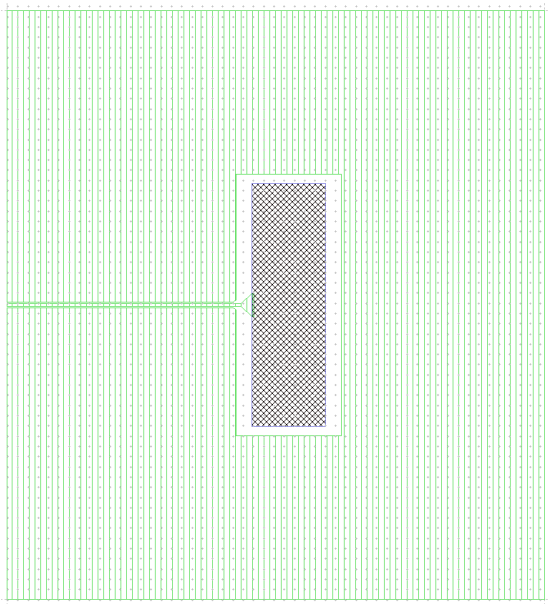


Figure 32 : Mask superposition of the masks used for antennas manufacturing.

Final step is to remove the photoresist to pattern the metallization.

5 PROGRESS IN THE ACTIVE THECNICAL WORKPACKAGE 4

5.1 WP4 : TEST ACTIVITIES

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
LAAS	TRT, CHALMERS, FORTH, LAAS, UPMC,IMT, GI, SHT,UNIVPM, LIU,TYNDALL	T_0 +15 – T_0+26	D4.1 to D4.7 MS4	T4.1 to T4.6	**On Going**

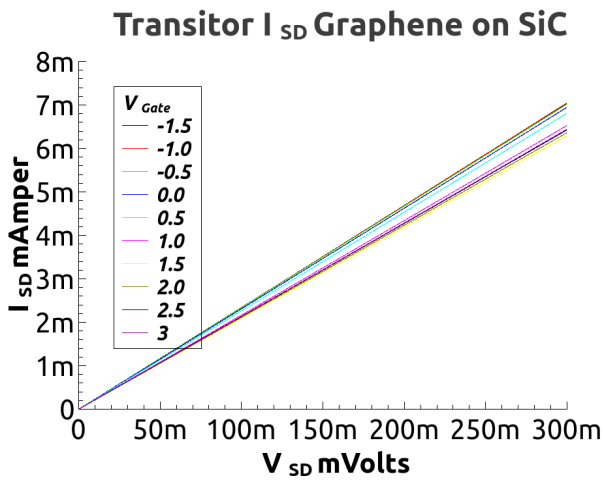
5.2 WP OBJECTIVES

This work package is dedicated to the electrical characterization (DC to RF) of all the devices fabricated in WP3. The results obtained will be compared with the results obtained through simulations in WP2 and basic equivalent circuit models will be calibrated following parameter extraction from static (DC) to high-frequency (HF) measurements. A strong interaction is planned with WPs 2 and 3, in order to take into account all the fabrication available parameters as well to feedback into fabrication and application design the needed optimization

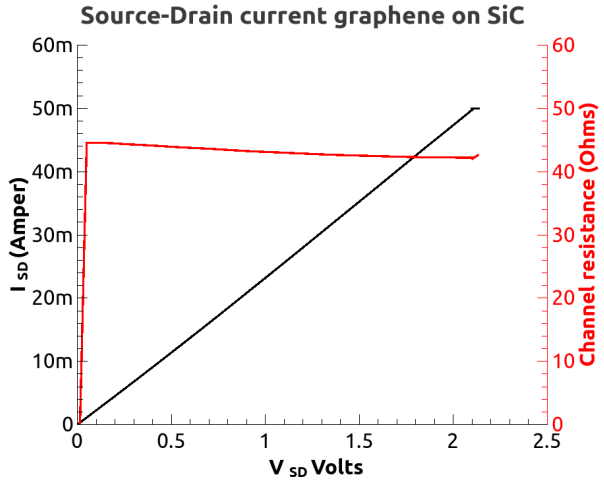
5.3 PROGRESS TOWARD OBJECTIVES : STATUS OF ACTIVES TASKS

5.3.1 T4.1: CNT and graphene FET tests

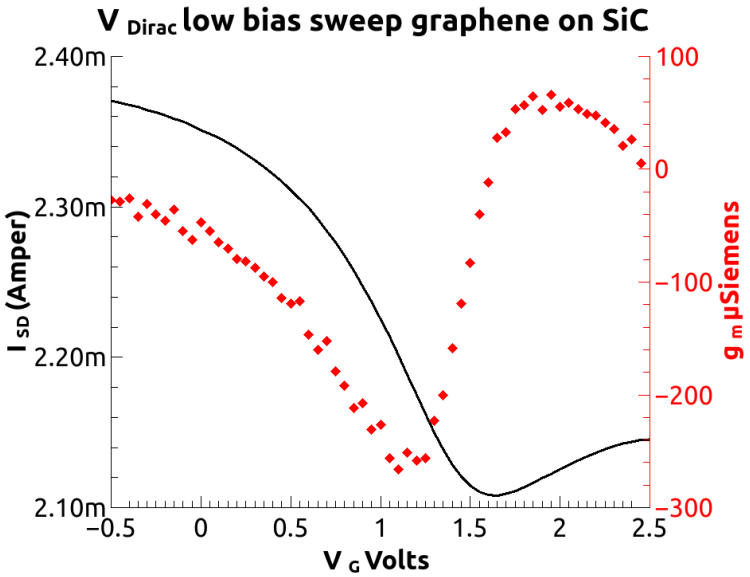
Electrical characterization is underway. The three figures below summarise initial results from the DC analysis of the GFET on Likoping material.



DC results on GFET on SLG/SiC: I_{sd} v. V_{sd}



Channel resistance



Low bias sweep (V Dirac and transconductance)

All transistors are currently under further DC scrutiny and upon completion of full mapping, they will be sent to IMT for RF evaluation.

5.3.2 T4.4: CNT and graphene based antenna tests

- **CNT antenna**

First layouts of vertical CNT layer-based test samples dedicated for microwave radiation from TRT/SHT/Chalmers process described the previous activity report have been set up (Figure 33). First CNT-based quarter-wave length monopole layouts have been processed and implemented in microwave test structures.
In this case, microwave access is assumed by a coaxial-type connector at the bottom of a monopole-type antenna.

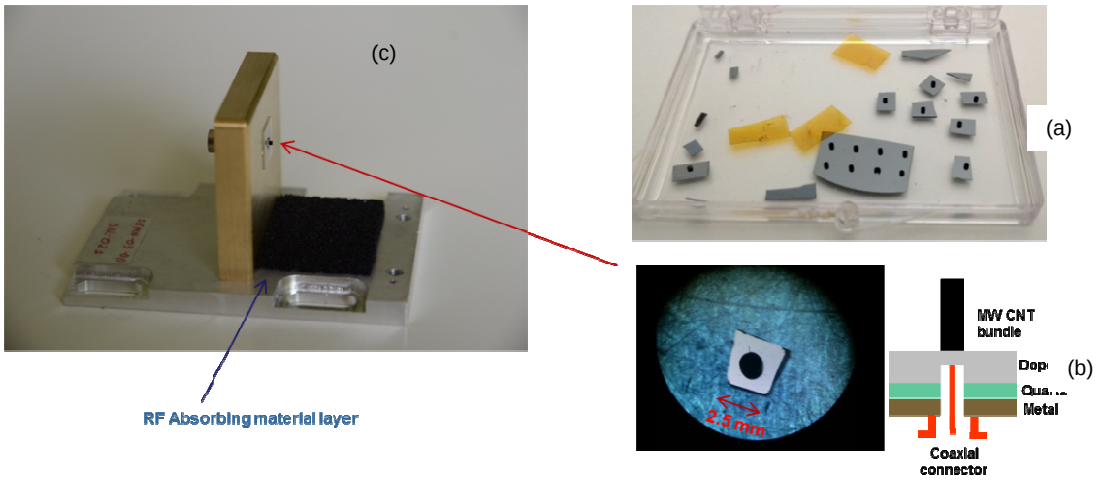


Figure 33 : First experimental microwave test structure configuration (c) of MW CNT bundle monopole on doped Si wafer (a) after wafer dicing/etching (TRT/MC2) and report on quartz substrate (b) implemented inside a protected microwave mounting with a 2,4 mm/50Ω coaxial access (with technical support of sub-contractor IEMN/MC2)

- **Experimental setup for microwave characterization**

A broadband microwave characterization is performed using a vectorial network analyzer in the 0.04 – 50 GHz frequency bandwidth allowing experimental determination of reflexion coefficient (S_{11}) of the CNT-based monopole in free space environment, after a coaxial-type SOLT calibration procedure.
Measurements are executed on two identical samples with and without CNT bundle presence, in order to identify CNT bundle contribution on the complete antenna performances.

- **Experimental results**

A qualitative analysis of the S_{11} coefficient in frequency status on the antenna impedance matching to impedance standard reference (50 Ohms) at 32.6 GHz, with any contribution of the 2mmx1mm circular CNT bundle in the response in magnitude. In contrary, a small sharp phase at a frequency of 12.4 GHz is detected on the angular response, attributed to MW CNT bundle conductivity change (Figure 34).

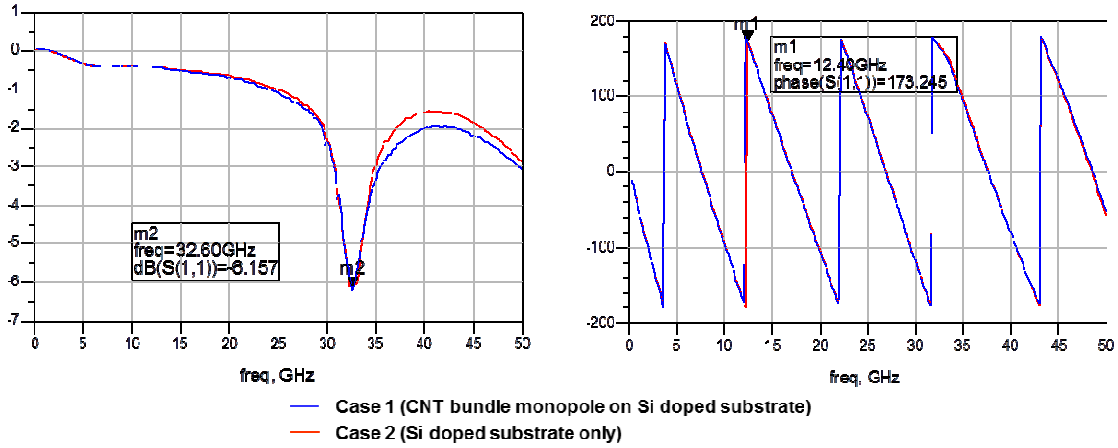


Figure 34 : Reflection coefficient (S11) in magnitude and phase of the free space MW CNT-based monopole , as a function of microwave frequency.

From S-parameters measurements, complex input antenna impedance (Z_e) is extracted (Figure 35). Measured periodic resonances on real/imaginary parts are directly attributed to conductive substrate presence, acting as a cavity with a 7.6GHz fundamental resonance frequency. Strong real part improvement and imaginary part reduction by CNT bundle presence demonstrate the MW CNT bundle influence on resistance and reactance. An enhanced field emission in a 5 – 20 GHz frequency band by CNT bundle presence is expected.

In this context, by applying deembedding techniques on measurements, the MW CNT bundle complex impedance (Z_{CNT}) can be extracted, leading to an equivalent inductive contribution. Exceptional hundred nH inductance values are experimentally demonstrated (Figure 36).

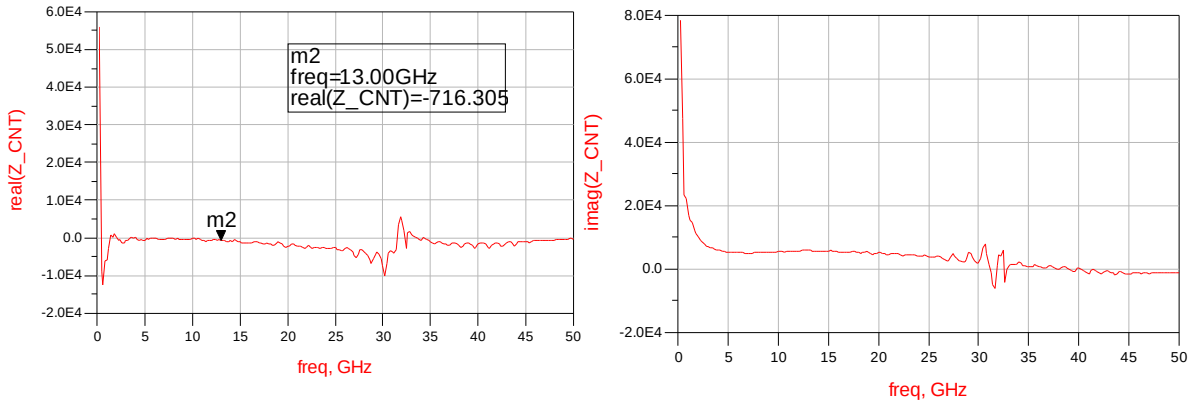


Figure 35 : Experimental real (left) and imaginary (right) impedance values of the 2mm x 1mm MW CNT bundle as a function of frequency.

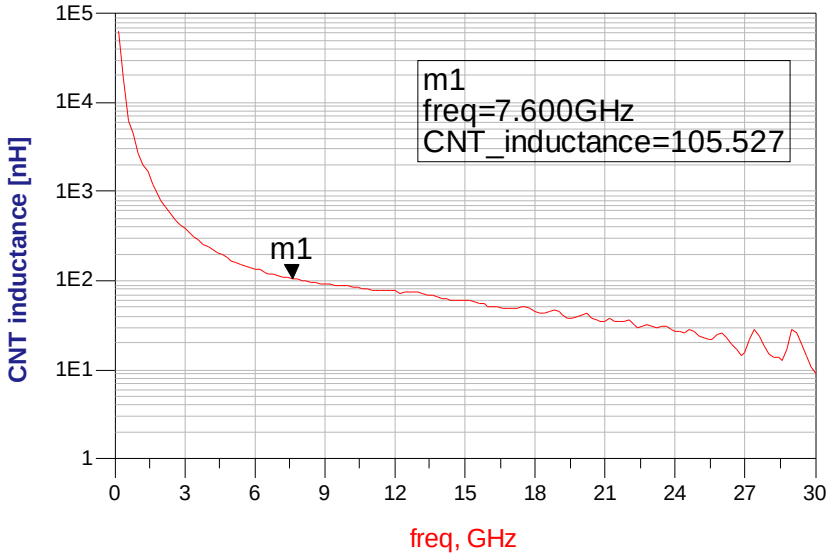


Figure 36 : Equivalent inductance value of the 2mm x 1mm MW CNT bundle as a function of frequency.

- **Measurement platform for CNT antenna properties**

To study the CNT bundle antenna, an RF test platform was devised, simulated and fabricated at CNRS-LAAS.

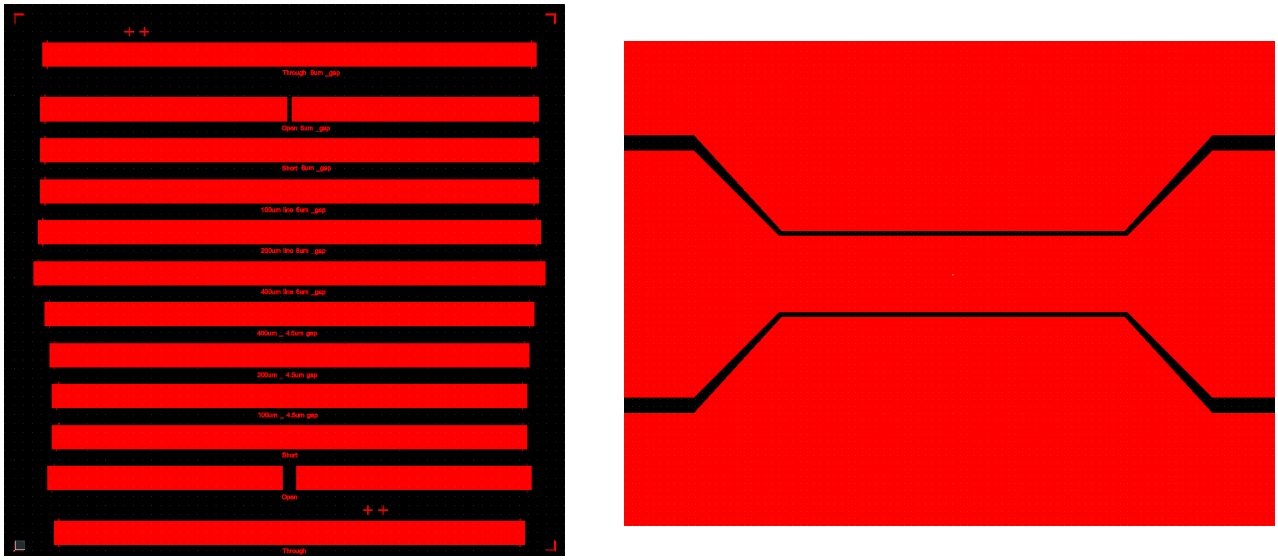


Figure 37: Design Period (left) and taper down detail (right) of the Coplanar waveguide test bench realized for the CNT bundle properties measurements

It consists of a series of long (10mm) Coplanar waveguides to be fabricated on low dielectric coefficient substrates. This provides a strong electric field at the space above the CPW that will interact with the CNT bundles. The later will be placed on top of the CPW center facing down.
To enable proper analysis of the CNT behavior, it is necessary to define the interaction length regardless of the CNT bundle size. That is achieved by fabricating a tapered part at the center of the CPW design. The taper serves to amplify the Electric field directly over the CPW and thus localize the interaction between the taper and the CNTs for the specified length.

Multiple taper lengths were designed to provide data for a multi-line TRL de-embeding method. This will eventually lead to RF data measurements of the response of the CNT bundle under the presence of an electromagnetic field. Thus giving the values necessary to analyze the CNT antenna design.

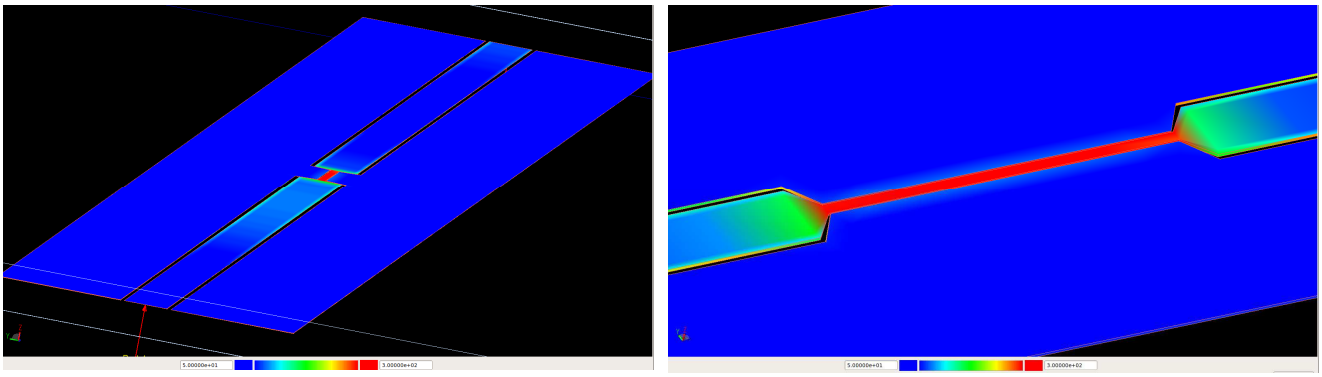


Figure 38: Simulation of Electromagnetic field distribution along the 10mm waveguide structure (left) and the field amplification effect due to the central taper (right)

The associated optical lithography mask was fabricated and sent to FORTH for fabrication.

5.3.3 T4.6 : CNT interconnect tests

We have also measure the resistance of the CNT vias fabricated using this new transfer method. The single via resistance is now less than 1 Ohm, which is less than half of the value we have reported from the old method. This indicates a good signal that the new method not only improves the yield but also the quality of the CNT vias after fabrication.

As can be seen, for identical via configurations the via resistance has decreased from 2.7 to 0.7 ohms. The via resistivity is now almost as small as the variation in the previous method when indium was used for transfer (Figure 39).

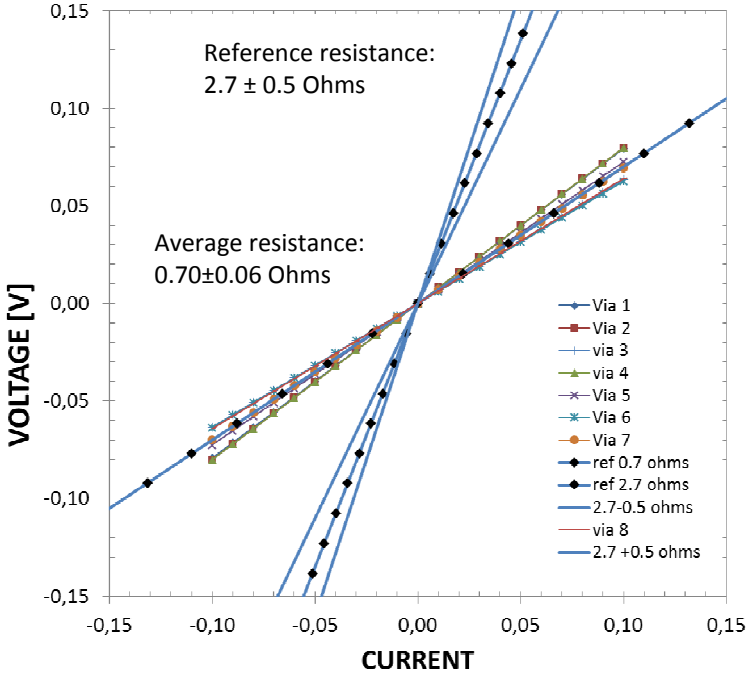


Figure 39 : Electical characterzation of the CNTs via

A simple CNT TSV LED demonstrator has also been fabricated where four parallel light-emitting diodes have their bias voltage supplied through CNT TSV:s. This demonstrator is shown below (Figure 40).

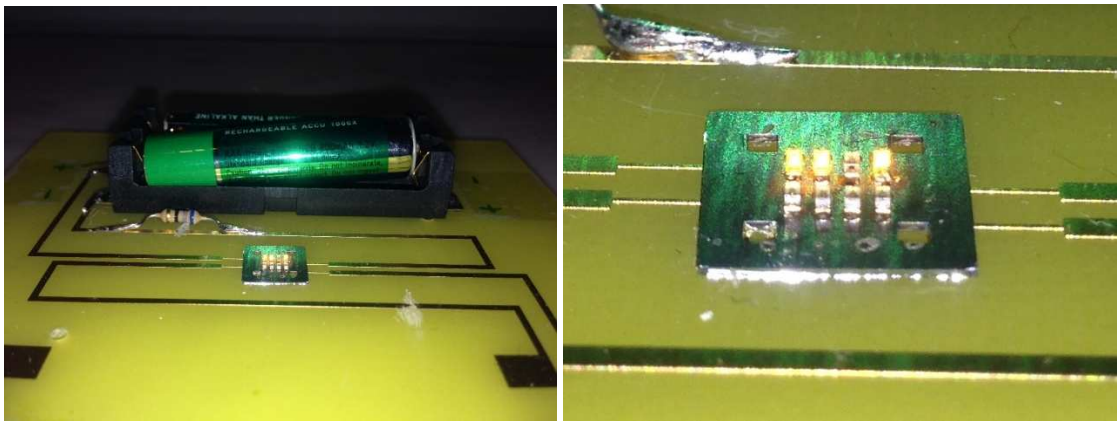


Figure 40 : CNT TSV LED demonstrator

6 DISSEMINATION AND EXPLOITATION ACTIVITIES (WP6)

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
TRT	TRT, ICN	T_0 +0 – T_0+36	D6.1 to D6.6	-	**On Going**

- **PUBLICATIONS & CONFERENCE**

a) C.Tripon-Canseliet, S. Xavier, M. Modreanu, A. Ziaei, J. Chazelas, Vertically-grown MW CNT bundles microwave characterization for antenna applications, submitted to NEMO2014, May14-16, Pavia , Italy

b) Tyndall-UCC has submitted a proposal for a symposium at E'MRS Spring Meeting 2015, Lille, France entitled "Current Trends in Optical and X-Ray Metrology of Advanced Materials for Nanoscale Devices IV.

c) D. Mencarelli, L. Pierantoni, T. Rozzi, F. Coccetti, "Nanoscale Simulation of Three-Contact Graphene Ballistic Junctions", Nanomaterials and Nanotechnology, 2014, 4:14, pp. 1-7, ISSN: 1847-9804, DOI: 10.5772/58547

d) D. Mencarelli, L. Pierantoni, A. Di Donato, M. Farina, "Microwave characterization of anisotropic graphene by applying the Duality theorem," submitted to: IEEE Transactions on Terahertz Science and Technology

e) L. Pierantoni, D. Mencarelli, "Efficient Characterization of the Electromagnetic-Quantum Transport Coupling of Wired CNT- and Graphene Antennas", 8th IEEE European Conference on Antennas and Propagation (EuCAP), The Hague, The Netherlands, 6-11 April 2014.

f) L. Pierantoni, D. Mencarelli, "Radio-Frequency Nanoelectronics - Bridging the Gap between Nanotechnology and R.F. Engineering Applications", to appear: 15th annual IEEE Wireless and Microwave Technology Conference (WAMICON 2014), Tampa, Florida, June 6, 2014.

g) D. Mencarelli, L. Pierantoni, "Electromagnetic Simulators for the Modelling of Magnetically Biased Graphene", to appear: 2014 International Microwave Symposium (IMS), Microwave Symposium Digest (MTT), Tampa Bay, FL, USA, June 1-6, 2014.

h) D. Mencarelli, L. Pierantoni, F. Coccetti, "Nanoscale Modeling of Three-Contacts Graphene Ballistic Junctions: Analysis of the Non-Linear Transport", to appear: 2014 International Microwave Symposium (IMS), Microwave Symposium Digest (MTT), Tampa Bay, FL, USA, June 1-6, 2014.

i) L. Pierantoni, M. Dragoman, D. Mencarelli, "Analysis of a Microwave Graphene-Based Patch Antenna", 16th European Microwave Week (EuMW), Nuremberg, Germany, Oct. 6-11, 2013.

j) D. Mencarelli, M. Dragoman, L. Pierantoni, T. Rozzi, F. Coccetti, “Design of a Coplanar Graphene-Based Nano-Patch Antenna for Microwave Applications”, 2013 International Microwave Symposium (IMS), Microwave Symposium Digest (MTT), Seattle, WA, USA, June 4-6, 2013.

h) L.Pierantoni, D.Mencarelli, F. Coccetti, “Advanced modeling of graphene nanodevices: metal-carbon transition and patch antennas”, 7th IEEE European Conference on Antennas and Propagation (EuCAP), Gothenburg, Sweden,8-12 April 2013.