INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

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European Platform for Low-Power Applications on Silicon-On-Insulator Technology

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RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

Table of contents

1.- Introduction.

The EUROSOI Newsletter was born in June 2008 following the efforts that the EUROSOI network is making to improve its work and with the dedication that has been shown thus far. The aim of this monthly publication is to collect and summarize the main advances and achievements of the SOI technology.

The Newsletter is organized in different sections covering a wide variety of topics such as international SOI events, industrial news, workshop announcements, outstanding features… hence showing the progress and steps forward of the network, whose ultimate goal is to become an open platform for all the SOI community. During these past months the EUROSOI Newsletter has become a cornerstone of the network since it has been in most cases the best stand from which the call for cooperation and development of SOI material have been performed.

In a network there is nothing more important than keeping in touch with colleagues, and we are very proud to state that our Newsletter is reinforcing every month the idea of converging efforts that allows each of us to become aware of the great capacity to succeed we all share.

EUROSOI Newsletters

(June 2008 — June 2011)

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME I

JUNE, 2008

IN THIS NUMBER:

EDITORIAL

Francisco Gámiz
Professor
Univ. Granada (Spain)

Ten years ago, Prof. Sorin Cristoloveanu provided me with the opportunity to convene the European Silicon-on-Insulator community in Granada. That was the beginning of a very long friendship. As a tireless scientist, a great pioneer and a man with a view to the future, Prof. Cristoloveanu thought it was the right moment to do something about SOI. Silicon bulk technology was approaching its limits and SOI technology was identified by the International Semiconductor Industry as a good candidate for the following years. Wide-ranging efforts to research this technology had been made since the sixties in labs all over Europe, even when it was thought that SOI technology was no more than a niche for some romantic and over-optimistic "troubadours".

With the city of Granada and its Alhambra palace as witnesses, we organised, in October 2000, a rather informal and lively meeting, the main objective of which was to discuss the place of SOI technology in Europe. Many key players in the European SOI scene have joined us since then: Prof. Denis Flandre, Prof. Cor Claeys, Prof. Jean-Pierre Colinge, Dr. Carlos Mazuré and many others. It was the first time the word EUROSOI entered our minds. After two days of fruitful discussion, the following conclusions were drawn: a) The position of European industry with regard to SOI/SOS technology was weak, in spite of the fact that more than 20 research groups (from academia and research labs all over Europe) were successfully working on SOI technology with a very broad scope, from materials to final user applications; b) The main reason for this was the wide gap between industry and research centres with regard to SOI; c) There existed many commercial applications (RF, wireless communications, high temperature, etc.) where European industry could have a dominant position if the appropriate technology were provided. d) It was necessary to take advantage of the previous experience of research groups and to join forces to maximise the synergy between individual skills, thus achieving the best global results.

In order to improve the situation, it was necessary to work towards a European initiative aimed at organising the existing research work on SOI topics and supporting all the actions that might guide the European semiconductor industry to a dominant position in SOI-based applications. This was the birth of the EUROSOI network, with the sponsorship and support of the European Commission.

Now, after several years of intense work and networking, the situation is different to that of those early days. In 2003, the European Commission supported the creation of a European Network on Silicon on Insulator Technology, Devices and Circuits, whose main goal was to create a discussion forum for the exchange of ideas and results on the topic of Silicon-On-Insulator technologies in Europe, and to facilitate the synergy between research groups which would enable the use of Silicon-On-Insulator (SOI) technology as an effective tool to push the limits of CMOS and prepare for post-CMOS.

(continues on page 4)

ANNOUNCEMENT

EUROSOI+ fundings for exchanges aimed at scientists in order to enhance collaborations and information exchange.

EUROSOI+ will fund exchanges in terms of travelling and research visits for scientists (students and senior scientists) in order to enhance collaborations and information exchange. Priority will be given to visits involving an industrial partner to allow a better integration of the European industry in the Network.

Applications must be received before June 15th, including a short CV, an invitation letter from the institution to be visited and a comprehensive description of the visit (purpose, destination, duration, budget, etc). Further information can be found at the EUROSOI web site http://www.eurosoi.org.

NEWS

Emerging materials on the Roadmap for silicon-based IC systems

Table 1. Emerging materials status*

Emerging material	First year coverage	Chip products on market	Close to mainstream acceptance	Change of importance since 2005		
				Increased	No change	Decreased
Global strained Si	2003	No	No		•	
Global strained SOI	2003	No	No	•		
Germanium channel transistors	2003	No	No	•		
III-V channel transistors	2007	No	No		N/A	
Isotopically pure Si	2003	No	No			•
Silicon on diamond	2005	No	No		•	
Silicon on SiC	2005	No	No		•	
Silicon on alumina	2005	No	No		•	
Channel orientation	2005	Yes	Yes	•		
Surface orientation	2005	No	No		•	
Carbon nanotubes	2005	No	No		•	
High resistivity Si	2003	Yes	Yes	•		
Optical interconnection on Si	2003	No	No		•	
Phase change memory	2007	No	No		N/A	

*listing the technologies that have been covered by the *ITRS* Emerging Materials committee since its inception in 2003, along with several status columns.

Emerging materials status

In general, emerging materials will augment silicon transistor technology by providing enhanced speed, lower-power consumption, improved heat dissipation, improved memory capacity/data retention, or added RF/analog functionality while maintaining the large scale integration capability of CMOS. The augmentation of the silicon starting material need not be entirely silicon-based as long as CMOS system improvement is the end goal. As an example, the integration of III-V compound optoelectronics on silicon (Si) for enhanced bandwidth for I/O-limited CMOS technologies would be considered an emerging material application.

The definition of emerging materials is as follows: novel starting materials, structures, and processing methodologies that will enable anticipated roadmap requirements and enhance silicon-based CMOS technology.

The International Technology Roadmap for Semiconductors (ITRS) Emerging Materials Committee has now tracked technologies for close to four years. In that time, some technologies have demonstrated progress towards mainstream applications (i.e., have moved beyond 'emerging' status); some technologies have continued to stay active but have not moved into mainstream applications; and some technologies have shown some loss of momentum.

[*Source: Solid State Technology*]

NEWS

AMD unveils three chips for embedded systems

"The latest chips will make it easier for system designers to use their existing AM2 board designs for single core chips", AMD said.

Advanced Micro Devices has launched three dual-core processors for embedded systems that span entry-level networked storage systems to telecommunication products, digital signage, and point-of-sale, gaming, and kiosk systems.

The AMD Athlon X2 dual-core processors, models 3400e, 3600+, and 4200+, run at low-power envelopes of 22 watts for the 3400e and 35 watts for the other two products. The latest chips are AM2 socket-compatible, which will make it easier for system designers to use their existing AM2 board designs for single-core chips, AMD said.

The processors are designed to be paired with the AMD M690E chipset. They also can be combined with Broadcom chipsets, including the HT-2100 and HT-1000. The new products are expected to ship in the second quarter and will have a five-year life cycle.

Along with the new chips, AMD unveiled a reference design kit for the Storage Bridge Bay 2.0 specification based on the AMD Athlon processor. The SBB defines mechanical, electrical, and low-level enclosure management requirements for a slot that supports storage controllers from a variety of independent hardware and system vendors.

[*Source: EE Times*]

NEWS

AMD Launches World's First x86 Triple-Core Processors

AMD announced the availability of AMD Phenom™ X3 8000 series triple-core processors, providing gamers and digital media enthusiasts with exceptional performance at mainstream price points. AMD Phenom X3 processors are designed to improve multi-threaded application performance over dual-core processors at the same clock speed.

As the world's only triple-core x86 processor, AMD Phenom X3 processors bring multi-core technology to a broader audience in search of desktop PCs that easily handle today's digital entertainment workloads.

"In 2007, AMD committed to delivering AMD Phenom triple-core processors in Q1 2008 and today the company makes good on that promise," said Bob Brewer, "AMD understands that today's PC applications are best accelerated with a range of multi-core products from quad- to triple- to dual-core processors, and that's why we now deliver the broadest multi-core desktop lineup in the industry."

[*Source: AMD*]

NEWS

Honeywell Announces New High Temperature Analog Silicon Chip for Aerospace and Deep Drilling Operations

Honeywell announced that its Aerospace business has unveiled a new high temperature Silicon On Insulator electronic component with dualapplications in the aerospace and oil industries.

The chip can withstand high temperatures and be used in aircraft

engines or in deep drilling operations to enhance the nation's energy supply. It was designed and developed as part of Honeywell's diverse suite of aerospace and industrial electronics.

"The aerospace and oil and natural gas industries each require high

performance components that operate over wide temperature ranges," said Brian Link, Business Director, Honeywell Defense and Space. "Honeywell's Silicon On Insulator technology is critical for instrumentation and sensor measurements in these environments. The dual precision chip will be used in high temperature zones on jet engines for instrumentation and control, as well as operating in temperatures up to 225 degrees C and at depths exceeding 20,000 feet in deep drilling operations.

Honeywell's high temperature electronics improve system reliability and help to reduce operators' equipment downtime and weight.

Honeywell's new high temperature dual precision operational chip model HTOP01 was developed with several industrial partners as part of the U.S. Department of Energy's Deep Trek Program.

[*Source: PRNewswire*]

NEWS

Timing not right for 450mm, says AMD's Grose

Speaking at The ConFab in Las Vegas, AMD's Doug Grose said that the timing is not right for a transition to 450mm wafers, and suggested that the concept of the industry historically moving to a new wafer size every ten years was flawed.

Describing the present macroeconomic picture as "pretty bleak," Grose gave a nod to the cost that equipment and material suppliers must carry in making a wafer size change a reality. "Distribution of profit across our industry is really not equitable. We all know that we can't create shareholder value without the equipment and software and materials suppliers and neither can they," Grose said. "So what sense does it really make to pursue an industry strategy that's not really a win-win for everybody? The last thing in the world we need right now is to starve our suppliers. That's obviously like shooting ourselves in the foot."

Grose estimated that 4% of the industry's 25%-20% annual gains in productivity really come from increased wafer size. The rest comes from smaller die sizes, process improvements and obviously improved yields, defect density, etc. "The cost to the industry of driving to get that 4% a year is going to be very, very large. It seems inevitable we're going to have to make that move because the benefits are significant," he said, and asked: "But when, and how do we get the most from 450mm once we do make that move?"

[*Source: Solid State Technology*]

"what sense does it really make to pursue an industry strategy that's not really a win-win for everybody?", said Grose

EUROSOI NEWS

First Announcement of the EUROSOI Workshop 2009

A year on, as is tradition since 2005, and for the fifth consecutive time within the framework of the EUROSOI Network, a new edition of the EUROSOI Workshop will take place next January. Next year 2009 event will be held in Chalmers, Sweden.

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world.

EUROSOI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and applications oriented engineers.

Complete information about the 2009 Workshop will soon be available at the EUROSOI web site http://www.eurosoi.org

EDITORIAL (cont.)

We are just at the beginning of this exciting stage. The challenges are many and the road not easy

Today, the EUROSOI network comprises more than 30 partners from all over Europe, with expertise in all fields of SOI technology. The EUROSOI network has already made possible the achievement of a large part of this objective by successfully organising and bringing to fruition during the last three years a significant number of events such as the EUROSOI roadmap and state of the art documents, workshops, training events and scientific exchanges.

In the framework of the new FP7, a new project, EUROSOI+ has been launched, started on January 1st 2008. The first goal of the new project is the upgrading and maintenance of this important forum, providing updated versions of the State-of-the-Art report and Roadmap, facilitating scientific exchanges between partners, organising workshops and later, using it as a launch-pad for other important objectives:

•To create a durable European School of SOI Technology.

•To foster and co-ordinate the initiatives and activities required to successfully face up to some of the challenges identified and listed in the EUROSOI Roadmap.

•To co-ordinate the development of a research-dedicated platform in order to address circuit design aspects, focusing on the advantages of SOI for Low Power applications. In two to three years, this platform will provide, through its integration in EUROPRACTICE, prototyping and Multi-Project-Wafers (MPW) in SOI open to European research groups and Fabless Semiconductor companies (SMEs) using the LETI SOI process.

We are just at the beginning of this exciting stage. The challenges are many and the road not easy, but with the help of all of you, I am sure we will be successful, and this will also mean success in rejuvenating the old Europe.

This is the first of what I hope will be a long series of EUROSOI Newsletters. Periodically this short publication will collect brief announcements and links to advances in SOI technology all over the world. Here, you will also find the steps forward, activities and progress of our/your EUROSOI Network, whose ultimate goal is to become an open platform for all our people, the SOI people. To this end, I sincerely invite all of you to contribute in developing this publication.

I wish you an interesting and fruitful SOI adventure. Good luck.

NEWS

IBM Unveils Three Energy-Efficient Servers Powered by Quad-Core AMD Opteron™ Processors

AMD announced growing industry support for the Quad-Core AMD Opteron™ processor among global OEMs continues with IBM's launch of three updated System x™ servers. Designed to address customer priorities such as energy efficiency, performance, scalability, and virtualization, the Quad-Core AMD Opteron processor-based servers from IBM offer an exceptional power-efficient platform for today's most demanding datacenters.

"Quad-Core AMD Opteron processor-based servers deliver energy-efficiency even in the context of satisfying IBM's most demanding high-performance computing solutions," said Randy Allen, senior vice president, Computing Solutions Group, AMD. "Datacenter managers are increasingly seeking a balance of performance, energy-efficiency, and advanced virtualization functionality in order to optimize server resources amidst skyrocketing power, cooling and space costs. The Quad-Core AMD Opteron processor is at the forefront of addressing this new real-world definition of datacenter performance."

"IBM continues to deliver innovation and choice in the x86 market with today's introduction of System x servers based on AMD's new Quad-Core processors," said James Northington, vice president, IBM System x. "The new System x3755 allows clients to grow the system along with their business, affordably scaling from the standard 2 socket system to 3 and 4 socket configurations while delivering industry leading price and performance."

[*Source: AMD*]

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

Mail: eurosoi@ugr.es

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

CALENDAR

- MIGAS International Summer School
Autrans-Grenoble, France.
June 28th - July 4th, 2008

- European School On Nanosciences & Nanotechnologies
Grenoble, France.
August 24th - September 13th, 2008

- Third SINANO Device Modeling Summer School
Bertinoro, Italy.
September 1st - 5th, 2008

- 38th European Solid State Device Research Conference and 34th European Solid State Circuits Conference
Edinburgh, United Kingdom.
September 15th - 19th, 2008

- 2008 IEEE International SOI Conference
Hudson River Valley
New York, USA
October 6th - 9th, 2008

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME II

JULY, 2008

IN THIS NUMBER:

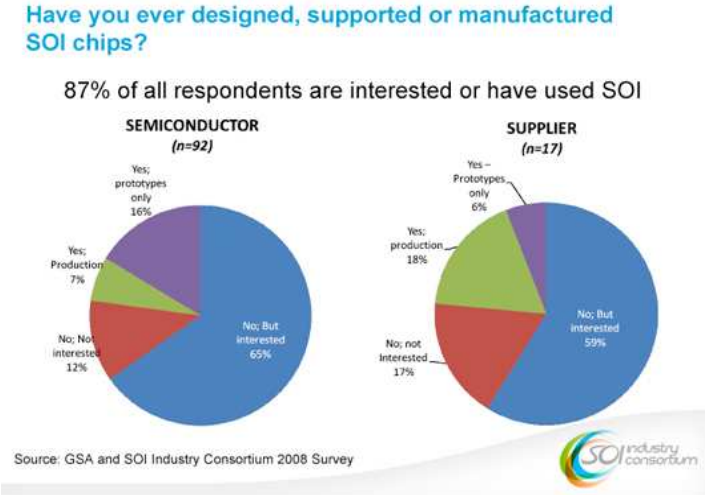
NEWS

GLOBAL INDUSTRY SURVEY RESULTS REFLECT STRONG INTEREST IN SOI FOR LOW POWER AT MAINSTREAM TECHNOLOGY NODES

The Global Semiconductor Alliance (GSA), an organization focused on accelerating the growth of the global semiconductor industry, and the SOI Industry Consortium, a group of leading companies throughout the electronics industry focused on accelerating silicon-on-insulator (SOI) innovation into broad markets, have announced the completion of a global study focused on SOI.

Over 100 semiconductor companies involved in the design of integrated circuits responded to the survey about their needs and perceptions of SOI. Eighty-seven percent of respondents indicated that they are interested in evaluating or are already using SOI, particularly for power savings at mainstream technology nodes starting with 90 nanometers. The survey also confirms the need to educate the market on available solutions, methodology and training across the global ecosystem, points that are being addressed by the SOI Industry Consortium.

"We are pleased to field the study which will gauge perceptions of semiconductor companies on SOI technology," said Jodi Shelton, GSA co-founder and executive director. "The collaboration on this survey with the SOI Industry Consortium provides us with a platform from which we can determine industry education for the global community on SOI potential alternatives and benefits."



"The results of the study show that there is an interest in SOI throughout the greater chip design, manufacturing and electronics community," notes Horacio Mendez, executive director of the SOI Industry Consortium. "Respondents indicate that one of the main reasons they're looking at SOI is to solve low-power challenges."

[*Source: SOI industry consortium & GSA*]

EUROSOI ANNOUNCEMENT

Distinguished Lecturers list elaboration

EUROSOI+ is now elaborating a complete list comprised by experts in the SOI field (fabrication, materials, devices, circuits, simulation, etc). This list will be specially useful to prepare all the training events in the next EUROSOI+ events.

See the EUROSOI web site for downloading the file that must be filled out and sent back before July 9th.

Do not hesitate to include yourself if you are considered as an expert in any specific SOI topic.

You can also:

1.- Include people that do not belong to the EUROSOI network or currently working out of Europe

2.– Widely broadcast this announcement to other colleagues out of the network.

NEWS ANALYSIS

Semiconductor companies eye SOI advantages and obstacles

"The SOI Consortium is actively working to resolve all of the issues that survey respondents cited as obstacles", Méndez said.

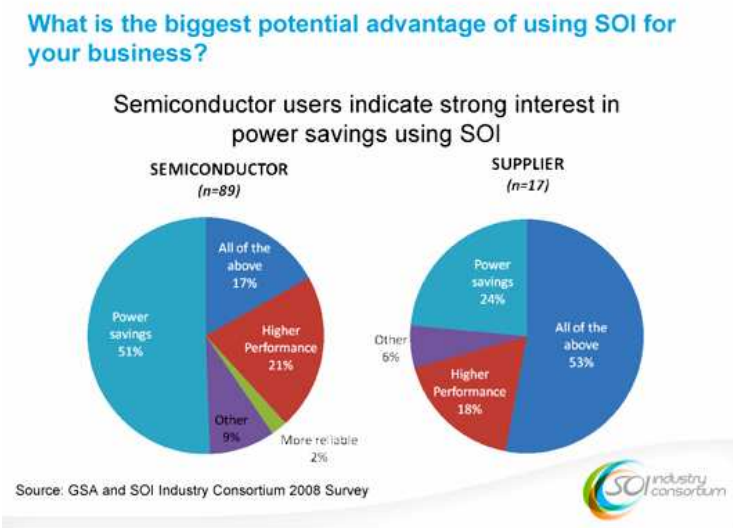
Fabless semiconductor suppliers are interested in silicon-on-insulator (SOI) because the technology allows power savings, but they remain concerned about costs, lack of silicon intellectual property (IP), and availability of EDA tools, according to a survey conducted by the Global Semiconductor Alliance (GSA) in cooperation with the SOI Consortium. The survey identified obstacles that must be overcome for wider SOI adoption.

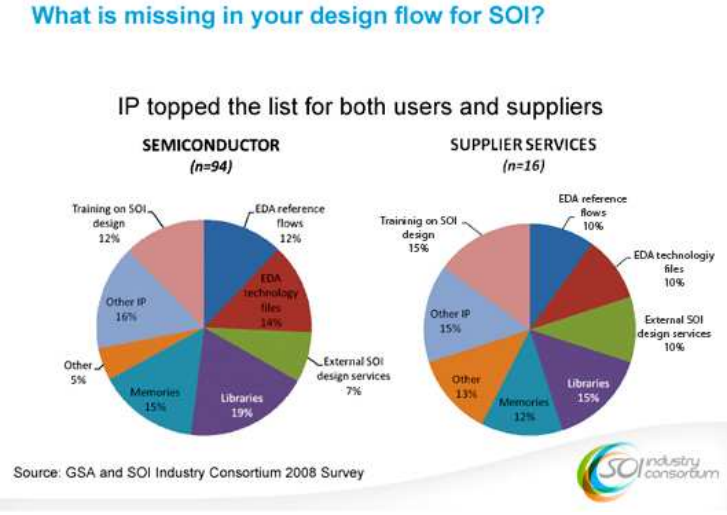
The survey, available now on the GSA web site, compiled responses from 110 industry respondents holding positions such as CEO, CTO, director of engineering, and vice president of engineering. 94 are from semiconductor suppliers, design services providers, and systems companies. While several IDMs are represented, most of the semiconductor suppliers are fabless. 16 respondents are from supplier companies including IP, EDA, wafer foundries, equipment providers, and back-end service providers.

On the plus side, the survey found that 23 percent of respondents already use SOI. Another 64 percent don't use it today but are "interested." Power savings is seen as the most significant advantage, with many respondents willing to accept a higher total product cost to save power. Respondents expressed interest in SOI at conventional process nodes, such as 90 nm and 65 nm, in addition to advanced process nodes.

On the other hand, some respondents cited cost and lack of design knowledge as obstacles to SOI adoption. 56 percent were unsure whether their EDA tools are ready for SOI, and 12 percent said they are not, even though SOI advocates say that no significant tool changes are needed. Nearly half of the respondents noted that SOI intellectual property (IP) libraries are still inadequate or completely missing from the design flow today.

SOI, which electrically insulates the silicon active layer from the underlying substrate, has been adopted primarily by IDMs and used in fairly narrow niches such as high-end CPUs, and high-voltage and radiation-hard applications. The SOI Consortium is working to build an IP, EDA and foundry ecosystem that would broaden the adoption of SOI and bring it into the IC design mainstream.





The SOI Consortium is "actively working" to resolve all of the issues that survey respondents cited as obstacles, Mendez said. One approach is education. Mendez said that the consortium is organizing worldwide tutorials that show designers how to work with SOI. "There's a history effect," he said. "It's not tricky, it's just different. In a half day or so we can bring people up to speed."

[*Source: SCDsource*]

NEWS

Intel explores floating-body cells on SOI

At the 2008 Symposium on VLSI Technology in Hawaii, Intel Corp. revisited its research on floating-body cells (FBCs) for advanced cache designs in microprocessors.

The big question is whether Intel is finally endorsing silicon-on-insulator (SOI) technology, as the company will describe the world's smallest FBC-based planar device on SOI for possible use at the 15-nm node. In related paper, Intel is also expected to describe new adaptive circuit techniques for SRAM cache cells. Both technologies are in R&D and still in the lab, it was noted.

Waiting in the wings in the race towards FBCs--or sometimes called floating-body RAMs (FB-RAMs)--is rival Advanced Micro Devices Inc. (AMD). Two years ago, AMD licensed an embedded FBC technology from Innovative Silicon Inc. (ISI).

For years, FBC has been touted as an alternative to conventional cache memory, because current capacitor-based technology is running out of gas. FBC is a candidate for increased memory density, compared to the standard six transistor (6T) cache memory that is used on all microprocessors today.

"In a standard DRAM, there is a capacitor and a transistor," according to ISI. "The capacitor stores the logic state, 1 or 0, and the transistor provides the rest of the circuitry access to the capacitor. To read a DRAM memory cell, the transistor is turned on and the charge on the capacitor is allowed to flow onto a bitline, creating a small voltage which can then be detected."

Jeff Lewis, vice president of marketing at ISI (Santa Clara, Calif.), warned that there are some major issues cropping up with the capacitor in DRAMs, prompting the need for a new architecture. "Capacitor scaling is becoming almost impossible," Lewis said in a recent interview at the Design Automation Conference (DAC) in Anaheim, California.

[*Source: EE Times*]

NEWS

Selete Achieves 5 GHz Pulses on Silicon Photonics IC

Optical interconnects using an optical fiber and on-chip light guide are being developed as interconnects in servers, circuit boards, and on silicon chips, leveraging advantages such as higher speed transmission and lower power consumption. To that end, the Selete (Tsukuba, Japan) consortium said it has succeeded in transmitting a 5 GHz pulse waveform through a 4 mm light guide produced on a silicon IC. The consortium made the announcement at the recent Selete Symposium 2008.

The light guide serves as an optical interconnect using silicon as the base material, SiON as the core light guide, and SiO2 for the cladding layer. It connects to a light-emitting diode (LED) or laser diode made of a compound semiconductor. A Schottky barrier diode with a silver electrode is used as the photodetector. The light guide layer is produced on a silicon on insulator (SOI) wafer that is attached to the wafer holding the logic circuits, both with face-to-face electrodes.

Connections between the light-guide chip and logic IC are created with a gold-tin (Au-Sn) alloy, which allows for alignment of both electrodes. A previous proposal included optical connections between an optical interconnect wafer and circuit wafer, but that approach was deemed unrealistic because of the difficulty of aligning both light guides.

In the technology developed by Selete, bump electrodes on the silicon wafer are connected to bumps on a light guide wafer, then the silicon substrate of the wafer with the light guides is etched off. The light guide consists of a SiON layer with a refractive index that is slightly higher than the surrounding SiO2 cladding layer. The refractive index of the silicon layer is ~40% higher than that of SiO2. The silicon core has a higher transmission loss of 1-3 dB/cm, compared with 0.2-0.3 dB/cm for a SiON core.

[*Source: Semiconductor International*]

EUROSOI NEWS

First Call and Web site now available for the EUROSOI 2009 Workshop

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007) and Cork 2008, EUROSOI 2009 will be held at Chalmers, Göteborg. It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions. EUROSOI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and application-oriented engineers.

Information about the 2009 Workshop is now available at the Workshop web site

http://chalmers2009.eurosoi.org

Abstract submission and registration will be available in October.

CHALMERS

MC2 Microtechnology and Nanoscience

NEWS

CISSOID introduce a new High Temperature Logic Family

CISSOID is a Fabless Semiconductor company, leader in High Temperature Electronics. They develop and sell Integrated Circuits (IC) designed for the highest reliability in the widest range of temperatures. Their products will operate at least from -55° C to +225°C. They have been tested from -200°C to +300°C. The reliability of CISSOID products is based on long years of experience in silicon technologies, design for reliability, assembly techniques and test.

CISSOID products are commonly used under extreme conditions and harsh environments, for example in demanding Oil&Gas, Aerospace and Automotive applications. They enable exploitation of deep oil resources, energy savings in aircrafts and automobiles, optimal exploitation of geothermal resources, etc.

CISSOID proposes a portfolio of High Temperature standard products, such as Voltage Regulators, Voltage References, Clock Generators & Timers, Analog-to-Digital Converters, Amplifiers, High-Voltage MOSFET's and Drivers. Custom solutions can also be developed as an Application Specific Monolithic IC (ASIC) or as a Hybrid multi-chip assembly solution.

Most of CISSOID's products are built on Silicon-on-Insulator (SOI), a fabrication process that offers tremendous advantages for High Temperature operation and high levels of radiation (Rad-Hard products). Cissoid's products inherit over 20 years of R&D activities in the field of SOI and was the very first company to exploit this technology.

[*Source: CISSOID*]

EVENTS

MIGAS International Summer School

This school is addressed to PhD students, engineers and researchers coming both from the university and from industry of the semiconductors. Through a program based on lessons given by the best international scientists, the participants are given the opportunity of improving their knowledge on state of the art and future nanodevices.

Each session is focused on a different theme, and is managed by a different Scientific Chair. This year, for its 11th session, MIGAS'08 has been focused on Nanoscale CMOS and Si-based Beyond CMOS Nanodevices.

The scientific programme for this edition was:

- Advanced materials, technology and characterization methods for nanoscale CMOS.
- Novel CMOS architectures.
- Beyond-CMOS Nanodevices.
- Innovative Memories.

This year the selected venue was Autrans, a reknown resort, dedicated to alpine and cross-country skiing in winter, and to tourism in summer, located in the Regional Natural Park of the Vercors mountains, 30 km away from Grenoble.

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

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If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

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- EUROSOI 2009 Workshop
Chalmers University of Technology
Göteborg, Sweden
January 19th - 21st, 2009
http://chalmers2009.eurosoi.org

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME III

AUGUST, 2008

IN THIS NUMBER:

EDITORIAL

Sorin Cristoloveanu
IMEP, Grenoble (France)

About 8 years ago, I was asking myself a number of questions:

- How prominent will the SOI technology be in the future landscape of the microelectronics?
- How good are we Europeans in SOI?
- How many are we all together?
- Are we collaborators or just competitors?
- What is the quantitative rate and qualitative impact of the European papers at international conferences, and in particular at the IEEE SOI Conference?
- Is there any SOI bridge somewhere in Europe?
- Is there any serious competitor for SOITEC in the arena of SOI wafer fabrication?
- Why the European industry is so shy and does not go into the SOI chip business?
- Why then are LETI and IMEC developing such wonderful technologies?

Over a memorable diner in Granada, Paco Gamiz double checked my calculations. They looked accurate. We asked further verification by our good SOI friends: Olivier (Faynot), Denis (Flandre), Steve (Hall), Bruno (Ghyselen), Stefan (Bengtsson), Francis (Balestra), Jean-Pierre (Colinge… from US) and many others (a bottle of wine for everybody I missed). Anyway, they all confirmed.

The conclusion was straightforward: we need to initiate a European SOI conference. Actually, 'resuscitate' rather than 'initiate'. A European SOI Workshop had been organized already, 2-3 times in Grenoble, in the 80's. It dried out because nobody wished to take the relay in a discipline which, at that time, looked more like a wonderful speculation.

We decided to call this event EuroSOI. Then, Paco said "This is good, as good as any good tapas can be. But just tapas is not enough, we need meat." A few seconds later, the idea of European SOI network emerged. Paco took care of the rest.

We wanted to design a network with whatever ingredients a network can carry. We got in contact with all European SOI groups and the returns rated between positive and enthusiastic. Then we asked benediction from Brussels and you know by now the rest of the story. The EuroSOI network started officially a couple of years later.

EuroSOI workshops were organized yearly with reasonable audience, good papers and, even more importantly, a positive gradient in quality. Selected papers were published in extensive versions in Solid-State Electronics. Since the network performed and well, the European Union Commission gave us a 'plus' and accepted to help us to continue. This is how we became, early this year, EUROSOI+.

We did lots of useful things, at technical and human interaction levels. More can be done and will come next. After reviewing the past and the future, I feel that SOI is like 'Return to Forever'. The problem is that these brilliant musicians do not have a clue about SOI. Why don't we invite them at EuroSOI?

ANNOUNCEMENT

Proposals of Scientific Exchange Visits funded by EUROSOI+ approved

At the end of May, and in the hopes that this initiative —in addition to increasing the mobility possibilities of scientists— will result in an enhancement of collaborations and information exchange, EUROSOI+ launched fundings for scientific exchanges and research visits.

Once the evaluation process finished, and considering that the applications received fulfilled the requirements, the Management Board of EUROSOI decided to approve all of them.

Further information and results can be found at the EUROSOI web site http://www.eurosoi.org.

NEWS

Soitec Ready With Ultrathin SOI Wafers

"The ultrathin SOI layers may permit technologists to create planar structures with a back gate underneath the channel", André-Jacques said.

Soitec (Bernin, France) announced at SEMICON West that it has qualified silicon on insulator (SOI) wafers with ultrathin buried oxide (BOX) and silicon layers. The SOI wafers — named XUT+ to describe the ultrathin top silicon and BOX layers — are aimed at both partially depleted (PD) and fully depleted (FD) devices, including multi-gate transistor architectures, such as finFET and trigate, that may play a role at 22 nm and beyond.

CEO André-Jacques Auberton-Hervé said, "The very thin oxide layer allows backside control [of the channel], which is important for limiting the threshold voltage variability. That is a necessity for embedded SRAMs in particular because the threshold variability is being affected by the difficulty in controlling the number of dopants inside the channel. Even one atom can affect the threshold voltage," he pointed out.

The ultrathin SOI layers may permit technologists to create planar structures with a back gate underneath the channel, providing many of the advantages of finFETs while preserving the easier-to-manufacture planar structure, he said.

Also, the thin BOX is required for the SOI-based floating body cell (FBC) memories being developed by Toshiba Corp. (Tokyo), Intel Corp. (Santa Clara, Calif.) and others. At the recent 2008 Symposium on VLSI Technology in Honolulu, Intel researchers presented research on a FBC memory for embedded cache on microprocessors.

[*Source: Semiconductor International*]

NEWS

Nvidia Joins SOI Industry Consortium

Joining the organization may mean that Nvidia is looking forward to design chips that will be made using silicon-on-insulator technology.

Nvidia Corp., the world's largest supplier of graphics processing units, has joined the SOI Industry Consortium. Joining the organization may mean that the fabless developer of semiconductors is looking forward to design chips that will be made using silicon-on-insulator technology.

"Nvidia is pleased to join the SOI consortium. We are looking forward in participating on the advancement of such an innovative technology and its applications to future products," said John Chen, vice president of technology and foundry operations at Nvidia.

Even though Nvidia is a fabless developer, hence, does not operate its own fabs, it is tremendously interested in rapid development of chip manufacturing technologies and design tools so that to be in position to continue creating leading-edge graphics processing units as well as other chips.

The SOI Industry Consortium, which was formed in October 2007 by a group of companies from across the electronics industry, is aimed at accelerating silicon-on-insulator innovation into broad markets by promoting the benefits of SOI technology and reducing the barriers to adoption.

Nvidia brings the SOI Consortium membership to twenty three companies. Other members include: AMD, Applied Materials, ARM, Cadence Design Systems, CEA-Léti, Chartered Semiconductor Manufacturing, Freescale Semiconductor, IBM, Innovative Silicon, KLA-Tencor, Lam Research, Magma Design, Samsung, Semico, Soitec, SEH Europe, STMicroelectronics, Synopsys, TSMC, Tyndall Institute, UCL and UMC.

The SOI Industry Consortium is open to any company, organization or academic institution with an interest in SOI.

[*Source: X-bit labs*]

EVENTS

European School On Nanosciences & Nanotechnologies

The fifth session of this European school, which will be held this year in Grenoble (France), will begin the fourth week of this month and will last until September 13th.

This 3 weeks course is aimed at providing training for graduate students, postdoctoral and junior scientists from European universities and laboratories in the field of NANOSCIENCES and NANOTECHNOLOGIES in Physics, Biology and Chemistry.
The academic and practical courses cover the elaboration, functioning and characterization of nano-objects. The program emphasizes the role of laboratory courses (half of the program is devoted to practical work).

The proposed programme is endowed with two key points. The first is interdisciplinarity, since research in Nanoscience demands a combination of various skills in physics, chemistry and biology. Learning the basic knowledge necessary to communicate with other scientific communities is a determining ingredient to create new nano-objects and to connect them to the macroscopic world.

The second point emphasises the role of laboratory courses. In general, summer schools do not address this issue which is, however, of fundamental importance both for basic science and for applications.

The program is structured to highlight the fundamental and technological advances in Nanoelectronics and at the interface between Physics and Biology.
The two sessions will run in parallel but they will share common lectures and praticals.

EUROSOI NEWS

First EUROSOI Working Group Meeting

One of the important goals of EUROSOI+ is to boost the exchanges of information about the Fully Depleted SOI Technology developed by LETI (which makes reference to devices that are fabricated on ultra-thin SOI films and coupled with high-K and metal gates).

In this framework, EUROSOI planned the organization of three Working Group Meetings, first of which will be held in Grenoble by October or November. The final date and the list of speakers will be conveniently announced through the next volume of this Newsletter (September) and also through the EUROSOI website.

All EUROSOI+ beneficiaries will attend these meetings and in addition, different experts from the rest of EUROSOI partners and from Industrial Advisory Board members will also be invited.

The global idea is to organize a technical event with several presentations in order to see:

- What is available today with regard to LETI FDSOI technology?
- What would be needed to go further?

ANNOUNCEMENT

SOI Inventory list elaboration

EUROSOI is currently elaborating an inventory of SOI training material in order to create a database of books, publications, short courses… that could be useful to synthesize the present SOI knowledge.

You may forward to eurosoi@ugr.es any material that you consider to be outstanding or just indispensable.

This call is open to all EUROSOI members as well as to other members from the International SOI Community.

EUROSOI NEWS

First Call of the EUROSOI 2009 Workshop

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007) and Cork 2008, EUROSOI 2009 will be held at Chalmers, Göteborg. It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

EUROSOI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and application-oriented engineers.

Information about the 2009 Workshop is now available at the Workshop web site

http://chalmers2009.eurosoi.org

Abstract submission and registration will be available in October.

CHALMERS

EUROSOI NEWS

Short course on Circuit Design

It is becoming urgent to involve design people in next future to work using SOI devices and SOI technology

Last January and in the frame-work of the EUROSOI Workshop held in Cork, it was organized a first short course dedicated to Multi-Gate Silicon on Insulator Technology. The Short Cour-se Lectures were given by world-leading experts and focus on the opportunities offered by Multi-Gate FETs and on the challenges they pose in the field of fabrication, device physics and circuit design.

And now a second short course is being prepared to be held during the EUROSOI 2009 Workshop in Göteborg. One of the main conclusions of the Workshop held in Cork was that it is becoming urgent to involve design peo-ple in next future to work using SOI devices and SOI technology. As a consequen-ce, this second Short Course in Chalmers will be devoted to Circuit Design on SOI substrates.

A final list of lecturers will be announced in September.

The importance and relevance of design is clearly a matter of consideration as can be seen for example in the last num-ber of the *Advanced Substrate News* which devotes several articles to SOI Design written by important figures such as Remy Pottier, Kevin Kranen, Tony Bonaccio or Michael White.

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

CALENDAR

- European School On Nanosciences & Nanotechnologies
Grenoble, France.
August 24th - September 13th, 2008

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Edinburgh, United Kingdom.
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- 2008 IEEE International SOI Conference
Hudson River Valley
New York, USA
October 6th - 9th, 2008

- First EUROSOI Working Group Meeting
Grenoble, France
October-November, 2008

- EUROSOI 2009 Workshop
Chalmers University of Technology
Göteborg, Sweden
January 19th - 21st, 2009
http://chalmers2009.eurosoi.org

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME IV

SEPTEMBER, 2008

IN THIS NUMBER:

HIGHLIGHT NEWS

'Pretouch,' wireless energy: Intel CTO surveys tech future

Intel Corp. is celebrating its 40th anniversary in 2008, and Intel CTO Justin Rattner devoted his keynote address at the Intel Developer Forum on Aug. 21st to "what the next 40 years of technology might look like."

"I'm addressing how we expect to see the gap between human intelligence and machine intelligence close over the next 40 years," said Rattner.

Intel commissioned futurist Ray Kurzweil to describe in a video presentation the quickening pace of technology that "may go exponential in the next few years -- where technology is literally advancing on a moment-by-moment basis." Rattner predicted that CMOS devices would not run out of steam until device designers switched from using electronic charges to encode information to something like the spin of individual electrons -- an advance Rattner said remains in the distant future.

"If you are using charge to represent information, then CMOS is the most efficient architecture," said Rattner. "So our near-term focus is on improvements [in] processing."

Rather than burying circuitry in bulk silicon, Intel said it is progressing with the development of its Tri-gate transistor, a surface device that wraps a 3-D, high-K metal gate around a vertical thin-film channel, which Rattner said the company might turn to at features sizes below 32 nm.

"The important thing is that all these vertical structures will be on the surface, no longer being built in the bulk," said Rattner.

"Once you are on the surface, you could even add III-V materials" like the indium phosphide material Intel uses for its silicon lasers. Beyond CMOS, Rattner predicted that the amount of charge stored for each bit would become so small as device sizes shrink that a new representation for information will be needed -- something besides charge.

"Will future electronic devices be charge-based like they are today for our CMOS technologies, or are they going to rely on some other quantum property like spin? Or might they use some sort of molecular technology where we use molecules to perform the logic function?" Rattner asked.

The Intel CTO also predicted that devices might be possible over the next 40 years that would give robots the ability to behave more like humans. Some devices could endow robots with unique abilities that humans don't have, such as the robotic sense called "pretouch."

Pre-touch "gives robotic hands the ability to sense an object before it touches it," said Rattner. "This is the kind of sense that fish have: Sharks can do it and eels can do it, but if we ever had it as humans we've long since lost that capability."

[*Source: EETimes*]

ANNOUNCEMENT

SOI Inventory list elaboration still in progress

EUROSOI is currently elaborating an inventory of SOI training material in order to create a database of books, publications, short courses… that could be useful to synthesize the present SOI knowledge.

You may forward any material that you consider to be outstanding or just indispensable.

This call is open to all EUROSOI members as well as to other members from the International SOI Community.

NEWS

Market for SOI to reach $1.1B by 2012, VLSI Research reports

Although 2008 sales of SOI are expected to be slightly down from 2007, the following years will see double-digit growths .

Following the general trend of the semiconductor manufacturing ecosystem, sales of SOI (silicon on insulator) technology slowed in 2007 to a 6% year-over-year revenue increase at $654 million. The single-digit growth pales in comparison to the 46% and greater growth in each of the three previous years, according to to Santa Clara, Calif-based VLSI Research Inc.
The market research company pointed out that Soitec continues to be the leading force in SOI with a 67% worldwide market share, followed by number two player Shin Etsu Handotai, which licenses Soitec's Smart Cut technology for the production of its thin SOI wafers.

In 2007, SOI wafers comprised approximately 1.4% of total silicon demand, in terms of area, which is nearly three times what it was in 2002, and since SOI technology is primarily used in high-end consumer devices, demand can be unpredictable, especially when consumer disposable income diminishes. However, VLSI noted that the market as a whole is very healthy and has been growing at a compounded annual growth rate (CAGR) of 36% for the past three years.

Growth of SOI technology is driven by major semiconductor manufacturing node transitions, and since it acts as a technological enabler, SOI becomes the solution because of its ability to create less complicated isolation structures on a circuit, resulting in higher-end devices can be built with each new node transition using SOI, VLSI said.

While 2008 sales of SOI are expected to be slightly down from 2007, the following years will see double-digit growths stimulated by the 45-nm transition by existing SOI users as well as potential new customers.

[*Source: Electronic News*]

Source: VLSI Research Inc

NEWS

THE SOI INDUSTRY CONSORTIUM WELCOMES A KEY IP SERVICES PROVIDER

Symmid Semiconductor and partners see SOI technology as key to low-power solutions in 45nm and smaller geometries.

The SOI Industry Consortium announced at the end of August that Symmid Semiconductor Technology (SST), based in Silicon Valley, California, a provider of ASIC design services and intellectual property (IP) porting, has joined the organization as a technical member. With the addition of SST, the SOI Industry Consortium now comprises 24 leading companies from across the electronics industry covering a spectrum of users, enablers, suppliers and manufacturers. This new addition complements the IP focus of the SOI Industry Consortium.

SST, which is a technology partner for leading foundries, focuses primarily on system-on-chips (SoCs) with the most stringent performance, power and area requirements. The company is also a design partner of Arrow's Custom Logic Solutions (CLS) Group, one of North America's broadest custom logic solutions providers.

"Symmid Semiconductor Technology foresees increased interest in SOI technology for low-power SoC designs. We are excited about our participation in the SOI consortium and we plan to contribute to the momentum of SOI adoption through enablement of IP development and porting," said Alex Parshad, CEO of Symmid Semiconductor.

[*Source: SOI Industry Consortium*]

EVENTS

Third SINANO Device Modeling Summer School

The third summer school on "Semiconductor Device Modeling and Simulation" was held at the beginning of this month (September 1st-5th) at the Summer School facility of the University of Bologna, located in Bertinoro, a picturesque medieval village.

The SINANO Summer School was held in 2005 and 2006 in the framework of the SINANO European Network of Excellence, and is currently continued under the auspices of the new NANOSIL Network of Excellence and of the Integrated Project PULLNANO, two European research initiatives bringing together the top European Universities, Research Institutes and Companies with expertise in advanced Nano-CMOS technology, devices and simulation.

This school consists of a comprehensive set of classes aimed at doctoral level researchers from both industry and academia, taught by world's leading experts in the fields of device modelling and characterization via a program consisting of lectures, tutorials and advanced discussion groups.

The aim of this Summer School was to further enhance the knowledge of PhD students and postdoctoral researchers in the advanced modeling, simulation and characterization techniques amenable to conventional and novel nano-CMOS devices.

The 5 days program of the School were dedicated to the following topics:

- Prospects for further development of CMOS technology
- Transport models for device simulation
- Experimental electrical device characterization
- Analytical and compact models
- Post CMOS devices
- Silicon technology for photo-voltaic energy conversion

EUROSOI NEWS

First EUROSOI Working Group Meeting

One of the important goals of EUROSOI+ is to boost the exchanges of information about the Fully Depleted SOI Technology developed by LETI (which makes reference to devices that are fabricated on ultra-thin SOI films and coupled with high-K and metal gates).

In this framework, EUROSOI planned the organization of three Working Group Meetings, first of which will be held on November 17th-18th in Grenoble. The lecturers participating in this first edition are F. Gámiz, O. Faynot, S. Cristoloveanu, F. Andrieu, A. Asenov and D. Bol.

The global idea is to organize a technical event with several presentations in order to see:

- What is available today with regard to LETI FDSOI technology?
- What would be needed to go further?

The announcement of this meeting can be also found visiting the EUROSOI website http://www.eurosoi.org

CONFERENCES

ESSDERC-ESSCIRC Conferences

The aim of the ESSDERC conference is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and technologies. ESSDERC and its sister conference ESSCIRC, which deals with solid-state circuits, are jointly organised.

The conferences are held this year in Edinburgh, Scotland, from 15-19 September.

For more information and programmes visit the ESSDERC-ESSCIRC web site http://www.essderc.org

EUROSOI NEWS

Fifth EUROSOI Workshop

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007) and Cork 2008, EUROSOI 2009 will be held at Chalmers, Göteborg. It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

EUROSOI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and application-oriented engineers.

Information about abstract submissions and registrations will be announced in the next volume of the EUROSOI Newsletter (October)

For further information and important dates take a look at

http://chalmers2009.eurosoi.org

CHALMERS

EuroSOI

MC2 Microtechnology and Nanoscience

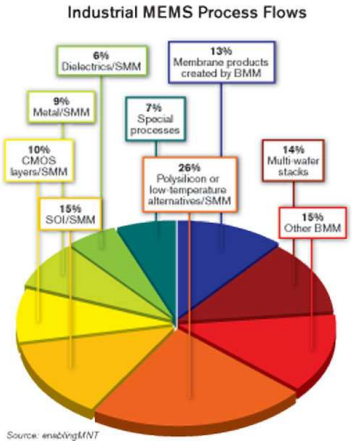
FEATURE

Diversity in MEMS Processing

Diversity is good, but is more diversity better? Diversity enables a species to survive, it weeds out dead-end developments, and it's a source of seemingly infinite improvement. So is more better? Not always, at least from a processing/production point of view. Let's look at MEMS: how many processes already exist or are proposed as production technologies? Does every MEMS product have its own technology as some believe? Is it good to have such diversity in MEMS processing? Is the MEMS world becoming more or less diversified in terms of technology? To find answers to these questions, over 110 MEMS processes from established MEMS suppliers, start ups, universities, etc. have been analyzed. Surprisingly, from all these products only a few (7) can be regarded as product/company unique. The rest can be more or less easily divided into standardized process techniques.

So what are the differences between these processes? You don't need much to make a MEMS device: a free-hanging structure, a construct to detect the movement of the free-hanging part, and, as always, some electronics. To make a free-hanging structure you need a suitable material: a structural layer and a process to remove the material around that layer (sacrificial etching). If material is removed from the substrate, the process is called bulk micromachining (BMM), and if deposited layers are removed, the process is called surface micromachining (SMM).

The process you will choose is of course very much product-based. Pressure sensors are still mainly created using BMM, accelerometers and gyroscopes by polysilicon-based SMM (or low-temperature alternatives), RF MEMS products by metal SMM, and microphones by dielectric-based SMM. If you decide to build a micropump with MEMS technologies, using multi-stack wafers structured with BMM is the technology of choice.



[*Source: R&D Magazine*]

For the beginning of 2009 a second short course is being prepared to be held during the EUROSOI Workshop in Göteborg

EUROSOI NEWS

Short course on Circuit Design

A second short course like the one celebrated last year in the framework of the EUROSOI Workshop held in Cork is being prepared to be held during the EUROSOI 2009 Workshop in Göteborg.

One of the main conclusions of the Workshop held in Cork was that it is becoming urgent to involve design people in next future to work using SOI devices and SOI technology. As a consequence, this second Short Course in Chalmers will be devoted to Circuit Design on SOI substrates.

A final list of lecturers will be available in mid-september and announced in the following number of this Newsletter.

EVENTS

2008 EUROPRACTICE Workshop

The "Europractice" brand has become synonymous with high quality Microelectronics and Microsystems services in Europe.

The Europractice Workshop is an ideal opportunity to meet and exchange ideas with colleagues from different European service oriented projects. This year the workshop was held at IMEC, Leuven (Belgium) September 4th and arranged to cover the following topics:

- Overview of Europractice service projects, showing how multiple projects are working together to provide an overall service.
- Update from each EC service projects: what's new, services offered, success stories etc.
- Discussion: identify best practice and learn from the experiences of other EC projects, how projects can work together, define actions for moving forward.

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

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THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME V

OCTOBER, 2008

IN THIS NUMBER:

HIGHLIGHT NEWS

AMD and Advanced Technology Investment Company of Abu Dhabi to Create New Leading-Edge Semiconductor Manufacturing Company

AMD and the Advanced Technology Investment Company (ATIC) of Abu Dhabi announced the creation of a U.S.-headquartered, leading-edge semiconductor manufacturing company to address growing demand for independent, leading-edge foundry production capabilities. The new global company, to be temporarily called "The Foundry Company", will serve this need by combining advanced process technology, industry-leading manufacturing facilities and aggressive plans to expand its global capacity footprint. At the same time, the Mubadala Development Company will increase its current investment in AMD to 19.3 percent on a fully diluted basis.

AMD will contribute to The Foundry Company its manufacturing facilities, including two fabrication facilities in Dresden, Germany, as well as related assets and intellectual property rights. ATIC will invest $2.1 billion to purchase its stake in The Foundry Company, of which it will invest $1.4 billion directly in the new entity and the remainder will be paid to AMD to purchase additional shares in The Foundry Company. The Foundry Company will also assume approximately $1.2 billion of AMD's existing debt. ATIC has committed additional equity funding to The Foundry Company of a minimum of $3.6 billion and up to $6.0 billion over the next five years to fund the expansion of The Foundry Company's chip-making capacity beyond the manufacturing facilities initially contributed by AMD. These funds will be used by The Foundry Company to (i) proceed with capacity expansion at its fabs in Dresden, Germany, including an upgrade of one of its fabs to a state-of-the-art facility, and (ii) begin construction on a new state-of-the-art facility in Saratoga County, New York, subject to the transfer of previously-approved New York State incentives. The New York facility is expected to create more than 1,400 direct jobs, and, through its operation, to generate an additional 5,000 jobs in the region. Once operational, the New York facility will be the only independently-managed, leading-edge semiconductor manufacturing foundry in the United States.

The Board of Directors of The Foundry Company will be equally divided between representatives of AMD and ATIC. AMD will own 44.4 percent and ATIC will own 55.6 percent of The Foundry Company's fully-converted common stock upon its formation.

"Today is a landmark day for AMD, creating a financially stronger company with a tightened focus," said Dirk Meyer, president and chief executive officer of AMD.

The Foundry Company will join the IBM joint development alliance for both silicon-on-insulator (SOI) and bulk silicon through the 22nm generation. The alliance consists of a group of leading semiconductor companies collaborating on next generation silicon technologies.

[*Source: AMD*]

ANNOUNCEMENTS

First FDSOI tutorial of the EUROSOI Network and Second Call for the Chalmers Workshop

EUROSOI has launched two outstanding announcements for this month.

The first one is the Second Call for the EUROSOI 2009 Workshop and the opening of abstract submission and registration process online.

The second is the first announcement of the FDSOI Tutorial to be held in Grenoble from 17-18 November.

More information on page 3

NEWS

The SOI Industry Consortium launches SOI Implementation Guide

The SOI Implementation Guide features a series of white papers and presentations to promote a common understanding of the value and challenges of SOI .

The SOI Industry Consortium, focused on accelerating silicon-on-insulator (SOI) innovation into broad markets, announced today the availability of the first chapters of its SOI Implementation Guide. The SOI Implementation Guide features a series of white papers and presentations from industry experts on specific topics to promote a common understanding of the value and challenges of SOI.

"Education is key to reducing barriers to adoption. Having easily accessible information is essential to providing the knowledge and expertise needed to inform the industry and eliminating present misconceptions," said Horacio Mendez, executive director of the SOI Industry Consortium. " The ongoing creation of chapters for the SOI Implementation Guide represents great teamwork and individual contributions from the companies and academic and R&D organizations within our consortium."

SOI process technologies have been used to implement high-performance, cutting-edge, custom designs, such as microprocessors, for several process generations. The benefits of SOI demonstrated by these designs – higher performance with the same power consumption, or lower power consumption with the same performance – have made SOI an attractive alternative for more mainstream designs as well.
The SOI Implementation Guide features subjects such as a methodology for comparing bulk and SOI process technologies for design teams investigating the potential benefits of SOI. Another chapter addresses the partially depleted SOI circuit design advantages such as improved chip performance and lower power consumption, as well as the design issues raised by the bulk CMOS circuit design community. Other upcoming chapters will cover subjects such as an SOI overview and assessment for Analog and Mixed Signal (including 6 individual chapters on the application of SOI to RF and Analog), SOI cost analysis, FinFets and SOI, SRAM scalability in bulk and SOI, followed by a guide on how to port IP from bulk to SOI.

[*Source: SOI Industry Consortium*]

CONFERENCES

2008 IEEE International SOI Conference

The IEEE International SOI Conference is the premier meeting of engineers and scientists dedicated to current trends in Silicon-on-Insulator technology and provides a forum for open discussion in all areas of silicon-on-insulator technologies and their applications.

The IEEE Electron Devices Society sponsored the 34th SOI Conference (6 – 9 October, 2008) at the Mohonk Mountain House in the beautiful Hudson River Valley in upstate New York.

The areas of focus in this edition were:

•SOI device physics and modeling

•Manufacturability and process integration of soi devices

•Low-power SOI technology and circuit design infrastructure

•SOI circuit applications (high-performance mpu, sram, asic, high-voltage, rf, analog, mixed mode, etc.)

•SOI double & multiple gate/ vertical channel structures; other novel SOI structures

•New SOI structures, circuits, and applications (3d integration, displays, microactuators, novel memories, optics, etc.)

•SOI reliability issues (hot-carrier effects, radiation effects, high-temperature effects, etc.)

•SOI material science/ modification, material characterization, manufacture, and substrate engineering.

•SOI sensors, MEMS and RFIDs technology and applications

EVENTS

First FDSOI tutorial of the EUROSOI Network

One of the major objective of EUROSOI+ network is to coordinate the elaboration of European platform dedicated to Low Power applications. This platform will use the Fully Depleted SOI technology developed at CEA-LETI. Training on SOI devices and on FDSOI technology is also a strong objective of EUROSOI+. 3 tutorial events will be organized during the project. This first one, organized in Grenoble from 17th-18th November is dedicated to the training of European scientists on Fully Depleted SOI technology.

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(1) Devices physics

(2) Technology description

(3) Modeling and circuit design

(4) Variability issues

(5) FDSOI platform development status.

The organizing committee is formed by Olivier Faynot (Chair) and Sorin Cristoloveanu (Co-chair). And the steering committee is composed by Francisco Gámiz (U. Granada, SPAIN), Cor Claeys (IMEC, BELGIUM), Jean-Pierre Colinge (Tyndall, IRELAND), Sorin Cristoloveanu (IMEP, FRANCE), Olof Engström (Chalmers, SWEDEN), Olivier Faynot (CEA-LETI, FRANCE), Denis Flandre (UCL, BELGIUM) and Andrés Godoy (U. Granada, SPAIN)

Information about registration and accommodation can be found at the EUROSOI web site. This tutorial is free of charge for the EUROSOI+ members.

EUROSOI NEWS

Visionary Rump Session

In the framework of the next EUROSOI Workshop to be held next January in Göteborg, Sweden, a Visionary Rump Session has been arranged. This session will be about *"SOI as a fuel injection along the More Moore road"* and is Sponsored by the European FP7 Network of Excellence NANOSIL.

The Panel of Speakers will be announced soon through this EUROSOI Newsletter and through the EUROSOI 2009 Workshop website.

CHALMERS MC2 Microtechnology and Nanoscience

EVENTS

First SOI Industry Consortium Event

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The Programme will include:

•A keynote from John Chen, VP, Technology and Foundry Operations at NVIDIA on graphics silicon technology needs and its impact on SOI.

•Methodology breakout sessions presented by members covering subjects such as SOI vs. Bulk future challenges, SOI power, frequency and area considerations, and SOI cost analysis.

•A select press panel and one-on-one interviews for members interested.

The announcement of this event can be also found visiting the SOI Consortium website http://www.soiconsortium.org/

EUROSOI NEWS

Second Call for the EUROSOI 2009 Workshop

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007) and Cork 2008, EUROSOI 2009 will be held at Chalmers, Göteborg. It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

EUROSOI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and application-oriented engineers.

Abstract submission and registration are now available online at the Workshop website as well as new information about the programme, fees, accommodations…

For further information and important deadlines take a look at

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CHALMERS MC2 Microtechnology and Nanoscience

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

CALENDAR

- 2008 IEEE International SOI Conference
Hudson River Valley
New York, USA
October 6th - 9th, 2008

- First SOI Industry Consortium Event
Santa Clara, California
November 11th, 2008

- First FDSOI Tutorial
Grenoble, France
November 17th-18th, 2008

- EUROSOI 2009 Workshop
Chalmers University of Technology
Göteborg, Sweden
January 19th - 21st, 2009
http://chalmers2009.eurosoi.org

- 39th European Solid State Device Research Conference and 35th European Solid State Circuits Conference
Athens, Greece.
September 15th - 19th, 2009

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME VI

NOVEMBER, 2008

IN THIS NUMBER:

EDITORIAL

Francisco Gámiz
Professor
Univ. Granada (Spain)

EUROSOI is moving.

After these first months of taking off, EUROSOI+ network faces important challenges for the successful achievement of its goals. It's then time to put our shoulders to the wheel and strongly work together.

One of the ultimate goals of this network is the spreading of SOI technology all over Europe, and all over the World: "We want that SOI technology is reachable to any European research group or Fabless Semiconductor company; we want that any circuit design has the chance to become a SOI circuit using European technology." It is widely accepted by the International Semiconductor Community that most of the electronic circuits (in the whole application spectra) will have a better performance, and therefore, they will be more competitive, if they are built using SOI technology. However, nowadays it is not easy to have access to this technology, even when we count in Europe with some of the most advanced SOI technologies all over the World.

Up to now, a lot of research activities have been pursued in Europe around SOI at different levels: substrate, device, and circuit. Since few years, advanced SOI technologies have been developed in research labs in order to address the downscaling required for 32 nm nodes and below. Today such researches are mainly dedicated to technology development. Among the various ones, we can mention the LETI Fully Depleted SOI technology (developed with high-k and metal gate) that currently has enough maturity to be evaluated at circuit level. So, it becomes obvious that a research-dedicated platform is necessary in order to address the circuit design aspects, focussing on the advantages of such technology for Low Power applications. Access to such platform is a long-time wish of European researchers. Hence, the main goal of EUROSOI+ is to coordinate the formation of such research-dedicated platform which will provide, through the integration in EUROPRACTICE, prototyping and Multi-Project-Wafers (MPW) in SOI open to all European companies using LETI SOI process in two-three years. We are co-ordinating all the activities which will make this platform a reality in 2010. Some steps have already been given: for example, from the beginning of 2008, LETI has provided processed Fully Depleted SOI devices (fabricated on ultra-thin SOI films and coupled with high-k and metal gate) to different EUROSOI partners. On November 17th-18th, Dr.Olivier Faynot from LETI is organizing in Grenoble a tutorial (free of charge for the EUROSOI members) focused on the training of European scientists on Fully Depleted SOI technology. Well recognized technologists, as well as international experts on devices and circuit design will train the attendees on SOI specific aspects. Specific topics include: (1) Devices physics; (2) Technology description; (3) Modeling and circuit design; (4) Variability issues; (5) FDSOI platform development status. (http://www.eurosoi.org/conferenceinfo.asp?id=43).

Another important event organized by our network is the EUROSOI Workshop, an international forum to promote interaction and exchange between research groups and industrial partners involved in SOI activities all over the world. It includes a one-day tutorial followed by two days of regular conference format. The Fifth Edition of this successful meeting will be held in Goteborg, Sweden on January 19th-21st,2009, organized by Prof. Olof Engstrom from Chalmers. As usual, Prof. Engstrom has carried out a very professional work and has managed to bring to us very-well known specialists in hot topics such us electron devices using graphene on insulator, low-power and RF SOI circuit design, or a discussion about FinFET vs DGSOI vs. Bulk.

The deadline for paper submission is November, 15th. (http://chalmers2009.eurosoi.org/documents/Eurosoi2009-3rdCall.pdf).

I strongly encourage all of you to join us in this exciting adventure. And remember: "if we achieve EUROSOI objectives, we will modestly have contributed to a better Europe".

ANNOUNCEMENT

Second Announcement for the First FDSOI Tutorial of the EUROSOI Network

The Second Announcement for the FDSOI Tutorial to be held in Grenoble from 17th-18th of this month was launched at the end of October and can be found on the EUROSOI website.

Registration process for this Tutorial is also open through the online form that can be found with the Second Announcement.

(Continues on page 3)

NEWS

Freescale in 45nm SOI production

"We're bringing up the first 45nm SOI products as we speak", said Rich Beyer.

Freescale is bringing out its first 45nm SIlicon On Insulator (SOI) products and says it will be one of the first companies to use 32nm SOI processes.

"We're bringing up the first 45nm SOI products as we speak", said Rich Beyer, Chairman and CEO of Freescale at the Freescale Technology Forum 2008 in Paris. The first 45nm products are network processors.

Compared to bulk CMOS, SOI adds 30 per cent more performance at the same level of power dissipation, or 30 per cent less power for the same level of performance.

The 45 nm process was developed at Crolles 2 in association with NXP and STMicroelectronics before the alliance desintegrated at the beginning of the year, and Freescale went off to join the IBM process alliance.

Asked if Crolles was quicker to finalise its 45nm process than IBM, Beyer replied: "They're at par".

Beyer is happy with his fab-lite strategy. "It's inappropriate to build a 300mm fab", said Beyer, "so many of our products do not require advanced geometries, for instance analogue, microcontrollers, and some of the industrial products. We have eight inch and six inch fabs, we have a significant amount of production capacity. If you exclude wireless, you don't need to be at the cutting edge of advanced CMOS".

Asked if his fab-lite strategy was vulnerable to the foundries cutting back capex to force up wafer prices, Beyer replied: "The argument that says they're cutting back on capex so there'll be a massive shortage of wafers is not true. Whenever you have a discussion with a foundry they're always out of capacity. Then you get a call: 'Do you need any more wafers?' It's a natural part of our industry".

[*Source: ElectronicsWeekly*]

NEWS

e2v hits twice with new dual-core integrated processors for extended-reliability applications

The PC8641D and the PC8572 are extended-reliability versions of the MPC8641D and MPC8572 from Freescale Semiconductor.

e2v announced the availability of two dual-core integrated processors. The PC8641D and the PC8572 are extended-reliability versions of the MPC8641D and MPC8572 from Freescale Semiconductor, the latest and fastest high-reliability devices born of the long-standing partnership between e2v and Freescale Semiconductor.

These two dual-core devices were designed to service massive data processing embedded applications, including radars, flight computers and graphic displays, where reliability over severe environmental conditions is a key success factor. Both products are manufactured on Freescale Semiconductor's 90nm silicon-on-insulator (SOI) CMOS process technology.

"Aerospace and defence system designers are requiring extreme computing performance combined with efficient system connectivity and reliability", said Eric Marcelot, e2v's Hi-Rel Microprocessors Marketing Manager. "The PC8641D delivers unsurpassed performance to complete the most demanding computational tasks thanks to its AltiVec™ vector processing unit. Both the PC8641D and the PC8572 System-on-Chip (SoC) platforms allow system designers to solve their most complex system integration challenges".

The MPC8641D features two superscalar e600 cores running at up to 1250 MHz in a military temperature range of -55°C to +125°C. The e600 core has a 128-bit vector processing unit that is capable of performing data-intensive mathematical functions similarly to a digital signal processor. With 1MB of backside L2 cache for each core, combined with a dual 64 bit DDR2 memory controllers, the 8641D reaches and extremely high bandwidth capability. Also, the 8641D features a broad variety of system interconnect and communication interfaces including a 4-lane Serial RapidIO port, two 8-lane PCI-Express ports and four Gigabit-Ethernet controllers. The PC8641D dual e-600 integrated processor is now available in both industrial and military temperature ranges.

[*Source: e2v*]

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Online registration and information about accommodation can be found at the EUROSOI web site. This tutorial is free of charge for the EUROSOI+ members.

REMEMBER:

Abstract submission deadline for the EUROSOI 2009 Workshop is 15th November.

EUROSOI NEWS

Abstract submission and registration for the EUROSOI 2009 Workshop

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EUROSOI ANNOUNCEMENT

SOI Inventory list elaboration in progress

EUROSOI is currently elaborating an inventory of SOI training material in order to create a database of books, publications, short courses… that could be useful to synthesize the present SOI knowledge.

You may forward any material that you consider to be outstanding or just indispensable.

This call is open to all EUROSOI members as well as to other members from the International SOI Community.

EUROSOI ANNOUNCEMENT

EUROSOI+

fundings for exchanges aimed at scientists in order to enhance collaborations and information exchange.

EUROSOI+ will fund exchanges in terms of travelling and research visits for scientists (students and senior scientists) in order to enhance collaborations and information exchange. Priority will be given to visits involving an industrial partner to allow a better integration of the European industry in the Network.

These visits must be carried out during the first semester of 2009.

To apply send a proposal to Andrés Godoy (agodoy@ugr.es) before December 17th, including a short CV, an invitation letter from the institution to be visited and a comprehensive description of the visit (purpose, destination, duration, budget, etc). The following requirements must be fulfilled:

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- At least one EUROSOI member should be involved in the project research.
- Priority will be given to industrial partners.
- Less than 4 weeks.
- Gender aspects will be considered (promote the participation of women).
- Not salary costs or expenses generated by research activities.
- The visit should be carried out before the end of June 2009 (remember that there will be another call for proposals in May 2009, November 2009 and May 2010).

After the visit (less than one month), the participant should provide a report describing the work developed during the visit. Please, take into account that each visit must be shorter than 4 weeks.

The Management Board in its next meeting will decide which proposals are funded.

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- First SOI Industry Consortium Event
Santa Clara, California
November 11th, 2008

- First FDSOI Tutorial
Grenoble, France
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September 15th - 19th, 2009

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME VII

DECEMBER, 2008

IN THIS NUMBER:

EDITORIAL

Olof Engstrom
Chalmers Univ. Of Technology (Sweden)

Will SOI be the fuel for driving future nanoelectronics beyond the observable horizon of terrain described by the Roadmap? At the Fifth EUROSOI Workshop, which takes place at Chalmers University of Technology in Goteborg, Sweden on January 19 – 21, 2009, the question will be brought up in a separate discussion. A panel of specialists will be moderated by Sorin Cristoloveanu and the opinions will be aired by Jean-Pierre Colinge, Jerry Fossum, Cor Claeys, Bich-Yen Nguyen, Francis Balestra and Olivier Faynot. The headline of the debate is : *What is the killing advantage of multiple-gate SOI MOSFETs: electrostatics and scalability, transport or functionality?*

The necessity of making the silicon layer of SOI material thinner has been found to be counteracted by new mechanisms for charge carrier scattering decreasing the channel mobility of transistors. How far can it go? The ultimate limit is of course a one atomic layer thick material. Here graphene is a possibility that lies near at hand for further investigations. In the Tutorial on January 19th, Max Lemme from Harvard University will discuss this possibility. The Tutorial, which is defined by the title SOI from modelling to design, also includes Luca Selmi to talk about modelling, Siegfried Mantl on strained channel material, Jean-Pierre Raskin on SOI design for RF applications, Julien Arcamone to speak about MEMS/NEMS on SOI materials, Jean-Pierre Colinge on a comparison between partially and fully depleted SOI and David Bol about digital SOI design. After such an inflammatory day the heating system of the Chalmers localities probably will need to be switched off, in spite of the January weather outside. A reception party, therefore, is offered to relax the participants.

The Workshop in the following couple of days will present two invited talks and more than 50 regular papers. Jerry Fossum will continue along the line of the panel discussion and compare SOI FinFETs with the corresponding structures prepared in bulk. Also, Stéphane Monfray from ST Microelectronics will give an interesting industrial view of thin film devices for low power applications. Of the regular contributions, about one half will be given as oral presentations and one half as posters.

An often appearing expression these days is « the end of the CMOS era ». Can we really percieve that ? I think, that *(i)* the three-terminal device and *(ii)* the complementary transistor pair and *(iii)* the inverter idea all will have long lives, far beyond the fields that we can observe around ourselves today. It is just a matter of choosing the right materials. Do you agree or not ? In any case, welcome to discuss it at EUROSOI 2009!

(Olof Engstrom is Chairman of the Organizing Committee)

ANNOUNCEMENT

Third Call and Programme now available for the EUROSOI 2009

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EUROSOI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and application-oriented engineers.

A detailed programme as well as the third call for the Workshop are now available online at the Workshop website

For further information take a look at:

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CHALMERS

MC2 Microtechnology and Nanoscience

NEWS

IBM Extends Reach of Silicon on Insulator

"Today's [10th Nov.] announcement is a progression of this deep experience, providing a world-class resource for the industry to build on this proven, next-generation technology." said Mark Ireland.

IBM announced immediate availability of the semiconductor industry's first 45-nanometer (nm) Silicon on Insulator (SOI) foundry offering. The new offering adds industry-standard design tools and libraries to the intellectual property (IP) already available through IBM's existing SOI development infrastructure, and allows a wide range of client designs to take advantage of SOI's benefits. IBM testing has shown the potential for 45nm SOI to offer up to 30 percent performance improvement or 40 percent power reduction when compared to the industry-standard bulk complementary metal-oxide (CMOS) technology.

IBM was the first company to begin commercially shipping SOI technology in its server products during the 1990s. Custom designs for key clients took SOI to the market in a variety of applications including gaming, where IBM's SOI technology is currently used by all the major gaming providers continuing to help transform the gaming industry. Following the introduction of IBM's 45nm Cu-45 Application-Specific Integrated Circuit (ASIC) SOI offering to customers a year ago, the announcement of the 45nm SOI foundry access completes the SOI technology rollout to the industry.

"45nm is our 6th generation of SOI technology and is a key driver in many collaborative designs with clients – including networking, storage, gaming and other consumer applications," said Mark Ireland, vice president, IBM Semiconductor Platforms. "Today's [10th Nov.] announcement is a progression of this deep experience, providing a world-class resource for the industry to build on this proven, next-generation technology."

"This announcement from IBM, the industry leader in SOI technology, will continue to proliferate the adoption of SOI technology beyond the traditional high-end segment," said Horacio Mendez, executive director, SOI Industry Consortium.

[*Source: IBM*]

NEWS

ARM Announces Industry's First Silicon-On-Insulator Physical IP Library For IBM's New 45nm SOI Foundry

"With today's [10th Nov.] announcements, ARM and IBM have together taken the first step toward [...] making SOI a viable alternative for many more applications", said Joanne Itow

ARM announced the industry's first Silicon-on-Insulator (SOI) physical IP library including standard cell, memory and I/O libraries for IBM's fully enabled 45nm SOI foundry, also announced today. As lower power levels and increased system-on-chip (SoC) performance become more difficult to achieve with a traditional bulk CMOS process, SOI technology enables up to 30 percent better performance and 40 percent power savings at existing process nodes. The ARM® SOI library of physical IP is the only design platform of its kind in the industry and promises to significantly ease implementation of SOI technology and bring the benefits of this emerging process to a much wider range of semiconductor companies.

"As semiconductor vendors continue in the race toward higher speeds and lower operating power, an alternative to traditional bulk CMOS technology is critical to the continued evolution of the industry," said Joanne Itow, managing director, Semico Research Corp. "To date, two major barriers have inhibited the broad adoption of SOI as this alternative – foundry capacity and IP library availability. With today's [10th Nov.] announcements, ARM and IBM have together taken the first step toward breaking down these barriers and making SOI a viable alternative for many more applications in networking, storage, communication and consumer applications."

Tom Lantzsch, vice president of marketing for the ARM physical IP division said, "The delivery of our physical IP libraries in support of the industry's very first fully enabled SOI foundry is a testament to ARM's heritage of collaboration to remain at the forefront of technical innovation in the semiconductor industry. Our strong partnerships with industry leaders like IBM and Soitec continue to serve as the cornerstone of our business model and we look forward to working in tandem with them and others to ensure the semiconductor industry can reach new milestones in the battle for more power efficient products."

[*Source: ARM*]

FEATURE

First FDSOI Tutorial of the EUROSOI Network

Francisco Gámiz
Professor
Univ. Granada (Spain)

EUROSOI organized on November 17th-18th a Fully-Depleted Silicon-On-Insulator (FDSOI) tutorial at LETI, Grenoble. First of all, I would like to thank Dr. Olivier Faynot from LETI for the organization of the tutorial. I think it was indeed a very nice event, very profitable because of the quality of the invited speakers, and the quality of the lectures. Prof. Cristoloveanu from IMEP gave us a very nice lecture (as he always does) about the physics of FDSOI, higlighting the benefits of this technology and also the importance of the new characterization techniques which has been and are being specifically developed for these devices. Dr.Andrieu, Dr.O.Rozeau and Dr.A.Valentian from LETI showed us the devices and the first circuits that LETI is designing, fabricating and characterizing using its FDSOI technology. This is the technology chosen for the development of an European technological platform for the design of low-power high frequency circuits, main EUROSOI's goal. We also enjoyed the nice lecture of Prof.Asenov from Glasgow on varibility issues, where he showed the importance of SOI technology from this point of view. Finally, Mr.Bol also gave us some tricks about the design of ultra-low power circuits using FDSOI devices.

In summary, we greatly increased our knowledge on SOI technology, and mainly, in topics such as variability and circuit design. The number of attendees was also a measure of success (more than 45 people attended the tutorial). As coordinator of EUROSOI+ project, I'm particularly happy because I see nearer our goal/dream of having in Europe a technological platform where we (small centers and research groups) can develop and improve SOI circuits. Olivier, thank you very much for a very well-done work.
Thank you very much to all the attendees, thank you very much to the speakers, and specially to Olivier and LETI.

To those who could not attend this tutorial, we will have more in 2009: during the fifht EUROSOI Workshop (January 2009) organized by Chalmers at Goteborg (Sweden) and during MIGAS'2009 in June in Grenoble. I hope to see all you then.

(Francisco Gámiz is Coordinator of the EUROSOI+ Network)

EVENTS

First SOI Industry Consortium Event

The General Member's Forum was held at the TechMart in Santa Clara, California on November 11, 2008. The SOI Industry Consortium Forum is designed to further the consortium's mission of accelerating silicon-on-insulator (SOI) innovation into broad markets by promoting the benefits of SOI technology and reducing the barriers to adoption.

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These visits must be carried out during the first semester of 2009.

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- Priority will be given to industrial partners.
- Less than 4 weeks.
- Gender aspects will be considered (promote the participation of women).
- Not salary costs or expenses generated by research activities.
- The visit should be carried out before the end of June 2009 (remember that there will be another call for proposals in May 2009, November 2009 and May 2010).

After the visit (less than one month), the participant should provide a report describing the work developed during the visit. Please, take into account that:

- Each visit must be shorter than 4 weeks.
- 80€/day for daily allowance and including lodging and travel expenses a maximum of 1400€ per week.

The Management Board in its next meeting will decide which proposals are funded.

This announcement can also be found on the EUROSOI website http://www.eurosoi.org

FEATURE

New IBM 45 nm SOI foundry could open new doors for small devices

SOI is one of the design techniques that IBM's partner AMD has used to its advantage for years in its CPU market war with Intel.

With the handset and small device space being opened up by new platforms such as Android, mobile Linux, and the royalty-free Symbian, opportunities are arising for more vendors -- some of them major players, some of them newer ones -- to come to market with fairly high-performance hardware. But up until recently, the possibility of making a high-performance handset was out of reach for many vendors, including the smaller ones that can't yet even afford completely custom design.

That may have changed yesterday with the entry into the market of manufacturing of a new service from IBM. It's an option that enables companies to license building blocks of technologies from ARM and other suppliers, mix and match them to develop a workable composite design, and then have IBM produce those designs using energy-saving silicon-on-insulator (SOI) processes at the 45 nm level.

"The gap is closing in terms of complexity," stated Duncan Needler, IBM's program manager for semiconductor solutions, in an interview with BetaNews, "and that's a reason why we believe the time has come for SOI."

SOI is one of the design techniques that IBM's partner AMD has used to its advantage for years in its CPU market war with Intel. Historically, Intel's production processes use what's called bulk silicon, which is less expensive to produce. Recent advances by Intel, including a formula for using high-k+metal-gate substances in lithography, have helped solve the power leakage problem in its designs.

IBM, meanwhile, has had SOI as one of many tools in its arsenal; though it also produces chips with bulk silicon for itself and its customers, Needler tells us that SOI already gives its foundry clients most of the benefits of lower lithography levels. That's why going with 45 nm SOI now, rather than waiting for the 32 nm generation to roll around.

[*Source: BetaNews*]

NEWS

IC downturn in 'unknown territory', says Soitec CEO

As the economic crisis continues to wreck havoc on the market, the IC industry is looking down the abyss and attempting to make sense of the stormy climate.

Some compare the current IC cycle to the horrific downturn in 2001, which saw business drop like a rock amid the "dot.com" collapse. Some believe the current IC downturn is worse than 2001--a chilling thought that portends vast losses, layoffs and changes in the chip and fab-tool landscape. Still others indicate it's a media creation and that business is looking up.

Most are bracing for the worst. "This is not a traditional downturn," said one industry veteran, Andre-Jacques Auberton-Herve, president, CEO and chairman of Soitec SA (Bernin, France), a supplier of wafers for silicon-on-insulator (SOI) applications.

"It's a global economic down cycle," he told EE Times. "We are in unknown territory."

[*Source: EETimes*]

FEATURE

SOI Goes Mainstream

IBM and ARM are teaming up to simplify silicon-on-insulator chip development, cutting the time it takes to bring SOI to the next process node and making it more competitive with CMOS.

The big advantage is that SOI is significantly more energy-efficient than CMOS. But the complexity of developing in SOI has deterred many companies. With increasing pressure on electronics companies to reduce the energy consumption of devices, both IBM and ARM see a major opportunity.

"It's been hard for companies to see past the challenges of learning a whole new design methodology," said Joanne Itow, managing director at Semico Research. "They all think SOI has too many idiosyncrasies. ARM's support provides a significant amount of credibility. And the timing is right. If a company starts a design now, they can have a product ready when 45nm reaches a sweet spot in terms of volume and pricing at the foundries."

The deal calls for ARM to provide an SOI physical IP library, including standard cell, memory and I/O libraries for IBM's 45nm SOI foundry. ARM's entry into this market was made possible by its 2006 acquisition of SOISIC, a French company that was developing physical IP for SOI.

[*Source: System Level Design Community*]

EUROSOI Network

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Göteborg, Sweden
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- European School On Nanosciences & Nanotechnologies
Grenoble, France.
August 23rd - September 12th, 2009

- 39th European Solid State Device Research Conference and 35th European Solid State Circuits Conference
Athens, Greece.
September 15th - 19th, 2009

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME VIII

JANUARY, 2009

IN THIS NUMBER:

EDITORIAL

Jean Pierre Colinge
Tyndall National Institute, Cork

When I started to work on SOI, the most advanced personal computer -the Apple II- had a memory of 4kb (upgradable to 8kb). Never in a million years would I have dreamed typing this editorial on an airplane on a sublaptop computer that houses a 16Gb memory SD card the size of a postage stamp. At that time, people were arguing whether CMOS was really better than NMOS and whether 256k SRAMs were too big for any practical application. SOI was then in its infancy. It was highly experimental and exotic and. While the excellent properties of the SOI MOSFET were quickly discovered, the quality of SOI films was so poor that it was basically unconceivable to use SOI for any commercial applications. Twenty years later, SOI wafers are mass produced, microprocessors for PCs and gaming consoles are made in SOI, and so are many automotive electronics parts. When Sony announced the PlayStation 3 (PS3) would use SOI processors, my children told me "Well, for once your SOI stuff is used for something useful….. Do you think Sony will give you free PS3 games?"

Europe has done a lot for SOI technology. Among the pioneering research that originated in Europe, we can name some of the first 3D integrated circuits (a microcontroller with high-voltage transistors) that resulted from a French-Irish collaboration (1988), light emission from porous silicon (England), zero-capacitor DRAM (Switzerland), advanced SOI modeling (Spain, Italy and Scotland) and, last but not least, the great invention that made mass production of SOI wafers a reality: the Smart-CutTM process, invented by Michel Bruel of LETI. Yet, Sony sells the PS3 cheaper in the USA than in Europe, and the US version contains two SOI processors, while the European one contains only one, and, is therefore less performant.

Many people tend to 'conveniently' forget the past and re-invent or rename discoveries that were made and published a few years earlier. We should not forget that a great number of key SOI materials, devices and circuits were invented in Europe. Let me give you a few examples: volume inversion was published by a Grenoble team in IEEE EDL in 1987, but now that volume inversion becomes an important effect in ultrathin devices, you can see it being renamed 'bulk inversion' overseas. The 'gate-all-around' and 'quantum wire transistor' were published by Belgian teams at IEDM and the IEEE SOI Conference and Solid-State Electronics in 1990, 1995 and 1996, respectively. These have since been renamed 'wrapped-around gate', 'nanowire transistor' or 'omega FET'. More recently, transistors based on band-to-band or intraband tunneling that feature sub-60 millivolt per decade subthreshold slope have been invented and published by German (Solid-State Electronics, 2004) and French (Applied Physics Letters, 2003 and 2004) researchers. Now, the device has been renamed 'green transistor' in the US. Sometimes, the renaming of devices can reach comical proportions, like when 'partially depleted devices' were renamed 'non-fully depleted devices', when 'thin-film SOI' were re-baptised 'ultrathin-body SOI' and when variations on the Smart-CutTM process were called 'Smarter-Cut' and even 'Smartest-Cut'.

Anyway, I just had a glimpse at the papers submitted to the EUROSOI 2009 workshop, and I see that European teams are still producing excellent research and great ideas. Congratulations, and keep on with the good work!

ANNOUNCEMENT

EUROSOI 2009. Deadline for registration January, 15th

Almost everything is ready for the EUROSOI 2009 Workshop to be held in Chalmers, Göteborg this month (January 19th-21st).

Complete and detailed information about registration, tourist advices… of this outstanding event can be found on the Workshop website http://chalmers2009.eurosoi.org

Registration process is still open **until January, 15th.**

A final programme can also be downloaded from the EUROSOI 2009 web site.

(Continues on page 3)

NEWS

Leading design house joins the SOI Industry Consortium

"SOI can provide lower power for the same performance, making it a very important technology", said Bhanuprakash Cherukuri, TTM's Senior Vice President for Strategy.

The SOI Industry Consortium, aimed at accelerating silicon-on-insulator (SOI) innovation into broad markets, announced that Time To Market (TTM) Inc., an ASIC design and embedded software services company based in San Jose, California has joined the SOI Industry Consortium. TTM is a fully owned subsidiary of Infotech Enterprises Ltd (IEL), a global technology solutions provider headquartered in India. TTM has completed over 125 ASIC projects for leading electronics companies in the consumer, networking, and communications markets, and is well positioned to leverage SOI for low-power applications across all markets, especially in India's chip design and services sector.

"System-on-chips are both shrinking and getting denser each year, making the power/performance trade-off ever more critical," says Bhanuprakash Cherukuri, TTM's Senior Vice President for Strategy and Head of High Tech Vertical. "SOI can provide lower power for the same performance, making it a very important technology. We look forward to working with the SOI Industry Consortium, helping to bring this technology into the mainstream and making it accessible to our customers."

"We are very pleased to welcome Time To Market as a new member of the SOI Industry Consortium, complementing our focus on SOI design," says Horacio Mendez, executive director of the SOI Industry Consortium. "This addition is key to the overall strategy of the consortium to expand SOI design capabilities. Time To Market's excellent engineering talents will also play a critical role in educating the market and expanding SOI's low-power capabilities in India."

[*Source: SOI Industry Consortium*]

NEWS

Smart Cut™ technology inventor honored

Dr. Michel Bruel is receiving this prestigious award for inventing the Smart Cut™ layer transfer technology.

Soitec (Euronext Paris), the world's leading supplier of silicon-on-insulator (SOI) wafers and other engineered substrates used in the microelectronics industry, reported that Dr. Michel Bruel is receiving today the 2008 Cledo Brunetti Award during a ceremony at IEDM in San Francisco. As a former researcher of CEA-Leti, one of Europe's largest microelectronics research institutes, Dr. Michel Bruel is receiving this prestigious award for inventing the Smart Cut™ layer transfer technology that enabled widespread adoption of SOI for CMOS circuits, and the Soitec success story. Today, Smart Cut technology is supported by over 2000 patents worldwide owned both by CEA-Leti and Soitec, and accounts for 95% of all SOI production wafers.

Bruel's invention is a cost-effective process of atomic precision for slicing an ultra-thin layer and transferring it to another support. As such, it was the critical, pioneering step towards large-scale production of high-quality, high-volume SOI wafers. Today, the success of the Smart Cut technology can be attributed to its suitability for high-volume manufacturing; its inherent flexibility which enables substrates to be tailored to customer requirements; its scalability for future roadmap requirements; its applicability to any wafer diameter and material; and its use of standard IC manufacturing equipment.

The revolutionary nature of Bruel's breakthrough technology was first recognized by two of his colleagues: André-Jacques Auberton-Hervé and Jean-Michel Lamure, who were also CEA-Leti researchers and SOI experts. At this time in the early 1990's, Auberton-Hervé and Lamure had recently launched an SOI wafer-manufacturing start-up called Soitec in Grenoble using an older process technology. However, upon seeing Bruel's layer transfer process, Lamure and Auberton-Hervé contracted with Leti for an exclusive license. Trademarked as "Smart Cut™", the technology made its world debut in 1995, when Dr. Auberton-Hervé announced it at Semicon West.

[*Source: Soitec*]

EUROSOI ANNOUNCEMENT

EUROSOI 2009. Student Grants

EUROSOI+ network will fund students to attend the 5th EUROSOI Workshop to hold in Chalmers (January 19th, 21st) with student grants.

These grants will cover **travel expenses and registration fees up to 750€.**

Applicants have to fulfill the following requirements:

1.- She/he has to present a paper in the workshop (oral or poster).

2.- She/he has to work for an EUROSOI partner.

Interested students, please submit an application letter to Francisco Gamiz by e-mail (fgamiz@ugr.es) with an recommendation letter of your advisor.

All the applications will be studied by the Managament Board.

As soon as the decision is taken, Eurosoi will contact the selected students with instructions for the reimbursement.

EUROSOI ANNOUNCEMENT

SOI Inventory list elaboration in progress

EUROSOI is currently elaborating an inventory of SOI training material in order to create a database of books, publications, short courses… that could be useful to synthesize the present SOI knowledge.

You may forward any material that you consider to be outstanding or just indispensable.

This call is open to all EUROSOI members as well as to other members from the International SOI Community.

ANNOUNCEMENT

Visionary Rump Session

In the framework of the next EUROSOI Workshop to be held this month in Göteborg, Sweden, a Visionary Rump Session has been arranged. The session "What is the killing advantage of multiple-gate SOI MOSFETs: electrostatics and scalability, transport or functionality?" is Sponsored by the European FP7 Network of Excellence NANOSIL.

The moderator of this session will be Sorin Cristoloveanu, IMEP - INP Grenoble MINATEC, and the panel:

- Jean-Pierre Colinge, Tyndall National Institute, Cork
- Jerry Fossum, University of Florida, Gainsville
- Cor Claeys, IMEC, Leuven
- Bich-Yen Nguyen, SOITEC, USA
- Francis Balestra, IMEP - INP Grenoble MINATEC
- Olivier Faynot, IMEP - INP Grenoble MINATEC

REMEMBER:

Registration deadline for the EUROSOI 2009 Workshop is January 15th.

EUROSOI NEWS

Registration for the EUROSOI 2009 Workshop

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007) and Cork 2008, EUROSOI 2009 will be held at Chalmers, Göteborg. It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

EUROSOI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and application-oriented engineers.

Registration is now available online at the Workshop website **until January 15th** as well as new information about the programme.

For further information take a look at

http://chalmers2009.eurosoi.org

CHALMERS

MC2 Microtechnology and Nanoscience

EUROSOI Network

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- 215th ECS Meeting
San Francisco, California.
May 24th - 29th, 2009

- 13th International Workshop on Computational Electronics IWCE 2009
Beijing, China
May 27th - 29th, 2009

- MIGAS International Summer School
Autrans-Grenoble, France.
June 20th - 26th, 2009

- INFOS 2009
Clare College, Cambridge, United Kingdom.
June 29th - July 1st, 2009

- European School On Nanosciences & Nanotechnologies
Grenoble, France.
August 23rd - September 12th, 2009

- 39th European Solid State Device Research Conference and 35th European Solid State Circuits Conference
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THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME IX

FEBRUARY, 2009

IN THIS NUMBER:

EDITORIAL

Francisco Gámiz
Professor
Univ. Granada (Spain)

The fifth EUROSOI Workshop was held in Goteborg from 19th to 21st of January 2009. In this occasion, the Workshop was organized by Prof.Olof Engstrom from Chalmers University of Technology. As in previous editions, the event was a complete success, as shown by the number of attendees (almost 100) and accepted communications (more than 50) and also because of the quality of the contributions. As it is usual in EUROSOI Workshops, the first day was devoted to a training event which was attended by young researchers (more than 30) all over Europe. This year the training course was entitled "SOI from modelling to design", and comprises seven lectures focused in circuit design using SOI technology. During the following two days we had more than fifty contributions which were presented orally or on posters and headed by two invited talks, included discussions on non-planar, multi-gate and low-power devices, strained channel materials, the opportunities in RF, noise effects, radiation hardness and device characterization problems.

Attendants during a coffee break

Prof. Olof Engström

We also wanted to have the point of view of different specialists coming from Industrial Centers and Academia. We had two invited talks given by well-known experts in the field of SOI:

- Prof. Jerry Fossum, University of Florida, USA: "SOI vs. Bulk.Si nanoscale FinFET's"

- Dr. Stephane Monfray, ST Microelectronics, France, "Thin film devices for low power applications"

During the second day of the workshop, Prof.Sorin Cristoloveanu chaired the Panel Discussion "What is the killing advantage of multiple-gate SOI MOSFETs: electrostatics and scalability, transport or functionality?", with the sponsoring of NANOSIL Network of Excellence. During this discussion session Prof. Claeys from IMEC, Prof.Fossum from UF, Dr. Faynot from LETI, Dr.Monfray from STMicroelectronics, Prof.Colinge from Tyndall, and Prof.Balestra from IMEP-MINATEC, debated about the future of the SOI technology.

(*Continues on page 2*)

ANNOUNCEMENT

New Tutorial Section on the EUROSOI Website

Following the efforts that the EUROSOI team is making to improve its work and with the dedication that has been shown thus far, a new section containing the different tutorials held in the EUROSOI Workshops during these past years is now available.

In this section, the different tutorials are organized according to their dates and places and a search engine by years has been also developed. For further details take a look at:

http://www.eurosoi.org/tutorials.asp

Chalmers venue

As in previous editions, we had a rather informal and lively meeting, whose main objective was to discuss the situation of SOI technology in Europe. We had people from the EU, Switzerland, Japan, South Korea, Taiwan, Brazil, Iran, Ukraine, Russia and USA. There were more than 20 students, and several industrial participants from STMicroelectronics, EV group, and Nanofactory Instruments.

Once more, the main conclusion we can draw from this workshop is the importance that the achievement of EUROSOI+ goals will have for the European Semiconductor Industry. In this respect it was highlighted the lack of prototyping capability in SOI in EUROPE, in spite of the fact that European companies have developed the most advanced SOI devices which are not accessible to many fabless companies or research groups whose designs would be much more competitive.

The final outcome of this meeting was a consequence of the quality of the contributions and the spirit of friendly cooperation shown by all the contributors. We wish to thank all of them for their effort. We would also like to thank all the people who enabled this meeting to take place, in particular Prof.Olof Engstrom, and Chalmers University of Technology for its support.

A selection of the contributions presented at the Workshop will be published in a special issue of Solid State Electronics Journal devoted to the Fifth Workshop of the Thematic Network of Silicon on Insulator Technology, Devices and Circuits.

We are already looking forward to meeting you in the Sixth Workshop of EUROSOI to be held in January 2010 in Grenoble, France.

Gala dinner

Profs. Cristoloveanu and Engström

See you next year in Grenoble

(Francisco Gámiz is Coordinator of the EUROSOI+ Network)

NEWS

MOSIS announces IBM's SOI technology

IBM's 12SO 45nm SOI process technology available in low volume MPW service.

The MOSIS Service announced the availability of multiple project wafer (MPW) low volume fabrication services using IBM's sixth generation silicon on insulator (SOI) 12SO technology. System on chip designers (SoC) requiring integration, high speed and low power consumption will now have access to the 45 nanometre CMOS SOI process. Aimed at large SoC applications requiring a high gate count, the SOI technology provides low leakage and higher performance improvement, typically 30%, when compared to bulk silicon. Power reduction gain is in the range of 40%.

Deputy director of MOSIS, Wes Hansford, commented, "As the industry's first 45nm SOI process, this energy saving SOI process is suitable for a broad range of consumer electronics applications such as digital TVs and high end mobile applications. By using our MPW services, organisations can dramatically reduce the cost of sampling devices by having access to this leading edge semiconductor process in low volumes. Multiple designs are aggregated onto one mask set allowing customers to share the overhead costs associated with mask creation, fabrication and assembly."

[*Source: EuroAsia Semiconductor*]

"By using our MPW services, organisations can dramatically reduce the cost of sampling devices." said Wes Hansford.

NEWS

NXP unveils suite of efficient power supply products including GreenChip PFC and SR controllers

NXP Semiconductors, the independent semiconductor company founded by Philips, unveiled a suite of new power management solutions that will reduce power consumption in desktop PCs and laptops for the mass market. The highly efficient GreenChip PFC, GreenChip SR controllers and a portfolio of 30V power MOSFETs in LFPAK will be showcased at the Applied Power Electronics Conference (APEC) in Washington D.C. in February.

With this series of products NXP is demonstrating its continued investment in the development of more energy efficient solutions like the GreenChip family and the trend towards higher efficiency power, resulting in smarter ICs that enable energy saving in end products. "Every additional 1% increase in efficiency can make or break a product and we strive to lead the market in cost efficient, scalable products that are inevitably better for the environment by requiring less power and generate less heat resulting in a 20-30% improved efficiency." said Edwin Kluter, marketing director, Power Solutions, NXP Semiconductors.

[*Source: NXP*]

"Every additional 1% increase in efficiency can make or break a product", said Edwin Kluter

EUROSOI ANNOUNCEMENT

EUROSOI 2009. Student Grants

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These grants cover **travel expenses and registration fees up to 750€.**

After having studied the received applications EUROSOI will contact the selected students with instructions for the reimbursement.

FEATURES

Executive Outlook: Survival and Opportunities in 2009

Ardy Johnson
VP Marketing
Rudolph Tech. Inc.

The semiconductor industry is notorious for its cycles, but this one is different. Of course, one difference is the concurrent meltdown in world financial markets and the consequent reduction in consumer confidence and spending. Some recent forecasts predict that capital expenditures will not return to 2007 levels for at least five years. Consolidation will likely accelerate as weaker companies become acquisition targets or simply cease to exist. In uncertain times, customers will judge more critically a potential supplier's likelihood of survival and record of careful financial management. Well-managed growth and successful acquisitions will become a valuable competitive advantage.

A longer downcycle also brings increased focus on ROI. In shorter cycles, manufactures have used the time to implement new technologies in anticipation of recouping their investment in the next upswing. In this cycle, they will need to be satisfied that they can generate adequate returns. Clearly, this puts renewed emphasis on reduced acquisition and operating costs; faster, better decision making based on higher-quality information from tightly integrated inspection and metrology tools; and smarter, more efficient data acquisition with well-conceived sampling strategies and automated analysis.

We are also approaching the end of a technological era. For almost two decades we have single-mindedly pursued increases in device performance based on decreases in geometry. Few industries have ever achieved the level of coordination in development efforts that we did, indisputably documented by our industry roadmap. But we now find the future less clear, as increasingly difficult and expensive new technologies yield diminishing returns. Development consortiums, alliances and joint development projects have become more important as companies seek to share costs and risks that few can afford alone.

Ludo Deferm
Executive Vice President, IMEC

The worldwide economic crisis will certainly impact the R&D expenditures of commercial companies. During the first phase, they will reduce their internal R&D, giving them an immediate cost reduction. However, we expect that they will try to keep their outsourced R&D to be prepared for when the market ramps up again. They need to be ready with new products to guarantee their market position. Without new products, companies would require at least two years to become competitive again.

Although the current economic forecasts do not look bright, companies will continue to seek new markets. The consumer electronics market, for example, will dramatically expand in the coming years. Communications, entertainment, video-on-demand, multimedia services, gaming, etc. — all require more advanced chipsets with more bandwidth and functionality at lower power and cost. Companies that want a share of this promising market simply have to continue investing in R&D.

The biggest question is "What will happen with the energy market?" In 2008, the photovoltaics market has grown 50%. But how will the solar cell market cope with the economic downturn if demand keeps decreasing? And if governments reduce the grants to stimulate the use of renewable energy sources such as solar cells, a downturn in the energy market may be aggravated. The risk is real that the solar cell industry will become a cyclic industry just as the semiconductor industry due to cycles with larger supply than demand.

A third promising market where I see continuing R&D is the biomedical electronics market. Healthcare regulations and legislation make this a longer-term market. But to reach results and stimulate this market, continued technological developments are certainly needed.

ANNOUNCEMENT

International Summer School on Advanced Microelectronics. MIGAS 2009

MIGAS
International Summer School on Advanced Microelectronics

MIGAS Summer School is designed to foster and promote expertise in new, advanced topics of microelectronics. The aim of MIGAS is to offer every year a forum of detailed presentations on emerging topics of microelectronics.

It is also a unique opportunity for senior and junior researchers to update their knwoledge in a very specific and emerging field. MIGAS brings together scientists from all over the world and from research institutes, universities, R&D small, medium and large companies.

This year 2009 MIGAS Summer School will be held from 21st - 27th June in Autrans-Grenoble, a reknown resort, dedicated to alpine and cross-country skiing in winter, and to tourism in summer, located in the Regional Natural Park of the Vercors mountains, 30 km away from Grenoble.

MIGAS 2009 topic is "*Advanced SOI concepts: from materials to devices and applications*".

The lectures will be given by world-class experts, including: J-P. Colinge (Ireland), T. Hiramoto (Tokyo), A. Zaslavsky (USA), R. Schrimpf (USA), C. Fenouillet-Béranger (STMicroelectronics), A. Asenov (Glasgow),O. Faynot, T. Ernst and B. de Salvo (LETI), F. Gamiz (Granada), S. Cristoloveanu (Grenoble), etc.

Details and information for registration will be soon available on the MIGAS website: http://www.migas.inpg.fr/

IMEP-LAHC Grenoble INP MINATEC POLE D'INNOVATION

FEATURE

European collaboration and structuring in Nanoelectronics

Francis Balestra
IMEP

The European cooperation projects in the Nanoelectronics field are now mainly split between the following programmes:

-CATRENE, for short term activities,

-ENIAC Joint Technology Initiative, for mid term application-oriented activities, and

-FP7 Cooperation projects for long term activities.

In the Framework of the ENIAC Scientific Community Council, a position paper has been recently sent to the European Commission in order to optimise this European structuring. Some of the proposals are mentioned below together with some examples of recently created European entities.

The industry is increasingly relying on new ideas and competences coming from the academic community in order to continue technological innovation in the More Moore, More than Moore and, in the future, Beyond CMOS fields. The integration of MtM structures (sensors, actuators, RF components, biochips, etc.) and Beyond CMOS devices (nanowires, nanodots, carbon electronics, spintronics, molecular devices, etc.) on CMOS platforms will also certainly be needed in order to add functionalities to the ICs and pursue integration down to nm structures. Many new technological options in these fields have been and will be generated from start-ups and innovative SMEs emerging from academic research. This long term research, covering the MM, MtM and BC fields, must be supported now in order to prepare the path for future nanoelectronic technologies, as a 15-to-20 years time frame is usually necessary between the first validation of a new innovative idea and its full demonstration and acceptance into complex systems.

It is worth noting that the Sinano Institute (18 laboratories from 10 European countries) has been created in 2008 in order to ensure the coordination of the Academic Community in the Nanoelectronic field (MM, MtM and BC domains), to establish a durable EU Network of researchers forming a distributed Centre of Excellence, to explore the science and technology aspects for long term applications, to identify the most promising topics for future ICT, to develop high competence levels in Europe and to strengthen the overall efficiency of the European research in Nanoelectronics.

Nanoelectronics research is thus conducted in an arena of multidimensional complexity, spanning everything in the development cycle from idea to realization and in the supply chain from materials science to volume manufacturing. Keeping all stakeholders –industry, research institutes, academia connected and informed is therefore extremely important to achieve and maintain a strong multidimensional value ecosystem for nanoelectronics in Europe.

A substantial European funding is necessary for all the links of this virtuous chain. The supports coming from the ENIAC and CATRENE programs being mainly devoted to short and medium term researches, a substantial funding is needed for long term activities in the FP7 program in the MM, MtM and BC fields. A complementary support is also necessary for medium term research in FP7 in order to preserve the links along the whole value chain in Nanoelectronics research. These different funding will be needed to cover the whole research area underpinning this fundamental technology for the economy of the next decades (today 16% of the world economy is built on electronics products and related services - communication, computing, consumer electronics, health, transport, security, environment, etc. - this percentage is growing every year).

In the framework of the ENIAC Working Group devoted to Research Infrastructures, it has also been proposed to develop three kinds of complementary Infrastructures for nanoelectronics research:

-the flexible one dedicated to proving new concepts (using wafers in the 100-200mm range)

-the pre-industrial one integrating research concepts into complex systems (dedicated to n+2/3 technology nodes, working mostly on 200-300mm wafers)

-and the ones dedicated to the industrial feasibility of demonstrated concepts (e.g. the Grenoble-Crolles and Dresden ecosystems).

The realization of forward-looking ideas needs the so-called flexible research infrastructures driven by the European Academic Community, which will allow rapid screening and test of the explosive diversity of materials, technological options and devices, leading to a first proof of concept of the most promising solutions that will be afterwards applied in pre-industrial and industrial platforms. This infrastructure will be more flexible than the pre-industrial or industrial ones from a viewpoint of possible non-conventional processing and the handling of new materials.

Another important topic concerns the need of a continuous supply of well-educated and entrepreneurial engineers to sustain growth in the nanoelectronics industry. Looking at the new challenges to be addressed, the present number of graduates coming out of European Universities is not enough to maintain Europe's needs for nanoelectronics R&D. Therefore, the European scientific community needs also to address the human capital roadmap for nanoelectronics in Europe, attracting and motivating young scientists and preparing educational programs that deliver new, multidisciplinary skills and that have access to state-of-the-art infrastructures.

A strong European support covering the whole research area will allow Europe to stay in the forefront of the competition in nanoelectronics and will significantly contribute to the objective of making the European Union the most competitive economy in the world.

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Thematic network on silicon on insulator technology, devices and circuits.

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THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME X

MARCH, 2009

IN THIS NUMBER:

HIGHLIGHT NEWS

GLOBALFOUNDRIES Opens for Business

GLOBALFOUNDRIES

GlobalFoundries, a new leading-edge semiconductor manufacturing company formed by a joint venture between AMD and the Advanced Technology Investment Company (ATIC), announced its official launch and outlined plans to drive profound change and expand opportunities in the semiconductor industry. GlobalFoundries is led by an experienced semiconductor management team, including CEO Doug Grose, formerly senior vice president of manufacturing operations at AMD, and Chairman of the Board Hector Ruiz, formerly executive chairman and chairman of the board at AMD. The Company is the only U.S. based global semiconductor foundry and commences operations with approximately 2,800 employees worldwide with headquarters in Silicon Valley.

"The launch of GlobalFoundries represents a historic day for our industry, one which will permanently change the market landscape by launching the world's first truly global foundry services provider," said Doug Grose, Chief Executive Officer of GLOBALFOUNDRIES. "With two committed joint venture partners providing strong technology and capital resources, our company brings a unique set of global capabilities to the market that will enable our customers to fully unlock their potential to innovate."

GlobalFoundries will service the manufacturing needs of AMD and will also offer an expanded roadmap of technologies to third-party customers through its high-volume, global foundry services. This means that for the first time, early access to volume chip production using leading-edge technologies will not just be limited to only high-end microprocessor makers.

"As consumers move to increasingly smaller and more power-efficient devices we need to remain aggressive in our technology development and ensure we have the right foundry partners to get those products to market," said Simon Segars, Executive Vice President and General Manager, ARM. "Through the integration of our own processor and physical IP and our industry collaboration activities we continue to facilitate the adoption of next-generation consumer electronics. We look forward to working with GlobalFoundries as we explore their advanced technology capabilities on the ARM platform to support the growing needs of our customers around the world."

To meet the long-term needs of the industry, GlobalFoundries is proceeding with plans to expand its Dresden, Germany, manufacturing lines by bringing a second 300mm manufacturing facility with bulk silicon capabilities online in late 2009. The Dresden cluster will be re-named Fab 1 with Module 1 initially focused on production of high-performance 45nm Silicon-on-Insulator (SOI) technology, and Module 2 transitioning to 32nm bulk silicon capabilities.

In addition to Fab 1 the company also plans to begin construction on a new state-of-the-art 32nm and smaller features, $4.2B manufacturing facility at the Luther Forest Technology Campus in Saratoga County, NY, in 2009. This new facility will be named Fab 2 and is expected to create approximately 1,400 new direct jobs and more than 5,000 indirect jobs in the region. Once operational, Fab 2 will be the only independently-managed, advanced semiconductor manufacturing foundry in the United States, bucking the trend of manufacturing industries leaving the U.S.

GlobalFoundries is jointly owned by AMD and ATIC

[Source: GlobalFoundries]

ANNOUNCEMENT

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Following the efforts that the EUROSOI team is making to improve its work and with the dedication that has been shown thus far, the new tutorial section is now complete containing the different tutorials held since the first EUROSOI Workshop in Granada in 2005.

The different tutorials are organized according to their dates and places and a search engine by years has been also developed. For further details take a look at:

http://www.eurosoi.org/tutorials.asp

NEWS

Green tech drives ICs beyond silicon

"Now the equation is different, and the industry has a role to play optimizing power use." said Rene Penning de Vries.

The green technology era will drive semiconductor innovations in and beyond silicon across a wide variety of applications, according to Rene Penning de Vries, chief technology officer of NXP Semiconductors in a keynote at the International Solid State Circuits Conference (ISSCC) here.

"The electronics industry has grown by focusing on productivity and using power as a resource in a formula that has resulted in tremendous success in consumer electronics, computing and communications," said De Vries. "Now the equation is different, and the industry has a role to play optimizing power use," he said.

Traditional shrinks in CMOS process technology are not sufficient to meet all the needs of this green era. The new dynamics will drive a wide range of innovations beyond the traditional shrinks in CMOS technology, requiring new kinds of materials and processes, he said.

For example, the pursuit of power-efficient high-volt circuits "silicon-based solutions are coming to an end," De Vries said. "The next breakthrough will be based on new materials and gallium nitride is one of the promising ones," he said

In another example, he briefly described a new silicon-on-insulator circuit to drive a compact florescent light bulb to increase its lifetime and decrease operating temperature. The bulbs are rapidly replacing incandescent lamps, however they have lifetimes limited to less than 10,000 hours and generate as much as 150 degrees of heat.

The NXP technologist also outlined a range of new designs in existing silicon technology that could help reduce growth in greenhouse gas emissions. "The big win we can achieve is in power reduction in end equipment," he said.

For example, he described an improved TV backlight technology that if used in just ten percent of all sets could save 39 terawatt hours of energy per year. That's many times the 1.5 TWh/year NXP uses to make all its chips.

[*Source: EETimes*]

NEWS

IMEC joins the SOI Industry Consortium

IMEC is a world-leading independent nanoelectronics research center headquartered in Leuven, Belgium

The SOI Industry Consortium, aimed at accelerating silicon-on-insulator (SOI) innovation into broad markets, announced today that IMEC has joined the organization as an academic member. IMEC is a world-leading independent nanoelectronics research center headquartered in Leuven, Belgium. It has been active in the field of SOI technologies for more that two decades.

"SOI has long been one of the key routes on IMEC's roadmaps. In semiconductor technology, platform creation is of vital importance in making progress, creating critical mass, and identifying common interests between various players. That is what IMEC is doing, and that is what the SOI Industry Consortium is doing. We support the activities of the consortium and look forward to moving forward together," says Luc Van den hove, Chief Operating Officer and Executive Vice President of IMEC.

"We are extremely pleased to have IMEC as part of the SOI Consortium," says Horacio Mendez, Executive Director of the SOI Industry Consortium. "IMEC is recognized as one of the world's leading semiconductor R&D institutes. The expertise and knowledge they bring to this partnership will be exceptionally valuable in maximizing SOI's capabilities."

IMEC's collaborative CMOS scaling research platform targets technology generations two to three nodes ahead of state-of-the-art IC production. The activities are organized as a cluster of programs enabling very advanced research. Based on its long-standing track record and expertise, IMEC's central focus in these programs is on advanced process module and device research including the exploration of new materials. Beside fundamental studies related to device physics, IMEC is also processing both partially depleted (PD) and fully depleted (FD) SOI devices.

[*Source: SOI Industry Consortium*]

FEATURES

Executive Outlook: Survival and Opportunities in 2009

Martin van den Brink
Executive VP
Marketing and Technology,ASML

Manufacturing chips with features of 32 nm and below brings about significant challenges that will force closer working synergies among all aspects of IC design and production — what we call "holistic manufacturing." In lithography, the immediate challenges will be in double patterning, but the same needs will hold true for extreme ultraviolet (EUV) in the future. In both cases, chipmakers will have to manage operations with smaller margins for error and higher stakes than ever before, and incremental adaptations will not provide acceptable levels of risk and reward.

Currently, design for manufacturing (DFM) is the mainstream approach to chip production — incorporating many manufacturing techniques that are developed and implemented separately for each wafer processing area. For the lithographic process, this entails increasingly complex offline adjustments to mask patterns and shapes before the designs are delivered to the fab. This approach has served well, but it is running out of steam — at 32 nm and below, margins for CD uniformity and overlay approach the atomic level. Therefore, the lithographic process must become more holistic and integrate all of the separate offline disciplines, and it can no longer use a single generic model of one scanner.

A holistic approach must place more emphasis on pushing computational lithography to the fab floor in applying full-chip modeling and analysis to fleets of scanners. Metrology data will be used to further fine-tune the scanners. This is the only way to achieve the needed precision under real-world conditions, and ensure reliable production ramp of future chip designs.

Execution of holistic lithography, of course, is a tremendous challenge — a computational lithography task of the highest order will need to be available to chipmakers. But once implemented, fleets of scanners can be quickly optimized for every layer of every design, and the worlds of design and manufacturing will have moved several large steps closer.

Franklin Kalk
Executive Vice President and
CTO, Toppan Photomasks

Semiconductor industry forecasts agree that 2009 will be a difficult year, with second-half improvement appearing unlikely. Layoffs, financial losses, plant closures and company restructurings have begun to dominate the news, and the challenges for photomask makers mirror the semiconductor industry's malaise.

Downturns have a way of accelerating industry restructuring and forcing difficult decisions. While most visible in memory manufacturing, silicon foundries and EDA companies, the need for consolidation is also evident in mask manufacturing. Reduced trailing-edge demand, which is likely to be permanent, has led to plant closures and delayed investments. Programs to extend optical lithography as far as possible still are pursued, if only to avoid costly and risky technology migrations. But almost everything else is under critical review.

Though the timing is debatable, demand will return for new electronic products to connect consumers to the Internet, each other, and the world around them. According to one forecast, for example, large-screen HDTV sales are expected to soar to 250 million units in 2013, compared with 65 million in 2007.

The semiconductor industry must be prepared to meet the device demand that will accompany such growth. Semiconductor suppliers must invest in new products, processes and services, and streamline their cost structures. Good companies will emerge from 2009 leaner and stronger. And which companies are "good"? Those with the scale, development resolve, organizational stability, and financial resources to exploit the downturn and thrive in the next recovery.

ANNOUNCEMENT

International Summer School on Advanced Microelectronics. MIGAS 2009

MIGAS
International Summer School on Advanced Microelectronics

MIGAS Summer School is designed to foster and promote expertise in new, advanced topics of microelectronics. The aim of MIGAS is to offer every year a forum of detailed presentations on emerging topics of microelectronics.

It is also a unique opportunity for senior and junior researchers to update their knwoledge in a very specific and emerging field. MIGAS brings together scientists from all over the world and from research institutes, universities, R&D small, medium and large companies.

This year 2009 MIGAS Summer School will be held from 21st - 27th June in Autrans-Grenoble, a reknown resort, dedicated to alpine and cross-country skiing in winter, and to tourism in summer, located in the Regional Natural Park of the Vercors mountains, 30 km away from Grenoble.

MIGAS 2009 topic is “Advanced SOI concepts: from materials to devices

and applications”.

The lectures will be given by world-class experts, including: J-P. Colinge (Ireland), T. Hiramoto (Tokyo), A. Zaslavsky (USA), R. Schrimpf (USA), C. Fenouillet-Béranger

(STMicroelectronics), A. Asenov (Glasgow),O. Faynot, T. Ernst and B. de Salvo (LETI), F. Gamiz (Granada), S.

Cristoloveanu (Grenoble), etc.

Details and information for registration will be soon available on the MIGAS website: http://www.migas.inpg.fr/

IMEP-LAHC Grenoble INP MINATEC POLE D'INNOVATION

FEATURE

SOI Technology Goes Mainstream

Ruth DeJule
Semiconductor International

More than a decade ago, the first commercially available devices based on silicon-on-insulator (SOI) technology were introduced in IBM's high-end 0.25 µm servers — the result of a 20-year journey from initial bonding of silicon-on-sapphire substrates. Today, SOI-based products (Fig. 1) can be found wherever speed, functionality and low power consumption are needed, including servers, processors, printers, game consoles, network and storage systems, and ultralow-power applications such as wristwatches and automotive applications. "We are seeing with each new technology generation the market opening up for SOI, driven by client interest and SOI's ability to solve unique problems," said Mark Ireland, vice president, semiconductor platforms at IBM (Essex Junction, Vt.).

To help facilitate market expansion, the SOI Industry Consortium (Austin, Texas) was formed in late 2007, and has 25 members from foundries, equipment manufacturers, IDMs and independent design houses. The objective to ease SOI's transition into the mainstream begins by putting in place the necessary infrastructure and ecosystems.

What makes SOI unique?

Where bulk technologies start with a single-crystal silicon substrate, the SOI starting material has an embedded oxide layer just below the silicon surface. The significance is a reduction in leakage current and power/performance advantages over devices designed and built in bulk wafers.

Internal studies at IBM comparing 45 nm SOI-based circuits to the same circuits in 45 nm bulk yield 30% performance benefit using transistors of comparable leakage. "If higher performance is not required for your design, the SOI advantage can be turned into a lower-power design point," Ireland said. As much as 40% lower power has been demonstrated. Further studies indicate lower soft error rates are also intrinsic to SOI technology, with a 5–7× improvement over bulk.

Furthermore, SOI-based devices generally have better temperature sensitivity so that they can be operated at high temperatures and latchup does not exist because device isolation prevents parasitic bipolar device formation between FETs.

Some advantages over bulk are also seen in processing, such as not requiring complex isolation techniques nor deep n and p channel implantations. As technologies scale, bulk processes must add extra processing steps to implantations and STI modules — overhead that SOI eliminates.

Two types of devices

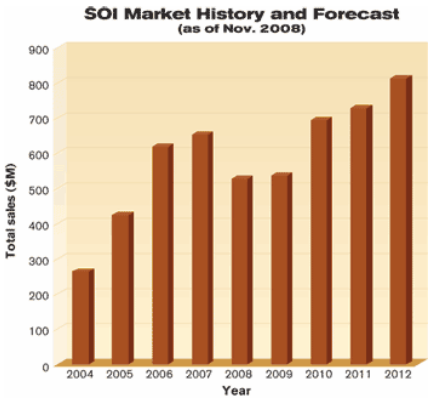
SOI devices can be fully depleted or partially depleted, where the amount of depletion refers to the channel region of a transistor. Partially depleted SOI transistors resemble their bulk counterparts, where doping concentrations in the channel determine the depletion depth, leaving a neutral silicon "floating body" isolated from the grounded substrate residing below the buried oxide.

In contrast, a thin-film SOI transistor in which the depletion region extends down to the buried oxide, leaving no neutral region, is considered fully depleted. Fully depleted transistors require an ultrathin silicon film to control short-channel effects, where the threshold voltage (Vt) depends heavily on the gate length, and in general provide only low-Vt transistors.

Looking ahead

SOI technology can potentially provide the platform for other materials beyond SOI. For example, it could incorporate high-mobility materials such as GaAs and InP, which are extremely expensive and cannot be used as full wafers. Alternatively, they may be placed either on top of SOI or, using the technology, placed locally on the surface to form islands of high-mobility substrates.

Other types of layers have been considered such at putting strained silicon on an insulator to increase device performance by introducing strain into the transistor channel. However, in one demonstration, the remaining strain proved too little to enhance performance in the final transistor product. Strain was introduced more effectively through modifications made during wafer processing. Similarly, IMEC used a substrate with strain upon which to build finFETs, but the strain relaxed completely as fin sizes approached 20 nm, Jurczak said, resulting in only a small performance benefit of 5–10%.



1. The graph indicates a steady increase in revenue after 2009, with the total market reaching ~$800M by 2012. (Source: VLSI Research Inc.)

There is no doubt SOI is an attractive choice for key markets, giving its strong position in the industry. Though the demand for SOI products declined in 2008, this was a reflection of a macroeconomic trend in the semiconductor market in general, according to VLSI Research's Zlatan Kremonic. However, he said, "Stable growth is seen after 2009 (Fig. 1), with the total market reaching ~$800M by 2012, indicating a 22% increase over last year's earnings."

As wafer prices come down and processes are fine-tuned, other consumer markets that push performance with the lowest possible active power — such as digital television and high-end mobile Internet device space — will necessarily opt forSOI-based devices.

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THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XI

APRIL, 2009

IN THIS NUMBER:

HIGHLIGHT NEWS

CEA/Leti and IBM to Collaborate on Future Nanoelectronics Technology

CEA/Leti (the Electronics and Information Technology Laboratory of the CEA, based in Grenoble), and IBM announced that they will collaborate on research in semiconductor and nanoelectronics technology.

This five-year agreement is focused on advanced materials, devices and processes for the development of complementary metal oxide semiconductor (CMOS) process technology for the production of microprocessors and integrated circuits at 22nm and beyond.

With this agreement, CEA/Leti becomes a research associate of IBM and IBM's semiconductor Joint Development Alliance ecosystem centered in Albany, N.Y. CEA/Leti will reinforce this ecosystem through its specific expertise in low-power CMOS (such as SOI technologies), in e-beam lithography and in nanoscale characterization and modelling. This agreement strengthens the links between the IBM and Crolles-Grenoble ecosystems, following STMicroelectronics' decision to join the IBM Alliance in 2007, for the development of core CMOS and value-added application-specific derivative technologies and industrialization of these processes.

"Due to increasing complexity, CMOS technologies can only be developed through global alliances. CEA/Leti chose to partner with IBM since its alliance directly benefits companies with strong industrial activity based in Europe," said Laurent Malier, General Manager of CEA/Leti. "With 22 and 16nm nodes ahead of us, many challenges remain to be tackled and we are strongly committed to speeding up the advent of the best options for these technologies".

"This agreement reinforces the IBM ecosystem of leading companies and research organizations who are working together to achieve significant advances in semiconductor and nanoelectronics technology," said Scottie Ginn, vice president, IBM design enablement and packaging. "This unique model of collaborative development can help accelerate the production of more powerful and energy efficient chips for next-generation computers, consumer electronics and mobile devices."

Complementary expertise

This collaboration will focus on three key areas:

* Advanced lithography for fast prototyping and 22nm chip technology

* CMOS technologies and low-power devices for 22nm chip technology and beyond

* Technology enablement, including innovative nanoscale characterization techniques for research and for the monitoring of manufacturing protocols

This development work will bring complementary expertise to the IBM Research Alliance. Research work will be carried out on CEA/Leti's 300mm silicon platform in Grenoble, as well as at the College of Nanoscale Science and Engineering of the University at Albany, N.Y., STMicroelectronics' facility in Crolles, and IBM's 300mm fab in East Fishkill, N.Y. A team from CEA/Leti will be assigned to work on the program at Albany Nanotech.

[Source: IBM]

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NEWS

LogicVision Announces Memory BIST & Repair Solutions for 45nm SOI Foundry Customers

"The memory test and repair capabilities [...] will assist our foundry customers in achieving their overall quality and yield objectives." said Regina Darmoni.

LogicVision, Inc., a leading provider of semiconductor built-in-self-test (BIST) and diagnostic solutions, announced that IBM Corporation has included LogicVision's ETMemory™ memory BIST and on-chip self-repair solution for embedded memory test and yield improvement within its advanced 45nm silicon-on-insulator (SOI) semiconductor foundry flow. The ETMemory solution will be recommended by IBM to its 45nm SOI customers to assist them in performing their own design work.

LogicVision's ETMemory solution provides a comprehensive, integrated and low area overhead solution for at-speed test and repair of embedded memories. The solution provides automation for integrating and verifying embedded memory test and repair capabilities which not only provide a high quality manufacturing test solution, but also deliver yield improvement through on-chip memory repair analysis and eFuse management.

"In 45nm designs, memory takes up a large portion of the die and, therefore, has a large impact on quality and yield," said Regina Darmoni, Director, Analog/Mixed Signal & Digital Foundry, IBM. "The memory test and repair capabilities provided by LogicVision's ETMemory product will assist our foundry customers in achieving their overall quality and yield objectives."

"We continue to see increasing adoption of our solutions at the deeper technology nodes," said Jim Healy, president and CEO of LogicVision. "Having a technology leader such as IBM adopt some of our key products not only serves as a powerful endorsement, but helps ensure we maintain our competitive edge as we continue to meet their leading edge technology needs."

[*Source: LogicVision*]

NEWS

IBM Ships 50 Millionth Processor for the Nintendo Wii Game System

Microprocessors based on IBM's Power Architecture and SOI technology span applications including, gaming, consumer electronics, networking, computer storage and servers.

IBM has announced that it has reached a significant milestone as the microprocessor supplier for Nintendo Co., Ltd., by completing the shipment of 50 million processors for the Wii(TM) game system, which has tremendous worldwide sales momentum.

IBM first began supplying the processors that serve as the digital heartbeat for Nintendo's Wii in 2006, as part of a multi-year, custom microprocessor design and production agreement. The chips are manufactured at IBM's advanced chip fabrication facility in East Fishkill, N.Y. IBM's worldwide supply chain supported consistent, dependable module deliveries and met strong consumer demand for the Wii console, including through three high-demand holiday seasons.

The chip is based on IBM's Power Architecture® and features IBM's silicon-on-insulator (SOI) technology. IBM's Power Architecture is a semiconductor design platform that offers clients scalability and design customization, while SOI can offer improvements in both chip performance and reduced power consumption, providing energy savings advantages. Microprocessors based on IBM's Power Architecture and SOI technology span applications including, gaming, consumer electronics, networking, computer storage and servers.

IBM partnered with Nintendo to develop and manufacture in volume a custom-designed, high-performance microprocessor to support Nintendo's goals of participatory game play and a compact, energy efficient console.

"We are proud to have achieved this important milestone in supplying the microprocessor for Nintendo's Wii system, which has brought millions of new consumers to the gaming experience," said Brian Connors, vice president, games and power platforms for IBM Microelectronics. "IBM has a long, successful relationship with Nintendo combining silicon technology with game system creativity to deliver winning products."

[*Source: IBM*]

NEWS

The SOI Industry Consortium announces key focus areas for 2009

The SOI Industry Consortium, aimed at accelerating broad adoption of silicon-on-insulator (SOI) across semiconductor markets, announced its key areas of focus for the current year: IP, low power, and the fabless community. These three pillars form the foundation upon which the consortium will orient both internal resources and external outreach. More specifically, the consortium will work to identify and close any remaining gaps in SOI-specific design IP, further quantify and promote the low-power advantages of SOI, and reach out to educate designers, particularly in the fabless community.

"Despite the uncertainty of the global economy, we are looking at significant market opportunities and expansion for SOI. Those that can play the innovation card this year will be the ones ready with the right new products and technologies when the global economy resumes its upward course. I recently visited many companies in the US, Japan and Europe, who are expressing keen interest in the broad cross-section of expertise the Consortium can leverage," says Horacio Mendez, Executive Director of the SOI Industry Consortium. "By focusing on IP, low power and the fabless community, the SOI Consortium is providing the most value both for our members and the industry at large."

A joint survey between the SOI Industry Consortium and the Global Semiconductor Alliance (GSA) last year indicated that low power is the primary driver for designers considering SOI-based solutions. Therefore, both the IP and outreach efforts will put a special emphasis on the green, energy-saving advantages of SOI.

NEWS

Freescale speeds 45-nm processors to market for next-gen wireless equipment

At the Embedded Systems Conference in San Jose, this week, Freescale Semiconductor announced that it has begun sampling communications products based on 45-nm process technology to more than a dozen OEM customers for use in the development of next-generation 3G and 4G wireless infrastructure equipment.

The PowerQUICC MPC8569E processor, the dual-core QprlQP2020 device, and the six-core MSC8156 Star Core DSP devices were sent out for sampling recently. Customer validation activities have continued or are ahead of schedule and volume production is expected to begin by the end of 2009, according to the company.

The PowerQUICC MPC8569E communications processor is a high-performance, low-power device based on 45-nm SOI (silicon-on-insulator) technology. It supports a wide range of wireless protocols while delivering up to 1.3 GHz of performance.

The QorIQ P2020 communications processor is designed to deliver multicore processing at single-core pricing, Freescale said. It features two 3500-based cores ranging from 800 MHz to 1.2 GHz.

The MPC8569E PowerQUICC III processor has an integrated design in a single chip and is said to deliver up to 1.3 GHz performance within a sub-10 W power envelope.

"In the current economic environment, it is encouraging to see tremendous worldwide demand for enabling technology that facilitates deployment of broadband infrastructure equipment for advanced 3G and 4G networks," said Lisa Su, senior VP and general manager of Freescale's networking and multimedia group, in a statement. "By accelerating delivery of our high-performance 45-nm products to customers, Freescale is playing a key role in delivering the performance and cost reductions required to bring next-generation networks to life."

[*Source: Electronic News*]

FEATURE

Executive Outlook: Survival and Opportunities in 2009

Paul Lindner
Executive Technology Director, EV Group

In 2009, the semiconductor and MEMS markets will continue to see the effects of 2008's macroeconomic fallout. This will be specifically true in segments on the front lines — automotive- and consumer-product driven — where the impact will be significant. Even so, we expect that companies in these markets will remain committed to innovation. In their quest to bring novel technologies to market, we suspect that manufacturers will continue to invest in new production technologies, including 3-D/TSVs and nanoimprint lithography, to overcome yield and performance challenges as they scale down toward 32 and 22 nm geometries.

In striving to meet the stringent form factor and performance requirements at these advanced nodes, we expect to see manufacturers first apply 3-D/TSV and nanoimprint lithography technologies to low-hanging fruit, specifically for the manufacture of devices designed to be failure intolerant. This includes chipsets with increased functional density and 3-D memory. We anticipate that the latter will be brought to market in 2009. These new technologies will also impact the manufacture of backside-illuminated CMOS image sensors, where it is critical to meet cost, performance and quality requirements, along with logic devices and microprocessors.

Because IDMs and foundries will remain the signature early adopters of new technologies in 2009, we expect to see these manufacturers establishing and proving the processes for 3-D IC integration, TSVs and nanoimprint lithography in their fab lines. These application successes, we suspect, will in turn accelerate industry-wide adoption of 3-D/TSV and nanoimprint lithography equipment through the year and into 2010.

FEATURE

Plumbing 101: Current Leakage And What to Do About It

Brian Fuller

"Leakage is a huge problem for the industry, and it's worse as we scale," says Ted Speers.

Rising demand for mobile products and the march of Moore's Law have created conditions for a perfect storm that threatens to swamp electronics designs and the market growth those designs target.

The catalyst for that storm is leakage, which worsens the smaller devices become. Even in an "off" state, systems can leak like poorly insulated houses. But as the nation thinks about energy usage on a large—making homes and buildings more energy efficient—the electronics industry also grapples with the best energy-efficient design tools and techniques.

Leakage wasn't a huge consideration until recent years, with electronics designs not only enabling mobile phone market growth but also bringing mobility and smaller form factors into a host other markets as well, including smart meters, medical devices, and the like. Most of those need to be miserly with power because they're battery operated. And if they're not, a greater sensitivity to the impact electronics has on the overall power grid and our national energy consumption is an important consideration.

"Leakage is a huge problem for the industry, and it's worse as we scale," says Ted Speers, head of product architecture and planning and fellow at FPGA vendor Actel Corp.

And designer concern is scaling just as quickly. "The (concern) has gone from a 10% problem to a 60% problem in the past four years," said Steve Carlson a vice president in Cadence's R&D organization. He is referring to customer-feedback studies that rate the importance of various design issues, such as power, leakage, performance and timing.

There are different types of leakage and scores of methods, tools and technologies to minimize it.

Dr. Leaky, I Presume

Leakage happens in capacitors as a small amount of current inevitably drains away in an off mode to transistors or diodes. Imperfections in the dielectric material insulating capacitors—which can occur in manufacturing—can contribute to the problem, discharging the capacitor. While the leakage is generally in the micro-ampere range, over time it will drain a portable device's battery, rendering it useless until it's recharged.

Leakage increases exponentially the thinner the insulator becomes. Electrons can also leak across semiconductor junctions between heavily doped P-type and N-type semiconductors—the tunneling effect. And they also can leak between the source and drain, when the device should be off—the sub-threshold leakage problem.

To lower threshold voltages, designers squeeze oxides thinner and thinner, but the thinner the oxide, the higher the sub-threshold leakage. Often leakage can be more than half of total power consumption. Some experts have estimated that each process generation increases leakage current by a factor of 10.

Given these physical challenges, it's a wonder advanced portable devices have any battery life at all. But they do. Battles are waged every day from the transistor level up through system-optimization, each contributing its part to the war on leakage.

[*Source: Low-Power Design Community*]

ANNOUNCEMENT

International Summer School on Advanced Microelectronics. MIGAS 2009

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It is also a unique opportunity for senior and junior researchers to update their knwoledge in a very specific and emerging field. MIGAS brings together scientists from all over the world and from research institutes, universities, R&D small, medium and large companies.

This year 2009 MIGAS Summer School will be held from 21st - 27th June in Autrans-Grenoble, a reknown resort, dedicated to alpine and cross-country skiing in winter, and to tourism in summer, located in the Regional Natural Park of the Vercors mountains, 30 km away from Grenoble.

MIGAS 2009 topic is "Advanced SOI concepts: from materials to devices and applications".

The lectures will be given by world-class experts, including: J-P. Colinge (Ireland), T. Hiramoto (Tokyo), A. Zaslavsky (USA), R. Schrimpf (USA), C. Fenouillet-Béranger (STMicroelectronics), A. Asenov (Glasgow),O. Faynot, T. Ernst and B. de Salvo (LETI), F. Gamiz (Granada), S. Cristoloveanu (Grenoble), etc.

Details and information for registration will be soon available on the MIGAS website: http://www.migas.inpg.fr/

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

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If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

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June 20th - 26th, 2009

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Clare College, Cambridge, United Kingdom.
June 29th - July 1st, 2009

- European School On Nanosciences & Nanotechnologies
Grenoble, France.
August 23rd - September 12th, 2009

- 39th European Solid State Device Research Conference and 35th European Solid State Circuits Conference
Athens, Greece.
September 15th - 19th, 2009

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XII

MAY, 2009

IN THIS NUMBER:

EDITORIAL

EUROSOI+: The balance of the first year.

Francisco Gámiz
Professor
Univ. Granada (Spain)
Coordinator of the EUROSOI+ Network

The main and last objective of EUROSOI Network is to establish Europe as the international scientific leader in Silicon on Insulator (SOI) Technology, Devices, Circuits and Systems. In this sense, the EUROSOI+ co-ordination efforts during this first year have been focused on the starting of those activities which contribute to improving the role of the European Semiconductor Industry with regard to SOI and to the knowledge that will enable Europe to compete internationally. Although EUROSOI achievements during FP6 have been many and very important for the European SOI technology, and the situation of SOI technology in Europe has greatly improved during the last three years, there are plenty of challenges at the near future. Even if we now are in the right direction, Europe is still far away from the pursued international leadership. After the elaboration of the State-of-the-Art report and EUROSOI Roadmap, we have identified the main actors, the strong points and weaknesses of Silicon-On-Insulator technology in Europe. All this information is collected in the EUROSOI Roadmap, where the challenges which will have to be faced in the future are also identified. Our first stage was a passive one (collecting and structuring the information). This second stage is being much more active; we are not only looking at around us, collecting and restructuring the available information, but we have passed to the action in a more active role, developing the tasks, fostering creation of consortiums and leading the projects and proposals which give Europe and the European Semiconductor Industry the international leadership which they deserve as pioneers and big developers of SOI technology.

The best way to reach this goal is to try to spread the SOI technology all over Europe, making it accessible to any European semiconductor actor:

"*We want that SOI technology is reachable to any European research group or Fabless Semiconductor company; we want that any circuit design has the chance to become a SOI circuit using European technology.*"

To do so, we have to work in three directions:

- Training of researchers and engineers in the particularities of this technology, i.e., in the design of circuits taking advantage of SOI technology.
- Spreading and promotion of the benefits and advantages of SOI technology.
- Development of a platform which offers SOI technology for the actual fabrication of SOI circuits

It is widely accepted by the International Semiconductor Community that most of the electronic circuits (in the whole application spectra) will have a better performance, and therefore, they will be more competitive, if they are built using SOI technology. However, nowadays it is not easy to have access to this technology, even when we count in Europe with some of the most advanced SOI technologies all over the World.

Up to now, a lot of research activities have been pursued in Europe around SOI at different levels: substrate, device, and circuit.

(*Continues on page 2*)

ANNOUNCEMENT

Tutorial Section on the EUROSOI Website Complete

Following the efforts that the EUROSOI team is making to improve its work and with the dedication that has been shown thus far, the new tutorial section is now complete containing the different tutorials held since the first EUROSOI Workshop in Granada in 2005.

The different tutorials are organized according to their dates and places and a search engine by years has been also developed. For further details take a look at:

http://www.eurosoi.org/tutorials.asp

EUROSOI+ BALANCE

EUROSOI+ activities during the first year

"Although EUROSOI achievements during FP6 have been many and very important […] , there are plenty of challenges at the near future ." said Francisco Gámiz.

"We want that SOI technology is reachable to any European research group or Fabless Semiconductor company; we want that any circuit design has the chance to become a SOI circuit using European technology."

The following two points summarize EUROSOI+ activities during this period:

I. **Training and promotional activities.**

a) **Website database**
http://www.eurosoi.org

i. **EUROSOI Virtual Journal**
http://www.eurosoi.org/articles.asp
ii. **EUROSOI Landmark publications**
http://www.eurosoi.orglandmark_publications.asp
iii. **EUROSOI Newsletters**
http://www.eurosoi.org/newsletters.asp
iv. **EUROSOI News&Announcements**
http://www.eurosoi.org/news.asp
v. **EUROSOI Training material database**
http://www.eurosoi.org/tutorials.asp

b) **Organization of Training events and Tutorials**

i) Multigate SOI MOSFETs (*January 23rd,2008, Cork, Ireland, 2008*)
ii) SOI from modelling to design (*January 19th, 2009, Goteborg, Sweden*)

c) **Organization of Workshops.**

i) **Fourth Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits**
(Tyndall National Institute, Cork, Ireland, Jan 23-25th, 2008):
http://www.tyndall.ie/eurosoi2008/
(56 communications, 80 attendants)

ii) **Fifth Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits**
(Chalmers University of Technology, Goteborg, Sweden, Jan 19-21st, 2009):
http://chalmers2009.eurosoi.org
(60 communications, 90 attendants)

(Continues on page 3)

EUROSOI+: The balance of the first year. *(cont.)*

Since few years, advanced SOI technologies have been developed in research labs in order to address the downscaling required for 32nm nodes and below. Today such researches are mainly dedicated to technology development. Among the various ones, we can mention the LETI Fully Depleted SOI technology (developed with high-k and metal gate) that currently has enough maturity to be evaluated at circuit level. So, it becomes obvious that a research-dedicated platform is necessary in order to address the circuit design aspects, focussing on the advantages of such technology for Low Power applications. Access to such platform is a long-time wish of European researchers. Hence, the main goal of EUROSOI+ is to coordinate the formation of such research-dedicated platform which will provide, through the integration in EUROPRACTICE, prototyping and Multi-Project-Wafers (MPW) in SOI open to all European companies using LETI SOI process in two-three years. We are co-ordinating all the activities which will make this platform a reality in 2010.

EUROSOI+ BALANCE

EUROSOI+ activities during the first year (*cont.*)

d) Discussion Panels. The opinion of SOI experts.

i) "Key Issues in SOI: Solutions and Ideas", chaired by Prof. Sorin Cristoloveanu, January 24th, 2008, Cork, Ireland

Participants:
Dr. Damien Bretegnier, SOITEC
Prof. Denis Flandre, UCL
Dr. Segei Okonin, Innovative Silicon
Dr.Olivier Faynot, CEA-LETI
Prof. Jean-Pierre Colinge, Tyndall

ii) "What is the killing advantage of multiple-gate SOI MOSFETs: electrostatics and scalability, transport or functionality", chaired by Prof. Sorin Cristoloveanu, January, 20th, 2009 Goteborg, Sweden

Participants:
Prof. Cor Claeys, IMEC
Prof. Jerry Fossum, University of Florida
Prof. Jean-Pierre Colinge, Tyndall
Dr.Olivier Faynot, CEA-LETI
Dr.Stephane Monfray, STMicroelectronics, Crolle
Prof.Francis Balestra, IMEP, SINANO Institute

e) Student and travel grants.

- 13 student grants to attend EUROSOI workshops have been given to PhD students who works towards their PhD in European Universities in the field of SOI technology.
- 20 travel grants have been also distributed among EUROSOI network partners to partially cover their registration and travel expenses to attend EUROSOI workshops.
- Financial support for major conferences and promotional travels.

f) Scientific Exchanges

- 7 Exchange visits of EUROSOI members to other European Research Centers have been funded by EUROSOI+ during this first year.

g) Elaboration & Upgrading of Technical Focused Reports (TFRs).

i) EUROSOI State of the art report: http://www.eurosoi.org/public/EUROSOI_State_of_the_art.pdf

ii) EUROSOI roadmap. http://www.eurosoi./public/EUROSOI_Roadmap.pdf

iii) EUROSOI who is who. http://www.eurosoi.org/public/EUROSOI_who_is_who.pdf

iv) Benchmark of UTB vs. FinFET vs. DG SOI transistors. Which SOI device is favourite and for which application? http://www.eurosoi.org/public/D4.15.focused.report.utb_finfet_def.pdf

II. Development of EUROSOI fabrication & prototyping platform for the design of low-power SOI circuits.

a) Coordination of information exchange on LETI FDSOI technology. FDSOI wafers with functional devices have been provided to UCL, and IMEP. Also, electrical measurements have been provided to UGR. On November 17th-18th, Dr.Olivier Faynot from LETI organized in Grenoble a tutorial (free of charge for the EUROSOI members) focused on the training of European scientists on Fully Depleted SOI technology. Well recognized technologists, as well as international experts on devices and circuit design trained the attendees on SOI specific aspects, including: (1) Devices physics; (2) Technology description; (3) Modelling and circuit design; (4) Variability issues; (5) FDSOI platform development status. See the link: http://www.eurosoi.org/tutorialinfo.asp?id=7

(Continues on page 4)

EUROSOI+ BALANCE

EUROSOI+ activities during the first year

(cont.)

"The main goal of EUROSOI+ is to coordinate the formation of a research-dedicated platform" says Francisco Gámiz.

b) Coordination of activities for the documentation, promotion and spreading of Research-dedicated Design Kit (RDK). The development of the research design kit is progressing in phase with what has been planned in the European project called DECISIF. This design kit contains a digital part that includes device model, Design Rules Control file and Layout Versus Schematic file. These files are essential to model and control the layout generated by the designers. This part is completed at 85%. The design kit contains also an analog part that includes Matching parameters, RF parasitics and related model (competed at 50%). The design kit finally contains an automated digital Design flow that includes Standard cell library and SRAM memory cuts. This last part is completed at 30%. With such level of achievement, the design kit can already be used to design some elementary circuits. It is scheduled to complete this design kit by mid-2009.

c) Promotion of the FDSOI technology. Promotion of the FDSOI technology has been made by LETI during this period to the following companies:

- Presentation of the technology and results are regularly (every 3 months) made to SOITEC.
- Technology and electrical results have been also presented to ST Microelectronics in order to highlight the interest of such technology for Low Power applications.
- Promotion of FDSOI technology has also been done to AMD and ARM through a presentation at the SOI consortium meeting in November 2008. More detailed meetings will be planed for each company in 2009

d) Coordination of activities for the evaluation of the possible integration by the end of 2009 in the existing EUROPRACTICE structure.

We are now considered as one of the EUROPRACTICE projects (http://www.europractice.org/).

We participated in the EUROPRACTICE Workshop held in Leuven on September 4th, 2008.

ANNOUNCEMENT

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- 39th European Solid State Device Research Conference and 35th European Solid State Circuits Conference
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September 15th - 19th, 2009

- 2009 IEEE International SOI Conference
Foster City, California.
October 5th - 8th, 2009

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XIII

JUNE, 2009

IN THIS NUMBER:

EDITORIAL

Denis Flandre
Université Catholique de Louvain, Belgium

FD SOI Revival and Promises

Following the adoption of partially-depleted (PD) SOI by the industry about ten years ago, the ever postponement of fully-depleted (FD) wider introduction and the focus of R&D on FinFETs and multiple-gate transistors, it was generally believed that the roadmap would jump onto the latter for scaling to ultimate CMOS. Intensive research on FD SOI was then substantially dropped, as can be clearly noticed from a lack of development of new FD device compact models.

The mood has changed since a bit more than a year. The emergence of the variability issue as the main limiting factor for circuit performance beyond the 65nm node has triggered a revamping of FD SOI in the form of undoped, ultra-thin body (UTB), and possibly ultra-thin buried oxide. With such features, FD SOI sub-45nm processes have been presented in major conferences and journals, demonstrating unrivaled "(un)variability" figures of merit and electrostatic control for gate lengths as short as 15nm. As discussed at the last EUROSOI conference in Goteborg, European groups with CEA-LETI (using SOI substrates with about 10nm thick body and down to 11nm BOX) and STM (using their SON process) are clearly leading the pack, along with IBM in the USA.

Our group in UCL has further shown at the 2008 IEEE Int. SOI Conference, that taking such excellent device properties into account, undoped UTB FD SOI 45nm-CMOS holds the promise at circuit level, as compared to Bulk, for delay improvement by up to a factor 8 or power reduction at isospeed by more than 3, at supply voltages below 0.5V. This is way beyond the previous expectations of a twofold benefit.

But there is no free lunch. The electrical behaviours of undoped UTB FD SOI MOSFETs, especially with ultra-thin BOX, reveal several surprises. One recently unconvered dominant effect on device characteristics is that the channel can't any longer be assumed to lie at the front gate oxide interface. Depending on biases, it can move all through the film depth, a bit like with volume inversion in double gate transistors, with impact on mobility values, subthreshold swing, short channel effects, etc. This is a major issue for FD compact models which all presently appear to be using the charge-sheet approximation. Precise circuit simulations of UTB devices thus require new compact modelling concepts which have lately been quite disregarded, as mentionned above.

To conclude, I think that the EUROSOI community has the potential to yield a significant contribution for solving the modelling issue and developing high-performance FD UTB circuits, thanks to the CEA-LETI technological platform promoted within our project. Strong European leadership on FD UTB SOI is our horizon...

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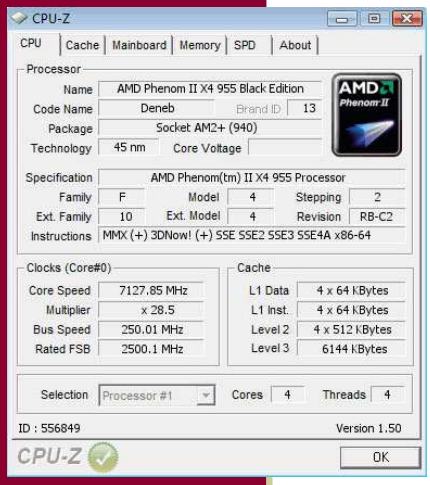
NEWS

AMD smashes the 7.1 GHz barrier with Phenom II 955 CPU!



AMD and Phenom II - everybody knows the name of current overclocking darling. Manufacturing wizards at GlobalFoundries tweaked up the 45nm SOI [Silicon-On-Insulator] with Silicon-Germanium material and enabled a flexible transistor design.

Combine that manufacturing skill with architectural improvements and the results are in: World Record for a multi-core CPU goes to Phenom II 955, originally clocked at 3.2 GHz. The team of overclockers in LimitTeam, consisted out of Sigh, Qooitry and Ultra40 overclocked the Phenom II 955 to 7,127.85 MHz, or 7.13 GHz, using a HyperTransport base clock of 250 MHz.

The team used ASUS M4A79T Deluxe motherboard, ATI Radeon 4800 series graphics card and 2x2GB of DDR3-833 memory by Apacer Technology. You can see the screenshot of CPU-Z validated score on the left, and the Phenom II 955@7.13 GHz project ID is 556849.

Both the graphics and memory were seriously underclocked to achieve as high clock as possible, with processor eating all the juice that motherboard was able to give.

This CPU belongs to Deneb's C2 revision, equal to the one we have in our Labs. So far, our Phenom II 955 achieved stable 4.1 GHz clock on air... it would be really, really interesting to see could this 7.1 GHz overclock pass the Linpack test... that score would be sure to give a lot of wet dreams to HPC administrators and engineers.

In any case, kudos to the LimitTeam and AMD for making a seriously overclockable processor.

[*Source: Bright Side of News*]

NEWS

New Six-Core AMD Opteron™ Processor Delivers Up to Thirty-Four Percent More Performance-per-Watt in Exact Same Platform

"The new Six-Core AMD Opteron processor meets the increasing need for a combination of low total cost of ownership, superior performance-per-watt and scalability", said Patrick Patla

AMD announced availability of the world's first six-core server processor with Direct Connect Architecture for two-, four- and eight-socket servers. Six-Core AMD Opteron™ processors (code-named "Istanbul") extend AMD's commitment to offering server customers superior value at every price point with unmatched platform flexibility.

Across a single platform, AMD can address the need for more cores and greater scalability with the new Six-Core AMD Opteron processor and offer a cost- and power-efficient solution with Quad-Core AMD Opteron processors. Systems based on Six-Core AMD Opteron processors are expected to be available beginning this month from leading OEMs including Cray, Dell, HP, IBM and Sun Microsystems, along with support from motherboard and infrastructure partners. HE, SE and EE versions of the Six-Core AMD Opteron processor are planned for the second half of 2009.

• Six-Core AMD Opteron processors leverage existing platform infrastructure and a low-cost, power-efficient DDR-2 memory architecture which can help lower system acquisition costs;

• HPC, virtualization and database workloads can benefit from increased 4P STREAM memory bandwidth of up to 60 percent enabled by HyperTransport™ technology HT Assist, which helps reduce processor to processor latency and traffic;

• AMD Virtualization™ (AMD-V™) technology and the AMD-P suite of power management features are available across all performance and power bands, ensuring no-compromise choice;

• The new Six-Core AMD Opteron processor has up to 34 percent more performance-per-watt over the previous generation quad-core processors in the exact same platform.

"The new Six-Core AMD Opteron processor meets the increasing need for a combination of low total cost of ownership, superior performance-per-watt and scalability. Simply put, Six-Core AMD Opteron processors deliver top-line performance that's bottom-line efficient.", said Patrick Patla, vice president and general manager, Server and Workstation Business, AMD

[*Source: AMD*]

NEWS

AMD Introduces Next Generation AMD Athlon™ II Processor, Adds Dual Core to Record-Setting AMD Phenom™

Bringing its acclaimed 45nm technology to new high-volume processor designs, AMD announced two new dual-core desktop processors. Building on 10 years of AMD Athlon™ processor innovation, the new 45nm AMD Athlon™ II X2 250 processor gives mainstream consumers exceptional performance, efficiency and value. For enthusiasts and overclockers, AMD also announces the AMD Phenom™ II X2 550 Black Edition processor, the first ever dual-core AMD Phenom II CPU. With this latest addition to the AMD Phenom II processor family, users can now experience the power of AMD platform technology, codenamed "Dragon," with dual-, triple- and quad-core configurations.

AMD Athlon II X2 Processor Details

• The AMD Athlon II X2 250 performs exceptionally well when combined with AMD chipsets and integrated graphics solutions to create an all-AMD platform. Platforms featuring all-AMD technology can deliver up to twice the graphics performance of those with Intel integrated graphics.

• Windows® 7 is optimized for multi-core processors like AMD Athlon™ II processors to give consumers an amazingly fast, simple and engaging PC experience.** For example, Windows 7 is tuned to make the most of these new processors' power management features, such as AMD PowerNow!™ 3.0 technology. AMD power management technologies, in combination with Windows 7, can help OEMs and partners to build exceptionally green, cool and quiet PCs.

• Based on AMD's acclaimed 45nm process technology, the AMD Athlon II dual-core processor has a TDP of 65W and can slash power consumption by up to 50 percent when doing basic tasks, up to 40 percent when running heavy workloads and up to 50 percent when at idle.

AMD Phenom II X2 550 Black Edition Details

• AMD Black Edition processors, like the AMD Phenom™ II X2 550, help users to take control and unleash the maximum potential of Dragon platform technology's unprecedented performance tuning capabilities.* The same massive headroom that set world records in recent months is at users' finger tips, offering impressive performance at a price the competition can't beat.

• Users can also maximize their overclocking experience by utilizing the new features and capabilities of AMD OverDrive™ 3.0, designed to enable quick and effective tuning of their PC experience for optimal performance.

• With dual-, triple- or quad-core processors, AMD provides platform level solutions at multiple price points, each of which exceeds expectations for virtually any user.

[*Source: AMD*]

FEATURE

GlobalFoundries gears up

Scott Wasson

AMD's decision to spin off its manufacturing business into a separate entity has created a fairly unique event in semiconductor manufacturing: an ostensible newcomer has opened some of the world's most advanced chip fabrication capabilities to paying customers of all stripes. Last week, we traveled to the new offices of GlobalFoundries in Saratoga County, New York to meet with the firm's executives and to understand their plans for the newly minted chip foundry.

Although much is new about GlobalFoundries, including the company's name and mission, key parts will be familiar to industry observers, because they include many assets and personnel formerly from AMD. Those assets include two chip fabrication plants in Dresden, Germany. Now called Fab 1 module 1, the former Fab 36 produces AMD's processors, including Phenom II and Opteron CPUs, using an advanced 45nm silicon-on-insulator process on 300 mm wafers. The former Fab 30 is being retooled for 300 mm wafers, as well, and has been renamed Fab 1 module 2 in GlobalFoundries' lexicon.

The transaction that created GlobalFoundries gave majority ownership in the firm to the Advanced Technology Investment Company, which is wholly owned by the government of Abu Dhabi, in exchange for a multi-billion-dollar investment. AMD retained 34% ownership in GlobalFoundries and voting rights equal to ATIC's. AMD will be GlobalFoundries' single most important customer for the foreseeable future, as well.

The big change introduced by the spin-off is GlobalFoundries' intention to enter the foundry business and, as we've noted, offer its chip fabrication capabilities to a range of clients. To that end, GlobalFoundries has been assembling a team of veteran executives, both from within the former ranks of AMD and from outside, with experience in key phases of the semiconductor business. Hearing them talk about GlobalFoundries as "a big startup" may fall strangely on the ear of anyone familiar with AMD, but there's more than a kernel of truth in the sentiment.

Grose point blank

GlobalFoundries CEO Doug Grose makes the case for a new entrant in this business by arguing that chip design is most fundamental to innovation. The foundry's role, as a partner, is to provide leading-edge manufacturing capabilities to its customers, so they can remain focused on design. Staying at the forefront of chipmaking technology is no trivial undertaking, he points out, with R&D budgets and fab construction costs ballooning in recent years. The barriers to reaching new process nodes, or "red brick walls," are getting higher and thicker. By consolidating the knowledge gained from its technology alliance with IBM and other partners, and by serving a diverse portfolio of customers, GlobalFoundries aims to provide a stable source of manufacturing capacity while remaining at the forefront of process advances.

ANNOUNCEMENT

EUROSOI Exchange Grants

There will be another call for proposals on November 2009 and May 2010.

EUROSOI+ launches the third Call for Proposals to fund exchanges in terms of travelling and research visits for scientists (students and senior scientists) in order to enhance collaborations and information exchange.

How to apply for this grants?

Send a proposal to agodoy@ugr.es before June 30th 2009, including a short CV, an invitation letter from the institution to be visited and a comprehensive description of the visit purpose, destination, duration, budget, etc)

The following requirements must be fulfilled:

- The field should fall within research domains defined by EUROSOI+
- At least one EUROSOI member should be involved in the project research
- Priority will be given to industrial partners to allow a better integration of the European industry in the Network
- Less than 4 weeks
- Gender aspects will be considered (promote the participation of women)
- Not salary costs or expenses generated by research activities.
- The visit should be carried out before the end of December 2009 (remember that there will be another call for proposals on November 2009 and May 2010)

After the visit (less than one month), the participant should provide a report describing the work developed during the visit. Please, take into account that:

- The daily allowance depends on the destination and including lodging and travel expenses with a maximum of 1400€ per week. More details can be provided in terms of specific information.
- Each visit must be shorter than 4 weeks.
- The reimburstment is always after the visit.

The EUROSOI Management Board in its next meeting will decide which proposals are funded.

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International Summer School on Advanced Microelectronics. MIGAS 2009

MIGAS Summer School is designed to foster and promote expertise in new, advanced topics of microelectronics. The aim of MIGAS is to offer every year a forum of detailed presentations on emerging topics of microelectronics.

It is also a unique opportunity for senior and junior researchers to update their knwoledge in a very specific and emerging field. MIGAS brings together scientists from all over the world and from research institutes, universities, R&D small, medium and large companies.

This year 2009 MIGAS Summer School will be held from 21st - 27th June in Autrans-Grenoble, a reknown resort, dedicated to alpine and cross-country skiing in winter, and to tourism in summer, located in the Regional Natural Park of the Vercors mountains, 30 km away from Grenoble.

MIGAS 2009 topic is "Advanced SOI concepts: from materials to devices

and applications".

The lectures will be given by world-class experts, including: J-P. Colinge (Ireland), T. Hiramoto (Tokyo), A. Zaslavsky (USA), R. Schrimpf (USA), C. Fenouillet-Béranger (STMicroelectronics), A. Asenov (Glasgow),O. Faynot, T. Ernst and B. de Salvo (LETI), F. Gamiz (Granada), S. Cristoloveanu (Grenoble), etc.

Details and information for registration available on the MIGAS website: http://www.migas.inpg.fr/

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

CALENDAR

- MIGAS International Summer School
Autrans-Grenoble, France.
June 20th - 26th, 2009

- INFOS 2009
Clare College, Cambridge, United Kingdom.
June 29th - July 1st, 2009

- European School On Nanosciences & Nanotechnologies
Grenoble, France.
August 23rd - September 12th, 2009

- 39th European Solid State Device Research Conference and 35th European Solid State Circuits Conference
Athens, Greece.
September 15th - 19th, 2009

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XIV

JULY, 2009

IN THIS NUMBER:

HIGHLIGHT NEWS

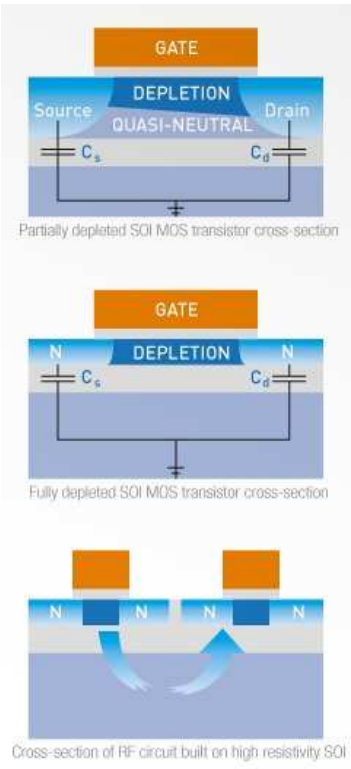
Soitec's 300mm ultra-thin SOI prepped for 22nm applications

The Soitec Group has completed development and qualification of its 300mm ultra-thin SOI (UTSOI) wafer platform for use in supporting fully-depleted device applications on the industry's CMOS roadmaps for 22nm and beyond. The system is now ready to support mainstream ramp-up of fully depleted applications at the 22nm node, delivering a film thickness uniformity control of ± 5Å.

The UTSOI platform, which was introduced last year, has been undergoing process optimizations and customer qualifications that now enable customers to tailor the final SOI substrate to specific parameters. The company can now manufacture SOI with extremely thin top-layer silicon (20nm) to a thickness uniformity tolerance of ± 5Å in high volume with high yields.

"On fully depleted SOI, we've demonstrated 25nm high-k metal-gate devices with matching characteristics far superior to those obtained on bulk silicon," reported Dr. Olivier Faynot, Director of Advanced SOI technologies Development at CEA-Leti. "As it eliminates the need to dope the channel region, FD SOI solves threshold voltage (Vt) variability challenges at current and future nodes, while maintaining excellent Ion and Ioff characteristics and drastically reducing gate leakage current. With this uniform ultra-thin film SOI substrate, Soitec is delivering a solution for substantially improving Vt control of the CMOS device."

[Source: FabTech]



EVENTS

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MIGAS 2009 topic was "Advanced SOI concepts: from materials to devices and applications" and lectures were given by world-class experts

(continues on page 2)

This year, for its 12th session, MIGAS'09 was focused on SOI concepts: from materials to devices and applications.

J-P. Colinge (Ireland), T. Hiramoto (Tokyo), A. Zaslavsky (USA), R. Schrimpf (USA), C. Fenouillet-Béranger (STMicroelectronics), A. Asenov(Glasgow),O. Faynot, T. Ernst and B. de Salvo (LETI), F. Gamiz (Granada), S. Cristoloveanu (Grenoble), etc.

MIGAS
International Summer School on Advanced Microelectronics

MIGAS '09 - 12th session

SOI Concepts: From materials to devices and applications

20 - 26 June 2009, Autrans-Grenoble, France

www.migas.inpg.fr

IMEP-LAHC MINATEC POLE D'INNOVATION Grenoble INP

NEWS

Luxtera Announces Production Status of World's First Commercial Silicon CMOS Photonics Fabrication Process

These CMOS Photonic transceivers offer better performance, increased reliability, and reduced power consumption.

LUXTERA

Luxtera, the worldwide leader in Silicon CMOS Photonics, announced its collaboration with Freescale Semiconductor as its foundry source to achieve production of the world's first commercial Silicon CMOS Photonics semiconductor manufacturing process. For a number of years, the companies collaborated on enhancing Freescale's SOI CMOS semiconductor fabrication process, at its Austin, Texas manufacturing facility, to add photonic circuit capabilities to an existing 130nm electronics manufacturing process. This new photonically enabled CMOS fabrication process enables development and manufacturing of low cost Electro-Photonic Integrated Circuits (EPIC) bringing CMOS Photonics to mainstream markets ahead of the competition. Silicon CMOS Photonics is widely recognized as the key enabler of the next-generation of data-networking, computer, multi-core processor, and consumer electronics products.

Silicon CMOS Photonics technology enables design and manufacturing of optics and electronics on a single CMOS die. This process combines standard transistors for digital and analogue electronic circuitry with passive nano-photonic optical structures, as well as monolithic integration of active photonic device elements and enables direct fiber-to-the-chip attachments. The new fabrication process allows the production of integrated single chip transceivers for a multitude of applications. These CMOS Photonic transceivers offer better performance, increased reliability, and reduced power consumption of opto-electronic circuits at a fraction of the cost of traditional optical assemblies.

[*Source: Business Wire*]

NEWS

Globalfoundries Demos 28nm, 32nm Wafers.

Globalfoundries, a joint venture between Advanced Micro Devices and Advanced Technology Investment Company, showed off its first wafers with logic produced using 32nm and 28nm process technologies. While existence of 32nm silicon-on-insulator wafers at Globalfoundries is hardly a surprise, bulk 32nm and 28nm wafers seems rather promising.

Globalfoundries is busy these days finding customers for itself as currently it has only one client: the parent company Advanced Micro Devices, which produces all of its central processing units (CPUs) at Globalfoundries and will also make its graphics processing units (GPUs) as well as core-logic sets using 32nm and 28nm bulk process technologies at Globalfoundries. The latter still needs to find more interested parties ahead of beginning to construct its third fab in New York, USA. No surprise, the firm brought its latest achievements to show at Computex Taipei 2009, the biggest technology trade-show in Asia.

At Computex, Globalfoundries demonstrated a wafer with six-core AMD Opteron "Istanbul" processors made using 45nm SOI process technology, a wafer with test chips produced at 32nm SOI node, a wafer with test chips processed at 32nm bulk node as well as a wafer with SRAM manufactured utilizing 28nm bulk fabrication process.

Since AMD's chief executive officer promised to ramp up processors using 32nm SOI process tech in the second half of 2010, it is hardly a revelation that Globalfoundries has test chips produced using the technology. What is more surprising is that the company demonstrated its 32nm and 28nm bulk wafers, which implies that that it has been working on 32nm/28nm fabrication processes for quite a while. Earlier this year the company said it would be ready to accept orders for 32nm bulk production in late 2009. Early risk production using 28nm fabrication process is anticipated in the second half of 2010.

While Taiwan Semiconductor Manufacturing Company has yield issues with its 40nm process technology, demonstration of 45nm, 32nm and 28nm capabilities seems to be just what the doctor ordered for Globalfoundries to attract attention of the industry

[*Source: X-bit labs*]

NEWS

Infineon and LS Industrial Systems Form Joint Venture to Forge Ahead in Molded Power Module Business for White Goods; Joint Venture to Accelerate Access to Power Module Market in Korea and Asia.

The Korean company LS Industrial Systems and Infineon Technologies AG announced the establishment of the joint venture LS Power Semitech Co., Ltd. which will focus on the development, production and marketing of molded power modules for white good applications. The establishment of the joint venture paves the way for Infineon and LS Industrial Systems to more rapidly access the promising market for energy efficient household appliances, such as washing machines, refrigerators and air conditioners, and also for other low-power consumer and standard industrial applications. The use of variable-speed motors to reduce the energy consumed by household appliances is growing in response to regulatory requirements and consumer demand. Concurrently, smart design of drive control electronics to make best use of these motors presents manufacturers with further opportunities for efficiency and savings.

LS Industrial Systems holds 54 percent and Infineon 46 percent of the joint venture with headquarters at LS Industrial Systems' site in the city of Cheonan which is located around 160 kilometers to the south of Seoul. Infineon will provide the joint venture with licenses to IP as well as technology and process know-how on its power module family CIPOS™ (Control Integrated Power System), and will transfer existing CIPOS backend manufacturing equipment from Regensburg, Germany. Both companies will closely cooperate in terms of marketing, international sales, and new product developments. LS Power Semitech expects to begin mass production for CIPOS modules by January 2010 in its Cheonan manufacturing site.

According to the current market report of the research firm IMS Research, Infineon holds the number one market position in semiconductor discretes and modules for power electronics having a 9.7 percent market share within the overall global market of US Dollar $13.6 billion in 2007.

CIPOS power modules increase energy efficiency and reliability of home appliance motors

The CIPOS modules incorporate a three-phase inverter power stage with a SOI (Silicon-On-Insulator) gate driver, boot strap diodes and capacitors, and auxiliary circuitry in a compact, high-performance, fully isolated package. Based on a combination of Infineon's leading-edge TRENCHSTOP™ IGBT (Insulated Gate Bipolar Transistor) and emitter controlled diode technology, they eliminate as many as 23 discrete components compared to a design based on discrete components. The CIPOS modules also offer the industry's lowest junction-to-case resistance, which increases output current by up to 20 percent compared to other available modules.

The CIPOS family today comprises various members including modules for three-phase IGBT inverters for the voltage classes 5V or 3.3V with and without fault detection, for three-phase IGBT inverters with closed common emitter and for two-phase IGBT inverters for switched reluctance drives. The CIPOS modules are available in a RoHS-compliant single-in-line package that is best-suited for washing machine applications.

[*Source: Infineon*]

NEWS

SOI Industry Consortium reinforces its academic and research support; three more prestigious universities join

"Together, we can facilitate cooperation with industry and other research organizations, helping to accelerate the use of SOI in both emerging and established application fields" says Horacio Méndez.

The SOI Industry Consortium, an international group aimed at accelerating broad adoption of silicon-on-insulator (SOI) materials technology across semiconductor markets, announced that it is reinforcing its academic and research support with the additions of three prestigious universities at the forefront of SOI applied research. Stanford University, University of California, Berkeley and Ritsumeikan University, Kyoto, Japan have all joined the consortium as academic members.

"We are very pleased to welcome Stanford, U.C. Berkeley and Ritsumeikan University. With these additions, we are expanding our excellent ecosystem of prestigious academic and research support," says Horacio Mendez, Executive Director of the SOI Industry Consortium. "Our members in academia are key contributors in both basic and applied SOI research. Together, we can facilitate cooperation with industry and other research organizations, helping to accelerate the use of SOI in both emerging and established application fields. Conversely, academia is our gateway to the future, providing our industry with researchers and engineers who have a strong grounding in the use and advantages of SOI."

The SOI Industry Consortium will continue promoting cooperation between commercial members and academia and research institutes. Representing leaders spanning the entire electronics industry infrastructure, the SOI Industry Consortium's membership now counts seven academic members and research institutes worldwide. The others include Tyndall Institute, "Université Catholique de Louvain" (UCL), as well as IMEC, and Leti. The group's expertise covers key areas such as ultra-low power applications, MEMS, advanced CMOS, Fully Depleted (FD) SOI, FinFETS, photonics, analog, SOC and RF applications.

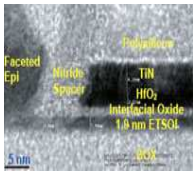
[*Source: SOI Industry Consortium*]

NEWS

Thin SOI Devices Shine at VLSI Symposium

IBM researchers went to the Symposium on VLSI Technology in Kyoto, Japan, to present a fully depleted CMOS process integration scheme for extremely thin silicon-on-insulator (ETSOI) devices, aimed at the 22 nm node and beyond.

The IBM process flow avoids implant steps, as does another thin buried oxide (BOX) SOI process flow presented at the symposium by researchers from the Hitachi Central Research Laboratory (Kokubunji, Japan). The Hitachi team said that in conventional CMOS on thin BOX substrates, halo implantation can cause damage to the gate oxide, especially at the gate edge. For the ultrathin BOX technology, which Hitachi calls Silicon on Thin BOX (SOTB), ion implantation was avoided to prevent damage to the oxide. Hitachi created SRAM devices that operated at 0.6 V, and said the ability to reduce the operating voltage was due to better control of the threshold voltage variations through the use of the thin buried oxide.



The IBM team developed prototype devices using its high-k/metal gate technology. The source/drain (S/D) and extensions were doped by an in situ epitaxial process, resulting in an implant-free flow to successfully reduce series resistance below 200 Ω/µm. "A zero-silicon-loss process was developed to eliminate loss of the thin SOI layer during gate and spacer processes, enabling structural demonstration of sub-2 nm ETSOI," the IBM team reported.

Even without strain boosters, the IBM paper claimed a "remarkable" pFET drive current of 550 µA/µm with a 6 nm SOI channel and a 25 nm physical gate length. A 15% reduction in parasitic capacitance was achieved by a faceted raised source/drain (RSD). "Excellent electrostatics and small device dimensions render ETSOI devices suitable for the 22 nm node and beyond," the IBM team reported.

IBM's VLSI symposium presentation said fully depleted SOI with an extremely thin body has advantages, including superior control of the short channel effect with negligible dopant fluctuation. However, ETSOI poses new challenges such as extension engineering, high series resistance, increased parasitic capacitance and nearly zero tolerance of silicon loss. The performance of the pFET is of particular concern, because the strain techniques that work well for pFETs in conventional CMOS, such as embedded silicon germanium (eSiGe) stressors, are not possible with ETSOI.

[*Source: Semiconductor International*]

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- European School On Nanosciences & Nanotechnologies
Grenoble, France.
August 23rd - September 12th, 2009

- 39th European Solid State Device Research Conference and 35th European Solid State Circuits Conference
Athens, Greece.
September 15th - 19th, 2009

- 2009 IEEE International SOI Conference
Foster City, USA.
October 5th - 8th, 2009

- 216th ECS Meeting
Vienna, Austria.
October 4th - 9th, 2009

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XV

AUG-SEPT, 2009

IN THIS NUMBER:

HIGHLIGHT NEWS

IBM's Power7 heats up server competition at Hot Chips

IBM Corp. walked away from Hot Chips conference with bragging rights to having the most muscular microprocessor with its Power7. The eight-core, 45nm chip is expected to set new watermarks in parallelism and cache that could translate into leading-edge performance for servers using it. Addressing the broader market for x86-based systems, Advanced Micro Devices will describe its 12-core Magny-Cours, its first to use a multichip module. Intel Corp. will detail its Nehalem EX, a souped-up version of the Xeon 5500 that debuted earlier this year.

Sun Microsystems, still waiting for approval of its merger with Oracle Corp., will present the latest version of its Sparc-based Niagara processor at the annual processor confab hosted by Stanford University.

When the dust settles, IBM likely will stand above the competition. The Power7 is expected to support as much or more cache, threads and memory bandwidth as any of the competition.

"I am sure Power7 will be the fastest processor around, probably faster than Intel's Nehalem in some benchmarks," said Nathan Brookwood, principal of market watcher Insight64 (Saratoga, Calif.).

Among its several advances, Power7 uses a mix of SRAM and IBM's embedded DRAM technology to pack on to the same die as the processor as much or more cache as any of its competitors. That's a big shift from the past three Power generations that used cache on separate die in a multichip module.

The shift from the two-core Power6 to the 4-, 6- and 8-core Power7 drove the need for more memory, a change that took years of effort both in IBM's silicon-on-insulator process technology and in memory architecture, said Bill Starke, an IBM Power architect who has worked on four generations of Power chips.

"We knew when we hit this level of multicore design, we would have to make the shift," Starke said. "We've been talking about this for several processor generations," he said.

The eDRAM cache of more than 32 Mbytes, improved off-chip signaling techniques "and a few more ingredients," helped IBM get beyond the 300 Gbyte/second memory bandwidth of the Power6. In addition, Power7 is said to pack as many as eight DDR3 memory channels.

"IBM will have far greater memory bandwidth than anyone else, and that matters because with multicore design the issues is getting data in fast enough to feed the beast and the Power7 beast will be well fed," said Brookwood. Early reports suggested Power7 had at least 16 Mbytes eDRAM. But the paper revealed IBM packed a whopping 32 Mbytes eDRAM as L3 cache on the 567 mm-square chip.

The Power7 is expected to scale back on the blistering 5 GHz data rate of the Power6 but ratchet up the support of multithreading from two to as many as four threads per core, the watermark previously held only by Sun's Niagara processors.

[Source: EETimes]

ANNOUNCEMENT

6th International SemOI Conference and 1st Ukrainian-French Seminar

First announcement and call for papers for the 6th International SemOI Conference and 1st Ukrainian-French Seminar to be held from 26th-30th April 2010 in Kyiv (Ukraine) have just been launched.

The goal of the Conference is to debate about the recent developments in nanometer down scaled Semiconductor-on-Insulator (SemOI) Systems which are basis blocks for modern high-sensitive sensors in a wide range of applications such as telecommunications, radiation control,, boimedical instrumentation, Chemicals análisis, etc.

FEATURE

High-end server chips breaking records

IBM spent years developing a new kind of eDRAM that would work with SOI (silicon on insulator) manufacturing processes, and the Power7 is the most advanced product to use the new technology.

Peter Glaskowsky

How would you like a single-chip microprocessor with more than four times the performance (on some applications) of Intel's best Core i7?

Then consider that up to 32 of these chips can be directly connected to form a single server, achieving four times the built-in scalability of Intel's next-generation Nehalem-EX processor.

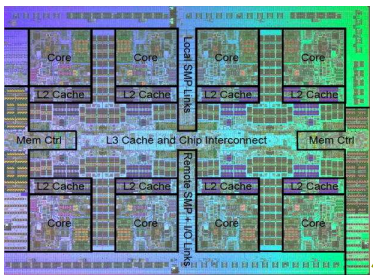
That's IBM's widely anticipated Power7, which it described at last week's Hot Chips conference. But if you're interested, you'd better be prepared to spend a lot more than four times as much per chip. IBM isn't talking about pricing, but large Power servers can cost more than $10,000 per processor.

What makes the Power7 so powerful? Each chip has eight cores, and each core supports four-way multithreading. There's 32MB of level-3 cache on the chip, made using embedded DRAM (eDRAM) cells. Most CPUs use SRAM for cache because it's generally easier to combine with high-performance logic, but DRAMs--with only one transistor per bit--offer compelling density advantages. IBM spent years developing a new kind of eDRAM that would work with SOI (silicon on insulator) manufacturing processes, and the Power7 is the most advanced product to use the new technology.

Interestingly, the Power7 cores run much more slowly than those in the Power6 processor, which I wrote about here in 2007 ("Live from Hot Chips 19: Session 1, IBM's Power6"). The Power6 was designed to run very fast using a long CPU pipeline in order to deliver the highest possible performance on each thread of execution.

Maybe that strategy didn't work out as well as IBM hoped, because the Power7 returns to a more traditional microarchitecture with a shorter pipeline and much lower clock rates--though IBM didn't say exactly what those rates would be.

IBM did, however, promise that the Power7 would be roughly four times as fast as the Power6, chip for chip. Since it has four times as many cores, each of the new slower-clocked cores must still deliver about as much performance as those in the previous generation.



NEWS

Smaller, cheaper cell phones possible

The paper outlines a new method for integrating a cell phone's power amplifier on the same chip with the rest of its internal parts using standard CMOS technology.

Ph.D. candidate Sataporn Pornpromlikit played a critical role in research at UC San Diego that made a big impact at a recent conference, and might provide manufacturers with the means for making cell phones both smaller and cheaper.

Pornpromlikit, who goes by the name Aui (pronounced way), was the lead author on the prize-winning paper, which was based on research carried out in the Power Amplifier Lab at UC San Diego's California Institute for Telecommunications and Information Technology (Calit2). The paper outlines a new method for integrating a cell phone's power amplifier on the same chip with the rest of its internal parts using standard CMOS technology.

CMOS, or Complementary Metal Oxide Semiconductor, is a low-cost integrated circuit process technology that has been driving the communications industry for the last few decades. Although the majority of cell phone circuitry has been successfully integrated onto a single silicon chip using CMOS, until recently the power amplifier -- the part of the device that amplifies the telephone signal -- needed a separate chip because of its high voltage requirement.

"Power amplifiers are among the most power-consuming components in the transceiver and need to be designed for the best power efficiency to maximize the cell phone's battery life," explains Aui. "They also need the best signal quality and to provide the required large output power.

"With the low breakdown voltage limit allowed by the advanced CMOS process," he adds, "the power efficiency suffers severely."

But his design solves the problem, Aui says, by distributing the required voltage equally among stacked transistors to allow for safe operation, even with the highest power output.

[*Source: Physorg.com*]

NEWS

NXP Dual Channel Class-D Amplifiers Bring Power Efficient Concert Hall-Like Sound Into the Vehicle

NXP, the independent semiconductor company founded by Philips, extended its leadership in vehicle audio entertainment, introducing a new family of dual channel Class-D amplifiers that deliver cutting-edge sound quality and energy efficiency. The new NXP TDF8599 Class-D amplifier family operates with maximum output power from 70 – 130 watts (250 watts mono), significantly reducing power dissipation in the vehicle head-unit when compared to traditional Class-AB amplifiers and ensuring more efficient heat management.

With an extremely high dynamic audio range, the new Class-D amplifiers transform the vehicle entertainment experience, delivering concert hall-like sound quality for best-possible audio enjoyment on the move. The TDF8599 amplifier family complements NXP's existing broad portfolio of highly energy-efficient Class-D amplifiers, and were developed to fit our customers' highest requirements.

Christian Seidel, Group Leader Hardware, Mechanics & Layout Audio System Engineering Group from Harman Becker Automotive Systems in Straubing, Germany said, "The TDF8599 series gives us the opportunity to dramatically reduce the power dissipation in our multichannel audio amplifiers and at the same time increase the sound quality to satisfy our customers' needs."

[*Source: Business Wire*]

NEWS IN BRIEF

Chartered to start 32nm pilot runs in 4Q09, sources say

Chartered Semiconductor Manufacturing is scheduled to launch its 32nm process technology in the fourth quarter of 2009, and move to 28nm in the first half of 2010, industry sources have revealed. The Singapore-based foundry is expected to update its process advancement at an upcoming technology forum in Taiwan.

Chartered's 28nm node will be based on high-k metal-gate (HKMG) technology from the IBM-led joint-development alliance, and built on a gate-first approach.

[*Source: Digitimes*]

NEWS

MOSIS MARKS EXPANDED SEMICONDUCTOR FOUNDRY OFFERINGS WITH SHUTTLE RUNS FOR SILICON-ON-INSULATOR (SOI)

The MOSIS Service, a leading provider of semiconductor fabrication solutions, announced that it has expanded its relationship with IBM to now include silicon-on-insulator (SOI) technology at multiple advanced lithography nodes. MOSIS is offering IBM's 45-nm SOI technology on 300mm wafers and IBM's 180-nm SOI technology on 200mm wafers. MOSIS customers now have a low-cost route to prototyping and low-volume production with leading-edge SOI foundry technologies that provide enhanced performance and very high integration capabilities.

The initial 45-nm shuttle run is scheduled for September 1, 2009. IBM's 45-nm 12S0 technology is the company's sixth generation of leading-edge SOI technologies and the first 300mm SOI technology to be offered through the MOSIS Service. This process provides significant transistor performance improvement (up to 30 percent) over traditional bulk technology at the same lithography node. The 45-nm SOI process offers four transistor options (Regular, High Vt, Super High Vt, Ultra High Vt), in addition to up to 11 metallization layers. A range of SRAM (Static Random Access Memory) and embedded DRAM (Dynamic Random Access Memory) options are also available, as well as a number of ESD (Electrostatic Discharge) protection options and high-quality passive elements. In addition to providing excellent isolation for analog circuit performance, this SOI offering can reduce the circuit area by up to 25 percent relative to bulk CMOS, which cuts the cost of overall semiconductor content.

The first available 180-nm SOI shuttle run has successfully been completed, with the next shuttle run scheduled for September 14, 2009. The low insertion loss and high isolation makes this technology an ideal choice for components such as RF switches that perform the function of On/Off devices in wireless applications like cell phones, WiMAX and WLANs (Wireless Local Area Networks).

"MOSIS is delighted to partner with IBM to now offer SOI foundry technologies," said Wes Hansford, Deputy Director of MOSIS. "The 180-nm 7RF SOI technology provides a very compelling alternative to GaAS (Gallium Arsenide) technology for RF switches, while the 45-nm SOI technology delivers outstanding performance while maximizing power efficiency and minimizing overall chip size for SOC (System-on-Chip) applications. By broadening our portfolio, MOSIS provides a single interface between designers and a greater range of foundry services, thereby enabling our clients with a faster and lower-cost route to market."

"This is a natural next step for our partnership with MOSIS and makes our advanced SOI technology accessible to an even broader array of innovators," said Regina Darmoni, IBM's Director of Analog/Mixed Signal & Digital Foundry. "MOSIS provides IBM with additional channels to market, and we are looking forward to this further expansion of our fabrication solutions to enable a new generation of advanced devices and clients."

[*Source: MOSIS*]

NEWS

Cadence Validates ARM Optimized Libraries for 45nm SOI Process

"These new silicon-validated libraries 45nm SOI libraries enable the creation of power efficient SOC's, while reducing development time and cost." says Tom Lantzsch.

Cadence Design Systems, Inc., the leader in global electronic design innovation, announced that they have validated a new generation of ASIC libraries from ARM using the Cadence® Encounter® Digital Implementation System targeting IBM's 45-nanometer silicon-on-insulator (SOI) manufacturing process. The development marks another milestone in a multiyear collaboration enabling efficient utilization of IBM's low-power, high-performance SOI technology for next-generation designs.

"Our collaboration with Cadence on the early validation of their tools will ensure design readiness for customers of IBM's 45nm SOI technology. Collectively, ARM, Cadence and IBM offer a reliable design platform wherever speed, functionality and low power consumption are needed," said Tom Lantzsch, vice president, physical IP division, ARM. "These new silicon-validated libraries 45nm SOI libraries enable the creation of power efficient SOC's, while reducing development time and cost."

The ARM 45nm SOI libraries were developed using the Cadence Virtuoso® custom design platform 6.1 and validated on multiple designs in the Cadence Encounter Digital Implementation System, a complete RTL-to-GDSII design environment that features the Si2 Common Power Format (CPF) for low power design, native signoff-in-the-loop for interconnect extraction, timing, power, and signal integrity plus fully integrated Cadence design-for-manufacturing (DFM) technology. The entire Cadence end-to-end design, implementation, and verification solution is proven to fully support the SOI manufacturing process.

"The collaboration among Cadence, ARM and IBM is vital to designers targeting our SOI technology," said Richard Busch, director, IBM ASIC Products. "It's imperative that these libraries are designed, verified and implemented in close correlation to our SOI process so designers can achieve the full benefits of higher performance and lower power consumption versus bulk CMOS technologies."

[*Source: Cadence*]

NEWS

GlobalFoundries outlines roadmap, plans to break fab ground

Taking on UMC, TSMC and others, foundry startup GlobalFoundries Inc. has outlined its process roadmap and disclosed plans to break ground on its new U.S. fab.

The foundry startup will break ground on the fab. As previously reported, it plans a $4.5 billion, 300-mm fab in Malta in N.Y.'s Saratoga County that is expected to come online in 2012 with 35,000 wafer starts per month at full capacity.

GlobalFoundries (Sunnyvale, Calif.) is the silicon foundry venture created by the spinoff of Advanced Micro Devices Inc.'s manufacturing operations and backed by an investment from Advanced Technology Investment Co. (ATIC) of Abu Dhabi. It officially opened for business in March.

In the meantime, the company is ramping up its existing fabs in Dresden, Germany, which were once part of AMD. As expected, the company is going after the leading-edge foundry business, thereby competing against UMC, TSMC, and, to some degree, its fab partners in Chartered and Samsung. GlobalFoundries is part of IBM Corp.'s "fab club," which includes Chartered, IBM, Samsung and others.

"We feel we have an opportunity" despite the downturn, said Tom Sonderman, vice president of manufacturing systems and technology at GlobalFoundries. "Customers are looking for choices at the leading-edge."

At present, the company has one fab, dubbed Module 1. It is processing 45-nm wafers, based on silicon-on-insulator (SOI) technology and immersion lithography. Its only customer is AMD.

For critical layers, GlobalFoundries' main lithography vendor is ASML Holding NV. "We are also engaged with Nikon and Canon," Sonderman said. For low-k at 45-nm, the company is using Applied Materials Inc.'s Black Diamond films

[*Source: EETimes*]

REMEMBER:

First announcement and call for papers for the 6th International SemOI Conference and 1st Ukrainian-French Seminar

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EURO-SOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

CALENDAR

- European School On Nanosciences & Nanotechnologies
Grenoble, France.
August 23rd - September 12th, 2009

- 39th European Solid State Device Research Conference and 35th European Solid State Circuits Conference
Athens, Greece.
September 15th - 19th, 2009

- 2009 IEEE International SOI Conference
Foster City, USA.
October 5th - 8th, 2009

- 216th ECS Meeting
Vienna, Austria.
October 4th - 9th, 2009

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XVI

OCTOBER, 2009

IN THIS NUMBER:

HIGHLIGHT NEWS

IBM Announces Highest Performance Embedded Processor for System-on-Chip Designs

IBM Corporation announced the industry's highest performance, highest throughput processor for system-on-chip (SoC) product families in the communication, storage, consumer, and aerospace and defense markets.

LSI Corporation has collaborated with IBM on the development of the processor core, called the PowerPC® 476FP. LSI intends to utilize the 476FP PowerPC core in its next-generation multicore platform architecture for networking applications.

The PowerPC 476FP operates at clock speeds in excess of 1.6 GHz, and 2.5 Dhrystone MIPS (million instructions per second) per MHz, delivering over two times the performance of IBM's most advanced embedded core currently available for the original equipment manufacturing (OEM) market. This level of performance also positions the 476FP as the highest performing embedded processor for System-on-Chip designs yet announced and available in the industry.

The processor extends the scalability of IBM's Power Architecture® in traditional embedded applications, and provides a growth platform for emerging applications such as 4G networks and WiMax infrastructure products.

The processor dissipates just 1.6 watts at these performance levels when fabricated in IBM's 45-nanometer, silicon-on-insulator (SOI) technology, positioning the 476FP as one of the most energy efficient embedded processor cores in the industry.

The 476FP offering includes an architectural extension of IBM's CoreConnect local bus technology (PLB6), supporting coherency for multiple processors and providing a level of scalability that is ideal for customers designing families of products and focusing on software re-use. The 476FP provides a seamless performance boost to all customers currently using the PowerPC 4xx family of processor cores, maintaining IBM's long-standing practice of protecting legacy software investments.

"We are pleased to announce this new embedded PowerPC processor," said Richard Busch, IBM director of ASIC products. "This high-performance, power efficient, compact processor core allows customers to meet the needs of today's applications, while preserving legacy code. Our collaboration with LSI brings together IBM's expertise in processor development with LSI's experience in networking and storage architectures, optimizing this core to address today's high-speed embedded requirements."

LSI has designed a configurable level 2 (L2) memory cache that is tightly coupled to the processor, which helps the PPC476 achieve its leading performance. There are three configurations of the L2 (256K, 512K and 1M) to allow customer optimization in a given application.

"LSI will be the first to offer products with the PowerPC 476FP core produced from our close collaboration with IBM," said Gene Scuteri, vice president, Networking Components Division, LSI. "Our use of the PowerPC 476 core, along with the configurable L2 cache that LSI developed as part of the collaboration, results in a powerful multicore processor subsystem that is well suited to future networking applications. The PowerPC 476 is a key building block in the next-generation multicore platform architecture from LSI."

[*Source: IBM*]

ANNOUNCEMENT

First Call for the Sixth EUROSOI Workshop

First announcement and opening of online abstract submission for the EUROSOI 2010 Workshop to be held from 25th-27th January 2010 in Granoble (France) have just been launched.

More information on page 2

FEATURE

Building an SOI IP/EDA Infrastructure

As with all new technologies, SOI brings about a chicken-and-egg kind of situation. IP availability is needed to drive adoption, but most third-party IP providers will want to see adoption before moving ahead

Richard Goering

My last blog on silicon-on-insulator looked at the low-power benefits of SOI. But performance and power gains are meaningless if you can't design and manufacture a chip. Fortunately, the needed infrastructure to support SOI design is falling into place.

As the SOI Consortium noted in a Design Automation Conference presentation, the SOI semiconductor ecosystem is expanding. Foundry support is available from Chartered, GlobalFoundries, Freescale, IBM, and UMC. SOI-ready libraries and silicon IP, memory IP, EDA tools and methodologies, and design services are all available from various providers. As the presentation notes, one tool that supports SOI implementation is the Cadence Encounter Digital Implementation System.

ARM, which has been a strong supporter of SOI, offers a physical IP SOI library portfolio. It includes a standard cell library, I/O library, memories, and tools. At the recent Design Automation Conference, Cadence announced validation of 45 nm IBM SOI ASIC libraries from ARM using the Encounter Digital Implementation System. "This should accelerate the IP infrastructure build-out," commented Jeff Wolf, director of membership development at the SOI Consortium.

According to Rahul Deokar, product marketing director at Cadence, SOI does not significantly change the IC design flow. The main challenge for EDA tools is to correctly model the "history effect" that occurs because the threshold voltage of a transistor may depend on its previous states. This occurs because of the "floating body" transistor effect.

Chin-Chi Teng, vice president of research and development at Cadence, added that Cadence accurately accounts for the history effect in library characterization and that these models are then seamlessly used during timing/signal integrity (SI) analysis and design optimization. He said that Cadence offers a "two-pass" signal-integrity analysis capability that's especially useful for SOI. It mostly operates at the cell level, but has the capability to drop down to the transistor level for critical portions of the chip to ensure that no SI violation is missed.

"The Cadence SOI design flow is very pushbutton," Rahul said. "You just bring in the characterized library, and all of the other steps are the same IC design flow."

The biggest enabler for SOI, Rahul said, will be the availability of libraries and IP. "I believe the libraries are getting ready," he said. "IP will be an ongoing process." While there is "increasing interest for sure" in SOI, he noted, adoption is so far mainly limited to the IBM ecosystem.

As with all new technologies, SOI brings about a chicken-and-egg kind of situation. IP availability is needed to drive adoption, but most third-party IP providers will want to see adoption before moving ahead. I think ARM deserves a lot of credit for jumping in ahead of the curve. Now it's up to SOI advocates to make a strong enough case for the technology to move it from specialized, high-performance applications into the IC design mainstream.

[*Source: Cadence*]

NEWS

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Online Abstract Submission now available for the EUROSOI 2010 Workshop

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008) and Göteborg (2009), EUROSOI 2010 will be held in Grenoble, France. It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

EUROSOI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and application-oriented engineers.

Abstract submission is now available online at the Workshop website **http://chalmers2010.eurosoi.org** as well as complementary information.

NEWS

ARM 1176 in IBM SoI process demonstrates a cell-based flow

For several years it has been clear that SoI processes have a more favorable speed vs. voltage characteristic than comparable-node bulk silicon processes. This advantage can mean either lower operating voltage at a given speed---and thus lower power—or higher performance at a given voltage. And the presence of vast quantities of both the Xbox 360 and the PlayStation-3 should eliminate any question about volume manufacture, at least from IBM. So why is SoI still so rarely used?

The normal answer is the lack of design infrastructure. Early on, most SoI designs were at the high-performance fringe, and so people rightly associated SoI with custom design and highly-skilled teams. It would require new device models, new libraries, and new tools to make SoI work in a normal cell-based RTL flow, this reasoning said.

But three papers at the IEEE International SoI Conference strongly suggest that the situation has changed. Jean-Luc Pelloie of ARM, Kevin Kranen of Synopsys, and Michael Jacobs of Cadence described implementation of a synthesizable ARM 1176 core with its associated memories and I/Os in IBMs 45nm SoI CMOS, using an off-the-shelf Synopsys-based standard flow. Pelloie's paper described the design decisions and results, while Kranen's and Jacobs's papers described the flow and how it was possible to use standard tools.

[*Source: EDN*]

ANNOUNCEMENT

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The goal of the Conference is to debate about the recent developments in nanometer down scaled Semiconductor-on-Insulator (SemOI) Systems which are basis blocks for modern high-sensitive sensors in a wide range of applications such as telecommunications, radiation control,, boimedical instrumentation, Chemicals análisis, etc.

Download announcement in pdf format at *http://www.eurosoi.org*

NEWS

Leti's Planar-SOI Technology Meets Low-Power, 22nm Node Requirements, Supports Development of "Green" Products

Leti, a leading global research center committed to creating and commercializing innovation in micro- and nanotechnologies, today presented results at the SOI Industry Consortium workshop in Leuven, Belgium, that prove SOI-based planar CMOS meets requirements for low-power, 22nm node devices, offering a practical route to further feature shrink and enabling a significant jump for "green" products.

With unmatched access resistance and electrostatic characteristics, planar SOI is superior to other technologies based on bulk CMOS technology and FinFET architecture. It also shows outstanding performances for low-power applications requiring 22nm technology, such as consumer electronic devices including 4G mobile phones.

"Many transistor architectures have been proposed for the 22nm node and below. At Leti, we favored planar technologies for faster and easier transition to manufacturing," said Laurent Malier, CEO of Leti. "Our recent results prove the strength of this approach. Together with the recent ARM results demonstrating power reduction on 45nm technology, we have proven that SOI technologies offer solutions for low power at a wide variety of nodes, including 22nm and below. Furthermore, we have demonstrated that planar SOI dramatically improves the energy performances of many products that will change our lives, while offering long-term success for many companies involved in these fast-growing markets."

In addition, drain-induced barrier lowering (DIBL) below 100mV/V has been demonstrated and SOI has been proven to enable the reduction of electrostatic parasitics.

While variability is a major challenge to be addressed for the 22nm node, Leti's results prove that variability control is possible with today's state-of-the-art SOI wafers. In particular, variability on threshold voltage was reduced by a factor of two compared with FinFET technologies, at wafer and batch levels.

Leti also showed that fully depleted SOI (FDSOI) CMOS can be scaled down to the 10nm node through tuning the buried oxide and silicon layer thickness. Displayed results show that FDSOI approach also addresses the variability issues for this further shrink.

CEA is a French Research and Technology Organization, with activities in three main areas: Energy, Technologies for Information and Healthcare, and Defence and Security. Within CEA, the Laboratory for Electronics & Information Technology (CEA-Leti) works with companies in order to increase their competitiveness through technological innovation and transfers. Leti is focused on micro and nanotechnologies and their applications, from wireless devices and systems, to biology and healthcare or photonics. Nanoelectronics and Microsystems (MEMS) are at the core of its silicon activities. As a major player in the MINATEC innovation campus, LETI operates 8,000-m² state-of-the-art clean rooms, on 24/7 mode, on 200mm and 300mm wafer standards.

[*Source: NanoTechWire*]

EVENTS

ISCAS 2010

The IEEE International Symposium on Circuits and Systems (ISCAS) is the world's premier networking forum of leading researchers in the highly active fields of theory, design and implementation of circuits and systems.

ISCAS 2010, sponsored by the IEEE Circuits and Systems Society and supported by the Institut Supérieur d'Electronique de Paris, will be held in Paris, France from 30 May to 2 June 2010.

The Symposium will focus on circuits and systems employing nanodevices (both extremely scaled CMOS and non-CMOS devices) and circuit fabrics (mixture of standard CMOS and evolving nano-structure elements) and their implementation cost, switching speed, energy efficiency, and reliability.

NEWS

SOI Industry Consortium announces SOI Design Clinic at ARM TechCon3

The SOI Industry Consortium today announced an initiative to deliver a silicon on insulator (SOI) educational event in conjunction with ARM TechCon3 to help the electronics industry reap the benefits of SOI. Responding to the industry's need for education in this area, the SOI Design Clinic will provide IC designers and engineering management with a technical understanding of significant differences between designing on SOI versus bulk silicon, and how to receive the power-saving, integration, reliability and performance advantages of SOI. Respected experts from the semiconductor industry will deliver training and share their insights at this practical and timely event, to help attendees evaluate and plan their move to SOI.

Shrinking semiconductor feature sizes demonstrate that CMOS on bulk silicon is rapidly reaching its technological limits for many applications. Process complexity, variability, short-channel effects, leakage, power density, and reliability are just a few reasons why technology leaders transition to SOI. Today available foundry processes, libraries, EDA tools and designer training are making SOI accessible to fabless semiconductor companies and OEMs, and enabling first-time SOI design teams to achieve improved power, performance and area results in their customary design cycle times, as documented by ARM in a recent study.

The design clinic will take place in the Santa Clara Convention Center (California) on October 21, 2009, co-located with ARM TechCon3

[*Source: SOI Industry Consortium*]

NEWS

ARM teaches world how to use SOI process technology

ARM is working with the SOI Industry Consortium to run a silicon on insulator (SOI) design seminar.

The company recognises a need to help IC designers understand the significant differences between designing on SOI versus bulk silicon, to achieve power-saving and integration benefits.

The mantra coming out of this event is that srinking semiconductor feature sizes demonstrate that CMOS on bulk silicon is rapidly reaching its technological limits for many applications.

There is a theory that ARM could force a rethink on low-power process technology

ARM is claiming potential power savings of up to 40% using a silicon-on-insulator (SOI) 45nm test chip.

The SOI process, an alternative to the traditional bulk CMOS process used to fab ARM-based processors, was demonstrated on a test chip was based on an ARM 1176 processor.

According to ARM, the demonstration shows that SOI technology is a "viable alternative to traditional bulk process technology when designing low-power processors".

"Process complexity, variability, short-channel effects, leakage, power density, and reliabilityre just a few reasons why technology leaders transition to SOI," said the SOI Industry Consortium.

Foundry processes, libraries, EDA tools and designer training are making SOI accessible to fabless semiconductor companies.

[*Source: ElectronicsWeekly*]

IMPORTANT:

December 1st is the deadline for Abstract Submission fot the EUROSOI 2010 Workshop

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Mail: eurosoi@ugr.es

CALENDAR

- NanoICT School 2009
San Sebastián, Spain.
October 26th - 30th, 2009

- EUROSOI 2010 Workshop
Grenoble, France.
January 25th - 27th, 2010

- 217 ECS Meeting
Vancouver, Canada.
April 25th - 30th, 2010

- International Symposium on Circuits and Systems. ISCAS 2010
Paris, France.
May 30th - 2nd, 2010

- ESSDERC ESSCRIC 2010
Sevilla, Spain.
September 13th - 17th, 2010

- 218 ECS Meeting
Las Vegas, USA.
October 10th - 15th, 2010

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XVII

NOVEMBER, 2009

IN THIS NUMBER:

HIGHLIGHT NEWS

Soitec and CEA-Leti to Join Forces to Speed Commercial Adoption of 3D Integration; Plans Target a Joint Comprehensive Industrial Solution for Wafer-Level 3D Integration

The Soitec Group, the world's leading supplier of engineered substrates for the microelectronics industry, and CEA-Leti, a leading global research center committed to creating and commercializing innovation in micro- and nanotechnologies, announced plans to expand their collaboration on wafer-to-wafer 3D integration by offering customers a joint, comprehensive industrial solution. The global offer envisioned by the long-term partners begins with process customization for prototype demonstration and will include licensing, both in 200mm and 300mm.

3D-level integration allows stacking integrated circuits and connecting them vertically. The technology enables increased performance, smaller form factors, and reduced power consumption, while lowering the costs of next-generation electronic devices. Potential markets and applications include image sensors, logic on logic, memory on memory, sensors on logic, memory on logic and new heterogeneous solutions such as MEMS on logic and photonics on logic.

Soitec's contribution to the partnership includes its Smart Stacking(TM) technology, which enables wafer-to-wafer-level stacking of partially or fully processed circuits; its low-temperature Smart Cut(TM) process; and the copper-to-copper bonding technology already in development with CEA-Leti. This offer also leverages Soitec's core expertise in wafer bonding and thinning technologies as well as its unique industrial background in this field.

CEA-Leti, likewise, offers broad and deep 3D wafer-to-wafer technology and expertise. These include all the necessary process steps for different 3D approaches, such as connecting vias, and cost-effective technologies such as wafer pre-processing, bonding, thinning and TSV etching and filling, and post-processing wafer assembly.

"As the leaders in the building-block technologies that enable 3D integration at the wafer-to-wafer level, Soitec and Leti are uniquely positioned to offer customers a comprehensive solution," said Andre-Jacques Auberton-Herve, Soitec president and CEO. "Leveraging Leti's 3D expertise and our well known bonding industrial experience, we can offer customers prototyping solutions as well as the processes they'll need for rapid ramp to full-scale production."

"We are proud to expand our partnership with Soitec and make the Grenoble Valley a center for 3D technology. This partnership will leverage CEA-Leti's extensive work in this area, including our 3D integration technology toolbox," said Laurent Malier, CEO of CEA-Leti. "Given CEA-Leti and Soitec's successful history of innovation, industrialization and collaboration, we expect our global offer to significantly advance commercial adoption of 3D integration technologies."

[Source: Semiconductor International]

EUROSOI ANNOUNCEMENTS

Second Call and Online Abstract Submission for the Sixth EUROSOI Workshop

Second call and online abstract submission are now available for the EUROSOI 2010 Workshop to be held from 25th-27th January 2010 in Grenoble (France).

(More information on page 3)

NEWS

Soitec CEO sees positive momentum in SOI markets

"The loss is higher than in the first half of 2008-2009" but, Soitec CEO specified, "revenues are different." .

Despite a widening net loss, year-over-year, in the first half of fiscal year 2009-2010, French SOI specialist Soitec SA said it has detected signs of renewed optimism in SOI markets for 2010 and beyond.

For the first half of financial year 2009-2010, Soitec published consolidated sales of 94.2 million euros ($142 million), down 21.7 percent year-on-year. The operating loss amounted to 15.8 million euros ($23.8 million), versus 9.4 million euros ($14.1 million) in the first half of the previous financial year. And, the net loss reached 19.4 million euros ($29.2 million), compared to a loss of 8.0 million euros ($12 million) in the same period of 2008-2009.

At a press conference last week in Paris, André-Jacques Auberton-Hervé, president and CEO of Soitec SA (Bernin, France), acknowledged that "the loss is higher than in the first half of 2008-2009" but, he specified, "revenues are different."

Auberton-Hervé continued: "We have recorded a net financial charge but behind there is only good management as we have secured our investments. Our cash has been invested in treasury bonds thus remains available and protected. We have generated 306 million euros of free cash flow. The debt has been reduced on a sequential basis, from 35.3 million euros ($53.2 million) to 19.4 million euros ($29.2 million)."

Soitec's CEO noted that a particularity of the semiconductor industry is its ability to quickly overcome a crisis. He further commented: "The crisis is behind us. Forecasts have constantly improved throughout the year, and there is a sense of renewed optimism for the year 2010 with growth areas that reach again comfortable levels. The SOI technology is at the heart of this rebound. We have taken the right decisions to enable a rebound."

Auberton-Hervé noted that Soitec's R&D efforts remained unchanged as it was out of question to slow them down during and exiting the crisis. An effort was also made in overall expenses.

Taking a broader look at the industry, Auberton-Hervé said he has witnessed positive momentum in SOI markets. He declared: "Despite the crisis, all players have proven that the SOI offer is valid. The SOI consortium now counts more than 30 members, and this figure proves the interest of the SOI technology."

The recent ARM announcement is essential as it demonstrates the interest of a SOI platform for SoC applications, Soitec's CEO continued.

This reference takes us back to October, when ARM indeed reported on a silicon-on-insulator (SOI) 45-nm test chip that demonstrates potential power savings of up to 40 percent over traditional bulk process for manufacturing chips at the same geometry.

[*Source: EETimes*]

NEWS

Mentor Graphics joins SOI consortium

"We can help designers and manufacturers exploit all of the underlying goodness of SOI technology", commented Robert Hum.

The silicon-on-insulator (SOI) Industry Consortium announced that Mentor Graphics Corp. has joined the organization.

By joining the consortium, Mentor Graphics (Wilsonville, Ore.) said it aims at expanding EDA tool and methodology support for the SOI technology. More specifically, Mentor said it will work on advancing design automation support for SOI-based products and systems in collaboration with other members.

"As we engage our expertise in modeling, characterization, analytics and constructive design tools with the needs of the global SOI user community, we can help designers and manufacturers exploit all of the underlying goodness of SOI technology," commented Robert Hum, VP and GM, Deep Submicron Technologies at Mentor Graphics.

Formed in 2007, the SOI consortium aims at accelerating the SOI technology and promoting its benefits in the market.

The founding membership in the group includes AMD, ARM, Cadence Design Systems, CEA-Leti, Chartered Semiconductor Manufacturing, Freescale Semiconductor, IBM, Innovative Silicon, KLA-Tencor, Lam Research, NXP, Samsung, Semico, Soitec, SEH Europe, STMicroelectronics, Synopsys, TSMC and UMC.

[*Source: EETimes*]

ANNOUNCEMENTS

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Download announcement in pdf format at http://www.eurosoi.org

EUROSOI NEWS

EUROSOI Exchange Grants

EUROSOI+ will fund exchanges in terms of travelling and research visits for scientists (students and senior scientists) in order to enhance collaborations and information exchange. Priority will be given to visits involving an industrial partner to allow a better integration of the European industry in the Network. These visits must be carried out before the end of **June 2010**.

To apply send a proposal to Andrés Godoy (agodoy@ugr.es) before **January 15th**, including a short CV, an invitation letter from the institution to be visited and a comprehensive description of the visit (purpose, destination, duration, budget, etc). The following requirements must be fulfilled:

- The field should fall within research domains defined by EUROSOI+
- At least one EUROSOI member should be involved in the project research.
- Priority will be given to industrial partners.
- Less than 4 weeks.
- Gender aspects will be considered (promote the participation of women).
- Not salary costs or expenses generated by research activities.

The visit should be carried out before the end of June 2010 (remember that there will be another call for proposals on May 2010).

After the visit (less than one month), the participant should provide a report describing the work developed during the visit.
The Management Board in its next meeting will decide which proposals are funded.

REMEMBER:

Abstract submission deadline for the EUROSOI2010 Workshop is 15th December.

EUROSOI NEWS

Abstract submission and registration for the EUROSOI 2010 Workshop

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008) and Göteborg (2009), EUROSOI 2010 will be held at Grenoble, France. It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

EUROSOI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and application-oriented engineers.

Abstract submission (until December 15th) and registration are now available online at the Workshop website as well as new information about fees, accommodations…

For further information and important deadlines take a look at

http://grenoble2010.eurosoi.org

NEWS

Comparing SOI and bulk FinFETs: Performance, manufacturing variability, and cost

FinFETs offer improved channel control and, therefore, reduced short channel effects. While the gate in a planar transistor sits above the channel, the gate of a FinFET wraps around the channel, providing electrostatic control from both sides.

As the semiconductor industry looks toward the 22nm technology node, some manufacturers are considering a transition from planar CMOS transistors to the three-dimensional (3D) FinFET device architecture. Relative to planar transistors, FinFETs offer improved channel control and, therefore, reduced short channel effects. While the gate in a planar transistor sits above the channel, the gate of a FinFET wraps around the channel, providing electrostatic control from both sides.

Challenges of a 3D structure

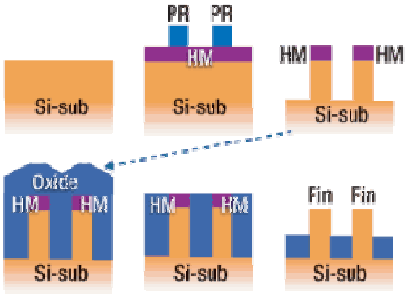
The 3D structure introduces new parasitic capacitances and new critical dimensions that must be controlled to optimize performance. The gate length in a FinFET is measured parallel to the length of the fin, while the gate width is the sum of twice the fin height plus the fin width. Fin height limits the drive current and the gate capacitance, while fin thickness affects threshold voltage and short channel control, as well as contributing to second order metrics such as power consumption.

In a 22nm node device, fin width might be on the order of 10-15nm. Fin height would ideally be twice that or more—increasing the fin height increases the transistor density, allowing more effective gate width to fit in a smaller planar footprint. As we will discuss, however, taller fins make both the fin etch and, for bulk FinFETs, the recess etch and isolation implant more difficult.

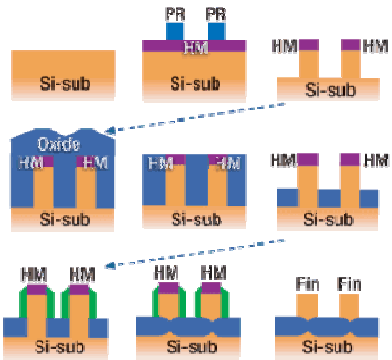
Controlled manufacturing of a 3D structure with such small features presents new process control challenges. The trench etch that creates the fins must maintain a vertical profile with minimal sidewall roughness over a 2:1 or greater aspect ratio. Variability and yield are important considerations as manufacturers decide which process flow to adopt.

This article analyzes the performance, variability, and cost of two potential FinFET process flows—one based on silicon-on-insulator (SOI) substrates, and one using bulk silicon substrates with an implanted junction for fin isolation.

SOI-based flow. The SOI-based flow is the most straightforward. The fin etch simply stops on the wafer's buried oxide layer; the fin height is defined by the initial SOI layer thickness. Moreover, because of the buried oxide layer, adjacent fins are fully isolated from each other and no additional isolation steps are required. In the fully-depleted, undoped-channel devices being considered for this node, only gate fabrication and source/drain implants are needed to complete the device.



Bulk silicon-based flow. In contrast, when a bulk silicon substrate is used, there is no clear demarcation of the base of the fin, and no inherent isolation layer. Instead, the process must manufacture transistor isolation. In a junction-isolated flow (Fig. 1), the fin etch is followed by an oxide fill step. The oxide deposition must fill a deep, high aspect ratio trench, without voids or other defects. Polishing the oxide back to the silicon sets the fin height, then a recess etch clears the space between fins. This recess etch, like the initial trench etch, has no obvious stop layer—etch depth depends on etch time, and is subject to microloading effects as the fin density varies through the design space. Though the oxide provides insulation between adjacent fins, the transistors are still connected underneath the oxide. A high-dose angled implant at the base of the fin creates a dopant junction and completes the isolation.



[*Source: ElectroIQ*]

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EURO-SOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

CALENDAR

- EUROSOI 2010 Workshop
Grenoble, France.
January 25th - 27th, 2010

- 217 ECS Meeting
Vancouver, Canada.
April 25th - 30th, 2010

- International Symposium on Circuits and Systems. ISCAS 2010
Paris, France.
May 30th - 2nd, 2010

- ESSDERC ESSCRIC 2010
Sevilla, Spain.
September 13th - 17th, 2010

- 218 ECS Meeting
Las Vegas, USA.
October 10th - 15th, 2010

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XVIII

DEC 2009/JAN 2010

IN THIS NUMBER:

HIGHLIGHT NEWS

Coming up: EUROSOI2010

EUROSOI, an international forum for promoting high-level scientific research and exchanges between research groups and industrial partners involved in silicon-on-insulator (SOI) activities all over the world, today announced the final program of its 6th annual conference, which will be held on January 25-27, 2010 in Grenoble, France. Horacio Mendez, executive director of the SOI Industry Consortium will kick off the conference with his plenary talk on "SOI for the Next 5 Years"; Professor Krishna Saraswat from Stanford University will present a plenary talk on "Germanium Integration on Silicon for High performance FETs and Optical Interconnects." In addition, 55 presentations have been selected for the technical program. World-class experts will give a five-session SOI tutorial entitled "Exploring New Routes with SOI" on the first day.

Key to EUROSOI's continued success is the exceptional synergy between fundamental science, applied physics, technology and SOI application-oriented developments. Following the tradition of previous meetings, EUROSOI'10 will be a lively experience featuring oral and poster sessions, key-note presentations, a training course as well as room for informal discussions. EUROSOI covers recent progress in SOI, including: (1) Synthesis of advanced SOI wafers (Ge, SiGe and strained layers, SOI heterostructures); (2) Materials evaluation, properties of ultra-thin films and buried oxides; (3) SOI MOSFETs: characterization, modeling and simulations, parameter extraction, reliability issues; (4) High performance and Low Power CMOS, (5) New domain of applications such as memories, sensors and MEMS; (6) Innovative devices: multiple-gates, tunneling transistors, nanowires, etc.

"SOI is entering a new era," notes conference co-chair Sorin Cristoloveanu, a professor and researcher at the IMEP research and education institute in Grenoble. Co-chair Olivier Faynot from CEA-Leti adds: "Originally used for high-performance technologies dedicated to the microprocessors market and gaming, it is now moving to other markets such as the Low Power and mobile applications, memory and power devices. These new markets offer huge opportunities, particularly with respect to the inherent energy savings of SOI, which will enable us to make a smooth transition to a greener world."

This year's EUROSOI conference is situated in the beautiful city of Grenoble, which can be considered the SOI capital of the world. Research on the fundamentals of SOI has been conducted in this area for more than 30 years by several local institutes including CEA-Leti (Applied research laboratory operated by the Technology Research Directorate of the French Atomic Energy Commission) and CNRS (National Council for Scientific Research), as well as the INP Grenoble University. It is also the home to Soitec, the world's leading manufacturer of SOI wafers.

EUROSOI'10 will be held on the MINATEC innovation campus, an international center for micro and nanotechnologies, which is home to 2400 researchers, 1200 students, and 600 technology transfer experts.

EUROSOI ANNOUNCEMENTS

Final Programme and Tutorials Information available for EUROSOI2010

The Final Programme as well as wide information about Tutorials are now available for the EUROSOI2010 Workshop to be held from 25th-27th January 2010 in Grenoble (France).

(More information on page 3)

NEWS

CMOS Transitions to 22 and 15 nm

Intel's director of process architecture and integration, said he and his Intel colleagues are "pretty pessimistic that partially depleted (PD) CMOS will extend to the 15 nm node." .

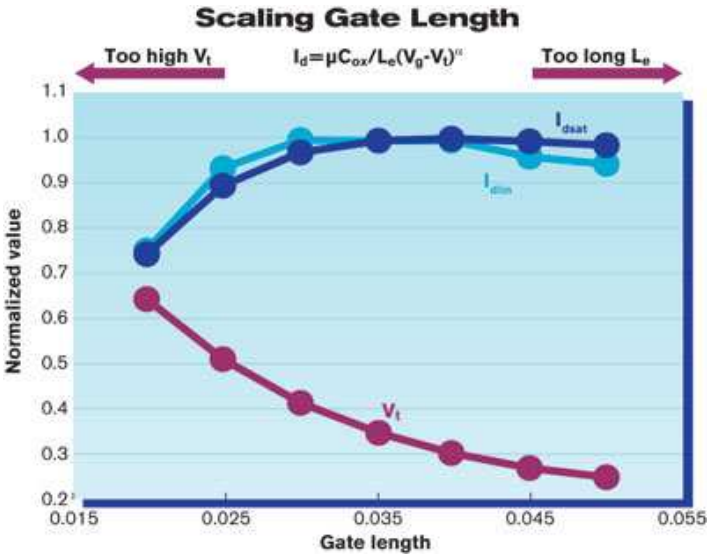
[…] the gate dielectric "is not thinning as fast as we need it to in order to make an appreciable improvement in gate length scaling," said Bruce Doris.

Technologists have long debated how far plain-vanilla planar CMOS transistors on bulk silicon wafers could be scaled. Now, the transition to new paradigms appears to be underway, with fully depleted CMOS almost definitely on the 15 nm roadmaps at IBM and Intel, with some form of vertical transistors being seriously considered as well.

Mark Bohr, Intel's director of process architecture and integration, said he and his Intel colleagues are "pretty pessimistic that partially depleted (PD) CMOS will extend to the 15 nm node." A planar, fully depleted (FD) technology could only be constructed on a silicon-on-insulator (SOI) substrate, Bohr said, but a tri-gate or finFET device could be created on either bulk or SOI wafers.

Gartner analyst Dean Freeman likens the current period to the early to mid-1980s, when first memory and then logic transitioned to CMOS. "The NPN transistor gave the CPU vendors a new lease on life. I think we are at a point like that again. But the question is out there: How do we keep innovating?"

Changes — whatever they may be — are coming because for the last generation or two, scaling the gate length (Lg) has resulted in reverse scaling (Fig. 1).1 To avoid short channel effects (SCE), more phosphorus and boron are being doped into the channel, raising threshold voltages and slowing transistors speeds. Random dopant fluctuations (RDF), in which the number of dopants in the channel vary as a function of the halo implantation, can have a large influence on the Vt, hurting performance and cutting overall yield.

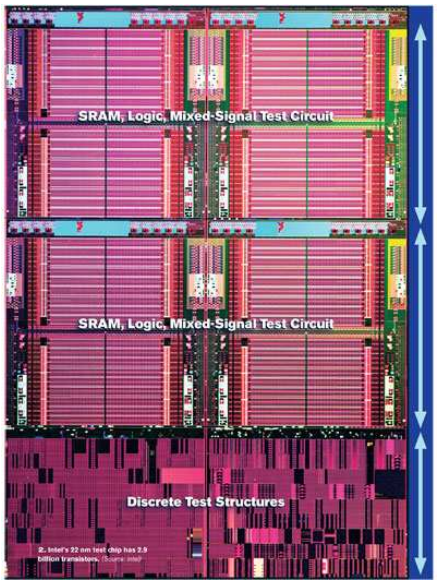


Strain also faces limits. More germanium can be added to the SiGe stressors — from the ~40% germanium level used at the 32 nm node — but there is less room for the material to create the strain.

While IBM, Intel and others are thinning the gate dielectric with high-k materials, the gate dielectric "is not thinning as fast as we need it to in order to make an appreciable improvement in gate length scaling," said Bruce Doris, manager of advanced device integration at IBM's Albany, N.Y., R&D center. Other knobs are getting harder to turn as well. Operating voltages are leveling off, making it more difficult to reduce power consumption. Making the junctions shallower is causing the source/drain resistance to increase.

What to do? At 22 nm, Intel will stay on a bulk technology, Bohr said. Intel is on track to introduce its 22 nm MPUs at the end of 2011. The Intel 22 nm test chip (Fig. 2) with SRAM arrays and logic peripheral circuits was introduced in September with a 364 Mb array size and 2.9 billion transistors. It includes a third-generation gate-last high-k/metal gate process that deposits both the dielectric and the metals at the end of the process.

[*Source: Semiconductor International*]



EUROSOI NEWS

EUROSOI Exchange Grants for scientists

EUROSOI+ will fund exchanges in terms of travelling and research visits for scientists (students and senior scientists) in order to enhance collaborations and information exchange. Priority will be given to visits involving an industrial partner to allow a better integration of the European industry in the Network. These visits must be carried out before the end of **June 2010**.

To apply send a proposal to Andrés Godoy (agodoy@ugr.es) before **January 15th**, including a short CV, an invitation letter from the institution to be visited and a comprehensive description of the visit (purpose, destination, duration, budget, etc). The following requirements must be fulfilled:

•The field should fall within research domains defined by EUROSOI+

•At least one EUROSOI member should be involved in the project research.

•Priority will be given to industrial partners.

•Less than 4 weeks.

•Gender aspects will be considered (promote the participation of women).

•Not salary costs or expenses generated by research activities.

The visit should be carried out before the end of June 2010 (remember that there will be another call for proposals on May 2010).

After the visit (less than one month), the participant should provide a report describing the work developed during the visit.

The Management Board in its next meeting will decide which proposals are funded.

REMEMBER:

Registration for EUROSOI2010 is open online at the Workshop website

NEWS

Soitec Bursts Into Solar Sector

Microelectronics substrate supplier the Soitec Group has announced a major shift into the solar technology sector with an agreement to acquire concentrating solar PV company Concentrix Solar GmbH.

Based in Freiburg, Germany, Concentrix is a 2005 spin-off company from the Fraunhofer Institute for Solar Energy Systems (ISE), and with its 80% share acquisition, Soitec also gains access to the concentrator solar cell technologies from the research institute, which will continue to hold the remaining 20%. Under the terms of the deal, Concentrix is valued at €55 million.

Simultaneously, Soitec signed a strategic technology alliance with both the Fraunhofer ISE and the CEA-Leti.

As part of the transaction, the Fraunhofer ISE has entered into a long-term technology license agreement with Soitec and the partners plan to develop the next generation of CPV cells based on Soitec's proprietary technologies. The collaboration includes CEA-Leti, Soitec's long-time partner within the Grenoble R&D cluster.

Soitec says it is entering the solar industry in order to expand its revenue base as worldwide demand for CPV is anticipated to ramp up strongly in the coming years. The company believes that its technologies in engineered substrates are key to improving solar cell performance, and therefore strongly complement Concentrix's high-efficiency CPV systems.

André-Jacques Auberton-Hervé, president and CEO of Soitec, commented: "This acquisition represents an exciting and natural expansion for Soitec into the fast-growing solar market, allowing us to leverage our technology and process knowledge in the development of high-performance and cost-competitive photovoltaic solutions up to the system level."

[*Source: RenewableEnergyWorld.com*]

EUROSOI NEWS

Registration for the EUROSOI 2010 Workshop

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008) and Göteborg (2009), EUROSOI 2010 will be held at Grenoble, France. It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

EUROSOI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and application-oriented engineers.

Registration is now available online at the Workshop website as well as new material such as Tutorials Information, Final Programme...

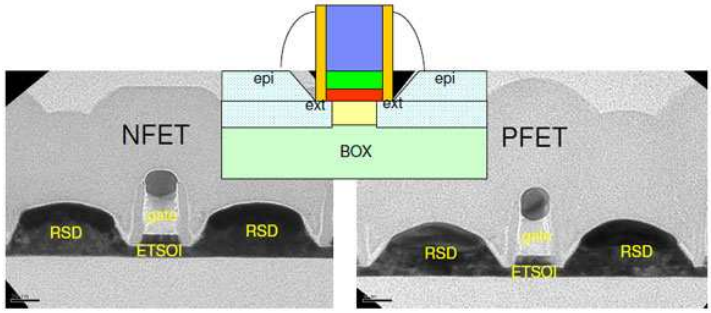
For further information and important dates take a look at

http://grenoble2010.eurosoi.org

NEWS

IBM Gains Confidence in 22 nm ETSOI

At the IEDM conference in Baltimore, IBM researchers indicated that a fully depleted CMOS on extremely thin SOI wafers may be the way to go at the 22 nm node. The approach allows reduced short channel effects, and supports gate length scaling to 25 nm and beyond. The fully depleted technology involves Soitec, which supplies wafers with a thin silicon layer on top of the buried oxide



The approach depends in part on the recent ability of SOI wafer provider Soitec to deliver SOI wafers with a silicon thickness in the 6 nm range, said Bruce Doris.

IBM researchers have developed a fully depleted CMOS technology on extremely thin SOI (ETSOI), aimed at the 22 nm technology generation and beyond.

In a presentation at the International Electron Devices Meeting (IEDM) in Baltimore, Kangguo Cheng, lead engineer on the 22 nm device integration team at IBM's Albany R&D center, said the FD-ETSOI process has a 25 nm gate length (Lg) and appears suitable for low-power applications. Besides FETs, IBM engineers created inductors, capacitors, veractors and other supporting devices needed to build system-on-a-chip (SoC) products on the thin SOI substrates.

The ETSOI technology incorporates several process innovations, including in situ doped epitaxial (implant-free) deposition of the source/drain and extension regions, and a faceted raised source/drain architecture.

The approach depends in part on the recent ability of SOI wafer provider Soitec (Bernin, France) to deliver SOI wafers with a silicon thickness in the 6 nm range, said Bruce Doris, manager of advanced device integration at IBM's Albany center. Most of the 300 mm SOI wafers delivered to IBM have an acceptable silicon thickness variation of ±5 Å, although the shipments from Soitec have been in limited quantities thus far.

Technologists face several challenges in scaling planar bulk CMOS to 25 nm gate lengths and beyond. The dopants in the channel are so few that random dopant fluctuations (RDF) cause threshold voltage (Vt) variations. Also, shallower junctions tend to have higher resistance. And voltage scaling has flattened for bulk CMOS, creating power consumption challenges.

[*Source: Semiconductor International*]

NEWS

Soitec and CEA-Leti to join forces to speed commercial adoption of 3D integration

The Soitec Group, the world's leading supplier of engineered substrates for the microelectronics industry, and CEA-Leti, a leading global research center committed to creating and commercializing innovation in micro- and nanotechnologies, announced plans to expand their collaboration on wafer-to-wafer 3D integration by offering customers a joint, comprehensive industrial solution. The global offer envisioned by the long-term partners begins with process customization for prototype demonstration and will include licensing, both in 200mm and 300mm.

3D-level integration allows stacking integrated circuits and connecting them vertically. The technology enables increased performance, smaller form factors, and reduced power consumption, while lowering the costs of next-generation electronic devices. Potential markets and applications include image sensors, logic on logic, memory on memory, sensors on logic, memory on logic and new heterogeneous solutions such as MEMS on logic and photonics on logic.

Soitec's contribution to the partnership includes its Smart Stacking™ technology, which enables wafer-to-wafer-level stacking of partially or fully processed circuits; its low-temperature Smart Cut™ process; and the copper-to-copper bonding technology already in development with CEA-Leti. This offer also leverages Soitec's core expertise in wafer bonding and thinning technologies as well as its unique industrial background in this field.

[*Source: Soitec*]

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EUROSOI Newsletter

VOLUME XIX

FEBRUARY, 2010

IN THIS NUMBER:

EDITORIAL

Francisco Gámiz
Professor
Univ. Granada (Spain)

EUROSOI has become an international forum for promoting high-level scientific research and exchanges between research groups and industrial partners involved in silicon-on-insulator (SOI) activities all over the world. A good example for this was its 6th annual conference, which was held on January 25-27, 2010 in Grenoble, France. Horacio Mendez, executive director of the SOI Industry Consortium kicked off the conference with his plenary talk on "SOI for the Next 5 Years"; Professor Krishna Saraswat from Stanford University presented a plenary talk on "Germanium Integration on Silicon for High performance FETs and Optical Interconnects." In addition, 55 presentations were selected for the technical program. Worldclass experts gave a five-session SOI tutorial entitled "Exploring New Routes with SOI" on the first day.

Prof. Sorin Cristoloveanu

Key to EUROSOI's continued success is the exceptional synergy between fundamental science, applied physics, technology and SOI application-oriented developments. Following the tradition of previous meetings, EUROSOI'10 was a lively experience featuring oral and poster sessions, keynote presentations, a training course as well as room for informal discussions. EUROSOI covered recent progress in SOI, including: (1) Synthesis of advanced SOI wafers (Ge, SiGe and strained layers, SOI heterostructures); (2) Materials evaluation, properties of ultra-thin films and buried oxides; (3) SOI MOSFETs: characterization, modeling and simulations, parameter extraction, reliability issues; (4) High performance and Low Power CMOS, (5) New domain of applications such as memories, sensors and MEMS; (6) Innovative devices: multiple-gates, tunneling transistors, nanowires, etc.

Some attendants having lunch.

Prof. Sorin Cristoloveanu from IMEP (Grenoble) and Dr. Olivier Faynot from CEA-Leti were these year the co-chairs of the conference. More than 150 researchers from all over the world attended the conference this year, which was held on the MINATEC innovation campus, an international center for micro and nanotechnologies, which is home to 2400 researchers, 1200 students, and 600 technology transfer experts.

(*Continues on page 2*)

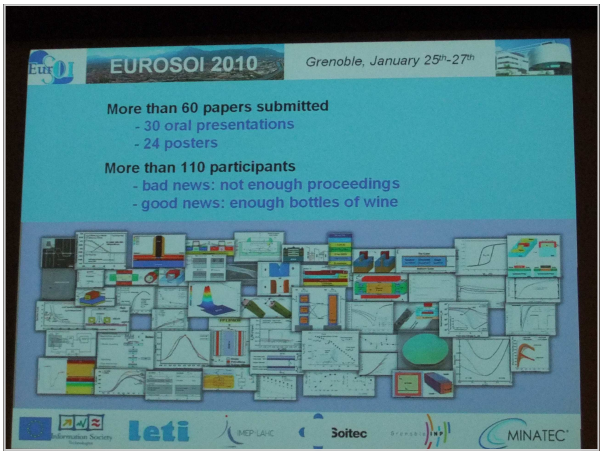
ANNOUNCEMENT EUROSOI2010

Tutorials added on the EUROSOI Website

Continuating the task initiated by EUROSOI with the publication online of the successive tutorials that have taken place during these last years, the tutorials of the Workshop held in Grenoble this past January are now available.

In this section, besides these last tutorials, the previous ones can also be found. They are organized according to their dates and places and a search engine by years has been also developed. For further details take a look at:

http://www.eurosoi.org/tutorials.asp



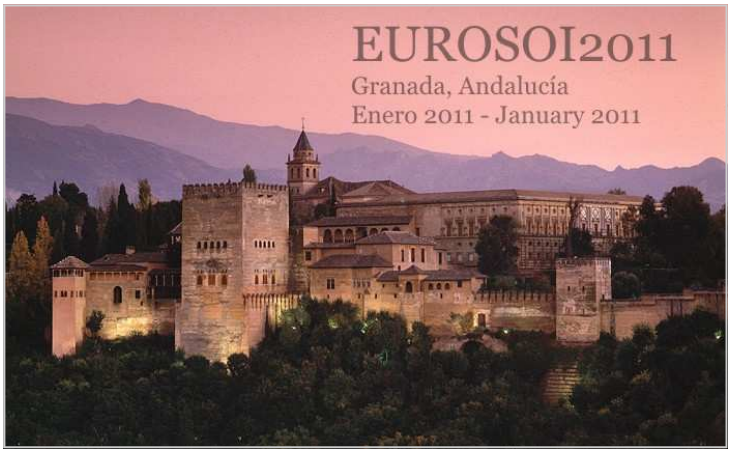
Overview of EUROSOI2010 statistics

Delicious French Chess

As main conclusion of the Conference, we could say that "SOI is entering a new era: Originally used for high-performance technologies dedicated to the microprocessors market and gaming, it is now moving to other markets such as the Low Power and mobile applications, memory and power devices. These new markets offer huge opportunities, particularly with respect to the inherent energy savings of SOI, which will enable us to make a smooth transition to a greener world."

We are already looking forward to meeting you in the Seventh Workshop of EUROSOI to be held in January 2011 in Granada, Spain.

MINATEC Venue



Coming up next year...

Prof. Colinge

(Francisco Gámiz is Coordinator of the EUROSOI+ Network)

NEWS

Concentrix Solar wins IEC certification for new PV module 'CX-75'

Concentrix Solar, a leading supplier of Concentrator Photovoltaic (CPV) systems and a new division of the Soitec Group (Euronext Paris), the world's supplier of engineered substrates, announced that the company has received IEC certification 62108 for its CX-75 FLATCON® module generation. The International Electrotechnical Commission (IEC) is the world's leading electrical and electronic standards organization. IEC 62108 is the CPV industry's standard, ensuring that modules and assemblies are suitable for long-term operation in a wide range of outdoor climates. By producing the CX-75 module in the company's industry-leading, fully-automated production line in Freiburg, Germany, Concentrix Solar is uniquely able to ensure consistent, highest-precision manufacturing in high volumes – a critical factor in ensuring high nominal AC system efficiency and long-term reliability.

"The IEC 62108 certificate is an important milestone, confirming that our new CX-75 module is ready for full, commercial deployment in utility-scale electricity production," said Concentrix Solar CEO, Hansjörg Lerchenmüller. "It attests that our systems are capable of withstanding prolonged exposure in harsh climates and are designed to withstand severe environmental conditions such as rain, hail and high winds."

[*Source: Soitec*]

"[...] our new CX-75 module is ready for full, commercial deployment in utility-scale electricity production." said Concentrix Solar CEO.

NEWS

TowerJazz and Soitec sign agreement to offer backside illumination platform for high-end image sensors

TowerJazz, the global specialty foundry leader and The Soitec Group (Euronext Paris), the world's leading supplier of silicon-on-insulator (SOI) and other engineered substrates for the microelectronics industry, announced that they have signed an agreement that will enable a turn-key solution for high-end backside illuminated (BSI) CMOS image sensors (CIS) for industrial, medical and automotive applications.

"The market for BSI CMOS image sensors replacing current Front Side Illumination (FSI) technology is expected to reach $800M in 2013," according to Jerome Baron, principal analyst at Yole Developpement. "The BSI image sensor market will be mainly driven by digital cameras and cell-phone applications, but high performance imaging applications such as medical, industrial and automotive vision sensors are also an important segment. We estimate the market for high-end BSI image sensors to reach $120M in the same time frame."

The TowerJazz BSI CIS offering will leverage the foundry's extensive expertise and leadership in CIS technology and will integrate SOI substrates and Soitec's new Smart Stacking™ circuit layer transfer technology, customized for the TowerJazz fabrication process. Soitec is the market leader in SOI wafers and circuit stacking solutions and TowerJazz is well-known for its industry leading pixel performance. This collaboration will enable a rapid ramp to a complete BSI foundry solution that can be transparently utilized by TowerJazz customers.

"We estimate the market for high-end BSI image sensors to reach $120M", said Jerome Baron

ANNOUNCEMENT

Korean International Summer School on Nanoelectronics

The Korean International Summer School on Nanoelectronics is a new annual event, starting in 2010. Nano-KISS will offer every year a panel of detailed lectures on emerging fields in nano-micro-electronics, given by world-class experts. The first edition in 2010 is dedicated to advanced SOI concepts and technologies. It is a unique opportunity for senior and junior researchers to update their knowledge in the rapidly growing field of SOI components. Nano-KISS will bring together scientists from all over the world universities, R&D centers and companies. Nano-KISS is based on the successful model of MIGAS, the international Summer School on Microeletronics, organized for many years in Grenoble area. Nano-KISS is organized by Kyungpook National University (KNU) and Grenoble Insitute of Technology (NPG) via World-Class University and Brain Korea 21 projects.

FEATURE

Remaking The Design Landscape

By Ed Sperling

Every now and then a new trend comes along in the semiconductor design world, often because an old tool doesn't work well anymore or because a new one is achieving critical mass. Lithography moved to immersion when the wavelength couldn't be refracted far enough anymore. Designers at the advanced end of Moore's Law began using tools like high-level synthesis and Transaction-Level Modeling 2.0 to help sort out the complexities of multicore, multi-voltage, multi-power island designs.

What's changing at 32nm and beyond is the number of different directions the industry is heading. In the past, each new node brought new changes. At 130nm, the changes were considered extremely difficult because manufacturing moved from 200mm to 300mm wafers, added copper interconnects and low-k dielectrics for insulation. Most developers and chipmakers heaved a sigh of relief when that transition was over. But in retrospect, that was relatively tame.

Interviews with dozens of engineers, vendors, scientists, researchers and business managers over the past six months show that what's ahead cannot be bounded into just one or two shifts. The change under way now is geographically global. It's moving to a higher and higher level of abstraction, from semiconductor to system to device. And it is as much driven by business as technology. Moreover, taken in total these changes will completely alter the basic fabric of the design community in ways that have never been seen before.

Business

Behind many of the changes afoot in the market there is always a business case. In the past, technology trumped business. Those with steely nerve and enough backing could often carve out a space for themselves in markets, and even if they weren't entirely successful they could minimize their losses.

Three things changed over the past decade to alter this approach. Business now trumps technology in almost all cases. First, the venture community has grown more cautious about the rate of return in hardware and EDA tools ever since the dot-com bubble burst in 2001. It's not possible to return to the tap anymore without a real product and a real business model.

Second, the cost of failure has gone up. It now costs $4 billion to $5 billion to build a state-of-the-art fab. Consortiums of very large companies and governments are now involved in this business. And it can cost upwards of $100 million to build a very complex SoC at the latest process node. Stalwart adherents to Moore's Law such as Freescale, which made the leap to the next process node without hesitation until 90nm, have begun skipping nodes on certain products.

Third, chips are now so complicated that it takes too long to build everything from scratch. That means chipmakers must buy IP from third parties. Even Intel doesn't make everything itself anymore. And all but a very few companies now use a fabless or fab-lite model for at least the digital portion of their chips, which forces them to adhere to design rules and process technology developed by the foundries.

Put these together and the result is that business issues are forcing a handoff of some of the most basic parts of semiconductor engineering—defining a unique architecture, tinkering with the layout, refining the process, and balancing all of these pieces together at tape-out. Fast yield, time to market and standardized interconnects and IP are no longer just goals. They are requirements. Some companies have handed off the building of chips entirely to a new class of value-chain producers like eSilicon, Global Unichip and Open-Silicon.

Globalization

For the first 50 years of its existence, the semiconductor industry defined global as North America, Europe and Japan. Taiwan was a latecomer to the part, and TSMC's vision of a foundry model was considered revolutionary well into the 1990s. Companies like Texas Instruments and AMD said they had no intention of letting go of their own fabs.

Fast forward through two downturns and 10 process nodes and the situation now looks much different. Software is increasingly a part of the design process, heavily automated foundries can be located anywhere in the world where tax breaks and the cost of power are lowest, and massive education programs are under way in multiple countries that see semiconductor and computer engineering as a fast way to economic health.

While many lament that the semiconductor industry is declining or not showing growth, the opposite is happening. It's expanding significantly. In 1977, the Semiconductor Industry Association reported total semiconductor sales of $2.88 billion, with about $1.92 billion of that in the Americas and only $182 million in Asia/Pacific (not including Japan). In the first 11 months of 2009, sales were $196 billion worldwide, with $102 billion in Asia/Pacific and $33 billion in the Americas.

By any standard this represents an enormous increase in sales, but the profits are now far more dispersed around the globe. Moreover, IP for chips is being developed in places like Eastern Europe and former Soviet republics, and in the future that kind of work will accelerate in other parts of the world because the barrier to entry into this market is one of the lowest—you don't need to build full systems—while the return on investment is one of the highest. Virage Logic, ARM and Synopsys have been snapping up these kinds of operations around the globe over the past couple years.

[*Source: System Level Design*]

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EUROSOI Newsletter

VOLUME XX

MARCH 2010

IN THIS NUMBER:

HIGHLIGHT NEWS

RF Micro Devices(R) Introduces First Silicon Switches for 3G Smartphones

RF Micro Devices, a global leader in the design and manufacture of high-performance radio frequency components and compound semiconductor technologies, announced that the Company has successfully qualified and released its first high power RF CMOS switch using high-resistivity silicon substrates sourced at a leading silicon foundry. RFMD(R) is leveraging this new process technology, as well as patent-pending design and circuit-related technology developed by RFMD, to introduce a product portfolio of high-performance silicon switch-based products for next-generation 3G and 4G smartphones, as well as other cellular handset, wireless infrastructure, wireless local area network (WLAN), CATV/ broadband and aerospace and defense applications.

Eric Creviston, president of RFMD's Cellular Products Group (CPG), said, "RFMD's CMOS-based cellular switches deliver meaningful performance, size and cost benefits, including excellent linearity and isolation capabilities, which are critical to today's multi-band 3G handsets. We are forecasting significant customer adoption in calendar 2010 driven by leading 3G smartphone manufacturers."

Bob Bruggeworth, president and CEO of RFMD, added, "For RFMD, these new CMOS-based products - and our entire Switch and Signal Conditioning product portfolio - highlight the increasing dollar content opportunities available to RFMD and the continued success of our diversification efforts. Equally important, our CMOS-based switch portfolio enables further improvement in our return on invested capital (ROIC) as we migrate technologies and IP developed by CPG into the markets served by RFMD's multi-market products group (MPG)."

RFMD's CMOS-based cellular switches meet or exceed the stringent linearity and isolation requirements of next-generation 3G and 4G smartphones while providing superior ESD performance (HBM data rated at 2000V). Also, by integrating the controller and RF switch on the same circuit, RFMD's patent-pending circuit-related technology and the innovative high-resistivity CMOS technology reduce product size while improving product performance. Accordingly, RFMD's silicon switches deliver a lower cost and higher performance 3G solution than is obtainable from competing silicon process technologies, including silicon-on-sapphire (SOS).

RFMD's first high power CMOS-based cellular switches include the RF1603, a single-pole, three-throw (SP3T) switch, and the RF1604, a single-pole four throw (SP4T) switch. RFMD has sampled both products to tier one customers, and commercial production is expected to commence in the first half of calendar 2010. Subsequent CMOS-based products will address increasing levels of end-product complexity and will include RFMD's growing portfolio of switch filter modules and switch duplexer modules for 3G smartphones.

RFMD offers the mobile device industry's broadest and most innovative portfolio of radio frequency components, including cellular power amplifier modules, cellular transmit modules, cellular switch and filter modules, and front ends for Wi-Fi, WiMAX and GPS applications. RFMD's product portfolio is on display at the 2010 Mobile World Congress in Barcelona, Spain, February 15 to February 18.

[*Source: RF Micro Devices*]

EUROSOI ANNOUNCEMENTS

EUROSOI2010 Tutorials on the web

The tutorials of the Workshop held in Grenoble this past January are now available in the tutorials section of the EUROSOI website.

In this section, besides these last tutorials, the previous ones can also be found. They are organized according to their dates and places and a search engine by years has been also developed. For further details take a look at:

http://www.eurosoi.org/tutorials.asp

NEWS

Skyworks Introduces Family of GaAs and SOI Antenna Switch Modules for 2/3/4G Wireless Broadband and Mobile Handset Applications

These compact solutions deliver state-of-the-art technology to meet both high performance and low-cost architectures, depending upon the interface requirements.

[…] "These solutions highlight the breadth and depth of our technology [...]" said Skyworks' senior director of engineering.

Skyworks Solutions, Inc., an innovator of high reliability analog and mixed signal semiconductors enabling a broad range of end markets, announced that it has introduced a family of antenna switch modules (ASMs) for 2/3/4G handset and data card platforms using both gallium arsenide (GaAs) as well as silicon on insulator (SOI) technologies. Skyworks products address the three primary switching functions: main antenna, diversity, and band/mode.

These compact solutions deliver state-of-the-art technology to meet both high performance and low-cost architectures, depending upon the interface requirements. By delivering a comprehensive RF switch portfolio based on both technologies, Skyworks is able to augment its already broad portfolio of world-class switches currently used in the company's front-end modules.

"Skyworks is pleased to be supporting such a broad range of next-generation wireless broadband and mobile handset applications with our new family of antenna switch modules," said Dr. Gene A. Tkachenko, Skyworks' senior director of engineering. "These solutions highlight the breadth and depth of our technology as we look to best serve our customers' needs on multiple fronts and with highly integrated architectures."

About Skyworks' 4G GaAs pHEMT and SOI Antenna Switch Modules

- The SKY13362 is a single-pole ten-throw (SP10T) ASM with an integrated complementary metal oxide semiconductor (CMOS) decoder and dual low pass harmonic filters. The small 3.0 x 3.8 mm switch has five 3/4G transmit-receive (TRx) ports, three receive (Rx) ports, and two global system for mobile communications (GSM) transmit signal low-pass harmonic filters that make it the flexible choice for multiple combinations of 2/3/4G multimode cellular applications. Using advanced switch technologies, the ASM maintains low insertion loss and high isolation on both transmit, transmit-receive and receive switching paths. Additionally, the switch was designed to meet or exceed system requirements for 2nd and 3rd harmonics into an antenna mismatch up to 5:1, while delivering linearity (excellent triple beat ratio), and second and third order (IP2, IP3) intermodulation distortion performance to provide manufacturers with sufficient margin in the certification process.
- The SKY14152 is a low-cost, single-pole eight-throw (SP8T) ASM for use in multimode embedded data cards. The compact 3.2 x 3.2 mm device is designed for universal mobile telecommunications system (UMTS), code division multiple access (CDMA2000), enhanced data for GSM evolution (EDGE), and GSM applications and supports flexibility with up to five 3/4G TRx bands. The device consists of an SP8T switch, GSM transmit signal low-pass harmonic filters, and a RX SAW filter.
- The SKY14153 is a low-cost, single-pole four-throw (SP4T) switch designed for wideband code division multiple access (WCDMA) and diversity switching applications that demand high linearity and low-insertion loss. The compact 2.0 x 2.0 mm switch is optimized for third generation partnership project (3GPP) 3/4G bands from 0.70 to 2.7 gigahertz (GHz).
- The SKY14155 is a low cost, double-pole four-throw (DP4T) switch designed for broadband, 3/4G band switching applications which demand low insertion loss, high isolation, and high linearity. The compact 2.0 x 2.0 mm switch is manufactured using a state-of-the-art SOI process, and is optimized for 3G WCDMA mode/band switching applications.
- The SKY18106 is a SP8T ASM designed for multimode, high power switching applications that demand low harmonics and insertion loss. The 3.2 x 4 mm switch is optimized for both 2G GSM/EDGE and 3G WCDMA applications and supports up to six 3/4G TRx ports with very low insertion loss, high isolation and excellent linearity under antenna mismatch conditions.

The newly introduced switch, ASM and FEM devices rely on state-of-the-art pseudomorphic high electron mobility transistor (pHEMT), SOI, integrated passive device (IPD), and wafer-level chip-scale package (WL-CSP) SAW technologies. No external blocking capacitors are required on any of the RF ports for all of these devices - thus minimizing customers' bill of materials and occupied board space.

[*Source: Skyworks*]

ANNOUNCEMENT

Korean International Summer School on Nanoelectronics

The Korean International Summer School on Nanoelectronics is a new annual event, starting in 2010. Nano-KISS will offer every year a panel of detailed lectures on emerging fields in nano-micro-electronics, given by world-class experts. The first edition in 2010 is dedicated to advanced SOI concepts and technologies. It is a unique opportunity for senior and junior researchers to update their knowledge in the rapidly growing field of SOI components. Nano-KISS will bring together scientists from all over the world universities, R&D centers and companies. Nano-KISS is based on the successful model of MIGAS, the international Summer School on Microeletronics, organized for many years in Grenoble area. Nano-KISS is organized by Kyungpook National University (KNU) and Grenoble Insitute of Technology (NPG) via World-Class University and Brain Korea 21 projects.

Pyeongsan Academy, located in the famous Palgong provincial park, is avery attractive place for combining top level lectures with scientific interactions and recreacional activities.

2010 Scientific Programme

• *Introduction to SOI devices and applications*

-Why SOI? -Prof. J.P. Colinge (Tyndall Ireland)

-Benefit for processors, low-power CMOS, RF, and high temperature applications - Prof. J.P. Colinge (Tyndall, Ireland)

-SOI Device Zoo - Prof. J.P. Colinge (Tyndall, Ireland)

-Technology Modules for SOI - Dr. D.W. Kim (Samsung, Korea)

• *SOI materials*

-Standard Smart-Cut and beyond (ETSOI, GeOI, alter BOX, etc) - Dr. Carlos Mazure (CTO SOITEC)

• *Physics of SOI transistors*

-Mechanisms in partially depleted, fully depleted and multiple gate MOSFETs - Dr. T. Ernst (LETI, France)

-Advanced modeling and simulation - Dr. T. Ernst (LETI, France)

• *Electrical characterization and reliability*

-Characterization techniques for SOI materials and transistors - Prof. Sorin Cristoloveanu (INPG & KNU)

-Reliability and variability issues - Prof. R. Schrimpf (Vanderbilt Univ. USA)

• *Designing SOI circuits*

-Circuit design for SOI - Dr. R. Ferrant (France)

• *From Micro to Nano*

-Ultimate CMOS scaling and More-than-Moore devices - Prof. Alex Zaslavsky (Brown Univ. USA)

• *Applications*

-MEMS, NEMS, sensors - Prof. S. H. Kong (KNU, Korea)

-SOI floating-body memories - Dr. S. W. Chung (Hynix, Korea)

REMEMBER:

***SemOI Conference* begins 26th April and notifications to authors were done in February**

ANNOUNCEMENT

Starting engines for EUROSOI2011

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be held at Granada, Andalucía (Spain). It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

As a first step the Workshop website is now available at

http://granada2011.eurosoi.org

ANNOUNCEMENT

6th International SemOI Conference and 1st Ukrainian-French Seminar

The second announcement for the 6th International SemOI Conference and 1st Ukrainian-French Seminar to be held from 26th-30th April 2010 in Kyiv (Ukraine) has been launched.

The goal of the Conference is to debate about the recent developments in nanometer down scaled Semiconductor-on-Insulator (SemOI) Systems which are basis blocks for modern high-sensitive sensors in a wide range of applications such as telecommunications, radiation control,, boimedical instrumentation, Chemicals análisis, etc.

SemOI is foreseen as a key technology for the integration of high quality and ressintant nanoscaled devices and integrated circuits which must operate in harsh environment.

The topics to be covered include:

-SOI material technology.

-Nanoscale CMOS devices and circuits.

-New SemOI materials and nanoscaled devices on its basis

-SemOI sensors and new SemOI Systems.

NEWS

CPV Consortium Elects New Board Members with Exceptional Solar Industry Backgrounds

"Their insight from Fraunhofer, the DOE and NREL will broaden the perspective of the organization, and hopefully facilitate the benefits that public and private cooperation can bring to an emerging technology at a critical time for CPV commercialization."

The CPV Consortium, a non-profit concentrator photovoltaic (CPV) solar industry organization, announced the addition of two respected solar industry veterans to its board: Andreas Bett, PhD and Martha Symko-Davies, PhD. The appointments come at a time when the Consortium has commissioned the University of California, Berkeley to undertake an economic analysis of the CPV carbon footprint, cradle-to-cradle.

The CPV Consortium is dedicated to supporting the development and optimizing the success of CPV technology as a mainstream energy source for distributed and utility-scale deployments. It is a global organization comprised of members from all segments of the CPV industry including system manufacturers, cell suppliers, power generators, tracker suppliers, system integrators, project developers, universities and research laboratories.

Dr. Bett is a deputy director of the Fraunhofer Institute for Solar Energy ISE, where he leads a department focused on materials for solar cells and technology. Dr. Symko-Davies is a senior supervisor of research at the National Renewable Energy Laboratory (NREL). Both have been elected by the members of the CPV Consortium to serve on the board of directors. "With the appointments of Drs. Bett and Symko-Davies, the CPV Consortium gains decades of expertise from the highest levels of solar industry research and development," said Nancy Hartsoch, director of the CPV Consortium. "Their insight from Fraunhofer, the DOE and NREL will broaden the perspective of the organization, and hopefully facilitate the benefits that public and private cooperation can bring to an emerging technology at a critical time for CPV commercialization."

Dr. Bett is one of the most respected CPV experts in the world. His Fraunhofer department includes the group "III-V-epitaxy and solar cells," which is one of the largest and most esteemed groups active in research and development for CPV cells, modules and components. He is also an active member in the IEC which develops standards for CPV. Bett is currently the chair and main organizer of the 6th International Conference on Concentrating Photovoltaics, which will be held in April 2010 in Freiburg, Germany.

Dr. Symko-Davies has worked for NREL since she received her doctorate in 1997. Symko-Davies is currently the manager of the PV Technology Incubator, a position she has maintained since its inception three years ago. While at NREL, she has held a variety of positions including photovoltaic (PV) manufacturing technology technical manager and high performance PV project manager. Symko-Davies is also an IEEE PVSC organizing committee member and APS member. She has authored and co-authored over 30 publications about the PV industry, and CPV technology throughout her career.

[*Source: Business Wire*]

NEWS

Concentrix Solar enters the US market with megawatt CPV deployment at a Chevron facility

"It is an important reference for our technology, [...] considering the outstanding performance demonstrated at our Spanish power plants," said Concentrix Solar CEO, Hansjörg Lerchenmüller."

Concentrix Solar, a leading supplier of Concentrator Photovoltaic (CPV) systems and a new division of the Soitec Group (Euronext Paris), the world's leading supplier of engineered substrates, announced that it has signed a contract with Chevron Technology Ventures for the deployment of a one megawatt (MW) CPV power plant to be installed at a Chevron Mining facility in Questa, New Mexico, USA. With this announcement, Concentrix Solar confirms full commercial readiness for worldwide deployment, and is paving the way to utility-scale CPV projects. Chevron announced this week that the company will install a one megawatt CPV solar power plant using Concentrix Solar's FLATCON® technology. This will be the largest CPV installation in the U.S. and one of the largest CPV power plants in the world. The power produced will be sold through a power purchase agreement to the Kit Carson Electric Cooperative, Chevron stated in their press release (February 23, 2010).

"This commercial deployment is a key milestone for us and our U.S. strategy. It is an important reference for our technology, and the next logical step considering the outstanding performance demonstrated at our Spanish power plants," said Concentrix Solar CEO, Hansjörg Lerchenmüller. "With their high direct normal irradiance and their high energy demand, the Southwestern states of the USA are perfectly suited for our CPV technology. Our FLATCON® technology's high-precision, two-axis tracking system helps utilities to match U.S. peak power demands. We are excited to prove our technology with Chevron on the Questa site and are planning new investments to further expand our business in the Southwest of the USA in the near future." [*Source: Soitec*]

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EURO-SOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

CALENDAR

- Semicon China
Shanghai, China.
March 16th - 18th, 2010

- Korean International Summer School on Nanoelectronics
Daegu, Korea.
April 7th - 10th, 2010

- 217 ECS Meeting
Vancouver, Canada.
April 25th - 30th, 2010

- 6th International SemOI Conference and 1st Ukrainian-French Seminar
Kyiv, Ukraine.
April 26th - 30th, 2010

- International Symposium on Circuits and Systems. ISCAS 2010
Paris, France.
May 30th - 2nd, 2010

- ESSDERC ESSCRIC 2010
Sevilla, Spain.
September 13th - 17th, 2010

- 218 ECS Meeting
Las Vegas, USA.
October 10th - 15th, 2010

- EUROSOI 2011 Workshop
Granada, Spain.
January, 2011

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XXI APRIL 2010

IN THIS NUMBER:

HIGHLIGHT FEATURE

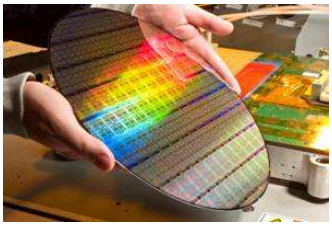
The Time is Right for SOI Technology Adoption

Susan Runowickz-Smith
Cadence Design Systems

The time for Silicon-on-Insulator (SOI) technology has finally arrived. As process technology shrinks, the power density of chips is climbing. Alternate technology approaches are going to be needed to address this challenge. Mike Muller, , ARM CTO, at the March 25 EE Times "Designing with ARM" virtual conference postulated: given the same power budget used for the 45 nm design today, if an 11 nm design has 16X the transistors running at 0.6X the power, "I can actually use only 10 percent of them in my new design," Muller said. "The rest is dark silicon. We need to find ways of lighting that silicon up."

Fortunately, as Muller postulated, SOI technology is an obvious contender to meet the power density test. For seven process generations, SOI has been quietly serving high-performance applications such as enterprise servers, networking and storage systems, and game consoles delivering on challenging speed requirements consuming up to 40% less power than bulk silicon technology. With scores of SOI based products deployed in the marketplace, SOI is a time-tested technology with proven custom and digital design flows. In addition, a growing base of IP is becoming available for a new set of consumer product applications such as digital TV, high-performance mobile internet devices, printers, and ultralow-power applications such as wristwatches and automotive applications. In addition, SOI's favorable radiation-tolerant characteristics have been recognized by companies such as Boeing for extraterrestrial semiconductor applications.

So, what makes SOI process deliver this superior performance/power profile? Bulk technologies start with a single-crystal silicon substrate, the SOI starting material has an embedded oxide layer just below the silicon surface. The significance is a reduction in leakage current and power/performance advantages over devices designed and built in bulk wafers.



Internal studies at IBM have compared 45 nm SOI-based circuits to the same circuits in 45 nm bulk silicon showing yield 30% performance benefit using transistors of comparable leakage. For designs not requiring higher performance, the SOI advantage can be turned into a lower-power design point. Additional IBM studies indicate lower soft error rates are intrinsic to SOI technology, with a 5–7× improvement over bulk. Furthermore, SOI-based devices generally have better temperature sensitivity so that they can be operated at high temperatures and latch up does not exist because device isolation prevents parasitic bipolar device formation between FETs.

Last week the SOI Industry Consortium announced the launch of its "Ready for SOI Technology" program, a global initiative to broaden access to energy-efficient silicon-on-insulator (SOI) technology for the electronics industry. Recognizing that SOI technology has not reached its full potential in the marketplace, a core group of SOI Industry Consortium (SOIC) members: ARM, Cadence and IBM came together to address some of the perceived obstacles to wider adoption of SOI process technology. In 2008, GSA and SOIC conducted a survey identifying EDA tools, IP and education as barriers to adoption of this promising technology. Today, these issues are being addressed via the SOIC's aggressive program aimed building a broad and complete ecosystem for SOI design. At launch of the program, ChipEstimate.com fielded a web portal dedicated exclusively to SOI IP and boasting more than fifty IP elements from IBM, ARM, Cadence, Boeing and Synopsys. The rich set of IP available from IBM, has been silicon proven within its ASIC technology offering and is now available to foundry customers as well. In addition, designers can take advantage of IBM's SOI foundry offering with embedded DRAM. IBM's SOI technology with eDRAM is a key enabler for multi-core processors and other integrated circuits and can result in improved systems performance and energy savings for a range of applications including networking, printer, storage, consumer and mobile products. Today the ChipEstimate.com/soi portal can enable designers to evaluate SOI process technology against other technologies for their next design.

[*Source: Chipestimate.com*]

NEWS

IBM, ARM and Cadence act to make SOI chips cost-effective

IBM is working with ARM and Cadence to remove one of the biggest barriers to more widespread adoption of silicon-on-insulator (SOI) semiconductor process technology. SOI is known to have definite power and performance advantages over commonly used bulk CMOS process technology. But its mainstream adoption has been slow because of higher cost and a lack of process proven silicon intellectual property (IP).

Collaboration between IBM, ARM and Cadence, as part of the wider SOI Industry Consortium, will make semiconductor IP blocks proven on the IBM SOI process, such as memory, IO and power management, available for licensing. ARM has provided 18 IP blocks including memory compilers, IO libraries and power management functions. IBM's embedded DRAM IP is also included. The intention that the 50 IP block available at launch of the programme will be added two by further IP blocks from across the industry. Boeing and Synopsys are the next companies to provide IP to the programme.

According to Horacio Mendez, executive director of the SOI Industry, the aim of the IP library is to remove one of three barriers to what he called "mainstream adoption of SOI in the consumer and mobile phone markets". Another obstacle has been access to SOI process technology, but according to Mendez, this has been addressed with foundries such as IBM, Globalfoundries and Chartered offering services. The other main obstacle to adoption is the higher cost of the SOI process compared to equivalent bulk CMOS processes. "As we are seeing the complexity of bulk CMOS process increasing to match performance and power budgets we are seeing the cost of SOI falling," said Mendez.

According to a spokeswoman from IBM Microelectronics, there are already SOI devices in consumer products such as games consoles. "That gives us a data point about how the price differential is changing," said. "It is possible that there could be price parity between SOI and bulk CMOS within a few generations," said Mendez. But this is not likely to be the current 45nm generation where Mendez predicted the cost differential will be in "single digits". ARM offered its first physical IP libraries for IBM 45nm SOI process more than a year ago. These included standard cell, memory and I/O libraries for IBM's fully enabled 45nm SOI foundry. This IP is now commercially available.

[*Source: ElectronicsWeekly*]

"It is possible that there could be price parity between SOI and bulk CMOS within a few generations," said Mendez.

NEWS

Education to reduce barriers to SOI adoption

The SOI Industry Consortium has launched the 'Ready for SOI Technology' program to stimulate adoption of energy-efficient silicon-on-insulator (SOI) technology. A cornerstone of the program is education.

Initiated by IBM, ARM and Cadence, the 'Ready for SOI Technology' program aims to provide chip and system designers access to SOI design intellectual property (IP) and make this IP available through a SOI portal hosted on the ChipEstimate.com website.

And, to enable the formation of a complete ecosystem that enables designers to take full advantage of the benefits of SOI technology, IBM, ARM and Cadence decided to deliver educational tools such as trainings and seminars.

A survey conducted by the Global Semiconductor Alliance (GSA) and the SOI Consortium in 2008 highlighted the need for more SOI education and awareness. A question indeed asked what the biggest reason was for not evaluation or using SOI today, and the top reason cited was the perceived additional cost of SOI, followed by lack of design knowledge and then risk and IP availability.

This survey proved that education is key to reducing barriers to adoption, confirmed the need for a group dedicated to SOI to provide the knowledge and expertise needed to inform the industry and debunk present misconceptions.

"Making sure that we educate people is precisely what we are trying to do," stated Horacio Mendez, executive director of the SOI Industry Consortium. "Education is a broad perspective. We are trying to educate designers on how to design with SOI but also on how they can access the IP and the advantages of SOI."

[*Source: EETimes*]

[…] "We are trying to educate designers on how to design with SOI but also on how they can access the IP and the advantages of SOI." said Méndez.

NEWS

ARM CTO warns of dark silicon

ARM Moore's Law keeps marching relentlessly forward, thanks to engineers conjuring up increasingly clever tricks to push back against the laws of physics. According to ARM, in the last seven years mobile phones have shown a 50X improvement in talk-time per gram of battery, while at the same time taking on new computational tasks that only recently appeared on desktop computers, such as 3D graphics, audio/video, internet access, and gaming. Now you can use your Blackberry to watch streaming video from YouTube or play interactive online games while pretending to check your email.

Still, there's trouble in paradise. This Thursday, ARM's CTO Mike Muller will deliver the keynote address at EE Times' Designing with ARM virtual conference. According to Mike, despite process scaling down to 11 nm, fixed power budgets may soon make it impossible to utilize all the available transistors on a chip. Without fresh innovations, designers could find themselves at some point in an era of "dark silicon," able to build dense devices they cannot afford to power.

Muller makes his argument with the following numbers: Compared to a 45-nm die, 22 nm will enable a 4X die shrink; 11 nm, 16X. Again taking 45 nm as the reference point, the peak frequency at 22 nm can increase 1.6X and at 11 nm, 2.4X. All well and good. However, while power consumption may remain constant at 22 nm vs. 45 nm, at 11 nm it drops to 0.6. All this means that at a 45-nm power budget, at 22 nm only 25% of the silicon is exploitable and only 10% is usable at 11 nm. Clearly this isn't an acceptable trend line.

In his keynote Mike will detail both tactics and strategies for lighting up what would otherwise be "dark silicon." Silicon on insulator (SoI) will play a big role—the first ARM-based 22-nm test SoI chips taped out last October; SoI goes a long way toward addressing the leakage problem at smaller geometries. Energy-efficient and robust high-density memories will facilitate reduced operating and retention voltages. 3D silicon integration (3D ICs) will enable high levels of energy efficiency and performance improvements.

Other recommendations and predictions: Muller sees Neon++ as the future of vector processing, improving single-threaded performance and extending Neon's reach to new application domains. Stream programming on the GPU—using the OpenCL programming model—makes possible high-throughput computations on floating-point intensive applications. Mike sees MP++ as "the future of multi-core scalability" and in his talk goes into some of the architectural implications and scalable coherence techniques. He will also discuss the evolution of the SoC interconnect and some of the ins and outs of sub- and near-threshold circuit design.

On the strategy side Muller explains a new approach to dynamic voltage scaling, referred to as Razor, which is based on dynamic detection and correction of speed path failures in digital designs. The key idea of Razor is to tune the supply voltage by monitoring the error rate during operation. Muller proposes a combination of circuit and architectural techniques for low-cost, in-situ error detection and correction of delay failures. [*Source: Embedded.com*]

ANNOUNCEMENT

Extended deadline for ESSDERC-ESSCIRC 2010

The final extended deadline for ESSDERC and ESSCRIC 2010 is April 18th.

These conferences will take place in Sevilla (SPAIN) from September 13th to September 17th, 2010

The two conferences have been running together for several years and they provide an excellent annual forum for the presentation and discussion of most recent advances in solid-state devices and circuits both from industry and from academia. In 2010, the two conferences will have a common schedule and will share Plenary Keynotes Presentations, Joint Sessions, Tutorials on September 13th and Workshops on September 17th. Besides taking benefit from a thoroughly selected Technical Program and having a place to networking and interacting with peers from worldwide, conference attendees will have the opportunity of enjoying the not-to-miss city of Sevilla. With more than 3000 years of splendorous history, Sevilla is a modern european city with very well-kept, outstanding historical remaining from the Roman Empire, the Muslim Kingdoms and the Spanish Empire, nice climate and friendly, hospitable people.

REMEMBER:

Submission deadline for ESSDERC and ESSCIRC 2010 is April 18th

EUROSOI ANNOUNCEMENT

Looking ahead: EUROSOI2011

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be held at Granada, Andalucía (Spain). It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

As a first step the Workshop website is now available at

http://granada2011.eurosoi.org

FEATURE

Are you ready for Silicon-on-Insulator technology?

By Clive Maxfield

Silicon-on-Insulator (SOI) refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing to reduce parasitic device capacitance and thereby improve performance.

SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide or (less commonly) sapphire. The choice of insulator depends largely on intended application, with sapphire being used for radiation-sensitive applications and silicon dioxide preferred for improved performance and diminished short channel effects in microelectronics devices.

In order to bring us all up to speed, the SOI Industry Consortium is launching a "Ready for SOI Technology" program, a global initiative to broaden access to energy-efficient silicon-on-insulator (SOI) technology for the electronics industry. With this program an initial offering of SOI intellectual property has been provided by IBM, ARM, and Cadence Design Systems. More IP has been added by Boeing and Synopsys, with an invitation extended to other developers to add to the growing SOI IP ecosystem.

SOI process technology can provide up to 30 percent chip performance improvement and 40 percent power reduction compared to bulk silicon technology. SOI is widely used today in market leading products found in data centers, offices, vehicles, homes and elsewhere in applications for computing, storage and networking, as well as for graphics-intensive game consoles. The Ready for SOI program is now making necessary design building blocks available to a broader population of chip designers seeking to harness SOI technology's benefits for new applications, including mobile and consumer products.

A key enabler for this effort is the new SOI Portal hosted on the popular ChipEstimate.com site at www.ChipEstimate.com/SOI. The SOI Portal provides chip designers access to available design building blocks and to the companies supporting chip development on SOI processes.

"ChipEstimate.com has become a critical resource to over 26,000 registered SoC designers by providing central access to over 200 of the world's largest IP suppliers and foundries," said Adam Traidman, General Manager at Cadence. "Our new SOI micro-site will serve as an invaluable resource to designers wishing to explore the benefits of SOI technology for their chip design projects."

To help IP and chip designers transition to SOI, the Ready for SOI program is sponsoring SOI Jump Start Training. This special training event will be hosted by Cadence on April 28, 2010 at the Cadence Engineering Center Auditorium, in San Jose, CA. Jump Start Training will also be available as both a live and recorded webcast.

[*Source: TechBites*]

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NEWS

Soitec supplying SOI substrates to CSMC for display and other applications

Soitec The Soitec Group,the world's leading supplier of engineered substrates for the microelectronics industry, announced that the company has entered into an agreement to supply silicon-on-insulator (SOI) substrates to CSMC Technologies Corporation ("CSMC"), a leading pure-play specialty analog foundry based in China. Soitec is sampling SOI substrates for High Voltage (HV) and CMOS applications initially aimed at color plasma display panel (PDP) driver integrated circuits (ICs) and other mixed signal and analog applications. The company is seeing high levels of interest and support in China for SOI projects. SOI is a cost-optimized technology increasing device performance and reliability, while lowering power consumption. These advantages are an excellent complement to consumer electronics markets, as well as continued expansion into worldwide markets for automotive, RF/wireless, high-voltage, power management, photonics, imaging, lighting and more.

"With this agreement, CSMC will use Soitec's wafers on several major SOI projects for High Voltage and CMOS technology. We believe the partnership with Soitec will help us to provide a more cost-effective solution to our customers," said Filian Wu, VP of Analog Process Technology Development Center."

As the world's leader in SOI substrates, we are very pleased to collaborate with CSMC and will support their plans to ramp up SOI based products," said Paul Boudre, Chief Operating Officer (COO) of the Soitec Group. "Over the last two years, we have experienced a strong acceleration of interest in SOI substrates in China mainly by the majority of the largest local foundries and institutes. Today these development projects are moving to first production ramp up and we expect a significant growth of SOI based products in China in the coming years." [*Source: Soitec*]

"With this agreement, [...] we believe the partnership with Soitec will help us to provide a more cost-effective solution to our customers," said Filian Wu

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

CALENDAR

- Korean International Summer School on Nanoelectronics
Daegu, Korea.
April 7th - 10th, 2010

- 217 ECS Meeting
Vancouver, Canada.
April 25th - 30th, 2010

- 6th International SemOI Conference and 1st Ukrainian-French Seminar
Kyiv, Ukraine.
April 26th - 30th, 2010

- International Symposium on Circuits and Systems. ISCAS 2010
Paris, France.
May 30th - 2nd, 2010

- ESSDERC ESSCRIC 2010
Sevilla, Spain.
September 13th - 17th, 2010

- 218 ECS Meeting
Las Vegas, USA.
October 10th - 15th, 2010

- EUROSOI 2011 Workshop
Granada, Spain.
January, 2011

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XXII

MAY 2010

IN THIS NUMBER:

HIGHLIGHT NEWS

IBM, Peregrine roll new Si-on-sapphire process

Seeking to gain more traction for its silicon-on-sapphire technology in RF designs, Peregrine Semiconductor Corp. has formed an exclusive joint development and foundry agreement with IBM Corp.

Fast-growing Peregrine (San Diego)--which is looking to file an initial public offering (IPO) in the next 12-to-15 months--has also altered its foundry strategy as part of the major announcement.

Prior to the announcement, Peregrine's foundry partners included MagnaChip, Oki/Rohm, Sapphicon and UMC. Now, fabless Peregrine has added IBM to the mix for its latest and greatest technology.

As part of the plan, IBM and Peregrine will jointly develop Peregrine's next-generation, silicon-on-sapphire technology, based on a 180-nm process on 200-mm wafers. Peregrine's technology, dubbed UltraCMOS, will be manufactured on a foundry basis within IBM's 200-mm fab in Burlington, Vt.

A form of silicon-on-insulator (SOI) technology, silicon-on-sapphire is formed by depositing a thin layer of silicon onto a sapphire wafer. This in turn creates an insulating sapphire substrate, which is said to have advantages over bulk silicon and gallium arsenide (GaAs) in RF applications.

Until now, Peregrine shipped devices based on 0.25-micron technology (and above) on 150-mm substrates. Peregrine refers to the new 180-nm silicon-on-sapphire process as its Step7 technology. The company claims Step7 produces devices that are 50 percent smaller with 100 times better linearity.

The technology is expected to propel a new class of RF devices, including high-power switches and tunable components, said Rodd Novak, chief marketing officer for Peregrine.

With the technology, it also hopes to enter the power amplifier business, thereby competing against Anadigics, RF Micro, Skyworks, TriQuint and others, Novak said.

"Our vision is to develop multimode power amps" on a single chip, based on silicon-on-sapphire technology, he added

The deal will also enable Peregrine to migrate to the 130- and 90-nm nodes. If it makes good on its promises, the company could become the next RF chip powerhouse

[*Source: EETimes*]

Peregrine's New SP5T RF Switch Offers High Isolation for Infrastructure Apps.

Peregrine Semiconductor Corporation announced the new PE42451 SP5T (single pole five throw) RF switch. The newest IC in the RF switch portfolio, designed on Peregrine's UltraCMOS' silicon-on-sapphire (SOS) process technology, delivers exceptional isolation of >50 dB, providing an ideal alternative to switch matrix designs in demanding applications such as communications infrastructure and point-to-point radios.

The HaRP'-enhanced 50-Ohm switch features five symmetric, absorptive RF ports. On-chip CMOS decode logic facilitates a three-pin low-voltage CMOS control interface and an optional external Vss feature (VssEXT). In wireless infrastructure applications, the SP5T design allows up to four power amplifiers to share a common Digital Pre-Distortion (DPD) feedback receiver path with an additional RF path for calibration, enabling a single, low-distortion, high-isolation switch to replace multiple SPDT switches.

'Wireless infrastructure equipment manufacturers no longer need to build costly SPDT-based switch matrices to achieve their high isolation switching needs,' said Mark Schrepferman, director of marketing for High-Performance Solutions business unit at Peregrine. 'Being able to reduce component count and cost is an ideal solution for today's high-performance infrastructure applications,' he added.

The new absorptive switch delivers market-leading RF performance across a frequency range of 450 MHz to 4 GHz: IIP3 of +58 dBm, IIP2 of +95 dBm, and Insertion Loss of 1.6 dB (450 MHz). The switch handles maximum +33 dBm input power (across the range) with world-class ESD tolerance of 3.5 kV HBM.

[*Source: CEN*]

NEWS

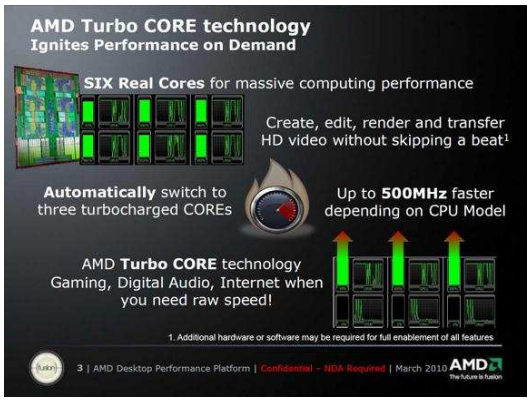
AMD's Turbo Core Technology

Instead of spending billions to create a new, advanced process at once (as Intel does) [...], AMD integrated new technologies into existing nodes.

The beauty of Intel's technology was the granularity of control.

While AMD will not be releasing their actual 6 core desktop processors for a few weeks yet, they did want to release a few teasers about one of the bigger features they are including in this chip. AMD has had 6 core server chips for some time now, but because these parts are significantly larger in terms of die size than the previous "Shanghai/Deneb" based quad core 45 nm parts they were not exactly predisposed for the desktop due to clockspeed and TDP issues. Not only are these parts larger, but all those extra transistors running at multiple GHz speeds increased the TDP of the 6 core parts as compared to the smaller quad core Phenom IIs and Opterons. Certainly AMD could have released 6 core parts shortly after the server introduction, but these would not have had the impact many were hoping due to their relatively low clockspeeds which would cause the chips to stumble when running single threaded or lightly threaded loads.

Istanbul is the code name for the server version of the 6 core processor, and it was a slightly tweaked version of the previous 45 nm quad cores. Not a huge amount of work was done on the architecture, but rather some simple optimizations which should increase performance to a very small degree, and perhaps more importantly work on the power and thermals of the part. The desktop version is now codenamed Thuban, and it is again slightly changed from the previous Istanbul in a number of ways. While clock for clock performance is the same, AMD has added a major new feature that is not available in the Istanbul based chip.



Power and Heat

Before diving into the Turbo Core feature, we need to take a look at what AMD has done to improve the thermals and power draw of their upcoming Thuban part. Current Istanbul parts are rated by ACP rather than TDP, but we can somewhat extrapolate TDPs. The top speed processor is 2.8 GHz and it looks to have a TDP of around 125 watts. When we consider that a year and some months ago, the top Phenom II X4 940 was running at 3.0 GHz with a TDP of 125, we can see that AMD has been working to get power draw down.

GLOBALFOUNDRIES (GF) manufactures all of AMD's processors right now, as it was previously the manufacturing arm of AMD. Now that it is spun off, we see that their overall process philosophy is basically unchanged when it comes to CPUs. AMD could not afford to do what Intel does with process tech, and so they had to take a "small steps" method to improving their lines. Instead of spending billions to create a new, advanced process at once (as Intel does) and leave it basically unchanged throughout its useful existence, AMD integrated new technologies into existing nodes. So when AMD would make a jump to a new process, it was not nearly as large in terms of thermals and transistor switching performance as compared to what Intel experienced. Those processes would however improve sometimes dramatically throughout its useful existence. GF is essentially keeping that method intact.

Thuban will stay in the 125 watt TDP range, even though it looks like we will see 3.0+ GHz speeds. GF apparently has included a new materials technology in the process line that it uses for Thuban. GF has been a leading manufacturer of SOI (Silicon on Insulator) in the industry, and they have relied upon that to minimize gate leakage. It seems as though GF has added another wrinkle to their 45 nm SOI process, and that is the further use of low-k dielectrics. This again adds to the efficacy of SOI by lowering leakage. It does not improve upon transistor switching performance though.

This is not a huge technological feat, as quite a few other processes around the world utilize low-k dielectrics. But this is another good example of how GF is able to inject new technologies into current process nodes to effectively keep up with Intel without spending the billions needed to develop a whole new process node from scratch. Also, GF does a lot of other work behind the scenes in terms of their process technology which again refines the node and allows for higher speeds and better thermals even on existing products. The improvements made by these process engineers have helped AMD to release their current quad cores in the revision C3 variant which now has a maximum clockspeed of 3.4 GHz all the while keeping in the 125 watt TDP envelope.

NEWS

AMD's Turbo Core Technology (cont.)

Turbo Core

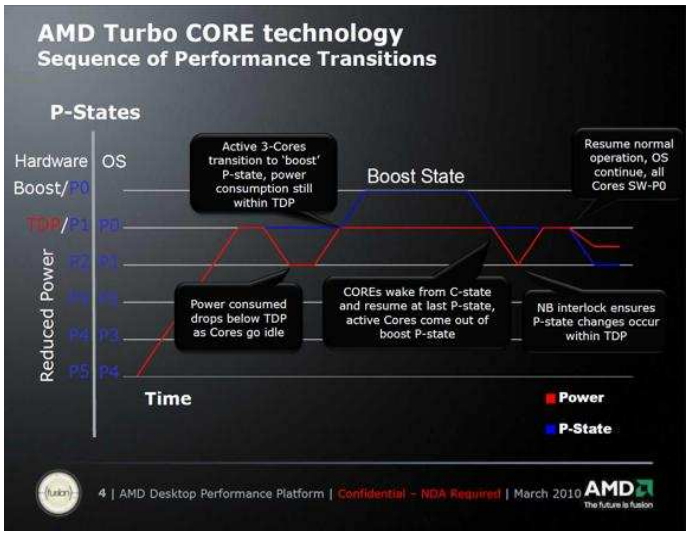
Intel released a turbo mode with their i7 processors, which dynamically adjusted the clockspeeds of the individual cores, as well as totally powered down unused cores. This was a very complex, but effective feature which maximized processor performance across a variety of usage scenarios. AMD is releasing something similar, but far simpler, with their upcoming Thuban based parts.

The beauty of Intel's technology was the granularity of control. If one core was being used, it would be clocked upwards quite a bit, while the other cores were shut down. If two cores were being used, those two would see a boost while the others were powered off. If all four cores were in use, but the top TDP was not being exceeded, then all four cores would receive a clockspeed boost.

Unfortunately for AMD, they did not have the time to integrate such a complex design into their chips, and instead have taken a rather simplistic approach to boosting clockspeed when all six cores are not in use. The processor is essentially divided into three parts. The uncore is clocked at its usual speed and does not change or power down. The six cores are essentially divided into two processor blocks of three a piece.

When the processor determines that three or less cores are being fully utilized, it will place the underutilized cores into a lower power, low clockspeed state. In this case the cores will be clocked at 800 MHz and will have their voltage decreased. The other three cores will be placed into a boost mode, with their clockspeeds increased as well as their voltages per core increased. AMD is designing these cores to be run between 400 MHz and 500 MHz faster. A theoretical six core clocked at 3.2 GHz would then see a boost of three cores up to 3.6 GHz.

[*Source: PCPerspective*]



REMEMBER:

2010 IEEE International SOI Conference submission of papers until June 4th

ANNOUNCEMENT

Starting engines for EUROSOI2011

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be held at Granada, Andalucía (Spain). It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

As a first step the Workshop website is now available at

http://granada2011.eurosoi.org

ANNOUNCEMENT

Submission of papers for the 2010 IEEE International SOI Conference extended

The 2010 IEEE International SOI Conference Committee has extended the deadline for submission of papers to be considered for presentation at the conference to be held in San Diego, California this October until **June 4th**.

This year's SOI conference will be highlighted by exciting plenary and invited talks. NASA JPL will discuss challenges in electronic design for interplanetary explorations. IBM will cover topics on SOI ASIC design, and FDSOI technologies; IMEC and Intel will discuss silicon photonics, ST Microelectronics will discuss RF applications while Tohoku University will discuss 3D integration. The SOI conference is the ideal forum to exchange and network. The SOI conference is an enriching forum where not only digital and power IC electronics is discussed but also expands discussion to wafer engineering and circuit transfer techniques opening up a spectrum of new applications like 3D, photonics, nanotechnologies and devices architectures beyond CMOS.

Catamaran Resort & Spa, San Diego.

NEWS

Cadence agrees to help IBM make IP for 32-nm SOI

"The IP we're working on [...] will allow [...] to build more powerful, higher bandwidth networking and communications technology."

Under the agreement, the companies will develop double data rate memory PHY cores, memory controllers, and protocols such as PCIe and Ethernet for use on 32-nanometer silicon-on-insulator manufacturing processes. The technology will be used in servers, video games and other devices.

"Qualifying and integrating complex IP is a costly and growing burden for many of our customers," said Vishal Kapoor, vice president of product management at Cadence, in a statement. "We look forward to teaming with IBM to relieve some of that burden for engineering teams as they grapple with SoCs and systems that will only continue to grow in size and complexity."

"The IP we're working on with Cadence will provide state-of-the-art building blocks that will allow our customers to build more powerful, higher bandwidth networking and communications technology," said Marie Angelopoulos, a director with IBM Microelectronics, in the same statement.

[*Source: EETimes*]

NEWS

MEMS Piezoresistive Low Pressure Sensing Die

This introduction of a new pressure sensor die marks the fifth major silicon pressure sensor die topology to be introduced over the past fifty years.

All Sensors Corporation announces the introduction of a low pressure sensor die for high volume applications requiring pressure measurement to as low as a quarter inch of water full scale. This introduction of a new pressure sensor die marks the fifth major silicon pressure sensor die topology to be introduced over the past fifty years.

Die Features

The MEMS Piezoresistive Low Pressure Sensing Die utilizes an open bridge configuration, measuring 2mm x 2mm square. Industry best sensitivity specifications are made possible by break though process technology in combination with innovative MEMS topology. The new die design features maximum pressure response while maintaining low package stress susceptibility. By utilizing a bossless structure the position sensitivity is minimized (typically 0.1% inH2O/g).

History

In the 1960's Bell Labs developed and Honeywell commercialized the first silicon pressure sensor using longitudinal and transverse strain sensitive resistors with square micromachined diaphragms. This design provided acceptable performance to as low as one psi.

In the 1970's Motorola introduced a shear strain silicon pressure sensor with performance targeted for automotive manifold absolute pressure (MAP) applications. These sensors incorporate shear strain sensitive resistors with square micromachined diaphragms with superior performance at 15 psia.

Also, in the 1970's several companies developed and commercialized silicon variable capacitance structures designed to detect either parallel plate changes in capacitance with pressure or changes in edge effect variable capacitance with changes in pressure. These sensors provided excellent response to pressures less than one inch of water. These sensors where either too large or too expensive for many applications.

In the 1980's several companies, most notably Silicon Microstructures, introduced longitudinal and transverse strain sensors with enhanced silicon microstructures to provide excellent pressure sensing to as low as several inches of water. Honeywell and others have been able to use this structure in conjunction with Honeywell patent 6,023,978 to extend the range to below an inch of water full scale.

[*Source: Design World*]

NEWS

Gefran launches dedicated website for IMPACT series melt pressure sensors

Gefran, the process control and industrial automation specialist has launched a new dedicated website for its IMPACT series high temperature fluid pressure transducers and transmitters. With product specifications and application information for plastics extrusion, injection moulding, blow forming and polymer production, the website covers the complete IMPACT range which is based on innovative MEMS technology to produce a fluid-free piezoresistive sensor capable of operation in high temperature environments of up to 350°C with exceptional durability.

Unlike conventional melt pressure sensors which use mercury or oil filling, the silicon on insulator (SOI) sensing element is suited to RohS compliant uses for medical and food industry plastics production, and as the process contact membrane can be up to 15 times thicker, a much improved resistance to dynamic pressures, increased resilience to abrasive materials and longer life is realised.

[*Source: Process and Control Today*]

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Mail: eurosoi@ugr.es

CALENDAR

- International Symposium on Circuits and Systems. ISCAS 2010
Paris, France.
May 30th - June 2nd, 2010

- Third International Workshop on Compact Thin-Film Transistor (TFT) Modeling for Circuit Simulation (C-TFT)
Tarragona, Spain.
July 2nd, 2010

- ESSDERC ESSCRIC 2010
Sevilla, Spain.
September 13th - 17th, 2010

- 2010 IEEE International SOI Conference
San Diego, California (USA)
October 11th-14th, 2010

- 218 ECS Meeting
Las Vegas, USA.
October 10th - 15th, 2010

- EUROSOI 2011 Workshop
Granada, Spain.
January, 2011

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XXIII JUNE 2010

IN THIS NUMBER:

HIGHLIGHT NEWS

Cadence Announces Comprehensive SOI Design Hub

Cadence Design Systems, Inc., the leader in global electronic design innovation, introduced the Cadence® SOI Design Hub, a new Web portal that lowers the barriers to adopting silicon-on-insulator (SOI) technology through comprehensive silicon-proven design enablement solutions and services. The SOI Design Hub is aimed at reducing SOI adoption start-up costs, cutting time to market for SOI intellectual property (IP), and improving design quality.

Cadence has been working with IBM, the leading SOI foundry, and with ARM to deliver methodologies, reference flows, IP access and services for SOI design. This includes the recent delivery of a 45-nanometer SOI SerDes receiver. Cadence also recently announced a joint development agreement with IBM to develop complex IP, including SOI designs, as part of the Cadence open integration platform. Forty-five-nanometer SOI technology offers up to 30 percent performance improvement or 40 percent power reduction when compared to the industry-standard bulk CMOS technology.

The Cadence open integration platform is a key component of the EDA360 vision, which, among other things, helps integrators close the profitability gap by providing new capabilities for IP creation, selection and integration.

"Cadence and IBM have collaborated for several SOI process generations to deliver silicon-proven methodology to our mutual customers," said Mark Ireland, vice president, Semiconductor Products and Services, IBM. "Providing this proven technology and Cadence services expertise is an excellent way to help customers in adopting SOI technology."

Through the SOI Design Hub, Cadence now offers three new solutions: An SOI IP porting service, where Cadence Services migrates analog, digital, and mixed-signal IP blocks to an SOI process technology, and delivers a self-contained macro that will integrate smoothly with the target design environment; turnkey design services, where customers can outsource any aspect of their design to the SOI design-experienced Cadence team; and a software-as-a-service (SaaS) offering with a complete do-it-yourself IP porting environment that provides access to a production-proven Cadence design environment within a secure IT infrastructure.

"As adoption of SOI technology continues to grow it is important to have a central point for accessing design enablement tools and IP to accelerate the design cycle and industry adoption," said John Heinlein, vice president of marketing, ARM, Physical IP division. "The Cadence SOI Design Hub, coupled with ARM physical and processor IP, provides engineers a silicon-proven route for leveraging this advanced technology to deliver high-performance, low-power consumer devices while reducing design risk and cost."

"We've been working diligently with IBM and ARM to make SOI adoption easier for our customers and enable them to benefit from this advanced technology," said Vishal Kapoor, vice president of product management at Cadence. "The new SOI Design Hub will help realize designs for those interested in leveraging the power and performance benefits of this technology with the solutions and services they need to ensure success."

"This innovative offering by Cadence provides a range of new options for companies to leverage the power efficiency and integration benefits of SOI technology in their products," said Horacio Mendez, executive director of the SOI Industry Consortium. "The SOI Design Hub is a significant addition to the SOI design chain for the electronics industry."

[*Source: Cadence*]

ANNOUNCEMENT

Coming up: EUROSOI 2011

Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be held at Granada, Andalucía (Spain) **from January 17th to January 19th.** It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

http://granada2011.eurosoi.org

NEWS

Startup proposes SOI JFETs for low power

SuVolta is "developing a variety of technologies and methodologies for significantly lowering semiconductor power consumption.", said Lewis.

SuVolta Inc. (Los Gatos, Calif.), a startup formerly known as DSM Solutions Inc., has revealed some details of the company's plan to achieve low power IC operation through the use of complementary junction FET technology.

Ashok Kapoor, CTO of SuVolta, made a presentation at the 2010 CMOS Emerging Technologies Workshop held in Whistler, British Columbia, May 19 to 21. In this case CMOS stands for communications, Microsystems, optoelectronics and sensors. Kapoor's presentation was variously entitled "VLSI with complementary JFET" and "JFET technology for very low power." The lateral junction FET differs from a MOSFET in that it uses a reverse-biased p-n junction to separate the gate from the body of the transistor, rather than an insulation layer. Also its channel doping is the same as the doping of its source and drain creating similarities in operation to proposed junction-less nanowire transistors.

Kapoor was part of the team of founders that formed DSM Solutions in 2005. The company has raised $25 million since then and taken on to its board of directors Bill Joy and Andy Rappaport to represent the interests of venture capital firms Kleiner Perkins Caufield & Byers and August Capital, respectively. SuVolta raised $3 million in December 2009, by which time the company had changed its name to SuVolta and Bruce McWilliams, former chairman, president and CEO of chip packaging company Tessera Technologies Inc. (San Jose, Calif.), had joined as CEO. The company has been granted a number of patents on the use of JFET technology for low-power logic, memory and signaling.

In his Whistler presentation Kapoor proposed the use of a double-gated JFET as it has a near-ideal sub-threshold swing. He gave measurements for NFET and PFET structures built with a 60-nm gate.

Kapoor also showed results for 99-stage ring oscillator built with complementary JFETs on bulk silicon. He also discussed the drawbacks of high p-well capacitance and the area penalty incurred to isolate transistors for JFETs implemented in bulk silicon. Kapoor's proposed solution is to build complementary JFETs on a silicon-on-insulator (SOI) substrate.

In his summary to the Whistler presentation Kapoor said: "Subsequently, functional logic circuits made with JFET on SOI have also been demonstrated." He concluded: "JFET operation has been simulated for channel length below 20-nm with reasonable Ion/Ioff ratio for voltage supply of 0.5V, making it a candidate for scaling to shorter dimensions."

Jeff Lewis, recently-appointed vice president of marketing and business development, said SuVolta is "developing a variety of technologies and methodologies for significantly lowering semiconductor power consumption." Lewis also told EE Times: "We are not going to make our own chips; instead we will make the technology available to others so they may include it in their own products."

[*Source: EETimes*]

NEWS

Kilopass Announces Embedded Logic NVM for SoCs

Gusto Delivers 4Mb One-Time-Programmable Ultra-Secure Storage for Consumer and Mobile applications .

Kilopass Technology Inc., a leading provider of semiconductor logic non-volatile memory (NVM) intellectual property (IP), announced **Gusto**, the industry's first and only 4 megabit (Mb) one-time programmable (OTP) NVM IP. Gusto is the only NVM IP large enough to store the firmware and boot code traditionally stored in external serial-flash and EEPROM chips. It is ideal for cost-, power- and form factor-sensitive applications, including mobile application processors and multimedia processors, as well as for high-security applications such as mobile banking and conditional access. Kilopass has successfully taped out Gusto 40nm test chips at three leading foundries – IBM, TSMC, and UMC. Initial silicon data is available now, and qualified proven silicon will be available later this year.

Gusto eliminates the limitations of traditional embedded NVM technology, including poor scalability to advanced processes and capacity limitations of less than 128Kb. Moreover, it does not require the complex manufacturing technology changes generally required by today's traditional embedded NVM. Instead, using standard CMOS manufacturing processes, Gusto scales to meet embedded NVM size and complexity challenges that grow exponentially as SoCs migrate to 40nm, and soon 28nm.

[*Source: ChipDesign*]

NEWS

TEGAL receives repeat order for TEGAL 4200 SE Cluster tool Silicon drie process module

Tegal Corporation, an innovator of specialized production solutions for the fabrication of advanced MEMS, power ICs and optoelectronic devices, announced it has received an order for an additional Tegal 4200 SE™ DRIE cluster tool process module from a leading EU-based supplier of MEMS and Power IC devices. The Tegal 4200 SE DRIE process module will be shipped and installed at the customer's site in the next fiscal quarter, and will add to the customer's overall production capacity for high volume manufacturing of MEMS and Power IC devices.

The Tegal 4200 SE cluster tool silicon DRIE process module order from this repeat Tegal DRIE customer follows the successful installation, process qualification, and sustained use of silicon Deep Reactive Ion Etch processes on the customer's first Tegal 4200 SE cluster tool PM.

"Our customer is known for their technological leadership in the MEMS and Power IC markets, and we see this repeat order as confirmation of the Tegal silicon DRIE tool's superior performance in high volume manufacturing," said Yannick Pilloux, DRIE Product Manager at Tegal Corporation. "We believe that our DRIE process modules are the most reliable and most advanced on the market and, as this repeat order shows, we have been able to meet our customer's demanding technical requirements for silicon DRIE cluster tools, while providing excellent value along the way."

The Tegal 4200 SE™ is an advanced, world-class cluster tool system dedicated to Deep Reactive Ion Etch applications. Featuring an inductively coupled plasma etch reactor and magnetic plasma confinement, the tool can run Tegal's patented SHARP – Super High Aspect Ratio Process, achieving etched feature aspect ratios of >100:1 in production environments. The Tegal 4200 cluster tool can be configured with up to 4 process modules, and 2 cassette modules, for High Volume Manufacturing applications for the most frequently used materials in MEMS and semiconductor device fabrication: Silicon (Si), Silicon On Insulator (SOI), and Silicon Dioxide (SiO2)

Tegal silicon DRIE tools are presently employed in numerous research and development laboratories throughout the world, engaging in both commercial and academic research programs, and are also found in MEMS foundries and other dedicated commercial High Volume Manufacturing lines world-wide.

[*Source: Tegal*]

NEWS

BroadPak joins SOI Industry Consortium

The SOI Industry Consortium, aimed at accelerating silicon-on-insulator (SOI) innovation across broad markets, announced that BroadPak has joined the worldwide organization. BroadPak is a premier provider of semiconductor package design and development services. The addition of BroadPak, with its unique silicon-package co-design methodology, expands opportunities for SOI chip developers to reduce product cost and improve chip and system performance without impacting chip development schedules.

"BroadPak brings its expertise in advanced high-performance, high pin-count package design and test to the SOI community," said Farhang Yazdani, president and chief technical officer of Broadpack.

[*Source: Soi Industry Consortium*]

REMEMBER:

Early registration deadline for ESSDERC ESSCIRC 2010 is July 28th

ANNOUNCEMENT

Finalizing details for ESSDERC / ESSCIRC 2010 in Sevilla

The 40th **European Solid-State Device Research Conference** (ESSDERC) and the 36th **European Solid-State Circuits Conference** (ESSCIRC) will be held in Sevilla on 13 - 17 September 2010.

The aim of the ESSDERC and the ESSCIRC conferences is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits.

ESSDERC and its sister conference ESSCIRC are governed by a single Steering Committee. The increasing level of integration for system-on-chip design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction among technologists, device experts, and circuit and system designers. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC will share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions.

Detail of the Cathedral in Sevilla.

NEWS

Freescale Extends QorIQ Family with Quad-Core P3 Platform Optimized for Low Power

The P3041 offers optimal integration and new intellectual property that delivers improved functionality for end products

Freescale Semiconductor is expanding the performance range of its QorIQ™ communications processor product lines with the introduction of the quad-core QorIQ P3 platform. The new P3041 processor offers an advanced feature set leveraging Freescale's P4 platform technology and optimized for low power, enabling increased system performance and improved overall power consumption.

The new QorIQ P3041 expands the reach of Freescale's P4 platform into lower power applications. Manufactured in 45nm silicon-on-insulator process technology, the P3041 offers optimal integration and new intellectual property that delivers improved functionality for end products. The P3041 processor integrates four e500mc cores based on Power Architecture® technology running up to 1.5 GHz at less than 12 watts, and delivers about 2.5 DMIPS/MHz. Key features include a three-level cache hierarchy for optimized latencies, a hardware hypervisor for robust support of multiple operating systems within the device, a trusted boot architecture to ensure code is not tampered with or reverse engineered, efficient data path handling, and improved Serial RapidIO and SATA IP.

[*Source: EDACafé*]

NEWS

IBM 'fab club' aligns 28-nm process, jabs rival

IBM's group has also come out of its shell and launched a subtle verbal attack on the rival foundry camp, reportedly Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC).

Four companies in IBM Corp.'s "fab club"--IBM, Samsung, GlobalFoundries and STMicroelectronics--said that they are in collaboration to "synchronize" the production of chips, based on its previously-announced, 28-nm low-power process.

The group will begin shipping 28-nm wafers starting by the later part of 2010. IBM's group has also come out of its shell and launched a subtle verbal attack on the rival foundry camp, reportedly Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC).

The group did not mention TSMC by name, but the Taiwan foundry giant has been critical of the high-k technology implemented by IBM's group. IBM's 28-nm process is based on a high-k/metal-gate scheme, built around a gate-first technology.

In contrast, TSMC uses the rival gate-last technology in its high-k technology. Members of IBM's fab club defended its technology, saying that it's superior over competitive offerings.

In any case, leading-edge foundries are rushing to bring their latest and greatest processes to the market--and for good reason: The IC market is hot and the outsourcing specialists hope to capitalize on the up cycle. Many of the foundries have also boosted their capital spending and launched marketing campaigns to gain mindshare.

At present, leading-edge foundries are shipping their 45-/40-nm processes, which do not include high-k and metal gates. All are gearing up to ramp their 32- and/or 28-nm processes, which brings the foundries into the high-k era.

In the foundry space, IBM's fab club, TSMC and UMC have separately announced 28-nm processes based on high-k. IBM's group and TSMC claim to be the leaders in the segment.

[*Source: EETimes*]

NEWS

SOI Industry Consortium confirms new board members

The SOI Industry Consortium, a not-for-profit organization aimed at accelerating innovation and adoption of energy-efficient silicon-on-insulator (SOI) technology across the electronics industry, announced new additions to its board of directors: Michael J. Cadigan, general manager, IBM Microelectronics Systems & Technology Group, as the new board chair; Simon Segars, executive vice president and general manager, Physical IP Division, ARM Ltd.; and Laurent Malier, chief executive officer of CEA-Leti, as its new treasurer.

[*Source: SOI Industry Consortium*]

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

CALENDAR

- International Symposium on Circuits and Systems. ISCAS 2010
Paris, France.
May 30th - June 2nd, 2010

- Third International Workshop on Compact Thin-Film Transistor (TFT) Modeling for Circuit Simulation (C-TFT)
Tarragona, Spain.
July 2nd, 2010

- ESSDERC ESSCRIC 2010
Sevilla, Spain.
September 13th - 17th, 2010

- 2010 IEEE International SOI Conference
San Diego, California (USA)
October 11th-14th, 2010

- 218 ECS Meeting
Las Vegas, USA.
October 10th - 15th, 2010

- EUROSOI 2011 Workshop
Granada, Spain.
January, 2011

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XXIV

JULY-AUGUST 2010

IN THIS NUMBER:

HIGHLIGHT NEWS

AMD's Opteron 4100s march into x64 price war

AMD The future is fusion

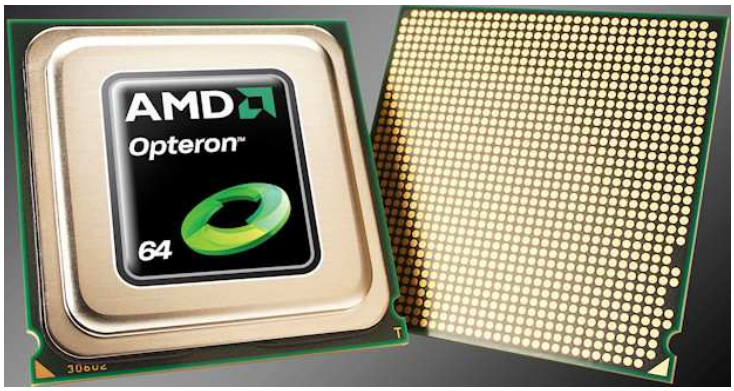
The big guns are already on the field in the x64 server processor war, and the troops are finally going all in with today's launch by Advanced Micro Devices of its entry "Lisbon" Opteron 4100s.

The Opteron 4100s are similar in many respects to the "Magny-Cours" Opteron 6100s that entered the battle against Intel's "Westmere-EP" Xeon 5600 and "Nehalem-EX" Xeon 7500 processors in March. Both chips are implemented in a 45 nanometer silicon on insulator process and manufactured by GlobalFoundries, the chip foundry that AMD spun out last year.

The Lisbon cores are quite similar to those used in the six-core "Istanbul" Opteron 2400 and 8400 processors from a year ago, with the transistor counts and processor areas being essentially the same, as are the cache memories. The big change is the shift from DDR2 to DDR3 memory for the integrated memory controllers. The Istanbul chips already supported HyperTransport 3 (HT3) point-to-point interconnect links, although the chipsets that the Istanbuls talked to did not. (They had a backwards compatibility mode).

The Magny-Cours chips, which come in variants with eight or twelve cores per socket, basically cram two Lisbon processors side-by-side in a single chip package and slap them into a new G34 socket that is serviced by AMD's own chipsets. The Lisbon chip comes with either four or six cores per socket on a single die. Both AMD processors have 64 KB of L1 data and 64 KB of L1 instruction cache per core, plus 512 KB of L2 cache per core. The Lisbon chip has 6 MB of L3 cache per processor package, and the Magny-Cours, being a double-stuffed socket, has 12 MB of L3 cache per socket.

The Opteron 6100s are aimed at



standard platforms that need lots of cores, clocks, and memory to support big databases or server virtualization hypervisors that in turn have lots of virtual machines running atop them. On these machines, raw performance and performance per watt are the two key metrics. Which is why AMD created the Opteron 6100s to support both two-socket and four-socket servers with the same chips and chipset.

Although, if you think about each physical chip as its own processor and look at the HyperTransport links coming into each socket, you could argue that what AMD has really done with the Opteron 6100s is crunch an eight-socket box into four sockets and a four-socket box into two-sockets.

This is a great strategy for customers who pay for their software based on socket count – and if you want to make a cheap four-socket box that can compete against Intel's more expensive Xeon 7500s. These latter chips from Intel have Itanium prices and scalability, but Xeon instruction set compatibility, and AMD figured that by crunching down the socket count on Opteron processors by a factor of two by doubling up the processors for the Opteron 6100s while at the same time creating an inexpensive, low-power server lineup for single- and dual-socket servers using the Opteron 4100s was the best way to undercut both the Xeon 5600s and the Xeon 7500s. The market will decide if this was indeed the right move.

What AMD has said this year, and what is no doubt true, is that it needs to get more market share in the server racket and it has to compete on price and performance to do that. However, it may just be that what many server customers want more than anything now is memory expandability within a 2P or 4P box, and the memory controllers inside the Opteron 4100 and Opteron 6100 processors can't address more than 512 GB, and a number of server OEMs, wanting to catch the server virtualization wave, have put two-socket and four-socket Xeon 7500 machines into the field that address 1 TB or more of memory.

[*Source: The Register*]

NEWS

Silicon-on-sapphire transducers

Silicon-on-sapphire technology is known for its superior accuracy and replaces solid state silicon and silicon-on-insulator technologies.

esi technology ltd

Ellison Sensors has expanded its range of pressure transducers and transmitters. Using silicon-on-sapphire sensor technology and the latest digital electronics, the new range of process pressure transmitters and transducers is one of the most advanced in the market.

The range is aimed at industries requiring process pressure measurement including requirements such as high temperature or those requiring sensors with higher levels of resolution and better long-term stability.

Silicon-on-sapphire technology is known for its superior accuracy and replaces solid state silicon and silicon-on-insulator technologies. The sapphire measuring diaphragm eliminates the insulation break down and the instability that is found in silicon pressure sensors, enabling the transmitter to operate at high temperatures. Sapphire is elastic with no measurable hysteresis, giving these transducers excellent repeatability.

The GS4200 USB digital pressure

transducer is powered from the USB port of a PC. Data is displayed on the PC and can be logged and recorded, making this an ideal solution for pressure measurement tests and requirements.

[*Source: SA Instrumentation & Control*]

NEWS

EDA Consolidation Continues

The consortium noted that the biggest upticks came in the categories of CAE, IC Physical Design, and semiconductor intellectual property (IP).

EDA CONSORTIUM

The EDA Consortium recently announced a second consecutive quarter of sequential revenue growth for overall electronic design automation (EDA) revenues. For Q4 2009, EDA industry revenues of $1.26 billion grew 8.1% over the quarter while declining 4.2% over the year. The consortium noted that the biggest upticks came in the categories of CAE, IC Physical Design, and semiconductor intellectual property (IP).

No wonder, then, that Sinopsis is continuing with its acquisition spree. The company recently acquired the intellectual property provider Virage Logic Corporation for nearly $315 million. Synopsys believes that high-quality IP will remain key for "enabling designers to reduce integration risk and speed time-to-market." It is hopeful that the Virage acquisition will broaden its portfolio and help it to address the market in providing a quick way to incorporate standard functions into their systems-on-chips (SOCs). Last fiscal year, Virage reported revenues of $47.4 million. I agree with Daniel Nenni that the acquisition will give Synopsys a near monopoly in the design enablement space and make it a bigger threat to competitors such as Cadence and Mentor, although not so much to ARM.

Synopsys also acquired high-level synthesis technology from Synfora, Inc. Synfora's technology enables designers to create and synthesize IC building blocks from a description written in the C or C++ programming languages.

Synopsys is looking to strengthen its position in system-level design and verification and to enhance its field-programmable gate arrays (FPGA)-based prototyping solutions through this acquisition.

Meanwhile, the company announced mediocre Q2 results. Revenues for the quarter were relatively flat at $338.1 million and EPS dipped to $0.41 from $0.45 a year ago.

Synopsys is also continuing to expand its existing product portfolio with products such as Yield Explorer *(continues on next page)*

NEWS

EDA Consolidation Continues (cont.)

which accelerates yield ramp by diagnosing yield issues during design for 90-nanometer and 40-nanometer design. Existing products are getting good reviews, and the company's Galaxy Design platform won the EDN Magazine Innovation Award.

The company projects revenues of $330 million–$338 million with EPS of $0.36–$0.38 for the current quarter. For the year, it projects revenues of $1.340 billion–$1.355 billion with EPS of $1.52–$1.62.

The stock is trading at $20.87 with a market capitalization of $3.09 billion. It touched a 52-week high of $23.74 in November of last year.

Synopsys' competitor, Cadente, also recently made a rather expensive acquisition. Cadence acquired Denali, a privately held leading provider of EDA software and intellectual property provider for $315 million. The transaction is expected to expand Cadence's solution portfolio to "deliver efficient and cost-effective system component modeling and IP integration."

Sanjay Srivastava, Denali's CEO, I believe owned most, if not all of the company, so he had a nice payday.

Cadence's Q1 revenues of $222 million were higher than the previous year's $206 million. During the quarter, the company earned $0.02 a share compared with $0.10 a year ago.

It too is expanding its product portfolio and launched a comprehensive silicon-on-insulator (SoI) Design Hub, a new Web portal that will help lower barriers to adoption of SoI technology by reducing initial start-up costs, reducing time to market for the SoI intellectual property, and improving design quality. I am hearing that some EDA players are trying to get into the SaaS model of delivering software, but don't know for sure if that initiative is coming from Cadence. It's possible.

The company projects revenues of $215 million–$225 million with a loss of $0.03–$0.05 a share in the current quarter. For the full year, it expects revenues of $865 million–$900 million with EPS of $0.05–$0.15.

The stock is trading at $5.79 with a market capitalization of $1.66 billion. In October of last year, it reached a 52-week high of $8.18.

[*Source: Sramana Mitra on Strategy*]

NEWS

EUROSOI 2011, starting engines

Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be held at Granada, Andalucía (Spain) **from January 17th to January 19th.**

It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

More information at

http://granada2011.eurosoi.org

REMEMBER:

Early registration deadline for ESSDERC ESSCIRC 2010 is July 28th

ANNOUNCEMENT

Finalizing details for ESSDERC / ESSCIRC 2010 in Sevilla

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FEATURE

ARM, Cadence Webinar: How SOI Impacts Timing and Signal Integrity

[...] "there are a few things you need to know about timing and signal-integrity análisis", according to an August 25 webinar presentation by ARM and Cadence.

By Richard Goering

You probably know that silicon-on-insulator (SOI) technology offers lower power and/or better performance than bulk CMOS, and that qualified IP libraries are available. But what's the impact on the digital design flow? Fairly minimal, but there are a few things you need to know about timing and signal-integrity analysis, according to an August 25 webinar presentation by ARM and Cadence.

Entitled "Are You Ready for Silicon On Insulator Design Process," the webinar was presented by Mike Jacobs, senior product manager at Cadence, and Remy Pottier, head of SOI marketing and business development at ARM. The webinar was the second in a series of Digital Implementation and Signoff webinars that will be rolling out over the next few weeks. I blogged separately about the first webinar, which covered on-chip variation and statistical timing analysis.

As Remy noted, ARM has IBM 45nm SOI physical IP libraries available today, and expects to roll out a 32nm library in the fourth quarter. He also pointed to the wide variety of third-party IP currently available at the Chipestimate.com SOI Portal. He believes that SOI is ideal for gaming, networking, and base station markets, and is increasingly attractive for mobile phone applications.

FEATURE

SOI the Holy Grail solution for addressing the power gap in advanced SoC designs?

"SOI may provide new avenues to enable efficient design that provides optimal power management", says the author

By Remy Pottier

According to some industry pundits Silicon on Insulator (SOI) technology clearly enables more power efficient SoC designs. But is this advanced manufacturing technology the Holy Grail solution for addressing the power gap between performance and battery life in advanced SoC designs?

What are the factors behind the power gap? Well, let's start with the obvious – design complexity. You don't have to look very far to see that consumer and embedded devices are becoming more intelligent and supporting the latest in robust features. From the iPad to home entertainment, advanced functionality is abundant in products that just a few years ago were one step above dummy terminals. In parallel, products are finding themselves risking extinction fueled by hybrid devices offering a myriad of applications that were once the secure domain of function specific device, i.e. GPS systems and the new iPhone or Droid.

However, these adding these rich features can come with a cost: power consumption. SOI may provide new avenues to enable efficient design that provides optimal power management.

But how do you start to incorporate SOI design advantages into your next design? That's where ARM, Cadence and partners as IBM, SOITEC, and the SOI Industry Consortium come into the picture. These companies began to actively start to work on reducing the barriers to entry of SOI technology by developing the design infrastructure critical to the fabless / foundry communities.

[*Source: ARM Community Blogs*]

EVENT

FDSOI Workshop in Japan

The University of Tokio, the SOI Consortium and Soitec are organizing a one day Workshop at the Komaba Research Campus of the University of Tokio on Saturday the 25th of September 2010 following the SSDM Conference focusing on the FDSOI ecosystem readiness.

This Workshop is co-organized by Dr. Ishimaru from Toshiba, Dr. Wakabayashi from Sony, Prof. Hiramoto from Tokio University, Dr. Mogami from Selene, Dr. Fukuma from the Semiconductor Industry Research Institute Japan, Dr. Mazure and Mrs. B.Y. Nguyen from Soitec, and Dr. Méndez from the SOI Consortium.

Planar FDSOI technology offers today performance gain at very low power consumption in addition to a Vt variability reduction by 50-60% compared to bula based processes. FDSOI technology enables low Vdd operation for logia and high density SRAM cells at sub-0.6V Vdd regime with excellent SNM and minimum cell size

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July 2nd, 2010

- ESSDERC ESSCRIC 2010
Sevilla, Spain.
September 13th-17th, 2010

- FDSOI Workshop
Tokio, Japan
September 25th, 2010

- 2010 IEEE International SOI Conference
San Diego, California (USA)
October 11th-14th, 2010

- 218 ECS Meeting
Las Vegas, Nevada (USA)
October 10th-15th, 2010

- EUROSOI 2011 Workshop
Granada, Spain
January 17th-19th, 2011

- CDE 2011
Palma de Mallorca, Spain
February 8th-11th, 2011

- Ultimate Integration on Silicon Conference (ULIS)
Cork, Ireland
March 14th-16th, 2011

- 219 ECS Meeting
Montreal (Canada)
May 1st-6th, 2011

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XXV

SEPTEMBER 2010

IN THIS NUMBER:

HIGHLIGHT NEWS

IBM claims fastest MPU

IBM Corp. said Wednesday (Sept. 1) that it will begin shipping Sept. 10 a new mainframe computer computer capable of 50 billion instructions per second, powered by 96 microprocessors with clock speeds up to 5.2 gigahertz.

IBM (Armonk, N.Y.) said the z196 processor is a four-core chip that contains 1.4 billion transistors on a 512-square millimeter surface. The chip was designed by IBM engineers in Poughkeepsie, N.Y., and was manufactured using IBM's 45-nm silicon-on-insulator process at the company's 300-mm fab in East Fishkill, N.Y., IBM said.

The mainframe processor makes use of IBM's embedded DRAM technology, which allows IBM to place dense DRAM caches, or components, on the same chips as high-speed microprocessors, resulting in improved performance, according to the company.

A spokesperson for IBM said the company was not disclosing any other z196 benchmark data at this time.

The new mainframe, the zEnterprise System, is the most powerful commercial IBM system ever, according to the company, capable of executing roughly 17,000 times more instructions per second than the most advanced system available in 1970, according to the company.

The z196 processor features new software to optimize performance of data-heavy workloads, including up to a 60 percent improvement in data intensive and Java workloads, according to IBM.

Last week, IBM engineers at the Hot Chips conference sketched out plans for a petaflops-class supercomputer built from as many as 64,000 Power7 processors.

The zEnterprise System offers 60 percent more capacity than its predecessor, the System z10, but uses about the same amount of electricity, IBM said. Energy efficiencies were achieved through advances in microprocessor design, 45-nm silicon technology, more efficient power conversion and distribution and advanced sensors and cooling control firmware that monitors and makes adjustments based on environmental factors such as temperature and humidity levels and air density, according to IBM.

[*Source: EETimes*]

Soitec announces Concentrix Solar joining the Transgreen Initiative

Soitec the world's leading supplier of silicon-on-insulator (SOI) and advanced solutions for the electronics and energy industries, announced that its Concentrix Solar division focusing on concentrator photovoltaic (CPV) systems, has joined the Transgreen Initiative. Transgreen was recently created within the context of the Mediterranean Solar Plan to stimulate the development of a Trans-Mediterranean electric power transmission network to respond to the significant expected needs for electricity exchange between the two sides of the Mediterranean. Concentrix Solar's CPV technology is designed for use by large-scale solar power plants in hot and arid regions. The systems are extremely efficient, modular, flexible and very well-suited to the needs and challenges of the Mediterranean region to produce low cost electricity.

"Transgreen is a perfect vector to support our activities in the Mediterranean area. We are looking forward to working with this ecosystem of companies and the countries of the Mediterranean region to demonstrate the value of CPV," said Concentrix Solar CEO, Hansjörg Lerchenmüller. "We have an opportunity to make a significant contribution to the region's energy needs for renewable energy sources and to export energy to European countries."

With 25 percent AC system efficiency, Concentrix Solar's CPV systems provide the highest efficiency of all solar technologies available. Especially at locations with extremely hot ambient temperatures, CPV systems perform better than conventional solar systems and therefore guarantee a high and constant power production throughout the day.

[*Source: Soitec*]

NEWS

Anatomy Of A (Better) Gaming Platform

The original design was on 90nm and then migrated to 65nm [...] The size and power reduction possible with a 45nm process changed that architecture.

At the 45nm node and on an SOI process the design can be implemented with a method to minimize leakage and standby current. .

Microsoft's third-generation Xbox360 engine uses a 45nm silicon on insulator (SOI) process—and a new architecture.

The original design was on 90nm and then migrated to 65nm. In both of these cases the fundamental architecture of the system remained the same—a CPU (central processing unit) chip, a GPU (graphics processing unit) chip, and memory management chip for the front-side bus (FSB) to the DRAM.

The size and power reduction possible with a 45nm process changed that architecture. With the ability to now integrate 347 million transistors on a single die, the new design is a single-chip CPU, GPU and FSB memory controller. The design features three CPU cores with L1 and L2 cache, a GPU core with GDDR3 memory interface, a video-out controller, a PCIe interface and a FSB manager. The chip is placed as part of a CPU module that includes a HSIO (high-speed input/output) interface to an EDRAM die.

Filling out the system is a South Bridge block that contains an interface to the system Flash, HDD, Optical Disk Drive, USB, IR Remote, and wireless 802.11n circuits. This architecture was chosen partly on the needs of the system and partly on the capability of the process. At the 45nm node and on an SOI process the design can be implemented with a method to minimize leakage and standby current. That allows Microsoft to bring these simultaneous high-power blocks onto a single monolithic die. The architecture includes system-level temperature sensors and control, as well as block-based power down. Using the capabilities of the SOI, the power down is implemented with multiple power domains.

The chip now has 6 PLLs that support a total of 12 clock domains. The design uses an adaptive power supply system (APS), which results in 8 power domains. These separate the memory, CPUs and GPUs into different power domains, as well as the I/Os and interface logic. In order to facilitate interconnection to these blocks, the design used C4 pads on a 35mm PC-PBGA with a 3-2-3 buildup of layers. This reconfiguration resulted in a total net power reduction of more than 60% from the original design and more than 50% reduction in silicon area.

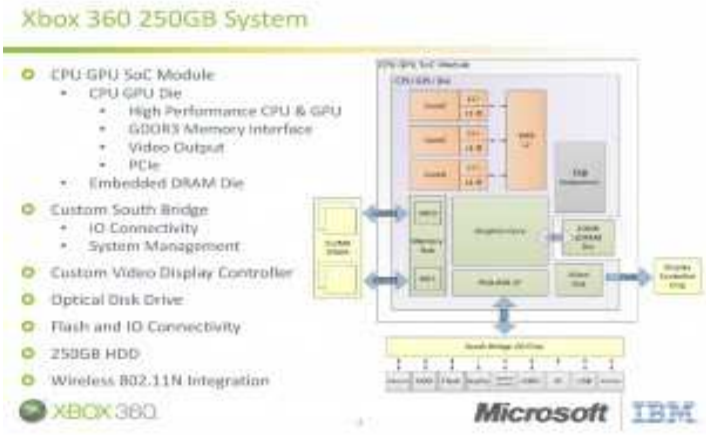
As the major blocks of the SoC came from different sources, the final chip was built using three different design methodologies. The CPUs were built using a semi-custom design methodology that supported synthesizable macros, full-custom macros, an 18-track, high-performance base library, a full independent clock grid and transistor-level timing analysis. The GPU area was build using an ASIC-style standard cell methodology—using a 12-track high-density (as opposed to high performance) base library, only synthesized macros, a combination of traditional H-Tree and full clock grid, and then finalized with gate level timing analysis.

The overall chip and the block infrastructure were built using a full-chip hierarchical methodology that called the CPUs and GPUs as "hard macros" in the top level of the design. The timing was performed hierarchically and partitioned along the blocks and paths. The hierarchical nature required a mix of device-level and gate-level verification of the signals based on their criticality. At this top level, the chip design for test was put in and pushed down hierarchically though the blocks including the hard macros for the CPUs and GPU.

The top-level logic verification had a challenge from the new architecture: It had to be backward-compatible to support the existing library of games and have no change in game play. As a result, the design used sequential equivalence to validate the design. This is comparing the corresponding sequential path outputs from the two different design representations and making sure they are the same in both performance and function.

The advanced process provides for loss of capabilities in a new SoC, but with dramatic changes in device architecture and the incorporation of multiple design flows and tools to complete the task.

[*Source: System Level Design*]



NEWS

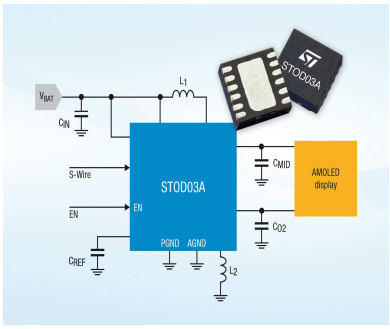
STMicroelectronics Powers High-End Mobile Internet and Video Experiences on AMOLED Displays

STMicroelectronics, a leader in power semiconductors, is powering the AMOLED and Super AMOLED displays that enable today's advanced handheld devices to deliver high-quality web and video experiences on the move, with a family of ICs consolidating all the display module's power requirements in a single chip.

AMOLED (Active-Matrix Organic LED) technology enables sharp and vibrant images for mobile multimedia devices such as 3G smartphones and digital-still cameras. These devices do not use backlighting and so offer key advantages over active-matrix LCDs, in terms of power saving and extremely low profile: typical thickness for AMOLED devices is now less than 1mm for the entire display module allowing stylish and space-efficient new designs. iSuppli has predicted annual shipments of phones with AMOLED displays will grow to more than 180 million by 2014.

ST is the major provider of power-supply ICs for AMOLED displays. Its latest STOD03A provides the needed positive and negative supply voltages from a single chip, and improves on the performance of the well established STOD02. Only six external components are needed to complete the power-supply circuitry. Alternative approaches require more components and use more power, making ST's solution the most attractive for handset builders.

The STOD03A uses highly efficient synchronous operation for both voltage outputs, achieving up to 85% overall efficiency for longer overall battery life. Other power-saving features include automatic pulse-skipping operation for low power consumption at light loads, and a true shutdown mode drawing less than one microamp activated through the enable pin (EN). ST has achieved its high performance using its Silicon-On-Insulator (SOI) technology as part of its latest-generation BCD fabrication process, which enables analog, digital and closely spaced high-power circuitry to be built on the same chip.



Compact, energy efficient AMOLED power chip increases battery life for super-slim 3G smartphones

IMPORTANT:

Abstract submission for EUROSOI 2011 will be opened soon.

ANNOUNCEMENT

Finalizing details for EUROSOI2011

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be held at Granada, Andalucía (Spain). It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

Training course and Key-Note talks will be announced in the following Newsletter (October issue)

Detailed information:

http://granada2011.eurosoi.org

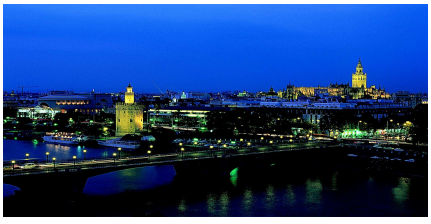
EVENT

ESSDERC / ESSCIRC 2010 in Sevilla

The 40th **European Solid-State Device Research Conference** (ESSDERC) and the 36th **European Solid-State Circuits Conference** (ESSCIRC) will be held in Sevilla this month (September 13th-17th)

The aim of the ESSDERC and the ESSCIRC conferences is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits.

ESSDERC and its sister conference ESSCIRC are governed by a single Steering Committee. The increasing level of integration for system-on-chip design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction among technologists, device experts, and circuit and system designers.



Views of the Cathedral and the Torre del Oro

NEWS

Safari lodge's concentrated photovoltaic plant could be precursor to 50-MW project

The 60-kW array consists of ten trackers and took about two weeks to install and commission.

South Africa's first concentrated photovoltaic (CPV) solar demonstration plant of 60 kW was operational in the Western Cape, and supplying the daytime power requirements for the Aquila safari lodge, near Touws River.

The plant was built by German solar engineering company Concentrix solar, which is a subsidiary of France-based technology company Soitec.

Besides powering the game reserve, the plant will become a training ground to develop solar skills in the area. Discussions are under way with the University of Cape Town's Energy Research Centre as to what kind of curriculum could be developed around the demonstration plant.

The 60-kW array consists of ten trackers and took about two weeks to install and commission. The technical installation was done by Johnson Controls.

Each tracker consists of a number of concentrator modules comprising high-performance multijunction cells with a Fresnel lens, as well as an inverter and a tracking system.

[*Source: Engineering News*]

NEWS

Soitec strengthens industrial operations team with the nomination of Francis Taroni

Soitec, the world's leading supplier of silicon-on-insulator (SOI) and advanced solutions for the electronics and energy industries, announced today that the company has appointed Francis Taroni to the position of Senior Vice President, Industrial Operations. In keeping with the group's continuing growth and expanding operations, Taroni will develop and implement the most appropriate industrial organization for the development of Soitec, which is renowned for its strong high-volume production capabilities.

A graduate of the Ecole Française de Radioélectricité, d'Electronique et d'Informatique, Francis Taroni (52) has worked in the semiconductor industry for his entire professional career. He began in 1982 at IBM, where his responsibilities included various management roles in France and the United States. More recently, Francis Taroni has successively held posts as Chief Technology Officer and Chief Operating Officer at Altis Semiconductor.

The appointment of Francis Taroni reflects the desire of Soitec to further strengthen its management team whilst the group pursues its development strategy in electronics as well as in the promising area of large-scale power supply.

"We are delighted to welcome a high class executive like Francis Taroni into our group. With his successful international background and his in-depth knowledge of the industry, he will bring the experience and vision we need to deploy our industrial strategy, supporting the demands of our clients and the growing needs of the market," said Paul Boudre, Soitec's Chief Operating Officer.

[*Source: Soitec*]

NEWS

Soitec confirms Q2 2010-2011 outlook

Following recent news flow from the semiconductor industry, Soitec (Euronext Paris) confirmed today that it expects almost stable consolidated sales as compared to first quarter sales at constant exchange (i.e. 1.27). A slight decrease in total wafer sales around two percent at constant exchange should be offset by other Group activities including Concentrix deliveries related to Chevron contract. Guidance for sequential total Group sales growth in H1 of around 20% is therefore confirmed.

Q2 sales for 2010-2011 will be published on 18th October 2010 after the close of the Paris Stock Exchange.

[*Source: Soitec*]

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EURO-SOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

CALENDAR

- ESSDERC ESSCRIC 2010
Sevilla, Spain.
September 13th-17th, 2010

- FDSOI Workshop
Tokio, Japan
September 25th, 2010

- 2010 IEEE International SOI Conference
San Diego, California (USA)
October 11th-14th, 2010

- 218 ECS Meeting
Las Vegas, Nevada (USA)
October 10th-15th, 2010

- EUROSOI 2011 Workshop
Granada, Spain
January 17th-19th, 2011

- CDE 2011
Palma de Mallorca, Spain
February 8th-11th, 2011

- Ultimate Integration on Silicon Conference (ULIS)
Cork, Ireland
March 14th-16th, 2011

- 219 ECS Meeting
Montreal (Canada)
May 1st-6th, 2011

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XXVI

OCTOBER 2010

IN THIS NUMBER:

HIGHLIGHT NEWS

CEA-Leti makes a R&D 20nm Fully Depleted SOI process available through CMP

CEA-Leti and CMP (Circuits Multi Projets®) announced during the FDSOI Workshop at Tokyo University the launch of an Exploratory MPW (Multi Project Wafers) initiative based on FDSOI (Fully Depleted SOI) 20nm process, opening the access of its 300mm infrastructure to the design community. This MPW offer is partly supported by EUROSOI+ network that gathers the main European academic partners on SOI.

"The Leti has pioneered the SOI technology for years, leading track records in the most advanced research in FDSOI, assessing its key advantages for low power high performance applications with several industrial customers" said Laurent Malier, CEO of the CEA-Leti. "It is time now to enlarge the diffusion of the FDSOI technology enabling test case on 20nm process and beyond. This hit will change the game, breaking the wall of technology to give an open access to the R&D international design community and a unique opportunity to touch Silicon with innovative designs."

"CMP is very proud to offer such a very advanced process to the community. Such a process will allow Researchers and Engineers to experiment the benefits of SOI on an advanced technology node" said Bernard Courtois, head of CMP.

CEA-Leti has been involved with FDSOI R&D for a number of years and has developed internally both an advanced High-K/Metal Gate FDSOI process and a number of specific design and simulation tools based on industry standard design flow packages. FDSOI technology presents key advantages over conventional bulk technology for future nodes. The electrostatic integrity of the transistors is ensured by the thinness of the body without the need for extra litho steps, like in the case of FinFETs, or of channel doping. The consequence is a planar technology that exhibits at the same time excellent short channel behaviour and significant improvement of the variability as shown in a number of recent papers.

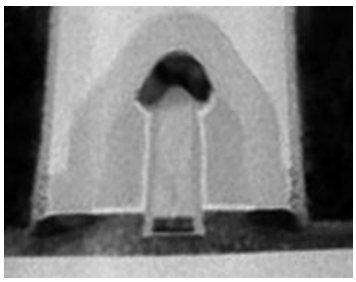
The basis of our technology offer will be the following:

•CMOS transistors with an undoped channel and a silicon film thickness of 6nm

•High-k / Metal Gate stack

•Single threshold voltage (Vth) n- and pMOSFET with balanced Vth of ±0.4V

•Associated Design Kit, including SPICE model (Verilog-A language), model cards extracted from silicon data, p-cells, DRC, LVS, schematic, parasitics



•Design Kit documentation

The first run is scheduled to be launched in September 2011. All details will be available on the CMP website.

[*Source: CEA-Leti*]

ANNOUNCEMENT

Registration opened for EUROSOI 2011

Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be held at Granada, Andalucía (Spain) **from January 17th to January 19th.** It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

Registration form is now available online at the Workshop web site. Early registration is possible before January 4th. Participants are also allowed to attend only to the Training course or to the Conference.

Special prices are offered for students.

All the information at:

http://granada2011.eurosoi.org

NEWS

Soitec announces global alliance with Johnson Controls to capture utility scale solar energy projects

The combination of the respective strengths of both companies [...] will provide an unbeatable force to accelerate and widen the successful installation of solar renewable energy utility scale plants.

Soitec Soitec, the world's leading supplier of silicon-on-insulator (SOI) and advanced solutions for the electronics and energy industries, announced that its Concentrix Solar division focusing on concentrator photovoltaic (CPV) systems, has concluded a global alliance with Johnson Controls (NYSE: JCI), the global leader in delivering products, services and solutions that increase energy efficiency in buildings.

Johnson Controls provides turnkey project development, engineering, procurement, construction, operation and maintenance of large scale energy efficiency and renewable energy projects. Under this collaboration, Johnson Controls and Concentrix Solar will identify and respond to commercial opportunities for the project development, and construction of utility scale solar energy facilities. Johnson Controls will build, operate, maintain and provide lifecycle support for solar installations using Concentrix CPV technology.

The combination of the respective strengths of both companies: efficient and cost effective technology on the one hand, and a worldwide leader in energy efficiency and sustainability on the other hand, will provide an unbeatable force to accelerate and widen the successful installation of solar renewable energy utility scale plants in Direct Normal Irradiation (DNI) regions across the globe.

"Before forming our alliance with Concentrix Solar, we studied all primary solar technologies and market participants. We concluded that the combination of Soitec's technical capabilities in engineered substrate solutions and Concentrix Solar's module design together provides the market leading solution for solar power generation in high DNI regions around the world," stated Iain Campbell VP & GM of Global Energy and Workplace Solutions, Johnson Controls.

"We are delighted to team up with Johnson Controls, who shares our vision for sustainable and economically viable, solar renewable energy," said André-Jacques Auberton-Hervé, chairman and CEO, Soitec. "Together, we understand the market opportunity and positive environmental impact that solar renewable energy power will bring to both existing and future facilities, and are excited to provide integrated solutions to our customers."

Concentrix Solar's cost effective and innovative CPV technology, with its high efficiencies and two-axis tracking, is ideally suited to areas in the world that have high direct solar irradiation.

Concentrix Solar will exhibit in booth #2701 at Solar Power International, October 12-14 in Los Angeles.

FEATURE

Planar fully depleted SOI: the technological solution against variability

F. Andrieu, O. Weber, J. Mazurier, O. Faynot
CEA-Leti

[FDSOI architecture] improves the variability of the electrical characteristics thanks to an undoped channel.

It is well known that the planar fully depleted silicon-on-insulator (SOI) (FDSOI) architecture is a technological booster of the CMOS performance, thanks to better electrostatics than devices on bulk. This article shows that it also greatly improves the variability of the electrical characteristics, thanks to an undoped channel. This leads to good matching performance.

This technology mainly addresses low-power applications, even if it is compatible with wafer-level or process-induced stressors for high performance. In particular, it yields a 22% energy-consumption reduction at a given speed for ring oscillators at the 45nm node compared to the same circuit on bulk. Finally, one of the main advantages of this technology is the low variability obtained.

The variability issue and solution

For the 20nm CMOS technology node and below, the variability of the electrical characteristics is becoming as important as the electrical performances themselves. Especially, the threshold-voltage (VT) variability is a key for the stability of the SRAMs, which represent a huge proportion of an integrated circuit area. Indeed, improving the VT variability directly lowers the SRAM dispersions and, in turn, the minimal supply voltage (VDDmin) of the memory blocks.

Historically, for CMOS on bulk, the dopant concentration in the

[*continues on page 4*]

NEWS

Training Course Programme and Key-Note talks of EUROSOI 2011

As in previous editions of EUROSOI Workshop, this international event covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and applications oriented engineers.

Typical topics include:

(1) Synthesis of advanced SOI wafers (Ge, SiGe and strained layers, SOI heterostructures)

(2) Materials evaluation, properties of ultra-thin films and buried oxides, defects and stress, interface quality

(3) SOI MOSFETs: characterization, modeling and simulation of typical mechanisms, parameter extraction, reliability issues

(4) Circuit design, process and applications: low power/voltage and RF circuits, innovative memories, high voltage devices, imagers, sensors, photovoltaics and MEMS

(5) More than Moore perspectives: multiple-gates, 3D stacks of devices and circuits, nanowires, NEMS, tunneling transistors, heterogeneous integration etc.

For 2011 edition to be held next January in Granada (Spain)., EUROSOI is trying its best and now putting the final touches.

Although there are still some details missing that will be announced soon, the final programme for the Training Course, Key-Note Talks and Workshop has been scheduled and is now available:

Monday, January 17th. Training Course. Tutorial.

• 9.15h-9.30h: Introduction and Tutorial Overview. *F. Gámiz (University of Granada)*

• 9.30h-10.30h: SOI solutions for next technological nodes. *Prof. Sigfried Mantl, FZJülich, Germany*

• 10.30h-11.30h: ETSOI Technology. *Dr. Bruce Doris, IBM, USA*

• 12.00h-13.00h: CMOS-SOI-MEMS Imagers. *Prof. Y. Nemirovsky, Technion, Israel*

• 15.00h-16.00h: SOI Low-power applications. *Dr. N. Sugii, LEAP, Japan*

• 16.00h-17.00h: Memories on SOI. *TBD*

• 17.30h-18.30h: SOI Photonics. *Dr. Jean Marc Fedeli, LETI, France*

• 20.00h-21.30h: Welcome Reception at Hotel Nazaries

Tuesday-Wednesday, January 18-19th. Workshop

Key-Note Talks.

• FDSOI Ecosystem. *Dr. Carlos Mazure, SOITEC, France*

• Monte Carlo transport of advanced SOI devices. How far can we go? *Prof. Max Fischetti, UTDallas, USA*

• Nanoelectronics: the point of view of EU Commission *TBD*

NEWS

Student Grants for EUROSOI 2011

To foster the participation of students to the Training Course and to EUROSOI 2011 Workshop, **EUROSOI will give 15 grants to Ph.D. students** which submit and defend a contribution to EUROSOI workshop.

The grant will consist on **the waiver of the registration fee (tutorial and Workshop) and the accommodation** (4 nights of hotel at Hotel Luna, Granada) from Sunday, January 16th to Thursday, January 20th, 2011. If you are a Ph.D student you can apply for these student grants when you submit your contribution.

EUROSOI 2011. IMPORTANT DATES:

• Dec. 1st, 2010: Deadline for abstract submission.

• Dec. 15th, 2010: Notification of acceptance.

• Dec. 31st, 2010: Deadline for advanced registration.

ANNOUNCEMENT

Abstract Submission for EUROSOI 2011

The submission period for EUROSOI 2011 is now open until December 1st.

In this edition an extended abstract must be submitted online through the Workshop web site

http://granada2011.eurosoi.org

using the available abstract template.

Abstracts exceeding the 2 pages limit will be rejected.

Following the Workshop, the committee will select the best contributions and offer their authors the opportunity to submit an extended version to Solid-State Electronics.

Students are strongly encouraged to send their contributions in order to be eligible for one of the appealing grants offered in this edition by the organization.

Authors will be notified of acceptance in mid-December

Detail of the Alhambra and the Palace of the Emperor Carlos V

FEATURE

Planar fully depleted SOI: the technological solution against variability (cont.)

Variability performance is much better for planar FDSOI than for planar bulk technology, for which variability is governed by random dopant fluctuation within the channel, and much than for FinFETs, for which the fin width fluctuation is the limiting parameter.

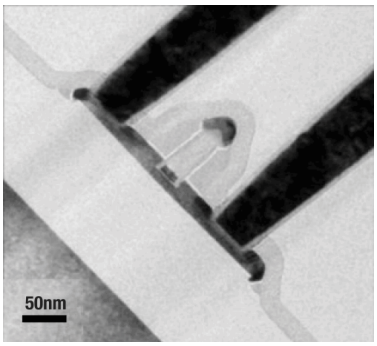


Fig.1. TEM image of a transistor on FDSOI with a Tbox=145nm thick Buried Oxide (BOX), L=30nm gate length and a mesa isolation.

channel of the transistors (Ndop) increases node after node (by a factor k) when the device dimensions (the active width W, the gate length L and the effective gate oxide thickness in the inversion regime Tinv) are scaled by a factor 1/k. This scaling law is only based on electrostatic considerations and not on variability considerations. However, for sub-65nm CMOS, one of the most important showstoppers is the VT variability, which is no longer negligible. Actually, the VT standard deviation varies as

$$\sigma_{V_T N_{dop}} \propto T_{inv} \cdot \frac{\sqrt[4]{N_{dop}}}{\sqrt{W.L}}$$

when it is limited by the random dopant fluctuation (RDF). This means that the intrinsic variability of CMOS on bulk theoretically degrades node after node (by a factor $k^{1/4}$). For the moment, the solution used by IC manufacturers to keep the VT standard deviation of the nominal device quite constant with the scaling is not to play on the channel doping but to slow down the (gate length L and supply voltage Vdd) scaling or to counterbalance by electrostatic improvements (Tinv lowering or junction optimizations) or by design solutions. However, for the 20nm node and below, considerations on the dynamic power consumption require a Vdd scaling and electrostatic/ performance considerations already require a challenging Tinv.

In this context, we propose another paradigm based on the planar FDSOI with undoped channels. In this architecture, the scaling is not governed by the channel doping but rather by the film thickness below the gate (Tsi). This enables an excellent electrostatic behavior (better than CMOS on bulk) without any intentional channel doping. Such devices thus resist the root cause

$$\sigma_{V_{T,L}} \propto \sigma_L \cdot \left(\frac{dV_T}{dL}\right)_{T_{inv},T_{Si},V_d}$$

of the RDF (i.e., the channel doping) and simultaneously improve the electrostatics. Indeed, FDSOI is really an electrostatic booster, similar to the Tinv reduction. This enables a lower sensibility of the VT vs. the gate length (L) and, consequently, an additional reduction of the second major source of variability in bulk devices, namely line edge roughness (LER). This latter indeed influences the VT standard deviation following:

(σL being the effective channel-length fluctuation). Finally, the two major sources of variability (RDF and LER) are strongly or even completely reduced thanks to the FDSOI architecture. This is evidenced by Fig. 2, which shows that the LER-induced fluctuation (in blue and red) can be neglected compared to the "surface" sources of variability attributed to the gate stack (charge or gate work-function fluctuations), even down to L= 25nm.

Variability performance of FDSOI devices

Thanks to the undoped channel, we highlight a low variability, as evidenced by Fig. 3. It exceeds the one obtained on bulk devices or on

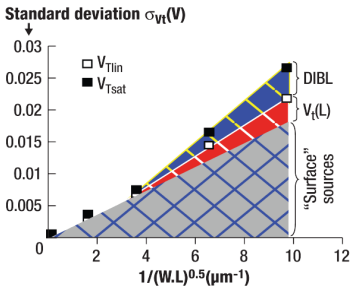


Fig. 2.Pelgrom plot with VT measured in the linear and in the saturation regime for TSi=8nm.

FinFETs (not shown here). Indeed, for 3D devices and, contrarily, as for planar FDSOI architectures, VT strongly depends on W. Thus, there is an additional contribution induced by the fluctuation of the fin width (Wfin), which is the smallest dimension of FinFETs:

$$\sigma_{V_T,W} \propto \sigma_{W_{fin}} \cdot \left(\frac{dV_T}{dW_{fin}}\right)_{T_{inv},T_{Si},V_d}$$

For planar FDSOI, however, SOI thickness (TSi) is the smallest dimension. However, Tsi is not defined by the lithography but rather by the Smart Cut process. This guaranties a very good process uniformity of Tsi. We demonstrated that the Tsi uniformity now reached by SOI wafer manufacturers (Tsi range around 10Å) is in the specifications for the 20nm node.

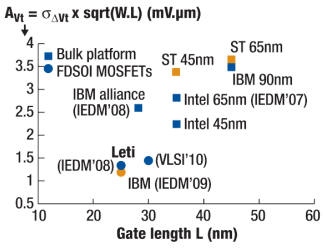


Fig.3. Benchmark of the matching factor vs. the gate length for bulk or FDSOI devices

[*Source: Solid State Technology*]

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THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XXVII NOVEMBER 2010

IN THIS NUMBER:

HIGHLIGHT FEATURE

Driving Light

Adele HARS
Advanced Substrate News

SOI is poised to take center stage in the impending lighting revolution, with companies like NXP leading the charge. Here's why.

Incandescent bulbs are being phased out or banned worldwide: European bans started taking effect in 2009; the US, Canada, Japan and Russia will start in 2012. India, Brazil, China and many more have all taken action.

Compact Fluorescent Lamps – CFLs – are poised to take the relay in the short term, followed later by LEDs (as they become more cost-competitive).

But consumers are in an uproar about the quality of most CFL lamps – and with good reasons: even though 4 billion a year are sold, they're usually too slow to get up to full brightness, they don't last as promised, they're expensive, the color's cold and unfriendly…and so the list goes on.

Lighting designers need chip solutions that solve these challenges without compromising time-to-market and cost. With SOI-based processes, lighting components leader NXP's got the answer.

But to understand these challenges, it helps to understand a few basics about CFL lighting technologies past, present and future.

INCANDESCENT VS. CFL BASICS

The meaning of "incandescent" is to produce light by heat. The modern incandescent light bulb, with its swirl of tungsten filament, has been doing that more or less unchanged in our homes for the last 100 years.

Electricity enters the bulb on a metal wire, comes up against the resistance of the tungsten (also a metal) filament, causing said filament to glow: ie. produce light. But it does this very inefficiently: only about 10% of the energy going in to an incandescent bulb comes out as light; most is dissipated as heat. The rule of thumb is that it takes an incandescent bulb one watt to produce around 15 lumens of light, so a 60-watt bulb produces about 900 lumens.

The fluorescent light – and its more recent incarnation, the CFL – works on a very different principle. Essentially, you have to get electrical current flowing through a tube containing mercury vapor and coated on the inside with a phosphor. The electrons around the mercury atoms get excited by the current, jumping into higher orbitals then dropping back, thereby releasing ultra-violet (UV) photons (which are invisible). These UV photons in turn excite the phosphor, which emits visible light photons.

With just one watt, a CFL can produce 50-70 lumens. So, to produce 1000 lumens takes the CFL as little as 20 watts.

It sounds straightforward, but when it comes to making light with electricity, gas has one very different characteristic from metal. Metal – the heart of incandescent lights – is by its very nature resistant. And the resistance in metal is very constant and predictable – affected only by the kind of metal, how thick it is, and temperature.

With gas, however, the more current you run through it, the more it loses its resistivity. If you were to just plug a fluorescent tube into the mains, the amount of current flowing through the gas would quickly climb and climb til the bulb – literally – blew out. So you have to control the current very carefully: this is where ballasts come in.

All fluorescent lamps must have ballasts at the ends of the tube, which get the current flowing through the gas and then control it. Old fluorescent lamps where not terribly good at this. They had a complex preheat system to ionize the gas in the tube and get the current flowing. But those old ballasts were based on electromagnetics (think: wire coils): the unsteady current produced those awful flickering, humming fluorescent lights of our childhood.

To make fluorescent bulbs that would fit into the same size light sockets as incandescents required a much smaller solution. Enter the electronic ballast: a little circuit board with independent passive and active components, including rectifiers, capacitors, switching transistors and inverters. They have to kick off with a very high-frequency jolt of electricity – about 40,000 Hz to ionize the mercury vapor – then settle right back to a normal operational levels (such as 50 Hz in Europe, 60 Hz in the US).

[*Source: Advanced Substrate News*]

NEWS

THINKING THIN: NXP'S EZ-HV-SOI

In high-power systems, it allows sophisticated control logic and high voltage drive circuits to be integrated into a single IC

First announced a decade ago, NXP's EZ-HV™ is process technology for the production of commercial high-voltage (HV) SOI-enabled ICs. It is at the heart of NXP's GreenChip technology, and is ideal for implementing optimal solutions for a wide range of lighting applications. In high-power systems, it allows sophisticated control logic and high voltage drive circuits to be integrated into a single IC (replacing the separate high and low voltage chips), halving the cost of the overall unit.

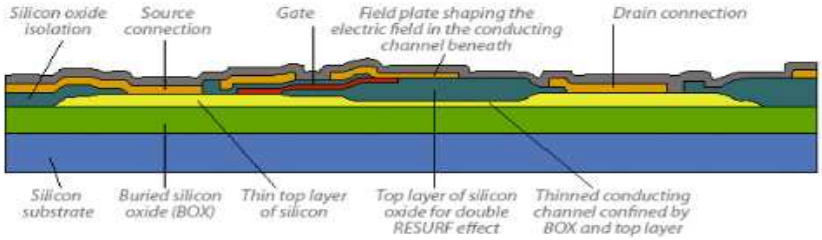
It represents a radical departure from "thick SOI" solutions, in which a 10 to 20 micron layer of silicon overlaying an insulating material limits the electric field strength to prevent a regenerative, killer effect called 'avalanche breakdown'.

Instead, the EZ-HV process uses SOI wafers with a relatively thin layer of top silicon (only 0.5 microns thick), which is much cheaper to produce. Even with 650 volts applied across this layer there is still insufficient distance between the upper and lower layers of the silicon for charge carriers to be accelerated to avalanche breakdown energy levels.

Other advantages include:

- lower cost
- higher integration density
- latch-up immunity, even with multiple power components on a single chip
- significantly reduced parasitic capacitance for far faster switching
- RDS(on) values halved enables handling of higher currents
- drift region fully depleted doubles effectiveness of RESURF, simplifying high-voltage design trade-offs

[Source: Advanced Substrate News]



Cross Section of EZ-HV LDMOS Structure: Producing this critical high-voltage component requires the use of only 13 mask steps, making the production of basic EZ-HV ICs cost-effective even for price sensitive applications

NEWS

Made in IBM Labs: New Chip Technology Paves the Way to a Faster Internet

IBM announced a new chip-making technology that can be used to create advanced semiconductors that can keep pace with the exploding number of internet-connected devices and the tidal wave of data they are generating.

The Cu-32 Custom Logic offering employs unique IBM technology -- designed by IBM Research -- to dramatically increase the memory capacity and processing speeds of chips used in fiber-optic and wireless networks, and in such gear as routers and switches. The technology can help manufacturers and network operators handle the data deluge driven by consumers' appetites for smart phones and other Web-connected devices.

Systems using chips made with Cu-32 for example, can result in:

- Cellular infrastructure that can move one year's worth of text messages (six trillion, worldwide in 2010) in less than ten seconds
- A consumer downloading a feature-length film on a smart phone in less than ten seconds; or a HD version in under a minute
- Routers that can stream every motion picture ever produced in less than one minute

The number of people using the internet has doubled in the past five years, with two billion logging-on in 2010. Manufacturers of communications infrastructure will increasingly need breakthrough semiconductor technologies such as Cu-32 to keep up with the demand to secure, store and move an ever-growing amount of web traffic.

[*Source: IBM*]

NEWS

Analyst: Intel to endorse SOI at 22-nm

For years, Intel Corp. has dismissed the need to use silicon-on-insulator (SOI) technology for its processors.

Instead, Intel has solved the power, leakage and mobility issues with high-k/metal gates, strained-silicon and other technologies. Intel's rival, Advanced Micro Devices Inc. (AMD), has been using SOI in its microprocessors for years.

According to an analyst, Intel will reverse its strategy and embrace SOI at the 22-nm. In recent months, Intel has tipped some (but not all) details of its 22-nm process. It has certainly not talked about SOI. The chip giant tends to dismiss it.

"We believe Intel will introduce a germanium (III V) channel and full depleted SOI at 22-nm. This will give Intel a quantum leap in performance over what they are achieving and leave competitors 3-5 years behind. The 22-nm process should be in manufacturing at Intel in Q4:CY11," said Gus Richard, an analyst with Piper Jaffray & Co., in a report.

'Intel's lithography roadmap is to use immersion double and multi- patterning at the 22-nm and 16-nm nodes," Richard said. "We note that Intel has consistently pushed lithography one generation further than any other manufacturer. What enables the company to do this in our view is the fact it is vertically integrated (design and manufacturing), has its own mask shop and uses restrictive design rules."

Then, Intel could make a switch. "At 11-nm in 2015, Intel's options are multi-beam e-beam, EUV and quintuple patterning with 193 immersions. It is questionable whether any of these alternatives will be economically viable," he said.

[*Source: EETimes*]

EUROSOI 2011. IMPORTANT DATES:

- **Dec. 1st, 2010: Deadline for abstract submission.**
- **Dec. 15th, 2010: Notification of acceptance.**
- **Dec. 31st, 2010: Deadline for advanced registration.**

CONFERENCE

Abstract Submission and student grants for EUROSOI 2011

The submission period for EUROSOI 2011 is now open until December 1st.

In this edition an extended abstract must be submitted online through the Workshop web site

http://granada2011.eurosoi.org

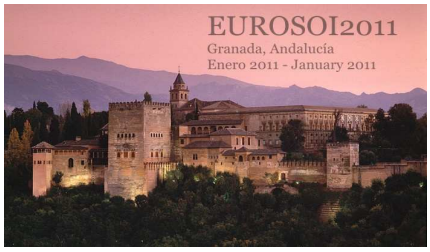
using the available abstract template.

Abstracts exceeding the 2 pages limit will be rejected.

Following the Workshop, the committee will select the best contributions and offer their authors the opportunity to submit an extended version to Solid-State Electronics.

Students are strongly encouraged to send their contributions in order to be eligible for one of the appealing grants offered in this edition by the organization. The grant will consist on **the waiver of the registration fee (tutorial and Workshop) and the accommodation** (4 nights of hotel at Hotel Luna, Granada) from Sunday, January 16th to Thursday, January 20th, 2011

Abstract authors will be notified of acceptance in mid-December.



View of the Alhambra and the Palace of Emperor

NEWS

NXP GreenChip Technology Enables Breakthrough Quality in Non-Dimmable CFLs

NXP Semiconductors N.V. announced the release of the UBA2211, a new generation of non-dimmable CFL driver ICs for 230V and 110V fluorescent lamps based on GreenChipTM technology. The UBA2211 offers a fully integrated CFL driver along with a current controlled preheat function, enabling more compact fluorescent lamp designs, highly efficient power conversion, and extended CFL lifetimes in the range of 12,000 to 15,000 hours. In addition, NXP announced today the availability of the UBA2024B, also based on GreenChip technology, its first CFL driver with integrated switches tailored for the 110V market.

[*Source: NXP*]

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

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Tempe, Arizona (USA)
October 3rd-6th, 2011

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XXVIII DECEMBER 2010

IN THIS NUMBER:

HIGHLIGHT NEWS

WILL FUTURE TRANSISTORS APPEAR IN GLORIOUS 3D?

Richard LEWINGTON

Imagine two micrographs side-by-side, one of a transistor from an Intel 286 microprocessor from 1982 and one of a transistor from the brains of the latest smartphone. While they appear quite similar, the new one is 100 times smaller.

But conventional transistor scaling is reaching its limits. Beyond the 22nm technology node – sometime in the middle of this decade – traditional two-dimensional, or planar, transistors may be a thing of the past. To continue the incredible advances in speed, battery life and cost, the technology must change. Two new approaches are being considered: three-dimensional transistors and enhancements to planar transistors.

I recently attended a forum that Applied Materials hosted in San Francisco where a panel of experts debated the relative merits of these approaches. Speaking to an audience of over 200 technologists, the panel included experts from leading chip companies: GlobalFoundries, IBM, Qualcomm, Samsung and STMicroelectronics and was moderated by Professor Yuan Taur from U.C. San Diego.

The most serious shortcoming of current planar transistors is leakage current, a major source of wasted battery power. The 3D approach splits the transistor gate into multiple parts (multi-gate), allowing more effective suppression of the leakage current. 3D transistors also tend to be taller and narrower than planar ones, allowing more transistors to be packed into the same area on the chip.

Panelists Witek Maszara, GlobalFoundries; Ghavam Shahidi, IBM; Thomas Skotnicki, STMicroelectronics and DK Sohn, Samsung (from left to right).

Witek Maszara, principal member of technical staff at GlobalFoundries, Inc. came out in favor of 3D technology. He believes that 3D transistors offer the lowest power density, key to giving mobile devices the endurance to match their performance. Ghavam Shahidi, Fellow in the Research Division at IBM Corp., agreed that 3D transistors are promising, but will be difficult to make in high-volume manufacturing and ultimately will also suffer leakage problems, limiting their long-term viability.

Going a step further, Thomas Skotnicki, Fellow and director of Advanced Devices at STMicroelectronics asserted that 3D transistors will never be the best choice for low power applications because the structure of 3D transistors prevents the use of "body bias" which can cut leakage in half during idle periods.

Instead, Shahidi and Skotnicki favor an enhanced planar transistor approach, which aims to overcome existing scaling bottlenecks while retaining the same basic physical arrangement. In this technique, a very thin channel of "fully-depleted," or pure, silicon is placed over a layer of insulating material – therefore called fully-depleted silicon-on-insulator (FD-SOI). By isolating the channel from the underlying silicon wafer in this way, leakage current can be greatly reduced and remarkable switching speeds achieved.

Dong Kyun Sohn, vice president in charge of the logic lab at Samsung Microelectronics' R&D Center said that his company is still evaluating both approaches. The winner, he said, must balance design restrictions, cost, performance and scalability to achieve the best overall performance.

Offering a different perspective, Geoffrey Yeap, vice president in charge of silicon technology at Qualcomm, Inc. pointed out that every part of a smartphone, the processor, the modem, the software etc., makes different tradeoffs to add up to the best overall user experience. The key to success for a fabless company such as Qualcomm is "holistic co-design" where they engage multiple steps up and down the value chain to deliver "More than Moore" performance.

[*Source: Applied Materials*]

[...] "This enables designers to reach the highest possible frequencies with a high confidence level."

NEWS

ARM TUNES SOI SPICE FOR PPA

Adele HARS
Advanced Substrate News

"SOI SPICE models that predict actual results with the greatest accuracy enable designers to fully exploit design trade-offs in terms of power, performance and area (PPA)," says ARM SOI guru Jean Luc Pelloie.

With that in mind, the ARM team presented a quiet paper at the last IEEE SOI Conference (Oct. 2010) – but one that has important implications for the industry. "Timing Verification of a 45nm SOI Standard Cell Library" is not yet available on the IEEEXplore site, but Jean Luc summarized the key points for Advanced Substrate News (ASN)

The take-away message: "It's important for the designers to have real and accurate timing data in order to avoid too much pessimism during the timing closure phase of circuit design. ARM's new measurement process correctly characterizes the history effect. This enables designers to reach the highest possible frequencies with a high confidence level."

The history effect is just another "corner". Since it's accurately accounted for in the physical IP libraries, it's pretty much transparent in the design flow, he explains.

[Source: Advanced Substrate News]

CONFERENCE

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CONFERENCE

Registration opened for EUROSOI 2011

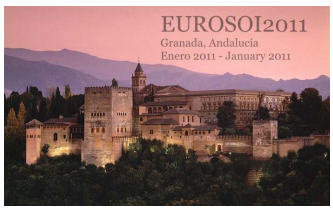
Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be held at Granada, Andalucía (Spain) **from January 17th to January 19th.** It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

Registration form is now available online at the Workshop web site. Early registration is possible before January 4th. Participants are also allowed to attend only to the Training course or to the Conference.

Special prices are offered for students.

All the information at:

http://granada2011.eurosoi.org



View of the Alhambra and the Palace of Emperor Charles V

FEATURE

RIGHT TIMING

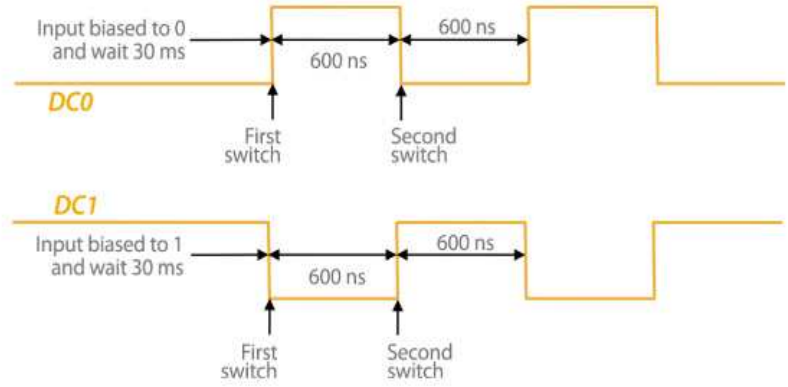
Jean-Luc PELLOIE
Director of SOI Technology, Fellow, ARM

SPICE models are used for checking the integrity of circuit designs and predicting circuit behavior prior to commiting a design to silicon. Each SPICE model is based on critical electrical response information that is specific to the fab that will produce the chips. SPICE models that predict actual results with the greatest accuracy enable designers to fully exploit design trade-offs in terms of power, performance and area (PPA).

ARM has recently developed new methodology(1) to validate the timing verification for SOI-based chips, and is currently working with foundry clients to tune their SPICE models accordingly.

To maximize accuracy, partially-depleted (PD) SOI timing verification must take into account the "history effect", wherein the body voltage of a transistor is a function of its recent on/off history. While early SOI adopters had to deal with this on their own, for today's designers the history effect is just another "corner" accounted for in the physical IP libraries, making it essentially transparent in the design flow.

We have done the work behind the scenes to ensure that both the foundries and fabless designers have models in which they can be completely confident.



Input signal testing first and second switch delays starting from DC0 or DC1.

IN THE LIBRARY

For standard cell libraries, ARM characterizes and incorporates timing verification in the library (.lib) files. SOI design requires two libraries per process-voltage-temperature (PVT) corner (whereas bulk silicon design uses one library per corner). For each function, a Max-SOI is characterized for the slowest operation possible, while a Min-SOI library is characterized for the fastest possible operation due to the history effect. The timing analysis tool uses these libraries.

However, it's important for the designers to have real and accurate timing data in order to avoid too much pessimism during the timing closure phase of circuit design. ARM's new measurement process correctly characterizes the history effect. This enables designers to reach the highest possible frequencies with a high confidence level.

ARM has developed and proven this reliable timing verification methodology on a 45nm SOI standard cell library. This methodology, which can be applied to any cell, also enables our foundry customers to fine tune their SPICE models, dissociating NMOS from PMOS (rise/fall transition). The same methodology is applied to the 32 and 22nm nodes.

[*Source: Advanced Substrate News*]

NEWS

Samsung predictions in IC scaling

As IC technology enters the sub-20-nm era, chip scaling will become even more difficult and expensive, thereby possibly requiring new materials, structures and processes, according to a technologist from Samsung Electronics Co. Ltd.

During a keynote at the International Electron Device Meeting (IEDM) here, Kinam Kim, president of Samsung Advanced Institute of Technology, said that the cost of IC scaling could force the industry to migrate to 3-D devices, based on through-silicon via (TSV) technology.

Memory technology will scale to the 1x-nm node, but the industry must also look at a new class of products that could replace existing DRAM and NAND, such as MRAM, phase-change and ReRAM, Kim said.

'The current 30-nm node silicon technology is meeting the demand for extremely low power, multifunctional chips that are able to maintain high performance to process and store huge amounts of heterogeneous data," Kim said. "However, there are concerns on whether the current silicon technology can satisfy the technical requirements and overcome the ultimate limits attached to transistors scale down."

[*Source: EETimes*]

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THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XXIX

JANUARY 2011

IN THIS NUMBER:

EDITORIAL

Francisco Gámiz
Professor
Univ. Granada (Spain)

Happy New SOI year!!

With the arrival of the new year, EUROSOI holds its annual meeting as every year. And it goes the seventh. The small "baby" who was born in Granada in January 2005, comes back again home, six year later, but with the same enthusiam, and much closer to the achievement of our goals. This last year there was plenty of good news for SOI community.

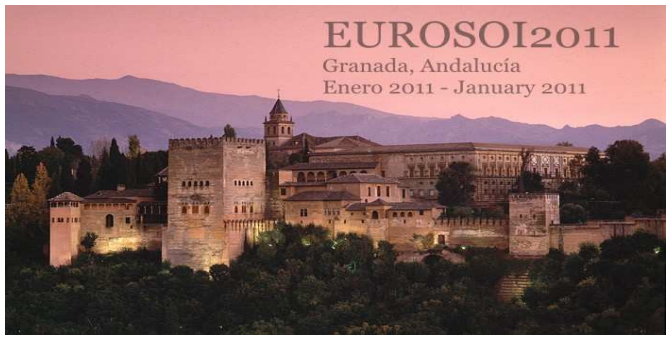
There are many fields where SOI technology shows all its potential to circumvent the problems found in bulk technology: i) Shrinking the conventional MOS transistor below the 22nm-node, ii) the continuous demanding for low power consumption in ubiquitous mobile applications, iii) new memory designs, iv) high-temperature and power electronics, and so on. The steady work of the SOI community is demonstrating everyday that this technology can gain a higher portion of the electronic market. However, researchers have to face new challenges. The combination of hard work, imagination and creativity will lead us to success.

At this point, EUROSOI initiative plays its main role: EUROSOI network was born as the meeting point where all these efforts should converge. Since its beginning in Granada (2005) and touring through Grenoble (2006), Leuven (2007), Cork (2008), Chalmers (2009) and Grenoble (2010), the workshop served as the ideal forum for inspiring discussions and to foster strong interactions among specialists in different fields.

Following previous experiences, we have prepared an informal, lively meeting with space for short presentations within a framework of larger discussion sessions. Relevant speakers have been invited to present the state-of-the-art in different fields of SOI. Dr. Carlos Mazure, from SOITEC, will open the conference describing the bright future of the FDSOI technology. Then Prof. Max Fischetti, from UTDallas, will take us as far as we can go. Prof. Carl Das, from IMEC, will introduce us in the Europractice network. Last, but not least, Mrs Gisele Roesems, from EU Commission, will talk about the future European research projects in the Nanoelectronics arena, formulating the strategy for the coming years. A Rump session chaired by Prof. Francis Balestra, from IMEP, promises to be an exciting brainstorming.

Before the Workshop, and following the tradition, we have organized an interesting training course. The lectures are given by six experts covering the areas from technology, memories, imagers, low-power and photonics. It will take place on Monday, January 17th. We would like to highlight the magnificent venue where the Workshop will be held. We are sure that the "Parque de las Ciencias" will create a warm atmosphere prone to the exchange of scientific and technical ideas.

[*Francisco Gámiz is Coordinator of the EUROSOI+ Network*]



CONFERENCE

EUROSOI 2011: great reception among participants

Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be held at Granada this month **from January 17th to January 19th.**

It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

A large numer of participants have been confirmed so far. All of them are welcome and invited to join us in what we expect to be a very pleasant conference.

Participation of students is especially encouraged through special prices offered to them.

All the information at:

http://granada2011.eurosoi.org

NEWS

Material Effects: Trading Performance For Power

Ann Steffora Mutschler

Power impacts everything, even when it comes to semiconductor manufacturing materials. While bulk CMOS technology still reigns supreme, there are a number of advanced materials being suggested as replacements when it runs out of steam at around 15nm, including silicon on insulator (SOI)—particularly in combination with FinFET multigate structures on SOI—silicon germanium, gallium nitride, and aluminum nitride

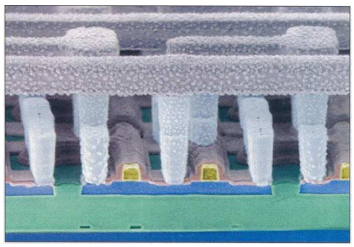
SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide, offering improved performance and diminished short channel effects in microelectronics devices.

Most promising is SOI, already in use by IBM and AMD, which uses a layered silicon-insulator-silicon substrate instead of conventional silicon substrates to reduce parasitic effects and improve performance. Specifically, SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide, offering improved performance and diminished short channel effects in microelectronics devices. SOI can be implemented in two forms: partially depleted and fully depleted.

Jamil Kawa, group director of R&D in Synopsys' implementation group, emphasized that SOI is not new. "It has been with us for a long, long time. It has a lot of proven benefits, yet it never became mainstream.

He explained that SOI could be compared to bulk CMOS by a rule of thumb: you can buy either a node in power for the same speed, or a node in performance for the same power. For example, comparing 90nm SOI to 90nm bulk, if they are running at the same clock frequency, the 90nm SOI will have the lower leakage characteristics of the 120nm bulk. Another way of looking at it is if the SOI is operating at 90nm with the same power budget that a bulk is allowed to consume, then it can give the performance that the next-generation (65nm bulk, in this example) will provide.

While it appears to be a simple formula that is carried from node to node to node, SOI didn't it catch fire as everybody thought it would mainly because of cost. "Given the lack of wide-scale adoption, the cost of initial wafers was more expensive and cost is extremely sensitive in our industry," he explained.



SOI Chip.

A second obstacle to SOI adoption has been the history effect inherent in the technology. There is no substrate with SOI. It is oxide. Therefore, charge accumulates and has nowhere to go, and this alters the behavior of the device over time. Guardbanding is used to get around the history effect. "If you want to go conservative by guardbanding 15%, all the advantages in speed that you got by going SOI you've given up by going conservative. There are techniques to alleviate that, but bulk has remained the easy way out, a proven technology, cheaper, with a lot of momentum in terms of history of use," Kawa noted.

SOI is gaining renewed interest, however. At 20nm and 15nm, CMOS leakage is a big problem.

FinFETs are being looked at, sometimes in combination with SOI, as well. "At 15nm, you don't have too many choices. Bulk is more or less dead. If you insist on going with planar, you go the SOI way. Or you go the FinFET way. There is also a third variation, which will most likely gain hold, which is FinFET on SOI. Nothing is ruled in or out yet, but the excessive variability of bulk at extremely advanced nodes is giving a second life to SOI. The verdict is still out so I'm not advocating one course or the other, but the move toward FinFETs on bulk or FinFET on SOI is clearly the way to go in terms of leakage control," Kawa added.

[*Source: Low-Power Engineering*]

CONFERENCE

General Information about EUROSOI 2011

A set of tickets corresponding to conference lunches (only Tuesday and Wednesday) and Gala Dinner (Tuesday) will be provided to each participant at the moment of registration.

Gala Dinner restaurant is at walking distance from the Parque de las Ciencias. After Gala Dinner a bus service will carry participants to the Sacromonte for a Flamenco Show. At the end of it a shuttle service will be available to every official Hotel.

(Nazaries, Alhamar and Luna)

PROGRAMME

Training Course Programme and Key-Note talks of EUROSOI 2011

As in previous editions of EUROSOI Workshop, this international event covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and applications oriented engineers.

Typical topics include:

(1) Synthesis of advanced SOI wafers (Ge, SiGe and strained layers, SOI heterostructures)

(2) Materials evaluation, properties of ultra-thin films and buried oxides, defects and stress, interface quality

(3) SOI MOSFETs: characterization, modeling and simulation of typical mechanisms, parameter extraction, reliability issues

(4) Circuit design, process and applications: low power/voltage and RF circuits, innovative memories, high voltage devices, imagers, sensors, photovoltaics and MEMS

(5) More than Moore perspectives: multiple-gates, 3D stacks of devices and circuits, nanowires, NEMS, tunneling transistors, heterogeneous integration etc.

For 2011 edition EUROSOI is trying its best and now putting the final touches.

The final programme for the Training Course, Key-Note Talks and Workshop has been scheduled and is now available:

Monday, January 17th. Training Course. Tutorial.

• 9.15h-9.30h: Introduction and Tutorial Overview. *F. Gámiz (University of Granada)*

• 9.30h-10.30h: SOI solutions for next technological nodes. *Prof. Sigfried Mantl, FZJülich, Germany*

• 10.30h-11.30h: ETSOI Technology. *Dr. Bruce Doris, IBM, USA*

• 12.00h-13.00h: CMOS-SOI-MEMS Imagers. *Prof. Y. Nemirovsky, Technion, Israel*

• 15.00h-16.00h: SOI Low-power applications. *Dr. N. Sugii, LEAP, Japan*

• 16.00h-17.00h: Memories on SOI. *Dr.Malgorzata Jurczak, IMEC Belgium*

• 17.30h-18.30h: SOI Photonics. *Dr. Jean Marc Fedeli, LETI, France*

• 20.00h-21.30h: Welcome Reception at Hotel Nazaries

Tuesday-Wednesday, January 18-19th. Workshop

Key-Note Talks.

• Readiness of FDSOI technology platform: overview. *Dr. Carlos Mazure, SOITEC, France*

• Issues on the Physics of Electronic Transport in 10 nm-scale SOIs: "How Far Can We Go?" *Prof. Max Fischetti, UTDallas, USA*

• EUROPRACTICE. *Prof. Carl Das, IMEC*

• Nanoelectronics: a bright future? *Mrs. Gisele Roesems-Kerremans. Deputy Head of Unit Information Society and Media / Nanoelectronics European Commission.*

CONFERENCE

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The grant will consist on **the waiver of the registration fee (tutorial and Workshop) and the accommodation** (4 nights of hotel at Hotel Luna, Granada) from Sunday, January 16th to Thursday, January 20th, 2011.

EUROSOI 2011.

IMPORTANT DATES:

• Jan. 17th, 2011:

Training Course.

• Jan. 18-19th, 2011:

Workshop.

CONFERENCE

Free Entrance to the Parque de las Ciencias to badge Holders

The EUROSOI Workshop is held at the Parque de las Ciencias, which is an interactive museum of over 70.000 m^2 located a few short minutes from the historic city centre of Granada, with one of the most varied offers for cultural and scientific leisure in Europe.

El Parque de las Ciencias has several areas or different rooms starting from the conception of the universe and the cosmos to the fascinating phenomenon of life that is contained in the Biosphere. There are many activities and attractions for children.

The Organizing Committee has reached an agreement thanks to which all participants can enjoy free entry during EUROSOI 2011 to visit it on presentation of their Conference Badges.

Detail of the Parque de las Ciencias in Granada

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January, 17th-19th, 2011

- SEMICON Korea 2011
Seoul, South Korea.
January 26th - 28th, 2011

- CDE 2011
Palma de Mallorca, Spain
February 8th-11th, 2011

- ISS Europe 2011
Grenoble, France.
February 27th - 1st, 2011

- Ultimate Integration on Silicon Conference (ULIS)
Cork, Ireland
March 14th-16th, 2011

- 219 ECS Meeting
Montreal (Canada)
May 1st-6th, 2011

- International Symposium on Circuits and Systems. ISCAS 2011
Rio de Janeiro, Brazil.
May 15th - 18th, 2011

- ESSDERC ESSCRIC 2011
Helsinki, Finland.
September 12th - 16th, 2011

- 2011 IEEE International SOI Conference
Tempe, Arizona (USA)
October 3rd-6th, 2011

- 220 ECS Meeting
Boston, MA (USA)
October 9th-14th, 2011

THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XXX FEBRUARY 2011

HIGHLIGHT NEWS

Fully depleted SOI shows its stuff in CPU design

IN THIS NUMBER:

ARM An ARM

Cortex M0 paper design suggest that FDSOI could be a strong contender at 20 nm.

The The Silicon-on-Insulator (SOI) Industry Consortium this morning revealed results of an analysis showing a strong advantage for fully depleted SOI (FDSOI) over bulk silicon at 20 nm.

Researchers at ARM Ltd designed a Cortex M0 CPU core using FDSOI cells characterized by IBM at its Albany, NY, fab. The ARM team then analyzed the design for performance at various operating voltages. They found that at 0.9V, FDSOI offered about the same performance at 20 nm as a good bulk planar LPCMOS process. But at lower operating voltages, FDSOI showed significantly higher performance gains than bulk when compared to a previous-generation bulk process.

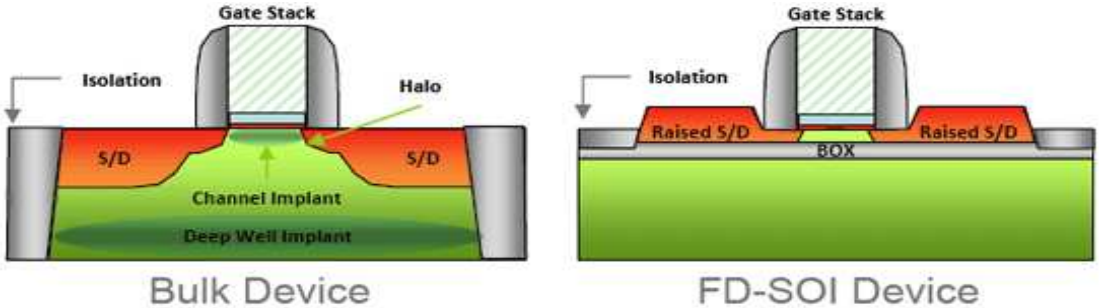
By 0.7V-still a viable operating voltage-the ARM team estimated designers would gain 25% in performance by moving from the previous node to 20-nm LPCMOS, but 80% by moving to 20-nm FDSOI. The comparison was based on the 30K gates of logic in the M0 core, placed and routed using standard tools.

Consortium executive director Horatio Mendez said that FDSOI SRAM cells were stable at these low voltages, as well. "Our analysis of the memory cell indicates it is stable at voltages 150 mV below the minimum stable voltage for 20-nm bulk CMOS," he claimed. This could be a very significant point in the aggressive power-management strategies used in mobile devices. The immediate importance of the findings will be for developers of mobile devices, Mendez asserted. By giving designers access to operating voltages in the range of 0.7V at high performance, FDSOI could enable a substantial jump in both capability and battery life. Mendez explained that FDSOI FETs display a steeper sub-threshold characteristic than bulk silicon FETs: in effect, they switch faster. This difference becomes more pronounced as you compare the transistors at lower supply voltages. "In many cases," Mendez said, "you can lay out fewer fingers in the FDSOI cell and still meet your delay requirements." This compactness in turn brings further savings in metal resistance and parasitic capacitance, all contributed to speed improvements and/or power savings.

The results are promising, but Mendez pointed out that they are first steps in a long journey. The FDSOI library ARM used was characterized with real wafer measurements at IBM. But ARM hasn't tried to fabricate the M0 design. There are still not market-ready libraries or RAM compilers for FDSOI, although work is reportedly under way. Nor is there a high-volume supply yet for the special FDSOI wafers, which must have an incredibly thin top silicon layer. Soitec is expected to make an announcement soon in this regard.

There is process work to do, as well. Current FDSOI FETs are simple transistors without strain engineering, and hence limited to relatively low speeds-in the low GHz region. Much opportunity remains for device engineering. And the process will generate new, probably simpler, design rules.

[*Continues on page 2*]



The fully depleted SOI transistor at 20 nm is significantly simpler than even a simplified version of the bulk CMOS transistor.

FDSOI could enable a substantial jump in both capability and battery life

NEWS

Fully depleted SOI shows its stuff in CPU design (*cont.*)

This simplicity could be the technology's greatest strength. Because the gate in a FD transistor completely controls the entire channel region down to the insulating box layer, the channel does not require an implant in order to achieve acceptable performance. Without the implant, the fabrication process is significantly simpler-perhaps enough simpler to compensate for the added cost of the wafers with this one point-and the entire problem of Random Dopant Fluctuation, with its huge impact on the variability of transistor threshold voltage, all but vanishes. Also, because the active channel extends all the way down to the box, there is virtually no charge trapping in the region under the channel, and hence the notorious SOI memory effect does not exist. This means that designers can work with normal CMOS timing files and timing tools without special provisions for the SOI process. Design teams can simply drop the FDSOI models into their existing flow.

The ARM announcement adds a significant new data point to the debate over the future of process technology at 20 nm and beyond. With FDSOI showing the potential for superior performance, simpler and more robust design, and no need for problematic structures such as finFETs, the weight of the argument for an FDSOI future appears to be growing.

[Source: EDN]

CONFERENCE

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More information: http://www.soiconsortium.org

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Tempe Mission Palms Hotel and Conference Center

FEATURE

SOI: It's Elementary, My Dear Watson

Adele HARS
Advanced Substrate News

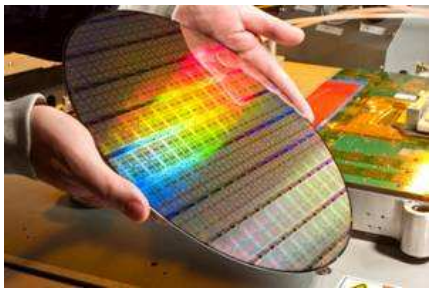
The other night, IBM's "Watson" supercomputer beat the world's two best players in the popular "Jeopardy" game show, in which the contestants are told the answer, but then have to figure out the right question. In that spirit, here's an ASN spin on the game:

Category: semiconductor design & manufacturing.

Answer: The starting substrate for the Power7 processors in IBM's Jeopardy-winning "Watson" supercomputer.

Question: What is SOI?

Yes, Power7 is the 4th generation of Power processors that IBM has based on SOI. (The first was the Power4 – dual core, 174 million transistors/processor; 0.18µm copper + SOI – that IBM introduced 10 years ago.)



So why SOI? Well, first consider the size of the thing, and the performance and power involved. Then read on, because there's more to it than that.

Here are the Power7 specs:

- 45nm SOI
- 1.2B transistors
- 32MB onchip eDRAM shared L3
- 8 processor cores
- 12 execution units per core

For Watson, you have to keep multiplying. Watson is a cluster of 90 standard, commercially available IBM Power 750 servers – each with four Power7 processors. Each of those processors has eight 3.55-GHz cores, for a total of 2880 Power7 cores. The system has a combined total of 16 Terabytes of memory and can operate at over 80 Teraflops (trillions of operations per second).

OK, so SOI is helping with speed and power – that's clear.

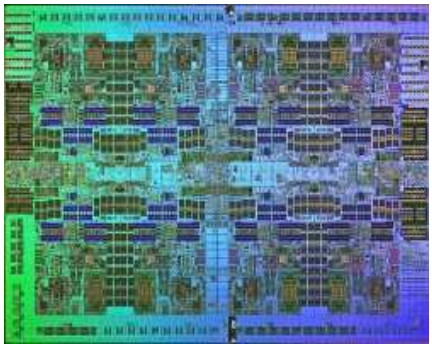
But in an ASN article five years ago (!), IBM Fellow Subramanian S. Iyer explained the importance of SOI in the memory part of the chip design equation. At that time, memory (mostly SRAM) was taking up almost 75% of the chip, so the push was on to shift at least some of that toward smaller, more stable and power-efficient embedded DRAMs (eDRAM).

As Dr. Iyer said, "The complexity adder is about half in SOI compared to bulk for deep trench based eDRAMs. […] We expect the use of eDRAM to proliferate to SOI in the 45nm generation."

Here is a cross section of IBM's 45nm SOI trench cell. The buried oxide is used to completely isolate the capacitor plate from the device.

What do you think of that?

[*Source: Advanced Substrate News*]



NEWS

Steve Longoria joins Soitec as SVP of Worldwide Strategic Business Development to drive FD-SOI adoption

Soitec (Euronext Paris), the world's leading supplier of silicon-on-insulator (SOI) and advanced solutions for the electronics and energy industries, today announced the appointment of Steve Longoria to Senior Vice President Worldwide Strategic Business Development. An industry veteran with extensive experience and a proven track record primarily at IBM Microelectronics, Longoria joins Soitec's leadership team with responsibility for strategic business development activities worldwide, to drive FD-SOI adoption. This appointment comes at a very strategic time for the company, as the SOI Industry Consortium recently announced the substantial advantages of FD-SOI for next-generation mobile and consumer applications.

"With his extensive knowledge of the overall microelectronics business and deep understanding of the role substrates play in chip design and manufacturing, Steve Longoria is a perfect fit for our senior management team," says Paul Boudre, Chief Operating Officer of Soitec.

[*Source: SOITEC*]

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THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XXXI MARCH 2011

IN THIS NUMBER:

HIGHLIGHT NEWS

Smart power semiconductor technology reduces power consumption

STMicroelectronics claims the next generation variation of its smart power technology could enable significant reductions in the power consumption of a range of electronic systems.

The company has produced a demonstrator chip with a medical equipment supplier for ultrasound scanners. Current technology typically handles eight channels, but according to ST the new semiconductor technology can handle more than 100 channels. Potential applications include new medical equipment and battery chargers in hybrid electric vehicles.

The new technology is a variation of ST's Bipolar cmos-dmos (BCD) smart power semiconductor technology that combines silicon on insulator (SOI) substrate technology with 0.16µ lithography. According to ST, this will enable chip designers to combine high density logic circuitry (1.8 and 3.3V cmos) with full dielectric isolation and a component portfolio including power mosfet transistors that can operate up to 300V, low noise devices, and high value resistors, leading to asics that cannot be implemented using conventional bulk silicon substrates.

"Semiconductor technologies that can drastically reduce electrical energy consumption in consumer and industrial appliances have existed in the labs for many years and their potential contribution to the reduction of worldwide power consumption is significant," said Claudio Diazzi, group vice president, Technology R&D, STMicroelectronics. "However, the cost of these technologies has previously been too high to make them commercially viable. We believe that this new smart power technology will make a significant difference." The development of the technology is part of an advanced European R&D project.

[*Source: New Electronics*]

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As the industry is preparing for the 14nm node that many believe will require a fully depleted device architecture, planar FDSOI offers today an excellent value proposition with an evolutionary CMOS solution for 20nm for low power and high speed. Published data show VT variability reduction by 60%, and best Ion/Ioff ratios from VDD 1V down to 0.5V compared to bulk based processes. FDSOI technology enables low VDD operation for logic and high-density SRAM cells at sub-0.6V VDD regime with excellent SNM and minimum cell size. Using an ARM Cortex™-M0 core, a team of SOI Industry Consortium members demonstrated that planar FDSOI technology enables designers to continue to decrease the voltage to reduce the overall power, while maintaining system performance.

More information:

Http://www.soiconsortium.org

FEATURE

The SOI Papers at ISSCC 2011

"the SOI papers were also notable for work reducing power consumption, extending scalability and overcoming threshold voltage variation", says Hars

Adele HARS
Advanced Substrate News

The International Solid-State Circuits Conference – better known as ISSCC – is of course where the big guns show us their big advances at the chip level. At the most recent conference, held a few weeks ago in San Francisco, advances that leveraged SOI were once again at the forefront.

As always, performance gains generate plenty of buzz. But the SOI papers were also notable for work reducing power consumption, extending scalability and overcoming threshold voltage variation.

IBM presented the world's highest frequency microprocessor to date, clocking in at 5.2 GHz. On 45nm SOI, it's the first commercial processor ever to break through the 5GHz speed barrier, and is the centerpiece of Big Blue's new zEnterprise 196 system.

In another paper, IBM presented the first embedded high-k/metal-gate (HK/MG) SRAM on 32nm SOI enabling operation at down to 0.7V.

AMD presented its Bulldozer 2-core modules, which are on 32nm SOI with HK/MG. Clocking in at 3.5GHz, we'll see them beginning in desktop and server Fusion chips this year.

In a quieter but clearly significant paper, ST and Leti compared 65nm low power (LP) partially depleted (PD) SOI with standard 65nm LP CMOS bulk. They found that PD-SOI, when combined with a low resistivity produced with forward body bias of the power switch, can reduce leakage current by 52.4% vs. bulk and increase the frequency by 20% at 1.2V, while decreasing power by 30% at 360MHz.

For summaries of additional SOI-based papers at ISSCC and other recent conferences, see ASN's PaperLinks.

[Source: Advanced Substrate News]

NEWS

Soitec announces major U.S. CPV solar power project

Soitec

Tenaska Solar Ventures Selects Soitec's Concentrix CPV Solar Power Technology To Produce 150 Megawatts of Clean Energy For San Diego Gas & Electric

Soitec will build a new 200MW CPV manufacturing facility in the San Diego region.

[Source: SOITEC]

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FEATURE

SOI for MEMS: A Promising Material

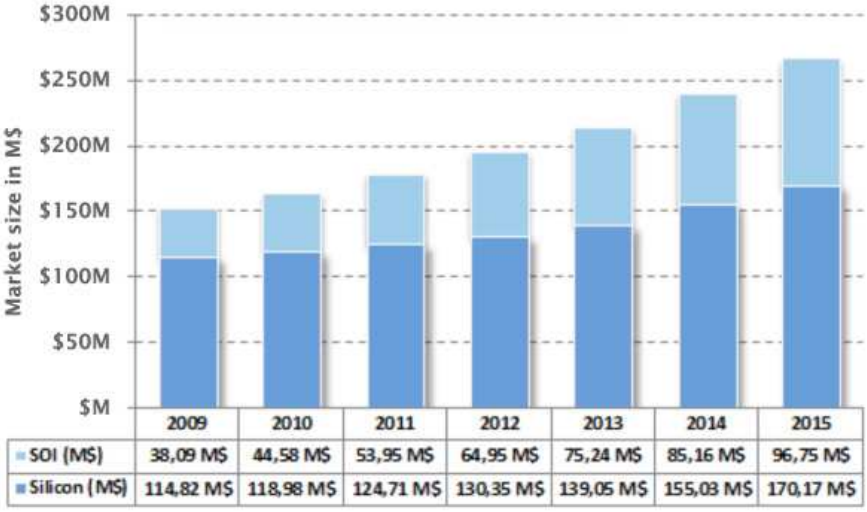
Éric MOUNIER
Yole Developpement

Although MEMS technologies are not driven by CD shrinking as ICs, that does not mean MEMS do not undergo strong technological evolutions. The ever-growing MEMS markets, today mostly driven by consumer applications, now have to be performance-driven, cost-driven and size driven.

SOI wafers are a promising substrate for MEMS manufacturing. We estimate the SOI market for MEMS devices will be close to $100M by 2015 (see Figure 1). That represents a CAGR (2011-2015) of 15.6% for SOI, compared to 8.1% for bulk silicon-based solutions.

One main reason for using SOI is to have more design freedom. Tronics, for example is using SOI with High Aspect Ratio Micromachining technology. This technology was developed to manufacture high performance custom inertial sensors (accelerometers and gyroscopes).

Other reasons cited for choosing an SOI-based solution for MEMS include the need for the smallest possible package, very tight control and precision of the structure, ability to withstand high pressure and temperature, long product lifetime, smallest possible die size and reduced cost.



	2009	2010	2011	2012	2013	2014	2015
SOI (M$)	38,09 M$	44,58 M$	53,95 M$	64,95 M$	75,24 M$	85,16 M$	96,75 M$
Silicon (M$)	114,82 M$	118,98 M$	124,71 M$	130,35 M$	139,05 M$	155,03 M$	170,17 M$

Substrate Market for MEMS

Additional features in SOI wafers can further simplify MEMS design and manufacturing. For example, "cavity-SOI", in which the SOI wafer has pre-etched cavities, enables the MEMS manufacturers to focus on their core competencies in reducing development time, which in turn can even lower production costs. Some MEMS manufacturers have found that pre-etched SOI cavities combined with dry etching simplifies the release of the devices.

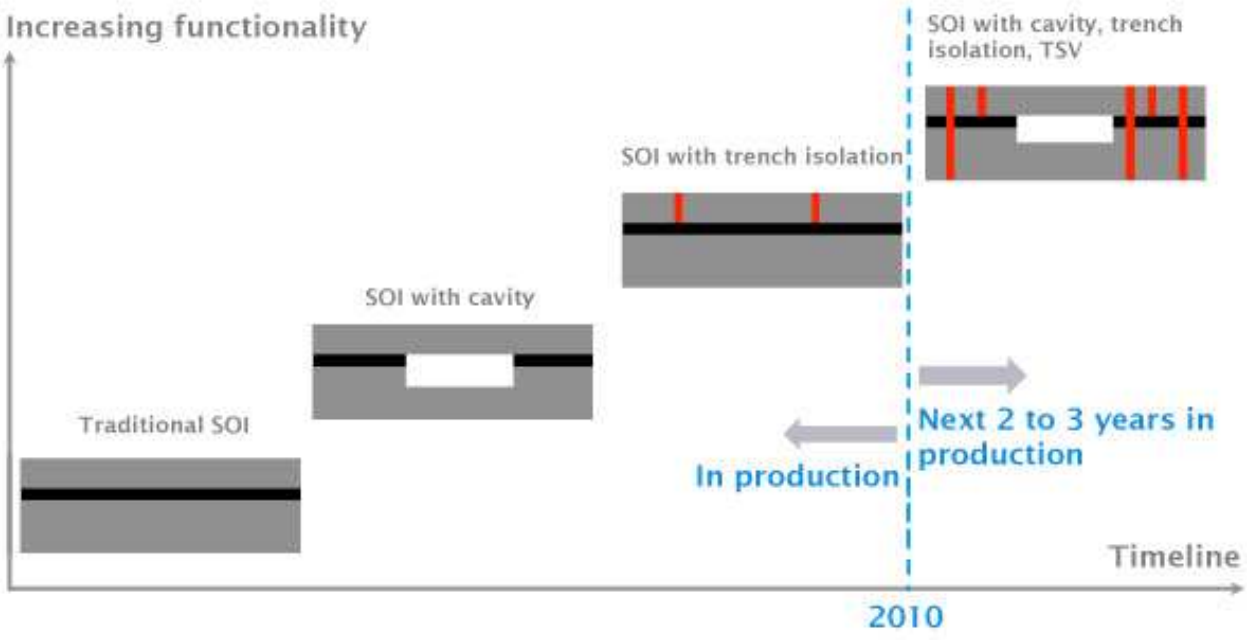
MEMS manufacturers using cavity-SOI include VTI Technologies, Invensense and other players in the seismic accelerometer (Tronics) and pressure sensor markets.

Figure 2 shows a roadmap for SOI wafers for MEMS. From "traditional" SOI, we are now using SOI with pre-etched cavities. Further developments will allow the realization of SOI wafers with trench isolation, cavities and Through Silicon Vias (TSV).

Suppliers of other substrate solutions are following similar added-value paths. Glass, for example, can be used as a thin wafer carrier for wafer level capping and/or packaging with Through Glass Vias interconnect.

Overall, we believe substrates will provide additional functionalities in the future, enabling more integrated MEMS devices.

[*Source: Advanced Substrate News*]



Roadmap for SOI wafers for MEMS

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EUROSOI Newsletter

VOLUME XXXII APRIL 2011

IN THIS NUMBER:

HIGHLIGHT FEATURE

MEMS on SOI – Growing Fast and Faster

Adele HARS
Advanced Substrate News

In the latest ASN posting by Dr. Eric Mounier of Yole Developpement, "SOI for MEMS: A Promising Material", he notes that SOI MEMS is growing at a CAGR (2011-2015) of 15.6%, compared to 8.1% for bulk silicon-based solutions.

MEMS designers are doing amazing things on SOI – which would explain that impressive growth rate.

One of my favorites is Debiotech's tiny insulin NanopumpTM targeting diabetes, fabbed by ST. As Debiotech's Laurent-Dominique Piveteau noted, "…the use of SOI wafers for fabricating the Nanopump MEMS device has significant medical and economic advantages. The SOI-based structure allows for the highest reliability in the smallest possible package, enabling very tight control and precision of the pumping mechanism. The flow rate is steady, and it is insensitive to pressure, temperature, viscosity and aging. It also offers extreme dosing precision."

Reasons cited by other contributors for using SOI for MEMS include:

• Eliminating the stress problems common in polysilicon;

• Ensuring well-defined film thickness for more accurate oscillation frequency of moving parts;

VTI's SOI-MEMS multi-axis accelerometer is the "stride sensor chip" in the miCoach real-time training system (Courtesy: VTI Technologies, adidas and Samsung

• Providing greater surface and sidewall smoothness;

• Enabling thinner structures;

• Increasing thermal conductivity of MEMS components.

But the bottom line is that it's the most cost-effective solution for their state-of-the-art MEMS devices.

MEMS also figure in two of the most recent ASN Buzz postings:

Intels's new transistors have tiny pillars, or fins that rise above the chips's surface

• Freescale and Leti just celebrated 10 years of SOI-MEMS collaboration, which includes producing a million SOI-based accelerometers a year for airbag and ESC apps in the automotive market.

• SiTime has expanded its line of SOI-MEMS-based silicon timing solutions with the industry's lowest power high-frequency oscillator. With 85% market share and over 35 million devices shipped, SiTime says it is driving the $5 Billion timing market's transition to 100% silicon-based timing.

If you'd like to see more of the why's and wherefore's of SOI-MEMS apps, just type "MEMS" into ASN's search engine. You'll get dozens of pieces from and about leaders like ST, ADI, Denso, VTI, Tronics, IBM and more.

[*Adele Hars is Editor-in-Chief at Advanced Substrate News and Director at High Tech International*]

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FEATURE

Photonics on the Move

George CELLER
Rutgers University

SOI is at the heart of silicon photonics. Here's an overview of past, present and future trends.

"probably nobody anticipated that SOI would be a perfect medium for short distance transmission and modulation of light beams", says Celler

The existence of Silicon Photonics owes much to serendipity. During the early years of the development of SOI wafer technology probably nobody anticipated that SOI would be a perfect medium for short distance transmission and modulation of light beams. Only in 1986 Richard Soref pointed out that SOI structure had the right properties for light confinement in near infrared1, and some years later Si waveguides started being designed.

A very large refractive index contrast between the Si and the SiO2 means that the light is very well confined inside the Si waveguide core, which can have sharp bends. This leads to very compact photonic integrated circuits (PICs) with densely spaced micron-scale photonic devices.

Silicon Photonics emerges

By coupling optical fibers with Si waveguides etched in SOI substrates, the light that is going into or coming out of such fibers can be processed.

In recent years the photonics community has developed all the devices needed for such processing, from light modulators and wavelength filters built in SOI to photodetectors made in germanium that was selectively grown on Si, all capable of handling data streams with a bandwidth of at least 10 Gb/s and often much higher.

Even the light sources, one missing component in the SOI device chain, are coming closer to Si.

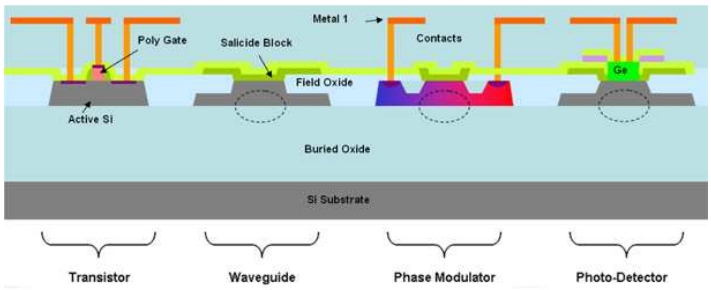
Just as multiple wavelengths can propagate in a fiber (wavelength division multiplexing or WDM), they can also propagate together in a Si waveguide, and devices to multiplex and demultiplex these data streams can also be built in SOI.

Power reduction is the key

We can expect that the future silicon PICs will be built with higher complexity and reduced cost, and with reduced power/bit of data. Fully integrated silicon photonics technology for transceivers used in short (10 – 100 m) and medium (1 km) range optical interconnects in data centers and supercomputers exists now at a few companies.

The enormous bandwidth requirements and power dissipation constraints in large IT systems will advance Si photonics for inter-board and inter-chip communication, and eventually for intra-chip links.

[Source: Advanced Substrate News]



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FEATURE

Smart power saves power

Paola GALBIATI
STMicroelectronics

ST's newest SOI-based smart power technology delivers big reductions in power consumption in medical equipment, hybrid-electric-vehicle chargers and more.

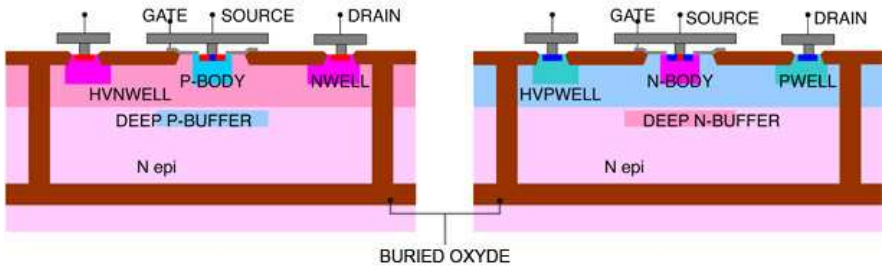
There is an urgent need for semiconductor technologies that can drastically reduce electrical energy consumption in consumer and industrial appliances. At STMicroelectronics, we have developed new SOI-based smart power technology that will make a significant difference in the power consumption of a wide range of electronic systems – from new medical equipment to battery chargers in hybrid electric vehicles.

This new work began under the aegis of an advanced European R&D* project called Smart Power Management (PM). The SmartPM project aims to put a halt to the increasing demand for energy by means of intelligent consumption, which may even reduce power usage by up to 20 percent by the year 2020.

STMicroelectronics and 17 other companies developed a range of energy-saving electronic technologies. To qualify for the program, the technologies had to be both inexpensive enough for wide market penetration and dramatic enough to make a significant impact on overall electric power consumption.

ST has been solving critical power management challenges with SOI-BCD (Bipolar-CMOS-DMOS) processes for almost a decade now. The technology we developed under the SmartPM project is a next-generation variation of our world-leading BCD smart power technology, combining SOI with 0.16-micron lithography.

This new technology enables chip designers to combine high-density logic circuitry (1.8V and 3.3V CMOS) with full dielectric isolation and a component portfolio. Included are power MOSFET transistors that can operate up to 300V, low noise devices and high-value resistors, leading to ASICs that cannot be implemented using conventional bulk-silicon substrates.



Cross Section of N-channel (left) and P-channel (right) power MOS

Ultrasound Proof

In cooperation with General Electric and Sintef, ST has verified the feasibility of this new semiconductor technology by producing a demonstrator chip for ultrasound scanners** that can handle hundreds of channels with extremely low power dissipation.

The goal is to address the next generation of scanners, which will require thousands of channels for real-time, 3D imaging. In terms of power consumption and dissipation, this requires a leap far beyond the best technology available today.

Ultrasound probes are basically made of a transmitter, a receiver and an acoustic element to convert electrical signals to mechanical waves and vice-versa.

The state of the art in this market is measured by the number of transmitting/receiving channels integrated into a probe. On today's leading edge, a typical number of channels is 128 or 192 for a 2D image probe, but even thousands for 3D image and endoscopic segments. The driving circuitry is realized with discrete components, with a total power consumption of about 3W. And since the probes touch the patient, the temperature must remain below 40 °C.

The market, however, is pushing to significantly increase the number of channels to a target beyond 2800 channels with no more than 1.8W of total power consumption. This reduces the power dissipation per channel from 3W / 128 = 23.4 mW to 1.8W / 2800 = 0.64 mW: i.e. 40 times less.

Such a target is impossible with discrete components: hence a new technology was needed, which would permit the integration of 200V or more driving circuitry in a single chip.

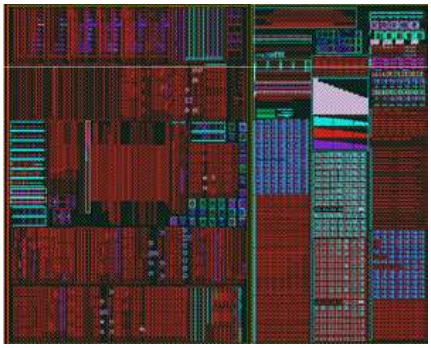
First silicon available

ST's new 0.18µm SOI-BCD technology with full dielectric isolation enables such integration. As such, it also enables many additional applications like power conversion, other electro-medical equipment, drivers for new batteries generation in electric cars and so on.

MOS devices for ultrasound machines need to handle different high-voltage classes: up to 300V, as well as 110V and 220V. Simulations helped to identify the best 220V components, and to ensure we could use the same masks for all classes.

Process integration and test chip layout have been completed. First silicon is now available, opening the door to the design of significantly more powerful yet dramatically more power-efficient end-user equipment.

Note: a related paper entitled "A Novel 0.16um – 300V SOIBCD for Ultrasound Medical Applications" will be presented at the 23rd International Symposium on Power Semiconductor Devices & ICs, to be held in San Diego May 23-26, 2011.



Top view of the test chip layout

[*Source: Advanced Substrate News*]

EUROSOI Network

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Hsinchu (Taiwan)
April 28th, 2011

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THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XXXIII MAY 2011

HIGHLIGHT NEWS

Intel Increases Transistor Speed by Building Upward

IN THIS NUMBER:

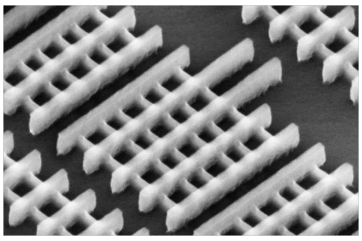
Intel announced on Wednesday that it had again found a way to make computer chips that could process information more quickly and with less power in less space.

The transistors on computer chips — whether for PC's or smartphones — have been designed in essentially the same way since 1959 when Robert Noyce, Intel's co-founder, and Jack Kilby of Texas Instruments independently invented the first integrated circuits that became the basic building block of electronic devices in the information age.

These early transistors were built on a flat surface. But like a real estate developer building skyscrapers to get more rentable space from a plot of land, Intel is now building up. When the space between the billions of tiny electronic switches on the flat surface of a computer chip is measured in the width of just dozens of atoms, designers needed the third dimension to find more room.

The company has already begun making its microprocessors using a new 3-D transistor design, called a Finfet (for fin field-effect transistor), which is based around a remarkably small pillar, or fin, of silicon that rises above the surface of the chip. Intel, based in Santa Clara, Calif., plans to enter general production based on the new technology some time later this year.

Although the company did not give technical details about its new process in its Wednesday announcement, it said that it expected to be able to make chips that run as much as 37 percent faster in low-voltage applications and it would be able to cut power consumption as much as 50 percent.



Intels's new transistors have tiny pillars, or fins that rise above the chips's surface

Intel currently uses a photolithographic process to make a chip, in which the smallest feature on the chip is just 32 nanometers, a level of microscopic manufacture that was reached in 2009. (By comparison a human red blood cell is 7,500 nanometers in width and a strand of DNA is 2.5 nanometers.) "Intel is on track for 22-nanometer manufacturing later this year," said Mark T. Bohr, an Intel senior fellow and the scientist who has overseen the effort to develop the next generation of smaller transistors.

The company's engineers said that they now felt confident that they would be able to solve the challenges of making chips through at least the 10-nanometer generation, which is likely to happen in 2015.

The timing of the announcement Wednesday is significant, Dr. Bohr said, because it is evidence that the world's largest chip maker is not slipping from the pace of doubling the number of transistors that can be etched onto a sliver of silicon every two years, a phenomenon known as Moore's Law. Although not a law of physics, the 1965 observation by Intel's co-founder, Gordon Moore, has defined the speed of innovation for much of the world's economy. It has also set the computing industry apart from other types of manufacturing because it has continued to improve at an accelerating rate, offering greater computing power and lower cost at regular intervals.

However, despite its promise and the company's bold claims, Intel's 3-D transistor is still a controversial technology within the chip industry. Indeed, a number of the company's competitors say they believe that Intel is taking a what could be a disastrous multibillion-dollar gamble on an unproved technology.

There has been industry speculation that Finfet technology will give Intel a clear speed advantage, but possibly less control over power consumption than alternative approaches.

By opting for a technology that emphasizes speed over low power, Intel faces the possibility that it could win the technology battle and yet lose the more important battle in the marketplace. The scope of Intel's gamble is underscored by the fact that while the company dominates in the markets for data center computers, desktops and laptops, it has largely been locked out of the tablet and smartphone markets, which are growing far more quickly than the traditional PC industry.

Those devices use ultra-low-powered chips to conserve battery power and reduce overheating.

[*Continues on page 2*]

NEWS

Intel Increases Transistor Speed by Building Upward (*cont*)

But like a real estate developer building skyscrapers to get more rentable space from a plot of land, Intel is now building up..

Apple, for example, uses Intel's microprocessors for its desktops and laptops, but for the iPhone and iPad it has chosen to use a rival low-power design, built by others, that Apple originally helped pioneer in the late 1980s.

Industry executives and analysts have said that Intel is likely to have a lead of a full generation over its rivals in the shift to 3-D transistors. For example, T.S.M.C., the Taiwan-based chip maker, has said that it does not plan to deploy Finfet transistor technology for another two years.

Other companies, like ST Microelectronics, are wagering that an alternative technology based on placing a remarkably thin insulating layer below traditional transistors will chart a safer course toward the next generation of chip manufacturing. They believe that the insulation approach will excel in low-power applications, and that could be a crucial advantage in consumer-oriented markets where a vast majority of popular products are both hand-held and battery-powered.

"Silicon-on-insulator could be a win in terms of power efficiency," said David Lammers, the editor in chief of Semiconductor Manufacturing and Design Community, a Web site. "From what I am hearing from the S.O.I. camp, there is a consensus and concession that Finfets are faster. That's the way you want to go for leading-edge performance."

In a factory tour here last week, Intel used a scanning electronic microscope to display a computer chip made using the new 22-nanometer manufacturing process. Viewed at a magnification of more than 100,000 times, the silicon fins are clearly visible as a series of walls projected above a flat surface.

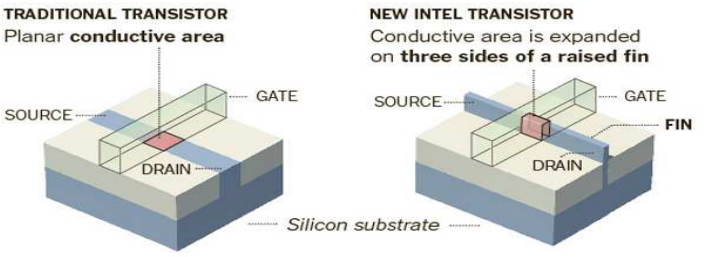
It is possible to make transistors out of one or a number of the tiny fins to build switches that have different characteristics, such as faster switching speeds or extremely low power. Looking at the chip under less magnification, it is possible to see the wiring design, which appears much like a street map displaying millions of intersections.

Despite the impressive display, Intel's executives acknowledge the challenge the company is facing in trying to catch up in the new consumer markets that so far have eluded it.

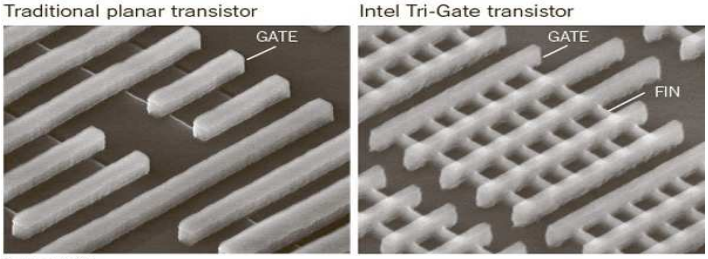
"The ecosystem right now is not aligned in our favor," said Andy D. Bryant, Intel's chief administrative officer, who now runs the company's technology and manufacturing group. "It has to be good enough for the ecosystem to take notice and say, 'We better pay attention to those guys.' "

New Transistor Grows in the Third Dimension

The new Intel transistor provides higher performance by increasing the conductive area between the source and drain regions of the chip, allowing more current to flow through.



The new transistor with its raised **fin** requires a smaller footprint, allowing more of them to fit in a computer chip. The new design can also reduce power consumption, yielding better battery life on devices.



Source: Intel

THE NEW YORK TIMES

CONFERENCE

2011 SOI Conference. Deadline for submission

IEEE

Submission period for 2011 International SOI Conference **has been extended till May 30th, 2011**.

For over 35 years the IEEE International SOI Conference has been the premier meeting of engineers and scientists dedicated to current trends in Silicon-on-Insulator technology. Sponsored by the IEEE Electron Devices Society,the conference traditionally provides a forum for open discussion in all areas of SOI technologies and applications as well as the introduction of new developments presented in original papers presented at the technical sessions.

FEATURE

GPU/CPU on SOI: the Xbox 360 did it first

Microsoft and IBM moved the CPU and the GPU of the best-selling game console in North America onto a single SoC – a year ahead of the pack.

There's a lot of excitement about the "latest trend" of integrating both the computing chip – the CPU and the graphics chip – the GPU – into a single chip. But in fact, the first GPU/CPU system-on-chip (SoC) came out in June 2010. It's on 45nm SOI, is produced by multiple foundries, and is at the heart of the hottest selling game console in North America: the Xbox 360.

The technical community refers to it as the Xbox 360 S – "S" for "slim", because the new chip enabled a host of slimming effects. The two most important were a slimmed-down power budget (43% less than the previous generation) and a serious reduction in the bill-of-materials (always good news for the bottom line).

Power down

You might think that the GPU/CPU combo also provided a major performance boost. But in fact, for game console lifetimes, one thing you can't do is toy much with performance. Game developers count on having a stable platform – they need it to work just the way they first planned it for the entire console life cycle.

One of the advantages SOI gives to chip designers is that it's a powerful "knob to turn" – they can ratchet up performance (and keep about the same some power budget), or drastically reduce power (in exchange for a less dramatic performance increase), or they can find a balance somewhere in between.

In the case of the Xbox 360 GPU/CPU, one can surmise that since they couldn't boost performance too much, they had the luxury of turning the knob way down for power. And that translates into a whole lot of benefits.

But first let's look at what they actually did.

2 for 1

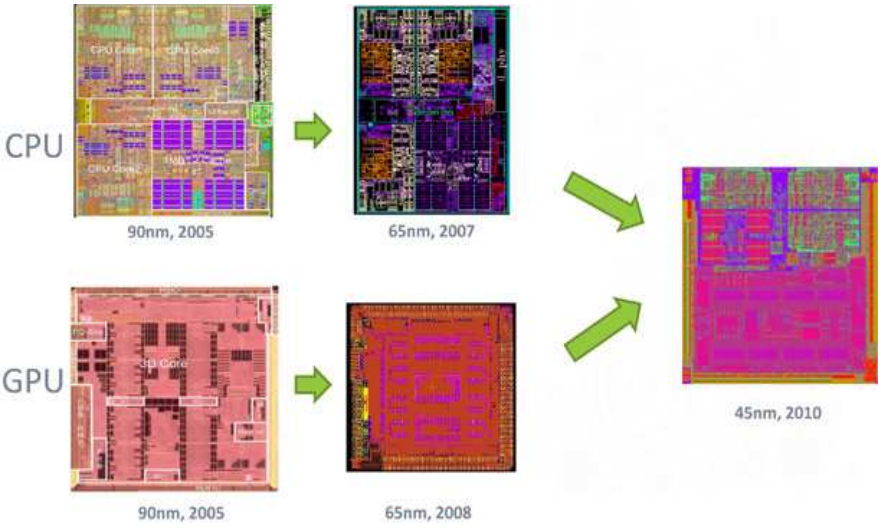
The first Xbox 360 came out in 2005, with a CPU on 90nm SOI (see ASN #6) and a GPU on 90nm bulk. A few years later, the chips were migrated to 65nm. Then in 2010, the two were combined on a single chip using 45nm SOI.

For the IBM and Microsoft chip design team, the latest challenge involved both a port (the bulk GPU to SOI), a shrink (to 45nm) and a complete redesign of the GPU (which had originally been designed by ATI). However, from a graphics standpoint, the resulting chip had to remain functionally identical to the old GPU, to ensure the backward compatibility of the games.

It also involved removing the front-side bus (FSB), which handles functional intercommunication between the CPU and GPU blocks.

Compared to having two chips, putting the two units into one chip saved 60% in power and 50% in area compared to the 90nm versions.

[*Source: Advanced Substrate News*]



FEATURE

ESD Protection for Advanced SOI

Shuqing (Victor) CAO
GlobalFoundries

Technology scaling unfavorably affects the electrostatic discharge (ESD) protection of integrated circuits mainly by reducing MOSFET oxide and junction breakdown voltage, diode current shunting capability, and by increasing the interconnect resistivity. The I/O data-rate increasingly limits the capacitive budget, exacerbating the shrinkage of ESD design space.

It is important to find ESD solutions that minimize parasitic loading while achieving superior robustness.

Silicon-on-insulator (SOI) technology presents some distinctive challenges to ESD design. The buried oxide (BOX) layer makes vertical and deep body ESD structures infeasible. The lateral SOI diode based ("rail-based") protection approach is becoming less effective in the high-current Charged Device Model (CDM) domain, owing to excessive voltage build-up along the ESD path involving power buses, power-clamps (Pclamp), and diodes.

The pad-based "local clamping" scheme is a promising option. By connecting an ESD device directly between the pad and Vss, it allows the ESD current to flow from the pad to ground without going through the resistive path (shown as crossed out in Figure 1) and the Pclamp. This way, the pad voltage is considerably reduced, immediately expanding the design space.

[*Source: Advanced Substrate News*]

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THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

VOLUME XXXIV JUNE 2011

IN THIS NUMBER:

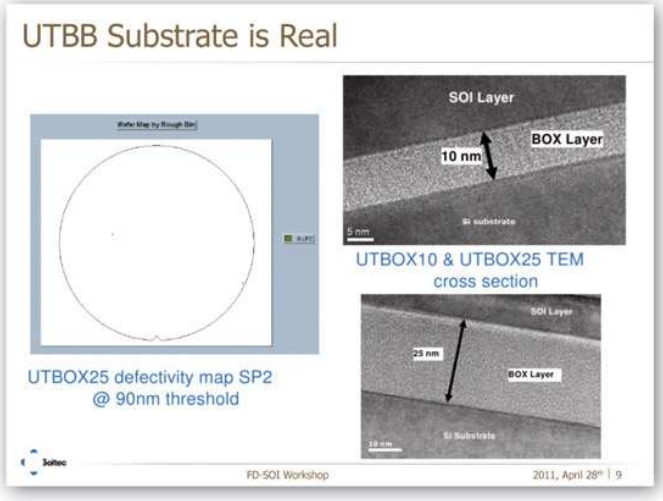
HIGHLIGHT FEATURE

FD-SOI: The Substrates Are Ready

Olivier BONNIN
Soitec

At the most recent SOI Consortium FD-SOI workshop, Soitec gave a presentation on FD-SOI substrate readiness. Here are some of the highlights.

The roadmap for FD-SOI architectures requires SOI wafer structures with ultra-thin top silicon and ultra-thin insulating BOX (Xtreme SOI TM). Using our industry-standard Smart CutTM technology, Soitec is ramping these wafers in production for high-volume manufacturing that meet all the current requirements for the 20/22nm node.



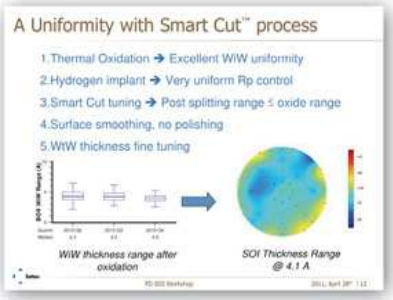
For this node, the thicknesses of the target structure are 12nm silicon and 25nm BOX to accommodate body bias strategies. The industry is referring to these wafers as UTBB, for ultra-thin body bias.

For manufacturing such wafers, the main challenges were ensuring that both the top silicon and BOX respected the extremely stringent requirements for thickness uniformity and site flatness.

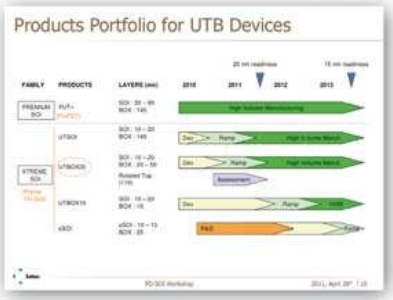
The reason for this is that for undoped FD-SOI transistors, thickness uniformity is the critical element in controlling threshhold voltage (Vt) variation.

By fine tuning of elementary process steps in our Smart Cut process, we are able to produce UTBB wafers. The following illustrations highlight how we do it.

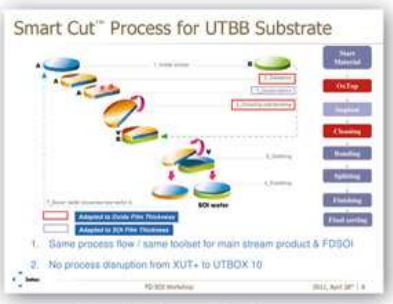
[*Olivier Bonnin is Product Integration Manager at Soitec*]



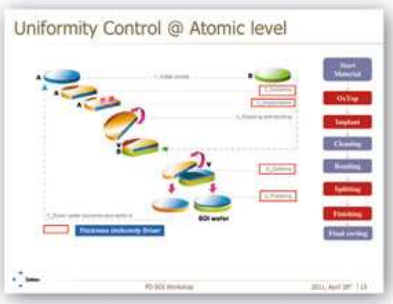
Thickness is within 4.1 Angstroms.



Wafers for nodes several generations away are currently sampling.



Ensuring ultra-thin silicon and BOX layers requires tuning the Smart Cut process oxidation and cleaning steps.



To control uniformity at the atomic level requires continual wafer-to-wafer and on-wafer control, feedback/feedforward and careful tuning of the Smart Cut process's oxidation, ion implantation, splitting and finishing steps.

FEATURE

Get Smart

Adele HARS
Advanced Substrate News

"technology like ST's SOI-BCD [...] enables chip designers to combine high-density logic circuitry (1.8V and 3.3V CMOS) with full dielectric isolation and a component portfolio", says Hars

ST's latest BCD shows how SOI yet again enables huge reductions in power consumption.

What if you had to reduce power dissipation by 40x?

That's exactly the task that fell to ST, under an EU program called Smart Power Management.

At the recent ISPSD (International Symposium on Power Semiconductor Devices and ICs) conference, STMicroelectronics and partners (GE Vingmed Ultrasound and Sintef) presented a paper on how they did it, using ST's latest SOI-based Smart Power technology.

Paola Galbiati, ST's Director of the BCD Technology Line, Technology R&D covered this project in her recent ASN article, "Smart Power Saves Power".

As she notes, ST has been solving critical power management challenges with SOI-BCD (Bipolar-CMOS-DMOS) processes for almost a decade now. The technology they developed under the SmartPM project is a next-generation variation of their BCD smart power technology, combining SOI with 0.16-micron lithography.

While the technology is applicable to chargers for electric car batteries, the first proof point was done for ultrasound probes.

The trend toward 3D ultrasound using internal probes imposes draconian limits on power. After all, you can't have the doctor putting something hot and bulky down your throat in order to image your heart.

2D probes typically have a couple hundred channels, consuming a total of about 3W of power. But for advanced 3D imagery, thousands of channels are needed – with total power consumption cut to 1.8W: about 40 times less.

This was not possible with discrete components, but it is with technology like ST's SOI-BCD, which enables chip designers to combine high-density logic circuitry (1.8V and 3.3V CMOS) with full dielectric isolation and a component portfolio. They can include power MOSFET transistors that can operate up to 300V, low noise devices and high-value resistors, leading to ASICs that couldn't be implemented using conventional bulk-silicon substrates.

ST's now got first silicon, so product design engineers can start planning a whole new generation of cutting edge solutions.

Add this to the fast-growing list of SOI-enabled game changers.

[Source: Advanced Substrate News]

TeTransesophageal probes,which are inserted into the esophagus via the throat, send a beam across the esophageal wall to image the heart structures. The constraints on space and power consumption for the embedded electronics are extremely stringent.

CONFERENCE

2011 IEEE International SOI Conference.

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More information as well as a detailed programme can be found at the conference site:

http://www.soiconference.org

Tempe Mission Palms Hotel and Conference Center

NEWS

Freescale's new QorIQ™ P2041 quad-core processor on 45nm SOI

Freescale's new QorIQ™ P2041 quad-core processor on 45nm SOI for security and other networking equipment delivers up to 10 Gb/s performance and operates at 12W typical power.

Freescale Semiconductor is making enterprise class features for security networking equipment available to small-medium businesses (SMB) with its new QorIQ™ P2041 quad-core processor. Targeting unified threat management (UTM) security appliances, the P2041 delivers up to 10 Gb/s performance in smaller, less expensive form factors such as the 1U chassis.

The P2041 combines high-end multicore processing engines with features such as hardware virtualization, cryptography and deep packet inspection technology in a single-chip solution. This integration reduces costs compared to UTM appliances based on common two- and three-chip models. In addition, the energy-efficient P2041 operates at 12W typical power.

"The P2041 integrates optimal processing performance with high-end features such as broad I/O scalability and advanced deep packet inspection functionality," said Danny Mulligan, director of marketing for Freescale's Networking Processor Division. "The processor offers UTM equipment manufacturers a quad-core, low-power solution with a mix of enterprise-like features and capabilities at SMB price points and form factors."

The P2041 is pin-compatible with Freescale's P2040 device and software-compatible with members of Freescale's range of QorIQ platforms from P1 to P5 levels. This allows customers to easily scale their end solutions and leverage their software investment across a broad array of products.

In addition to UTM systems/security appliances for SMB, the P2041 is ideal for applications such as LTE base station network interface cards (NICs), single-chip enterprise router solutions, multi-function printers, data centers, application delivery controllers, storage equipment, factory automation technology and iSCSI and switch management controllers.

Market-leading ODM Lanner, Inc. has adopted Freescale's P2041 device in its new MR-630 UTM solution. Demonstrating the outstanding performance and power profiles attainable with the P2041, the Lanner MR-630 appliance delivers 10 Gb/s processing power in a 1U chassis, hardware accelerated encryption capabilities and deep packet inspection. It also supports virtualization for application consolidation and in-service upgrades.

[*Source: Freescale Semiconductor*]

FEATURE

FD-SOI update

Horacio MÉNDEZ
Executive Director, SOI Industry Consortium

Data indicates that fully-depleted (FD) SOI offers an ideal combination for achieving ultra-low-power, high-performance and cost-effective manufacturability. Companies in the SOI Consortium are working together on furthering the development and technology evaluations.

February Results at the Circuit Level

A group of companies within the SOI Consortium (ARM, Global Foundries, IBM, SOITEC, ST and Leti), have collaborated to simulate the impact of using FD SOI on an ARM M0 Cortex core. These results were made available in a press release in February 2011 and are described below:

Benchmarking circuit: ARM Cortex M0 processor core

•Logic only (no memory)
•30k Gates

•Usual Arm core used to test advanced technologies

•P&R circuit using standard EDA tools

Target technology:

•20nm FD-SOI

Results: Impressive advantage at low Vdd

	LP Bulk Generation N	LP Bulk Generation N +1	FD SOI Generation N +1
VDD	Normalized frequency to 1	Typical % performance Improvement	Additional % performance Improvement
0.7	1	+25%	+80%
0.8	1	+25%	+40%
0.9	1	+25%	+25%

NEWS

NXP has introduced the GreenChip SSL4101T controller IC for Solid State LED lighting power supplies

NXP has introduced the GreenChip SSL4101T controller IC for Solid State LED lighting power supplies. Based on SOI, its industry-leading performance includes Total Harmonic Distortion (THD) of less than 20 percent, a high Power Factor (PF) of .99, and high efficiency of 94 percent.

[*Source: Advanced Substrate News*]

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October 9th-14th, 2011

- 5th International Workshop on Compact Thin-Film Transistor (TFT) Modeling for Circuit
Tarragona, Spain
November 9th-10th, 2011

- IEDMS 2011 : International Electron Devices and Materials Symposium 2011
Taipei, Taiwan
November 17th-18th, 2011

- 221 ECS Meeting
Seattle, Washington (USA)
May 6th-11th, 2012