INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

Grant Agreement nº 216373

D4.10 Report on EUROSOI+ Workshop held in Granada, 17-19 January 2011

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1. Introduction

The Seventh Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits took place in Parque de las Ciencias, Granada, Spain from January 17th to January 19th, 2011, organized by Prof. Francisco Gamiz (University of Granada).

EUROSOI is an international forum for promoting high-level scientific research and exchanges between research groups and industrial partners involved in SOI activities all over the world. EUROSOI activities are supported by the European Commission. Following the lively experience of the previous meetings (Granada-2005, Grenoble-2006, Leuven-2007, Cork-2008, Goteborg-2009 and Grenoble 2010), EUROSOI'11 featured oral and poster sessions, key-note presentations, as well as room enough for informal discussions. This year our *leitmotiv* was *"The contribution of SOI in the brilliant future of Nanoelectronics"*. A Special Issue of Solid-State Electronics will contain selected full-length papers.

In addition to the high level technical presentations, EUROSOI workshops are also characterized by their fringing events: in this occasion, a discussion panel (the opinion of the experts), a training course (January 17th) and the kick-off meeting of the new NANOTEC network (http://www.fp7-nanotec.eu) were organized.

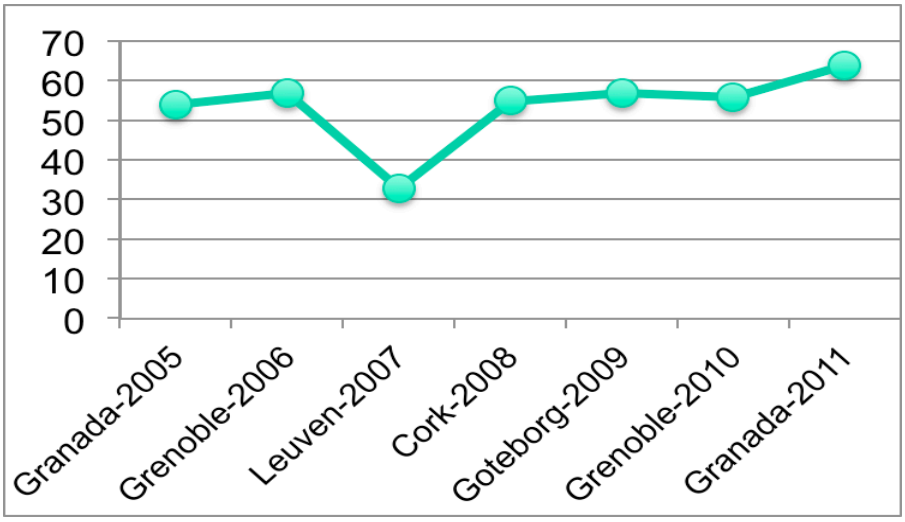
The panel of specialists was moderated by Prof. Francis Balestra (Sinano Institute & Grenoble INP) and and the opinions were aired by Dr. Malgorzata Jurczak (IMEC), Dr. Bruce Doris (IBM, USA), Dr.Olivier Faynot (CEA-LETI), Prof. Massimo Fischetti (UTDallas, USA), Prof. Carl Das (EUROPRACTICE & IMEC) and Dr. Nobuyuki Sugii (LEAP, Japan). The headline of the debate was: *"The contribution of SOI technology in the brilliant future of Nanoelectronics"*

The tutorial, which was defined by the title "Silicon on Insulator technologies for future electronics", also included Prof. Sigfried Mantl (FZJuelich, Aachen, Germany) to talk about SOI solutions for next technological nodes, Dr. Bruce Doris (IBM TJ Watson Research Center, NY, USA) on the scaling properties of ultrathin fully depleted SOI devices, Prof.Yael Nemirosky (Technion, Israel) on SOI Image sensors, Dr. Nobuyuki Sugii (LEAP, Japan) to speak Low-power applications of SOI technology; Dr. Malgorzata Jurczak (IMEC) introduced a very timely topic: Memories on SOI, and finally Dr. Jean-Marc Fedeli explored other SOI photonics.

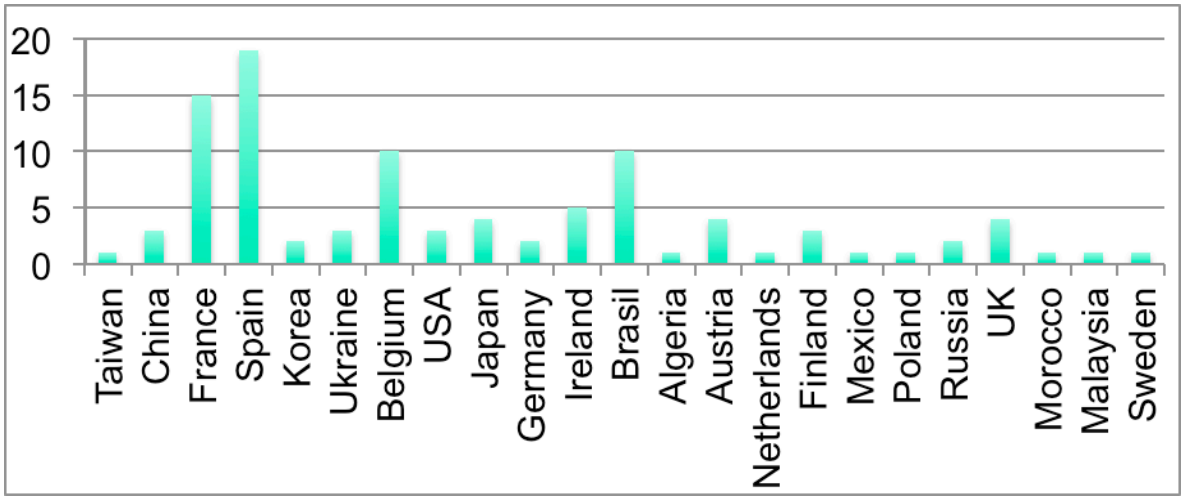
Sixty five (65) papers have been submitted this year and 60 contributions have been selected. Twenty seven (27) contributions were given as oral presentations and thirty three (33) as posters. Many of the contributions had their origin in strong national and international co-operations, born in previous EUROSOI meetings. Our special guests were Dr. Carlos Mazure (SOITEC), Prof. Massimo Fischetti (University of Texas at Dallas, USA), Dr.Carl Das (EUROPRACTICE & IMEC) and Mrs. Gisele Roesems (EU Commission) who kindly accepted to deliver outstanding keynote talks. The following graphs show

the evolution of the number of accepted contributions in EUROSOI Workshops, and the origin of the participants according to different criteria:

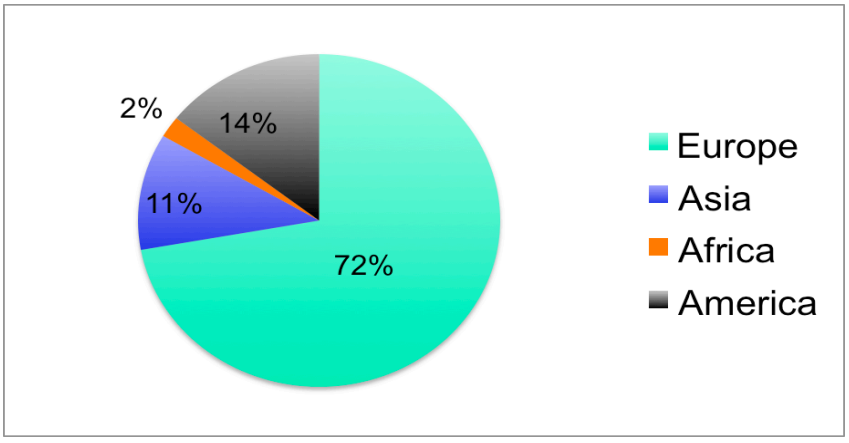
Evolution of contributions in EUROSOI workshops:



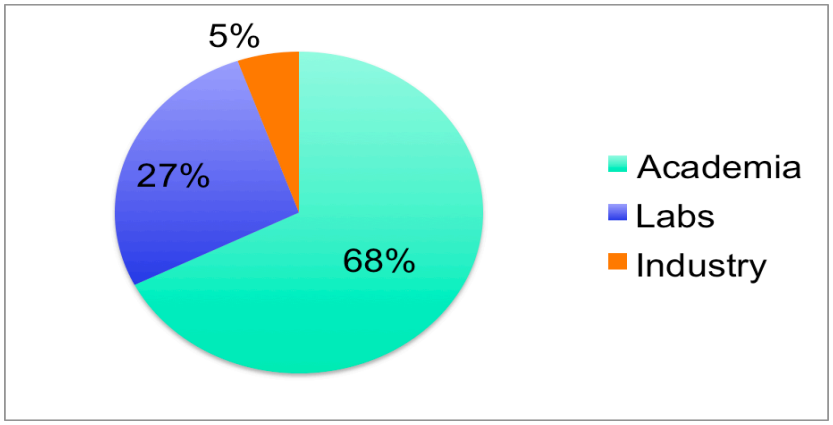
Distribution of authors in EUROSOI-2011



Distribution of authors in EUROSOI-2011 per continent:



Distribution of authors per affiliation:



2.- Agenda

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</table>

3.- Selection of papers to be published in Solid State Electronics Journal

	Title	Authors
1.	Role of the Bipolar Junction Transistor in the 40nm PD SOI NMOS Device with the Floating Body Effect	C. H. Chen, J. B. Kuo
2.	GIDL behavior with different TiN metal gate thickness and high-k gate dielectric on MuGFET devices	M. Galeti, M. Rodrigues, J.A. Martino, N. Collaert, E. Simoen, C. Claeys
3.	Subband Engineering in n-Type Silicon Nanowires using Strain and Confinement	Z. Stanojevic, V. Sverdlov, O. Baumgartner, and H. Kosina
4.	Quantum computing on silicon-on-insulator structure	S. Filippov, V. Vyurkov, and A. Orlikovsky
5.	Low Frequency Noise Spectroscopy in Advanced nFinFETs	R. Talmat, H. Achour, B. Cretu, J-M. Routoure, A.Benfdila, R. Carin, N. Collaert, A. Mercha, E. Simoen and C. Claeys
6.	Design of Silicon Double Gate Tunnel FETs with Ultra Low Ambipolar Currents	Costin Anghel, Andrei Vladimirescu and Amara Amara
7.	Electron-Hole Bi-Layers in Ultra-Thin SOI-Devices	S. Laakso, M. Prunnila and J. Ahopelto
8.	Reaching sub-32nm nodes: SGSOI optimization	C. Sampedro,F. Gamiz, L. Donetti, and A. Godoy
9.	Ultra-thin body and BOX SOI Analog Figures of Merit	V. Kilchytska, M.K. Md Arshad, S. Makovejev, S. Olsen, F. Andrieu, O. Faynot, J.-P. Raskin, D. Flandre
10.	Temperature Influence on the Analog Performance of 45^{o} Rotated Triple-Gate nFinFETs	M. A. Pavanello, M. de Souza, J. A. Martino, E. Simoen and C. Claeys
11.	TiN/GdScO3/strained Si0.5Ge0.5/SSOI stack for high mobility short channel p-MOSFETs	R. A. Minamisawa1, J. M. J. Lopes1, M. Schmidt, E. Durgun Özben1, J.-M. Hartmann2, D. Buca1, J. Schubert1, Q. T. Zhao1, and S. Mantl1

	Title	Authors
12.	LDMOS transistors on 150 mm silicon-on-polycrystalline-silicon carbide hybrid substrates	S. Lotfi, Ö. Vallin, L.-G. Li, L. Vestling, H. Norström and J. Olsson
13.	Confinement-Induced Mobility Increase in p-type [110] and [111] Silicon Nanowires	Neophytos Neophytou and Hans Kosina
14.	A2RAM: Novel dual-body 1T-DRAM cell on ultrathin SOI	Noel RodriÅLguez1, Francisco GaÅLmiz1, Sorin Cristoloveanu2
15.	Comparison of the switching speed in junctionless and accumolation-mode gate-all-around nanowire transistors	P. Razavi, R. Yan, I. Ferain, N. Dehdashti Akhavan, R. Yu, J.P. Colinge
16.	Issues on the Physics of Electronic Transport in 10 nm-scale SOIs:How Far Can We Go?	M.V.Fischetti
17.	Dispersion of Confined Acoustic Phonons in Ultra-Thin Silicon Membranes.	J. Cuffe, E. Chavez, P-O. Chapuis, E. H. El Boudouti, F. Alzina, D. Dudek, Y. Pennec, B. Djafari-Rouhani, A. Shchepetov, M. Prunnila, J. Ahopelto, C. M. Sotomayor Torres

4.- Minutes of the Management Board Meeting held in Granada, on January 17th, 2011

EUROSOI Management Board Meeting held in Granada, on 17-01-2011

Attendees:
Prof. Sorin Cristoloveanu, IMEP, Grenoble
Prof. Cor Claeys, IMEC, Leuven
Prof. Denis Flandre, UCL, Louvain la Neuve
Dr. Carlo Reita, CEA-LETI, CEA, Grenoble
Dr.Olivier Faynot, CEA-LETI, Grenoble
Prof. Andrés Godoy, UGR, Granada
Prof. Francisco Gámiz, UGR, Granada (Co-ordinator)

The fifth management board meeting of EUROSOI+ project (FP7-ICT-2007-216373) was held in Granada, Spain on January 17th, 2011, with the following agenda:

1.- Welcome.
2.- Running Guidelines.
3.- Training activities.
4.- Scientific Exchange Program.
5.- Student Grants.
7.- Technological platform. Working plan.
8.- Questions and suggestions.

1.- Welcome.

Prof. Francisco Gamiz, Co-ordinator of EUROSOI network, organizer and General Chairman of the 7th EUROSOI Workshop welcomed all the attendees to the MB meeting.

2.- Running Guidelines.

Prof. Gámiz, EUROSOI Co-ordinator, thanked all the attendees for being present at the meeting. He summarized the objectives of the project, and highlighted the tasks performed during the first year of EUROSOI+ project. Basically, we have followed the plan of activities detailed in the Annex I of the contract, Description of the Work (DoW). He also informed the MB members, that after this MB meeting, there would be a review meeting with the Commission to be attended by Mrs.Gisele Roesems, Project Officer, and

Prof.Adrian Ionescu from EPFL, Project reviewer, in addition to the members of EUROSOI+.

The agenda of the review meeting was the following:

16:00-16:15. Network status. EUROSOI-2011 (F.Gamiz)
16:15-16:30 Activity report (A.Godoy)
16:30-17:00 EUROSOI technology platform (O.Faynot & C.Reita)
17:00-17:30 Discussion
17:30-18:00 Conclusions

Prof. Gamiz also informed about the meeting to be held on Tuesday, January 18th, with Prof.Carl Das from IMEC, coordinator of EUROPRACTICE, with the goal of discussing the possible collaboration/interaction/integration of EUROSOI FD-SOI platform in EUROPRACTICE.

Finally, Prof. Gamiz informed the MB that the Commission finally accepted the extension of three months that we requested in December 2010. Thus, the final duration of the project is 42 months, finishing on June 30th, 2011.

3.- Training activities

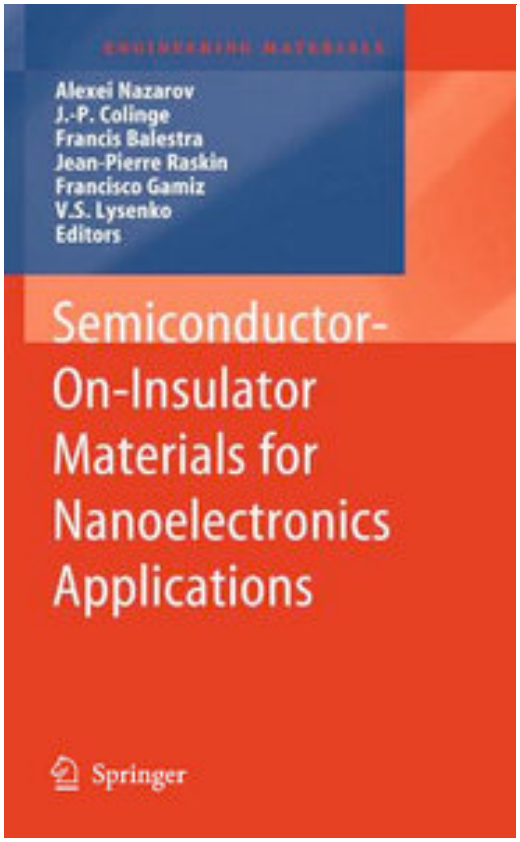
Two training events were directly organized during the last year:

i. **"Silicon on Insulator: Materials to Circuit Design " Seville, Spain, September 13th, 2010** (satellite event to ESSDERC-2010, 35 participants)
ii. **"Silicon-on-Insulator technologies for future electronics" Granada, Spain, January 25th 2011** (Training tutorial previous to EUROSOI-2011 workshop, 115 participants)

In addition**, EUROSOI** has sponsored two important training events during 2010:

1. nanoKISS 2010: Korean International Summer School on Nanoelectronics, Daegu, April, 2010
2. International SemOI Workshop "Nanoscaled Semiconducto on-Insulator Materials, Sensors and Devices, Kiev, Ukraine, October 2010

As a consequence of the second activity, the following book has been published by Springer:



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This Book is devoted to the fast evolving field of nanoelectronics, and more particularly to the physics and technology of nanoelectronic devices built on semiconductor-on-insulator (SemOI) substrates. It compiles the results of research work from leading companies and universities in Europe, Russia,

Brazil and Ukraine. Main of the Authors are involved in the NANOSIL Network of Excellence and the Thematic Network on Silicon on Insulator Technology, Devices and Circuits EUROSOI+, both of which are funded by the European Commission under the 7th Framework Program of the European Community.

This Book describes different technologies and approaches used to fabricate Semiconductor-On-Insulator materials, devices and systems. The contributed papers are articulated around four main themes:

1. Fabrication of new semiconductor-on-insulator materials
2. Physics of modern SemOI devices
3. Advanced characterization of SemOI devices
4 Sensors and MEMS on SOI.

The first chapter is focused on techniques for producing new SemOI materials. The formation of thin germanium-on-insulator films allows one to fabricate a wide variety of devices and constitutes a fundamental step towards the design of monolithic hybrid Si–Ge systems and integrated circuits. SOI wafers on high resistivity substrates can be used for RF and mixed-signal system-on-a chip (SoC) applications. Special substrates employing porous silicon technology allows one to fabricate III–V and column-IV alloy semiconductor films on dielectric substrates. Confined and guided growth of silicon nanoribbons creates new technological opportunities for the fabrication of field-effect transistors and ICs.

The second Chapter is devoted to the physics and electrical properties of novel SemOI devices such as ultrathin-body, fully depleted SOIMOSFETS scaled down to 22 nm and beyond, multigateFinFET devices, nanowire transistors using either lightly doped or highly doped silicon (junctionlessMOSFETs), carbon nanotubes (CNTMOSFETs) and single-electron devices. Novel phenomena such as quantum effects and Coulomb blockade effect occurring in nanoscale devices are described as well.

The third part of the Book focuses on advanced electrical characterization techniques for nanoelectronic devices, such as novel methods for extracting mobility, transconductance and noise.

Finally, the fourth Chapter is devoted to application of SemOI materials for biosensors, chemical sensors and MEMS. The use of SemOI substrates allow for considerable increase of sensitivity of the sensors, as well as for the fabrications of MEMS compatible with CMOS technology.

4.- Scientific Exchange Program

Prof. Andres Godoy reported on the Scientific Exchange Visits performed in 2010, and which are shown in the table below:

EUROSOI + Scientific Visits – 2010

ORIGIN (PERSON/AFFILIATION)	DESTINATION (RESPONSIBLE/AFFILIATION)	START DATE	END DATE OR DURATION OF THE VISIT	TOTAL EXPENSES	TOPIC OF THE VISIT
Jean Pierre Raskin / Universite Catholique du Lovain	University of Newcastle, UK	February, 2010	4 weeks	4205,6€	Electromechanical analysis of Si Nanowires
David Jiménez / Universidad Autónoma de Barcelona	Andres Godoy, Universidad de Granada	March, 2010	2 weeks	2767,1€	Ferroelectric Gated transistors based on SOI.
Noel Rodriguez, UGR (Spain)	Dr.Olivier Faynot, CEA-LETI, Grenoble	June, 2010	1 week	1319,39	1T-DRAM memory cells on FD-SOI transistors
Youhgo Bae, IMEP-MINATEC Grenoble on leave from University of Uiduk (Korea)	Noel Rodriguez Santiago; UGR, Granada	June, 2010	1 week	1077,91	Pseudo-MOSFET technique
Francisco Gamiz, UGR (Spain)	Prof. Sorin Cristoloveanu, IMEP-MINATEC, Grenoble	July, 2010	3 weeks	3392,99	1T-DRAM memory cells on FD-SOI transistors
Francisco Garcia, UGR (Spain)	Prof. Eddy Simoen, IMEC, Leuven	September, 2010	4 weeks	4793,37	Simulation of FinFETs

After the visit, each participant has provided to the coordinator a report describing the work developed during the visit. The reports of the visits performed during these reporting periods (M1-M42) have bee used as a basis to elaborate Deliverables D2.3, D2.4 and D2.5.

A total of 17556,40 € have been used to fund the 6 visits (15 weeks) performed along this third reporting period (M27-M36).

A Sixth Call for Proposals of Scientific Visits was launched in November, 2010. These visits will take place in the first semester of 2011. The proposals received are summarized in the table below:

EUROSOI + Scientific Visits – First Semester, 2011

ORIGIN (PERSON/AFFILIATION)	DESTINATION (RESPONSIBLE/AFFILIATION)	START DATE	END DATE OR DURATION OF THE VISIT	TENTATIVE BUDGET	TOPIC OF THE VISIT
Maryline Bawedin, Université Montpellier, France	Francisco Gamiz, UGR (Spain)	January, 2011	1 week	1400 €	2D/3D TCAD simulations of transient effects in SOI 1T-DRAMs.
Frederic Allibert, SOITEC, Bernin, France	Francisco Gamiz, UGR (Spain).	February, 2011	1 week	1400 €	Characterization of ultrathin-BOX silicon on insulator wafers
Jose Luis Rodriguez, UGR, Granada, Spain	Sigfried Mantl, FZJuliech, Aachen, Germany.	March, 2011	4 weeks	5500 €	Characterization and simulation of Schottky Barrier MOSFETs.
Noel Rodriguez, UGR, Granada, Spain	Frederic Allibert, SOITEC, Bernin, France	June, 2011	1 week	1400 €	Three-interface pseudo-MOSFET models for the characterization of SOI wafers with ultrathin film and BOX

The Board approved all the proposals since all of them agreed with the procedure and rules approved in January, 2008

5.- Student Grants

Prof. Gamiz reported that for EUROSOI'2011 fifteen (15) student grants were allocated to the following PhD students:

	Student	Advisor	Institution	EUROSOI presentation
1	Jianhua Zhou	Prof. S.C. Zhou	Chinese Academy of Science	"Hole Tunneling from Valance Band and Hot-Carrier Induced Hysteresis Effect in 0.13μm Partially Depleted SOI n-MOSFETs"
2	Amer El Hajj Diab	Prof. S.Cristoloveanu	IMEP, Grenoble France	"Low-Frequency Noise in Ultrathin SOI Pseudo-MOSFET: Where is the Noise Coming From?
3	Dimitri Soussan	Prof. Marc Bellevile	CEA-LETI, Grenoble, Framce	"65nm Partially Depleted SOI Output Buffer with Active Body-Biasing Control"
4	Guillaume Pollissard	Prof. Denis Flandre	UCL, Louvain, Belgium	A circuit level 65nm node bulk and SOI technologies comparison for analog amplifiers
5	Rudolf Theoderich Buhler	Prof. Cor Claeys	IMEC, Kapeldreef 75, B 3001 Leuven, Belgium	Fin Shape Influence on Analog Performance of MuGFETs at Room and at Low Temperature
6	Mike Schwarz	Prof. Alexander Kloes	University of Applied Sciences Giessen-Friedberg, Germany	2D Analytical Calculation of the Current in Lightly Doped Schottky Barrier Double-Gate MOSFET
7	Adam Makosiej	Prof. Andreiç Vladimirescu	ISEP, Paris, France	ULP Variability-Insensitive SRAM Design in sub-32nm UTBB FDSOI CMOS
8	Ghader Darbandy	Prof. Benjamin Iñiguez	URV, Tarragona, Spain	Study of Potential High-k Dielectrics for sub 15 nm UTB SOI MOSFETs, Using Analytical Models of the Gate Tunneling Leakage
9	Nima Dehdashti Akhavan	Prof.Jean Pierre Colinge	Tyndall, Cork, Ireland	Influence of single-atom impurity scattering on quantum transport in silicon nanowire transistor
10	Talitha Nicoletti	Prof. Cor Claeys Prof. Joao Martino	IMEC, Kapeldreef 75, Leuven, Belgium and University of Sao Paulo, Brasil	Rotated SOI MuGFETs at High Temperatures
11	Sara Lotfi	Prof. Jorgen Olsson	Uppsala University, Sweden	LDMOS transistors on 150 mm silicon-on-polycrystalline-silicon carbide hybrid substrates
12	Raul Valin	Prof. Antonio Garcia	Universidad Santiago Compostela	Multi-Subband Monte Carlo Simulation of Oxide Thickness Fluctuation on SGSOI MOSFETs
13	S.-J. Chang	Prof. S.Cristoloveanu	IMEP, Grenoble France	Scaling of SOI FinFlash Memory with Buried Storage ONO Layer (author asks for oral presentation)
14	Francisco Martinez	Prof. F. Gamiz	University of Granada	Transport mass of holes in ultra-thin DGSOI devices
15	Jose L. Padilla	Prof. F.Gamiz	University of Granada	Transport mass of holes in ultra-thin DGSOI devices

The MB agreed to fund all the proposals with a maximum of 750€/each.

6.- Report Upgrading

Prof. Godoy, Leader of WP2 (Networking activities), reminded that according to our Plan of Activities, Upgraded versions of State-of-the-Art report and EUROSOI Roadmap should be delivered for the next review meeting. He mentioned that we already composed preliminary versions of these reports, and that they were distributed for critical reading, and that the final versions are being composed taking into account the inputs of the partners.

7.- Technological platform

Dr. Carlo Reita (LETI) reported that CEA-LETI announced in October, 2010 the launch of an Exploratory MPW (Multi Project Wafers) initiative based on FDSOI (Fully Depleted SOI) 20nm process, opening the access of its 300mm infrastructure to the design community. This MPW offer is partly supported by EUROSOI+ network that gathers the main European academic partners on SOI.

This process will allow Researchers and Engineers to experiment the benefits of SOI on an advanced technology node.

CEA-Leti has has developed both an advanced High-K/Metal Gate FDSOI process and a number of specific design and simulation tools based on industry standard design flow packages. FDSOI technology presents key advantages over conventional bulk technology for future nodes.

The electrostatic integrity of the transistors is ensured by the thinness of the body without the need for extra litho steps, like in the case of FinFETs, or of channel doping. The consequence is a planar technology that exhibits at the same time excellent short channel behaviour and significant improvement of the variability as shown in a number of recent papers.

The basis of LETI technology offer will be the following:

- CMOS transistors with an undoped channel and a silicon film thickness of 6nm
- High-k / Metal Gate stack
- Single threshold voltage (Vth) n- and pMOSFET with balanced Vth of ±0.4V
- Associated Design Kit, including SPICE model (Verilog-A language), model cards extracted from silicon data, p-cells, DRC, LVS, schematic, parasitics
- Design Kit documentation

The first run is scheduled to be launched in September 2011. All details will be available on the CMP website.

8.- Questions and suggestions.

Prof. Gamiz commented to the Board on the need of elaborating a plan for extending EUROSOI activities after the end of the financial support of the Commission.

CONCLUSIONS

The seveth EUROSOI Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits was held in Granada (Spain) on 17-19 January, 2011 and was focused on recent theoretical, experimental and industrial progress on SOI materials, devices, and circuits. The meeting was attended by more than 120 researchers from labs, universities and industries all over Europe. Sixty (60) accepted contributions were presented and widely discussed, successfully covering SOI topics, such as: **i)** ***SOI Materials, Devices and Systems*****; ii)** ***Modelling and characterization;*** **iii)** ***Simulation; and*** **iv)** ***SOI Circuits and Applications.***

This workshop became the appropriate forum to promote interaction and the exchange of information between research groups and industrial partners working in SOI. The main idea of the meeting was that each participant group should communicate their findings, opinions, experiences and conclusions about SOI questions. In this sense, the main workshop's goal is becoming a first step towards preparing future European task forces in SOI (RTD projects, collaborations, etc.)

We also wanted to have the point of view of different specialists coming from Industrial Centers. We had four invited talks given by well-known experts:

- Dr.Gisele Roesems, EU-Commission, Belgium "Nanoelectronics: a bright future?"
- Dr. Carlos Mazure, SOITEC, France "Readiness of FDSOI technology platform: overview"
- Dr. Carl Das, EURORACTICE & IMEC, "EUROPRACTICE: Design and Prototyping Support for European Universities and Research Institutes"
- Prof. Massimo Fischetti, UTDallas, USA, "Issues on the Physics of Electronic Transport in 10 nm-scale SOIs: How Far Can We Go?"

We organized this rather informal and lively meeting, whose main objective was to discuss the situation of SOI technology in Europe. We had people from the EU, Switzerland, Japan, South Korea, Taiwan, China, Brazil, Ukraine, Russia, India, Canada, USA, Israel. There were 45 students. There were 25 industrial participants from SOITEC, IBM, CISSOID, ST, and Infineon.

We also organized a panel discussion chaired by Prof. Francis Balestra from IMEP-MINATEc, and Sinano Institute, Grenoble entitled "The contribution of SOI in the brilliant future of Nanoelectronics" and composed by the following six experts:

1. Prof. Massimo Fischetti, University of Texas at Dallas, USA
2. Prof.Carl Das, IMEC & EUROPRACTICE, Leuven, Belgium
3. Dr. Malgorzata Jurczak, IMEC, Leuven
4. Dr. Bruce Doris, IBM, USA
5. Dr.Olivier Faynot, CEA-LETI, Grenoble
6. Nobuyuki Sugii, Leap, Tokyo, Japan

After the initial explanations, there was a long and live debate among the panellists and the audience. Among the different applications where SOI technology could successes, ultra-low power and mobile applications were selected. Mobile internet and medical applications will create a huge semiconductor business. Memory applications based on SOI technology are not clear at this point, and more research and breakthroughs are necessary. To successfully face these demands, technology will have to provide very low power consumption, high-density memory and computational power. SOI technology provides viable solutions to these challenges thanks to the new substrate materials and device and circuit designs.

However, the main drawbacks are:

1. The lack of a large portfolio of Standard Cells Library and available IP for SOI.
2. The cost still remains as a major drawback compare to traditional bulk MOSFETs.

Both problems become a barrier to broad adoption of SOI.

In summary, SOI technology has demonstrated a significantly superior device and circuit performance and an extraordinary power reduction compared to standard bulk silicon technology. However, the range of commercial applications that currently use SOI substrates is still reduced. New business opportunities are opening and SOI technology should find its way on them. The final success of these new markets depends on two important tasks to be addressed:

i) Cost reduction compared to currently available technology.

ii) Development of a large portfolio of SC libraries and IP for SoC.

The final outcome of this meeting is a consequence of the quality of the contributions and the spirit of friendly cooperation shown by all the contributors. We wish to thank all of them for their effort. We would also like to thank all the people who allowed this meeting to take place, in particular, to the members of the Nanoelectronics Research Group at the University of Granada, to the Rector of the University of Granada, Prof. Gonzalez-Lodeiro, and Parque de las Ciencias de Granada.

A selection of the contributions presented at the Workshop will be published in a special issue of Solid State Electronics Journal devoted to the Seventh Workshop of the Thematic Network of Silicon on Insulator Technology, Devices and Circuits.

EUROSOI 2011

VII Workshop of the Thematic Network on Silicon On Insulator Technology, Devices and Circuits

January 17-19
Parque de las Ciencias
Granada, SPAIN

Conference Proceedings

ugr | Universidad de Granada

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Nanoelectronics Research Group

Departamento de Electrónica y Tecnología
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Universidad de Granada

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General Chairs' Foreword

There are many fields where SOI technology shows all its potential to circumvent the problems found in bulk technology: i) Shrinking the conventional MOS transistor below the 22nm-node, ii) the continuous demanding for low power consumption in ubiquitous mobile applications, iii) new memory designs, iv) high-temperature and power electronics, and so on. The steady work of the SOI community is demonstrating everyday that this technology can gain a higher portion of the electronic market. However, researchers have to face new challenges. But, the combination of hard work, imagination and creativity will lead us to success. These proceedings are a good example of the above.

At this point, EUROSOI initiative plays its main role: EUROSOI network was born as the meeting point where all these efforts should converge. Since its beginning in Granada (2005) and touring through Grenoble (2006), Leuven (2007), Cork (2008), Chalmers (2009) and Grenoble (2010), the workshop served as the ideal forum for inspiring discussions and to foster strong interactions among specialists in different fields.

Following previous experiences, we have prepared an informal, lively meeting with space for short presentations within a framework of larger discussion sessions. Relevant speakers have been invited to present the state-of the-art in different fields of SOI. Dr. Carlos Mazure, from SOITEC, will open the conference describing the bright future of the FDSOI technology. Then Prof. Max Fischetti, from UTDallas, will take us as far as we can go. Prof. Carl Das, from IMEC, will introduce us in the Europractice network. Last, but not least, Mrs Gisele Roesems, from EU Commission, will talk about the future European research projects in the Nanoelectronics arena, formulating the strategy for the coming years.

A Ramp session entitled "The contribution of SOI in the brilliant future of Nanoelectronics" and chaired by Prof. Francis Balestra, from IMEP, promises to be an exciting brainstorming.

Previous to the Workshop, and following the tradition, we have organized an interesting training course. The lectures are given by six experts covering the areas from technology, memories, imagers, low-power and photonics. It will take place on Monday, January 17th. We would like to highlight the magnificent venue where the Workshop will be held. We are sure that the "Parque de las Ciencias" will create a warm atmosphere prone to the exchange of scientific and technical ideas.

Finally, we would like to thank all the authors for their contributions making the workshop successful. We would also like to acknowledge the dedication of the Organizing and Technical Committees as well as the Workshop Management team for making this meeting possible. Welcome to all the participants coming from so many different places to the charming city of Granada.

Sincerely,

Francisco Gamiz & Andres Godoy
EUROSOI-2011 Organizing Committee

Organizing Committee

Francisco Gámiz
Andrés Godoy
Carlos Sampedro
Noel Rodríguez
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Cor Claeys	*IMEC, Belgium*
Denis Flandre	*UC Louvain, Belgium*

Program at a Glance

Monday, January 17th
Training Course - Gutenberg Hall

09:15-09:30		Introduction and Tutorial Overview
09:30-10:30		SOI solutions for next technological nodes
10:30-11:30		ETSOI Technology
11:30-12:00		Coffee Break
12:00-13:00		CMOS-SOI-MEMS Imagers
13:00-15:00		Lunch
15:00-16:00		SOI Low-power applications
16:00-17:00		Memories on SOI
17:00-17:30		Coffee Break
17:30-18:30		SOI Photonics
20:00-21:30		Welcome Reception - Hotel Nazaries

Tuesday, January 18th
EUROSOI 2011 Workshop - Auditorium

08:45-09:00		Conference Welcome
09:00-09:40	0.1	Readiness of FDSOI technology platform: overview (Invited) Dr. Carlos Mazuré, SOITEC *Chair: Olivier Faynot*
09:40-11:00		SESSION 1: SOI CHARACTERIZATION *Chair: Sorin Cristoloveanu*
11:00-11:20		Coffee Break
11:20.12:00	0.2	EUROPRACTICE (Invited) Dr. Carl Das, IMEC *Chair: Cor Claeys*
12:00-13:20		SESSION 2: MEMORIES *Chair: Malgorzata Jurczak*
13:20-15:00		Lunch
15:00-16:00		SESSION 3: MULTIGATE DEVICES *Chair: Carlos Mazuré*
16:00-17:00		RAMP SESSION: The contribution of SOI in the brilliant future of Nanoelectronics *Chair: Francis Balestra*
17:00-17:20		Coffee Break SESSION 4: POSTER *Chairs: Carlos Sampedro & Noel Rodríguez*
17:20-18:30		Oral Presentations
18:30-19:30		Posters Exhibition with Wine & Cheese
20:00		Bus for Gala Dinner

Wednesday, January 19th
EUROSOI 2011 Workshop - Auditorium

09:00-09:40	0.3	Issues on the Physics of Electronic Transport in 10 nm-scale SOIs:How Far Can We Go? Prof. Massimo V. Fischetti, UTDallas *Chair: Francisco Gámiz*
09:40-11:00		SESSION 5: Device Physics *Chair: Sigfried Mantl*
11:00-11:20		Coffee Break
11:20-12:00	0.4	Nanoelectronics: a bright future? (Invited) Mrs. Gisele Roesems, EU Commission *Chair: Andrés Godoy*
12:00-13:20		SESSION 6: ADVANCED SIMULATION *Chair: Massimo V. Fischetti*
13:20-15:00		Lunch
15:00-16:20		SESSION 7: ANALOG PERFORMANCE & CIRCUITS *Chair: João Antonio Martino*
16:20-16:40		Coffee Break
16:40-18:00		SESSION 8: SOI DEVICES *Chair: Jouni Ahopelto*

End of EUROSOI 2011

Training Course Program

Monday, January 17th
Gutenberg Hall

09:15-09:30	Introduction and Tutorial Overview Prof. Francisco Gámiz, University of Granada
09:30-10:30	SOI solutions for next technological nodes Prof. Sigfried Mantl, FZJülich, Germany
10:30-11:30	ETSOI Technology Dr. Bruce Doris, IBM, USA
11:30-12:00	Coffee Break
12:00-13:00	CMOS-SOI-MEMS Imagers Prof. Y. Nemirovsky, Technion, Israel
13:00-15:00	Lunch
15:00-16:00	SOI Low-power applications Dr. N. Sugii, LEAP, Japan
16:00-17:00	Memories on SOI Dr.Malgorzata Jurczak, IMEC, Belgium
17:00-17:30	Coffee Break
17:30-18:30	SOI Photonics Dr. Jean Marc Fedeli, LETI, France
20:00-21:30	Welcome Reception Hotel Nazaries

Technical Program Schedule

Tuesday, January 18th
Auditorium

08:45-09:00		Conference Welcome
09:00-09:40	0.1	Readiness of FDSOI technology platform: overview (Invited) Dr. Carlos Mazuré, SOITEC *Chair: Olivier Faynot*
		SESSION 1: SOI CHARACTERIZATION *Chair: Sorin Cristoloveanu*
09:40-10:00	1.1	Role of the Bipolar Junction Transistor in the 40nm PD SOI NMOS Device with the Floating Body Effect C. H. Chen, J. B. Kuo
10:00-10:20	1.2	Low-Frequency Noise in UT-SOI Pseudo-MOSFET: Where is the Noise Coming From? A. El Hajj Diab, I. Ionica, S. Cristoloveanu, F. Allibert, N. Rodriguez, F. Gamiz, M. Bawedin, Y.H. Bae, J. Chroboczek, G. Ghibaudo
10:20-10:40	1.3	Impact of mobility variation on Vth extraction by transconductance change and gm/Id methods in advanced SOI MOSFETs T. Rudenko, A. Rudenko, V. Kilchytska, M.K. Md Arshad, J.P. Raskin, A. Nazarov, D. Flandre
10:40-11:00	1.4	Impact of Gate Voltage on Hysteresis Effect in 0.13μm Floating-Body PDSOI n-MOSFETs J. Zhou, S. Cao, C. Gao, S.K. Pang, J.X. Luo, S.C. Zou
11:00-11:20		Coffee Break
11:20.12:00	0.2	EUROPRACTICE (Invited) Dr. Carl Das, IMEC *Chair: Cor Claeys*
		SESSION 2: MEMORIES *Chair: Malgorzata Jurczak*
12:00-12:20	2.1	A2RAM: Novel dual-body 1T-DRAM cell on ultrathin SOI N. Rodríguez, F. Gámiz, S. Cristoloveanu
12:20-12:40	2.2	Scaling of SOI FinFlash Memory with Buried Storage ONO Layer S.J. Chang, M. Bawedin, W. Xiong, J.-H. Lee, S. Cristoloveanu
12:40-13:00	2.3	ULP Variability-Insensitive SRAM Design in sub-32nm UTBB FDSOI CMOS A. Makosiej, A. Vladimirescu, O. Thomas, A. Amara
13:00-13:20	2.4	0.42-V 576-kb 0.15-μm FD-SOI SRAM with 7T/14T Bit Cells and Substrate Bias Control Circuits for Intra-Die and Inter-Die Variability Compensation K. Yamaguchi, S. Okumura, M. Yoshimoto, H. Kawaguchi

13:20-15:00 **Lunch**

SESSION 3: MULTIGATE DEVICES
Chair: Carlos Mazuré

15:00-15:20 **3.1** **Multi-Gate Voltage Selectable Silicon-Nanowire-FETs**
F. Wessely, T. Krauss, U. Schwalke

15:20-15:40 **3.2** **Comparison of the switching speed in junctionless and accumulation-mode gate-all-around nanowire transistors**
P. Razavi, R. Yan, I. Ferain, N. Dehdashti Akhavan, R. Yu, J.P. Colinge

15:40-16:00 **3.3** **Fin Shape Influence on Analog Performance of MuGFETs at Room and at Low Temperature**
R. T. Bühler, J. A. Martino, P. G. D. Agopian, R. Giacomini, E. Simoen, C. Claeys

16:00-17:00 **RAMP SESSION:**
The contribution of SOI in the brilliant future of Nanoelectronics
Chair: Francis Balestra

17:00-17:20 **Coffee Break**

SESSION 4: POSTER
Chairs: Carlos Sampedro & Noel Rodríguez

17:20-18:30 **Oral Presentations**

18:30-19:30 **Posters Exhibition with Wine & Cheese**

4.1 **Hole Tunneling from Valance Band and Hot-Carrier Induced Hysteresis Effect in 0.13 μm Partially Depleted SOI n-MOSFETs**
J. Zhou, S. K. Pang, S. Cao, S. C. Zou

4.2 **Highly Bi-Axially Orientation-Controlled Si Thin Films on Glass Substrates by Double-Line-Beam CW Laser Annealing**
S.Kuroki, Y. Kawasaki, S. Fujii, K. Kotani, T. Ito

4.3 **Extraction of flat-band voltage and parasitic resistance in junctionless MuGFETs**
A.N. Nazarov, C.W. Lee, A. Kranti, I. Ferain, R. Yan, N. Dehdashti Akhavan, P. Razavi, R. Yu, JP Colinge

4.4 **Low Frequency Noise Spectroscopy in Advanced nFinFETs**
R. Talmat, H. Achour, B. Cretu, J.M. Routoure, A.Benfdila, R. Carin, N. Collaert, A. Mercha, E. Simoen, C. Claeys

4.5 **Analysis and Optimization of Lateral Thin-Film Siliconon-Insulator (SOI) PMOS Transistor with an NBL layer in the Drift Region**
I. Cortés, G. Toulon, F. Morancho, D. Flores, E. Hugonnard-Bruyère, B. Villard

4.6 **Ballistic Spin Field-Effect Transistors Built on Silicon Fins**
D. Osintsev, V. Sverdlov, Z. Stanojevic, A. Makarov, S. Selberherr

4.7 **Analog Performance of 60 MeV Proton-Irradiated SOI MuGFETs with Different Strain Technologies**
P.G.D. Agopian, J.A. Martino, D. Kobayashi, M. Poizat, E. Simoen and C. Claeys

4.23 A Compact Double-Gate MOSFET Model Consistent with a Multi-Subband Ensemble Monte Carlo Model
M. Cheralathan, C. Sampedro, J.B. Roldán, F. Gámiz, B. Iñiguez

4.24 1/f Noise in Strained SGOI MOSFETs
J. Gyani, J. El Husseini, F. Martinez, M. Bawedin, M. Valenza, C. Le Royer, J. F. Damlencourt

4.25 Influence of the orientation and geometry on the Phonon-limited Mobility of Square Silicon Gate-All-Around MOSFETs
I. M. Tienda-Luna, F. G. Ruiz, A. Godoy, F. Gámiz

4.26 Subband Engineering in n-Type Silicon Nanowires using Strain and Confinement
Z. Stanojevic, V. Sverdlov, O. Baumgartner, H. Kosina

4.27 Quantum computing on silicon-on-insulator structure
S. Filippov, V. Vyurkov, A. Orlikovsky

4.28 Asymmetric Series Association of SOI MOSFET to Improve the Device Analog Characteristics
I. C. B. Santos, M. de Souza, D. Flandre, M. A. Pavanello

4.29 Impact of Mismatch on the Analog Properties of Standard and Graded-Channel SOI nMOSFETs
M. de Souza, D. Flandre, M.A. Pavanello

4.30 Insights on Device Performance of SOI MOSFET with 60 nm and 15 nm BOX Thickness
A. Suhaila Mohd Zain, B. Cheng, X. Wang, A. Asenov

4.31 Using Diamond SOI nMOSFETs to Improve the Frequency Response of the Analog Integrated Circuits
S. Pinillos Gimenez, R. Claser, D. Manha Alati

4.32 DFT Simulation of SOI Devices: Semiconductor/Oxide Interfaces
B. Biel, L. Donetti, A. Godoy, F. Gámiz

4.33 Multi-Subband Monte Carlo Simulation of Oxide Thickness Fluctuation on SGSOI MOSFETs
R. Valin, C. Sampedro, N. Seoane, M. Aldegunde, A. Garcia-Loureiro, A. Godoy, and F. Gamiz

4.34 Universal relationship between substrate current and history effect in SOI MOSFETs and its importance for physical compact modeling
A. Toda, N. Higashiguchi, K. Ohyama, Y. Shintaku, S. Amakawa, M. Miyake, H. Kikuchihara, M. Miura-Mattausch

20:00 Bus for Gala Dinner

Wednesday, January 19th
Auditorium

09:00-09:40	0.3	**Issues on the Physics of Electronic Transport in 10 nm-scale SOIs:How Far Can We Go?** **Prof. Massimo V. Fischetti, UTDallas** *Chair: Francisco Gámiz*
		SESSION 5: Device Physics *Chair: Sigfried Mantl*
09:40-10:00	5.1	**Confinement-Induced Mobility Increase in p-type [110] and [111] Silicon Nanowires** **N. Neophytou, H. Kosina**
10:00-10:20	5.2	**Transport mass of holes in ultra-thin DGSOI devices** **L. Donetti, F. Gámiz, F. Martínez-Carricondo, J.L.Padilla, N.Rodriguez**
10:20-10:40	5.3	**Electron-Hole Bi-Layers in Ultra-Thin SOI-Devices** **S. Laakso, M. Prunnila, J. Ahopelto**
10:40-11:00	5.4	**Dispersion of Confined Acoustic Phonons in Ultra-Thin Silicon Membranes** **J. Cuffe, E. Chavez, P-O. Chapuis, E. H. El Boudouti, F. Alzina, D. Dudek, Y. Pennec, B. Djafari-Rouhani, A. Shchepetov, M. Prunnila, J. Ahopelto, C. M. Sotomayor Torres**
11:00-11:20		**Coffee Break**
11:20-12:00	0.4	**Nanoelectronics: a bright future? (Invited)** **Mrs. Gisele Roesems, EU Commission** *Chair: Andrés Godoy*
		SESSION 6: ADVANCED SIMULATION *Chair: Massimo V. Fischetti*
12:00-12:20	6.1	**Reaching sub-32nm nodes: SGSOI optimization** **C. Sampedro, F. Gámiz, L.Donetti, A. Godoy**
12:20-12:40	6.2	**3D Monte Carlo simulations of a 25 nm gate length SOI FinFET using unstructured tetrahedral grids** **M. Aldegunde, A.J. Garcia-Loureiro, N. Seoane, R. Valin, K. Kalna**
12:40-13:00	6.3	**Comprehensive Simulation Study of Statistical Variability in 32nm SOI MOSFET** **N. M. Idris, B. Cheng, A. R. Brown, S. Markov, A. Asenov**
13:00-13:20	6.4	**Quantum simulation of an UTB FD SOI FET with channel imperfections** **V. Vyurkov, I. Semenikhin, A. Orlikovsky**
13:30-15:00		**Lunch**

SESSION 7: ANALOG PERFORMANCE & CIRCUITS
Chair: João Antonio Martino

15:00-15:20	**7.1**	**65nm Partially Depleted SOI Output Buffer with Active Body-Biasing Control** **D. Soussan, S. Majcherczak, A. Valentian, M. Belleville**
15:20-15:40	**7.2**	**A circuit level 65nm node bulk and SOI technologies comparison for analog amplifiers** **G. Pollissard-Quatremère, D. Flandre**
15:40-16:00	**7.3**	**Ultra-thin body and BOX SOI Analog Figures of Merit** **V. Kilchytska, M.K. Md Arshad, S. Makovejev, S. Olsen, F. Andrieu, O. Faynot, J.P. Raskin, D. Flandre**
16:00-16:20	**7.4**	**Temperature Influence on the Analog Performance of 45o Rotated Triple-Gate nFinFETs** **M. A. Pavanello, M. de Souza, J. A. Martino, E. Simoen, C. Claeys**
16:20-16:40		**Coffee Break**

SESSION 8: SOI DEVICES
Chair: Jouni Ahopelto

16:40-17:00	**8.1**	**TiN/GdScO3/strained Si0.5Ge0.5/SSOI stack for high mobility short channel p-MOSFETs** **R. A. Minamisawa, J. M. J. Lopes, M. Schmidt, E. Durgun Özben, J.-M. Hartmann, D. Buca, J. Schubert, Q. T. Zhao, S. Mantl**
17:00-17:20	**8.2**	**2D Analytical Calculation of the Current in Lightly Doped Schottky Barrier DG MOSFET** **M. Schwarz, A. Kloes, B. Iñíguez**
17:20-17:40	**8.3**	**LDMOS transistors on 150 mm silicon-on-polycrystalline-silicon carbide hybrid substrates** **S. Lotfi, Ö. Vallin, L.-G. Li, L. Vestling, H. Norström, J. Olsson**
17:40-18:00	**8.4**	**Lateral Transient Voltage Suppressor for SOI Technologies** **J. Urresti, S. Hidalgo, I. Cortés, D. Flores**

End of EUROSOI 2011

Session 1: SOI Characterization

Chair: Sorin Cristoloveanu

Role of the Bipolar Junction Transistor in the 40nm PD SOI NMOS Device with the Floating Body Effect

C. H. Chen, J. B. Kuo*

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***Abstract*-This paper reports the role of the parasitic bipolar device in the 40nm PD SOI NMOS device with the floating body effect. Using a unique extraction method, the function of the parasitic bipolar device during transient operations could be modeled. During the turn-on transient by imposing a step voltage from 0V to 2V at the gate, the case with a slower rise time shows a faster turn-on in the drain current due to a stronger function of the parasitic bipolar device from smaller displacement currents through the gate oxide, as reflected in the current gain, as verified by the experimentally measured results.**

I. Introduction

Floating body effect of PD SOI CMOS devices have been studied intensively in the past [1][2]. The parasitic bipolar device in the PD device, which could cause the Kink effect, is difficult to model [3][4]. In fact, the parasitic bipolar device is important for the behavior of the PD SOI CMOS devices. In this paper, using a unique extraction method, the function of the parasitic bipolar device during DC and transient operations could be modeled. In the following section, the test device is described first, followed by the DC and the transient operations and discussion.

II. 40nm PD SOI NMOS Device

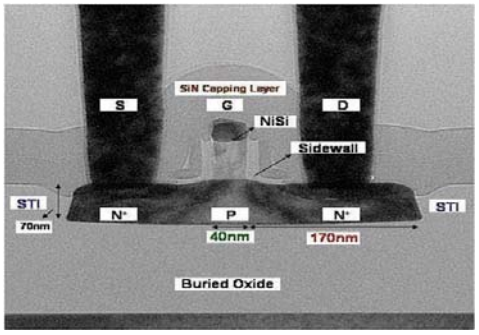

Fig. 1 TEM cross section of the 40nm PD SOI NMOS device under study.

Fig. 1 shows the TEM cross section in the channel length direction of the 40nm PD SOI NMOS device under study [3]. The test device has a 70nm thin film doped with a p-type doping density of $3x10^{18}cm^{-3}$ above a buried oxide of 145nm and a gate oxide of 1.5nm. A 65nm LDD region doped with an n-type density of $10^{19}cm^{-3}$ under a sidewall spacer has been used. A nickel polycide is formed on the top of the gate and a SiN capping layer is deposited over the device. The effective channel length of the device is 40nm. Experimental measurement of the test device and 2D device simulation have been used to carry out the study.

III. Transient Operation

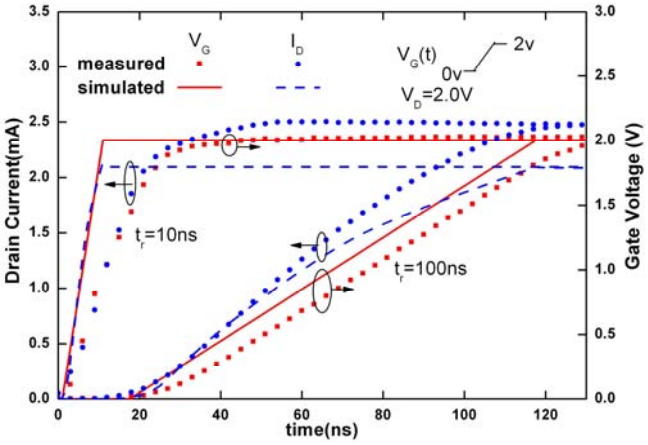

Fig. 2. Drain current of the test device during the turn-on transient by imposing a step voltage from 0V to 2V at the gate based on experimentally measured data and the 2D simulation .

The behavior of the parasitic bipolar device during the transient of the PD SOI NMOS may be quite different from that operating at DC. Fig. 2 shows the drain current of the PD device during the turn-on transient by imposing a step voltage from 0V to 2V at the gate of the test device based on the experimentally measured data and 2D simulation result for the cases with the rise times of 10ns and 100ns. As shown in the figure, with a rise time of 10ns for the gate voltage, the drain current could not reach its peak value at the end of the gate voltage ramp while with a rise time of 100ns, it almost reaches it. The different slew rates of the drain current curves during the ramp up transients between the cases with different rise times may have some implications.

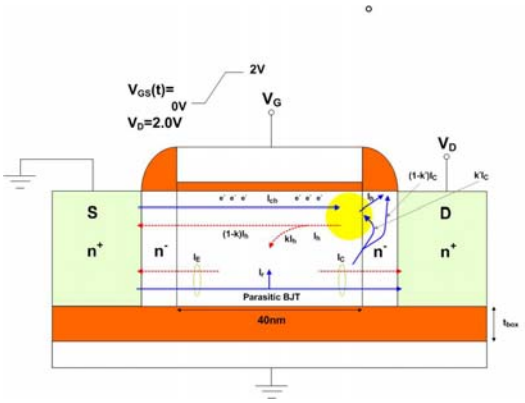

Fig.3.Current conduction mechanism during the turn-on transient by imposing a step voltage from 0V to 2V at the gate of the test device.

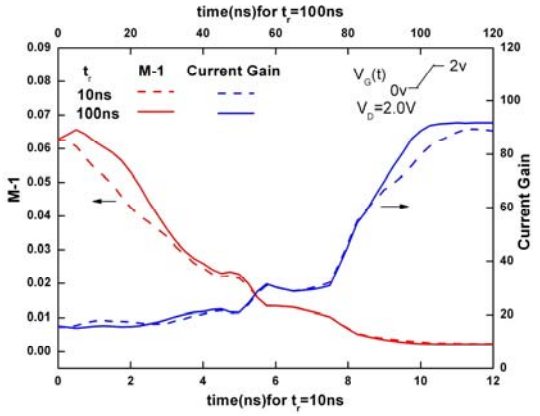

Fig. 4. Multiplication factor (M-1) and current gain of the parasitic bipolar device of the PD SOI NMOS device during the turn-on transient the gate for the cases with the rise times of 10ns and 100ns.

Fig. 3 shows the current conduction mechanism during the turn-on transient by imposing a step voltage from 0V to 2V at the gate of the test device. Different from the DC condition, during the turn-on transient, the drain and the source displacement currents (dQ_D/dt, dQ_S/dt) through the gate oxide need to be considered. Taking into account the partitioned charge model (Q_S, Q_D) for the surface channel of the device with the current conduction mechanism described in the DC condition, one may obtain the multiplication factor (M-1) and the current gain of the parasitic bipolar device during the turn-on transient of the test device. Fig. 4 shows the multiplication factor (M-1) considering the impact ionization in the post-saturation region in the lateral channel and the current gain of the parasitic bipolar device of the PD SOI NMOS device during the turn-on transient by imposing a step voltage from 0V to 2V at the gate for the cases with the rise times of 10ns and 100ns based on the 2D simulation result. As shown in the figure, along with the progress of time during the ramp-up period, the multiplication factor (M-1) decreases due to the increase of the gate voltage leading to a smaller post-saturation region. On the other hand, when the gate voltage is small during the initial stage of the ramp-up period, the current gain of the parasitic bipolar device is relatively small, indicating that the parasitic bipolar device is not turned on yet. During the final stage of the gate ramp-up period, the current gain suddenly increases, which implies the turn-on of the parasitic bipolar device. As shown in the solid-lines, for the case with the longer rise time of 100ns, both M-1 and the current gain are larger, which means the impact ionization in the post-saturation region is larger and the parasitic bipolar device functions stronger.

More insight into the operation of the parasitic bipolar device in the PD SOI NMOS device during the turn-on transient could be obtained by the studying the 2D density contours in the thin film of the device at the end of the gate voltage ramp as shown in Fig. 5. As shown in the figure, for the rise time of 100ns, the less electron content in the thin film implies a stronger

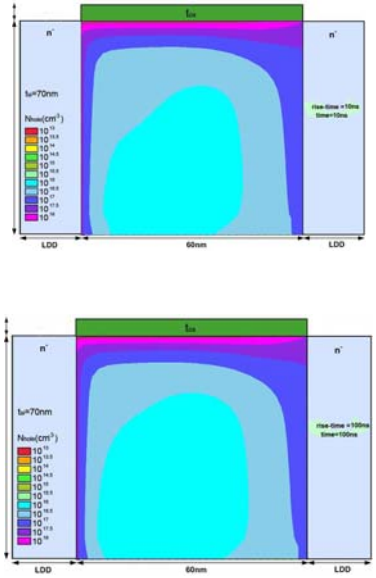

Fig. 5. 2D electron density contours in the thin film of the 40nm PD SOI NMOS device during the turn-on transient by imposing a step voltage from 0V to 2V at the gate.

function of the parasitic bipolar device. Hence, the drain current is larger for the case with the rise time of 100ns. With a larger rise time, the drain and source displacement currents (dQ_D/dt, dQ_S/dt) become smaller. As a result, more holes generated by the impact ionization in the post-saturation region stay at the bottom of the thin film, becoming the base current of the parasitic bipolar device. Therefore, the function of the parasitic bipolar device is stronger, leading to a larger drain current.

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Low-Frequency Noise in Ultrathin SOI Pseudo-MOSFET: Where is the Noise Coming From?

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1. Abstract

Noise measurements at wafer level were performed using the pseudo-MOSFET. We discuss 1/f noise behavior in relatively thick and ultrathin SOI layers. The influence of wafer surface defects is demonstrated and further confirmed in gold decorated SOI. An explanation is proposed for the noise sources.

2. Introduction

Low-frequency noise (LFN) measurements have already been carried out on fully processed MOSFET on SOI [1]. Here we propose to directly characterize SOI substrates by noise measurements in the pseudo-MOSFET (Ψ-MOSFET) configuration. The Ψ-MOSFET is a powerful tool, routinely used for wafer inspection (mobility, threshold voltage, subthreshold swing, density of traps) [2]. Ψ-MOSFET simply requires two probes on the silicon film that are used as source and drain. The current is controlled by the substrate bias (back gate) and the buried oxide (BOX) serves as gate dielectric (Fig.1, inset). LFN is a suitable technique for detailed investigation of BOX defects [1]. However, noise measurements have not been reported yet for Ψ-MOSFET with pressure contacts.

3. Measurement Results

The samples under test are SOI wafers with 20-88 nm thick silicon film and 145 nm BOX thickness. Two types of Ψ-MOSFET measurements were performed: static I_D (V_G) curves and noise. Noise measurements show *1/f* (flicker noise) behavior on 88 nm film thickness (Fig.1). *1/f* noise is related to conductivity fluctuations due to either carrier number or mobility fluctuations [3]. Fig.2 shows normalized power spectral density (PSD) versus drain current I_D on the 88 nm thick film for different pressures applied to the probes. The curves follow the 'carrier number fluctuation' (CNF) model as they are proportional to $(g_m/I_d)^2$ [4]. It is well known that the probe pressure controls the series resistance [5]. In Fig.2, no pressure dependence of the noise is observed; we conclude that the series resistance does not play the dominant role as a noise source. The density of traps (D_{it}) obtained with LFN is one order of magnitude higher than the value extracted from the subthreshold slope. Is this difference due to the top interface defects? To answer this question we probed thinner films where the coupling between the top surface and the film-BOX interface is stronger. Fig.3 shows drain current and transconductance versus back gate voltage in double sweep mode (forward and backward) for 21 nm film. The forward sweep (from 0 to V_G) is safer than the backward sweep (from V_G to 0) and makes more accurate D_{it} extraction ($D_{it\text{-}Forward} < D_{it\text{-}Backward}$).

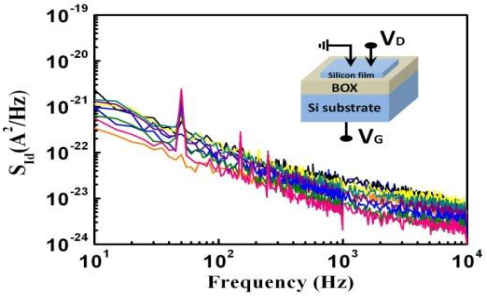

Fig.1: *Power spectral density versus frequency in 88 nm thick film Ψ-MOSFET, showing 1/f noise. Inset: Experimental configuration.*

Inset of Fig.4 shows that PSD versus frequency S_{Id} (f) follows 1/*f*. Unlike the case of 88 nm film, the PSD noise in 21 nm films is not correlated with $(g_m/I_d)^2$ for 60 g pressure (Fig.4). Surprisingly, this correlation is recovered for a higher pressure of 75 g (Fig.5) and the CNF model is again applicable. Nevertheless, the extracted D_{it} values are 3 orders of magnitude higher than the ones calculated from the subthreshold slope. This huge difference could come from two sources. Firstly, the geometrical factor $W \cdot L$ is difficult to

evaluate in Ψ-MOSFETs. Secondly, the top interface might play a crucial role. Indeed, the samples have not been passivated, so they are covered by native oxide which forms a very poor interface with the silicon film. The extra noise source observed might be connected to this top interface.

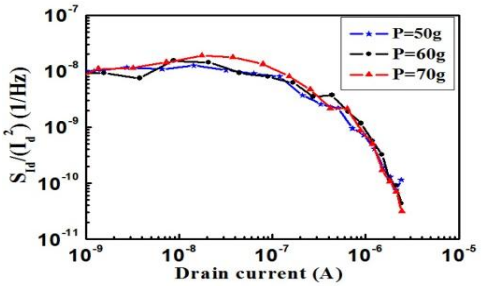

Fig.2: *Normalized power spectral density noise versus drain current in Ψ-MOSFET with 88 nm film thickness for various probe pressures (50 g, 60 g and 70 g).*

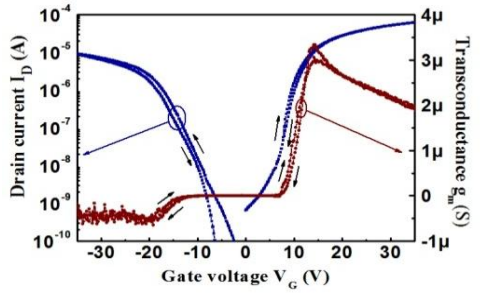

Fig.3: *Drain current I_D and transconductance g_m versus gate voltage V_G in 21 nm film Ψ-MOSFET for double sweep mode.*

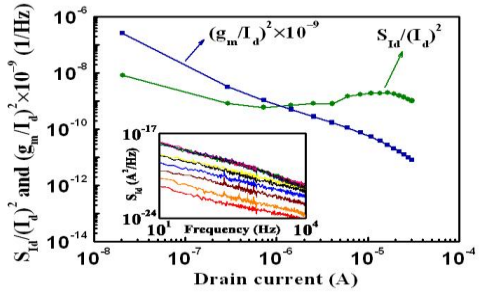

Fig.4: *Normalized PSD and $(g_m/I_d)^2\times10^{-9}$ versus drain current for a 21 nm film thickness (60 g probe pressure). No correlation is observed; therefore CNF model cannot be applied. Inset: PSD versus frequency, showing 1/f noise.*

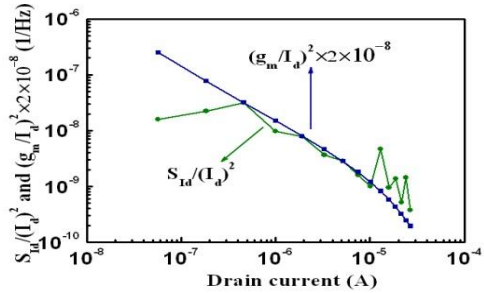

Fig.5: *Normalized PSD and $(g_m/I_d)^2\times2\times10^{-8}$ versus drain current for 21 nm thick film (75 g probe pressure). Curves are correlated with CNF model.*

In order to demonstrate that the top interface is responsible for the extra-noise, we added gold nano-particles of 5 nm diameter on the sample surface. These particles are expected to become gradually charged and to act as additional traps and/or fixed charges. A simple model accounting for the influence of gold particles on I_D (V_G) curves will be presented. Fig.6 shows the normalized PSD and $(g_m/I_d)^2$ curves for 70 g pressure. No correlation with CNF model is observed, at least at high drain current. Increasing pressure does not allow recovering the correlation. We will show that the correlation with the 'mobility fluctuation' model does not work either. The question about the dominant noise sources in ultra-thin films may be addressed by comparing SOI samples with passivated and unpassivated surfaces [6].

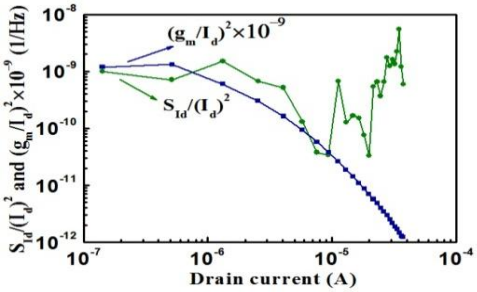

Fig.6: *Normalized PSD and $(g_m/I_d)^2\times10^{-9}$ versus drain current for gold decorated 20 nm film (pressure=70 g). No correlation is visible.*

4. Conclusions

We demonstrated the feasibility of noise measurements in virgin SOI wafers. In thick SOI films the noise follows the 'carrier number fluctuation' model which implies carrier trapping in BOX. The top surface acts as a source of very high noise and its importance is increased in ultra-thin films. Open questions are related to the accurate extraction of the trap density and to the impact of series resistances.

Acknowledgements
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Impact of mobility variation on threshold voltage extraction by transconductance change and g_m/I_d methods in advanced SOI MOSFETs

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1. Abstract

In this work, we investigate the effect of the gate-voltage-dependent mobility on the threshold voltage extraction by the transconductance change method and recently proposed g_m/I_D method, using analytical modeling, numerical simulations and experimental data obtained on SOI FinFETs and UTB SOI MOSFETs.

2. Introduction

Accurate and reliable determination of threshold voltage V_{TH} is of crucial importance for CMOS characterization and modeling. One of the most popular methods is the V_{TH}-determination by the transconductance change, i.e. from the peak position of d^2I_D/dV_g^2 vs gate voltage V_g, which is believed to be relatively insensitive to mobility and series resistance effects [1]. The threshold voltage criterion of this method is based on the maximum of the second derivative of the inversion charge or carrier density d^2N_{inv}/dV_g^2, which corresponds to the inflection point in the rate of the inversion charge growth. This seems to be particularly physically justified in case of MOSFETs with extremely thin gate dielectrics and undoped-body thin-film SOI MOSFETs, featuring gradual transition from weak to strong inversion.

Recently we have proposed another method for the V_{TH} extraction, namely, from the peak position of the $d(g_m/I_d)/dV_g$ function [2]. This method is based on the same V_{TH}-criterion; however, it is expected to be less sensitive to second-order effects, such as V_g-dependent mobility and series resistance effects, than the d^2I_D/dV_g^2 method. In this work, we derive analytical expressions for the shifts of the peak positions of d^2I_D/dV_g^2 and $d(g_m/I_d)/dV_g$ relative to the maximum of d^2N_{inv}/dV_g^2, caused by V_g-dependent mobility near threshold, and show that this deviation is much smaller for $d(g_m/I_d)/dV_g$ than for d^2I_D/dV_g^2. Experimental test is performed on long-channel SOI FinFETs and UTB SOI MOSFETs.

3. Analytical modeling

We define the threshold voltage V_{TH} as the gate voltage at which d^2N_{inv}/dV_g^2 exhibits a maximum, that is, when $d^3N_{inv}/dV_g^3=0$. Below we demonstrate that, in the case of mobility μ variation with V_g around threshold, the peak position of d^2I_D/dV_g^2 does not coincide with that of d^2N_{inv}/dV_g^2. For simplicity, we assume a linear $\mu(V_g)$ dependence around $V_g=V_{TH}$:

$$\mu(V_g) = \mu_0 + b(V_g - V_{TH}) \quad (1)$$

where μ_0 is mobility value at $V_g=V_{TH}$ and b is the rate of mobility variation at threshold. In this case, the drain current I_D at low drain voltage V_D can be computed as:

$$I_D(V_g) = q\frac{W}{L}\cdot V_D \cdot \left[\mu_0 + b\left(V_g - V_{TH}\right)\right]\cdot N_{inv} \quad (2)$$

where W and L are channel width and length respectively. Differentiating (2) with respect to V_g, we obtain:

$$\frac{d^3I_D}{dV_g^3} = qV_D\frac{W}{L}\left(3b\cdot\frac{d^2N_{inv}}{dV_g^2} + \mu\cdot\frac{d^3N_{inv}}{dV_g^3}\right) \quad (3)$$

At $V_g=V_{TH}$, where d^2N_{inv}/dV_g^2 reaches maximum value and $d^3N_{inv}/dV_g^3=0$, (3) results in:

$$\left.\frac{d^3I_D}{dV_g^3}\right|_{V_g=V_{TH}} = 3qV_D\frac{W}{L}b\cdot\left.\frac{d^2N_{inv}}{dV_g^2}\right|_{\max} \quad (4)$$

From (4) it follows that for $b\neq0$ at $V_g=V_{TH}$, $d^3I_D/dV_g^3\neq0$, which means that the peak position of d^2I_D/dV_g^2 does not coincide with V_{TH} (i.e. the peak position of d^2N_{inv}/dV_g^2): for $b>0$ it lies above V_{TH}, while for $b<0$ it is below V_{TH}. The quantitative assessment of the shift of the peak position of d^2I_D/dV_g^2 has been performed by considering a triangular formed by the tangent to the d^3I_D/dV_g^3 curve at the point $V_g=V_{TH}$ (Fig. 1) and using the unified charge control model [3]. The resulting expression for this shift is:

$$\Delta V\left[\max I_D^{"}\right] = \frac{3^4}{2^3}\cdot(\eta V_T)^2\cdot\frac{b}{\mu_0} \quad (5)$$

where η is the body factor and V_T the thermal potential.

Using similar approach, we calculated the shift of the peak position of $d(g_m/I_d)/dV_g$:

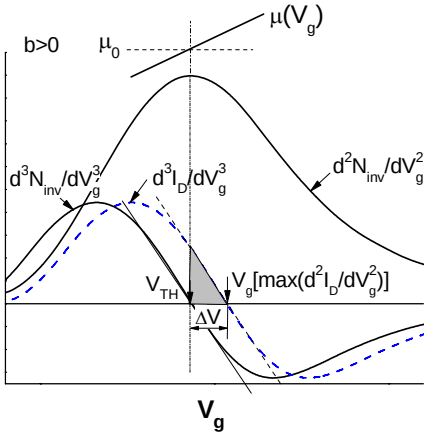

Fig.1: *Illustration of the shift of d^3I_D/dV_g^3 relative to d^3N_{inv}/dV_g^3 in the case of the V_g-dependent mobility (b>0)*

$$\Delta V[\max(-g_m / I_D)'] = -\frac{(b/\mu_0)^3}{\left(\frac{2^4}{3^6}\right)\frac{1}{(\eta V_T)^4} - 3\left(\frac{b}{\mu_0}\right)^4} \quad (6)$$

It is interesting that for both d^2I_D/dV_g^2 and $-d(g_m/I_d)/dV_g$ $\mu(V_g)$-induced shifts depend only on the ratio of the rate of mobility variation to its value at threshold b/μ_0.

Table 1 presents the comparison of the expected $\mu(V_g)$-induced shifts for d^2I_D/dV_g^2 and $-d(g_m/I_d)/dV_g$ at room temperature for different b/μ_0 ratios and η=1. It is evident that for the same b/μ_0, the shift for $d(g_m/I_d)/dV_g$ is much smaller (by 1.5-2 orders) than for d^2I_D/dV_g^2 and lies within reasonable experimental errors.

Table 1

b/μ_0	1	2	3	5
ΔV [max I_D''], (mV)	6.7	13	20	34
ΔV[max$(-g_m/I_D)'$], (mV)	-0.02	-0.16	-0.55	-2.6

4. Experimental results

To check experimentally the above findings, we compared the results of d^2I_D/dV_g^2 and $d(g_m/I_d)/dV_g$ methods, applied to advanced SOI devices, with results of the gate-to-channel capacitance derivative (dC_{gc}/dV_g) method [3], which is not affected by mobility variations. Fig. 2 presents such comparison for a 10 μm-long N-channel FinFET, and Fig. 3 presents similar comparison for UTB SOI MOSFET. Both types of the devices feature ultra-thin high-k gate dielectrics, so that one can expect mobility increase with V_g around V_{TH}, i.e. at low N_{inv}, where mobility is controlled by Coulomb scattering at interface charges [4,5]. This means that b>0 should be expected. For both types of the devices, dC_{gc}/dV_g and $d(g_m/I_d)/dV_g$ methods yield very close V_{TH} values, as expected from the above developments, while the d^2I_D/dV_g^2 method yields a higher V_{TH} value, namely, by ~27 mV in Fig. 2 and ~35 mV in Fig. 3 at V_D =10mV.

According to the previous analysis, such discrepancy between d^2I_D/dV_g^2 and dC_{gc}/dV_g methods, suggesting b/μ_0 ~ 4-5, can be attributed to mobility rise with V_g near threshold due to Coulomb scattering.

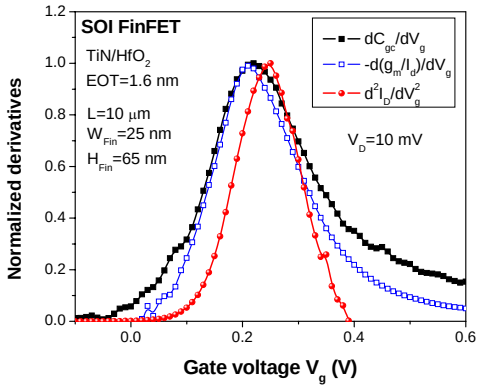

Fig.2: *Comparison between dC_{gc}/dV_g, d^2I_D/dV_g^2 and $d(g_m/I_d)/dV_g$ methods for 10 μm-long N-channel SOI FinFET*

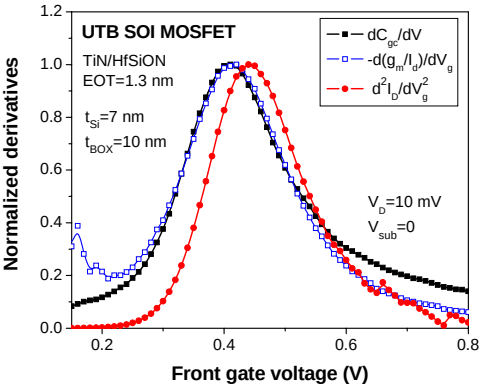

Fig.3: *Comparison between dC_{gc}/dV_g, d^2I_D/dV_g^2 and $d(g_m/I_d)/dV_g$ methods for N-channel undoped UTB SOI MOSFET (W=10 μm, L=10 μm)*

5. Conclusions

Analytical expressions for the shifts of the peak positions of d^2I_D/dV_g^2 and $-d(g_m/I_d)/dV_g$ relative to that of d^2N_{inv}/dV_g^2, induced by mobility variation around threshold, have been derived. Along with experiments, the study demonstrates that, for the same mobility variation, the resulting error on V_{TH} extraction is much smaller for $d(g_m/I_d)/dV_g$ than for d^2I_D/dV_g^2.

Acknowledgements

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Impact of Gate Voltage on Hysteresis Effect in 0.13µm Floating-Body PD SOI n-MOSFETs

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1. Abstract

The hysteresis effect dependence on V_{GS} is studied in the transient output characteristics. In this study, it is firstly found that the hysteresis effect enhances as V_{GS} stepping from 0 V to 0.86 V, but drops as V_{GS} increased to larger value. The depletion layer forced majority carriers' redistribution and impact ionization occurring at different V_{DS} cause the charging/discharging in the floating body, which leads to the unique dependence of the hysteresis effect on V_{GS}.

2. Devices Technology

The PD SOI n-MOSFETs used in the study are fabricated in a 0.13-µm SOI processing using STI isolation scheme, a 1.8-nm nitrided gate oxide, a 130-nm polysilicon gate, and 70-nm nitride spacers. The Processing was performed on 200-mm UNIBOND wafers, resulting in a top Si film thickness of 100 nm. The buried oxide (BOX) thickness was 145 nm. All experimental curves were measured using an Agilent 4156 semiconductor parameter analyzer.

3. Results and Discussions

Figure 1 shows the transient I_{DS}-V_{DS} characteristics of PD SOI n-MOSFET after V_{DS} forward and reverses sweeps with the delay time setting at 0 s [1]. Positive and negative $I_{DS\text{-}hysteresis}$ can be observed at low and high V_{DS}. Gate direct tunneling and impact ionization induced slow generation-recombination process leads to the hysteresis effect which is discussed in another abstract submitted to EUROSOI. It is also found

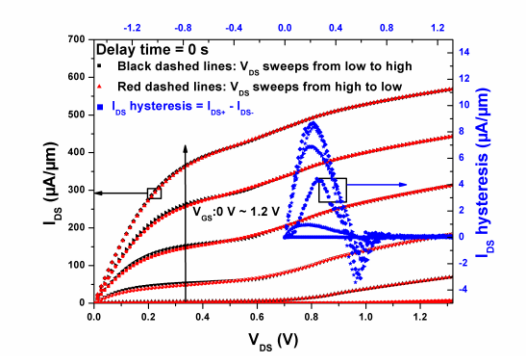

Fig. 1: *Left Y-axis: I_{DS}-V_{DS} characteristics of 0.13-µm core floating-body PD SOI n-MOSFET with delay time setting at 0s; Right Y-axis: Transient $I_{DS\text{-}hysteresis}$ characteristics of 0.13-µm floating-body PD SOI n-MOSFET, I_{DS} hysteresis is de$_{fined\ a}$s: I_{DS} hysteresis = I_{DS+}-I_{DS-}, I_{DS+} and I_{DS-} stand for I_{DS} of V_{DS} forward and reverse sweeps, respectively.*

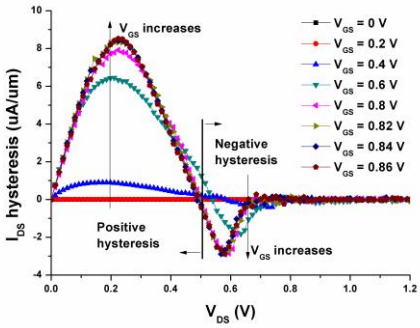

Fig. 2: *Transient $I_{DS\text{-}hysteresis}$ characteristics when V_{GS} steeps from 0 to 0.86 V.*

that the dependence of hysteresis effect on V_{GS} in the output characteristics. As can be seen in the Fig. 2, both the positive and negative hysteresis behavior becomes more obvious as the V_{GS} steppes from 0 to 0.86 V. And the hysteresis behavior comes down when V_{GS} continue to step to 1.2 V as shown in Fig. 3.

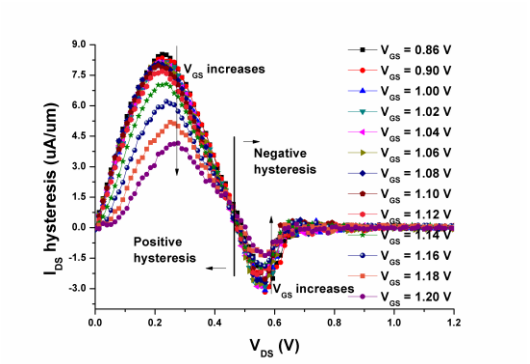

Fig. 3: *Transient $I_{DS\text{-}hysteresis}$ characteristics when V_{GS} steeps from 0.86 V to 1.2 V.*

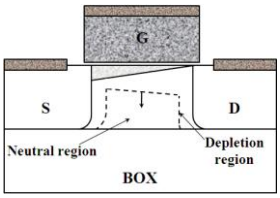

Fig. 4: *Dynamic floating-body effects due to majority carrier redistribution when V_{GS} increases.*

For the positive I_{DS} hysteresis behavior, the channel depletion layer grows wider when V_{GS} changes from low to high level, driving away holes to accumulation in the neutral region as shown in Fig. 4 [2]. This process enhances the floating-body potential that leads to more positive hysteresis effect. As V_{GS} increase to a certain value, the depletion layer wouldn't grow any more. So no holes can be generated by the forced depletion formation. However, when V_{GS}–V_{TH} < V_{DS}, transistor operates under the saturation mode [3]. As shown in Fig. 5, when V_{GS} increases, transistor operates from saturation mode to linear mode. And thus the drain-body depletion layer constricts. The floating-body potential drops due to the holes supplied to constrict the drain-body depletion layer, causing the hysteresis effect comes down.

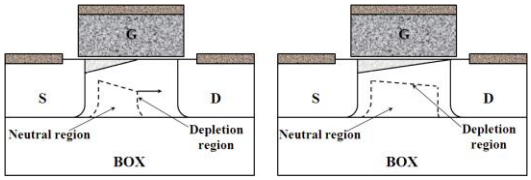

Fig. 5: *Contraction of depletion layer induced majority carrier redistribution at fixed V_{DS} when V_{GS} increases. Left: saturation-mode. Right: linear-mode.*

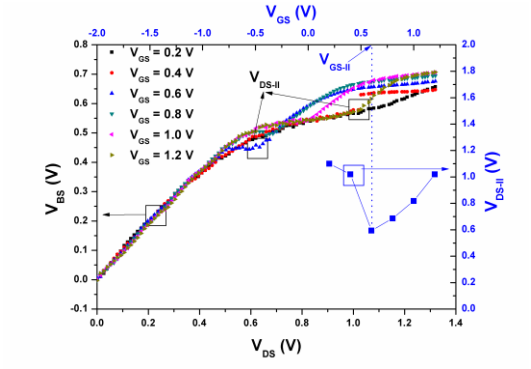

Fig. 6: *Left: Body-source voltage vs. V_{DS} of body contact structure. Right: Extracted $V_{DS\text{-}II}$ vs. V_{GS}.*

For the negative hysteresis behavior, the similar hysteresis behavior change can also be observed. As shown in Fig. 6, $V_{DS\text{-}II}$ that is defined as V_{DS} when impact ionization becomes to be obvious, decreases at first and then increases as the increase of V_{GS}. And the V_{GS} turning point is labeled as $V_{GS\text{-}II}$. When the V_{GS} is biased at $V_{GS\text{-}II}$, the $V_{DS\text{-}II}$ is the smallest. So as the V_{DS} reverse sweeps, impact ionization keeps in high level in a wider V_{DS} range for the case of $V_{GS\text{-}II}$, which contributes more holes to the floating body, and that leads to the most obviously hysteresis effect. Then, that's why the hysteresis effect comes down for the case of lower or higher V_{GS}.

4. Conclusions

The hysteresis effect dependence on V_{GS} is experimentally investigated for the output characteristics of PD SOI n-MOSFETs. The majority carrier redistribution due to depletion layer variation as V_{GS} increases causes the V_{GS} dependence of the positive hysteresis effect. On the other hand, as the increase of V_{GS}, impact ionization lasting in different V_{DS} ranges causes different amount of holes injection into the floating body, which leads to the V_{GS} dependence of the negative hysteresis effect.

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Session 2: Memories

Chair: Malgorzata Jurczak

A2RAM: Novel dual-body 1T-DRAM cell on ultrathin SOI

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1 . Introduction

1T-DRAMs are attractive for replacing the conventional DRAM where the scaling of the storage capacitor is a critical issue [1-3]. Floating Body (FB) 1T-DRAMs use electrons and holes coexisting in the same body. This coexistence becomes impossible in ultrathin films [4] (necessary for ultimate CMOS scaling) due to the supercoupling effect [5]. We propose a different approach: a multi-body 1T-DRAM which ensures scalability thanks to a dedicated body partitioning by a PN junction.

2. The dual body concept and operation

The cell architecture is shown in Fig.1a. A fully depleted SOI-MOSFET is modified by connecting the N^+ source and drain through a buried N-type layer (*N-bridge*). Typical total thickness is in the rage of 15-20 nm. Note that this cell is different from the recently proposed multi-body A-RAM cell which features an intermediate dielectric layer (MOX) [6] (Fig. 1b).

The device introduces a new concept with respect to the conventional 1T-DRAM cells [7]. The top body, lightly P-type doped, is used as the storage node, whereas the bottom body (N-bridge: highly N-type doped) is used for current sensing. When the upper body is charged with holes (generated by band-to-band tunneling (BTB) or impact ionization (II), and retained with a negative gate bias), the vertical field is screened by the top hole accumulation layer (Fig. 2a) and cannot deplete totally the N-bridge. If V_D is increased, electron current flows through the neutral region of the N-bridge (state '1', Fig.2b). No current flows through the P-body. When the top body is discharged of holes, the gate field is no longer screened and fully depletes the N-bridge ('0' state, Fig.2c): when the cell state is read by increasing V_D, the resulting drain current becomes very low (Fig.2d). The thickness of the N-bridge can be selected according to Fig. 3. This memory window guarantees high '1' state current and simultaneously achieves full depletion of the N-bridge during the '0' state.

The potential of the device as memory cell is demonstrated from the I_D-V_G hysteresis curve (Fig. 3). If V_G is scanned forward to a high voltage value (A→B), the holes are removed from the storage node by forward biasing the source and drain junctions (capacitive coupling; the top body operates as an N-MOSFET). Scanning backward the gate voltage (B→C), makes the electrostatic potential to fall due to the lack of holes (there is no immediate source to supply them); the N-bridge becomes depleted and the current decreases by several orders of magnitude. Further decrease in the gate voltage (C→D) generates holes by BTB tunneling, screening again the gate electric field, undepleting the *bridge* and increasing the current to reach the '1' state stable level.

Pragmatic bias conditions for 1T-DRAM operation of the cell are shown in Table 1. These signals are applied in a sequence (Fig. 5) demonstrating the complete 1T-DRAM operation of the cell. As observed, only the reading of the '1' state leads to a substantial drain current. We will show that the cell can be optimized to present negligible '1' state writing current by embedding the gate pulse into the drain pulse during the writing process.

The electron and hole concentration after writing the '1' and '0' states in Fig. 5 are show in Fig. 6. The difference in accumulated charge (holes) reaches two order of magnitude at the gate-interface, and more than six orders in the middle of the P-body, whereas the electron concentration varies by about three orders of magnitude between '1' and '0' states, which basically corresponds to the three orders of magnitude that are obtained for the current ratio I_1/I_0 in Fig. 5. This dramatic current margin with such an ultrathin device is observed also from the 2D-current density (Fig. 7) when reading the '1' and '0' states. It can be noticed that the supercoupling effect is effectively suppressed thanks to the junction partitioning: the electrons and holes are cohabitating in a stunning 18nm thick device.

The retention time of the cell has been studied at 85ºC (Fig. 8). The '1' state is always stable (even if the initial hole density injected by BTB tunneling is larger than the value sustained by the negative V_G, the equilibrium is reached rapidly). The '0' state is unstable since several generation mechanisms (thermal generation, junction leakage, GIDL) contribute to repopulate the top P-body with holes. A non-optimized device shows a retention time in the order of 2µs (limited by BTB tunneling). However, a simple 3nm underlap gate can increase the retention time to 120µs. Further optimization regarding the source/drain doping profiles and gate overlap regions can increase the retention time in the rage of several hundreds of miliseconds.

3. Conclusions

The new concept of 1T-DRAM cell features N/P body partition which enables the electrical and physical separation of hole storage and electron current. The hole concentration controls the partial or full depletion of the N-body. The cell is compatible with ultimate scaling and shows attractive performance (long retention, wide memory window, simple programming, nondestructive reading, and low power operation) for embedded systems on SOI.

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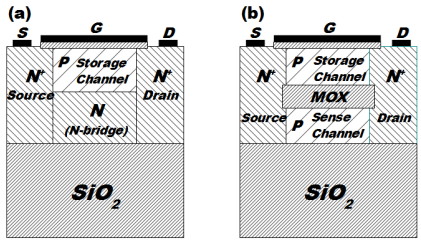

Fig. 1: *(a) Schematic configuration of the dual-body A2RAM; (b) Previously proposed A-RAM cell.*

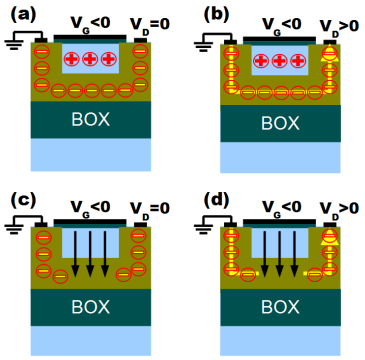

Fig. 2: *A2RAM operation principle.* ***(a)*** *Retention '1' state.* ***(b)*** *Reading '1' state (high drain current).* ***(c)*** *Retention after writing '0' by evacuating the holes: unscreened gate field.* ***(d)*** *Reading '0' state (no drain current).*

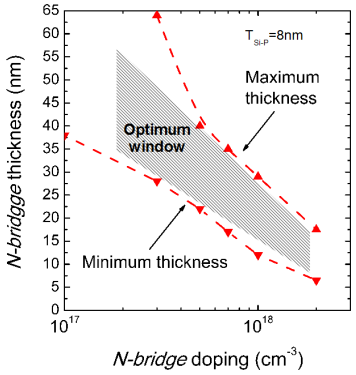

Fig. 3: *Cell design window. Typical maximum and minimum values of the N-bridge thickness versus doping needed to achieve a current margin I_1/I_0>100. P-body thickness is 8nm.*

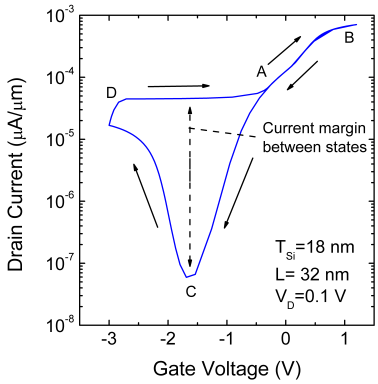

Fig. 4: *Numerical simulation of I_D-V_G curve demonstrating A2RAM hysteresis. The loop has been completed in 10µs. T_{OX}=2nm, $T_{Si\text{-}P}$=8nm, $T_{Si\text{-}N\text{-}bridge}$=10nm, L=32nm, T_{BOX}=82nm.*

	Write '1'	Write '0'	Hold	Read
V_{GATE}	-3V(BTB)/ 1V(I.I.)	1 V	-1.2V...-1.5V	-1.2V...-1.5V
V_{DRAIN}	1.2 V	0 V	0 V	0.1 V
V_{SOURCE}	0 V	0 V	0 V	0 V

Table. 1: *Bias example for 1T-DRAM operation*

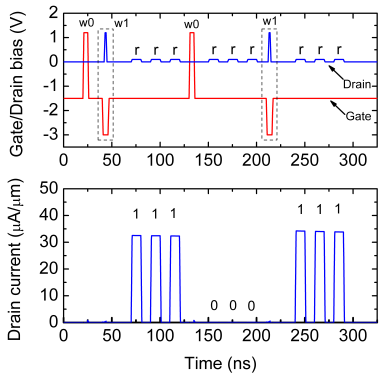

Fig. 5: *Simulation waveforms demonstrating A2RAM functionality. Drain and gate signals during operation (top). Read drain current (bottom). T_{OX}=2nm, $T_{Si\text{-}P}$=8nm, $T_{Si\text{-}N\text{-}bridge}$=10nm L=32nm, T_{BOX}=82nm.*

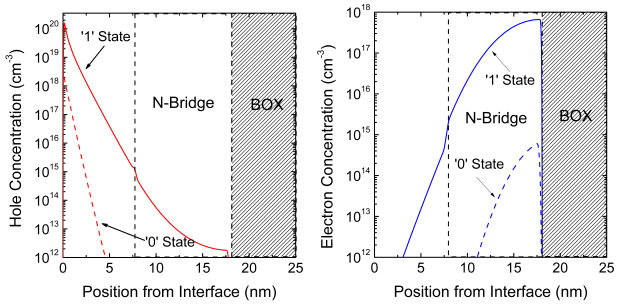

Fig. 6: *Hole (left) and electron (right) concentrations 10ns after writing the '1' and '0' states in the device of Fig. 5.*

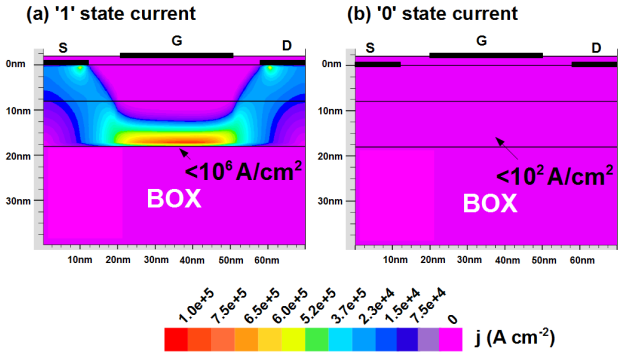

Fig. 7: *2D-electron current density while reading the '1'* ***(a)*** *and '0'* ***(b)*** *states in the device of Fig. 5. V_D=0.1V.*

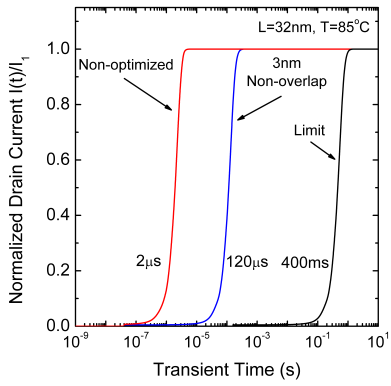

Fig. 8: *Evolution of the '0' state current (worst case models) under continuous reading operation (V_D=0.1V, V_G=-1.5V, T=85°C). A 3nm gate underlap increases the retention time by a factor of 50. The theoretical retention time limit from the simulations is about 400ms.*

Scaling of SOI FinFlash Memory with Buried Storage ONO Layer

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1. Abstract

Advanced FinFETs fabricated on alternative SOI substrate with high-k, SiO_2-Si_3N_4-SiO_2 (ONO) buried insulator are investigated for non-volatile memory applications. The back threshold variation, ΔV_{THB}, induced by trapped charges in the Si_3N_4 layer can be used as memory effect. Systematic measurements reveal the memory window size as a function of bias, geometrical parameters and measurement conditions.

2. Introduction

The usual non-volatile flash memory cells are based on the charge storage in a floating gate. The trapping medium and the conduction channel are located within the same gate. For the next technology nodes, the scaling of the cells down to 22 nm will bring in several issues linked to the channel length and the tunnel oxide thickness reduction, which will deteriorate the cell reliability especially the retention time. The use of programming bias compatible with logic applications is another important matter. The actual flash memory technology requires minimum programming voltage of 8 V [1] which induces additional cost for the co-integration. For these reasons, the oxide/nitride/oxide (ONO) flash cells, where the nitride is used to store the charge have been developed. The ONO process simplicity and the improved retention characteristics due to the deep trap levels of the nitride allow to enhance the integration density and reduce the program/erase voltages. In the recent years, several ONO concepts have been proposed to push the scaling limits of the conventional non-volatile cells further, like ONO FinFlash [2], ONO nanowires [3] or back-gate storage flash cells [4,5] etc.

In this paper, the scaling effects on the charging efficiency and the retention capability will be studied for FinFET devices implemented on ONO buried insulator.

The key advantage of this device is that the same cell can be used either for analog/logic or memory applications due to the decoupling of the storage and read operations. Carrier trapping occurs in the ONO buried dielectric whereas the read current is controlled by the front gate. The basic mechanism has been recently presented [6].

As a result, the front-gate oxide thickness can be scaled down following the technology design rules and, at the same time, the immunity against short-channel effects is granted when the transistor works at low bias, still providing effective read operation in the memory mode. The experimental results will be reported for gate length and width down to 90 nm and 55 nm, respectively. The influence of the history effects on the "normal" analog/logic FinFET behavior will be also discussed.

3. Device Structure

The nitride/oxide/nitride multi-layer buried oxide was used as starting material. Wafers with ONO buried insulator were fabricated using the Smart-Cut™. The 2.5 nm (SiO_2), 20 nm (Si_3N_4) and 70 nm (SiO_2) layers were stacked under the silicon film. Si_3N_4 is a suitable material for flash memory, but the Si-Si_3N_4 interface degrades the transistor performance [7]. This is why, the Si_3N_4 layer was surrounded with two SiO_2 layers. The Si film thickness (65 nm) defined the Fin height. Hydrogen annealing was performed to smooth the Fin sidewalls. The gate oxide thickness grown by wet oxidation was 1.8 nm and TiSiN grown by LPCVD was used as gate material. To investigate the geometrical effects, FinFETs with variable fin width and gate length were prepared. Fig. 1 shows the structure of the SOI FinFETs fabricated on the ONO buried layer.

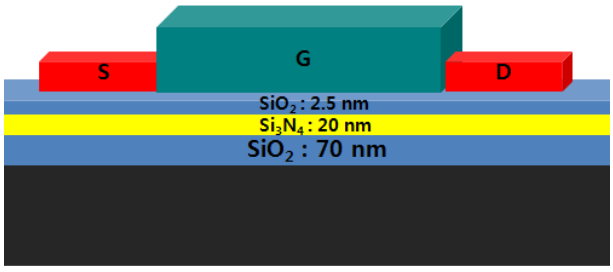

Fig 1: *Structure of the SOI FinFET with ONO buried insulator. The thickness of buried insulator is 2.5 nm (SiO_2), 20 nm (Si_3N_4) and 70 nm (SiO_2).*

4. Results and Discussions

The non-volatile charges (*i.e.* electrons) are trapped/detrapped into/from the nitride (Si_3N_4) layer by applying a high back-gate bias. The charge injection mechanism is Fowler-Nordheim tunneling [1]. First, the influence of the front-gate bias and the geometrical parameters on the nitride charging efficiency will be discussed. The effectiveness of the memory mechanism is related to the hysteresis, *i.e.*, to the back threshold variation ΔV_{THB} which can be observed when the back-gate voltage is swept back and forth inducing trapping and detrapping of electrons.

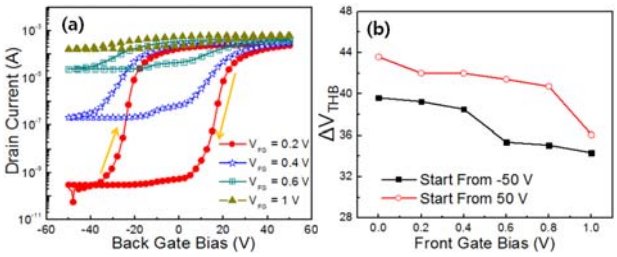

Fig. 2: *(a) Drain current hysteresis as a function of back-gate bias for variable front-gate bias. (b) ΔV_{THB} as a function of front-gate voltage and starting bias value. V_D = 0.1 V, W_F = 90 nm, L_G = 1 µm, N_F = 100.*

Fig, 2 shows the effect of front-gate bias on drain current. As the front-gate bias increases, the controllability of the front channel is enhanced. Hence, for higher front gate bias, the drain current level increases but, at the same time, the lateral gates tend to block the back-surface potential. Consequently, the impact of the trapped charge is reduced and ΔV_{THB} decreases leading to a lower programming efficiency.

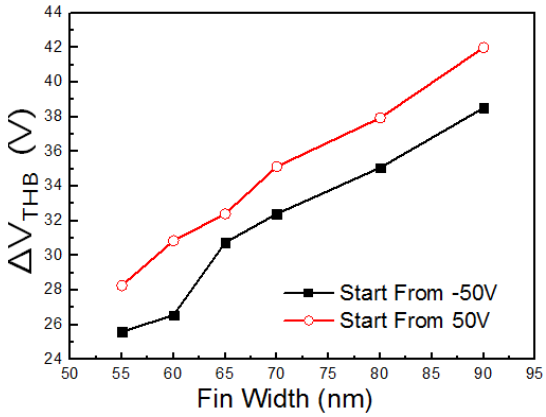

Fig. 3: *The effect of fin width on the back threshold variation, ΔV_{THB} (30 sec hold time). V_D = 0.1 V, V_{FG} = 0.4 V, L_G = 1 µm, N_F = 100.*

The back threshold variation, ΔV_{THB}, also depends on the geometrical parameters such as gate length and fin width. In narrow FinFETs, the fringing field from the lateral gates controls more effectively the film-BOX interface and again ΔV_{THB} decreases. Fig. 4 shows the effect of the channel length on the ΔV_{THB}. The most striking feature is the ΔV_{THB} increase when the channel length is scaled down below 200 nm. This phenomenon is also explained by 3D coupling effects [8]. For shorter device, the longitudinal coupling component induced by drain bias enhances the back-gate efficiency. The longitudinal fringing field from drain and source through the BOX opposes the gate action, enabling more impact from the stored charge.

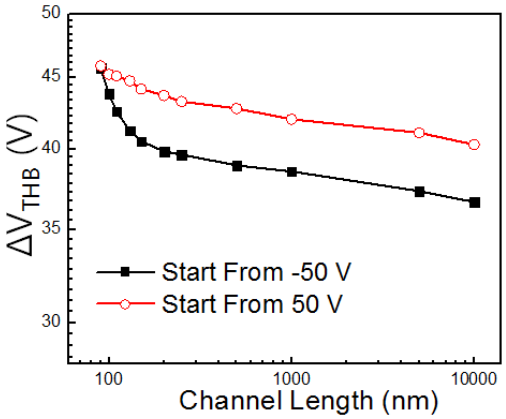

Fig. 4: *The effect of channel length on the back threshold variation, ΔV_{THB} (30 sec hold time). V_D = 0.1 V, V_{FG} = 0.4 V, W_F = 90 nm, N_F = 100.*

In Fig. 2(a), a drain current hump is observed when the back gate is swept from 50 V to -50 V. We will show that the hump results from a non-equilibrium parasitic channel related to carrier trapping-detrapping process.

5. Conclusions

In this paper, FinFETs on ONO buried insulator have been considered for achieving nanoscaled memory cells. A large ΔV_{THB}, the memory window, is induced by the trapped charges in the Si_3N_4 layer. The size of ΔV_{THB} depends on the bias condition and geometrical parameters. These results can be applied for flash memory devices according to the concept of the 'unified' memory.

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ULP Variability-Insensitive SRAM Design in sub-32nm UTBB FDSOI CMOS

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1. Abstract

This paper describes a design approach based on optimization of embedded SRAMs that takes advantage of an Ultra-Thin Body and Box (UTBB) Fully-Depleted (FD) SOI CMOS process. Optimization is performed on an analytical model including statistical variations for Static Noise Margin (SNM) of CMOS SRAMs operating in subthreshold. Distributions of retention and read SNM are derived as a function of V_{TN} and V_{TP}. Improvements of up to 2x of the retention- and read-mode SNM μ/σ are obtained by optimizing the V_{TN}/V_{TP} ratio with back bias.

2. Introduction

In today's systems-on-a-chip (SOC) very often most of the chip area is taken by embedded SRAM, which leads in some cases to the leakage power to dominate the overall power consumption. Therefore, for low-power design, suppressing leakage current becomes crucial. The solution adopted in this work to the leakage problem is sub-threshold operation; this solution is particularly attractive, as lowering supply voltage does not only reduce the leakage in retention, but also reduces dynamic power consumption in active mode. Previous work on this subject was presented in [1], where a model for sub-threshold SNM evaluation for 45nm CMOS is presented and in [2], where it is extended for the purpose of evaluating optimum SRAM operation conditions in read and retention modes. In this work sub-threshold variability-resistant SRAM design is investigated further by taking advantage of an UTBB FDSOI process [3] with reduced-parameter variability and increased body factor. The stability of large SRAM arrays is characterized taking into account the statistical variations of device parameters, evaluating the optimum V_T ratios for best yield and the backgate bias to achieve this optimum.

3. UTBB FDSOI

The UTBB-FDSOI device [3] (Fig.1) consists of an undoped Silicon thin film on a thin Buried Oxide (BOX) layer of thickness T_{BOX} ($10nm<T_{BOX}<30nm$) covering a highly doped Back Plane (BP) (Fig.1). Reducing the BOX thickness and doping the BP (i) boosts the channel electrostatic control (ii) gives the possibility of obtaining a V_T modulation by applying different kind of BP doping using a single gate stack work function and (iii) results in a very high body factor for V_T adjustment, reaching more than 100mV/V for T_{BOX} = 10 nm.
Dopant variations are the most important factor in process variations in CMOS bulk devices. Since in this technology the thin film is undoped and the V_T is modified through the application of a different BP and/or body bias, the standard deviation σ_{VT} is expected to be almost half that of typical bulk with an A_{VT} below 1.4mVμm [4]. An additional feature is the availability of multiple V_Ts, such as high-V_T (HVT), standard-V_T (SVT) and low-V_T (LVT).

4. Static Noise margin

Static noise margin (SNM) is the key parameter for SRAM cells and was first introduced in [5]. It can be described as the biggest value of noise voltage between both inverters in a 6T memory cell (Fig. 2), for which the cell can still retain its data, graphically represented in Fig. 3 as the smallest of the two largest possible squares that can fit between the "butterfly curves"; these are obtained from a direct and an inverse voltage-transfer curve (VTC) of each cell inverter. The VTCs that go between V_{DD} and 0 represent the cell in retention, and the other two VTCs are for the cell in read mode (access transistors are included).
The SNM model is implemented in Matlab and applied to optimize yield by maximizing the $\mu/6\sigma$ of the SNM in the presence of local V_T variation of $\pm 3\sigma$.

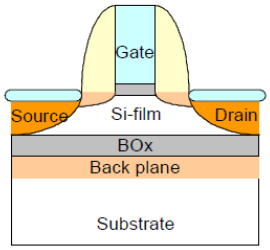

Fig.1 *UTBB-FDSOI transistor cross section*

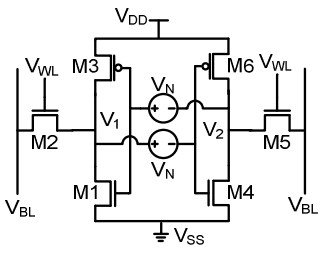

Fig.2 *SRAM cell with noise sources for SNM evaluation*

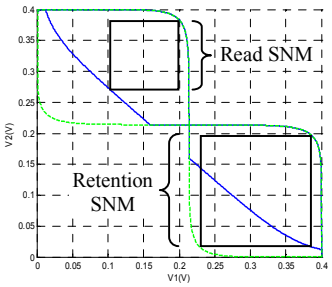

Fig.3 *Butterfly curves for read and retention operation obtained from Matlab*

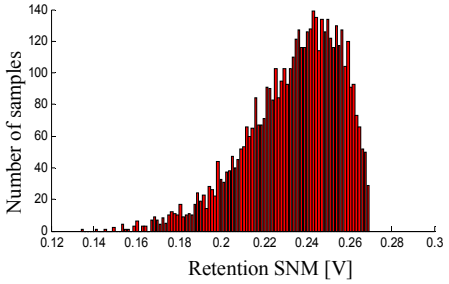

Fig.4 *Histogram representing retention SNM distribution*

5. Statistical Variation and Cell Optimization

Ideally, the SRAM array should meet the 6σ criterion, meaning that for any given process parameter variation, the mean of the SNM distribution divided by the standard deviation should be higher than 6. The focus of the analysis performed in this work is to increase the stability of a large SRAM-cell array by applying global and local parameter tolerances to the MOS transistor, and maximizing the ratio mean(μ)/σ of the derived SNM distribution by various techniques. V_{DD} can also be minimized when optimum operating conditions of the SRAM array are achieved by adjusting the V_T to the desired value using backgate bias.

A histogram of the SNM in retention for V_{DD}=0.6V, and NMOS and PMOS transistors with equal nominal $|V_{T0}|$ is plotted in Fig. 4. The SNM value and distribution depend on the V_{TN}/V_{TP} ratio. The shape of this plot can be explained by the fact that in retention mode having NMOS and PMOS transistors with the same $|V_{T0}|$, yields close to optimal SNM. Therefore, when random variation is applied, some samples will reach the highest possible SNM value (270mV vs. $V_{DD}/2$=300mV), hence the shape of the distribution is tilted towards these maximum SNMs (see Fig. 4). Fig. 5 and Fig. 6 show the μ/σ distributions of retention SNM at V_{DD}=0.3, and read SNM at V_{DD}=0.5, respectively, for various V_T values. It can be seen, that the optimum values of the N and PMOS V_Ts differ between the two plots requiring a compromise between best V_{TN}/V_{TP} ratios in retention and read, slightly below 1 and above 1.5, respectively.

Due to its high body factor, UTBB-FDSOI allows a wide range of V_T adjustment that can lead to an optimum. For the purpose of this analysis, we assume the UTBB-FDSOI transistor parameters from [3], where in a high-V_T configuration V_{TP}=-427mV and V_{TN}=604mV, and maximum applicable reverse and forward bias voltage values at V_{DD} and $V_{DD}/2$, respectively. These V_T values correspond to point A in Figs.5.b and 6.b. The position of this point shows that the retention μ/σ is less than 6; however, by applying body bias to both transistors we can modify V_{TP} and V_{TN} in the range of 100mV (Reverse) and 50mV (forward) respectively and thus, obtain a V_T ratio corresponding to point B, where μ/σ is almost 12 (2x stability gain). The initial V_T ratio (point A in Fig. 5 and 6) is almost optimal for read mode, but even higher stability and also faster read operation due to lower V_{TN} values, can be achieved by shifting V_T values to point C (see Fig. 6).

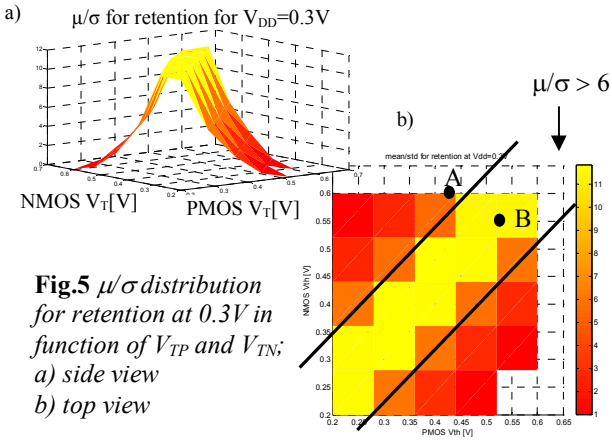

Fig.5 *μ/σ distribution for retention at 0.3V in function of V_{TP} and V_{TN}; a) side view b) top view*

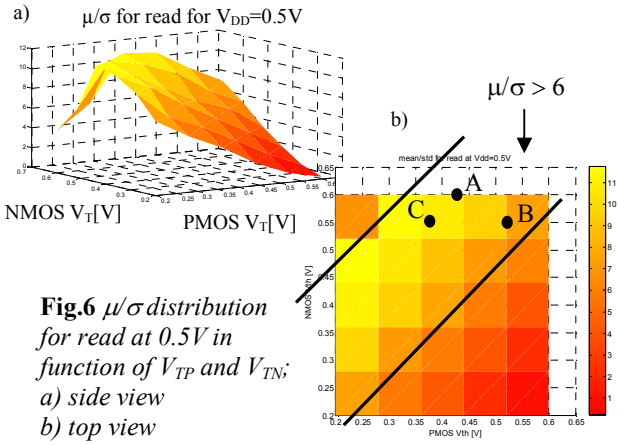

Fig.6 *μ/σ distribution for read at 0.5V in function of V_{TP} and V_{TN}; a) side view b) top view*

6. Conclusions

Due to a high body factor of UTBB-FDSOI it is possible to obtain up to 2x increase of μ/σ for retention and read. Appropriate body bias in each operation mode also allows setting a lower V_{DD} and can be adjusted on a post-processing basis. Analyzing the results one can notice, that the lines representing the crests of the 3D SNM plots are parallel, and a shift of $|V_{TP}|$ and V_{TN} by the same amount will not cause a change of μ/σ, as their ratio stays the same. Figs. 5 and 6, and the relations between points A, B and C, show that in order to provide the optimum stability in both read and retention operations the right value of the V_T ratio needs to be set.

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0.42-V 576-kb 0.15-µm FD-SOI SRAM with 7T/14T Bit Cells and Substrate Bias Control Circuits for Intra-Die and Inter-Die Variability Compensation

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1. Abstract

We propose 7T/14T FD-SOI SRAM with a substrate bias control mechanism. The 14T configuration suppresses intra-die variation in a bit cell. The substrate bias control circuits detect a threshold voltage and automatically change it with the substrate bias. Thereby, the inter-die variation is suppressed. By combining these two schemes, we confirmed that a 576-kb SRAM test chip in a 0.15-µm FD-SOI works at 0.42 V.

2. Introduction

In an SoC (system on a chip), SRAM occupies an area of 90% or more of a silicon die [1], meaning that SRAM is the most sensitive device to process variation. To make matters worse, read and write margins in a 6T bit cell are decreased with lowering a supply voltage. Fig. 1 (so-called Yamaoka plot [2]) illustrates it by relations between read/write limit lines and process corners. At an FS (SF) corner, SRAM has the least read (write) margin.

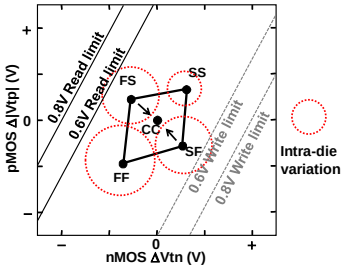

Fig. 1: *Yamaoka plot.*

3. 7T/14T SRAM with Substrate bias

To maximize the operating margin in SRAM, both of the inter-die and intra-die variations must be suppressed. As shown in Fig. 2, the FS/SF corner can be converged on the CC corner with an FD-SOI substrate bias [3], which means the suppression of the inter-die variation. In this paper, we apply this FD-SOI substrate bias control to a 7T/14T bit cell [4] in order to suppress the other component: the intra-die variation.

Fig. 3 portrays the 7T/14T bit cell that has two operating modes: normal mode and dependable mode. In the normal mode, a 7T bit cell stores one-bit information. In the dependable mode, a 14T bit cell combining a pair of 7T bit cells does so, too; however, it can suppress the intra-die variation. This is because a β ratio is doubled in a read operation, and a conductance of access gates are averaged in a write operation. The normal
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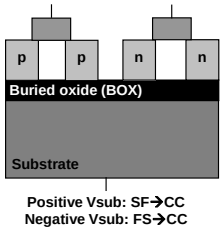

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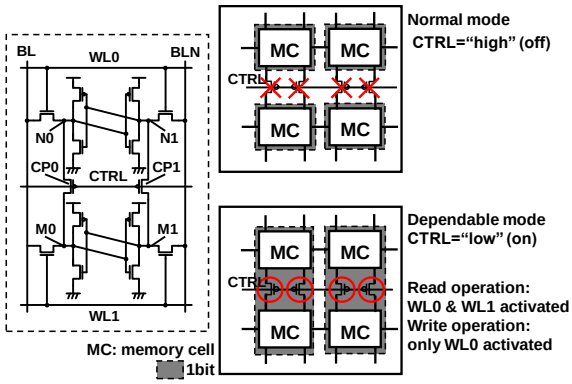

Fig. 3: *7T/14T bit cell.*

4. Circuit Implementation and Results

Fig. 5 is a micrograph of a 576-kb (512 rows × 8 columns × 16 bits/word × 9 blocks) 7T/14T SRAM test chip in a [redacted] substrate bias contr

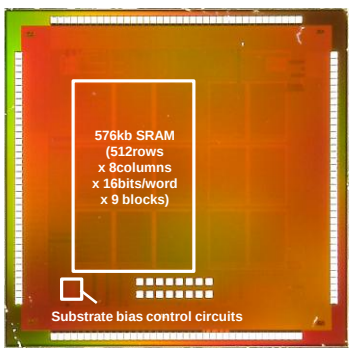

Fig. 4: *Test chip (FS corner).*

Fig. 5(a) shows a block diagram of the proposed substrate bias control circuits. Fig. 5(b) shows a Vt detector. "Detect" is an analog signal that changes from Vdd to the ground according to a process condition. Fig. 5(c) shows a half-Vdd generator using body-tie transistors. Respective "Ref+" and "Ref–" are set to slightly higher and lower voltages than a half Vdd, regardless of the process condition. The substrate bias (Vsub) is controlled so that "Detect" is always kept between "Ref+" and "Ref–". In this way, the FS/SF corners converge on the CC corner.

Fig. 6(a) expresses simulated output voltages of the Vt detector and half-Vdd generator when the process condition is varied. Fig. 6(b) depicts measured data obtained from the test chip around the FS corner. In this case, the proposed control circuits outputs a substrate bias of 3.4 V to suppress the inter-die variation.

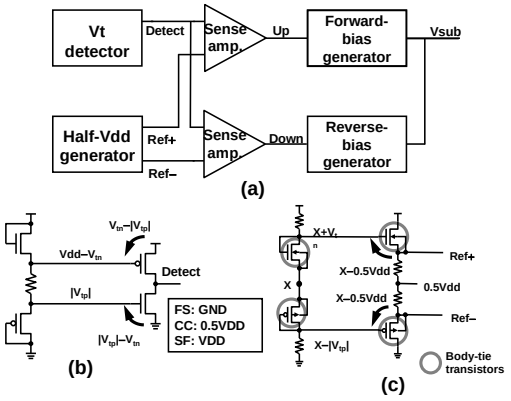

Fig. 5: *Proposed substrate bias control circuits: (a) block diagram, (b) Vt detector, and (c) half-Vdd generator.*

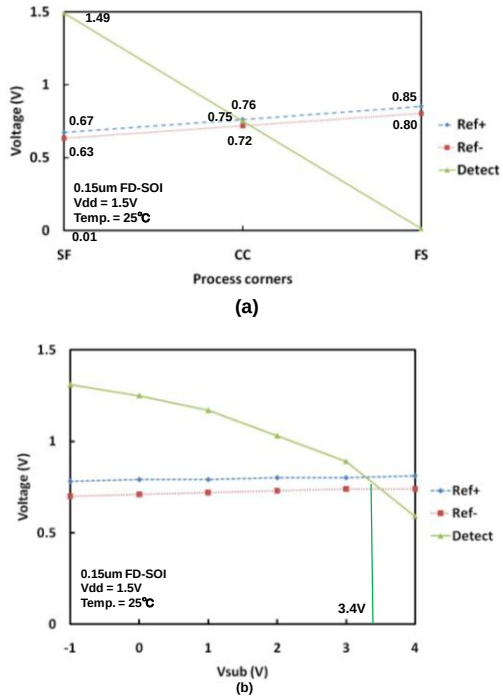

Fig. 6: *(a) Simulated and (b) Measured output voltages of Vt detector and half-Vdd generator.*

Although the retention voltage on the test chip is 0.43 V without the 14T configuration or substrate bias control, it can be lowered to 0.28 V with the two schemes (Fig. 7(a)). The operating voltage is also improved from 0.74 V to 0.42 V in the case where the intra-die and inter-die variability compensation is both treated (Fig. 7(b)).

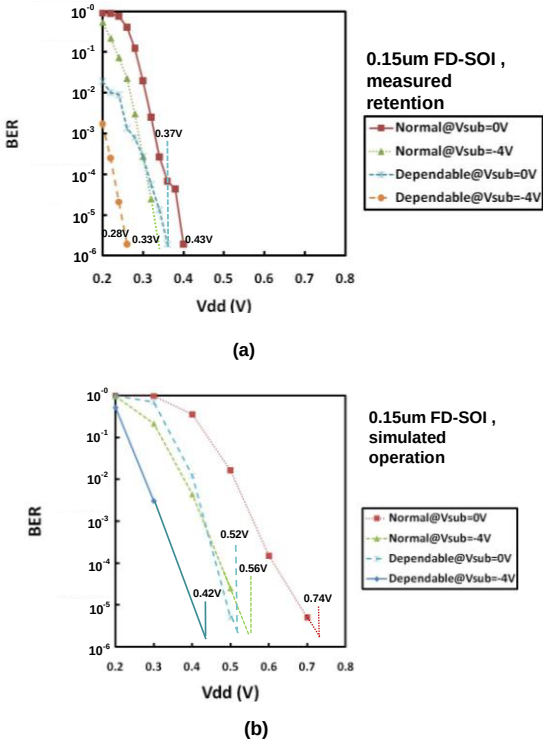

Fig. 7: *Bit error rates (BERs) in: (a) retention and (b) operation (read/write) on the test chip.*

6. Summary

We proposed 7T/14T FD-SOI SRAM with substrate bias control circuits. We confirmed that the 0.15-µm SRAM test chip can reduce the minimum retention and operating voltage to 0.28 V and 0.42 V, respectively.

Acknowledgments

This work was supported by KAKENHI (20360161). The test chip was fabricated by Oki Semiconductor Co., Ltd. We thank Dr. Satoshi Kuboyama with Japan Aerospace Exploration Agency (JAXA) for technical discussion.

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Session 3: Multigate Devices

Chair: Carlos Mazuré

Multi-Gate Voltage Selectable Silicon-Nanowire-FETs

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1. Abstract

In this paper, we report on the fabrication and characterization of voltage-selectable (VS) nanowire (NW) field-effect-transistor (FET) devices suitable to broaden the flexibility in logic circuit design. Silicon NW-structures with mid-gap Schottky S/D junctions on silicon-on-insulator (SOI) substrate were fabricated as unipolar MOSFETs. The versatility of our approach is demonstrated experimentally using a VS-NW-CMOS inverter circuit on a multi-SOI like set-up.

2. Introduction

Silicon nanowires are intensively investigated by many research groups and considered as promising replacement for standard MOSFET based transistor technology, since classic geometric downscaling of the MOSFET devices dimensions is approaching critical physical barriers and is reported to come to an end [1]. However, the ambipolar [2] nature of the nanowires turns out to be a roadblock, as p-type and n-type transistors are necessary basic building blocks for today's complementary MOS logic, i.e. its simplest device, the inverter [3]. Problems concerning fabrication and its compatibility to standard CMOS fabrication procedures [4] could be circumvented by the fabrication of unipolar nanowire devices, using Schottky-barrier contacts as source and drain metallization. Moreover, our devices behavior can be influenced by a control voltage, leading the way for switchable transistor characteristic changeable on the fly. Simple fabrication by means of well known silicon based top-down technology was used, forming the nanowire. Fig. 1. gives a schematic view of the device set-up on a MultiSOI substrate, however, simplifying prototype fabrication, split SOI substrates, are used.

2. Fabrication

Device fabrication is performed on ultrathin-body SOI substrates with a top-silicon thickness of 70nm, a buried oxide of 145nm and a boron doping level of ~10^{15}cm^{-3}. Preparation of alignment marks for the electron beam lithography (EBL) is followed by the patterning of a ~90nm wide fin into negative resist. The active area - i.e. a silicon fin - is then transferred into the top-Si via reactive ion etching, using a hydrogen-bromide based plasma. The gate oxide is formed by dry thermal

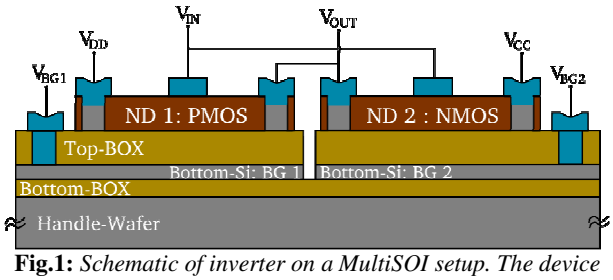

Fig.1: *Schematic of inverter on a MultiSOI setup. The device type, i.e. PMOS or NMOS, is simply selected via switching back-gate voltage polarity. For example by applying a negative back-gate voltage to back-gate 1 (BG1) a PMOS forms and by applying a positive voltage to back-gate 2 (BG2) an NMOS forms.*

oxidation at 1000°C in a tube furnace, resulting in a gate oxide thickness of ~8nm. Back-end processing is again performed via EBL, the S/D areas are opened by wet etching in hydrofluoric acid, contact pads and metallization are defined with a specifically designed double-layer lift-off resist system. Electron beam evaporation is used to deposit the mid-gap metallization consisting of 70nm nickel capped with 180nm of aluminum. The gate contact is defined likewise. A salicidation annealing at 500°C for 5 minutes finalizes the fabrication. During this forming gas treatment, the nickel reacts with the silicon NW forming a mid-gap Schottky-barrier contact [5] to the lowly doped silicon nanowire. By means of process metrology via AFM, SEM and high resolution cross-section SEM (XSEM) a NW-channel width of ~85nm and a channel height of 60nm is characterized (not shown).

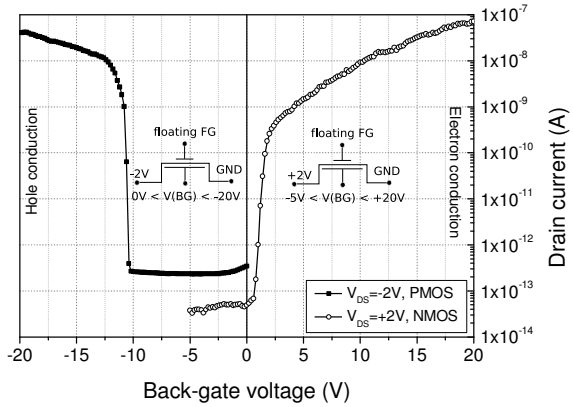

Fig.2 *Back-gate (BG) voltage sweep of NW-FET at open front-gate (FG) conditions. Squares represent hole conduction, as in PMOS FETs, circles electron conduction like in NMOS FETs. It is clearly seen that the charge carrier type changes with interchanged back-gate bias.*

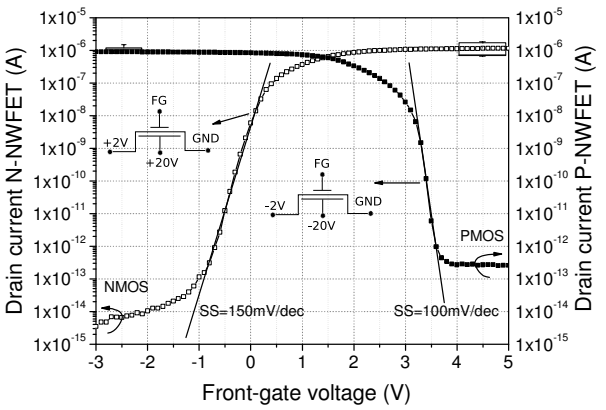

Fig.3: *Subthreshold characteristic of a VS-NW device at two contrary back-gate biasing conditions of $V_{BG1,2}$ = ±20V at drain biases of V_{DS} = ±2V. Filled symbols represent PMOS-like behavior, i.e. hole conduction, open symbols represent NMOS-like behavior, i.e. electron conduction.*

Note, that during the entire fabrication no doping is required, making this process independent of several issues arising in modern MOSFET fabrication like statistic dopant fluctuation, rising process complexity as from the necessity of using lightly doped drains, halo implantations and more.

3. Results and Discussion

Fig. 2 shows a back-gate (BG) sweep of a single nanowire device for two different BG bias conditions, namely $V_{BG1/2}$ = ±20V, at a drain bias of V_{DS} = ±2V. Applying a negative voltage to the BG of the NW device leads to an accumulation of majority carriers in the thin top-silicon layer, hole conduction occurs (squares). In the contrary, electron conduction occurs through a narrow inversion layer forming at the top-Si BOX interface at sufficiently positive BG bias (circles). With this knowledge, performing a front-gate (FG) voltage sweep, at constant BG voltages, MOSFET-like transfer characteristics are achieved as illustrated in Fig. 3. The VS-PMOS like NW exhibits a subthreshold slope of about SS_p≈100mV/dec, the VS-NMOS SS_n≈150mv/dec. Wiring up two devices, attempting to

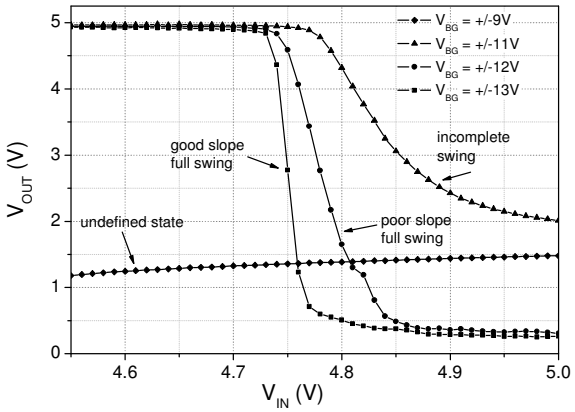

Fig.4: *Development of the inverter output characteristic by application of appropriate bias to the nanowires corresponding back-gate contact*

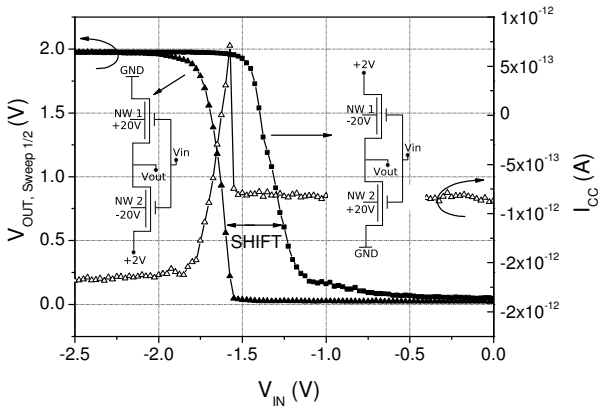

Fig.5: *Inverter transfer characteristic. Triangles represent the high-low transition curve of the inverter including the characteristic current peak, squares represent the transfer characteristic of the NWs at interchanged back-gate bias.*

form a simple digital logic gate, i.e. an inverter, is described in Fig. 4. By ramping of the BG voltage of each NW to form a NMOS and PMOS respectively, the evolution of the matching process of the two transistors finally forming a CMOS inverter can be observed. The matching devices are used to characterize the resulting current levels and threshold voltage. Further characterization of this inverter setup is shown in Fig. 5. A clear inverter characteristic can be found at unsymmetrical and symmetrical (not shown) bias. The characteristic cross-current (I_{CC}) peaking at the inverters HIGH-LOW transition point indicates comparable behavior to a standard CMOS inverter set-up with conventional MOSFET devices. Additionally the output characteristic was measured with each devices electrical behavior interchanged i.e. NW1 working as PMOS, NW2 as NMOS, and vice versa, confirming the switchability of the devices via change of BG voltage. The observed shift in the inverter characteristic is based on the not perfectly matching prototype devices. Industrial scale fabrication would certainly circumvent this issue due to the elimination of process and dimensional variations.

In conclusion, a novel nanowire device architecture is demonstrated, leading the way for a new type of digital logic that is interchangeable on the fly, by application of a control voltage to the corresponding back-gate.

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Comparison of the switching speed in junctionless and accumolation-mode gate-all-around nanowire transistors

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1. Abstract

This paper represents the simulation and comparison of switching speed between junctionless and accumulation-mode (AM) gate-all-around nanowire transistors for different Si nanowire cross-sections ranging from 5x5 nm^2 to 7x7 nm^2 and for different doping concentration, using both 3D classical and quantum simulations. We show that for small dimension devices the switching speed of both devices is very similar.

2. Introduction

The semiconductor industry faces new challenges due to continuous shrinking of device dimensions. Since distance between junctions of modern devices are going to be less than 10 nm, extraordinarily high doping concentration gradients are needed. Due to the laws of diffusion and statistical nature of the doping atoms, fabrication of such junctions is a serious challenge for semiconductor industry. Recently the junctionless nanowire transistor has been proposed [1]. As there are no junctions and no doping concentration gradients in such a transistor, the fabrication process becomes less complicated. The previous study shows that these transistors are also less sensitive to short-channel effects [2]. Here we investigate and compare the switching speed of junctionless and accumulation-mode (AM) gate-all-around (GAA) nanowire transistors using both 3D quantum and classical simulations.

3. Device Simulation

The 3D schematic and longitudinal cross-section view of the simulated devices are shown in Figures 1 and 2, respectively. We have used 3D quantum simulator based on non-equilibrium Green's function (NEGF) formalism for quantum simulations and the Atlas 3D device simulator [3] for our classical simulations. Simulations have been carried out for low (3×10^{19} cm^{-3}) and high (7×10^{19} cm^{-3}) doping concentration for the junctionless devices. The AM devices have also low (3×10^{19} cm^{-3}) and high (7×10^{19} cm^{-3}) doping concentration in source/drain extensions and 1×10^{16} cm^{-3} in the channel. In all simulation results, the drain bias is 0.4 (V) and the gate length is 15 nm.

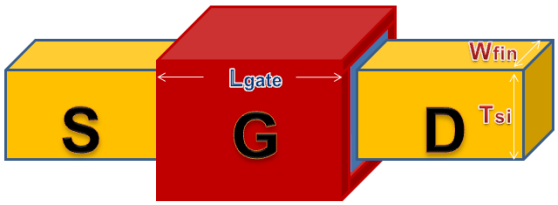

Fig.1: *3D schematic of AM and junctionless GAA nanowire transistors*

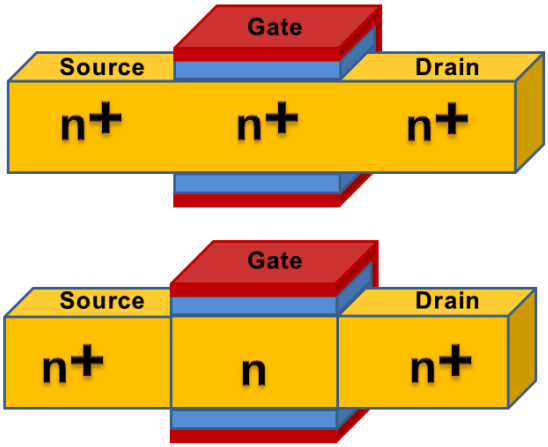

Fig.2: *Longitudinal cross-section view of junctionless GAA nanowire transistor (top) and AM GAA nanowire transistor (bottom) used in this work*

4. Results and discussion

To compare the switching speed of junctionless and AM gate-all-around nanowire transistors we use the switching time calculated using $\tau=Q/I$ which Q is charge in the gate when applying $V_g=V_{th}+0.2$ (V) and I is the drain current at $V_g=V_{th}+0.2$ (V). Tables 1 and 2 show the switching time of GAA nanowire transistors for different cross sections and doping concentration values, simulated using classical and quantum simulators, respectively. The quantum effect consideration results in increasing of threshold voltage of the device. As a result, the on-current calculated by

classical simulation is higher than on-current which is calculated by quantum simulation. And as it can be seen in tables 1 and 2, usually the classical simulations predict less switching time compared to quantum simulations.

Table 1

Switching time (ps) calculated by classical simulator at $V_g=V_{th}+0.2$ (V)

Cross section (nm^2)	AM Low doped S/D	Jless Low doped	AM High doped S/D	Jless High doped
5×5	0.3	0.48	0.3	0.53
6×6	0.3	0.49	0.3	0.55
7×7	0.3	0.51	0.3	0.56

Table 2

Switching time (ps) calculated by quantum simulator at $V_g=V_{th}+0.2$ (V)

Cross section (nm^2)	AM Low doped S/D	Jless Low doped	AM High doped S/D	Jless High doped
5×5	0.41	0.41	0.61	0.61
6×6	0.48	0.51	0.75	0.9
7×7	0.58	0.63	0.93	1.08

From the Table 1, it can be seen that the AM device has a lower switching time than the junctionless device for different cross sections and doping concentration values. Quite different results are obtained when quantum simulations are used (Table 2). From Table 2 it can be seen that for larger cross-sections the AM device has a lower switching time but by decreasing the cross section of the devices both junctionless and AM devices tend to have very similar switching times. The reason can be explained in Figures 3 and 4. Figure 3 shows the electron density of junctionless and AM devices calculated by quantum simulations. As it can be seen in this figure the current flow is in the middle of the junctionless device for both cross-sections. In AM devices the current flow is more at surface of the device when the cross section is large, while the current flows preferentially in the middle of the device when the cross section is decreased, due to quantum effects. Figure 4 shows the electron density in the junctionless and AM devices, calculated using classical simulations. As it can be seen in this figure, the current flow for 7x7 nm^2 AM transistor is mostly at the surface of the device but unlike the quantum simulation, the current density is still mostly at the surface when the cross section is reduced. This shows that classical simulations are no longer valid for small dimensions of devices.

4. Conclusions

In this paper we have simulated and compared the switching time of junctionless and AM gate-all-around nanowire transistors using quantum and classical simulators. We find that classical simulations are not valid for small dimension devices and may lead to wrong results in calculating of the switching speed in small dimension devices. We find that in larger devices, switching time of AM devices is lower than in junctionless devices but both devices have a similar switching time when they have small dimensions.

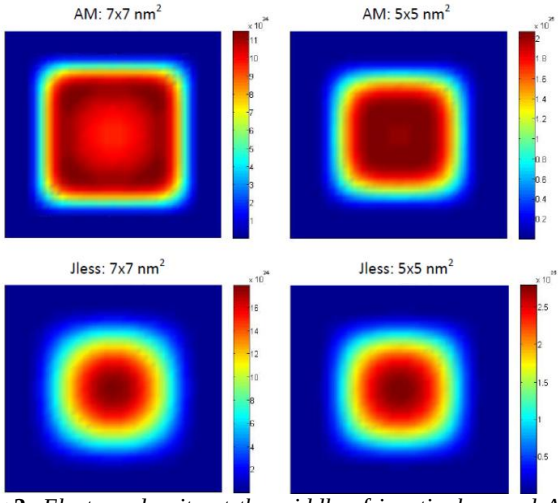

Fig.3: *Electron density at the middle of junctionless and AM devices for different cross-section dimensions (Quantum simulations)*

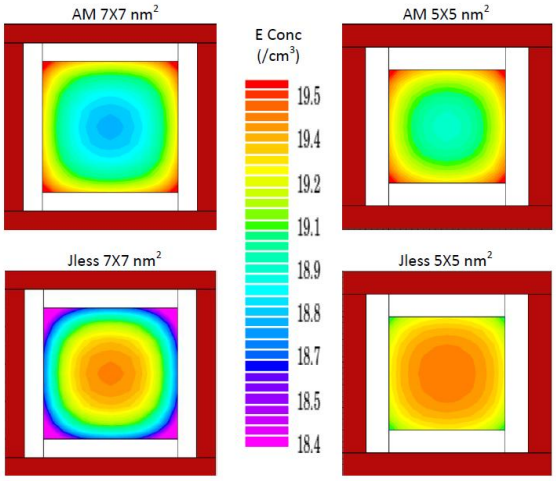

Fig.4: *Electron density at the middle of junctionless and AM devices for different cross-section dimensions (Classical simulations)*

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Fin Shape Influence on Analog Performance of MuGFETs at Room and at Low Temperature

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1. Abstract

MuGFETs are known to present better performance under scaling than single gate devices [1]. However, the fin shape definition may result in non-rectangular shapes (like in Fig. 1) [2], affecting the electrical parameters of the device. This work addresses for the first time how the geometrical fin parameters affect the analog performance of triple-gate MuGFETs through experimental and 3D numerical simulations at room temperature and at 200K.

2. Measured and Simulated Triple-Gate MuGFETs

The experimental devices used in this work are state-of-the-art triple-gate n-MuGFETs fabricated at imec, Belgium, following the process described in ref. [3]. The channel doping level is equal to $N_A=1x10^{15}cm^{-3}$. The fin height H_{FIN} is 65nm and the gate dielectric is composed of 2.3nm HfSiON (50% Hf) on 1nm SiO_2, resulting in an effective gate oxide thickness of 2nm. The midgap metal gate is obtained by deposition of a 5nm TiN layer and 100nm thick polysilicon capping to complete the gate electrode. Drain and source extensions lengths equal 50nm. Devices with 5 fins and a fin width W_{FIN} equal to 20nm, and channel lengths L of 100 and 900nm are measured at two temperatures T, 200K and 300K. The simulated devices present the four fin shapes showed in Fig. 2, with W_{Top} and W_{Bottom} equal to 20nm and Middle Fin Width (W_{mid}) equal to 0, 10, 20 and 30nm. Electrical parameters used in the 3D numerical simulations for the rectangular fin shape transistor (shape 3) were obtained from experimental data at room and at 200K.

3. Results and Discussions

Experimental and simulated data for threshold voltage (V_{th}) and subthreshold swing (SS) are presented in Fig. 3 as a function of W_{mid}, for two values of L and T. Both cases show good agreement between simulated and measured data, with errors below 4.5%. The increase of V_{th} with the reduction of the silicon fin width is due to the channel potential surpassing $2\cdot\phi_f$, raising the concentration of carriers in the channel more than the one observed for wider fins, causing the increase of V_{th} [4]. The increase of V_{th} with the reduction of T is related to the expected variation of ϕ_f with T [5]. The roll-off of V_{th} with the reduction of L from 900 to 100nm is also presented. A weak dependence of SS on the fin shape and length is observed, with values near the theoretical limit of $(k\cdot T/q)\ln(10)$, at both temperatures. Slightly lower SS values, down to 2.93%, are obtained for narrow W_{mid} and shorter L as a result of better electrostatic coupling between the gate walls. Fig. 4 shows g_m in the saturation regime. A better electrostatic coupling between the gate walls is expected for a reduction of W_{mid}, which enhances the gate control of the channel charges, improving g_m. However, for L=100nm the increasing parasitic series resistance R_S with W_{mid} reduction causes a nearly linear reduction of g_m for lower W_{mid}. For L=900nm, the R_S effect diminishes and devices with a smaller W_{mid} present slightly higher g_m, as expected. Higher g_m/I_D values are obtained with a reduction of T, as shown in Fig. 5, with higher g_m/I_D ratios at weak inversion for narrower W_{mid} devices (inset figure) as result of the lower SS, dependent on fin shape. This is more evident for devices with L=100nm. In the strong inversion regime, g_m/I_D also increases when T is lowered due to the increase of the carrier mobility. Devices with L=100nm present a lower g_m/I_D at both temperatures in strong inversion due to the high Rs. Fig. 6 shows the output conductance g_d and Fig. 7 the Early voltage V_{EA} for both values of L and T as a function of W_{mid}. The reduction of W_{mid} leads to lower (better) values of g_d and higher V_{EA}. This happens by reducing the penetration of the drain electric field into the channel through the enhancement of the electrostatic coupling between the gate walls as they come closer to each other. The reduction of T also causes a degradation (increase) of g_d and an enhancement (increase) of V_{EA}. The intrinsic voltage gain A_V, obtained by $A_V=g_m/g_d$, is shown in Fig. 8. For L=900nm, a higher A_V is obtained for devices with smaller W_{mid} and at lower T. For L=100nm, devices with smaller W_{mid} also present a higher A_V. However, a temperature reduction from 300K to 200K leads to decreased gains, in contrast to the L=900nm case. The reason for this temperature dependence is shown in Fig. 9. The gain (increase) caused by the reduction of T on g_m for L=100nm is from 3.8µS (W_{mid}=0) to 6.2µS (W_{mid}=30nm) and up to 1.8 times lower than the one obtained for L=900nm, while the degradation (increase) of g_d with reducing T for L=100nm is from 2.7nS (W_{mid}=0) to 2.9nS (W_{mid}=30nm) and up to 19 times higher than the one obtained for L=900nm. The small enhancement of g_m and the much higher degradation of g_d for L=100nm causes an inversed A_V trend from the one obtained for L=900nm. Fig. 10 presents the unit gain frequency (f_T). This parameter strongly depends on the fin shape for L = 100 nm. Following the same trend as for g_m, higher f_T values are obtained for devices operating at a lower T (higher g_m) and L=100nm.

4. Conclusions

The fin shape influence on the analog parameters of triple-gate nFETs at room and at low temperature (200K) is analyzed for the first time. The fin shape has a strong influence for shorter channel lengths and also on g_m/I_D in weak inversion. A T reduction causes a stronger g_d degradation for a shorter channel length than for a longer channel. A_V can be improved by a reduction of W_{mid}, increasing the performance up to 2.5dB compared with a rectangular device. The T reduction is beneficial for long channel devices, but not for shorter devices, where Av becomes worse. The unity gain frequency follows the same trend as g_m, proving to be better for short channel lengths and for low temperatures.

Acknowledgements

J. A. Martino, R. C. Giacomini, P. G. D. Agopian and R. Bühler thank CNPq and FAPESP for the financial support.

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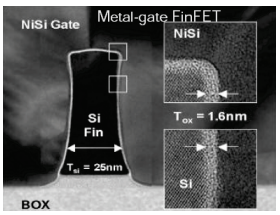

Fig. 1: *MuGFET cross-section showing concave sidewalls* [2].

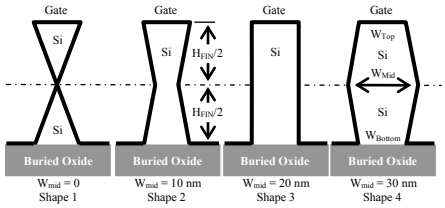

Fig. 2: *Fin-shape cross-sections used in this work.*

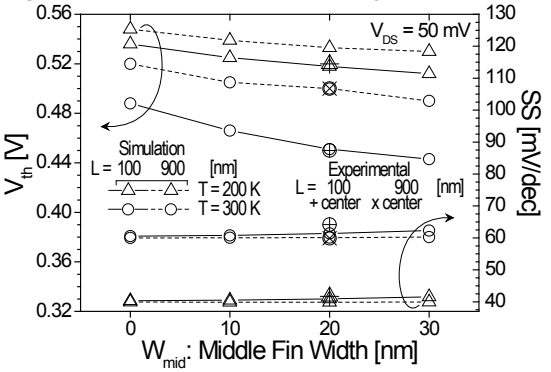

Fig. 3: *Simulated and experimental threshold voltage and subthreshold swing.*

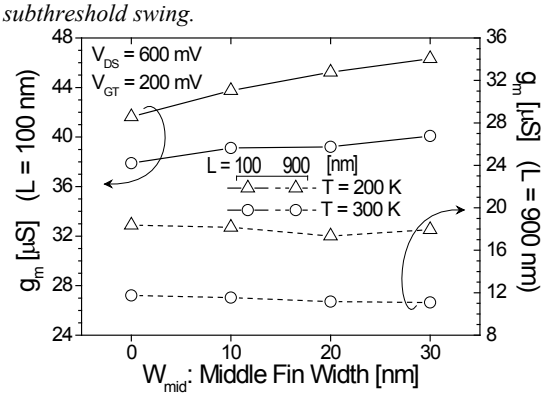

Fig. 4: *Transconductance as a function of fin-shape*

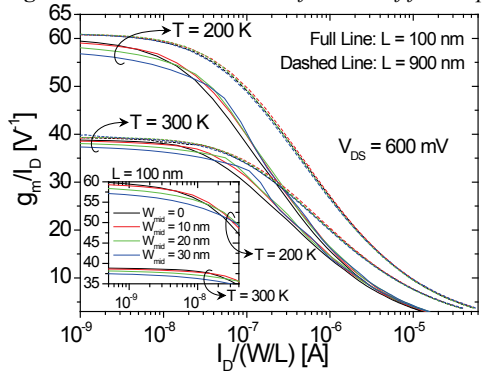

Fig. 5: *Transconductance to drain current ratio.*

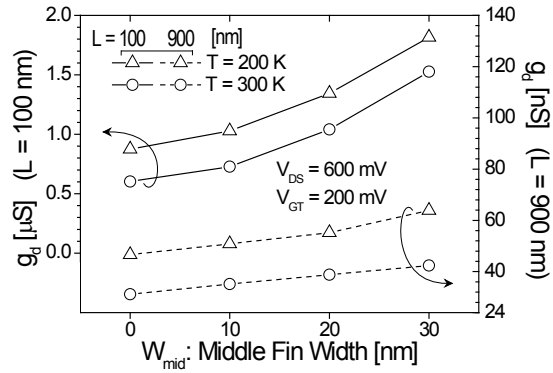

Fig. 6: *Output conductance as a function of fin-shape*

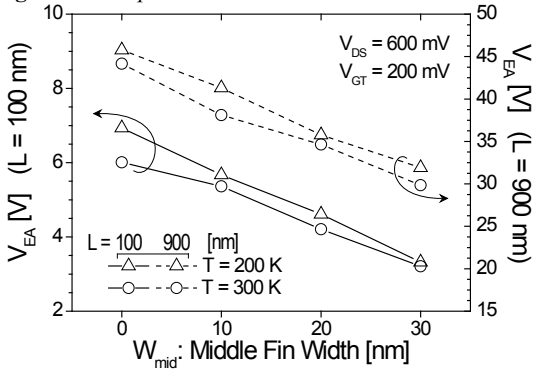

Fig. 7: *Early voltage as a function of fin-shape.*

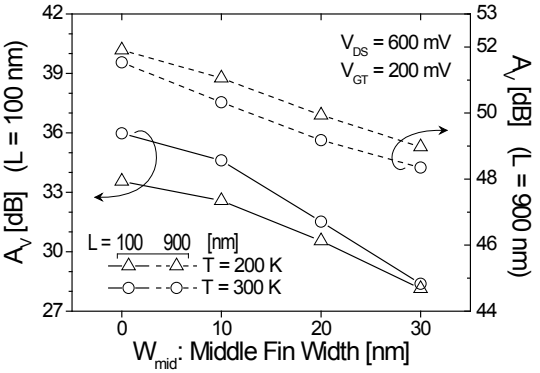

Fig. 8: *Intrinsic voltage gain as a function of fin-shape.*

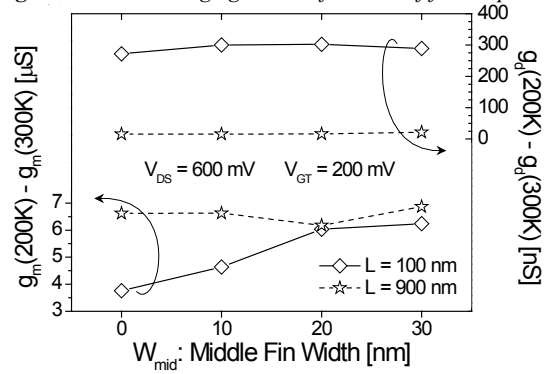

Fig. 9: *Transconductance and output conductance variation over the T = 300 K.*

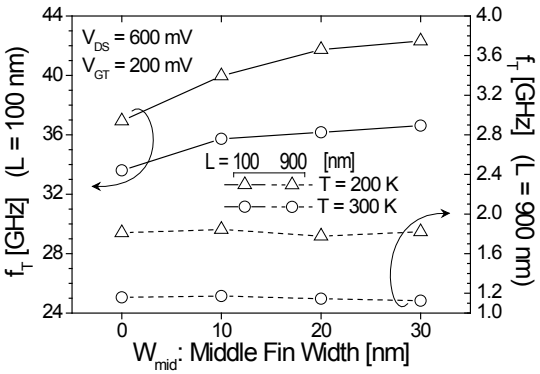

Fig. 10: *Unity gain frequency as a function of fin-shape.*

Session 4: Posters

Chairs: Carlos Sampedro & Noel Rodríguez

Hole Tunneling from Valance Band and Hot-Carrier Induced Hysteresis Effect in 0.13 μm Partially Depleted SOI n-MOSFETs

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1. Abstract

The hysteresis effect in the I_{DS}-V_{DS} output characteristics is studied in ultrathin gate oxide floating-body PD SOI n-MOSFETs. It is proposed that hole tunneling from valance band (HVB) causes positive hysteresis at lower V_{DS} region, while impact ionization (II) induced hot carriers leads to opposite phenomenon at high V_{DS}. And our findings reveal that hysteresis effect can be a serious reliability issue in SOI devices with floating body configuration.

2. Introduction

The primary feature of SOI MOSFET is with the body floating electrically, and thus the V_{BS} is not fixed. As V_{BS} changes, the device threshold voltage V_{TH} will change due to the body effect [1]. One manifestation of the V_{TH} variation is the hysteresis effect in the I_{DS}-V_{GS} characteristics [2~4]. However, the hysteresis effect in I_{DS}-V_{DS} output characteristics is rarely explored. Boudou et al. [5] only reported that I_{DS} - V_{DS} characteristics hysteresis of bulk MOSFETs in the high V_{DS} region. Shiao-Shien Chen et al. [6] only found the I_{DS} - V_{DS} characteristics hysteresis in the low V_{DS} region but without detailed explanation. In this paper, the further understanding of the hysteresis effect is investigated in I_{DS}-V_{DS} output characteristics and detailed physical explanation is given.

3. Results and Discussion

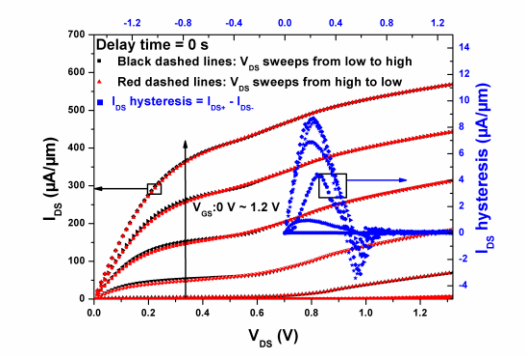

Fig. 1: *Left Y-axis: I_{DS}-V_{DS} characteristics of 0.13 μm core floating-body PD SOI n-MOSFET with delay time setting at 0s; Right Y-axis: Transient $I_{DS\text{-}hysteresis}$ characteristics of 0.13 μm floating-body PD SOI n-MOSFET.*

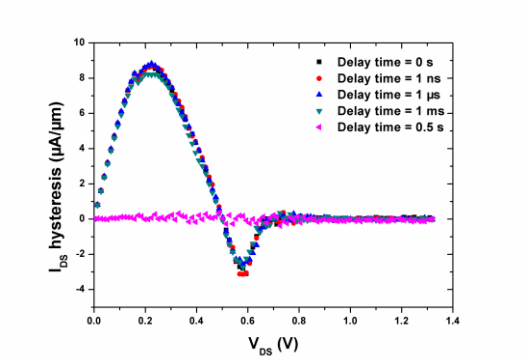

Fig. 2: *I_{DS}-hysteresis characteristics, delay time = 0s, 1ns, 1μs, 1ms and 0.5s at V_{GS} = 0.8V.*

Figure 1 shows the transient I_{DS}-V_{DS} characteristics of PD SOI n-MOSFET after V_{DS} forward and reverse sweeps with the delay time setting at 0s. Positive and negative $I_{DS\text{-}hysteresis}$ can be observed at low and high V_{DS}. As can be seen

from Fig. 2, obvious $I_{DS\text{-}hysteresis}$ can be found even if the delay time prolonged to 1ms. However, this effect can be eliminated as the delay time extends to 0.5s.

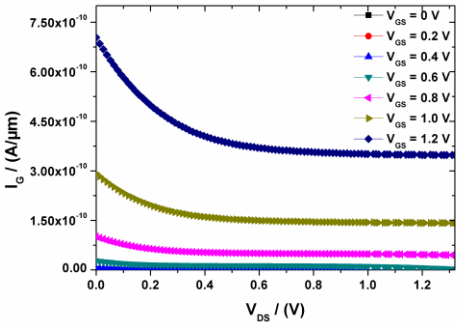

Fig. 3: *Gate tunneling current versus drain voltage of 0.13 μm core floating-body PD SOI n-MOSFET.*

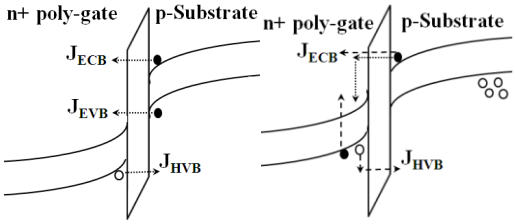

Fig. 4: *Three mechanisms for gate tunneling.* **Fig. 5:** *AHI model for an ultrathin gate oxide of a PD SOI n-MOSFET*.

Figure 3 illustrates that I_G reduces substantially due to the substantially reduced electric field at large V_{DS} [7]. When V_{DS} forward sweeps, large gate tunneling current causes plenty of carriers accumulation in the floating body. And the positive $I_{DS\text{-}hysteresis}$ value can be observed at low drain source voltage in figure 1. Conduction band electron tunneling (ECB) as shown in Fig. 4 flows through gate oxide from channel to gate when V_{GS} is larger than V_{TH} [8]. However, it does not affect the body potential of floating body. EVB tunneling current does not affect the floating-body potential when V_{GS} is lower than 1.12V. HVB contributes to gate-to-body tunneling current I_{GB} and modify the floating body potential. The recent proposed model of anode-hole-injection (AHI) [9] in Fig. 5 also explains gate tunneling current affect floating body potential when V_{GS} is lower than 1.12V. HVB and AHI modulate the floating body potential, thus causing the hysteresis effect of I_{DS}-V_{DS} characteristics at low V_{DS}. The negative $I_{DS\text{-}hysteresis}$ value can be observed at higher V_{DS} in the figure 1. When V_{DS} reverse scans, hot holes induced by impact ionization at high V_{DS} can accumulate and retain in the floating body during the retention time, which raises the floating body potential, thus decreases V_{TH} and increases I_{DS}. While V_{DS} forward sweeps, no hot holes generate by impact ionization due to not high enough V_{DS} is biased. So the floating body potential for the case of V_{DS} forward sweeps is lower than that for V_{DS} reverse sweeps. As a result, $I_{DS\text{-}}$ of V_{DS} reverse sweeps is larger, which results in negative $I_{DS\text{-}hysteresis}$.

4. Conclusions

The hysteresis effect in I_{DS} - V_{DS} characteristics is mainly resulted from variation of relatively slow generation-recombination processes. It is also found that the hysteresis effect is sweep-speed dependent. Furthermore, HVB and impact ionization in different V_{DS} region contribute to the floating body charging mechanisms and leads to the V_{TH} variation, which causes the hysteresis effect. And the hysteresis effect may occur during the transient V_{DS} switching and would be a serious reliability concern in ultrathin oxide PD SOI circuits.

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Highly Bi-Axially Orientation-Controlled Si Thin Films on Glass Substrates by Double-Line-Beam CW Laser Annealing

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1. Abstract

Bi-axially orientation-controlled Si thin films with very long grains (> 100 μm) were successfully fabricated on amorphous quartz glass substrates by continuous-wave laser crystallization with a parallel double-line beam. The newly-developed technique achieved highly-oriented Si films having (110), (111) and (211) orientations in the lateral crystalline plane, the transverse plane and the surface plane, respectively. This technique will be useful for fabricating 3 dimensional LSI devices as well as a possible alternative to the conventional SOI fabrication.

2. Introduction

Recently, laser annealing techniques for amorphous Si films have been greatly advanced by using, for example, a DPSS CW laser. The technique achieved one dimensionally-long and narrow grains; a size of 20 μm ×2 μm [(1), (2)]. High performance poly-Si TFTs with an electron mobility as high as 566 cm^2/ Vs were fabricated [(1)]. Surface orientations of the poly-Si films, however, were random and the statistical distribution of crystal grain orientations induced variation of TFT characteristics [(3)]. If the crystallographic orientations of Si films are fully controlled on amorphous insulators, characteristics of TFTs will be close to the conventional SOI transistors. Further, the technique will be useful for fabricating 3 dimensional LSI devices.

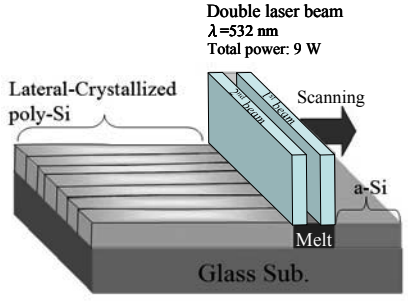

Fig. 1 Schematic diagram of laser crystallization

This paper reports on a new laser crystallization technique for fabrication of bi-axially orientation-controlled polycrystalline Si thin films without seed crystal, featuring linearly-arranged silicon large grains.

3. Double-line-beam laser crystallization

Figure 1 shows a schematic diagram of the laser crystallization. A DPSS CW green laser with a wavelength of 532 nm was used. The distribution of the original laser spot was non-uniform Gaussian profile. By use of diffractive beam homogenizer optics and shrinkage optics, this circular beam spot was deformed into a parallel double-line beam; 1st beam and 2nd beam, where each line beam had a size of 1.15 mm × 15 μm and the gap of the two beams was 15 μm. The laser energy distribution was practically uniform along longitudinal direction of the beam. An amorphous Si film deposited on a quartz substrate was set on an X-Y linear stage. The double-line beam was scanned over the surface of the film. Total laser power was fixed at 9.0 W and scan speed was 0.10 cm/s. The 1st beam melted the laser-irradiated region of the amorphous Si film and the 2nd beam kept the melted region at a high temperature. The incubation period of heating was expected to uniformly generate Si crystalline nuclei. The (110) orientation plane having the most dense Si atoms; $9.6x10^{14}$ cm^{-2}, was expected to preferentially appear as the growth plane which was observed in the conventional Si (110) epitaxial growth as the highest

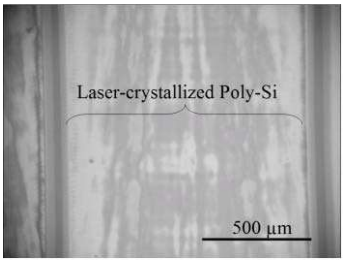

Fig. 2 Optical micrograph of laser crystallized Poly-Si thin film with the double-line beam CLC.

growth rate plane over (111) and (100).

Starting Si film preparation was as follows. A buffer SiO_2 film with a thickness of 1 μm was deposited on a quartz glass substrate by PECVD. An amorphous Si thin film was deposited with a thickness of 150 nm by PECVD using SiH_4 gas at 430°C. The samples were then annealed in N_2 ambient at 490°C for 20 min to reduce hydrogen content in the Si film. A cap SiO_2 thin film was deposited with a thickness of 100 nm by PECVD for preventing surface roughness. After the deposition of the thin films, double-line laser beam irradiation was employed to crystallize the amorphous Si film. Figure 2 shows an optical micrograph of a Si film crystallized with the double-line laser beam.

4. Crystallographic analysis of Si films

Figure 3 shows crystallinity of the double-beam laser-annealed Si thin film measured by in-plane XRD. In this measurement with in-plane-coupled scanning, the X-ray detector and the sample moved simultaneously, and the X-ray detector rotated twice as much as the sample rotation. Curve (a) in Fig. 3 shows the crystallinity in the direction of the laser scanning. The diffraction plane was always laterally fixed to the crystallization plane. The intent (220) and weak (440) peaks were typically observed over other slight peaks. The sum of the normalized X-ray area-intensity ratios for (220) and (440) was 82.6%. This result shows that orientation of the laser lateral crystallized plane was developed preferentially to (110). Curve (b) in Fig. 3 shows the crystallinity in the transverse plane of the Si film which was parallel to the laser scanning direction. The intent (111) peak was typically observed adding to slight peak of (220). The normalized XRD area-intensity ratio for (111) was 43.9%

Figure 4 shows inverse pole figures of EBSD. In the laser scanning direction indicating the lateral crystallized plane, the (110) crystal plane was dominant with an occupancy of 96.5%. Also in the transverse direction and the surface direction, the (111) crystal plane and the (211) crystal plane had high occupancies of 85.6% and 83.5%, respectively. All the Si grains were elongated to the laser scanning direction and linearly arranged. The grain length was longer than 100 μm and the average width was limited to 0.7 μm in this experiment.

5. Conclusion

The double-line-beam continuous-wave laser crystallization has been demonstrated to achieve highly bi-axially oriented Si thin films for the first time. The crystallized Si film had (110) , (111) and (211) crystal orientations in the laser lateral crystallized, the transverse plane and the surface plane, respectively. The occupancy of (110) in the lateral crystallized plane was 96.5%. In addition, silicon grains were elongated and linearly arranged with sizes of over 100 μm × 0.7μm. This technique will be useful to improve Si TFT characteristics and may be a possible alternative for fablicating future SOI directing 3 dimensional LSI.

Acknowledgment

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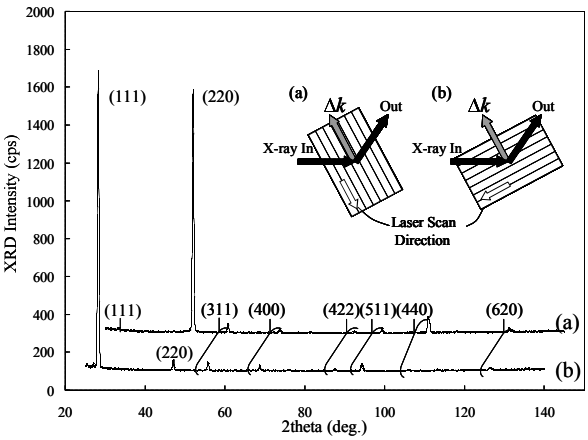

Fig. 3. Crystallinity of the laser-crystallized poly-Si thin films measured by in-plane XRD: (a) laser scanning direction and (b) its transverse direction.

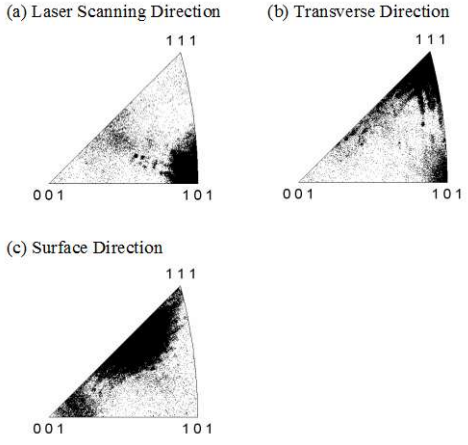

Fig. 4. Inverse pole figure of the laser-crystallized Si films: (a) laser scanning direction, (b) its transverse direction and (c) surface direction.

Extraction of flat-band voltage and parasitic resistance in junctionless MuGFETs

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1. Abstract

The paper investigates the influence of substrate bias on the parasitic resistance of source and drain regions of junctionless MuGFETs and suggests approaches for extraction the flat-band voltage, the parasitic resistance and the mobility in the bulk of the silicon wire.

2. Introduction

A new type of multigate MOSFET, called the junctionless (JL) transistor, has recently been proposed [1]. It contains highly doped silicon wire with the a pi-gate (Fig.1). The use of such a device avoids junction formation problem and can be used to make very short-channel devices [2]. The main parameters of the device can be determined by computer simulation to estimate the effect of parasitic resistance on the device current-voltage ($I_d(V_g)$ and $I_d(V_d)$) characteristics. One also needs to develop techniques to for extract the main electrical parameters. In this paper we present a method that allows the estimation of parameters such as the flat band voltage (V_{fb}), the source and drain parasitic resistance (R_{par}) and the mobility in the bulk channel (μ_b).

3. Device fabrication

The SOI layer was thinned down to T_{Si}=15-20nm and patterned into nanowires using e-beam lithography. Dry oxidation was performed to grow the gate oxide and ion implantation was used to dope the devices uniformly N^+ with a concentration of $N_d = 1\times10^{19}$ cm^{-3} to realize N-channel JL devices. Gate oxide thickness determined from HRTEM was 10 nm. Figure 1 shows schematic view of a JL MuGFET and a TEM cross-sectional view of the device. The width of the silicon channel was 15-20 nm (in Fig.1). The length of the gate (L_g) is 1 μm.

3. Results and discussion

The DC characterization of the devices was carried out using an Agilent B1500A semiconductor device parameter analyzer with 50 mV drain-source voltage (V_d) in order tooperate in the linear regime. For a doping concentration $N_d = 1\times10^{19}$ cm^{-3} a JL MOSFET has a large current in the bulk channel of the silicon wire (I_{ch}), but, if the gate voltage is large enough, conduction in surface accumulation channels can occur as well. Thus, in linear regime and in the case of accumulation the drain current (I_d) can be written as:

$$I_d = I_{ac} + I_{ch} \approx$$
$$\approx \mu_s C_{ox} \frac{W^*}{L_g}(V_g - V_{fb})V_d + q\mu_b n_c \frac{S}{L_g}V_d \qquad (1),$$

where C_{ox} is the gate oxide capacitance per unit area (3.36×10^{-7}F/cm^2), $W^*\approx W+2T_{Si}$ is the effective width of the accumulated channel (see Fig.1), n_c is the electron density in the channel layer ($n_c=N_d$), S is the cross-sectional area of the bulk channel. The area of bulk channel is a function of gate voltage ($S=S(V_g)$), but in case of accumulation mode it is saturated and can be estimated to be equal to as $W\times T_{Si}$.

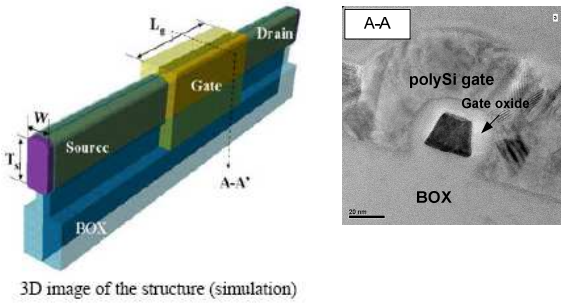

Fig.1: *Schematic view of JL MuGMOSFET and HRTEM picture of the device.*

Expression (1) shows that in accumulation mode the drain current has a linear dependence on the applied gate voltage and flat band voltage can be determined as point of transition into this linear operation regime [3]. However, the presence of additional parasitic source-drain resistance in JL devices results in violation of the linear dependency of I_d on V_g and in additional complications in the determination of the flat band voltage. Applying an additional voltage to the substrate (back-gate voltage, V_{bg}) allows us to control this source-drain parasitic resistance by either increasing or

decreasing it.

Fig.2 shows the influence of the back-gate voltage on the I_d-V_g characteristics of our JL device. In the region where the gate voltage is between 0.5 and 1.0 V, an enhancement of the linearity of the I_d-V_g characteristics with increase of the positive value of V_{bg} is observed (Fig.1a and b), which allows us to extract the value of the flat band voltage either from interaction point of two extrapolated straight lines (Fig.2c) or maximum point in the second derivative $d^2I_d(V_g)/dV_g^2$ (see Fig.2d). The extracted values of V_{fb} and the threshold voltage (V_{th}) of the JL MOSFET determined from maximum of $d^2I_d(V_g)/dV_g^2$ (Fig.2c) is presented in Fig.3a.

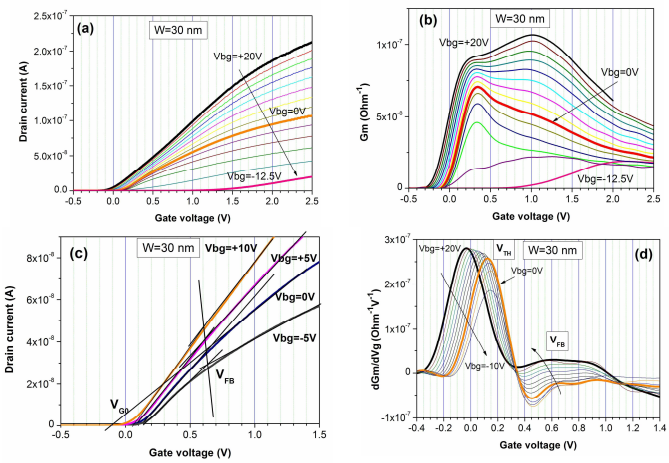

Fig.2: *The I_d-V_g characteristics (a), dI_d/dV_g-V_g characteristics (b) transconductance as a function of back gate voltage and schematic presentation of flat band voltage extraction from the I_d-V_g characteristics (c) and the d^2I_d/dV_g^2-V_g characteristics (d).*

The parasitic resistance can be estimated from expression for measured resistance ($R_{ds,meas}$) of the device operating in strong accumulation mode

$$R_{ds,meas} = R_{par} + \frac{1}{k(V_g - V_{fb})^n} \qquad (2),$$

where we assume that the resistance of the accumulated channel is small in comparison with that of the body channel in the strong accumulation mode. We also ignore the surface mobility dependence on electric field. The expression (2) shows that at high gate voltage the measured resistance will tend to R_{par}. Fig. 3b demonstrates the method of extraction of the parasitic resistance and effect of the back gate voltage on the value of R_{par}. It should be noted that any increase of the positive value of the back gate voltage results in an improvement of the linearity of the measured dependence $R_{ds,meas}$ on $(V_g\text{-}V_{fb})^{-1}$.

Knowledge of the flat band voltage and the parasitic resistance gives us a possibility to estimate mobility in the bulk channel of the JL device. Indeed, in the regime of "flat band" the measured resistance of the silicon wire can be expressed as:

$$R_{ds,meas}^{fb} = R_{par} + \frac{L_g}{q\mu_b N_d S} \qquad (3).$$

Thus, the bulk mobility can be estimated from the following expression

$$\mu_b = \frac{L_g}{qN_d S(R_{ds,meas}^{fb} - R_{par})} \qquad (4),$$

where the physical area of the bulk channel cross section, S, corresponds to total area of the silicon wire cross-section and can be estimated from electron microscopy pictures such as that shown in Fig.1.

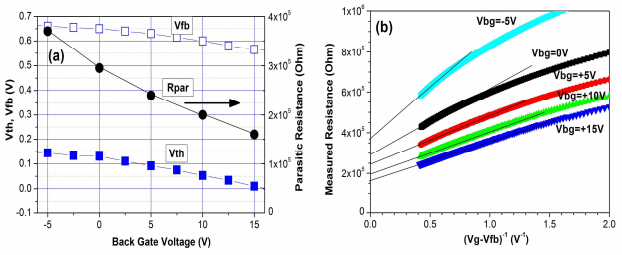

Fig.3: *(a) Threshold voltage, flat band voltage and parasitic resistance as a function of the back-gate voltage. (b) Measured resistance on inverse value of the gate voltage as a function of back-gate voltage.*

So, from our measurements we obtained that $R_{ds,meas}^{fb}$ =1.4x10^6 Ohm, R_{par} =2.95x10^5 Ohm and S=4.6x10^{-12} cm^2. Estimation of the N_d from the depletion depth and V_{th}-V_{fb} gave us smaller doping value than it was expected from the implantation data and (we find N_d=5x10^{18} cm^{-3}. using this parameter extraction technique). From expression (4) the extracted value μ_b is equal to 25 cm^{2}V^{-1}s^{-1}.

4. Conclusions

We analyze the influence of substrate bias on the parasitic resistance of the JL MuGFET. This allows us to propose a method for extracting parameters such as the flat band voltage, parasitic resistance and bulk mobility.

Acknowledgements

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Low Frequency Noise Spectroscopy in Advanced nFinFETs

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1. Abstract

In this paper, the low frequency noise is studied from 100 K to room temperature in n-channel triple-gate FinFET transistors with 25 nm fin-width and 65 nm fin-height, a high-k dielectric, metal gate and strained and unstrained substrates. These investigations allow to identify defects in the silicon film and to make a correlation with some technological steps.

2. Introduction

The multiple-gate FinFET transistors on a Silicon-On-Insulator substrate are considered as a promising candidate for the CMOS nanometer era, due to the controlled short channel effect by the 3D geometry, the low leakage current, and the higher mobility due to the undoped channel (10^{15}/cm^3). Strain engineering is used to increase the mobility which is one of the enabling techniques to boost the device performance further along the ITRS roadmap **[1].** In this work, low frequency noise measurements versus temperature are used as a device characterization tool in order to identify the defects present in the transistors. A powerful method for characterizing materials is provided by the Generation - Recombination (GR) noise, corresponding to a Lorentzian type of spectra and allowing for so-called noise spectroscopy when performed as a function of temperature **[2,3].**

3. Experimental

The n-channel transistors have been fabricated on standard and strained-SOI (sSOI) substrates. Additional splits use tensile stress induced by Contact Etch Stop Layers (CESL) across the gate stack and Selective Epitaxial Growth (SEG) for source and drain regions. The different wafers are indicated by SOI, SOI + SEG, SOI + SEG + CESL, sSOI, sSOI + SEG, sSOI + CESL, sSOI + SEG + + CESL. The gate stack consists of a high-k dielectric (HfSiON) on top of a 1 nm interfacial SiO_2, resulting in an equivalent oxide thickness (EOT) of 1.5 nm. The gate metal consists of 10 nm TiN covered by 100 nm polysilicon. Further processing details can be found in **[4].**

The gate lengths studied were L_G = 60 nm and L_G = 910 nm with 5 fins in parallel. The measurements were performed under linear operation at V_{DS} = 50 mV, the gate voltage was adjusted in order to keep the drain current constant at I_D = 1 µA over the whole temperature range, from 100 K to room temperature. The temperature was changed by a step of 10 K.

4. Results and discussion

Figure 1 presents a frequency normalized spectrum for standard (SOI) and strained nFinFETs with different strain techniques (sSOI + SEG + CESL) for a L_G = 60 nm. One can notice that the studied devices have a large number of Lorentzians (GR), giving rise to bumps in the spectra when they are normalized by the frequency. This has been observed for all studied devices and for all temperatures. It has been verified that the characteristic frequency of the Lorentzians does not change with the applied gate voltage; thus, the Lorentzians originate from defects in the depletion area. For each Lorentzian, the extraction of the characteristic frequency as a function of the temperature allows to plot an Arrhenius diagram; i.e. the evolution of $\ln(\tau \cdot T^2)$ versus $1/(kT)$ where τ is given by the inverse of the characteristic frequency. The energy difference between the conduction band energy and trap energy ΔE ($\Delta E = E_c - E_T$) and the capture cross section σ_n are extracted from the slope and the y intercept of the linear fit, respectively. The physical nature of these defects can be identified by comparing the energy and capture cross section of the traps with data in the literature **[5].** For each device, several defects were found. Some of them are clearly identified. Many other defects are still to be identified. However, the lack of data in the literature for these advanced materials and the fact that strain engineering may have an impact on the energy level and capture cross section, make it more challenging to identify all defects.

Figure 2 presents a typical Arrhenius diagram for a SOI nFinFET with SEG for L_G = 910 nm. In this example, three kinds of defects can be clearly identified: interstitial carbon-substitutional-phosphor complex (C_iP_s), interstitial boron interstitial-oxygen complex (B_iO_i) and divacancies V_2 (-/--).

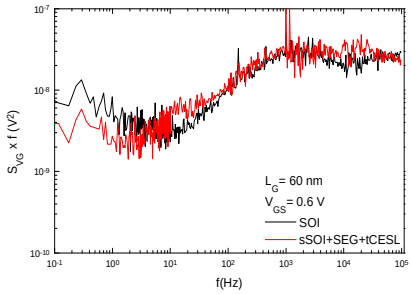

Fig.1: *Frequency normalized noise for unstrained (SOI) and strained (sSOI + SEG + CESL) for nFinFETs with L_G = 60 nm at V_{GS} = 0.6 V (V_{DS} = 50 mV).*

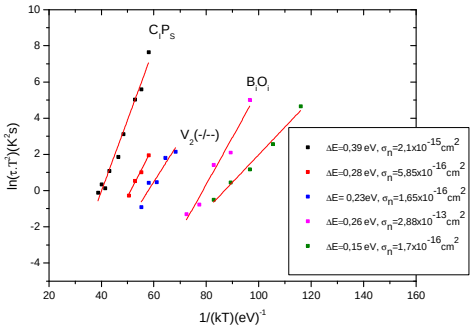

Fig.2: *Arrhenius plot of a strained nFinFET (SOI + SEG) with L_G = 910 nm.*

Table 1 shows the identified defects for all studied devices. One can notice that there are a number of defects which are frequently found in all studied devices but that not have been reported in the literature. For all the investigated technologies, 5 kinds of traps were identified: divacancies V_2(0/-) and V_2(-/--), traps related to hydrogen (noted H1), interstitial boron-interstitial-oxygen complex (B_iO_i) and interstitial carbon-substitutional-phosphor complex (C_iP_s). In addition to these, almost 10 kinds of unknown traps have been frequently observed. One can remark that the defect interstitial carbon-substitutional phosphor complex (C_iP_s) is found in all structures that are processed by using a SiC liner such as in standard (SOI) and strained (sSOI, SOI + SEG). This suggests a possible carbon contamination due to the SiC liner deposition step. The trap density of this defect can be evaluated; it was found that it varies from one structure to another (5 10^{15}-3 10^{17}/cm^3). The number of observed traps is important: this may be due to the relatively low value of the pure 1/f noise and the advanced technology used to process the devices. One can also notice that some traps (D7, D8) are observed in almost all the technologies studied; this suggests that these traps may be commonly found in silicon technologies. However, they could not be identified and therefore, might be related to the strain techniques which could modify the capture cross sections and the energy levels. On the other hand, D1, D2 are only observed in sSOI+SEG+CESL. A more detailed analysis of the process steps used in this technology could reveal the technological steps responsible for the creation of these defects.

Structures	V_2(0/-)	V_2(-/--)	H1	B_iO_i	C_iP_s	D1	D2	D4	D5	D7	D8	D9	D10
S0		X		x	X				x	x	X	x	x
S1	X	x			x			x	x		x	x	
S2	x		x	x	x			x		x	x	x	x
S3		X	x	x	x	x		x	x	x	X		
S4		x	x		x			x	X	X	X	X	x
S5		x	X	x						x	x		x
S6	x	x		x		X	X			x	x	x	x

Table 1*: The identified defects for all studied devices, the gray lines indicate the structures that are processed with a SiC liner.*

D1: ΔE=0.5 eV, σ_n=1.3x10^{-15}cm^2.
D2: ΔE=0.4 eV, σ_n=9.5x10^{-17}cm^2.
D4: ΔE=0.29 eV, σ_n=2x10^{-17}cm^2.
D5: ΔE=0. 29 eV, σ_n=1.8x10^{-19}cm^2.
D7: ΔE=0. 23 eV, σ_n=1.8x10^{-17}cm^2.
D8: ΔE=0.19 eV, σ_n=7.9x10^{-18}cm^2.
D9: ΔE=0. 15 eV, σ_n=2.1x10^{-18}cm^2.
D10: ΔE=0.2 eV, σ_n=1.8x10^{-15}cm^2.
V_2(0/-): ΔE=0.42 eV, σ_n=10^{-15}cm^2.
V_2(-/--): ΔE=0.23 eV, σ_n=10^{-15}-10^{-16}cm^2.
B_iO_i: ΔE=0.26 eV, σ_n=10^{-13}-10^{-14}cm^2.
H1: ΔE=0. 32 eV, σ_n=10^{-15}cm^2.
C_iP_s(0/-): ΔE=0. 38 eV.

S0: SOI; S1: SOI + SEG, S2: SOI + SEG + CESL, S3: sSOI, S4: sSOI + SEG, S5: sSOI + CESL S6: sSOI + SEG + CESL.
X*: found for both studied gate lengths;*
x*: found for one gate length only.*

5. Conclusions

In this work, a systematic study of the low frequency noise versus temperature has been performed on nFinFETs transistors. The analysis of the temperature evolution of the Lorentzians time constant allowed to identify the defects in the silicon film. For all the investigated technologies, 5 kinds of traps were clearly identified and almost 10 kinds of unknown traps have been frequently observed. In some cases, due to the lack of bibliographic data on strained silicon, it was not possible to identify the defect and to make a link to the related technological step. However, most likely, they can originate from the dry-etching or implantation damage. Finally, a carbon contamination probably due to the use of a SiC liner was revealed.

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Analysis and Optimization of Lateral Thin-Film Silicon-on-Insulator (SOI) PMOS Transistor with an NBL layer in the Drift Region

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1. Abstract

This paper is focused on the design and optimization of different power P-channel LDMOS transistors (V_{BR} > 120 V) with the purpose of being integrated in a new generation of Smart-Power technology based upon a 0.18 µm SOI-CMOS technology.

2. Introduction

P-channel lateral double diffused MOSFET (LDPMOS) transistors are widely used as high side power devices since it reduces its gate drive circuitry. Associated with the N-channel (LDNMOS) counterpart, they are employed in level shifters in many applications such as motor drivers or display panels. Good specific on-state resistance / breakdown voltage ($R_{on\text{-}sp}/V_{BR}$) trade-off of LDNMOS [1] is possible thanks to the Reduced SURface Field (RESURF) principle, since handle wafer is grounded and drain forward biased. However, for LDPMOS, this principle is inhibited because drain and handle wafer are commonly biased to the same potential. Some designs were develop in order to overcome this issue. In Bulk and thick film SOI technology the vertical depletion is possible with the inclusion of N-type floating layers at the surface [2] or deep inside the active Silicon region [3]. The presence of the N-type floating layer associated with a field plate defines the double RESURF [4] which leads to competitive $R_{on\text{-}sp}/V_{BR}$ trade-off. However, in thin-film SOI, the small active Silicon area reduces the possibility to define an N-type floating region without degrading the device $R_{on\text{-}sp}$. Consequently, only the effect of the field plate is possible and the doping concentration of the drift region which sustains the voltage has to be lowered, leading to an inevitable increase of $R_{on\text{-}sp}$. In this work, an LDPMOS design in Thin-SOI technology with a controlled N-type buried layer (NBL) obtained by means of high-energy Phosphorus and Boron multi-implantation sequence is defined by means of TCAD technological simulations. Fig. 1 shows the schematic cross-section of a conventional LDPMOS and the new proposed R-LDPMOS transistor, being both structures based upon a 0.18 µm smart power technology on Thin-SOI substrate. An STI (Shallow Trench Isolation) oxidation is previously defined, partially or totally covering the drift region length. The NBL layer, which is defined with the same P-well mask, could connect to the N-well diffusion, thus proportioning an evacuation path for the electrons generated by impact ionization. This fact guarantees high immunity to the well-known kirk-effect, thus safe-operating-area (SOA) could be significantly improved [5]. The addition of an NBL deep inside the drift region supports a space-charge depletion region which highly increases the RESURF effectiveness, thus improving the V_{BR}. Then, an optimum NBL implanted dose has to be set in order to ensure fully depletion before breakdown, thus achieving the best reliability conditions with a compensated charge balance among N and P doping in the drift region. Since the drift depletion action is enhanced with the addition of the NBL layer, the P-well implanted dose can be further increased to maintain charge balance, which could lead to a reduction of the $R_{on\text{-}sp}$ value. Nevertheless, if an active Silicon area of only T_{SOI} = 1.6 µm is considered, the NBL thickness (T_{NBL}) must be as small as possible in order to not excessively reduce the drift current path, defined by the P-well thickness ($T_{P\text{-}well}$), which could highly penalize the device $R_{on\text{-}sp}$ value. As it can be inferred from the schematic of Fig. 2, NBL is depleted by the combined action of substrate field-effect action, and the P-well/NBL junction. Then, the optimal NBL implanted charge must be appropriately chosen to compensate both depletion effects. Analytical expressions have been obtained in order to calculate the optimal P-well and NBL constant doping concentrations as a function of their respectively thickness in terms of voltage capability, the results being plotted in Fig. 3. On the other hand, Fig. 4 shows the structure cross-section and the resulted drift implantation profile of the analysed R-LDPMOS structure obtained by technological simulations. The simulation results of the $R_{on\text{-}sp}/V_{BR}$ trade-off in the case of the R-LDPMOS structure as a function of L_{STI} and ΔL_{poly} and P-well Boron implantation dose is plotted in Fig. 5. Extensive static and dynamic electrical simulations will be provided in the final manuscript.

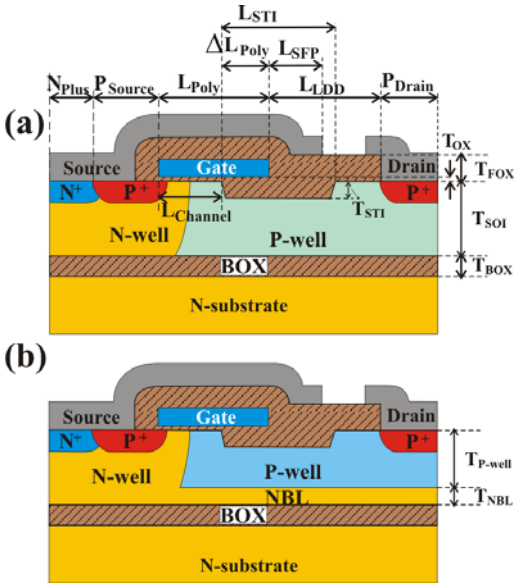

Fig. 1: *Schematic cross-section of the (a) conventional LDPMOS and (b) proposed R-LDPMOS transistors*

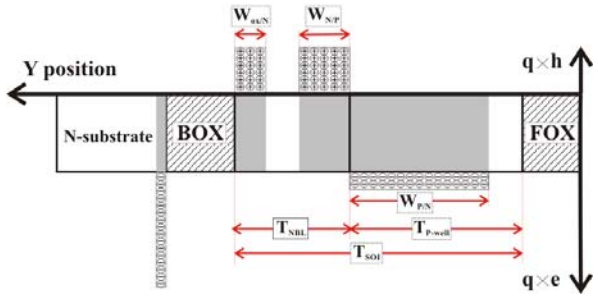

Fig. 2: *Schematic detail of charge distribution along the Silicon/BOX/Silicon region in R-LDPMOS structure*

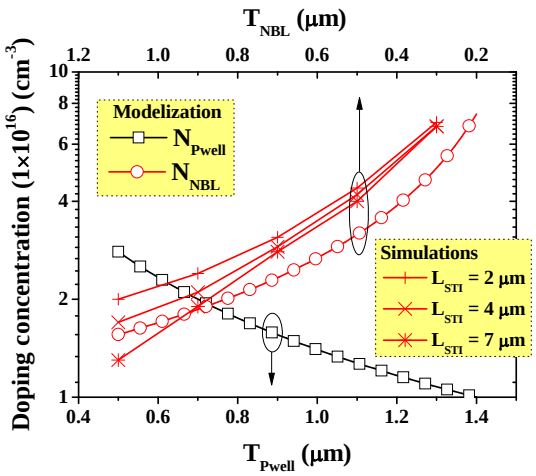

Fig. 3: *Calculated constant doping concentration in the P-well and NBL layers as a function of T_{Pwell} and T_{NBL}.*

4. Conclusions

The low RESURF effectiveness found in conventional P-channel LDMOS transistors requires the search of better optimal drift region design configurations such as the proposed R-PLDMOS with a NBL layer placed deep inside the SOI Silicon region. A significant improvement of the static performances can be achieved with the R-PLDMOS structure which assures competitive performances for switching applications.

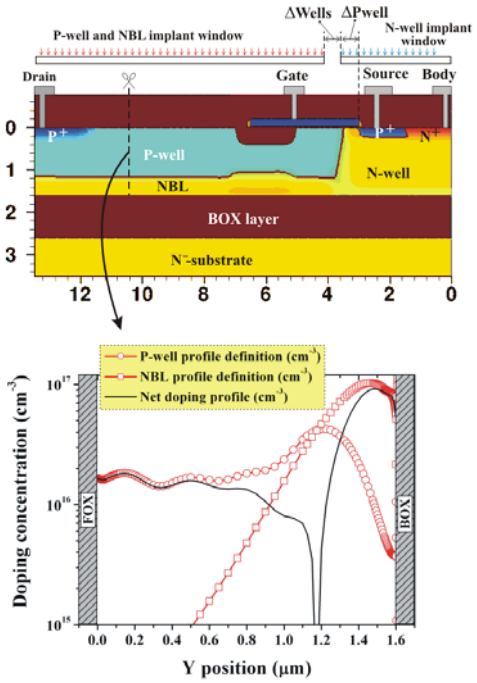

Fig. 4: *Schematic cross-section of the proposed R-LDPMOS transistor with the obtained doping profile throughout the SOI layer*

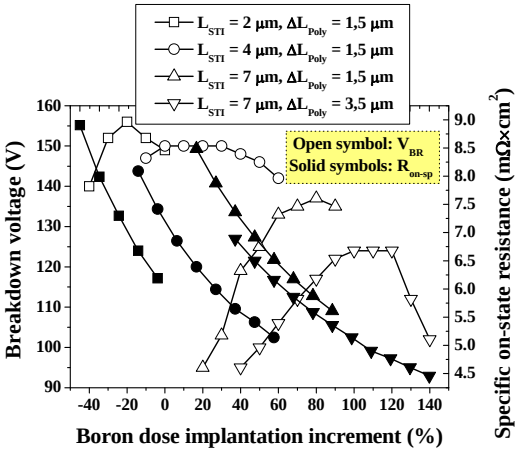

Fig. 5: *R_{on-sp}/V_{BR} trade-off as a function of P-well dose percentage increment in R-LDPMOS structures with different L_{STI} and ΔL_{poly} definitions*

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Ballistic Spin Field-Effect Transistors Built on Silicon Fins

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1. Introduction

The outstanding increase of computational power of integrated circuits is supported by the continuing miniaturization of semiconductor devices' feature size. With scaling approaching its fundamental limits, however, the semiconductor industry is facing the necessity for new engineering solutions and innovative techniques to improve MOSFET performance. Using spin as an additional degree of freedom is a promising way for future nanoelectronic devices in both memory [1] and logic [2] applications. Silicon, the main element of microelectronics, possesses several properties attractive for spintronics: it is composed of nuclei with predominantly zero spin and is characterized by small spin-orbit coupling. In experiments coherent spin transport through an undoped silicon wafer of $350\,\mu$m thickness was demonstrated [3]. Spin coherent propagation at such long distances makes the fabrication of spin-based switching devices in the near future quite likely.

2. Method and Results

We investigate the properties of ballistic fin-structured silicon spin field-effect transistors (SpinFETs). The original suggestion for the spin transistor by Datta and Das [4] employs the spin-orbit coupling for current modulation. The electric-field dependent spin-orbit coupling is assumed to be due to the geometry-induced breaking of the inversion symmetry (Rashba type). However, it was demonstrated recently [5,6] that the major contribution to the spin-orbit interaction in thin silicon films is due to the interface-induced inversion asymmetry (Dresselhaus type). The coefficient of the spin-orbit interaction in silicon heterostructures is a linear function of the electric field which opens the way to modulating the current by applying the gate voltage.

The non-zero spin-orbit interaction leads to an increased spin relaxation. In quasi-one-dimensional electron structures, however, a suppression of the spin relaxation was predicted [7].

In our studies silicon fins have a square cross-section with (001) horizontal faces. The parabolic band approximation becomes insufficient in thin and narrow silicon fins, where an accurate description of the conduction band based on the **k·p** model [8] is necessary. This leads to a subband shape being dependant on the fin height and thickness. Fig.1 demonstrates the dependence of the subband minima as function of the fin thickness *t*. The fin orientation is along [110] direction. The dependence of the splitting between the unprimed subbands with decreasing *t*, which are perfectly degenerate in the effective mass approximation, is clearly seen. The value of the valley splitting is in good agreement with recent results from density-functional calculations [9] (Fig.2). Splitting between the valleys in a [100] fin can be ignored [9]. In contrast, the dependence of the effective mass of the ground subband in [100] fins on *t* is more pronounced as compared to [110] fins. Results of the density-functional calculations confirm the mass dependences obtained from the **k·p** model (Fig.3).

To form the SpinFET we sandwich the silicon fin between two ferromagnetic metallic contacts. The degree of the spin polarization in each contact is $0<P<1$. The contacts can be in either parallel or anti-parallel configuration. The carriers in the contacts are characterized by the effective mass m_F and the Fermi-energy E_F. Following [10], delta-function barriers at the interfaces between the contacts and the channel of the strength $z = 2m_F U/\hbar^2 k_F$ are introduced. Contrary to [10], the spin-orbit interaction is taken into account in the Dresselhaus form [5-6]. We study the conductance G through the system for parallel and anti-parallel configurations of the contacts. Fig.4 shows the dependence of TMR$=(G_{\uparrow\uparrow}-G_{\uparrow\downarrow})/G_{\uparrow\downarrow}$ for [100] and [110] oriented fins with t=1.5nm on the value of spin-orbit interaction. Fins of [100] orientation display stronger dependence on β and are thus preferred for practical realizations of silicon SpinFETs. Because of the Dresselhaus form of the spin-orbit interaction, the TMR of [110] fins is most affected by the magnetic field along the transport direction (Fig.5), while the magnetic field orthogonal to the transport direction influences the TMR of [100] fins (Fig.6). Again, the TMR in [100] fins is most modified (Fig.6) by the external magnetic field, which provides an additional option to tune the performance of the silicon SpinFET.

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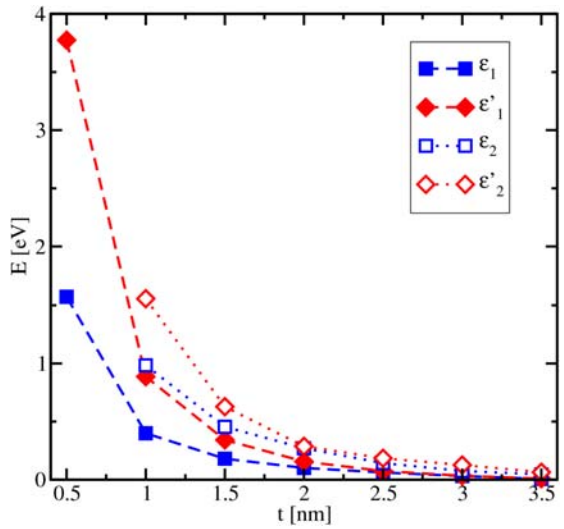

Fig.1: *Subband minima as a function of [110] fin thickness t.*

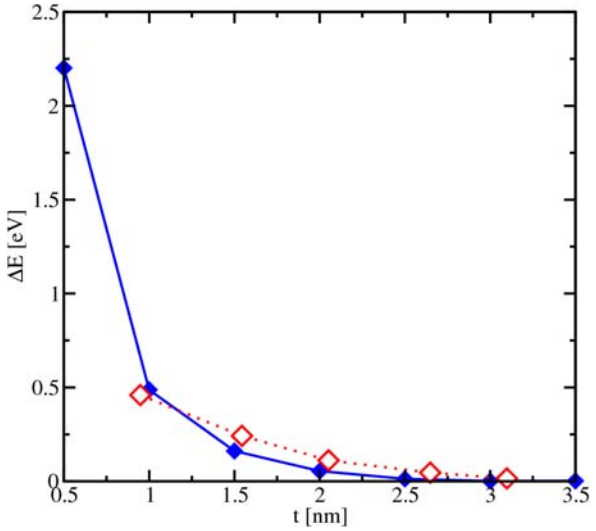

Fig.2: *Valley splitting in a [110] fin as a function of t. Open symbols are from [9].*

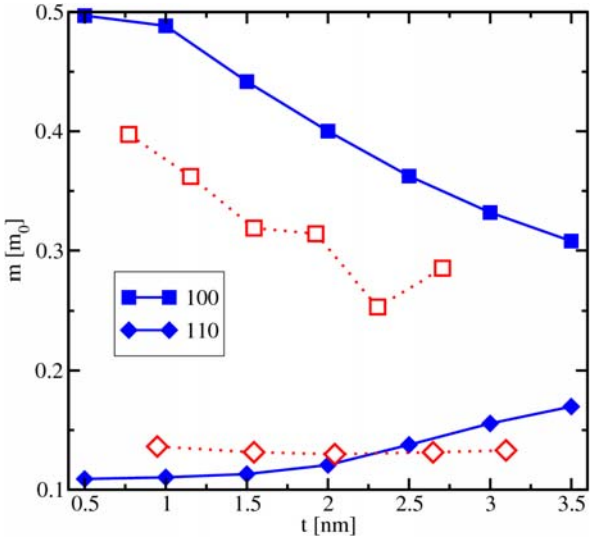

Fig.3: *Ground subband effective mass dependence on t in [100] and [110] fins. Open symbols are from [9].*

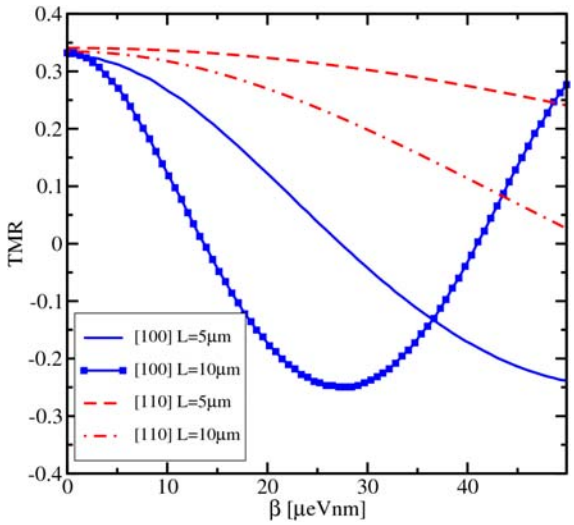

Fig.4: *TMR dependence on the value of the Dresselhaus spin-orbit interaction parameter for t=1.5nm, B=0T, P=0.4, z=5.*

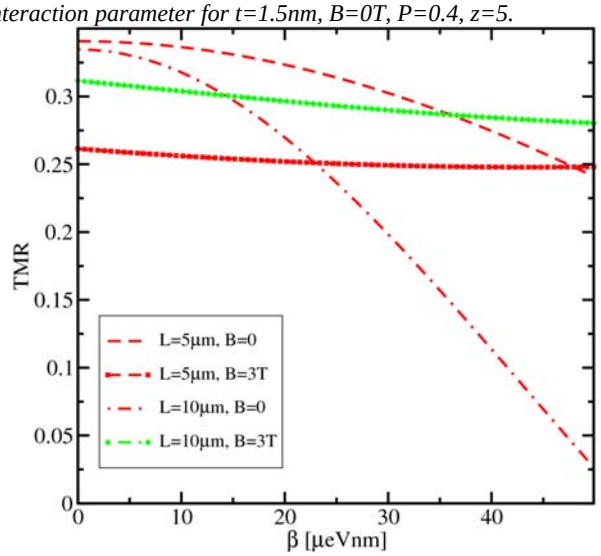

Fig.5: *The same as in Fig.4, for a [110] fin in a magnetic field parallel to the transport direction.*

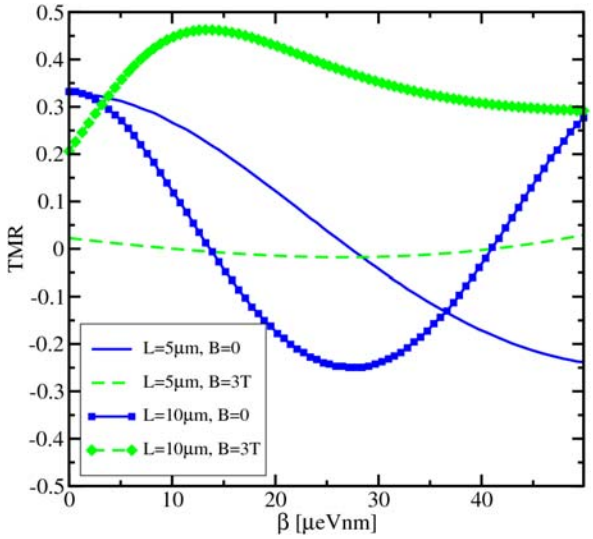

Fig.6: *The same as in Fig.4, for a [100] fin. The magnetic field is in [010] direction.*

Analog Performance of 60 MeV Proton-Irradiated SOI MuGFETs with Different Strain Technologies

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1. Abstract

This work studies the influence of a 60 MeV proton-irradiation on the SOI triple-gate FETs analog performance. The impact of the different strain technologies like CESL (uniaxial), sSOI (biaxial) and sSOI+CESL has also been analyzed. The transconductance, output conductance and the intrinsic voltage gain are obtained experimentally for n- and p-FET devices and the results are compared for the different process splits.

2. Introduction

Silicon-On-Insulator (SOI) technology is widely known to be radiation hard. However, the presence of charges into the buried oxide can affect the front gate characteristics owing to the strong coupling between front and back interfaces in Fully Depleted (FD) devices [1]. In spite of the improved performance of planar SOI devices, as the technology advances, multiple gate fin structures are considered as a promising alternative to planar ones due to a better coupling between gates and consequently improved short channel effects. MuGFETs may be even more attractive because these structures tend to suppress the back interface influence on the front transistor. For that reason, double [2,3] and triple gate [4-8] SOI transistors have demonstrated excellent radiation hardness, particularly for narrow fin-width (W_{FIN}) devices [9]. Additionally, it is known that mechanical strain can be used to improve the device performance through the mobility enhancement.

In this work, the impact of proton irradiation on analog characteristics of p and n SOI triple-gate MuGFETs is evaluated for different strain technologies for the first time.

3. Devices Characteristics

The triple-gate device characteristics are: 65 nm fin height, 150 nm thick buried oxide, channel length (L) of 150 nm and width (W_{FIN}) ranging between 20 and 870 nm. The gate dielectric consists of 2 nm HfSiON on 1 nm SiO_2, resulting in an Equivalent Oxide Thickness (EOT) of 1.5 nm. The gate is composed by 10 nm TiN covered by 100 nm polysilicon. The devices were fabricated by applying two tensile-strain-engineering techniques: sSOI substrates and dual Contact Etch Stop Layer (CESL) strain. The compressive c-CESL modifies the valence band structure resulting in an enhanced hole mobility for pFETs [10], while tensile CESL (t-CESL) enhances the electron mobility for nFETs. Biaxially tensile stressed substrates (sSOI) of ~1.5 GPa are also favorable for enhancing the performance of n-channel transistors. Four split types have been selected for proton irradiation: SOI (no stress = reference), SOI+CESL, sSOI and sSOI+CESL. The last split combines the biaxial stress of sSOI and the uniaxial stress of tensile CESL. Further process details can be found in [11]. All the analyzed devices have selective epitaxial growth (SEG) at source and drain in order to minimize the series resistance.

The 60 MeV proton irradiations have been performed at the Cyclone facility in Louvain-la-Neuve (Belgium) to a fluence of 10^{12} p/cm^2 with no bias applied.

4. Results and Discussions

Figure 1 shows the drain current (I_{DS}) as a function of gate voltage (V_{GF}) for W_{FIN}=870 nm for nMOS (SOI and sSOI+CESL) and for pMOS (SOI and CESL). It is noticed that after radiation the subthreshold behavior for nMOS (in both cases) is worsened (presence of back conduction) while it improves for pMOS (also for both technologies) devices (better subthreshold swing, SS). In order to better understand the subthreshold behavior with radiation, some 3D numerical simulations were performed. From figure 2 it can be noticed that for narrow nMOS devices (figure 2A), the electron current density at the back interface is almost the same for pre- and post-irradiated devices. But for devices with W_{FIN}>100 nm the electron current density near de back interface increases for post-irradiated devices due to the charges created at the buried oxide/back interface. For pMOS devices with W_{FIN} = 120 nm the hole current density shows the opposite behavior (figure 2B). It occurs because the radiation causes an increase of the buried oxide/interface trap charges which reduces the back interface threshold voltage (more negative) and consequently the pMOS becomes less susceptible to the back conduction which results in a better SS (lower).

The transconductance over drain current (gm/I_{DS}) curves as a function of normalized drain current for standard and strained devices before and after radiation are presented in figure 3. Focusing on nMOS devices (figure 3A) in the weak inversion region, the gm/I_{DS} degrades with radiation due to the interface charges increase (higher SS) for both strained and unstrained transistors. In moderate inversion, there is an anomalous behavior in gm/I_{DS} for wider devices due to back interface conduction. In strong inversion, for both narrow and wide devices, the radiation has no influence on this parameter, but the strain technology yields an increase of gm/I_{DS} owing to the mobility improvement. In addition, for narrow pMOS (figure 3B), gm/I_{DS} presents the same nMOS tendency observed on irradiated wide pMOS devices. However, the anomalous behavior of gm/I_{DS} for wider pMOS is suppressed after the irradiation due to a better back interface control resulting in a better gm/I_{DS} in both weak and moderate inversion regions.

Evaluating the transconductance extracted in the saturation region

(gm_{SAT}) for different fin widths (figure 4), it can be concluded that 60-MeV proton irradiation causes a small gm degradation even for wider devices. However, when the output conductance variation ($\Delta g_D = g_{D,POST} - g_{D,PRE}$) is analyzed (figure 5), it is clear that radiation has a stronger influence on g_D and it increases with fin width. The radiation causes an increase (worse) in g_D for nMOS devices, while for pMOS a reduction (better) is observed. Comparing strained and unstrained devices, it was observed that for both n and pMuGFETs, the strained (CESL for pMOS and sSOI+CESL for nMOS) devices suffer less influence of irradiation on g_D than their unstrained counterparts. The intrinsic voltage gain (A_V=gm/g_D) as a function of W_{FIN} is shown in figure 6. Since gm_{SAT} remains almost unchanged for pre- and post-irradiated devices, the A_V behavior has a strong dependence on g_D. As a consequence pMOS devices (SOI and CESL) present a higher A_V (better g_D) for irradiated devices. However, for nMOS devices the small gm degradation of the irradiated devices is compensated by the degradation in g_D, resulting into a similar A_V.

5. Conclusions

The influence of a 60 MeV proton-irradiation on SOI triple-gate p- and nFETs is studied focusing on analog parameters. The pMOS devices present an improvement in the subthreshold region (better SS) compared to nMOS (back channel activation) after irradiation due to the charge generated at the buried oxide/back interface. Different strain splits are analyzed, i.e., CESL (pMOS) and sSOI+CESL (nMOS) in order to investigate how the irradiation influences the best strain technology for each device type. It was observed that strained devices present a lower output conductance variation under radiation for both p- and nMOS. After irradiation the intrinsic voltage gain increases for pMOS (better g_D) and it is unchanged for nMOS due to the compensation between the gm and g_D degradation.

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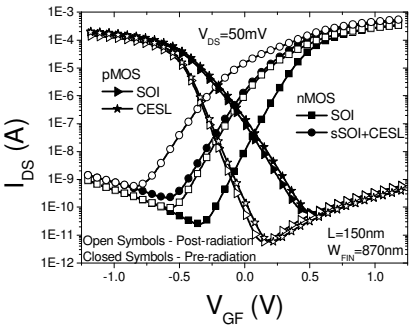


Fig.1: *I_{DS} as a function of V_{GF} for n and pMuGFETs before and after radiation.*

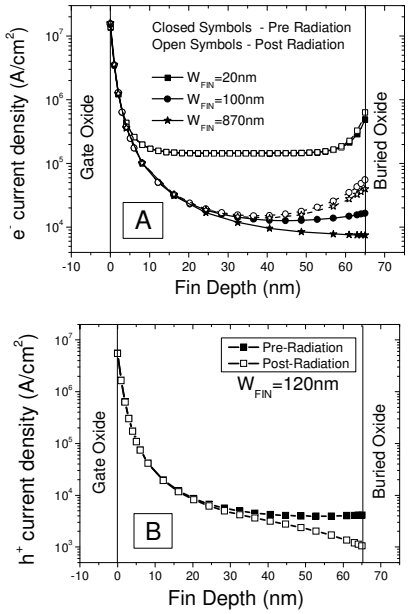
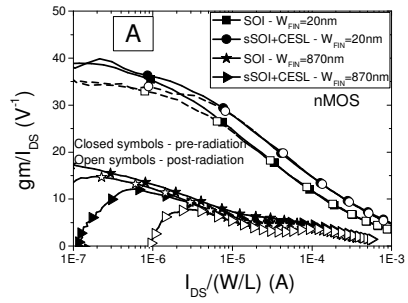


Fig.2: *Electron current density (A) and Hole current density (B) distribution.*



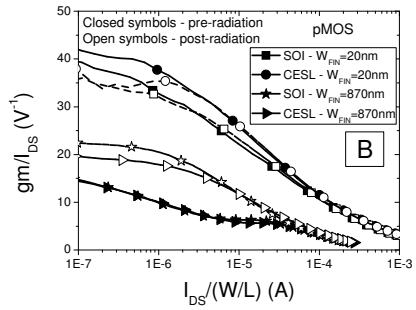


Fig.3: *gm/I_{DS} versus $I_{DS}/(W/L)$ for strained and standard devices pre and post radiation.*

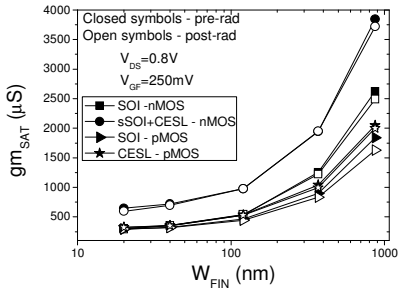


Fig.4: *Transconductance extracted in the saturated region versus fin width for strained and unstrained p and nMuGFETs.*

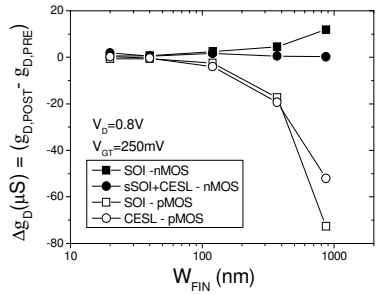


Fig.5: *The output conductance variation as a function of fin width for strained and unstrained p and nMuGFETs.*

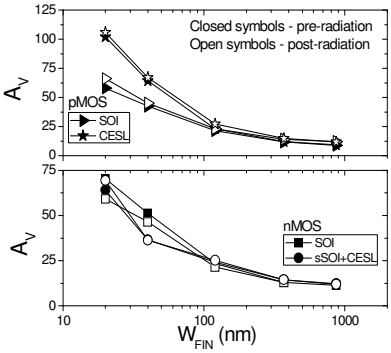


Fig.6: *The intrinsic voltage gain as a function of W_{FIN} for p and nMuGFETs.*

Simulation of non-standard multilayer 3D SOI-Structures and Microcavities

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1. Abstract. This paper presents simulation results of developed method for non-standard multilayer's local 3D SOI structures and microcavities fabrication. This technology allows creation and monolithic integration elements for MEMS and microlaboratories-on-chip.

2. Introduction

The creation and use of MEMS and microlaboratories-on-chip has significantly intensified for last years. Traditionally the planar CMOS, bipolar and Bi-CMOS technologies are used for MEMS and microlaboratories-on-chip fabrication. These technologies allow creating elements of digital and analog blocks, as well as sensor and actuator elements. The SOI-structures assumed to have better perspectives for development nanotransistors and others SoC devices based on higher speed, rigidity to external factors, growing degree of integration and for development of device structures with three-dimensional silicon-on-chip (3D SOI) architectures. The research and investigation of new low cost technological methods fabrication of original non-standard SOI-structures are desirable for development of new MEMS and microlaboratories-on-chip (LoC) elements. This article presents simulation results of local non-standard multilayer 3D SOI-structures and multilevel microcavities fabrication.

3. The base method of multilevel microcavities fabrication

The proposed method of multilevel microcavities fabrication is based on the results of one level cavities creation under surface of substrate. Cross section of a hermetical microcavity by this method is showed on Fig.1**.** This technology is compatible with the base technology of the local non-standard 3D SOI forming structures. Hermetic sealing microcavities are provided by the selection of topological sizes and technology for the local oxidation of the surface of cavities, with the following joining of hanging in the cavity nitride films (4) and deposition of sealing material (5) [1].

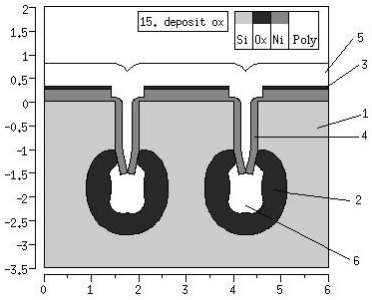

Fig. 1: *Cross-section of a hermetical microcavity: 1 – substrate (100); 2 – thick local thermal oxide; 3 – thin oxide; 4 – silicon nitride; 5 – polysilicon; 6 – hermetical microcavity.*

Multilevel cavities are formed using processes of industrial CMOS-technology: lithography, local thermal oxidation with masking by a silicon nitride film, isotropic and anisotropic plasma etching, formation of tunnels and cavities in a substrate, etc [1, 2]. Such local structures can be created at designed places on a silicon substrate according to the device layouts. The computer simulation results of base steps are shown in Fig.2.

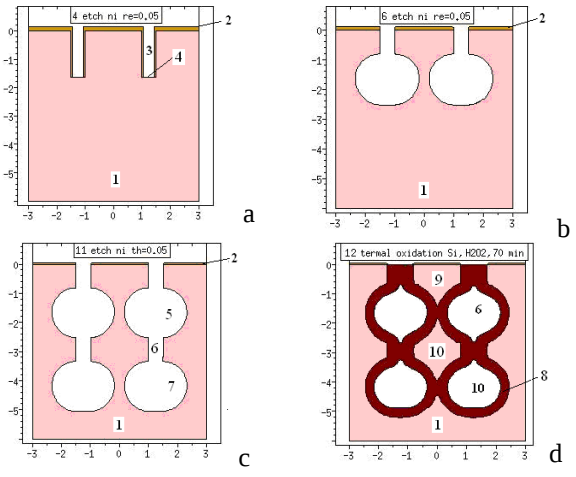

Fig.2. *The simulation results of base fabrication steps: a) initial substrate after anisotropic trenches etching; b) 1st level of cavities formed by isotropic etching; c) 2nd level of cavities formed by isotropic etching; d) hermetical microcavities: 1 – substrate, 2 – Si_3N_4, 3 – trench for 1st level, 4 – trench bottom, 5 – cavities of 1st level, 6 - trench for 2nd level, 7– cavities of 2nd level, 8 – local oxide, 9 – silicon-on-insulator, 10 – silicon-into-insulator*

It is possible to fabricate 1, 2 and more microcavity levels in substrate by proposed method. The hermetical cavities are obtained by thermal oxidation. At the same time are formed two levels of local 3D SOI structures. These cavities and channels could be used as elements for fluidic transport in microlaboratories-on-chip, as resonators, as elements of cooling system-on-chip, as microbattery elements builds into chip and other applications [5,6].

4. The method of non-standard multilayer 3D SOI-structures fabrication

This method is based on the results of non-standard local one-level 3D SOI-structures formation [2-5]**.** Fig. 3 shows the results of technology simulation of non-standard multilayer 3D SOI-structures which is compatible with the base method of multilevel microcavities fabrication.

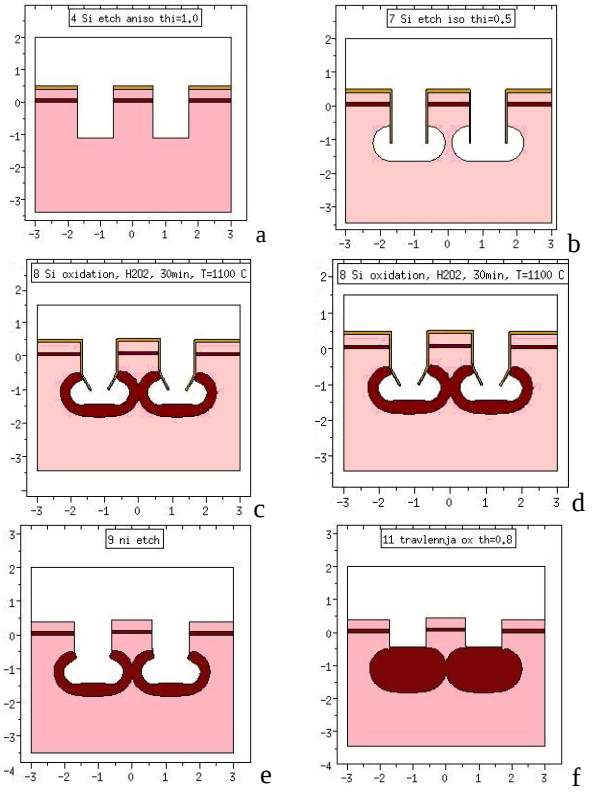

Fig.3. *The simulation results of base fabrication steps: a) initial SOI-substrate after anisotropic trenches etching of SOI-layer and substrate; b) microcavities formed by isotropic etching under surface of substrate; c) the structure (b) after thermal oxidation (80 min, 1100 °C); d) the structure (b) after thermal oxidation (30 min, 1100 °C); e) local two layers SOI-structure combined with non-hermetical microcavities; f) two layers SOI-structure after oxide deposition into cavities and partially etching. (In case, Fig.3, c the local SOI-island goes up and his level is higher than surface of initial SOI-substrate. The shorter time of oxidation (Fig.3, d) allows getting a planar surface of local two layers SOI islands and initial SOI wafer).*

Such 3D structures of "silicon-on-insulator" and "silicon-into-insulator" will extend possibilities of elements design for SoC and LoC. Hermetical microchannels and microcavities, whose are placed according to device layouts, can be used, for example, to build pressure sensors with monolitical integration of processing circuits on a chip, the elements of the cooling system on a chip, elements of microbatteries and energy storage embedded into chip.

5. Conclusions

This paper presents the simulation results of developed technological methods for non-standard multilayer's local 3D SOI-structures and microcavities/microchanels fabrication. These methods are compatible each other and allows creation and monolithic integration elements for MEMS, SoC and LoC.

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Strain investigation in Silicon-On-Porous Layer substrates and its evolution upon high temperature thermal treatment

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1. Abstract

This paper presents the structural properties of Silicon-On-Porous Layer (SOPL) substrates obtained by applying the Smart Cut™ technology to partially porous Si substrates. The crystalline quality of the different layers was studied by High-resolution X-Ray Diffraction (HRXRD) using Reciproqual Space Mapping (RSM) measurements. Tilt misorientation, mosaic spreads and strain values induced by the fabrication of SOPL substrates were accurately determined. Microstructural changes after high temperature thermal annealing in transferred non-porous/porous single crystalline bilayers were analyzed as well. Results demonstrate the compatibility of the SOPL structure with high thermal treatments, involved in device integration and post processing steps.

2. Introduction

Double transfer of thin single crystalline processed layer is a promising way to enhance functionality of microelectronic devices and circuits. It can be very interesting for 3D integration and for Back Side Imagers fabrication that require front and back side engineering of the Si active films [1]. To this purpose a recent approach was developed at the CEA-LETI [2], based on the use of porous Si substrates (Fig.1).

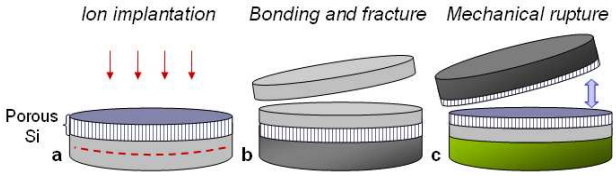


Fig.1: *Process scheme of the alternative technology developed at LETI.*

In this technology, 200mm p+ type Si substrates are superficially porosified by electrochemical anodisation in a HF based solution. Typical porous Si substrate shown in the Fig.2 was fabricated using a 200mm electrolytic wet bench made by Semitool. A mean porosity value of 60% and an effective thickness value of 400nm were measured by both gravimetric and spectroscopic ellispometric (SE) techniques. The substrate was used for layer transfer applying Smart Cut™ technology. The ion implantation was performed through the porous Si layer (Fig.1-a).

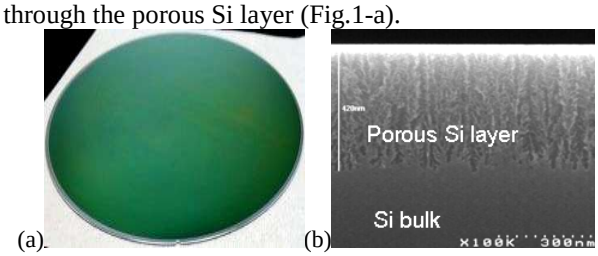


Fig.2: *(a) Picture of the 200 mm-porous Si substrate after anodization and (b) SEM cross-section of the porous Si layer.*

Fig.3-a shows the perfect transfer of a 200mm non-porous/porous Si bilayer onto a handling Si substrate, as confirmed by a SEM cross-section in Fig.3-b.

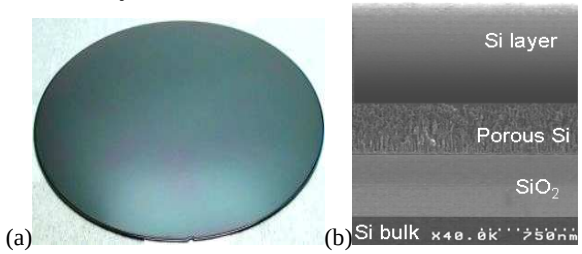


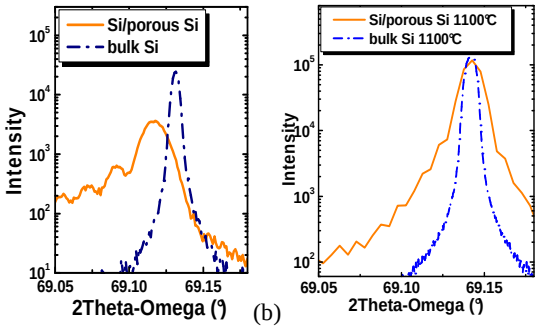
Fig.3: *(a) Picture of the 200mm SOPL substrate and (b) SEM cross-section of the SOPL structure after applying the Smart Cut™ technology to a partially porous silicon substrate.*

After splitting, a thickness uniformity value of the transferred bilayer was measured to be around 5% by SE characterization. A typical surface micro roughness of ~9nm RMS was measured by atomic force microscopy after the splitting. Such a SOPL structure is compatible with a second bonding onto another host substrate performed via a polymer layer. Subsequent mechanical separation was demonstrated by razor blade insertion in the fragile embedded porous Si layer.

3. Active transferred Si bilayer characterization

Crystalline properties of SOPL substrates were investigated by HRXRD. Triple axis RSM in (004) and (224) reflections were performed to assess precisely the strain induced in the non-porous/porous bilayer. First, XRD rocking curves were realized at ϕ and ϕ +180° for optimization of absolute measurements. After

splitting, a tilt misorientation of the transferred bilayer and the handling substrate was estimated to be 0.51°. It allows the precise identification of the signal coming from the transferred bilayer. The XRD rocking curves of the SOPL substrate confirmed the high crystalline quality of the transferred non-porous/porous Si bilayer. A mosaic spread was estimated to be 0.016°, four times higher than the one measured for Si bulk. XRD (004) 2θ-w curves were also performed before and after high temperature thermal annealing. Fig.4 shows the evolution of the XRD 004 2θ-w profiles of the SOPL substrate before and after annealing at 1100°C.

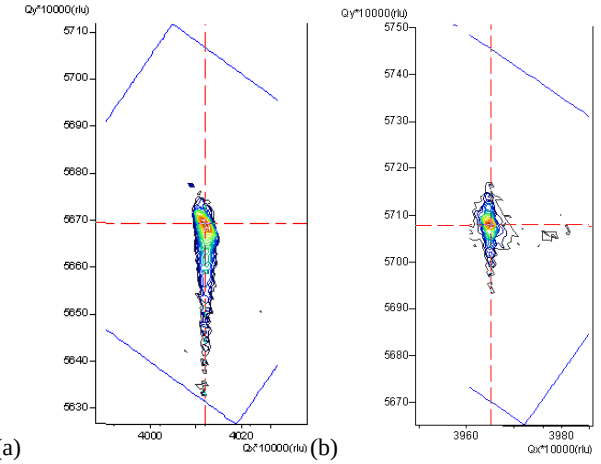


(a) (b)

Fig.4: *XRD (004) 2θ-ω profile of the transferred bilayer (a) after splitting and (b) after high temperature thermal annealing at 1100°.*

After splitting (Fig.4-a), two peaks can be well separated, one intense signal corresponding to the Si substrate at 2θ = 69.1313° and a less intense one for the transferred non-porous/porous Si bilayer at 2θ = 69.1168°. In addition, the second peak is asymmetrical and fringes are detected for lower angle values. This phenomenon could be attributed to the presence of both the underlying porous Si layer and the residual damage and strain in the top Si layer resulting from the ion implantation [4]. It is important to notice that anodization is a technological step which does not disturb the crystalline structure of the Si network of the porous Si layer [3]. After splitting and annealing at 1100°C (Fig.4-b), two peaks are still visible and are perfectly superimposed. This XRD (004) profile indicates a strain value equal to zero and the peak of the transferred layer became symmetrical which could be explained by the healing of the structural residual damages caused by ionic implantation.

Further investigations were performed to quantify accurately the out-of-plane strain of the transferred layer and to verify the possible presence of in-plane strain. Measurements of the RSMs in (224) reflection are illustrated in Fig.5.



(a) (b)

Fig.5: *RSM (224) of the transferred non-porous/porous Si bilayer (a) before and (b) aflter thermal annealing at 1100°C.*

After splitting (Fig.5-a), the RSM around the (224) reflection of the transferred bilayer gives evidence of a full in-plane coherency and confirms the out-of-plane strain in the transferred bilayer. A maximum out-of-plane compressive strain gradient value was estimated to be Δa/a=0.6% resulting from the ionic implantation damages and the presence of the embedded porous Si layer. After high temperature thermal annealing (Fig.5-b), the RSM in (224) reflection shows a significant reduction of the X-ray diffraction response. A very low out-of-plane compressive strain gradient value remains in the non-porous/porous Si bilayer and can be estimated to be Δa/a=0.15%.

4. Conclusions

Microstructural properties in SOPL substrate were studied by HRXRD measurements. After SOPL substrate fabrication, the transferred non-porous/porous Si bilayer was found compressively strained. After high temperature thermal annealing, the transferred non-porous/porous Si bilayer remains intact, no visible delamination of the layer occurs. Thermal treatments allow the reduction of the strain in the transferred non-porous/porous Si bilayer. The stability of the structure with high temperature thermal treatments and compatibility with subsequent devices integration were clearly demonstrated.

These works have been obtained in the frame of the CEA-SOITEC collaboration.

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Analytical Model for the Threshold Voltage of Junctionless Nanowire Transistors

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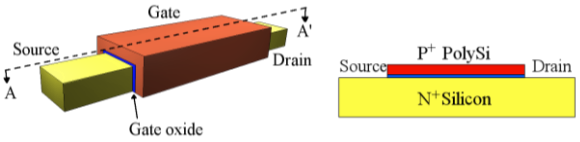
1. Abstract

This work proposes an analytical model for the threshold voltage of Junctionless Nanowire Transistors. The model is derived from the solution of the two-dimensional Poisson equation with the appropriate boundary conditions. The effects of quantum confinement are also considered. In order to validate the model, comparison with experimental data and three-dimensional numerical simulations has been performed.

2. Introduction

Multi-gate devices are considered very promising for the sub-20 nm era due to the better electrostatic control of the charges in the channel, which leads to short-channel effects reduction [1]. However, when the channel length is extremely reduced in multi-gate devices such as FinFETs and trigate FETs, ultra-sharp junctions with a high process complexity are needed, since the doping concentration varies several orders of magnitude over a few nanometers. Recently, a novel structure called Junctionless Nanowire Transistor (JNT) has been developed in order to address this issue [2-4]. In JNT devices, no source/drain to channel junctions or doping gradient is present. The schematic three-dimensional view of a JNT is presented in Fig. 1(A). Fig. 1(B) presents the cross-sectional view of an n-channel JNT device. The doping concentration is constant from source to drain.



(A) (B)

Fig.1: *Schematic view of a nMOS Junctionless Nanowire.*

3. Model Derivation

The 2D Poisson equation is given by:

$$\frac{d^2\Phi}{dx^2}+\frac{d^2\Phi}{dy^2}=-\frac{q\,N_D}{\varepsilon_{Si}} \quad (1)$$

where Φ is the potential, the x and y axes represent the width and thickness directions, respectively, N_D is the donor concentration, ε_{Si} is the silicon permittivity and q the electron charge. It is worthwhile noting that the carrier density has been neglected in the Poisson equation. The threshold condition is controlled by the depth depletion region and not by the formation of an inversion or accumulation layer.

Considering a GATE-ALL-AROUND (GAA) structure [5] with square cross-section, in order to simplify the model derivation, Φ variation in both x and y directions is the same ($d\Phi/dx = d\Phi/dy$). Multiplying both sides of the equation by ($d\Phi/dx$), equation (1) can be rewritten as:

$$2d\left(\frac{d\Phi}{dx}\right)^2=-\frac{q\,N_D}{\varepsilon_{Si}}2\,d\Phi \quad (2)$$

The term $d\Phi/dx$ is the component of the electric field in the x direction ($-E_{xx}$). To solve equation (2), it has been considered that the potential at the center of the channel is zero in the threshold condition. The threshold voltage (V_{TH}) is considered as the gate bias in which there is a point at the center of the cross section area of the device that is not depleted, such that bulk conduction can occur. As the source side of the channel is connected directly to ground and there are no junctions, when the center of the channel leaves the depletion region allowing for current conduction it is reasonable to assume the potential in this region is also zero. As it was considered a GAA structure, the derivative of the potential is zero in this point. To simplify the calculations, it has been assumed that the surface potential is constant along the two lateral and top surfaces, which can be considered as an effective surface potential at threshold (Φ_S). Also, it has been considered an effective surface electric field at threshold (E_S). Therefore, equation (2) can be integrated as follows:

$$-\int_0^{E_S} d\left(\frac{d\Phi}{dx}\right)^2=-\frac{q\,N_D}{\varepsilon_{Si}}\int_0^{\Phi_S} d\Phi \quad (3)$$

which results in:

$$E_S=\sqrt{\frac{qN_D}{\varepsilon_{Si}}\Phi_S} \quad (4)$$

Considering the MOS capacitor, the voltage drop in the oxide is:

$$V_{ox}=\frac{Q_{Si}}{C_{ox}}=\frac{\varepsilon_{Si}\,t_{ox}\,E_S}{\varepsilon_{ox}} \quad (5)$$

where Q_{Si} is the semiconductor charge density per unit area, C_{ox} is the gate capacitance per unit area, ε_{ox} is the gate oxide permittivity and t_{ox} is the gate oxide thickness. The relation Q_{Si}/C_{ox} can be rewritten as Q_{Si}'/C_{ox}' where Q_{Si}' is the gate capacitance per unit of length and C_{ox}' is the gate capacitance per unit of length. From this relation and equations (4) and (5):

$$\frac{Q_{Si}'}{C_{ox}'}=\frac{\varepsilon_{Si}\,t_{ox}}{\varepsilon_{ox}}\sqrt{\frac{qN_D}{\varepsilon_{Si}}\Phi_S} \quad (6)$$

Considering $Q_{Si}' = q.N_D.W.H$ and $C_{ox}' = \varepsilon_{ox}.W_{ox}/t_{ox}$ where W and H are the width and height of the device, respectively, and W_{ox} is the effective width of the gate oxide ($W_{ox} \approx 2H+W$), Φ_S can be isolated in equation (6):

$$\Phi_S = \frac{qN_D}{\varepsilon_{Si}}\left(\frac{W\,H}{W_{ox}}\right)^2 \quad (7)$$

From the MOS capacitor, it can be written:

$$(\Phi_{MS}\text{-}V_G\text{-}\Phi_S)C_{ox}' = Q_{Si}' \quad (8)$$

where Φ_{MS} is the difference between the workfunction of the gate material and the silicon, and V_G the gate voltage.

Substituting Φ_S given by (7), Q_{Si}' and C_{ox}' in equation (8), V_G at the threshold condition is given by:

$$V_{TH} = \Phi_{MS} - qN_D\left[\frac{WHt_{ox}}{\varepsilon_{ox}W_{ox}} + \frac{1}{\varepsilon_{Si}}\left(\frac{WH}{W_{ox}}\right)^2\right] \quad (9)$$

From equation (9), it can be seen that V_{TH} in JNT devices depends on the cross-section area ($W \times H$) and the effective width (W_{ox}). For narrow and/or thin devices, the carriers may be quantum confined. So, a term derived from the solution of the Schrödinger equation [6] can be added to equation (9) to account for this effect. Therefore, V_{TH} can be given by:

$$V_{TH} = \Phi_{MS} - qN_D\left[\frac{WHt_{ox}}{\varepsilon_{ox}W_{ox}} + \frac{1}{\varepsilon_{Si}}\left(\frac{WH}{W_{ox}}\right)^2\right] + \frac{\pi^2\hbar^2}{2qm^*}\left[\frac{1}{H^2}+\frac{1}{W^2}\right] \quad (10)$$

4. Model Validation

In order to validate the proposed model, 3D TCAD simulations were performed in Sentaurus tools [7]. V_{TH} was extracted using the double derivative method [8] for devices with different dimensions and doping concentrations with a drain bias of 50 mV. All the simulated devices present channel length of 1 μm and P^+ polysilicon gate. In the simulations, the width and the height of JNT vary between 5 nm and 30 nm, the t_{ox} between 1 nm and 7 nm and N_D in the range from 5×10^{18} cm^{-3} to 4×10^{19} cm^{-3}.

The V_{TH} calculated using the model compared to the simulated data is shown in Fig. 2 as a function of the W, H, t_{ox} and N_D. It can be noted an excellent agreement between the results for all devices.

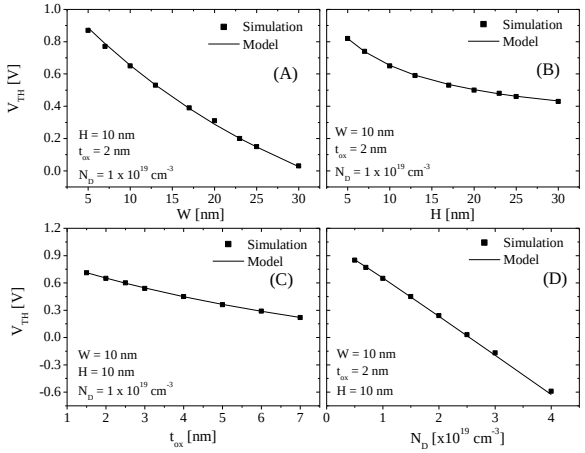


Fig.2: *Comparison between simulated and modelled V_{TH} as a function of the nanowire width (A), nanowire height (B), gate oxide thickness (C) and doping concentration (D).*

The measured devices were fabricated on SOI wafers following the process described in [2]. The nanowire height is approximately 10 nm. The mask nanowire width (W_{mask}) varies between 30 nm and 50 nm (the effective width of the nanowire is expected to be around 10~20 nm lower than W_{mask}). For each W_{mask}, three different devices were measured in different regions of the wafer which may have a slight variation on the dimensions and/or N_D. The devices present doping concentration around 1×10^{19} cm^{-3} and t_{ox} of 10 nm. Fig. 3 presents a comparison between the experimental data, considering a reduction of 20 nm in W_{mask}, and the proposed model. It can be seen that both data present a similar variation with the nanowire width.

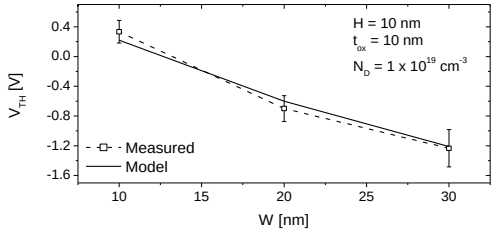


Fig.3: *V_{TH} comparison between experimental data and the proposed model as a function of the nanowire width.*

In Fig. 4 the threshold voltage shift due to the temperature variation (V_{TH}-$V_{TH,300K}$) obtained experimentally and through the model are exhibited. The incomplete ionization model described in [9] was used. The measured device present W_{mask}= 30 nm and $N_D = 3\times10^{19}$ cm^{-3}. The V_{TH} shift was calculated for three different widths. From this figure, it is possible to note that V_{TH} variation with temperature changes with W_{mask}. The V_{TH} shift of the measured device is similar to the shift of a modeled device with W = 20 nm, showing that the dependence of the V_{TH} on the temperature is accurately described by the proposed model.

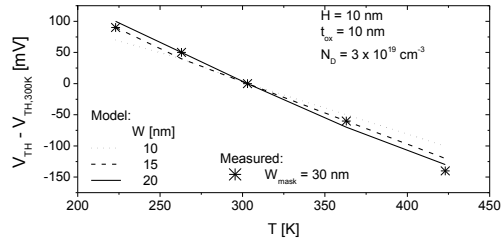


Fig.4: *V_{TH} shift due to the temperature variation comparing experimental data and the proposed model.*

5. Conclusions

This paper proposes, for the first time, an analytical model for the threshold voltage in junctionless nanowire transistors. The model was based on the solution of a 2D Poisson equation. The proposed model shows good agreement both with experimental data and 3D TCAD simulations.

Acknowledgements

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GIDL behavior with different TiN metal gate thickness and high-k gate dielectric on MuGFET devices

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1. Abstract

This work studies the influence of the TiN metal gate thickness on the gate-induced drain leakage (GIDL) in triple gate devices. In addition, also the impact of the high-k dielectric (HfSiON) is investigated. Higher GIDL is observed for thinner metal gate while a reduction of this leakage current was observed for the devices with a high-k gate dielectric.

2. Introduction

Multiple-gate (MuGFET) devices are one of the most promising candidates for enabling the continued MOSFET scaling, presenting a higher electrostatic control that results in a better short-channel behavior [1]. Additionally the gate dielectric thickness has been a limitation for this scalability by an unacceptable increase of the gate leakage current [2]. Alternatively the implementation of thicker high-k dielectrics allows a leakage reduction without loss in the gate capacitance [3]. The incorporation of nitrogen into these high-k materials can improve their thermal stability; reducing the dopant penetration and allowing further equivalent oxide thickness (EOT) scaling [4]. New gate materials have also been studied to achieve a proper threshold voltage (V_T) setting on both n- and p-channel devices in high-performance CMOS applications. The metal gate workfunction engineering has been shown as an attractive technique for V_T tuning whereby the poly gate material is replaced by metal gate electrodes [5-6]. For a MuGFET technology titanium nitride (TiN) has been widely studied showing low resistivity and a mid gap workfunction [7-8]. This effective workfunction can be tuned by varying its thickness, although a thicker TiN metal gate introduces a higher interface trap density and a correspondingly lower mobility [9]. The well known gate induced drain leakage (GIDL) [10], that originates from band-to-band tunneling in the drain region under the gate, seems to be sensitive to the gate workfunction. Recently GIDL has been applied for the write operation in a capacitorless one-transistor dynamic random-access memory (1T-DRAM) technology in order to achieve a reduction of the power consumption [11]. Therefore, the aim of the present work is to investigate the impact of GIDL on MuGFET devices with different TiN metal gate thicknesses and gate dielectric composition.

3. Experimental

The devices under investigation are n-SOI triple-gate FETs with 65 nm Si film on 150 nm buried oxide and a channel doping concentration of $1x10^{15}$ cm^{-3}. Two gate dielectrics were considered: 1.9 nm SiON chemical oxide and 1nm ISSG SiO_2 with 2.3 nm HfSiON on top. The TiN was deposited by metal organic chemical vapor deposition (MOCVD) and different splits were considered: 5 nm and 10 nm. The metal gate was covered by 100 nm polysilicon. Devices with 5 fins, an effective channel length of L_{eff}=0.91 µm and fin widths from 70 nm to 1870 nm were analyzed. More details on the device fabrication and their characteristics can be found in [12].

4. Results and discussion

Fig.1 shows the drain current extracted for a gate voltage overdrive of (V_{GT} =V_{GF} -V_T= -0.85 V) as a function of the effective fin width for the different TiN metal gate thickness and gate oxide. The current for negative gate voltage is dominated by a component of the off-state leakage current known as gate induced drain leakage (GIDL) current [10]. The GIDL current density can be modeled by equation (1), showing its dependence on the transverse electric field.

$$J_{GIDL} = A \cdot E_s \cdot \exp(-B / E_s) \quad (1)$$

$$E_S = \frac{(V_{DG} - V_{FB} - 1.2)}{3 \cdot t_{ox}} \quad (2)$$

Where A is a pre-exponential parameter, B (typically 23–70 MV/cm) is a physics-based exponential parameter and E_s is the transverse electric field at the surface [10]. As can be observed in Fig.1 higher I_{DS} (GIDL) is observed for thinner TiN metal gates and this effect is seen for both gate oxides. In addition, the SiON dielectric shows a higher GIDL current than the devices with a high-k gate dielectric.

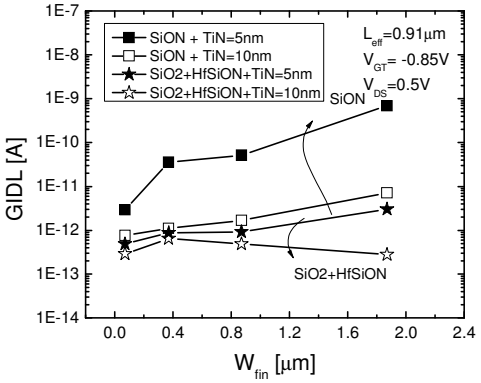

Fig.1: *GIDL as a function of the n-channel width for the different TiN metal gate thicknesses and dielectrics.*

In order to analyze this behavior the threshold voltage was extracted (Fig. 2). Higher V_T is observed for the thicker metal gate and this for both gate dielectrics. Comparing the different gate dielectrics, the high-k dielectric can gives rise to a larger V_T.

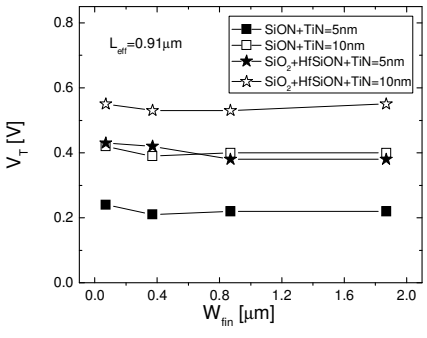

Fig.2: *V_T as function of W_{fin} for nMuGFETs with different TiN metal gate thicknesses and dielectrics.*

Figure 3 present the gate to channel capacitance (C_{GC}) as a function of the gate voltage curves for the different TiN metal gate thicknesses and dielectrics. Smaller C_{GC} (higher EOT) for 10 nm TiN is shown. This increase in EOT can be attributed to a reaction between the higher concentration of oxygen atoms (O_2) (generated during the deposition process) and the interfacial layer (IL) re-growing during the spike annealing [12]. Concluding, the V_T increase observed on Fig. 2 is related to this higher EOT and also due to the workfunction increment for thicker metal gate [6].

High-k gate dielectrics present lower EOT due to the increased permittivity. As a result the increased V_T observed for high-k dielectrics is related to a possible flatband V_{FB} variation. In agreement with the literature, increased defect density in the bulk of the HfSiON can be observed and not only at the metal interface, resulting in a V_{FB} and V_T shift [13]. The subthreshold slope extracted for devices with HfSiON indicates a slight increase of 9.8% as compared to the SiON dielectrics. This suggests a higher interface trap density variation for HfSiON dielectric. As a result the V_T variation can be attributed to an increase in HfSiON bulk defects.

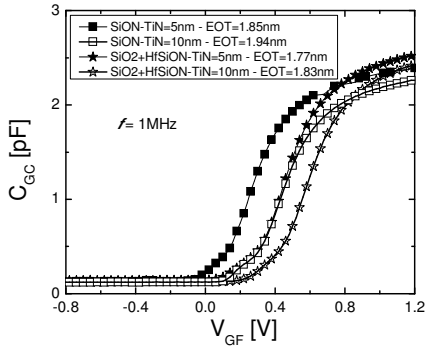

Fig.3: *Gate to channel capacitance (C_{GC}) as a function of the gate voltage for nMuGFETs with different TiN metal gate thicknesses and dielectrics.*

Considering the different TiN metal gate thicknesses, the EOT reduction with thinner metal gate should be the reason for the GIDL current increase as presented in Fig. 1. A thinner EOT (same dielectric) causes an increment of the transversal electric field E_s as presented in Eq. 1, and this increases the GIDL current (Eq. 2). Although for the high-k dielectrics (SiO_2 + HfSiON) in spite of the lower EOT, smaller GIDL is observed. In this case, a higher physical gate oxide thickness is observed, that can lead to a reduced E_s and GIDL.

In order to confirm this electric field variation, the Early voltage ($V_{EA} \cong I_D/g_D$) was also extracted through the output conductance (g_D) at V_{GT} =200 mV for the different TiN metal gate thickness and gate dielectrics. Lower V_{EA} is observed for thicker metal gate in Fig. 4 and this can be attributed to the lower GIDL. In summary, thicker TiN (higher EOT) leads to a reduction of the transversal electric field influence on the drain current. This emphasizes the horizontal electric field contribution and consequently decreases V_{EA} and GIDL. Lower V_{EA} is observed for the devices with a high-k gate dielectric (higher physical dielectric thickness) in agreement with the smaller GIDL current.

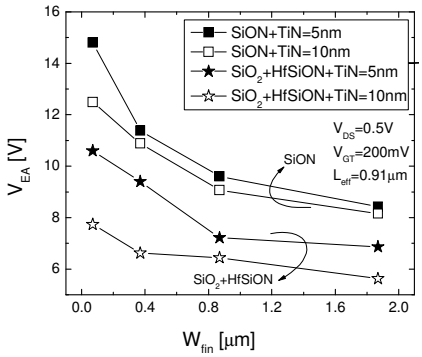

Fig.4: *V_{EA} as function of W_{fin} for different TiN metal gate thicknesses and dielectrics.*

5. Conclusions

In summary, in order to obtain higher GIDL, which is desirable for 1T-DRAM write condition a reduced physical gate dielectric thickness should be used. For the devices studied in this work the reduced physical gate thickness was obtained through thinner TiN (5nm) and a SiON gate stack. This phenomenon was also verified by looking the V_{EA} behavior. This V_{EA} increased for devices with reduced TiN metal gate thickness and for devices with a SiON gate dielectric. We also demonstrated that HfSiON gate dielectrics can achieve a smaller V_{EA} and GIDL.

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Effect of phonon confinement on heat dissipation in ridges

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1. Abstract

We have investigated experimentally the effect of lateral confinement of acoustic phonons in ridges as a function of the temperature. Electrical methods are used to generate phonons in 100nm large nanostructures and to probe the nanostructure temperature in the same time, what allows tracking the heat flux generated and its possible deviation to Fourier diffusive heat conduction.

2. Motivations

It is now well-established that Fourier's law of heat diffusion in solids breaks down when device sizes reaches the nanometer-scale [1]. Detailed studies of the characteristic lengths where the law has to be replaced or modified are required as these lengths might depend on the considered device geometries.

3. Fabrication of the nanostructures

We have fabricated special devices made of nanostructured ridges on top of planar substrate as represented on Figure 1. The top of a ridge is a wire made either of metal or of doped silicon that acts as a heater and as a thermometer in the same time. The lower part that supports the wire is made of an etched part of the wafer substrate. This type of structure enables to generate phonons in the ridge and to measure the heat flux flowing to the substrate.

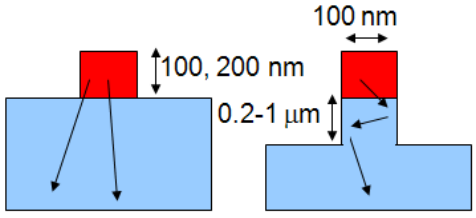

Fig.1: *Schematic of the nanostructures*

4. Measurement of the heat flux

Different electrical methods such as the 3ω method [2] are used to heat the wire. The goal is then to measure a wire-voltage component (dc or ac) proportional to the wire temperature. A model enables then to link the wire temperature to the heat flux transmitted to the substrate. In addition to the localized heat source effect due to the sub-mean free path size of the source [3], we have investigated experimentally the consequences of the fact that the source cannot be considered as a proper heat bath at equilibrium.

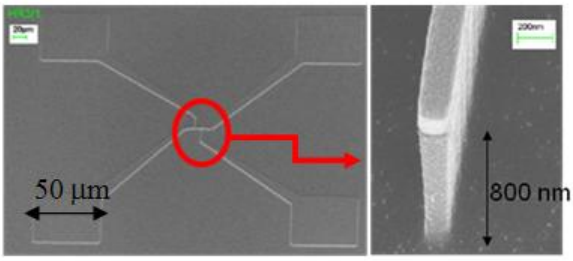

Fig.2: *Electrical accesses and ridge before mask removal*

4. Data analysis

We have quantified the effect as a function of the two characteristic numbers that can be associated with the problem, namely the constriction Knudsen number describing the transmission of the phonons and the nanostructure Knudsen number characterizing the nonequilibrium of the source. We compare our results with those of a recent theoretical paper [4] based on the ballistic-diffusive equations. The determination of the mean free paths of phonons as a function of the frequency remains a key point due to the consequences for heat transport and thermal management [1].

5. Conclusions

We observe a strong decrease of the thermal conductance through the ridge in comparison to a

prediction based on the Fourier diffusive as expected. But, more strikingly, we also observe a decrease in comparison to the ballistic prediction. We aim at ascribing part of this decrease to an effect of phonon confinement in the ridge.

5. Acknowledgements

We acknowledge the support of EU FP7 projects NANOPACK and NANOPOWER. We also acknowledge the support of Spanish MICINN project ACPHIN.

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Design of Silicon Double Gate Tunnel FETs with Ultra Low Ambipolar Currents

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1. Abstract

This work presents, through numerical device simulation, a study on the influence of the design parameters of the Tunnel Field Effect Transistors (TFET) on the ambipolar current. For the first time it is shown that top-and-bottom contacts structure limit the dependence of the ambipolar current on the gate voltage. It is also shown that structures with ultra low ambipolar current, totally independent of the gate voltage, are obtained by combining the layout of top-and-bottom contacts with low-k spacers.

2. Intorduction

The CMOS technology faces today many constrains related to the short-channel effects and the leakage currents that increase from one technological node to the next one. In this context, the static power dissipation became a huge problem. The Tunnel Field Effect Transistor (TFET) was proposed as a new possible solution to reduce the power dissipation. The TFET operates by quantum-tunneling effect and, therefore, does not suffer from the 60mV/dec subthreshold slope limitation, as does CMOS [1-3]. The TFET is different in its working principle from the MOSFETs. As the TFET is a reverse gated p-i-n junction, its conduction is based on the band-to-band tunneling. The tunneling should provide, in principle, better subthreshold swing than 60mV/dec, the minimum provided by CMOS [1-6].

However, TFET devices have to face two major road-blocks i.e. the intrinsic ambipolarity and the low I_{ON} current [4, 5]. The low I_{ON} influences negatively the switching speed, while the parasitic ambipolar current (I_{Amb}) would lead to a malfunction of the inverter-based logic. The large majority of the recent reports deal today with the improvement of the I_{ON} current of TFETs. Only a few of them targeted the suppression of the ambipolar current. In most of the cases I_{Amb} is reduced by the increase of the gate-drain distance [4, 5]. This results, however, in an expensive waste of Si surface. This work proposes an investigation on the reduction of the ambipolar current (I_{Amb}) as a function of the device design parameters.

2. Device Description and Results

The studied structures are Double Gate (DG) Si TFETs. The gate and the spacers are 30nm each. The Si film is 10nm thick, while the gate oxide is 3nm HfO_2 (ε_r=21). The source and drain doping are $2x10^{20}/cm^3$, p-type and n-type respectively. The tunneling junction is aligned with the left-hand side of the gate while the drain is aligned with the right hand side of the right spacer. Two different types of structures are studied: structures with the contacts on the sides (Figs. 1a and 2c) that correspond to the silicide contact structures and structures with the contacts layout on the top-and-bottom of the Si film (Figs. 1b and 2d) that correspond to the raised contacts structures. Two different possibilities are investigated for the above-mentioned structures: low-k (SiO_2) and high-k (HfO_2) spacer (Fig. 1).

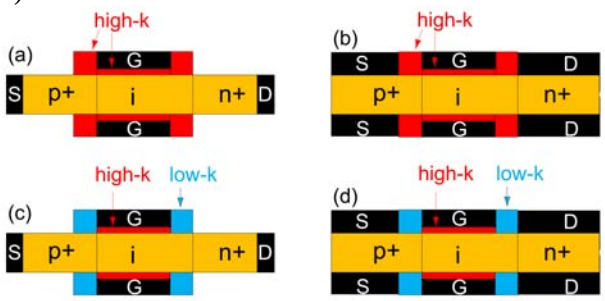

Fig.1: *Schematic representation of the studied devices: (a) high-k spacer, side contacts; (b) high-k spacer, top-and-bottom contacts; (c) low-k spacer, side contacts; (d) low-k spacer, top-and-bottom contacts.*

The devices transfer characteristics are presented in Figs. 2. The layout of the contacts does not influence the I_{ON} current. This result is normal, as the tunneling junction is aligned with the left-hand side of the gate. The impact of the nature of the dielectric spacer on the I_{ON} current was discussed elsewhere [6]. The ambipolar current is strongly influenced by the design of the structure. The ambipolar current presents a strong dependence on the gate voltage (Fig. 2a) for the side contacts and high-k spacer structure. The contacts layout on the top-and-bottom of the Si film proves to be

a powerful method to reduce the above-mentioned I_{Amb} dependence. I_{Amb} is lowered by almost six decades when the contacts are laid out in a top-and-bottom configuration with respect to the side contacts case (Fig. 2a). The comparison between the ambipolar current dependence in Figs. 2a and 2b reveals that almost the same reduction is obtained for the structures that use the contacts on the sides but with a low-k spacer. However, I_{Amb} loses two more decades and becomes totally independent of the gate voltage if the top-and-bottom contacts are used in combination with the low-k spacers (Fig. 2b).

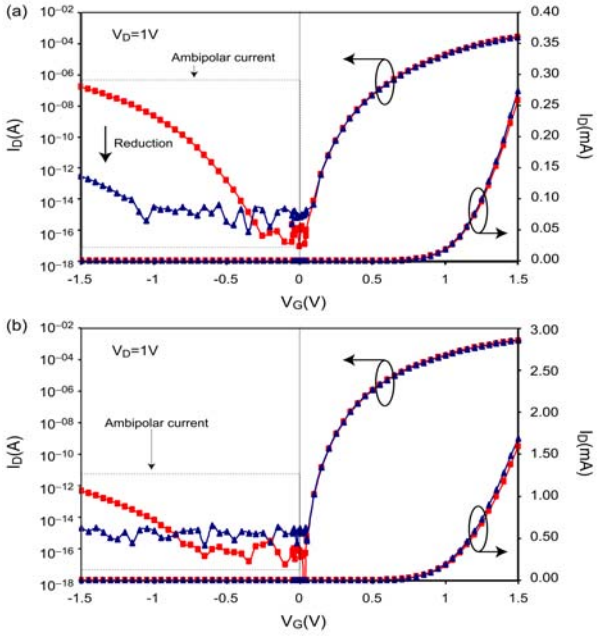

Fig.2: *Transfer characteristics of the studied devices: (a) squares: high-k spacer, side contacts; triangles: high-k spacer, top-and-bottom contacts; (b) squares: low-k spacer, side contacts; triangles: low-k spacer, top-and-bottom contacts.*

While the reduction of the ambipolar current by lowering of the permittivity of the spacer is normal and could be explained by the reduction of the coupling between the gate and the drain, the dependence of I_{Amb} on the layout of the contacts is not straightforward. The two-dimensional simulations present, in Fig. 3, the distribution of the potential in the worst-case conditions for the I_{Amb}. The potential distribution in Figs. 3 shows the concentration of the potential lines around the left-hand side of the drain for the side-contacts structure, while the potential is distributed much more uniformly inside the spacer for the top-and-bottom contact structure (Fig. 3b). As a direct consequence, for the side contacts, the electric filed is concentrated on the left-hand side part of the drain (Fig. 4a). The high electric field presence at the left of the drain leads to the increased parasitic ambipolar tunneling current for high negative gate voltage (Fig. 2a). Conversely, the uniform distribution of the potential lines inside the spacer for the top-and-bottom contacts leads to the uniform distribution of the electric field over the drain spacer. The uniform distribution of the field inside the spacer lowers the critical field on the parasitic tunnel junction, and therefore, reduces the parasitic ambipolar current (Fig. 4b).

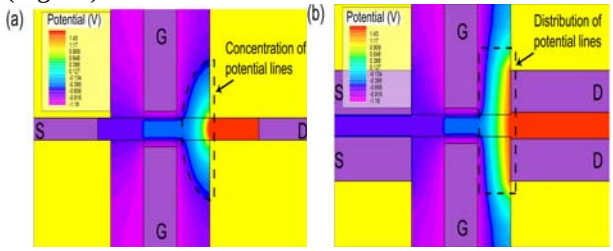

Fig.3: *Numerical simulation highlighting the distribution of the potential in the device for (a) high-k spacer, side contacts and (b) high-k spacer, top-and-bottom contacts. Worst case conditions for ambipolar current: V_G=–1.5V, V_D=1V, V_S=0V.*

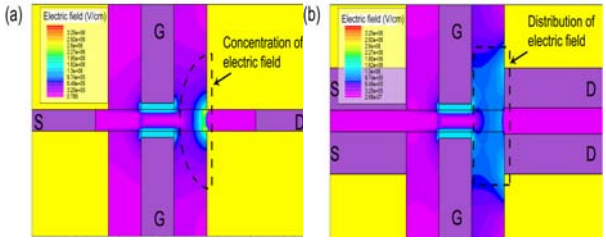

Fig.4: *Numerical simulation highlighting the electric field distribution in the device for (a) high-k spacer, side contacts and (b) high-k spacer, top-and-bottom contacts. Worst case conditions for ambipolar current: V_G=–1.5V, V_D=1V, V_S=0V.*

3. Conclusion

The influence of the design of the TFET device on the ambipolar current was investigated in this work. It was shown that the disposal of the contacts at the top-and-bottom of the Si film proves to be a very efficient method for the reduction of I_{Amb}, and a drop of 6 decades in the parasitic current was obtained in our simulations. The uniform potential distribution in the drain spacer, obtained for the top-and-bottom contacts, leads to the uniform field on the drain side and therefore the important reduction of the parasitic tunneling. It was also shown that for a 30nm structure, I_{Amb} can be reduced even further and becomes independent on the gate voltage if top-bottom contact structures are designed with low-k spacers.

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Study of Potential High-*k* Dielectrics for sub 15 nm UTB SOI MOSFETs, Using Analytical Models of the Gate Tunneling Leakage

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1. Abstract

Analytical models of the direct tunneling gate leakage current based on a proper description of the WKB tunneling probability and validated by TCAD simulation, were presented to determine the most promising dielectric materials for fully depleted UTB SOI MOSFETs with Equivalent Oxide Thickness (EOT) values and maximum values of gate leakage current according to the requirements of latest ITRS roadmap for two technological nodes.

2. Introduction

One of the key elements that allowed the successful scaling down of silicon based MOSFETs is the suitability of high *k* materials as a gate oxide dielectric. In fact the gate leakage tunneling current can be suppressed by using suitable high *k* dielectric materials [1, 2]. In our previous works we have studied the suitability of high *k* materials in Double-Gate SOI MOSFETs structure for the 22 nm node requirements assuming an ideal interface without any interfacial layer [3] and SiO_2 as an interfacial layer [4].
In this work, we have developed analytical models for the direct tunneling gate leakage current [5] through gate stacks based on a proper description of the WKB tunneling probability adapted to UTB SOI MOSFETs structure and we incorporate it to our new compact model for the potential and drain current of a UTB SOI MOSFET [6].

3. Simple analytical model with and without interfacial layer

A simple analytical model that includes some approximations for the direct tunneling leakage flowing between gate and channel as the main gate leakage component [5], using our new compact model of a UTB SOI MOSFET, was developed for the required conditions according to the requirements of ITRS (ITRS 2009) for the next generations of UTB SOI MOSFETs. The effects of the EOT, gate leakage current, electron effective mass in the high *k* dielectric materials (m^*), dielectric constant *k* value, barrier height and SiO_2 thickness as an interfacial layer were studied using the considered developed gate leakage tunneling current expressions.

4. Improved analytical model with and without interfacial layer

An improved analytical model can be obtained from the simple model by adding a correction function in order to take into account some effects that were not properly included in the simple model and lead to inaccuracies [7]. The direct tunneling gate leakage current as a function of gate voltage at $V_d = 0$ obtained by calculation of our model and TCAD numerical simulations is shown in Fig.1. There is a good agreement between model and simulation results.

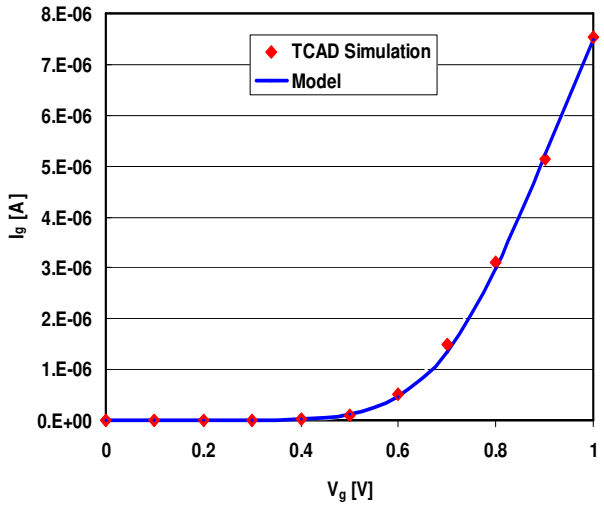

Fig.1: *Analytical model calculation and TCAD simulation for the gate leakage tunneling current for UTB SOI MOSFET.*

5. Results and discussion

We studied suitable high *k* materials by plotting band offset versus dielectric constant using the models for the considered conditions. Fig. 2 and Fig.3 show the most promising dielectric candidates for the given parameters

(mentioned in the captions) and latest ITRS requirements for two next generations of UTB SOI MOSFETs in the case of one layer and two layer gate insulators. Fig.3 shows that the most suitable dielectric candidates are such as HfO_2, ZrO_2 and La_2O_3 for the 14nm and 15nm nodes in the case of two layers insulators. The alternative dielectrics should satisfy the mentioned requirements.

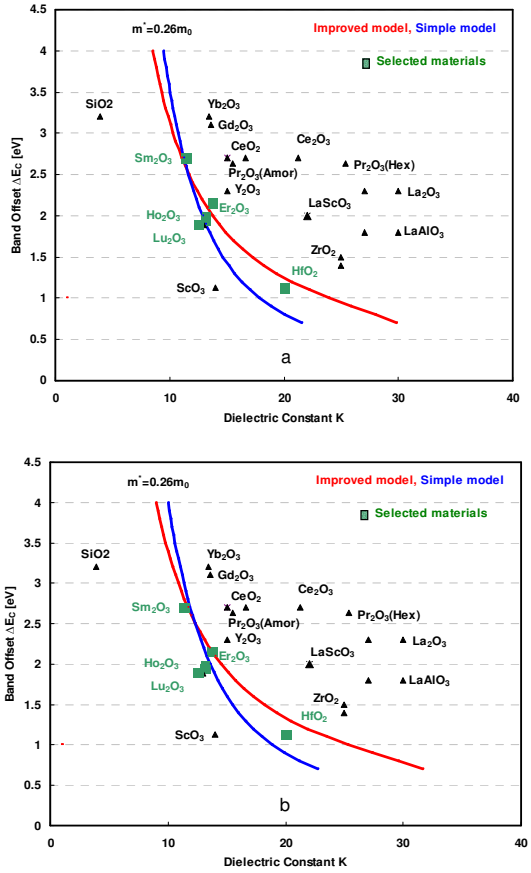

Fig.2: *Band offset as a function of k-value, for (a) 15nm node: EOT=0.85nm and J= 0.21 [A/cm^2] and (b) 14nm node: EOT=0.8nm and J= 0.23 [A/cm^2] according to ITRS at V_g = 1 V, m^*=0.26m_0 and V_d = 0 without interfacial layer.*

6. Conclusion

Analytical models of the gate tunneling leakage were developed to determine the most promising high *k* candidates for the UTB SOI MOSFETs structure for the requirements of low standby power applications according to the latest ITRS roadmap. Various issues/factors that need to be considered while replacing gate oxide materials have been studied to meet the requirements. Finding suitable materials depends on the technology node requirements and especially EOT, the electron effective mass and interfacial layer thickness, which can change the choice of the right dielectric candidate. HfO_2 and Lu_2O_3 are the most promising materials for the 14nm and 15nm nodes requirements assuming ideal case without interfacial layer.

Acknowledgements

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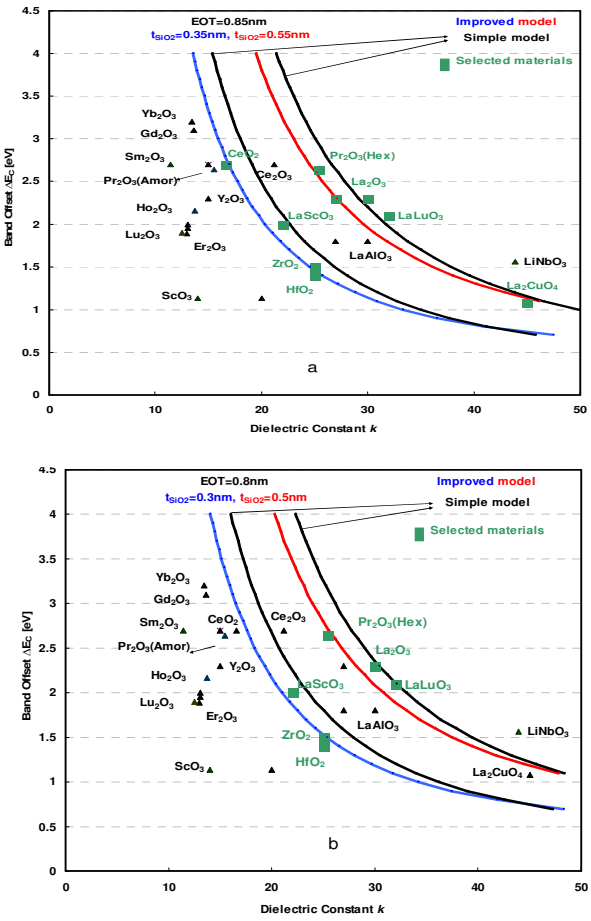

Fig.3: *Band offset as a function of k-value for (a) 15nm node: EOT=0.85nm and J= 0.21 [A/cm^2] and (b) 14nm node: EOT=0.8nm and J= 0.23 [A/cm^2] according to ITRS at V_g = 1 V, m_{sio2}=0.50m_0, m^*=0.26m_0 and V_d = 0 with SiO_2 as an interfacial layer.*

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Surface potential amplification model for the negative capacitance double-gate FET

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***Abstract*—It has been proposed in Ref. [1] that a ferroelectric material operating in the negative capacitance region could act as a step-up converter of the surface potential in a metal-ferroelectric-semiconductor structure, opening a new route for the realization of transistors with steeper subthreshold characteristics (*S*<60 mV/decade). In this work, a comprehensive physics-based surface potential model for the negative capacitance SOI double-gate field-effect transistor is reported. The model is aimed to evaluate the surface potential amplification capability. Additionally, this work clarifies how the negative capacitance operation region of the ferroelectric can be experimentally detected.**

I. INTRODUCTION

One of the most severe problems raised in the ITRS document [2] is the ever increasing power dissipation density at chip level caused by the relentless scaling down of transistors. This problem is often referred to as the power crisis in the microelectronics industry and its root can be traced back to the difficulty in increasing the transistor subthreshold slope, which, because of thermodynamic considerations, exhibits an apparent limit of S=60 mV/decade at room temperature, where S is an inverse slope. This apparent limitation has been termed the Boltzmann tyranny. Recently, it has been suggested [1] that a metal-ferroelectric-semiconductor (MFS) stack could provide a feasible solution to step-up the semiconductor surface potential (φ_s) above the gate voltage. The underlying idea consists in exploiting the negative capacitance (NC) region of the ferroelectric material (red dashed line in Fig. 1a), defined as $C_f=dQ/dV_f$, where Q and V_f refer to the charge density per unit area and the voltage drop in the ferroelectric, respectively. Provided the MFS stack could be operated in the region where $C_f<0$, the surface potential φ_s arising from the capacitance divider formed by C_f and the semiconductor capacitance, could be up-converted. This phenomenon might be used to enhance the electrostatic control of the gate electrode over the channel of a field-effect transistor (FET), thus opening a new route towards steeper subthreshold transistors exhibiting S<60 mV/decade. The NC-FET proof of concept has not been demonstrated yet, and still many open issues remain to be solved. At the time being, the main challenge is to identify a suitable MFS gate stack able to operate in the NC region with the consequent step-up conversion of the surface potential. In parallel with the efforts to demonstrate the concept, other developments have to be made in order to adequately model the surface potential up-conversion. To fill this gap, an analytic physics-based surface potential model for the NC-FET is proposed [3]. For the sake of simplicity, a double-gate (DG) geometry was assumed, although the model can be easily extended to other geometries such as for instance, single-gate or surrounding-gate geometries [4].

II. SURFACE POTENTIAL MODEL

Consider an undoped or lightly doped NC-FET with a symmetric DG geometry (Fig. 1b).

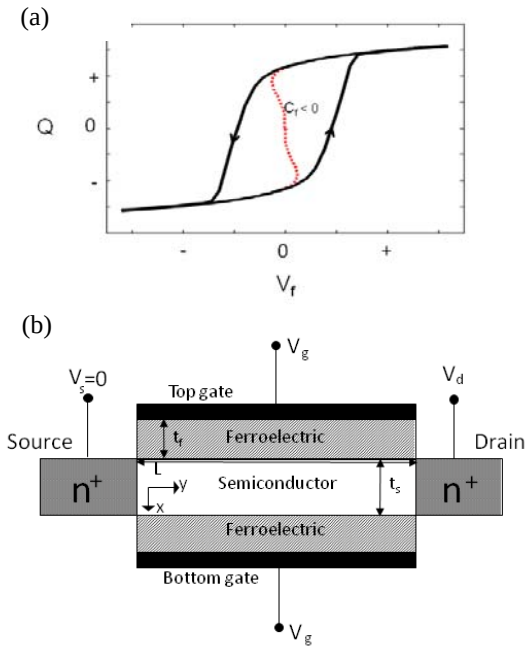

Figure 1. (a) Charge versus applied voltage in a ferroelectric oxide film. The solid line represents the typical hysteretic behaviour observed in experiments. The dotted line represents the negative capacitance region. (b) Cross-sectional view of a double-gate negative capacitance FET, showing the reference system considered in this work.

For this geometry the analytical solution for the electrostatic potential in the semiconductor can be written as [5]:

$$\varphi(x) = -\frac{2kT}{q}\ln\left[\frac{t_s}{2\beta}\sqrt{\frac{q^2 n_i}{2\varepsilon_s kT}}\cos\left(\frac{2\beta x}{t_s}\right)\right] \quad (3)$$

where β is a constant to be determined from the gate voltage equation:

$$V_g - \Delta - \varphi_S = a_0 Q + b_0 Q^3 + c_0 Q^5 \quad (4)$$

where V_g is the voltage applied to both gates, $\varphi_s=\varphi(0)$ and Δ the work-function difference between the gate electrode and the semiconductor. Note that the left side of (4) corresponds to V_f. The right side represents the Q-V_f characteristic of a ferroelectric oxide (Fig. 1a) given by the Landau-Ginzburg-Devonshire's (LGD) phenomenological theory, although a higher degree polynomial could be needed to properly describe the ferroelectric behavior. The coefficients a_0, b_0, c_0 are related to the Landau parameters a, b, c, of the ferroelectric material by the following relationships: $a_0=2t_f a$, $b_0=4t_f b$, $c_0=6t_f c$, where t_f is the ferroelectric film thickness. The coefficient $a_0 \sim 1/C_f$ represents the inverse of the ferroelectric capacitance at low V_f, and it is assumed to be $a_0 < 0$ as the key feature for up-conversion. From Gauss's law, the total mobile charge per unit gate area can be found from $Q=2\varepsilon_s(\mathrm{d}\varphi(t_s/2)/\mathrm{d}x)$, which equals $(2\varepsilon_s)(2kT/q)(2\beta/t_s)\tan(\beta)$. Substituting $Q(\beta)$ into (4) leads to:

$$\frac{q(V_g-\Delta)}{2kT} - \ln\left(\frac{2}{t_s}\sqrt{\frac{2\varepsilon_s kT}{q^2 n_i}}\right) = \ln(\beta) - \ln(\cos\beta) + a_0(2C_s)\beta\tan\beta + \\ + b_0(2C_s)^3\left(\frac{4kT}{q}\right)^2\beta^3\tan^3\beta + c_0(2C_s)^5\left(\frac{4kT}{q}\right)^4\beta^5\tan^5\beta \quad (5)$$

where $C_s=\varepsilon_s/t_s$ is a structural capacitance. Remarkably, (5) reduces to Taur's expression for a DG-MIS structure [7] after the identification $a_0=1/C_{ox}$, $b_0=c_0=0$, where C_{ox} represents the oxide capacitance. The range of β is $0<\beta<\pi/2$. For a given V_g, β is calculated from the condition $f(\beta)=(q/2kT)(V_g-V_0)$, where

$$V_0 = \Delta + \frac{2kT}{q}\ln\left(\frac{2}{t_s}\sqrt{\frac{2\varepsilon_s kT}{q^2 n_i}}\right) \quad (6)$$

In what follows, we examine the step-up conversion capability of the proposed device. We have assumed strontium bismuth tantalate (SBT) as the ferroelectric material, characterized by Landau parameters at room temperature: a=-1.3·10^8, b=1.3·10^{10}, c=0 (SI units). Figure 3 shows φ_s versus V_g for the MFS structure at room temperature for several t_f values, where t_s has been assumed to be 5 nm, and Δ=0 eV As a general rule, high-t_f values give rise to hysteretic behavior. Reducing t_f, hysteresis disappears and gain (G) >> 1 can be reached, where G is defined as $dQ/\mathrm{d}V_g$ (see the inset in Fig. 3). For low t_f values, the step-up conversion capability vanishes. As a consequence, a key part of the device design relies on tuning t_f. Interestingly, *the signature of operation in the NC region is a single-valued and peaked C_g-V_g characteristic* (Fig. 3b). A sharp peak is indicative of a large step-up conversion factor. For comparison, the C_g-V_g curve of an equivalent MIS structure with $C_{ox}=1/|a_0|$ is also shown. In summary, the step-up conversion capability could provide a key mechanism to obtain steeper subthreshold transistors.

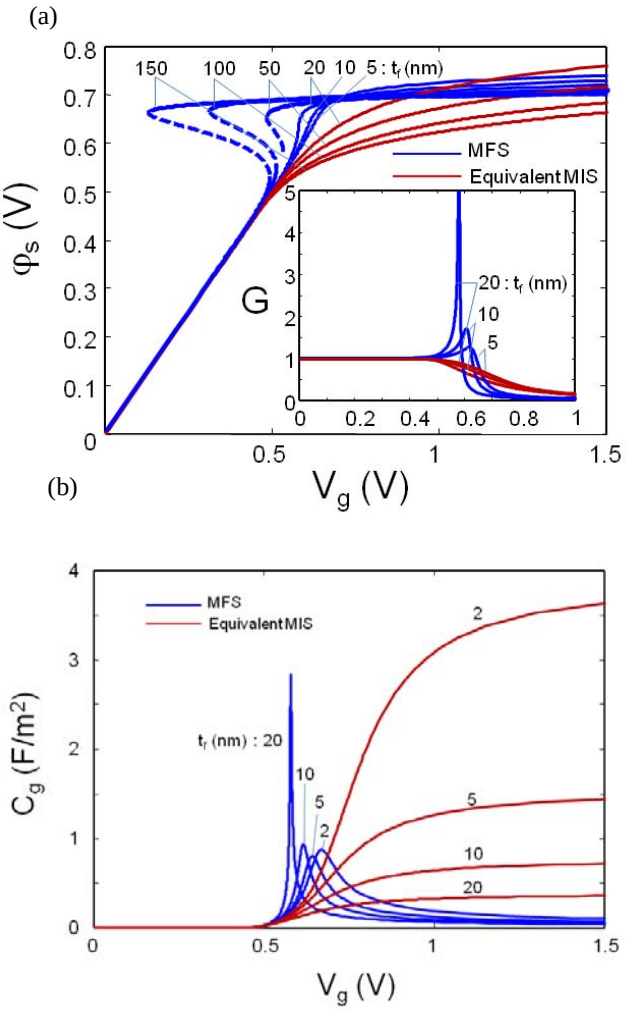

Figure 3. **(a)** Step-up conversion capability of the MFS structure as a function of the ferroelectric film thickness . Hysteretic behaviour arises for t_f values greater than 20 nm. The dashed blue line indicates the unstable region. For comparison, the surface potential of the equivalent MIS structure is shown. The inset shows the expected gain versus gate voltage. **(b)** The signature of operation in the negative capacitance region is a single-valued and peaked C_g-V_g characteristic. For comparison, the gate capacitance of the equivalent MIS structure is shown.

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Influence of single-atom impurity scattering on quantum transport in silicon nanowire transistors

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1. Abstract

In this paper we study the influence of impurity scattering due to a discrete donor atom in the channel of an n-channel silicon nanowire transistor. Using 3D quantum simulations, we show that a single donor impurity atom increases the off current by creating resonant energy levels in the channel and impact of impurity atom on the current below and above threshold region strongly depends on the distance from source-channel junction edge.

2. Introduction

As transistor gate length shrinks down to nanometer dimensions, device parameter variations due to random doping atoms in the channel region of silicon nanowire MOSFETs become important. Even in ideal processing conditions, the finite numbers of doping atoms in the channel region are placed at random due to the physics of ion implantation, doping diffusion and other processes involved in the doping of silicon device. In this paper we study the influence of a single donor atom on drain current using quantum mechanical approach.

3. Simulation approach

We have developed a three-dimensional simulation tool based on the non-equilibrium Green's function (NEGF) formalism in the coupled-mode space approach to study the effect of impurity scattering due to single donor atom in different channel region of undoped *n*-channel gate-all-around (GAA) silicon nanaowire. A single doping atom is represented by a small sphere with 0.5 nm diameter containing an equivalent doping concentration of $N_{atom}=1/V$, where V is the volume of the sphere. Then the Poisson equation will become [1]:

$$\nabla^2\Phi = -\frac{q}{\varepsilon_{si}}\left(p - n + N_{atom}\right)$$

Where Φ is the electrostatic potential, n is the electron density obtained from NEGF equations. We assume that the hole concentration p is negligible. We have used the fast coupled mode space approach (FCMS) to solve the quantum transport equation [2]. This method assumes that modes are coupled in the vicinity of the impurity while there is no mode coupling in other regions; hence the problem is reduced to solving coupled and fast uncoupled methods in each section of the nanowire.

3. Results and discussion

We have considered a GAA silicon nanowire with rectangular cross-section and $T_{si}=W_{si}=3nm$, a gate oxide thickness of 1nm, a gate length of L_g=10nm and a source and drain region length of 10nm. We define the distance *x-impurity* as the distance between the source-channel junction edge and the center of the impurity sphere as schematically shown in Fig. 1. Figure 2 shows the I_{DS}-V_{GS} curve for different locations of the impurity in the channel region at V_{DS}=0.4 V. As we can see introducing the impurity increases the off-current due to creation of resonance levels by the impurity as shown (Fig. 3). As the distance *x-impurity* is increased, the density of states (DOS) in the channel region increases and tunnelling through resonance levels becomes more probable and hence the off-current increases. This effect reaches a maximum when *x-impurity* becomes equal to $L_g/2$. We can observe a different trend for the current above threshold: up to a distance *x-impurity*=2.5nm, which is equal to $L_g/4$, we the magnitude of on-current increase as we increase *x-impurity*. However, if we increase *x-impurity* beyond $L_g/4$, the on-current starts to decrease. In order to understand the transport mechanisms involved above threshold, we have plotted the density of states for different values of *x-impurity* in Fig. 4. As we can see increasing the value of *x-impurity* moves the density of states to lower energies. When *x-impurity* becomes larger than $L_g/4$ the local DOS starts falling to energies below those of the available states in the source, making it impossible for the electron to tunnel through the impurity-induced energy levels. Hence the on-current becomes due to thermionic emission only and, therefore, decreases greatly. This quantum mechanical behaviour of carriers in the presence of random dopants in the channel region is completely different from that predicted by classical modelling. The most recent classical simulations claims that the threshold voltage variations due to random dopants is maximum when *x-impurity*=$L_g/2$ [1]. A recent study by three-dimensional quantum simulator on the effect of current variability due to random dopants from source/drain implantation in a silicon nanowire transistor has predicted the variation of the off-current [3]. However, this study lacks the complete study of random dopants on the full range of drain current values and in the channel region, which is essential for nanoscale MOSFET design.

4. Conclusions

Using three-dimensional quantum simulations, we study the influence of impurity scattering due to a single doping atom on the drain current of a silicon nanowire transistor. The introduction of a doping atom in the channel region creates resonance levels in the channel, which gives rise to tunneling from source to drain. These resonance levels always increase the current below threshold, while of the influence of the atom on the current above threshold strongly depends on the position of the atom in the channel.

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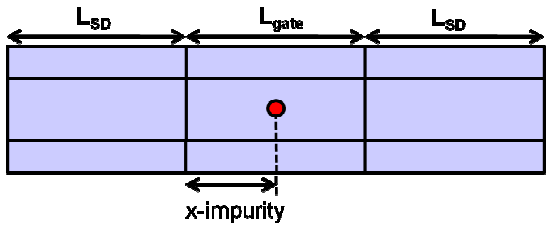

Fig.1: *schematic representation of a GAA nanowire transistor. x-impurity is the distance between source-channel junction edge and the center of the impurity sphere.*

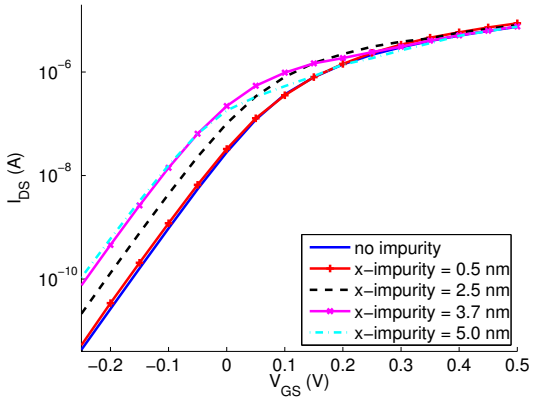

Fig.2: *I_{DS}-V_{GS} curve at V_{DS}=0.4 V for different values of x-impurity. The off-current always increase with x-impurity, however on-current start to decrease for x-impurity greater that 2.5nm.*

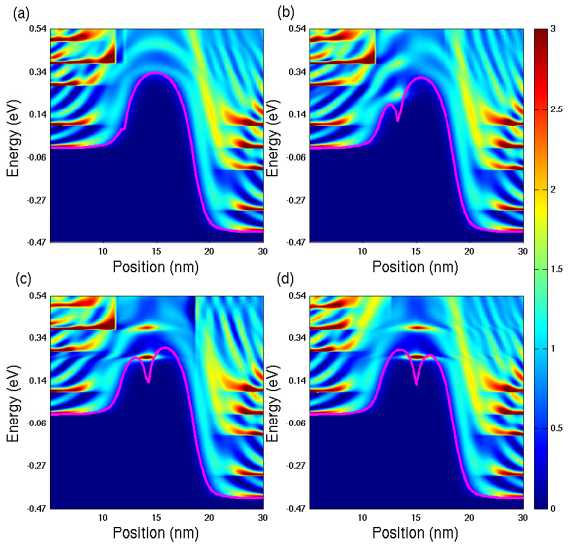

Fig.3: *Density of states(DOS) for V_{DS}=0.4 V and V_{GS}=-0.2 V for different values of x-impurity as shown in Fig. 2.as we can see impurity has created extra DOS in the channel region, which leads to high tunnelling current below threshold.*

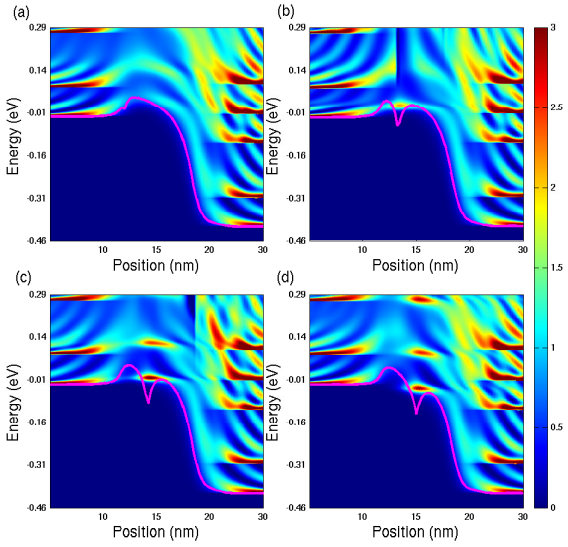

Fig.4: *Density of states (DOS) for V_{DS}=0.4 V and V_{GS}=0.2 V for different values of x-impurity as shown in Fig. 2. In Fig. 4d we can see that the extra DOS levels created by impurity have energies below those of the DOS in the source, which results in drastic reduction of on-current by annihilating the tunnelling current.*

Charging Effects in the MOS Structures with Silicon Nanocrystals Embedded in SiO_2.

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1. Abstract

MOS tunnel structures with a gate stack containing silicon nanocrystals embedded in SiO_2 were fabricated by deposition of a layer of silicon nanodots on the silicon substrate and its subsequent thermal oxidation. The current- and capacitance-voltage characteristics of the structures were measured and discussed.

2. Introduction

The MOS gate stacks with nanocrystalline quantum dots (NQD) embedded in an insulator can be exploited in a range of memory and single electron devices. If the barrier layers separating the nanocrystals from the silicon substrate and the gate electrode are in the range of few nanometers, the crystals can exchange electric charge with the outer electrodes via tunneling. In the paper, we report fabrication of MOS structures containing silicon nanocrystals embedded in SiO_2 and investigate charging effects taking place in the diodes.

3. Fabrication

The MOS diodes were fabricated on <100> phosphorus doped silicon wafers with the resistivity of 2.9-4.1 Ωcm. After conventional cleaning, thermal oxidation at 800°C in oxygen was performed on the wafers marked as *O* while the wafers marked as *S* were left bare. Next, the toluene solution of Si-nanodots was deposited by spin coating followed by low-temperature anneal to drive solvent out on both types of the wafers. The average size of the nanodots was specified by the supplier as 50 nm. Then, the deposited layers were thermally oxidized at the temperature of 800°C. The aluminum electrodes of the diameter of 540 μm were evaporated on the top surfaces of both types of wafers. After etching of the backside oxide, the aluminum contacts were evaporated.

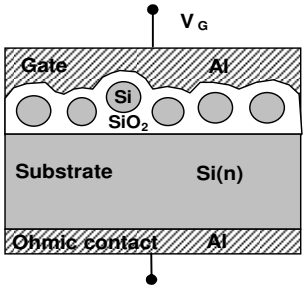

Fig.1: *The expected structure of the fabricated diodes.*

Figure 1 illustrates the expected physical structure of the diodes. The bottom oxide layer for the *O* diodes is expected to be thicker than for the *S* diodes. The spin coating process may result in the mono- or multilayer nanodots film.

4. Measurements

The current and capacitance characteristics of MOS structures were similar for both the *O* and *S* samples. Both the current-voltage and capacitance-voltage characteristics exhibited hysteresis resulting from the electric charging of the gate stack.

Figure 2a shows the current-voltage characteristics of the *S*-type structure measured for two directions of the voltage sweep – forward: from minus to plus, and then, reverse: from plus to minus. The characteristics were measured in the standard way, i.e., a successive voltage with a step ΔV_G was applied across the structure and the gate current was measured after a certain default time and an additionally defined delay time. In the case of Fig. 2a, the time between the subsequent measure-ments at no delay time was equal to about 0.8 s. Figure 2b shows the results of the same measurement performed at slow voltage sweeps (notice the increased delay time and the tenfold reduced voltage step ΔV_G). At large negative and positive voltages the current strongly increases probably as a result of Fowler-Nordheim tunneling through the SiO_2 layer adjacent to the emitter region. The current in the middle bias range depends on the rate and direction of the voltage sweep and reflects the charging processes of the silicon crystals. In this bias range, the *I-V* dependence exhibits a hysteresis at the negative gate voltages and additional current pulses for the fast reverse sweep (Fig. 2a) and the slow forward sweep (Fig. 2b). Fig. 3 compares the *I-V* characteristics for the *O*-type structure at different voltage sweeps.

Figure 4 shows the capacitance-voltage characteristics for the *S* and *O*-type structures measured for the fast forward and reverse sweeps (no delay time). The standard analysis leads to the theoretical C-V curves corresponding to the equivalent oxide thicknesses of 6.02 nm and 6.75 nm, donor concentration $2.7 \times 10^{15} cm^{-3}$ and oxide effective charge $3 \times 10^{12} cm^{-2}$ and $2.2 \times 10^{12} cm^{-2}$, respectively A hysteresis at the flat-band capacitance level corresponds to the incremental effective oxide charge of about $5 \times 10^{11} cm^{-2}$ for the *S*-type structure.

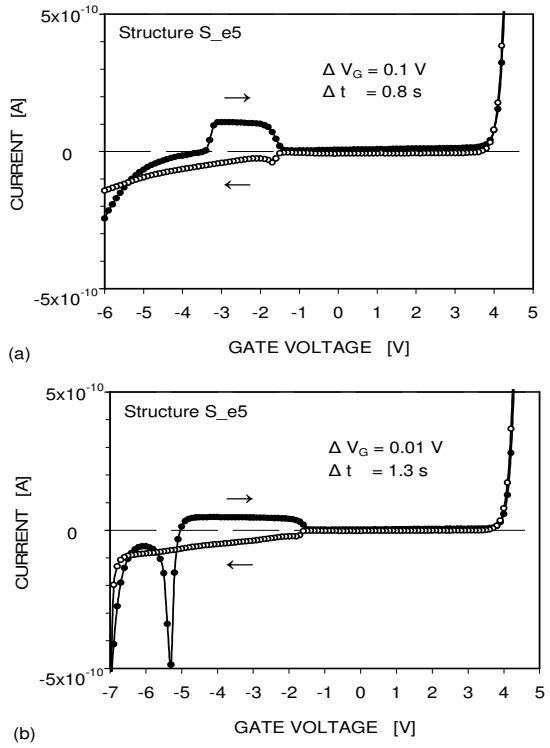

Fig. 2: *Current-voltage characteristics of the S-type structure measured at different voltage sweep rates: (a) fast sweep: $\Delta V_G/\Delta t$=125 mV/s, (b) slow sweep: $\Delta V_G/\Delta t$= 7.7 mV/s.*

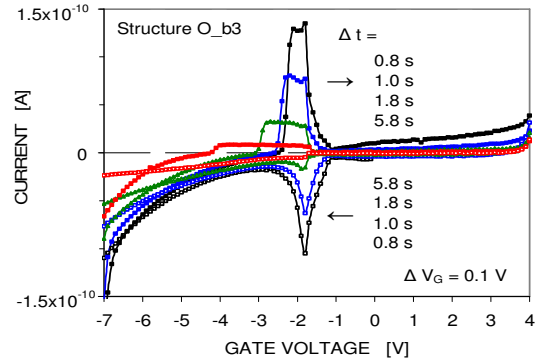

Fig. 3: *Current-voltage characteristics of the O-type structure measured at different voltage sweep rates.*

In order to facilitate an interpretation of the results shown in Fig. 3, the *C-V* characteristics of the O-b3 structure measured for different forward and reverse bias sweeps are shown in Fig. 5 in the $1/C^2$ scale. The current spikes for the forward sweeps in Fig. 3 correspond to the strong inversion in the silicon substrate, where the high-frequency capacitance does not depend on the gate voltage.

Figure 6 shows the time decay of the gate current after jump of the bias voltage from zero to large negative value. Large time constant of the second phase of this process suggests tunneling of electrons from the gate to the silicon crystal as a charging mechanism.

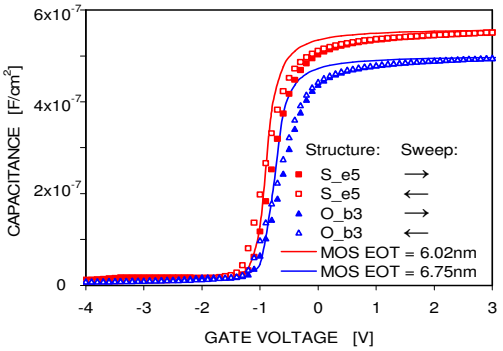

Fig. 4: *Measured capacitance-voltage characteristics and the theoretical characteristics of the equivalent MOS structures.*

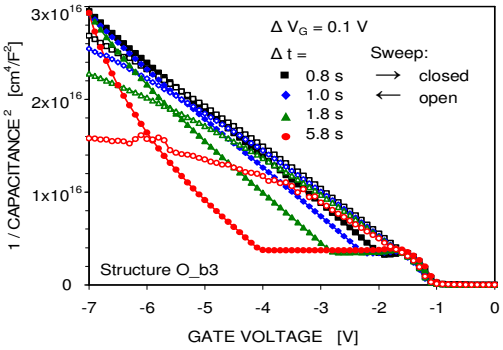

Fig. 5: *Capacitance-voltage characteristics of the S-type structure measured at different voltage sweep rates.*

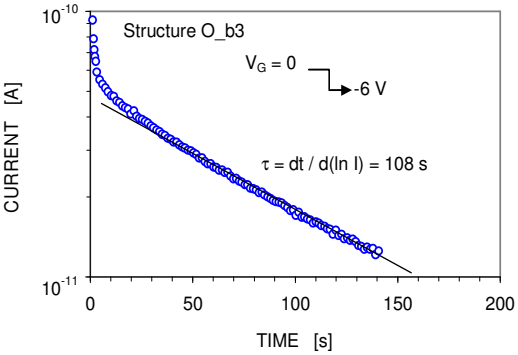

Fig. 6: *Time decay of the current charging the gate stack at large negative voltage.*

5. Conclusions

Electrical measurements performed did demonstrate device grade characteristics of the MOS gate stacks with silicon nanodots embedded in gate oxide. The observed charging effects result from the presence of Si nanodots in SiO_2. Further studied are needed to explain physical effects taking place, including in particular the exact nature of the charge transport mechanism.

Acknowledgments

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Rotated SOI MuGFETs at High Temperatures

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1. Abstract

This work presents a study of the influence of a 45° fin rotation on the main MuGFETs electrical parameters like gm_{max}, V_{TH}, DIBL, R_{SD}, V_{ZTC} at high temperatures (in a range of 298 K to 473 K) through experimental results. All the analysis was done comparing the results of MuGFET rotated devices with non rotated ones fabricated on the same wafer.

2. Introduction

In order to continue reducing the channel length of the devices and improve the speed of integrated circuits it is necessary to use new materials and architectures. The 3-D multiple-gate architecture improves the control of the charges in the channel which decreases the short channel effect [1]. There are different technologies in order to improve the mobility in MuGFET devices, such as introducing mechanical stress in the channel and rotating fin over 45° in order to change the crystallographic orientation., According to the theory, depending on the direction of the current flow, the electron mobility may degrade and in the case of MuGFETs the mobility degradation for electrons occurs in the (110) crystal orientation. Despite the regularity of the crystal, the space distribution of the atoms changes when the crystal is viewed in different directions (Fig. 1), according to that, properties as mobility, piezoresistive and piezoelectric coefficients depend on the direction inside the crystal. If the transistor layout is rotated 45º in the plane of the wafer, the sidewall crystalline orientation becomes (100) which enhance the electron mobility of the devices [2, 3].

The goal of this work is to study the main electrical parameters of 45° rotated MuGFETs in comparison to the non rotated one (reference) at high temperatures.

3. Device Characteristics

The studied MuGFETs in this work are state-of-art n-channel triple-gate transistors. The devices were fabricated on SOI wafers with 150 nm and 1.9 nm of buried oxide and a gate EOT, respectively. The gate stack consists of 2.3 nm HfSiON on 1 nm SiO_2, capped by 5 nm of TiN and 100 nm of polysilicon. Different effective channel lengths were considered with W_{FIN} of 20 nm. Selective epitaxial growth of the source and drain regions was used in these devices. More detail on the devices fabrication can be found in [4].

4. Results and Analysis

Fig. 2 illustrates the experimental gm_{max} as a function of the temperature for short and long channel lengths in the linear region. It is possible to observe that for large channel lengths the rotated devices present a better behavior, i.e., higher mobility compared to the reference one. This result has explained in [3] by the (100) sidewall crystal orientation improving the electron mobility [5]. Analyzing the short channel devices (60 nm and lower), an opposite behavior is obtained which can be attributed to the higher parasitic series resistance present in rotated devices as observed in figure 4. However, in the saturation region (V_{DS} = 1.2V) one can notice that the rotated devices show higher gm_{max} for all channel lengths studied once that in this case the channel resistance is higher than in linear region (Fig. 3).

The total resistance R_{TOTAL} was obtained by V_{DS} over I_{DS} with a fixed gate voltage overdrive V_{GT} = 0.6 V and it was observed that reference devices present higher values of R_{TOTAL} when long channels are used. For this condition the R_{SD} (parasitic source/drain resistance) is negligible, so that the increase in the R_{TOTAL} can be related to the lower transconductance and consequently, a lower mobility is obtained for reference devices compared to rotated ones. As the channel length becomes shorter there is an inversion of this behavior and rotated ones offer a higher R_{TOTAL}. In this case the R_{SD} cannot be neglected and its value is the main part of R_{TOTAL}. As expected there is an increase of this parameter with the temperature for both technologies.

The R_{SD} was estimated from $I_{DS}xV_{GS}$ curves using the method proposed by Terada and Muta [6] as shown in fig. 4. In terms of temperature, it is possible to see an increase of R_{SD} with the temperature. This is due to the resistivity increase in source and drain and in the LDD regions (extension regions) [7] for both rotated and reference devices. Also, rotated devices present higher R_{SD} compared to the references ones and a possible explanation for that can be associated to the different diffusion coefficient for each direction which results in different doping profiles. As seen in figure 2 for short channel lengths, the rotated devices have lower gm_{max} and consequently lower mobility which means an increase of the resistance.

The threshold voltage was also studied (fig. 5) and it can be observed that 45° rotated transistors yield about 30 mV higher V_{TH} than the reference devices for short and long channel lengths. The change in the band structure which is responsible to the different values of effective masses in (100) direction [8] could be related to V_{TH} increase. V_{TH} decreases with temperature rise at a rate of -0.53 mV/K for long channel devices and, - 0.63 mV/K for short channel devices. The value of about -0.57 mV/K for MuGFETs has been reported in previous work [7].

The Drain Induced Barrier Lowering Effect (DIBL) was also investigated in these devices. The DIBL values show a change in the threshold voltage caused by the decrease of the source potential barrier due to the increase in drain voltage. The decrease in the potential barrier is associated with the decrease of the charges in the channel region what means that short devices are more susceptible to the effect. DIBL is presented in

figure 6 for three different temperatures as a function of channel length. The values of DIBL are almost the same when the temperature changes and a variation of less than 20 mV/V is observed, indicating a temperature-independent drain-induced barrier lowering [7]. Comparing reference and rotated devices, for short channel lengths (60 and 50 nm) DIBL is larger in the latter, suggesting that the band structure changing in (100) direction can induce a higher DIBL in rotated devices.

Table 1 describes the Zero-Temperature-Coefficient (ZTC) point. The ZTC point represents the gate bias which ensures that the drain current remains constant with temperature variations [9]. This point is reached when the temperature mobility reduction compensates the threshold voltage shift with temperature. The decrease of mobility and threshold voltage are the main contributing factors to the position of the ZTC point [10]. At high V_{DS} both types of devices have similar values of ZTC point, in spite of the fact that they present a difference of about 30 mV in V_{TH}. This is due to the higher gm degradation factor (c) which compensates the impact of the V_{TH} change on the ZTC point. However, at low V_{DS} the gm degradation factor is not so strong influenced so that the ZTC point follows the same tendency as V_{TH}. Moreover, at low V_{DS} it can be noted that V_{ZTC} is lower for short channel lengths due to the lower V_{TH} obtained. These behaviors were also verified by the model presented in [11] and compared with the experimental results of table 1, presenting a maximum error of 7 %.

The subthreshold slope versus temperature for different L is presented in fig. 7. It is observed that for long channel lengths the S is near to the ideal value, while for short channel lengths the subthreshold slope is higher due to SCE in both devices (reference and rotated) and follow the same tendency at high temperature.

5. Conclusions

The behaviour of rotated devices at high temperatures is experimentally investigated. It was observed that in the linear region, rotated devices present a better gm_{max} for long channel lengths while the opposite is found for short channel devices. It was also observed that rotated ones present a higher R_{TOTAL} due to the higher R_{SD} for short channel lengths. On the other hand, in the saturation region the gm_{max} is higher for all channel lengths studied, presenting a lower degradation as a function of the temperature. In terms of DIBL, rotated devices showed higher values for short channel devices which suggest an influence of the change in the band structure. In the ZTC point at saturation both devices (reference and rotated) show the same values in spite of the difference of about 30 mV in V_{TH}. On the other hand, in the linear region the ZTC point followed the same tendency as V_{TH}, i.e. ZTC is higher for rotated devices. The rotated devices do not present differences in subthreshold slope compared to the reference devices at high temperature.

Acknowledgments

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Table 1: *ZTC point and gm degradation factor comparison for the different device types studied from 298 K to 373 K.*

	V_{DS} = 50 mV				V_{DS} = 1.2 V			
	Reference		Rotated 45°		Reference		Rotated 45°	
L(nm)	V_{ZTC}	c	V_{ZTC}	c	V_{ZTC}	c	V_{ZTC}	c
910	0.57	1.51	0.59	1.64	0.71	1.53	0.72	1.63
60	0.53	0.99	0.56	0.94	0.72	0.88	0.73	1.15

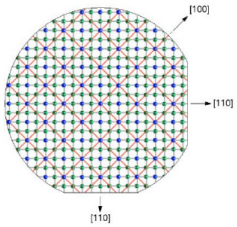

Fig.1.: *Crystal planes in the Si layer.*

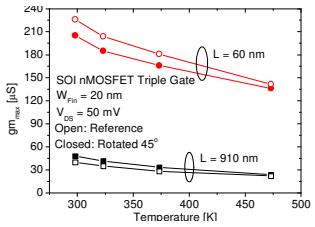

Fig.2.: *gm_{max} as a function of the T for short and long L at the linear region.*

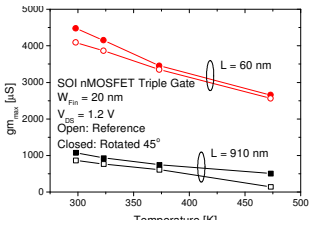

Fig.3.: *gm_{max} as a function of the T for short and long L at the saturation region.*

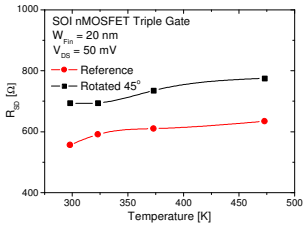

Fig.4.: *R_{SD} as a function of the temperature.*

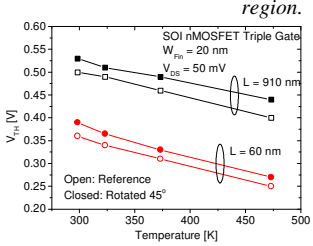

Fig. 5.: *V_{TH} as a function of the T for short and long L.*

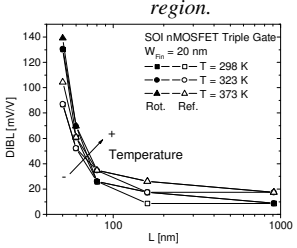

Fig. 6.: *DIBL as a function of L for different temperatures.*

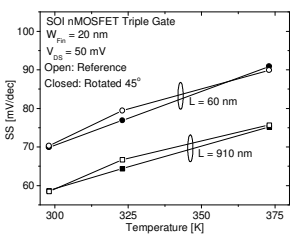

Fig.7.: *SS as a function of T.*

A Short-Channel Analytical Model for Triple-gate and Planar FDSOI Transistors

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1. Abstract

A short-channel analytical model for Triple-gate FETs (TGFETs) and planar Fully Depleted SOI (FDSOI) transistors is presented. The drain current characteristics are calculated in the subthreshold and strong inversion regime, and interpolated in the moderate inversion regime. The model is physics-based and features only two fitting parameters related to the smoothing functions used in the moderate inversion regime. It is experimentally validated for TGFET/planar FDSOI transistors with different gate widths and lengths.

2. Introduction

With the possible replacement of traditional bulk architectures by SOI in next technological nodes, Multiple-gate transistors are promising candidates [1]. TGFETs (Fig. 1) have the advantage of excellent front-gate control, and therefore relaxed scaling constraints. Planar FDSOI MOSFETs feature more on-state current compared to TGFETs but weaker gate control requiring more aggressive film thinning. There is currently a strong need for models of such architectures, in order to calibrate precisely their dimensions and evaluate their circuit performance.

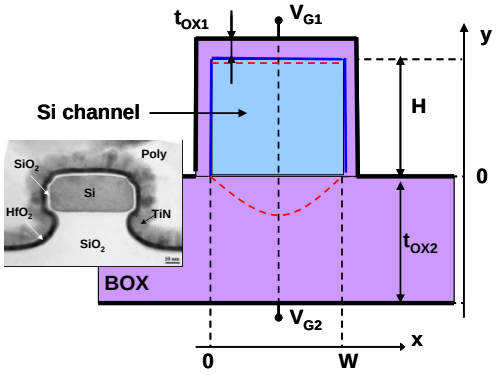

Fig.1: *TEM image and transversal cross-section of a TGFET with the notations used in this work.*

3. Analytical Model Derivation

Weak inversion – In the weak inversion regime and for undoped devices, the Poisson's equation reduces to the Laplace's equation, and the 3D potential in the structure can be expressed as a Fourier series [2][3]. It has been shown previously [1] that the value of the potential minimum is a good approximation to calculate the subthreshold current (the so-called 'most leaky path').

Once the position and value of the body potential in the source/drain direction is calculated, the minimum potential along the 'most leaky path' is integrated with mathematical simplifications. Calculation details are given in [2,3]. The drain current $I_{D,WI}$ in weak inversion is expressed as:

$$I_{DS,WI}(V_{G1},V_{DS}) = \frac{qn_i\mu V_t}{L_G}(1-e^{-V_{DS}/V_t})\times \left[WH\frac{2e^{\phi(\frac{W}{2},e_{OV},Z_C)/Vt}+e^{V_{G1}/Vt}}{3}\right] \quad (1)$$

with μ the mobility, V_t the thermal voltage, W the channel width, H the channel height, L_G the gate length, V_{DS} the drain to source bias, V_{G1} the front gate bias. φ(x,y,z) is the potential calculated with the Fourier series, and Z_C is the position of the potential minimum along the source/drain axis.

Strong inversion - The drain current in the strong inversion linear regime is expressed as:

$$I_{D,SI}(V_{G1}) = \mu C_{OX1}\frac{W+2H}{L_G}V_{DS}\eta_1 \ln\left[1+\exp\left(\frac{V_{G1}-V_{TH}-V_{DS}/2}{\eta_1}\right)\right] \quad (2)$$

with C_{OX1} the gate oxide capacitance, V_{TH} the threshold voltage (obtained with (1)), and η_1 a fitting parameter.

This modified expression from the 'traditional' current equation in strong inversion makes it tend smoothly toward 0 in weak inversion, and ensures a smooth transition between the different regimes (see later). We consider a full description of the effective mobility μ [4]:

$$\mu(V_G) = \frac{\mu_{0,EFF}}{1+\theta_1(V_G-V_T)+\theta_2(V_G-V_T)^2} \quad (3)$$

with $\mu_{0,EFF}$ the low-field effective mobility, and θ_1/θ_2 the mobility attenuation factors.

Moderate inversion, total characteristics – The case of moderate inversion is more difficult to reproduce since neither the approximations holding for weak or strong inversions can be applied. In order to obtain the complete $I_D(V_{G1})$ characteristics, we propose a simplified formula connecting the weak and strong

inversion regions. Using Eqs. (1) and (2) we express the total drain current as:

$$I_{D,TOT}(V_{G1}) = \left(\frac{I_{D,SI}(V_{G1})^{1/\eta 2}}{1 + \left(\frac{I_{D,SI}(V_{G1})}{I_{D,WI}(V_{G1})} \right)^{1/\eta_2}} \right)^{\eta_2} \quad (4)$$

with η_2 a fitting parameter.

The analytical model for $I_{D,TOT}$ in (4) includes the short-channel effects. The model is compared in Fig. 2 with experimental data for short-channel TGFETs featuring different channel widths. The model is able to reproduce accurately the transistor characteristics. Note the degradation of the subthreshold slope which occurs when the channel width increases because of the smaller control of the front gate on the channel.

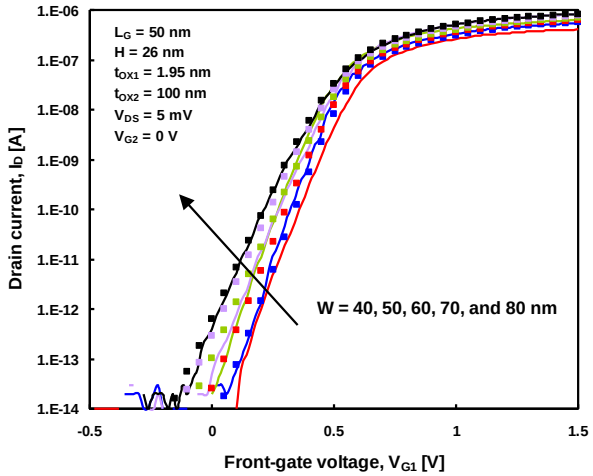

Fig. 2: *Analytical (symbols) and experimental (solid lines) drain currents I_D vs. front-gate bias V_{G1} for gate widths W from 80 nm down to 40 nm. Channel length L_G = 50 nm, channel height H = 26 nm, t_{OX1}=1.95 nm, t_{OX2} = 100 nm.*

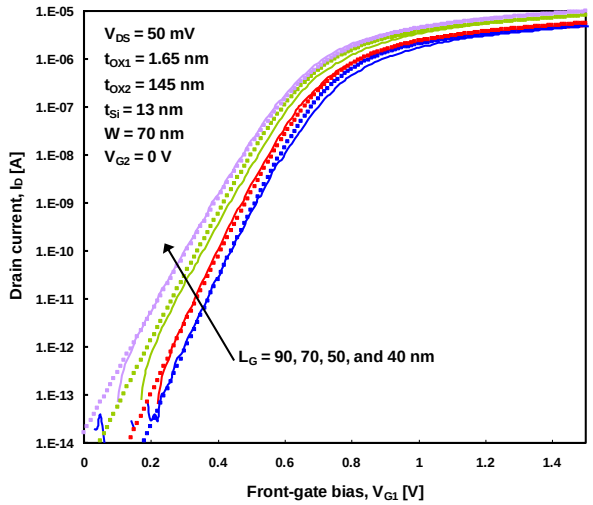

Fig. 3: *Analytical (symbols) and experimental (solid lines) drain currents I_D vs. front-gate bias V_{G1} for gate lengths L_G from 90 nm down to 40 nm. Channel width W = 70 nm, channel height t_{Si} = 13 nm, t_{OX1}=1.65 nm, t_{OX2} = 145 nm.*

The model can be straightforwardly extended to the case of fully depleted transistors (channel thickness t_{Si} << channel width W). The agreement between experimental devices (fabrication details and performance are given in [5]) and model for a fixed gate width and gate lengths from 90 to 40 nm is good (fig. 3). The dependence of the subthreshold slope to the gate length is correctly reproduced. It is noteworthy that planar FDSOI devices, even if often considered as purely 2D devices, might have narrow channels (e.g. W = 70 nm in this work). Our model, being in essence a 3D model, is able to capture the narrow-channel effects. Additional characteristics (transconductance, DIBL, etc) will be exposed and discussed. Additionally, it is noteworthy that since this model does not imply the charge sheet approximation, it can be used for UTB (Ultra Thin Body) FDSOI transistors like the one used in this work (t_{Si} = 13 nm).

4. Conclusions

In this work, a short-channel analytical model for TGFETs is presented. The drain current characteristics is calculated in the subthreshold and strong inversion regime, and interpolated in the moderate inversion regime. The model is fully physical, and features only two adjustment parameters related to the smoothing functions used in the moderate inversion regime. Additionally, it is demonstrated that the model can be extended to wide channel devices behaving as planar FDSOI MOSFETs. The model is also able to account for short and narrow channel effects. Finally, this analytical model can be used for device optimization and circuit applications.

Acknowledgements

This work was supported by the European Union IAPP FP7 'Marie Curie' COMON (COmpact MOdeling Network) project (ref. pro. 218255). Support from NANOSIL (contract 216171) and EUROSOI+ (contract 216373) contracts of the European Commission, the Spanish Ministry of Science under TEC2008-06758-C02-02/TEC, PGIR/15 grant from URV and ICREA Academia Prize are also greatly acknowledged.

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An inversion charge model for n-type and p-type DGMOSFETs accounting for different substrate orientations

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1. Abstract

An advanced inversion charge model for n-type and p-type symmetrical Double-Gate MOSFETs (DGMOSFETs) is presented. The role of different crystallographic orientations was successfully taken into account by including quantum mechanical effects (QMEs). Self-consistent Poisson and Schrödinger simulators were used to develop the model.
The validity of the model was checked for the three common wafer orientations (001), (011) and (111) and for devices with different silicon layer (t_{Si}) and oxide (t_{ox}) thicknesses. The model reproduces correctly the simulation data both in the subthreshold and in the strong inversion operation regime.

2. Introduction

Double-Gate MOSFETs (DGMOSFETs) are among the most promising devices in order to fulfil the future needs of scaling for the integrated circuit industry [1, 2]. The use of two gates (as well as a higher number of gates, such as in FinFets, Gate All Around devices, etc.) has demonstrated good electrostatic control of the channel charge. In these devices, drain-induced barrier-height lowering (DIBL) and threshold voltage roll-off are greatly reduced. The sharper subthreshold slopes (close to 60 mV/dec) characteristic of DGMOSFETs lead to a larger gate overdrive for the same power supply and the same off-current.
QMEs significantly affect the characteristics of MOSFETs [3, 4]. The inversion charge quantization obviously depends on the crystal orientation. Transistors fabricated in different crystal orientated substrates are becoming of great interest due to the fact that the carrier mobility can be largely enhanced. It has been shown that MOSFET mobility depends both on the substrate orientation and on the current flow direction; in fact, for p-MOSFET, hole mobility is 2.5 times higher on (011) substrates than on conventional (001) substrates. In addition, the adoption of vertical device structures such as the FinFET makes different surface orientations be easily achieved without having to use non-standard wafer substrates.
DGMOSFETs are currently subject of important efforts from the modeling point of view [5-6] because of the great need for accurate compact models that will show up in EDA tools in the future for circuit design purposes. In this context, we introduce our model.

3. Simulator description

The simulator used self-consistently solves Poisson and Schrödinger equations in DGMOSFET structures [3, 4]. For n-type devices we calculated the effective masses in our system assuming parabolic bands. Then, we empirically add a correction factor α following Kane's model [3]. For p-type double-gate SOI devices, the valence band structure properties were obtained by means of a fully self-consistent solver for the $\mathbf{k}\cdot\mathbf{p}$ and Poisson equations [4].
We have simulated symmetric DGMOSFETs. For each silicon layer thickness, three simulations were performed to study the influence of different crystallographic orientations (the substrate orientations chosen were (001), (011) and (111)). The gate insulator considered was SiO_2 with two different thicknesses: t_{ox}=1.5nm and t_{ox}=3nm, the substrate was left undoped and a midgap metal was chosen for both gates.

4. Inversion charge model

The expression used to model the inversion charge centroid (z_I) was the following,

$$\frac{1}{z_I} = \frac{1}{a + bt_{si} + ct_{si}^2} + \frac{1}{z_{I0}}\left(\frac{N_I}{N_{I0}}\right)^n \qquad (1)$$

where a, b, c, $z_{I0}(t_{si})$, and $n(t_{si})$ are fitting parameters. These parameters show different values for the substrate orientations considered. z_I was calculated considering the origin at the insulator-semiconductor interface. N_I stands for the carrier density (N_I=Q'/q, see Equation 2 for the expression to calculate Q'), q is the electron charge and $N_{I0}=7\times10^{12}$ cm^{-2}, the latter parameter is neither dependant on t_{si} nor on the substrate orientation.
The inversion charge centroid of devices grown in (001) substrates is given in Figure 1. As can be seen, the model (Equation 1) accurately fits simulated data.

The inversion charge model was developed using as starting point a previous classical model [5]. A first estimation of the inversion charge, Q'(V) (V corresponds to the electron quasifermi potential), was obtained as follows,

$$Q'(V) = 2C_{ox}\left(\left(-\frac{2C_{ox}\beta^2}{Q_o}\right)+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_o}\right)^2+4\beta^2\ln^2\left[1+\exp\left[\frac{V_{gs}-V_o-V}{2\beta}\right]\right]}\right) \quad (2)$$

$\beta=kT/q$, $Q_0=4\beta C_{si}$ ($C_{si}=\varepsilon_{si}/t_{si}$) and V_0 is given below,

$$V_0 = \Delta\varphi - \beta\ln\frac{qn_i t_{si}}{2Q_o} \quad (3)$$

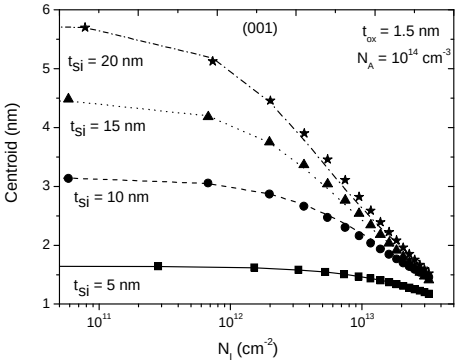

Figure 1: *Inversion charge centroid versus inversion charge for n-type DGMOSFETs grown on a (001) substrate. Simulation results are plotted in lines and modeled data in symbols. (squares - t_{si}=5 nm, circles - t_{si}=10 nm, triangles - t_{si}=15 nm and stars - t_{si}=20 nm).*

QMEs have been taken into account by means of an enhanced oxide capacitance where the inversion charge centroid and its derivative are included to correct the oxide thickness [6].

$$C_{ox}^{*} = \frac{\varepsilon_{ox}}{t_{ox}+\frac{\varepsilon_{ox}}{\varepsilon_{si}}z_I+\frac{\varepsilon_{ox}Q'}{\varepsilon_{si}}\frac{dz_I}{dQ'}} \quad (4)$$

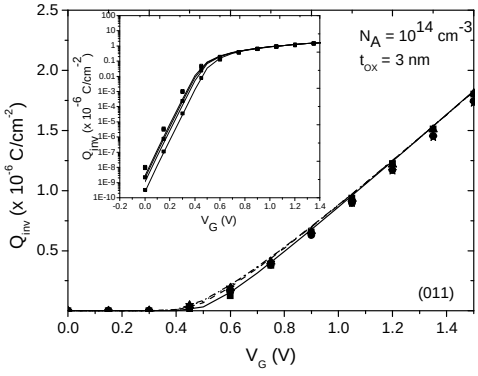

Figure 2: *Inversion charge versus gate voltage for n-type DGMOSFETs fabricated in (011) substrates. Simulations are plotted in lines, model in symbols (squares – t_{Si}=5 nm, circles – t_{Si}=10 nm, triangles – t_{Si}=15 nm and stars – t_{Si}=20 nm).*

Finally, the inversion charge is obtained as follows,

$$Q(V) = 2C_{ox}^{*}\left(\left(-\frac{2C_{ox}^{*}\beta^2}{Q_o}\right)+\sqrt{\left(\frac{2C_{ox}^{*}\beta^2}{Q_o}\right)^2+4\beta^2\ln^2\left[1+\exp\left[\frac{V_{gs}-V_{th}+\Delta V_{th}-V}{2\beta}\right]\right]}\right) \quad (5)$$

The inversion charge obtained for two n-type DGMOSFETs (for (011) and (001) substrates) is shown in Figures 2 and 3. Results for p-type devices are shown in Figure 4. A good fit is observed in all cases.

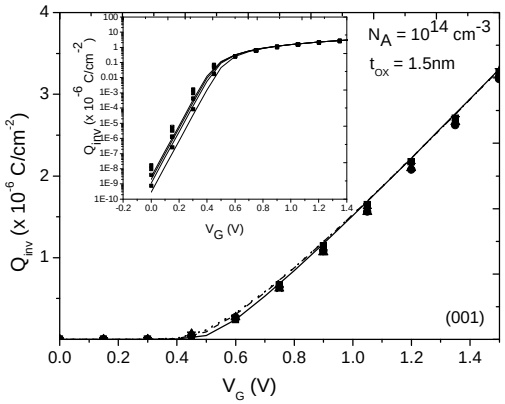

Figure 3: *Inversion charge versus gate voltage for n-type DGMOSFETs fabricated in (001) substrates. Simulations are plotted in lines, model in symbols (squares – t_{Si}=5 nm, circles – t_{Si}=10 nm, triangles – t_{Si}=15 nm and stars – t_{Si}=20 nm).*

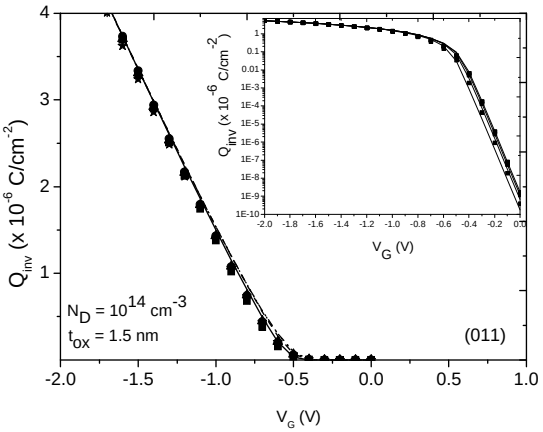

Figure 4: *Inversion charge versus gate voltage for p-type DGMOSFETs fabricated in (011) substrates. Simulations are plotted in lines, model in symbols (squares – t_{Si}=5 nm, circles – t_{Si}=10 nm, triangles – t_{Si}=15 nm and stars – t_{Si}=20 nm).*

5. Acknowledgements

This work was carried out within the framework of Research Project P08-TIC-3580 (Junta de Andalucía) and TEC2008-06758-C02-01 (Spanish Government). Financial support from EUROSOI+ (FP7-CA-216373) and EU-NANOSIL (FP7-NOE-216171) is also acknowledged.

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An analytical electric potential model for square Gate-All-Around MOSFETs

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1. Abstract

A new approach to solve analytically the two-dimensional Poisson equation including the inversion charge density in undoped square Gate-All-Around MOSFETs has been developed. With this procedure, we can obtain functions of different complexity degrees to model the electric potential in the devices under study. The results obtained are compared with data simulated by solving Poisson's equation numerically, showing an excellent agreement.

2. Introduction

Multiple-gate (MuG) MOSFETs are considered key devices in the current scaling landscape described by Moore's law (which considers for the near future channel lengths of 22nm and below). In particular, Gate-All-Around (GAA) MOSFETs present promising unique features to be considered for future low power and RF analog applications [1]. Square GAA MOSFETs have not been analytically described in depth so far, in comparison to their cylindrical counterpart, due to their complex geometry; new strategies are necessary to deal with their modeling. In this work, we will introduce a technique to build analytical functions to model the electric potential in square cross-sections of GAA MOSFETs. The proposed functions are solutions of the 2D Poisson equation, where the charge density in the silicon channel includes the inversion charge, which make feasible the modeling of the potential for the most important operation regions (from subthreshold to strong inversion).

The simulation data presented in this work have been obtained with a simulator developed within our research group [2]. The geometry and cross-section of the GAA MOSFETs studied is shown in figure 1. It can be seen that the gate completely surrounds the square silicon channel (left undoped) where conduction takes place. The t_{Si} values considered were 10 and 20 nm, and the parameter t_{Ox} (the thickness of the insulator layer, SiO_2) was 1.5 nm. A midgap metal gate was used.

3. Electric potential model

The electric potential, Ψ(x,y), in the silicon channel of the device (shown in Figure 1) has been obtained by solving the 2D Poisson's equation (Equation 1) making use of the coordinate system sketched in the same figure. We have only accounted for electron charge in our calculations:

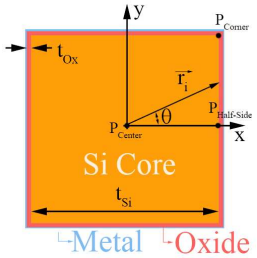

Fig.1: *Square GAA MOSFET device geometry.*

$$\frac{\partial^2\Psi(x,y)}{\partial x^2}+\frac{\partial^2\Psi(x,y)}{\partial y^2}=\frac{q}{\varepsilon_{Si}}n_i\exp\left(\frac{q\Psi(x,y)}{K\,T}\right) \qquad (1),$$

This equation has been solved analytically following an approach similar to [3], resulting into the following general solution:

$$\Psi(x,y)=\frac{1}{\beta}\ln\left(\frac{8\phi'(z)\phi'^{*}(z)}{\alpha\beta\left(1-\phi(z)\phi^{*}(z)\right)^2}\right) \qquad (2),$$

with $\alpha=n_i q/\varepsilon_{Si}$, $\beta=q/KT$, $z=x+iy$ and $\phi(z)$ an arbitrary complex holomorphic function ($\phi^{*}(z)$ the complex conjugate function). In order to determine completely the expression of the electric potential we considered the boundary conditions at the silicon-insulator interface and a heuristic procedure. Several holomorphic functions can be used in Equation 2 to generate different analytical expressions for the electric potential. Here, two of these functions were considered: $\phi_1(z)=mz$, and $\phi_2(z)=mz+nf(z)$, with $f(z)=(z-ia)^{-1}+(z+ia)^{-1}-(z+a)^{-1}-(z-a)^{-1}$.

Figure 2 shows the electron density achieved solving numerically Poisson equation in a GAA MOSFET with t_{Si}=20nm. In the subthreshold regime (Fig. 2a), the electron density, and therefore the potential, is almost flat; however, for gate voltages above threshold (Fig. 2b), a strong increase of the electron density is found near the Si-SiO_2 interfaces. The corners are more inverted since the potential well there is deeper. It can be deduced that for an inversion charge model to work properly in strong inversion it is essential to model

reasonably well the electric potential in the semiconductor perimeter. The electric potential $\Psi_1(x,y)$ found using $\phi_1(z)$ coincides with the expression proposed for cylindrical GAA MOSFETs in [4], and therefore, it is not expected to work well in the strong inversion regime for square devices. On the other hand, using $\phi_2(z)$, a potential function $\Psi_2(x,y)$ with additional parameters (m, n, a) is found, allowing a better fit of the simulated potential distribution in the device, at the cost of a higher complexity in the analytical expressions obtained (not shown here).

Figure 3 compares the simulated potential for a square GAA MOSFET with those found using $\Psi_1(x,y)$ and $\Psi_2(x,y)$. As can be seen, in the subthreshold regime both models are quite accurate regardless of the size of the device; however, for higher gate voltages, only $\Psi_2(x,y)$ provides accurate results. In the latter case, the results are accurate even in the areas close to the corners of the device, as can be seen in Figure 4.

3. Acknowledgments

This work was carried out within Research Project P08-TIC3580 (Junta de Andalucía), TEC2008-06758-C02-01 and FIS2008-05805 (Spanish Government). EU EUROSOI+ (FP7-CA-216373) and EU NANOSIL (FP7-NOE-216171) are also acknowledged.

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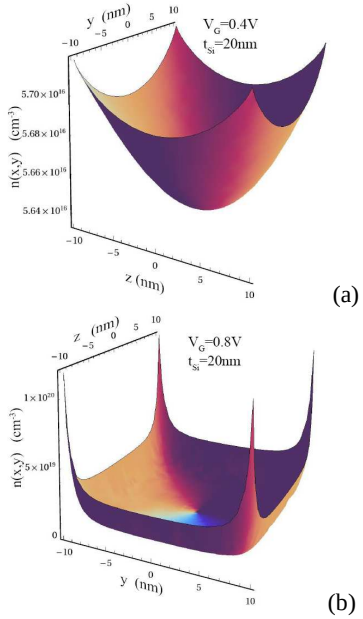

Fig.2: *Three-dimensional view of the simulated inversion charge density for a square GAA MOSFET with t_{Si}=20nm.*

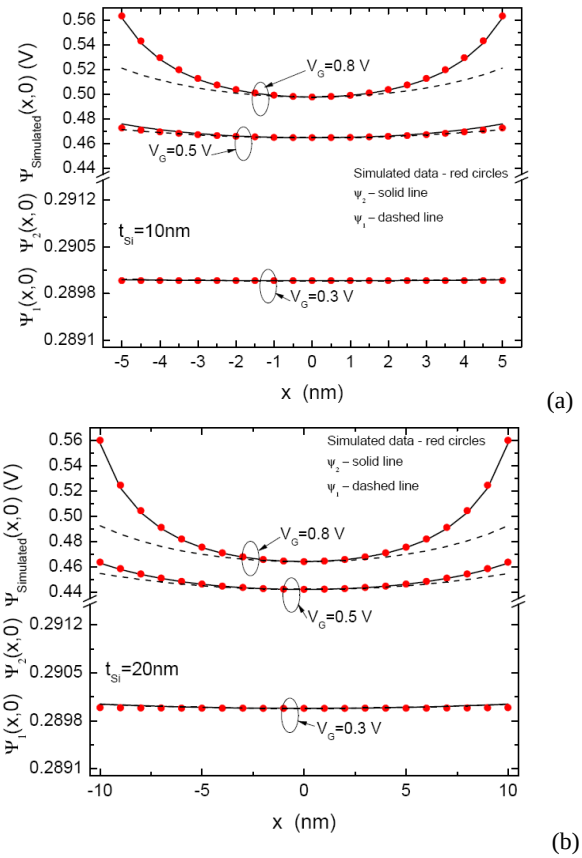

Fig.3: *Comparison of the electric potential functions $\Psi_1(x,y)$ (dashed-line) and $\Psi_2(x,y)$ (solid-line) with the simulated data (symbols) along the x coordinate of a square GAA MOSFET at y=0. (a) t_{Si}=10nm, and (b) t_{Si}=20nm.*

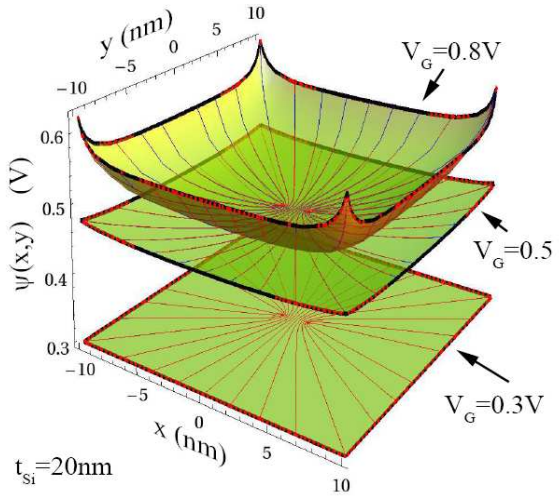

Fig.4: *Three dimensional view of the electric potential for a square GAA MOSFET with t_{Si}=20nm. The modeled (simulated) data are represented by the surface with dashed (continuous) borders.*

OCTO SOI MOSFET: An Evolution of the Diamond to Be Used in the Analog Integrated Circuits

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1. Abstract

This paper introduces a new transistor structure, entitled OCTO SOI MOSFET. This innovative layout style is an evolution of the Diamond structure that is able to further reduce the die area of the analog integrated circuits. OCTO was specially designed by changing the Diamond gate geometry from hexagonal to octagonal. This innovative gate geometry is able to further reduce the gate area and keep the Longitudinal (parallel) Corner Effect, that exist in the Diamond structure, increasing the longitudinal electric field along the channel and consequently the average drift velocity of the mobile carriers in the channel, the drain current, the transconductance and on-state series resistance as well.

2. Introduction

Regarding the classical planar single-gate SOI MOSFETs (CSM) [1], some devices have been proposed, focusing on "channel engineering", such as circular-gate [2] and graded-channel (GC) [3] to enhance their electrical performance. Recently, a new approach has been proposed to improve the performance CSM, called "drain/channel/source interfaces engineering" [4-5], resulting in a new transistor structure, named Diamond SOI MOSFET (DSM) (hexagonal gate geometry, HGG) [4-5], that uses the Longitudinal Corner Effect (LCE) [4-5] to enhance the resultant longitudinal (parallel) electric field ($\vec{\varepsilon}_{//}$) and consequently improve the average drift velocity ($<\vec{v}_x>$), drain current (I_{DS}) and transconductance (g_m). It was observed that by three-dimension numerical simulations (3DNS), the Partially Depleted (PD) DSM produces expressive improvements in terms of I_{DS} and g_m comparatively to the CSM counterpart, keeping the same gate area (A_G), geometric factor (W/L) and bias conditions. As the DSM drain current density (J_{DS}) is more intense in the edges of the HGG and aiming at further reduction of its effective channel length (L_{eff}) and its A_G to improve in the integration factor [f_I=(W/L_{eff})/A_G], and keeping the LCE along the channel, OCTO SOI MOSFET (OSM) was specially designed. This new structure was created when we cut the extreme corners of the DSM gate hexagonal geometry (Fig. 1), improving the electrostatic discharge (ESD) robustness and the breakdown voltage (BV_{DS}) [1] and generating an octagonal gate geometry (OGG) that enables mainly a die area reduction of the transistor and consequently of the analog ICs.

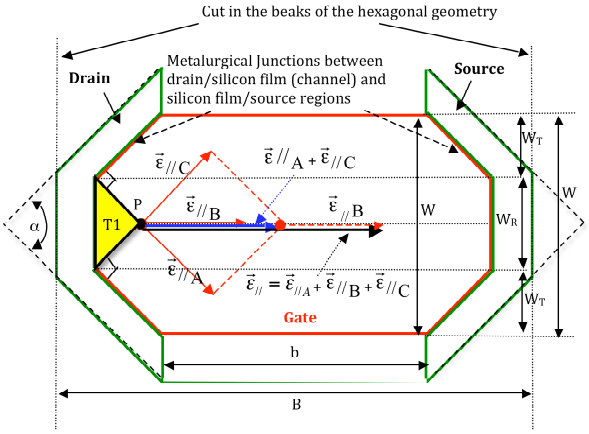

Fig. 1. *Example of the OCTO SOI MOSFET layout.*

In Fig. 1, b and B are the smallest and largest distances between the drain and source regions, respectively, W_T {=[(B-b)/2]tan(α/2)} and W_R (=W-2W_T) are the channel widths of the trapezoidal and rectangular parts of the octagonal gate geometry, respectively, W the is channel width (=W_R+2W_T) respectively, and α is the angle of the hexagonal geometry which led to the design of OCTO layout, $\vec{\varepsilon}_{//A}$, $\vec{\varepsilon}_{//B}$ and $\vec{\varepsilon}_{//C}$ are the longitudinal electric field components that are generated by the drain bias applied in each side of the metallurgical junctions of the drain/silicon film regions, and $\vec{\varepsilon}_{//}$ at the point P is equal to $\vec{\varepsilon}_{//A}$+ $\vec{\varepsilon}_{//B}$+$\vec{\varepsilon}_{//C}$ that is higher than that one found in the CSM counterpart, considering the same bias conditions. Observe that, in the T1 region of the OSM (Fig. 1), the vector sum of the $\vec{\varepsilon}_{//A}$, $\vec{\varepsilon}_{//B}$ and $\vec{\varepsilon}_{//C}$ does not occur, as happens in all DSM gate region, otherwise we found only the $\vec{\varepsilon}_{//B}$ that is similar to the one observed in the CSM counterpart. So, we can conclude that the resultant DSM $\vec{\varepsilon}_{//}$ is higher than the one found in the OSM, which in turn is higher than the one observed in CSM counterpart and consequently DSM I_{DS} is higher than the OCTO I_{DS}, which in turn is higher than the

CSM I_{DS}. The OSM equivalent circuit can be electrically represented by three transistors connected in parallel: two of them with trapezoidal gate geometry with effective channel length [$L_{eff\_T} \cong (B+b)/2$] (Fig. 1), and another one with rectangular gate geometry ($L_{eff\_R}=B$), respectively. So, in first approximation, the OCTO L_{eff} can be calculated by the arithmetic mean of the L_{effs} transistors and is given by (b+2B)/3.

The objective of this paper is to perform a comparative study between the three layout styles: one CSM (the base of the comparison), the DSM ($\alpha=90^o$) counterpart and the OSM ($\alpha=90^o$) which was designed by cutting in 50% the extreme corners of the DSM ($\alpha=90^o$) HGG in order to verify the benefits and disadvantages of the OSM in comparison to the DSM and CSM structures.

3. Simulation Results

Table I presents the dimensions of the PD CSM, DSM and OSM with $\alpha=90^o$ studied by the 3DNS (Sentaurus).

Table I. *Dimensions of the CSM, DSM and OSM with $\alpha=90^o$.*

#	W (µm)	L_{eff} (µm)	W/L	B (µm)	b (µm)	A_G (µm²)	A_G Gain
CSM	5.95	4.02	1.48	-	-	23.9	-
DSM	5.95	4.02	1.48	7.00	1.05	23.9	-
OSM	5.95	3.12	1.91	4.02	1.05	19.5	+18.5%

The technological parameters of these devices are: gate-oxide (t_{ox}), silicon filme (t_{SI}) and buried-oxide (T_{BOX}) thickness are 2.5 nm, 100 nm and 400 nm, respectively, and drain/source and channel doping concentrations are $1x10^{20}$ cm^{-3} and $5.5x10^{17}$ cm^{-3}, respectively. Philips unified mobility, enormal, high field saturation and Shockley-Read-Hall models were used in the Sentaurus 3DNS. Figure 2 presents the curves of $I_{DS}/(W/L_{eff})$ vs V_{GS} and V_{DS}, respectively and Table II compares the values of the g_{m_max}, $I_{DS}/(W/L_{eff})$, V_{EA} and R_{DSON} of the DSM and CSM.

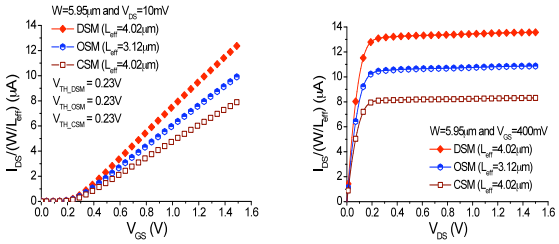

Fig. 2. *$I_{DS}/(W/L_{eff})$ as a function of V_{GS} and V_{DS}, respectively.*

Table II. *Dimensions of the CSM, DSM counterpart and OSM with $\alpha=90^o$.*

#	$I_{DS\_sat}/(W/L_{eff})$ (µA)	$g_{m\_max}/(W/L_{eff})$ (µS)	V_{EA} (V)	R_{ON} (kΩ)
CSM	8.17	6.59	55.5	13.3
DSM	13.3(+63%)	10.3 (+56%)	51.2 (-7.7%)	8.38 (+37%)
OSM	10.6 (+30%)	8.27 (+26%)	45.1 (-19%)	10.5 (+21%)

When we compare $I_{DS}/(W/L_{eff})$ of two different devices, the influence of the geometric factor is eliminated. So, Figure 2 shows an important result, where the DSM $I_{DS}/(W/L_{eff})$, $g_{m\_max}/(W/L_{eff})$ and R_{ON} are better than those observed in the OSM, due to the higher DSM $\vec{\varepsilon}_{//}$ comparatively to the one of the OSM, considering the same W and bias conditions, as explained before. Furthermore, notice also that OSM $I_{DS}/(W/L_{eff})$, $g_{m\_max}/(W/L_{eff})$ and R_{ON} are higher than one found in the CSM due to the higher OSM $\vec{\varepsilon}_{//}$ when we compare to the one found in the CSM, with a significant A_G reduction (18.5%). Thus, OSM is another option to be used to further reduce the die area (A) of the analog ICs, improving the ESD robustness and BV_{DS}.

3. Experimental Results

Knowing that OCTO layout style can be applied for any CMOS technology, we are also presenting some additional experimental results obtained by using devices manufactured with conventional CMOS technology (AMI, On-Semiconductor, MOSIS). Table III shows the dimensions of five transistors: one Diamond (DM) with $\alpha=37^o$, one conventional (CM) counterpart, and three OCTOs with $\alpha=37^o$.

Table III. *Dimensions of the CM, DM and OM with $\alpha=37^o$.*

#	W (µm)	L_{eff} (µm)	W/L	B (µm)	b (µm)	A_G (µm²)	A_G Gain
CM	5.95	9.98	0.596	-	-	59.4	-
DM	5.95	9.98	0.596	18.9	1.05	59.4	-
OM1	5.95	8.73	0.681	14.4	1.05	55.9	+5.89%
OM2	5.95	7.10	0.838	9.98	1.05	46.1	+22.4%
OM3	5.95	4.76	1.25	5.60	1.05	29.9	+49.7%

Figure 3 presents one example of the experimental results of $I_{DS}/(W/L_{eff})$ vs V_{GT} ($=V_{GS}-V_{TH}$) for $V_{DS}=0.2V$ and $I_{DS}/(W/L_{eff})$ vs V_{DS} for $V_{GT}=0.5V$ for all structures analyzed.

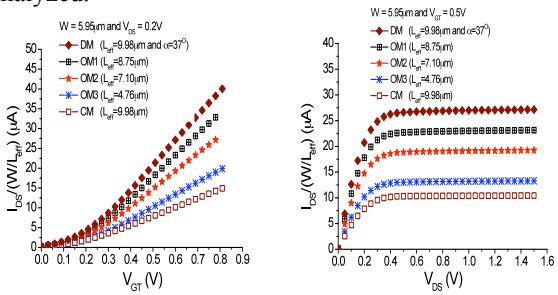

Fig. 3. *$I_{DS}/(W/L_{eff})$ vs V_{GT} for $V_{DS}=0.2V$ and $I_{DS}/(W/L_{eff})$ vs V_{DS} for $V_{GT}=0.5V$ of the CM, DM and OM with $\alpha=37^o$.*

The experimental results present the same tendencies than those observed in the 3DNS. Besides that, for a specific α, the OSM behaviour tends to be similar to the one found in the CSM counterpart, when its L_{eff} is reduced, due to small interaction between the $\vec{\varepsilon}_{//}$ components (enlargement of the OSM T1 region).

5. Conclusions

By 3DSN and experimental results, we can verify the benefits of the OSM in terms of the I_{DS_sat}, g_m and R_{ON}, and therefore we consider OSM another alternative for the analog ICs to reduce the die area and increase the robustness of the ESD and BV_{DS}.

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A Compact Double-Gate MOSFET Model Consistent with a Multi-Subband Ensemble Monte Carlo Model

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1. Abstract

In this paper we extend a Double Gate (DG) MOSFET model to nanometer technology nodes in order to include the hydrodynamic and quantum mechanical effects, and we show that the final model can accurately reproduce Multi-Subband Ensemble Monte Carlo Simulations. Template devices representative of 22nm and 16nm DG MOSFETs were used to validate the model. The final model includes the main short-channel and nanoscale effects, such as mobility degradation, channel length modulation, drain-induced barrier lowering, overshoot velocity effects and quantum mechanical effects.

2. Introduction

Ultra-thin-film body MOS transistors and, in particular, double-gate (DG) MOSFETs are considered to be a very attractive option to improve the performance of CMOS devices. Nanoscale DG-MOSFETs introduce challenges to compact modeling associated with the enhanced coupling between the channels, ballistic or quasi-ballistic transport, quantum confinement, etc. In this work we present the extension of a DG MOSFET model to nanoscale technology nodes by incorporating quantum mechanical and hydrodynamic transport effects validating it by comparison with Monte Carlo (MC) simulations. Our starting point in this paper is a classical analytical model for the undoped DG-MOSFET [1] based on a unified charge control model [2]. The final compact model for the drain-current includes mobility degradation, short-channel effects (SCE), or channel length modulation (CLM). Velocity overshoot is also modeled through the hydrodynamic transport and quantum effects are extended from the classical compact model [3]. The results of the comparison between the compact model and MC simulations are presented and discussed in this work.

3. Simulation Approaches

The advanced modeling approach used for th calibration of the compact model is based on the direct solution of the Boltzmann-Transport-Equation (BTE) using the Monte Carlo method. In particular, the Multi-Subband Ensemble Monte Carlo (MSB-EMC) simulator has been used [4]. This method is based on the mode-space approach of quantum transport. The Monte Carlo family model incorporates all relevant scattering mechanisms such as surface roughness (SR), acoustic and phonon scattering. We have accurately modeled these MC simulations using our compact model (with physical parameter values), taking into account the physical mechanisms included in their approach. The drain current expression is based on a unified charge control model which is written in terms of charge densities at the source and drain ends. This drain current expression includes the hydrodynamic transport model. Velocity overshoot is included in the model using a one dimensional energy-balance model [5]. We have included a correction in the oxide capacitance using the inversion-layer centroid [6] to take into account the quantum mechanical effects. The low-field mobility data are obtained from a model that takes into account the mobility degradation [7] due to quantum effects. We have also included the effects of channel length modulation (CLM) and drain-induced barrier lowering (DIBL). The quantum confinement correction is included in the model that makes a positive shift in the threshold voltage of the device (n-channel) [8].

4. Results and Discussions

Fig. 1 and 2 shows the transfer characteristics for 22 nm and 16 nm DG-MOSFETs, respectively. A good agreement between the compact model and the MSB-EMC simulations is obtained. In particular, the mobility degradation is well reproduced. Fig. 3 shows the output characteristics of the 22 nm (top) and 16 nm (bottom) DG MOSFETs. A good agreement between the compact model and the MSB-EMC simulations are seen. It can be seen that the model without the effect of velocity overshoot and quantum effects, a good agreement is obtained at low drain bias and becomes lower at higher drain bias. If the quantum effects are not included in the model, the current is significantly higher than the MC simulations. If the hydrodynamic transport is not considered the model gives much lower current values than the simulation. It can be inferred that the hydrodynamic model can be used to compare results from advanced transport models such as MSB-EMC simulations.

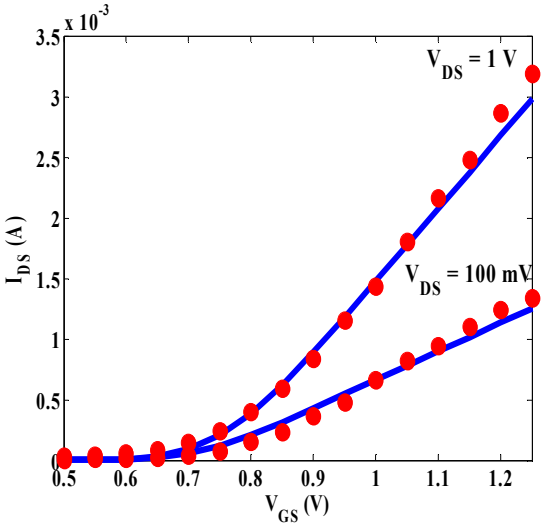

Fig.1: *Trans-characteristics of 22 nm DG-MOSFET for low and high V_{DS} Solid lines: Compact model, Symbols: Simulations (UGR MSB-EMC).*

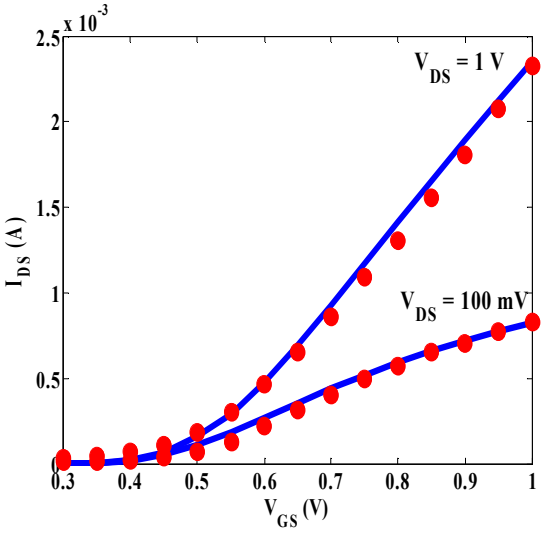

Fig.2: *Trans-characteristics of 16 nm DG-MOSFET for low and high V_{DS} Solid lines: Compact model, Symbols: Simulations (UGR MSB-EMC)*

5. Conclusions

The comparison between the advanced modeling approach and the compact model for the drain current in nanoscale DG MOSFETs are presented. We present a compact DG MOSFET model to reproduce results obtained from the Multi-Subband Ensemble Monte Carlo simulator for the 22 nm and 16 nm technology nodes. The model is valid and continuous through all operating regimes. Nanoscale and short-channel effects are taken into account, including velocity overshoot and quantum mechanical effects. The model shows a very good agreement with the MC simulations for the practical range of voltages considered.

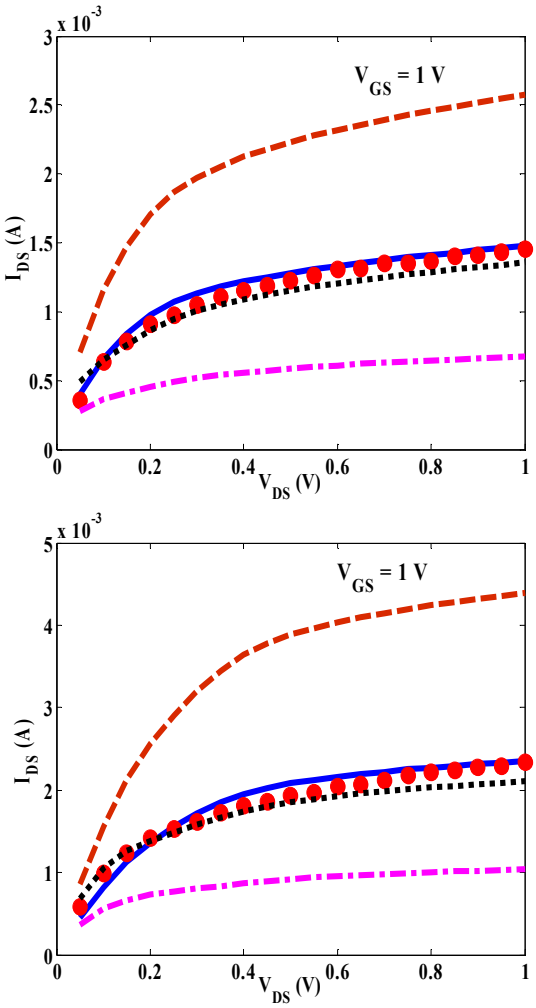

Fig.3: *Output characteristics of the 22 nm (top) and 16 nm (bottom) DG-MOSFET for V_{GS}=1V Dashed line: Without quantum effects, Solid line: Compact model, Dotted line: Without velocity overshoot and quantum effects, Dash-dotted line: Without hydrodynamic transport, Symbol: Simulation (UGR-MSB-EMC).*

Acknowledgements

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1/f Noise in Strained SGOI MOSFETs

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1. Abstract

Low-frequency noise in $Si_{0.85}Ge_{0.15}$ and $Si_{0.70}Ge_{0.30}$ p- and n-channel strained Silicon Germanium on Insulator (SGOI) MOSFETs with 15nm thick substrates obtained using the enrichment technique is studied. The gate oxide is composed of a $TiN/HfO_2/SiO_2$ stack. The different noise mechanisms in these devices are described. The extracted front interface average trap density is $N_t(E_{Fn})$ = 1-3 10^{18} cm^{-3} eV^{-1} and is irrespective of the Ge content. We obtain that the extracted back interface trap densities are comparable to those of GeOI substrates obtained using SmartCut™ technology (N_T=3-6 10^{17} $cm^{-3}eV^{-1}$) and is of the same order as Si/SiO_2 interfaces.

2. Introduction

Strained SiGe channel MOSFETs have attracted much attention due to the enhancement of the hole mobility. Fully Depleted Silicon On Insulator (FDSOI) technology presents several advantages over standard bulk CMOS [1]. The devices investigated in this contribution exhibit the combined previous advantages.
In this work, a comparative study between n and p channel devices as a function of different Si-Ge content ratios is carried out, where low-frequency noise characterization is performed on the front and rear interfaces of the SiGe substrate.

3. Experimental details

The studied devices are $Si_{0.85}Ge_{0.15}$ and $Si_{0.70}Ge_{0.30}$ p- and n-channel Strained Germanium-On-Insulator (SGOI) MOSFETs with 15nm thick substrates and with $TiN/HfO_2/SiO_2$ gate stacks (fig. 1). These substrates were obtained using the enrichment technique. Details on the MOS process are reported in [2].
The devices under test had dimensions WL=10µmx1µm in order to reduce the impact of singular events.
In order to measure the electrical characteristics at the Si/buried oxide (BOx) interface, the back of the substrate is polarised (V_{BG}) so as to use the BOx as a back gate. A bias is applied at the front gate (V_{FG}) to suppress the front interface channel conduction. Noise measurements were carried out at V_{DS}=50mV, and from weak to strong inversion. The low field mobility values (μ_0) are extracted using the Y function and are reported in Table 1.

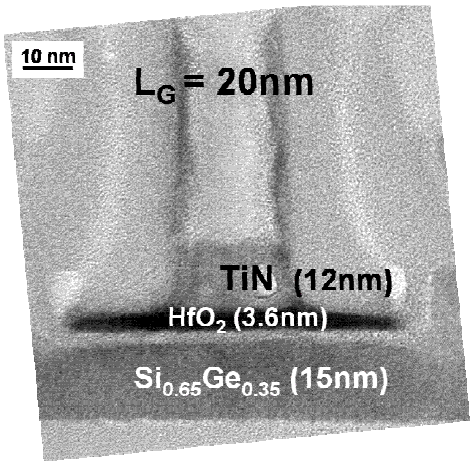

Fig.1: *Transverse X-TEM view of a 20nm gate length strained SGOI MOSFET(x_{Ge}=35%)*

	Front interface	Rear interface
nMOS x=15%	130	130
nMOS x=30%	100	105
pMOS x=15%	110	145
pMOS x=30%	130	235

Table 1: *Extracted low field mobility values, expressed in* $cm^2V^{-1}s^{-1}$

4. Results and discussion

Noise measurements have shown pure 1/f noise, which indicates that the distribution of the traps is uniform. Fig. 2 to 5 show typical drain current power spectral density extrapolated at 1 Hz versus drain current.
For p-MOSFETs, for front and rear conduction, the drain current 1/f noise can be modeled by the carrier number fluctuation (ΔN) from weak to strong inversion [3], allowing the extraction of trap density at both interfaces. For the front interface the average trap density extracted is $N_t(E_{Fn})$ = 1.2 10^{18} cm^{-3} eV^{-1}, and is irrespective of the Ge content. This value is the same as for Germanium on Insulator (GeOI) devices with an equivalent gate stack [4]. For the rear interface the trap densities extracted are very similar for all devices and are comparable to those of GeOI substrates obtained

using SmartCut^{TM} technology (N_T=~3 10^{17} $cm^{-3}eV^{-1}$) and is of the same order of magnitude as Si/SiO_2 interfaces. This demonstrates that the enrichment technique produces equally good quality interfaces.

For nMOSFETs, the measured noise deviates from the ΔN model in strong inversion. This behavior has equally been observed in GeOI devices and holds true for front and rear interfaces. However, this behavior can be modeled as a first approximation using the correlated carrier number-mobility model (ΔN-Δμ) indicating that the insulator charge fluctuation induces fluctuation of the effective mobility in the inversion layer [5]. The average trap density N_T and the Coulomb scattering coefficient α for front and rear interfaces are extracted. The obtained N_T values in weak inversion are the same for $Si_{0.85}Ge_{0.15}$ and $Si_{0.70}Ge_{0.30}$ devices. For the front interface, $N_t(E_{Fn})$ = 3.5 10^{18} cm^{-3} eV^{-1} , and for the rear interface $N_t(E_{Fn})$ = 6 10^{17} cm^{-3} eV^{-1}. These values are slightly above those extracted for pMOSFET devices. For the rear interface, the ΔN-Δμ model is suitable for $Si_{0.85}Ge_{0.15}$ as well as $Si_{0.70}Ge_{0.30}$ devices, with α between 2 and 5 10^4. For the front interface, in the case of $Si_{0.70}Ge_{0.30}$ the ΔN-Δμ model is also suitable with α between 2 and 3 10^4. $Si_{0.85}Ge_{0.15}$ devices exhibit an increase in noise by a factor of 10 in strong inversion compared to $Si_{0.70}Ge_{0.30}$ and cannot be satisfactorily described even using the ΔN-Δμ model.

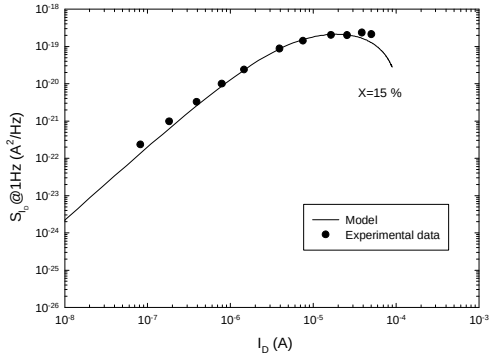

Fig.2: *Power spectral density measured at 1 Hz and the ΔN model for front interface of P-MOSFETs*

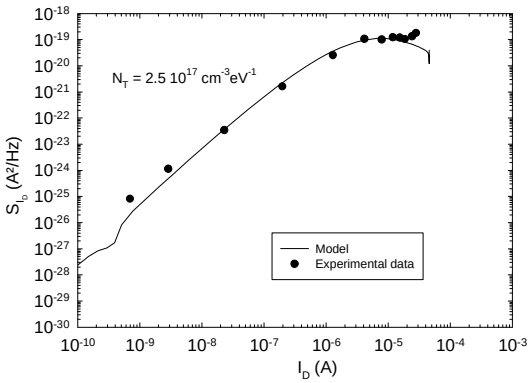

Fig.3: *Power spectral density measured at 1 Hz and the ΔN model for rear interface of P-MOSFETs.*

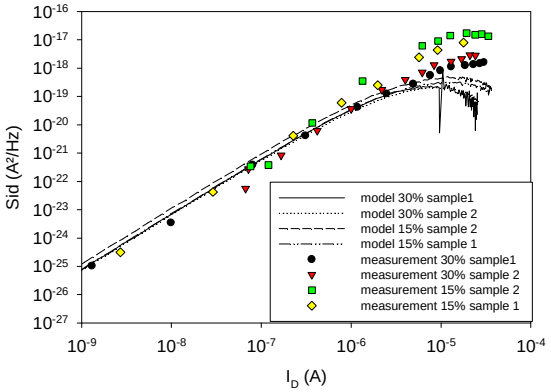

Fig.4: *Comparison between the power spectral density measured at 1 Hz and the ΔN model for front interface of N-MOSFETs..*

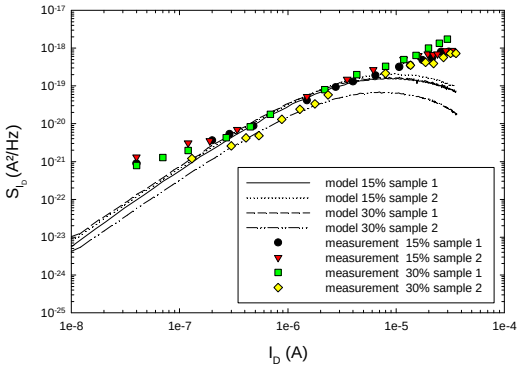

Fig.5: *Comparison between the power spectral density measured at 1 Hz and the ΔN model for rear interface of N-MOSFETs.*

5. Conclusion

Low frequency noise measurements are used to characterize the rear and front interfaces in $Si_{0.85}Ge_{0.15}$ and $Si_{0.70}Ge_{0.30}$ p- and n-channel strained Silicon Germanium on Insulator (SGOI) MOSFETs.

The extracted front interface trap densities are $N_t(E_{Fn})$ = 1-3 10^{18} cm^{-3} eV^{-1} and are irrespective of the Ge content. Moreover, the obtained back interface trap densities are comparable to those of GeOI substrates obtained using SmartCut^{TM} technology (N_T=3-6 10^{17} $cm^{-3}eV^{-1}$) and is of the same order of magnitude as Si/SiO_2 interfaces.

Acknowledgements:
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Influence of the orientation and geometry on the Phonon-limited Mobility of Square Silicon Gate-All-Around MOSFETs

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1. Abstract

In this work, we carry out a study of the phonon-limited electron mobility of Silicon Gate-All-Around SOI MOSFETs with square cross-section and varying size. The orientation dependence of the mobility is also taken into account. The study is based in the self-consistent numerical solution of the 2D Schrödinger and Poisson equations, and the subsequent use of the Kubo-Greenwood formula to estimate the electron mobility.

2. Results

Gate-All-Around (GAA) SOI MOSFETs are one of the most promising candidates to overcome the limitations imposed by the channel length reduction according to the ITRS [1]. Due to the 2D confinement, the mobility behavior of this kind of devices can significantly vary with respect to the single-gate (SG) SOI or double-gate (DG) SOI counterparts: the presence of an additional confinement direction, perpendicular to the wafer and the transport directions, modifies the population of each pair of valleys of the Silicon conduction band and thus the effective conduction mass. Besides, in square devices, the presence of corners modifies their electrostatics and can have an important effect on the device behavior.

To perform this study, we have developed a simulator that self-consistently solves the two-dimensional (2D) Schrödinger and Poisson equations in a transversal cross-section of GAA devices under the effective mass approximation (EMA), which is accurate enough for wires with sizes over the 4nm [2]. The penetration of the wave function into the oxide is allowed to get higher accuracy. When arbitrary orientation is considered, the effective mass tensor is no longer diagonal, and has to be modified to take into account the wafer orientation and the transport direction [3]. A detailed description of the simulator can be found elsewhere [4].

To calculate the mobility, for a given subband *i*, the Kubo-Greenwood formula is used [5]. The effect of the scattering mechanisms is included in this calculation through the Mathiessens rule. Both optical and acoustic phonons are taken into account. The phonon scattering has been included as described in [6].

We have studied the electron mobility for square nanowires with lateral size W_{Si} between 5nm and 15nm. Undoped substrate and midgap metal gate are considered, and SiO_2 with T_{ins}=1nm is employed as gate insulator through this work. Various confinement and transport directions have been taken into account. In Fig. 1, the phonon-limited mobility is plotted versus the inversion charge for 5nm and 15nm nanowires with various orientations. The orientation is specified by one of the confinement directions (defined by one of the faces of the device) and the transport direction. Specifically, we have simulated two devices with transport along the [001] direction (one with (100) and another with (110) as confinement planes), one with transport along [1-10] and (110) confinement and another with transport along the [111] direction and (1-21) confinement. As can be seen, regardless the device size, the mobility of (1-21)/[111] devices is the lowest. Among all the 15nm devices, the one with (100)/[001] orientation attains the highest mobility. However, for devices with W_{Si}=5nm the scenario is different, and the highest phonon-limited mobility is attained by the (110)/[001] device. Regardless the size, the (110)/[1-10] device achieves lower mobility than the devices with transport direction along the [001] axis. To get a deeper insight into this behavior, the effective conduction mass has been plotted in Fig. 2 for both 5 and 15nm devices against the inversion charge. As can be seen, the results can qualitatively explain the mobility behavior of (1-21)/[111] and (110)/[1-10] devices. However, the values achieved are similar for (110)/[001] and (100)/[001] devices for $N_{inv}<10^{12}$ cm^{-2}, with slightly higher values in the (110)/[001] one, which is consistent with the 15nm mobility curve behavior but not with the 5nm one. Thus, a reasoning only based on the effective conduction mass cannot be used to explain the mobility behavior in these devices. The phonon scattering rate mainly depends on two factors: the separation between the subband energy levels and the overlap integrals. Both factors have been plotted in Fig. 3 for the 5nm (100)/[001] (solid) and (110)/[001] (dashed) devices at V_G=0.6V. As can be seen, the overlap integrals shown in Fig. 3 for the first subbands

of the (100)/[001] devices are higher than those attained by the (110)/[001] one, while the separation between the first two energy subbands of each valley in the (100)/[001] device is lower than in the (110)/[001]. This fact increases the scattering probability, and thus reduces the mobility, explaining the curves shown in Fig. 1. In the 15nm devices case (Fig. 4), the energy separation between the different subbands is smaller and the relative occupation of the different subbands, reflected on the effective conduction mass, seems to be the most important term on the mobility calculation.

4. Conclusions

The phonon-limited mobility of square GAA nanowires with different orientations was studied. It was demonstrated that devices with transport along [001] achieve the largest mobility values. The confinement direction of such devices also plays a role, which is related to the energy levels of the confined structure and the overlap integrals that define the phonon-limited mobility.

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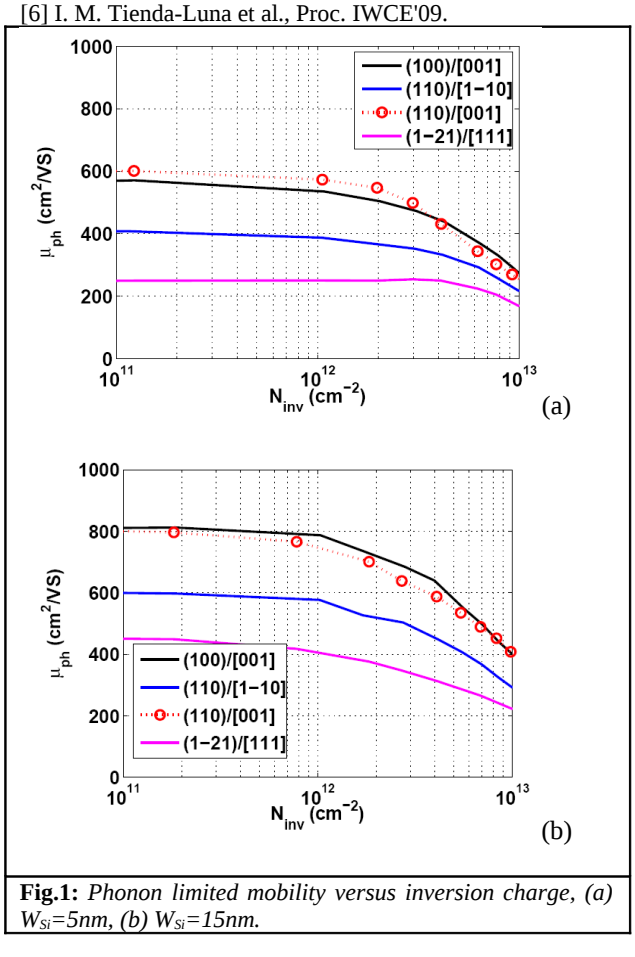

Fig.1: *Phonon limited mobility versus inversion charge, (a) W_{Si}=5nm, (b) W_{Si}=15nm.*

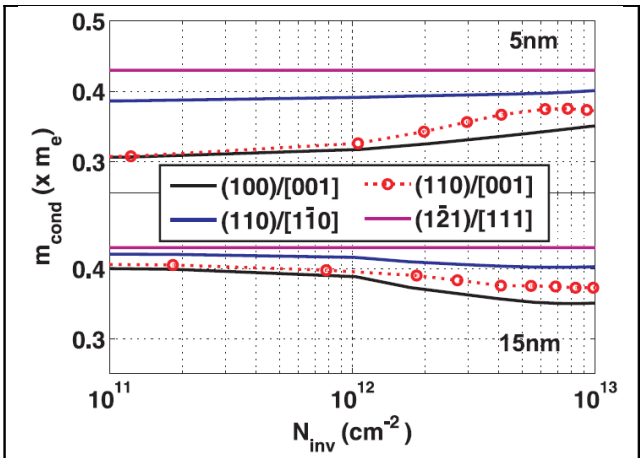

Fig.2: *Effective conduction mass versus inversion charge for W_{Si}=5nm and W_{Si}=15nm square nanowires with various orientations.*

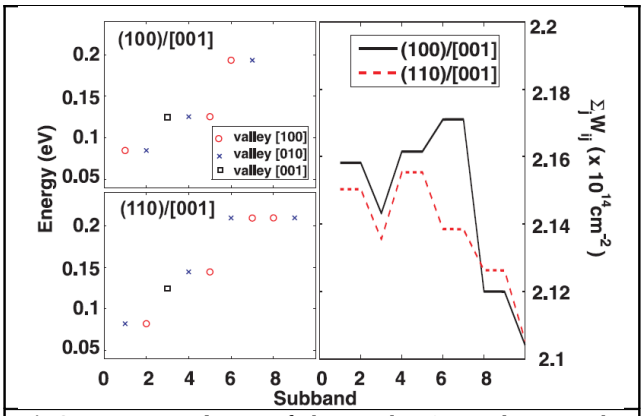

Fig.3: *Energy and sum of the overlap integral versus the subband for (100)/[001] (black solid) and (110)/[001] (red dashed) W_{Si}=5nm devices at V_G=0.6V.*

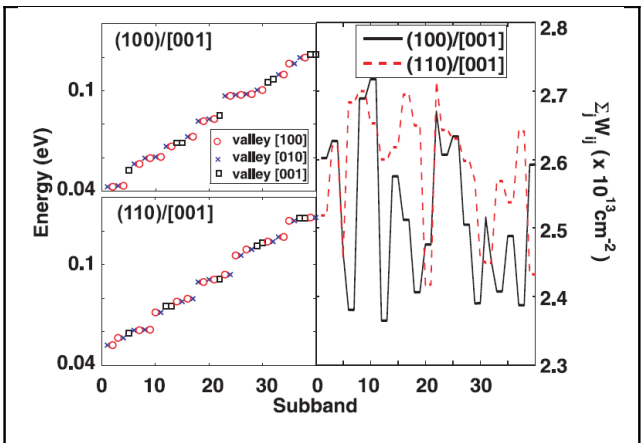

Fig.4: *Energy and sum of the overlap integral versus the subband for (100)/[001] (black solid) and (110)/[001] (red dashed) W_{Si}=15nm devices at V_G=0.6V.*

Subband Engineering in n-Type Silicon Nanowires using Strain and Confinement

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1 Abstract

We present a model based on $\mathbf{k}\cdot\mathbf{p}$ theory which is able to capture the subband structure effects present in ultra-thin strained nanowires. The effective mass and valley minima are calculated for different crystal orientations thicknesses and strains. The results show that transport enhancement can be achieved by both confinement and strain which is in agreement with recent experimental findings.

2 Motivation

Nanowire based gate-all-around transistors offer a perspective for further device size reduction in microelectronics. Apart from the enhancement of electrostatic control over the channel due to a high surface to volume ratio, nanowires exhibit transport properties which deviate significantly from what is observed in bulk silicon or inversion layers. In a recent experimental study [1] nanowires with gate-all-around structure as thin as 3 nm were successfully fabricated using a top down structuring process [2]. The produced nanowires had a [110] oriented axis and $(1\bar{1}0)$ and (001) oriented walls.

3 Modeling

To understand the transport properties in wires below 10 nm one must carefully take quantization effects into account. A simple treatment using effective masses fails to satisfactorily describe the subband structure of such thin devices. This is due to the energy of the lowest subband already being of the order of 100 meV where non-parabolicity effects become noticeable.
In this work we investigate the effects of both two dimensional confinement and strain using a two band $\mathbf{k}\cdot\mathbf{p}$ model for the conduction band [3, 4]. The model is valid for the conduction band and includes a first-order treatment of uniaxial and shear strain. The model Hamiltonian describing a pair of adjacent Δ-valleys reads as follows:

$$\mathbf{H} = \left(\frac{\hbar^2(k_{\mathrm{t1}}^2+k_{\mathrm{t2}}^2)}{2m_{\mathrm{t}}} + \frac{\hbar^2 k_{\mathrm{l}}^2}{2m_{\mathrm{l}}} + \Xi_{\mathrm{u}}\varepsilon_{\mathrm{l\text{-}l}} + V\right)\mathbf{I} + \frac{\hbar^2 k_0 k_{\mathrm{l}}}{m_{\mathrm{l}}}\boldsymbol{\sigma}_z - \left(\frac{\hbar^2 k_{\mathrm{t1}} k_{\mathrm{t2}}}{M} - 2\Xi_{\mathrm{u}'}\varepsilon_{\mathrm{t1\text{-}t2}}\right)\boldsymbol{\sigma}_x.$$

V denotes the conduction band edge; $m_{\mathrm{l}} = 0.91m_e$ are the longitudinal and $m_{\mathrm{t}} = 0.19m_e$ the transversal effective mass and $\frac{1}{M} \approx \frac{1}{m_{\mathrm{t}}} - \frac{1}{m_e}$; $k_0 = 0.15\frac{2\pi}{a}$ amounts to the distance between a X point and the nearest Δ valleys; $\varepsilon_{\mathrm{l\text{-}l}}$ and $\varepsilon_{\mathrm{t1\text{-}t2}}$ are uniaxial and shear strain components and Ξ_{u} and $\Xi_{\mathrm{u}'}$ the deformation potentials; $\boldsymbol{\sigma}_{x,z}$ denote the Pauli matrices and $\mathbf{I}$ the identity matrix. The Hamiltonian is rotated according to the nanowire axis and quantized in the cross section plane to obtain the subband structure.

4 Results and Conclusions

We predict a significant change of the effective mass with respect to its bulk value due to confinement and strain, as shown in Fig. 1 and 2. The trend of the change depends on the crystal orientation of the wire; while for a [111] wire the mass generally increases with confinement and strain, the situation is different for [110] wires. Here, the transport properties can be significantly enhanced using a combination of confinement and strain. We also show that the minima of the heavy unprimed valleys shift to higher energies with increasing strain (Fig. 6) and confinement (Fig. 3), while the opposite trend is observed for the unprimed valley (Fig. 4). This shift leads to a repopulation of the carriers towards the light unprimed valley and further improves the transport properties.
A strain induced current enhancement of up to 30% was shown in [1], which is in qualitative accordance with the results obtained from our calculations, where we found that tensile strain along the axis is beneficial in terms of effective mass for [110] oriented wires. This leads us to believe that transistors based on strained [110] nanowires with diameters below 10 nm are promising candidates for future digital integrated circuits where fast switching and low power consumption are important.

Acknowledgment

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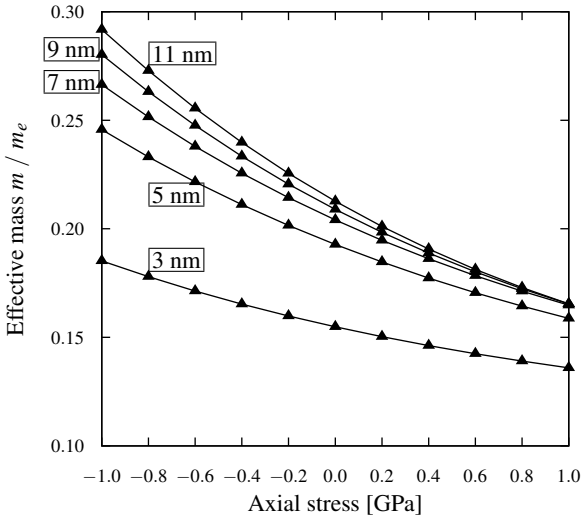

Fig. 1: Stress dependence of the effective mass in the unprimed (Γ) valley for [110] nanowires of different thicknesses

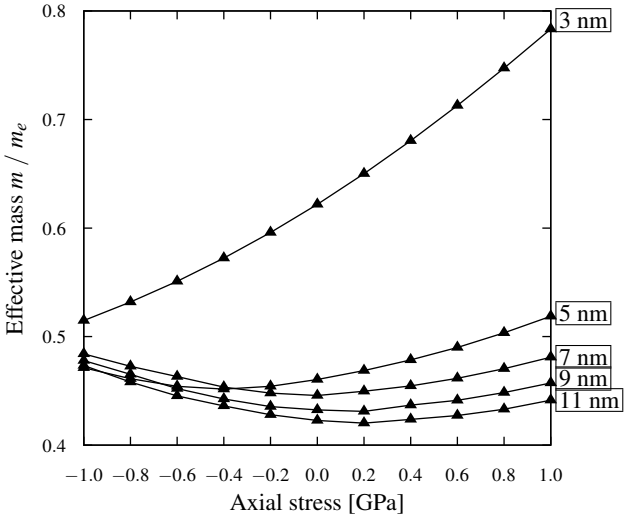

Fig. 2: Stress dependence of the effective mass for [111] nanowires of different thicknesses

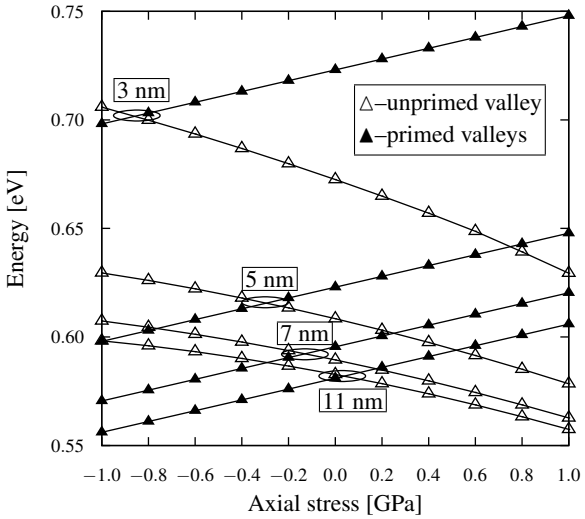

Fig. 3: Energy of valley minima for varying axial stress and different thicknesses of [110] nanowires

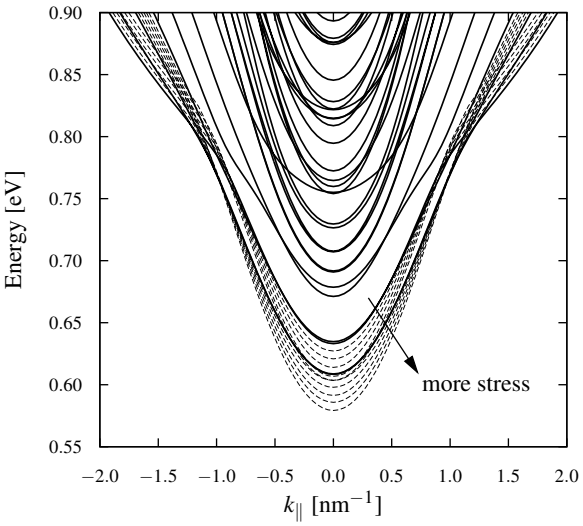

Fig. 4: Unprimed subbands in a [110] nanowire; solid line–unstrained, dashed lines–tensile axial stresses up to 1 GPa (shown for the four lowest subbands only)

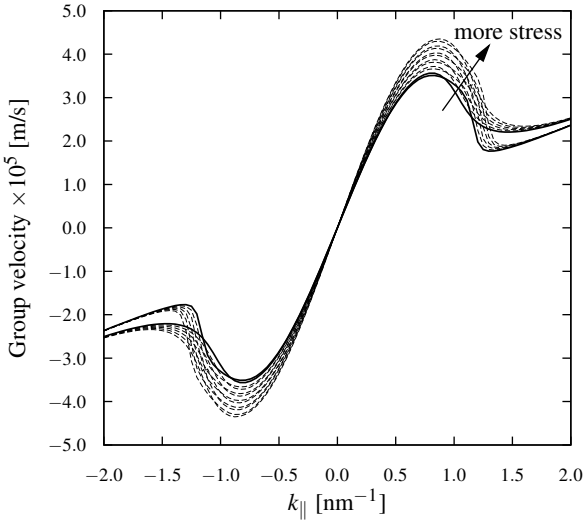

Fig. 5: Group velocities of the twol owest subbands in a [110] nanowire; solid line–unstrained, dashed lines–tensile axial stresses up to 1 GPa

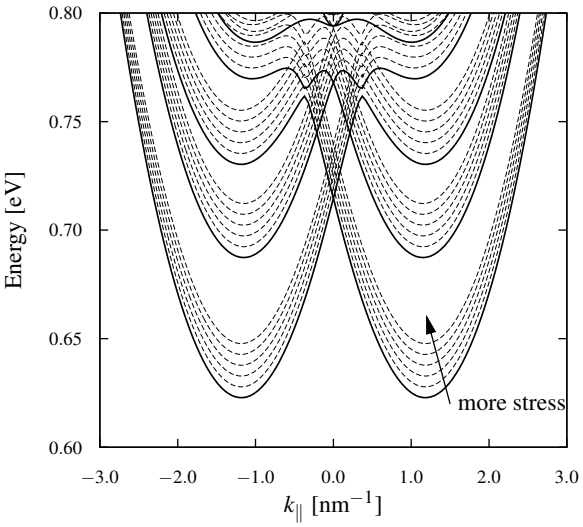

Fig. 6: Primed subbands in a [110] nanowire; solid line–unstrained, dashed lines–tensile axial stresses up to 1 GPa; plot is centered around the edge of the Brillouin zone.

Quantum computing on silicon-on-insulator structure

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1. Abstract

The structure for quantum computation based upon field-defined quantum dots in an ultrathin SOI body is proposed. The strong uncontrollable Coulomb interaction between qubits is suppressed because of no charge transfer during computation. The encoding and processing of quantum information is performed only on symmetric and antisymmetric states in double quantum dots.

2. Main issues of solid-state quantum computers

Quantum computers (QC) are much relied upon in view of their dramatic efficiency with regard to classical computers. Namely, there exist some quantum algorithms which allow to find a solution of a particular problem exponentially faster than their classical counterparts, e.g. the Shor's algorithm for factorization of large numbers into two prime numbers. Quantum computers are believed to revolutionize such fields of science as cryptography, communication, data storing and processing, computer science and algorithms, modeling of quantum processes and so on [1]. Despite advances in mathematical aspects of quantum computations, the practical realization of quantum computers still remains a formidable challenge. Nevertheless, the great interest to this problem resulted in several different approaches to organize a quantum computer architecture: ions in traps, liquid and solid state computers based on nuclear magnetic resonance, quantum dots with spin and space states, superconducting circuits. Although these proposals are very different, all of them should satisfy the following five rules for quantum computation to be possible: 1) Quantum register is composed of qubits, i.e two-level quantum systems (large-scale QC contains at least 1000 qubits); 2) Initialization procedure is to be provided; 3) Performance of one- and two-qubit operations with the accuracy not worse than 0.01%; 4) Decoherence processes of quantum register are much suppressed; 5) Read out of a final state as precise as possible. Unfortunately, the above suggestions have severe drawbacks and cannot meet all the necessary requirements. For the sake of brevity, we omit the advantages and shortcomings of various QC architectures in this abstract. Here, the only comment is that charge states are relatively easy to initialize and measure but they decohere too fast in comparison with spin states, but the latter ones are hardly measurable. The goal of our paper is to attack the problem from an alternative perspective, namely, to consider the possibility of creating a QC with the help of rapidly developing SOI technology.

3. SOI quantum computer

Following a major tendency from micro- to nano-electronics, the technology of semiconductor devices undergone a rapid development and gave rise to SOI layers. This fact enables us to manipulate individual quantum dots either by etching [2] or maintaining an adequate electric potential distribution. Further, quantum dots can be inhabited by electrons. As mentioned above, quantum information can be encoded in either spin or space degrees of freedom. We will focus attention to space states in quantum dots, since they can be controlled by electrical impulses only (initialization, one- and two-qubit operations, read-out). Moreover, such a consideration reflects and follows a natural way of nano-electronics history.

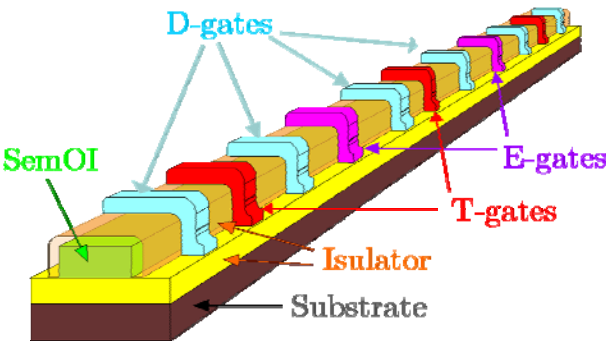

Fig.1: *Sketch of the designed structure for a quantum computer based on an ultrathin silicon body.*

Qubits are usually organized in the form of double quantum dots (DQDs), where quantum information is encoded in localized states of the electron.

Unfortunately, such a construction is vulnerable to an uncontrollable interaction between even distant qubits due to long-range Coulomb forces. The rough estimation of phase decoherence time for realistic two double quantum dot (DQD) qubits of a size 10nm placed at a relatively long distances of the order of 100nm from each other leads to decoherence time roughly 10^{-10}s which is far from practical requirements. The worst thing is that, in contrast to other sources of decoherence, this one cannot be suppressed by lowering the temperature.

Uncontrollable Coulomb interaction is absent whenever there is no charge transfer during computations and data storing. The coding of information seems to be impossible in this case. Luckily, it was shown recently [3,4] that quantum computation can be organized on space states of qubits without charge transfer. To anticipate, encoding and processing of quantum information is merely performed on symmetric and antisymmetric states in DQDs. Each qubit is implemented in a pair of quantum dots with a single electron (DQD).

Although the original proposal implied an identity of quantum dots and perfect symmetry of the structure [3], it was shown later that this severe obstacle for an experimental realization can be withdrawn [4]. The only demand remained is that the energy levels of individual dots coincide. It could be done with an appropriate voltage applied to adjacent electrodes.

The quantum register comprises a chain of qubits separated by gates operating on the strength of exchange interaction between adjacent DQDs. It is worth noting that one- and two-qubit operations as well as decoherence processes are investigated for such a structure in [3,4]. They indicate that there are no principal limitations for this scheme to work properly.

Employing the SOI technology, it is feasible to map the hypothetical idea onto a real physical structure (Fig. 1). In fact, if a SOI bar is covered by metallic gates as depicted in Fig. 1, then D-electrodes play two roles at the same time: they form quantum dots (by applying positive voltage) and adjust ground energy levels of quantum dots to coincide. The electrode E operates on the strength of exchange interaction between electrons in DQDs. The electrode T varies tunneling coupling between quantum dots constituting a DQD. Scalability of this scheme is evident and it opens up great possibilities for large-scale quantum computers.

The potential profile along the channel which defines quantum dots is scketched in Fig. 2. The quantum dots are designed in a way to take advantage of an ultrathin silicon body. Then the minimum confinement energy in a quantum dot could be roughly estimated via the relation

$$\varepsilon_0 \approx \hbar^2 \left[\frac{1}{m_l d_{Si}^2} + \frac{1}{m_t D^2} \right],$$

where $m_t=0.19m_0$ is a transversal electron effective mass, $m_l=0.98m_0$ is a longitudinal effective mass, d_{Si} is a silicon layer (body) thickness, D is a length of gates and a width of silicon bar. For the ultrathin silicon body $d_{Si}\approx$2nm and a technological node of D≈10nm one obtains the confinement energy approximately equals $\varepsilon_0\approx$0.01eV. Besides, the Coulomb repulsion energy of two electrons in a dot is also fairly high $\varepsilon_C\approx$ 0.01 eV to guarantee that any dot can be occupied with only one electron at sufficiently low temperature.

The output data of the computer must be encoded in charge states of DQDs. After that a read-out could be performed via manipulation with gate potentials and transmission of a current through the silicon bar. The value of current depends upon a charge distribution inside the channel [5].

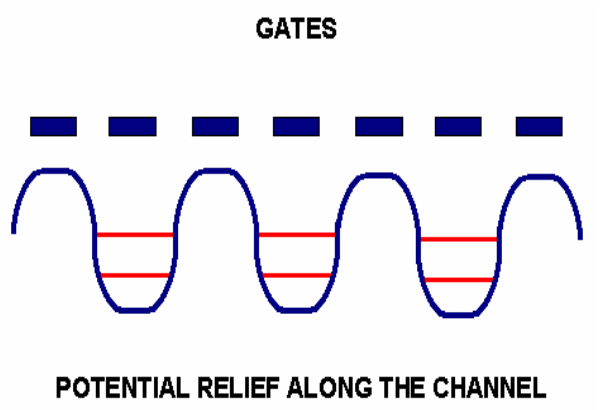

Fig.2: *Potential along the channel defines quantum dots.*

4. Conclusions

SOI structure for quantum computation is proposed. It reminds a multi-gate field-effect transistor. The quantum dots are formed with gate potentials. The lateral size of elements 10-20nm is sufficient to observe all requirements for solid-state quantum computers.

Acknowledgement

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Asymmetric Series Association of SOI MOSFET to Improve the Device Analog Characteristics

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1. Abstract

This paper proposes the use of asymmetric series association of SOI MOSFETs to improve the device analog characteristics and compares the asymmetric and symmetric series association. This analysis is done through results of numerical simulations and measurements.

2. Introduction

A common way to decrease the output conductance of MOSFETs is to use the cascode or series association of two transistors working as a single one (hereafter called symmetric series association)[1]. When the sizes are appropriately chosen, the DC characteristics of the composite transistor are the same as that of a singles transistor with a longer channel. Normally the two transistors in the series association have the same doping concentration applied to the channel region.

In this paper the asymmetric series association of SOI MOSFETs is proposed to improve the analog characteristics such as transconductance, output conductance and intrinsic voltage gain. The proposal is to have a device with lightly doped channel (N_{AL}) in the side of drain electrode (MD) of the composite transistor in series with a standard doped transistor (N_{AH}) in the source side (MS). A comparison between the asymmetric and symmetric series association with different technologies is done in order to analyze the impact of this new configuration on the analog parameters. Fig.1 shows the proposed architecture of an asymmetrical and the conventional symmetric series association of SOI MOSFETs.

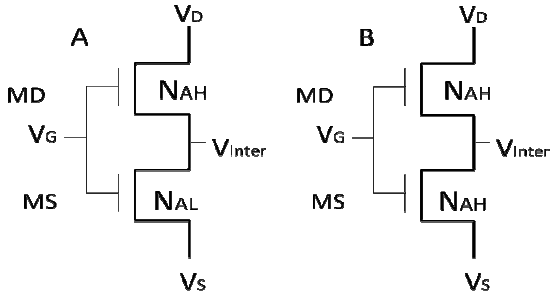

Fig.1: *Series association of two standard SOI transistors: proposed asymmetric one (A) and symmetric one (B).*

3. Experimental Results

Measurements of symmetric and asymmetric series association as well as for a single transistor have been performed using transistors implemented in a fully-depleted SOI technology featuring silicon film thickness of t_{Si}=80 nm, buried oxide thickness of t_{oxb}=390 nm and gate oxide thickness of t_{oxf}=30 nm. The devices present channel length (L) of 2 µm, 1 µm and channel width of 20 µm. The channel doping is $N_{AH}=6x10^{16}$ cm^{-3} for the standard doped transistor and $N_{AL}=10^{15}$ cm^{-3} for the lightly doped one. Table 1 shows the values of threshold voltage (V_{TH}) for different device architectures under study.

Table 1: *Threshold voltage for different structures.*

L [µm]	Threshold Voltage [V]		
	Asymmetric	Symmetric	Single Device
1	0.28	----------	----------
2	0.36	0.37	0.39

It is possible to verify that threshold voltage remains almost with the same for the devices composed by 2 µm long transistors as it is fixed by the transistor in the source side.

Fig. 2 presents the measured drain current (I_{DS}) and transconductance (g_m) *versus* gate voltage (V_{GF}) with drain bias (V_{DS}) of 1.5 V. The I_{DS} and output conductance (g_D) *versus* V_{DS} curves are presented in Fig. 3, measured with gate voltage overdrive, $V_{GT}=V_{GF}-V_{TH}$ of 200 mV.

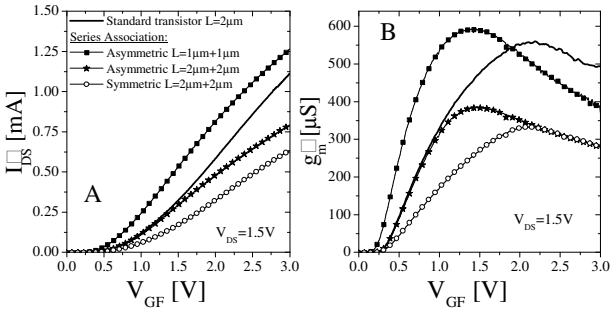

Fig. 2: *Experimental drain current (A) and transconductance (B) as a function of gate voltage for different structures.*

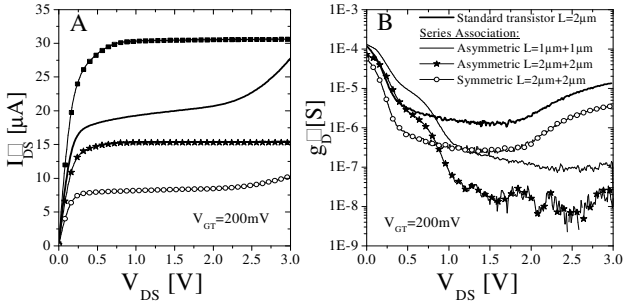

Fig. 3: *Experimental drain current (A) and output conductance (B) as a function of drain voltage for different structures.*

From the I_{DS} *versus* V_{GF} and I_{DS} *versus* V_{DS} curves one can

see that the symmetric series association presents almost half of the drain current of standard SOI transistor and asymmetric series association, since it acts as a single transistor with L=4µm (2µm +2µm) [4]. On the other hand, Fig. 2 (A) shows that I_{DS} of the asymmetric series association is close to the standard SOI transistor for V_{GF} values up to 1.5V. While the highly doped transistor is responsible for fixing the V_{TH} of the asymmetric structure, the second transistor, which is lightly doped and presents negative V_{TH}, acts as an extension of the drain region, reducing the effective channel length of the composite structure to the length of the transistor at the source side (MS). Therefore in the asymmetric series association with L=1 µm + 1 µm the g_m is larger than for the single transistor with L= 2 µm SOI, as it behaves as a single transistor with approximately L=1 µm, as can be seen in the figure 2 (B).

From the results of the fig. 3 (A) one can see that the asymmetric series association has larger I_{DS} in saturation than the symmetric one and both have smaller I_{DS} than the single transistor with L= 2 µm. On the other hand, one can note in Fig. 3 (B) that g_D in both studied asymmetric series association are lower than for the single SOI device and the symmetric series association.

Figure 4 presents the voltage in the intermediate node (V_{Inter}) node *versus* V_{GF} for the structures operating in saturation. In this figure it can be seen that for the symmetric series association initially the intermediate node voltage (V_{Inter}) is almost zero because the two transistors are in subthreshold region. After V_{GF} exceeds V_{TH}, V_{Inter} linearly increases while the composite transistor remains in saturation. Similar behavior is observed with V_{DS}=3V. For the asymmetric series association the value of V_{Inter} is always larger than for the symmetric one with similar dimensions as the transistor MD has smaller threshold voltage and, for the same V_{DS} and V_{GF}, smaller channel resistance. Also the variation of V_{Inter} in the overall excursion for the V_{GF} varies in a smaller range than for the symmetric one. In the asymmetric series association I_{DS} is larger than symmetric one due to fact that the asymmetric association presents reduced effective channel length (half of total channel length as mentioned earlier).

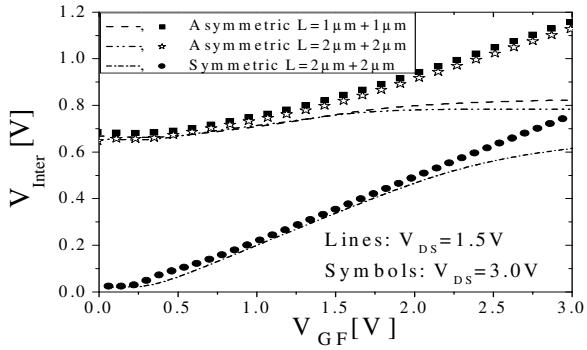

Fig.4: *V_{Inter} x V_{GF} operating in saturation region, with V_{DS}=1.5 V and 3V.*

Table 2 shows the intrinsic voltage gain ($A_V=g_m/g_D$) for asymmetric, symmetric series association and standard transistors. It can be observed that that gain obtained in the asymmetric series association is larger than that of standard SOI transistor and symmetric series association. Taking the standard SOI transistor as reference it is observed an increase of 40 dB when using the asymmetric association while for the symmetric series association this increase is of 8 dB. Even reducing the L of both transistors in the asymmetric series association an improvement of 20 dB with respect to the symmetric one can be obtained.

Table 2: *Intrinsic voltage gain voltage for different structures.*

L [µm]	Asymmetric [dB]	Symmetric [dB]	Single Device [dB]
1	59	----------	----------
2	78	39	31

4. Numerical Simulation Analysis

In order to verify if the proposed asymmetric series association is effective in more advanced technological nodes, two dimensional simulations were performed using Atlas [5]. For the simulations the technologies with minimum channel length of 150 nm (t_{si}=40 nm, t_{oxf}=2.5 nm, $N_{AH}=7x10^{17}$ cm^{-3} and t_{oxb}=155 nm [6]) and 100 nm (t_{si}=30 nm, t_{oxf}=50 nm, $N_{AH}=1x10^{18}$ cm^{-3} and t_{oxb}=100 nm [7]) have been used. In both cases the L has been fixed in 150nm. Physical models accounting for mobility dependence on velocity saturation and doping concentration, bandgap narrowing, Auger recombination, doping-dependent lifetime, mobility degradation due to the lateral and parallel electric fields have been considered in the simulations.

Table 3: *Transconductance, output conductance and intrinsic voltage gain for different configurations and technologies.*

Technology	Architectures	g_m [µS]	g_D [µS]	A_V [dB]
100 nm	Symmetric	245	5.16	34
	Asymmetric	400	0.98	52
150 nm	Symmetric	416	24.1	25
	Asymmetric	581	1.59	51

The gain is always larger in the asymmetric series association with an improvement of about 18 dB for the 100 nm technology and up to 26 dB for the 150 nm technology. These improvements are related to the g_D provided by the asymmetric series association.

5. Conclusions

A comparison between the analog performance of the proposed asymmetric series association of SOI transistors with standard uniformly doped SOI MOSFETs and symmetric series association was done. Asymmetric series association has better output parameters in comparison to symmetric series association and standard SOI transistor, leading to remarkably improved voltage gain. The improvements provided by the asymmetric series association have been verified experimentally and by numerical simulations in 150 nm and 100 nm technologies.

Acknowledgments

The authors acknowledge to the Brazilian research-funding agencies FAPESP, CAPES and CNPq for the financial support to this work.

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Impact of Mismatch on the Analog Properties of Standard and Graded-Channel SOI nMOSFETs

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1. Abstract

In this work an experimental evaluation of mismatch due to process variability influence over analog characteristics of fully-depleted graded-channel SOI transistors is presented. Uniformly doped transistors were also measured for comparison purposes.

2. Introduction

Graded-Channel (GC) Fully-Depleted (FD) SOI nMOSFET is an asymmetric channel device that has shown to efficiently improve the SOI analog characteristics [1]. In this device, the threshold voltage (V_{TH}) ion implantation is performed at the source side only, and the natural wafer doping concentration is kept in the region near the drain. This lighly doped (LD) region presents negative V_{TH}, and acts as an extension of the drain region, reducing the effective channel length (L_{eff}=L–L_{LD}, L is the total mask channel length and L_{LD} is the lightly doped region length). Several works report advantages of GC devices over uniformly doped ones for analog applications [1-3], namely larger transconductance (g_m), reduced drain output conductance (g_D), and improved linearity. The design of precise analog circuits relies on the concept of matched devices. Despite the advantages of GC transistors for analog applications, few information regarding the matching properties of GC SOI transistors is known [4], especially in saturation region.

In this work the impact of mismatch on the analog characteristics of GC FD SOI transistors is presented. The results obtained for uniformly doped transistors with standard doping concentration are also shown for comparison purposes. Focus will be given to the drain current, transconductance, Early voltage and g_m/I_{DS} ratio, looking at their standard deviation (σ) and/or relative mismatch (σ/mean value).

3. Test Structure and Devices Characteristics

Arrays of 20 identically-designed transistors each were fabricated in a FD SOI CMOS technology featuring t_{Si}=80nm, t_{oxf} =31nm, t_{oxf} =390 nm, $N_A \cong 6\times10^{16}$ cm^{-3} [5]. Uniformly doped and GC transistors with two different L_{LD}/L ratios were fabricated (L_{LD}/L=0.29 and 0.44). All devices present channel width (W) of 20 µm and length (L) of 2 µm. The experimental mean values for g_m as a function of the gate voltage (V_{GF}), drain current (I_{DS}) and g_D as a function of the drain voltage (V_{DS}) are presented in Fig. 1. From these curves it is possible to note the increase of I_{DS} and g_m promoted by the presence of the lightly doped region, and this improvement becomes larger as L_{LD}/L increases. In addition, an improvement (reduction) on g_D is observed.

4. Results and Discussion

Fig. 2 presents the V_{TH} relative mismatch as a function of $(W\times L_{eff})^{-1/2}$ for all measured devices. The obtained results follow a linear behavior intersecting the origin, as for the data reported in [6-7] for several bulk MOS devices. These results indicate that GC transistors V_{TH} mismatch behaves similarly to uniformly doped ones with reduced L_{eff}.

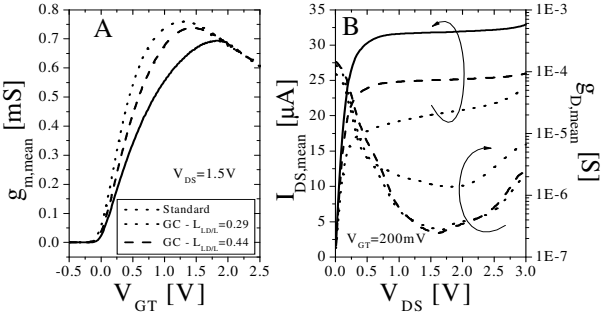

Fig.1: *Mean g_m as a function of V_{GF} (A), I_{DS} and g_D as a function of V_{DS} (B), measured for arrays of 20 identical transistors with L=2µm, with uniformly doped and graded-channel configurations.*

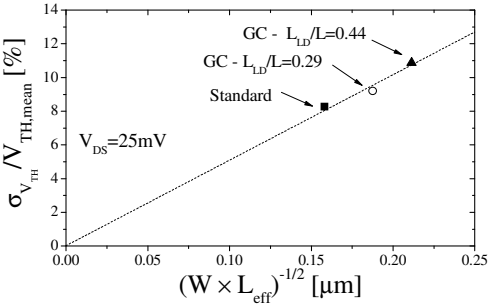

Fig.2: *Relative threshold voltage mismatch, extracted for uniformly doped and GC SOI transistors.*

The I_{DS} standard deviation and its relative mismatch, measured in linear and saturation regions (V_{DS}=25mV and 1.5V, respectively) as a function of the normalized mean drain current ($I_{DS,mean}/(W/L_{eff})$) are presented in Fig. 3. GC transistors present slightly larger I_{DS} standard deviation than the uniformly doped device for similar $I_{DS,mean}/(W/L_{eff})$, mainly due to the L_{eff} reduction and the mismatch that may occur in its definition during devices processing. As mean I_{DS} is increased by the use of GC architecture, the relative I_{DS} mismatch (Fig. 3B) can even be smaller than the observed for uniformly doped transistors, as in the case of GC transistor with L_{LD}/L=0.44. In weak inversion, the relative I_{DS} mismatch is nearly independent on V_{DS}, as it is dominated by the V_{TH} variation. As devices move to moderate/strong inversion (higher $I_{DS,mean}/(W/L_{eff})$), the mismatch is reduced both in linear and saturation regions, and all devices tend to the same values of relative mismatch. In addition, I_{DS} standard deviation and relative mismatch are worsened by V_{DS} increase in moderate/strong inversion.

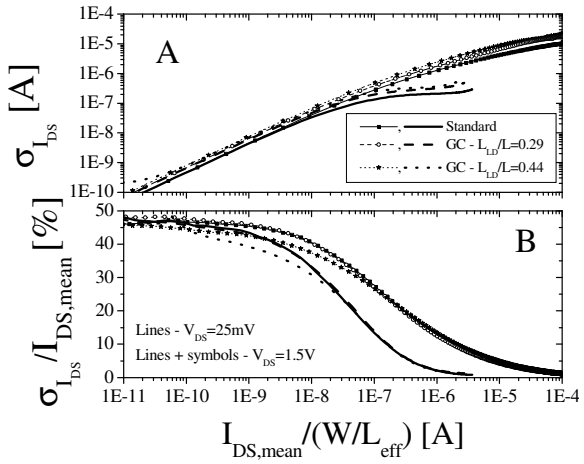

Fig. 3: *Standard deviation (A) and relative mismatch (B) of I_{DS} as a function of $I_{DS,mean}/(W/L_{eff})$, measured in linear (V_{DS}=25mV) and saturation (V_{DS}=1.5V) regions.*

Fig. 4 presents g_m standard deviation and relative mismatch as a function of the gate voltage overdrive ($V_{GT}=V_{GF}-V_{TH}$). As presented, g_m standard deviation is worsened both by the use of the GC structure and by L_{LD}/L ratio increase. However, g_m relative mismatch is only slightly higher for GC transistors (the worsening is smaller than 0.6 % for $V_{GT}\leq 0$ in all cases), as an effect of improved mean g_m value, as shown in Fig. 1A.

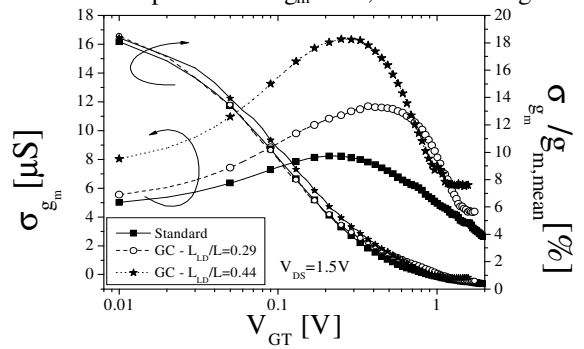

Fig. 4: *Standard deviation and relative mismatch of g_m as a function of V_{GT}, measured at V_{DS}=1.5V.*

The g_m relative mismatch has been extracted for different V_{GT} and V_{DS} values and is presented as a function of $(W\times L_{eff})^{-1/2}$ in Fig. 5A. As for V_{TH} (Fig. 2), g_m relative variation follows a straight line, proportional to $(W\times L_{eff})^{-1/2}$, showing that GC devices are behaving similarly to uniformly doped ones with reduced L_{eff}. While V_{DS} has no influence on g_m relative variation, the increase of V_{GT} reduces the mismatch, as V_{TH} variation have less impact on I_{DS} mismatch [8].

Fig. 5 also presents the relative variation of the Early voltage ($V_{EA}=I_{DS}/g_D$), extracted through the linear extrapolation of I_{DS} *versus* V_{DS} curves, for $1V \leq V_{DS} \leq 2V$, at different V_{GT} values. Even though the g_D (and consequently V_{EA}) standard deviation in GC devices is higher than for the standard ones, the relative V_{EA} mismatch is attenuated by the larger mean values of V_{EA} presented by GC transistors ($|V_{EA,mean}|$= 10.5V, 79.3V and 101.7V, for standard transistor, GC with L_{LD}/L=0.29 and 0.44, respectively).

From the analog design point of view, another important parameter is the g_m/I_{DS} ratio, since it is related to the intrinsic voltage gain ($A_V=V_{EA}\times g_m/I_{DS}$). The g_m/I_{DS} mean values and relative variation are presented in Fig. 6 as a function of V_{GT}.

As shown, the mean values of g_m/I_{DS} are virtually the same for all devices. On the other hand, the presence of the lightly doped region slightly increases g_m/I_{DS} variation, although the maximum degradation is in the order of 1%. For all devices, higher g_m/I_{DS} mismatch is observed around V_{TH} and, following both I_{DS} and g_m, the mismatch reduces with V_{GT} increase.

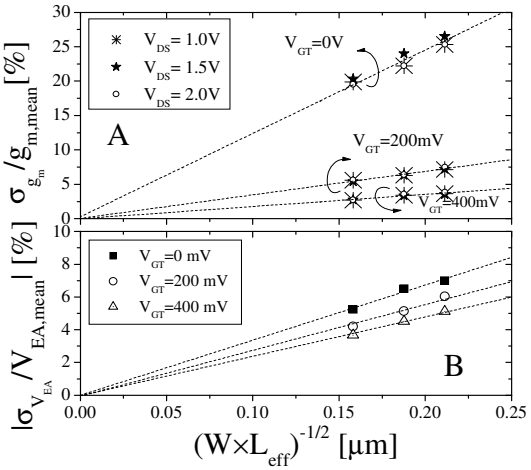

Fig.5: *Relative g_m and Early voltage mismatch as a function of $(W\times L_{eff})^{-1/2}$, extracted for uniformly doped and GC SOI transistors.*

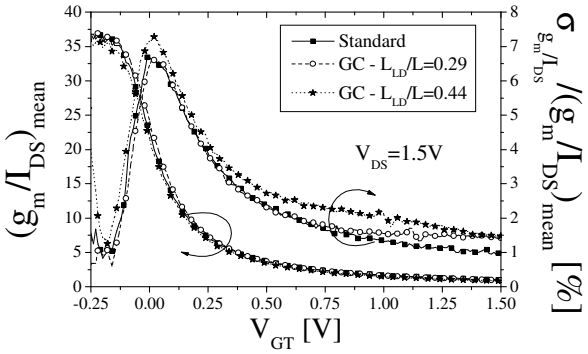

Fig.6: *Mean values and relative mismatch of g_m/I_{DS} as a function of V_{GT}, measured at V_{DS}=1.5V.*

5. Conclusions

This work presented the mismatch impact on analog parameters of GC SOI transistors in comparison to uniformly doped ones. Although a significant matching degradation for GC MOSFETs electrical parameters could be expected, due to device processing peculiarities which could cause errors in the L_{LD}/L definition, the obtained results had shown that the relative variation of the analyzed parameters are only slightly worsened by the GC structure, presenting values similar to those of standard transistors.

Acknowledgments

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Insights on Device Performance of SOI MOSFET with 60 nm and 15 nm BOX Thickness

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1. Abstract

A simulation study is carried out on low power 22 nm technology generation UTB SOI n-MOSFET based on thick (60nm) and thin (15nm) BOX thickness design scenarios. The impacts of global variations of silicon body thickness (T_{si}) and equivalent oxide thickness (EOT) on device performance are investigated in detail under these two BOX design scenario. The results indicate that although thick BOX design is compatible with traditional SOI CMOS process, thin BOX design can offer better electrostatic integrity and is more resilient to global variations of T_{si} and EOT.

2. Introduction

Progressive scaling of transistors have a huge impact on semiconductor industry due to the demand of high speed, low cost and multi functionality IC products[1]. Until now, scaling down the dimension of planar bulk transistors is the best way to increase the density of transistors in chip. However, progressive scaling of bulk MOSFET is approaching the limit due to high channel doping concentration and thin gate oxide needed to control an electrostatic integrity which results in increased leakage and very high dopant induce statistical variability [2], thus introduce problems such as statistical timing variability which complicate the circuit and system designs [3].Therefore, increasing efforts have been invested in developing new device structures to mitigate the leakage and variability challenge. It is expected that bulk MOSFET will be replaced very soon by UTB SOI devices due to the fact that UTB SOI structure can tolerate very low channel doping concentration. In adition the buried oxide (BOX) can reduce junction capacitances which contribute to a fast switching and signal propagation in circuit[4].The UTB SOI device could be introduced according ITRS 2009, starting from 22 nm physical gate length, to replace the bulk MOSFETs. This work presents a TCAD simulation study of UTB SOI MOSFETs for low power 22 nm technology generation. Two BOX thickness design scenarios are considered, with special emphasis on their corresponding response on globalvariation of T_{si} and EOT.

3. Nominal Device Design and Simulation

The 32nm TB SOI device designed by PULLNANO consortium is employed as the starting point in the design of 22nm device while design recommendations from latest ITRS is used as the reference. The device design is targeted at low power application, with supply voltage (V_{dd}) of 0.8V. A comprehensive design study has been carried out resulting in well behaved 22nm TB SOI device featuring TiN metal gate and high-k dielectric with EOT of 0.9nm. The silicon body thickness is 7nm and the channel doping concentration is 1.2e15 cm^{-3}. Apart from thin BOX design scenario with 15nm of BOX thickness, thick BOX design scenario with 60nm of BOX thickness is also considered here due to its compatibility with existing SOI process. The Ion / Ioff of proposed 22nm template devices are 858μA/μm / 5nA/μm (BOX of 15nm) and 964μA/μm / 72nA/μm (BOX of 60nm) respectively.

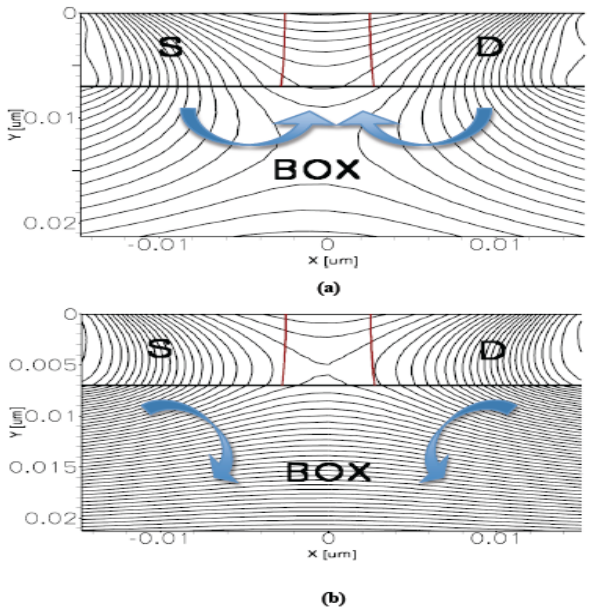

Fig.1: *Electrostatic potential (a) Thick BOX (b) Thin BOX at Vgs=0V, Vds=0.05V*

The 2D effect introduced by thick BOX is the primary reason behind the high leakage current that occurs in device with BOX of 60nm. Fig.1 illustrates the electrostatic potential distribution in both cases under

low drain bias condition. It clearly demonstrates that for thick BOX device, the electric field in BOX that originate from S/D region tend to terminate in the channel region, result in strong BOX-field fringing effect. While for thin BOX counterpart, in BOX, the electric field originates from S/D region and tends to terminate in BOX as well, resulting in much reduced BOX-field fringing effect. As a result, the degrees of electro-static integrity are different in these two devices; consequently, depending on the thickness of BOX, the impact of variation of T_{si} and EOT on device characteristics can also be different.

4. Simulation Set-up and Analysis

A set of simulations explore the design space of this device including the impact of global variation of EOT and Tsi on behaviors of two fundamental device figures of merits: Subthreshold Slope (SS) and Drain Induced Barrier Lowering (DIBL). The nominal values of EOT and Tsi are 0.9nm and 7nm respectively. In order to explore a broad range of design space, the EOT value is spread from 0.7nm to 1.1nm, and Tsi value is spread from 5nm to 9nm.

In this work, we treat each individual variability source separately, Tsi value is fixed at 7 nm in EOT variation study and EOT value is fixed at 0.9 nm in Tsi variation study. The impact of EOT and Tsi variations upon SS and DIBL of thick and thin BOX devices are presented in Fig.2 and 3 respectively.

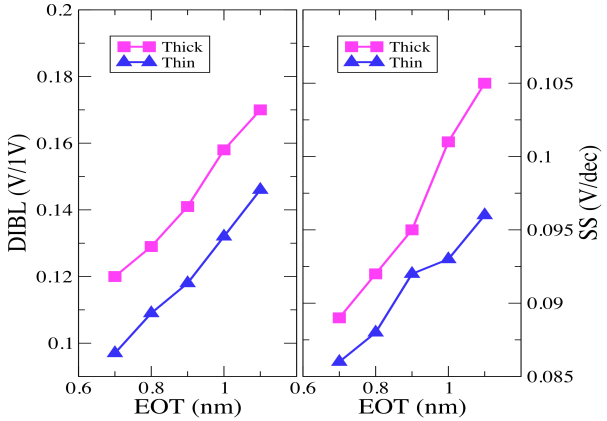

Fig.2: *Trend of DIBL and SS against variation of EOT*

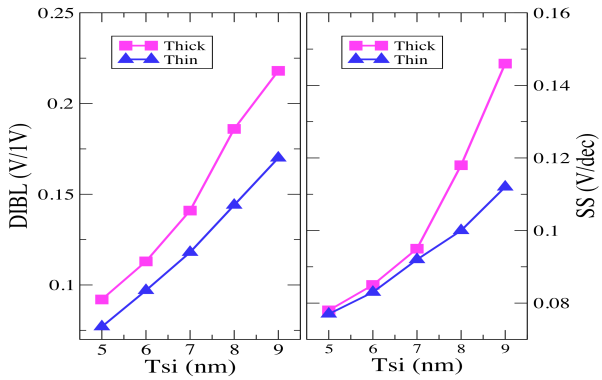

Fig.3: *Trend of DIBL and SS aginst variation of T_{si}*

With EOT varied from 0.9nm to 0.7nm, for device with thick BOX of 60 nm, the DIBL is reduced from 141mV per 1V to 120mV per 1V, and the SS is reduced from 95mV/dec to 89mV/dec. For device with thin BOX of 15nm, similar level of improvement is obtained, with DIBL reduced from 118mV per 1V to 97mV per 1V, and SS reduced from 92mV/dec to 86mV/dec. With EOT varied from 0.9nm to 1.1nm, for both thin and thick BOX devices, the amount of degradations on DIBL are similar, around 30mV per 1V. However, in respect of SS the device with thin BOX exhibits much strong resilience yielding degradation of 4mV/dec compared to 10mV/dec in thick BOX counterpart.

With Tsi varied from 7nm to 5nm, similar amount of DIBL and SS improvement can be achieved for both thin and thick BOX devices. However, with Tsi varied from 7nm to 9nm, device with thin BOX exhibits much strong resilience towards the degradation of DIBL and SS, with 52mV per 1V on degradation of DIBL and 20mV/dec on degradation of SS respectively. While for device with thick BOX, the corresponding values are 77mV per 1V and 51mV/dec respectively. It is observed, in general, that thick BOX renders larger sensitivities of electrostatics especially SS variations introduced by EOT and Tsi fluctuations.

5. Conclusions

Two BOX design scenarios are considered in design and simulation study of 22nm template TB SOI devices, the results indicate that not only the better control of short channel effect and extra electrostatics integrity can be offered by thin BOX devices. This is due to the capability of thin BOX to suppress the field fringing that originates from source/drain junctions. Simultaneously the thin BOX device has better variability performance under the influence of global variation of EOT and Tsi..

Acknowledgements

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Using Diamond SOI nMOSFETs to Improve the Frequency Response of the Analog Integrated Circuits

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1. Abstract

This paper performs a comparative study of the voltage gain (A_V) between the Diamond (DSM) and Conventional SOI nMOSFETs (CSM) by using three-dimensional numerical simulations (3DNS). The same tendencies of the 3DNS are observed by the experimental results when we used bulk CMOS process.

2. Introduction

In order to improve the performance of the analog and digital integrated circuits several efforts have been performed to develop new planar and three-dimensional (3D) SOI MOSFETs [1]. Concerning the planar conventional transistors and focusing on "channel engineering", the circular-gate (CGSM) [2] and the graded-channel (GCSM) [3] SOI MOSFETs are examples of devices that are capable to further improve the performance of this kind of integrated circuits (ICs), in term of the drain current (I_{DS}), transconductance (g_m), transconductance over drain current (g_m/I_{DS}), Early Voltage (V_{EA}) and harmonic distortion (THD). Another example of an innovative transistor structure, recently developed, was the Diamond SOI MOSFET (DSM) [4-6] which uses a new engineering approach, named "drain/channel/source interfaces engineering" (DCSIE) that changes the gate geometry from rectangular to hexagonal in order to use the corner effect along the channel, called Longitudinal Corner Effect (LCE) [4-6] to improve the resultant longitudinal (parallel) electric field ($\vec{\varepsilon}_{//}$) along the channel and consequently improve the average drift velocity ($<\vec{v}_x>$), drain current (I_{DS}), transconductance (g_m) and on-state series resistance (R_{ON}). Studies performed with the Partially-Depleted (PD) Diamond SOI nMOSFETs by 3DNS, demonstrated significant improvements in terms of I_{DS}, g_m and R_{ON} in relation to the CSM counterpart, depending on how much obtuse the hexagonal gate geometry is, when we maintain the same gate area (A_G), same geometric factor (W/L) and similar bias conditions. So, the objective of this paper is also to verify what benefits the DSM can bring to the analog ICs in terms of the low frequency voltage gain (A_{V0}) and unit voltage gain frequency (f_T) when compared with the conventional CSM counterpart.

3. Simulation Results

Table I presents the dimensions of the PD CSM and DSM (α=90°) counterpart studied by the 3DNS (Sentaurus).

Table I. *Dimensions of the CSM and DSM (α=90°) .*

#	W (µm)	L_{eff} (µm)	W/L	B (µm)	b (µm)	A_G (µm²)
CSM	5.95	4.0	1.48	-	-	23.9
DSM	5.95	4.0	1.48	7.00	1.05	23.9

The technological parameters of these devices are: gate-oxide (t_{ox}), silicon-film (t_{SI}) and buried-oxide (t_{BOX}) thickness respectively are 2.5 nm, 100 nm and 400 nm, and the channel and drain/source doping concentrations are $5.5x10^{17}$ cm^{-3} and $1x10^{20}$ cm^{-3}, respectively. The models used for the 3DNS were: Phumob, enormal, SRH, BandGapNarrow, Avalanche(CarrierTempDrive). Figure 1 presents the $I_{DS}/(W/L)$ and $g_m/(W/L)$ vs V_{GS} respectively, $I_{DS}/(W/L)$ vs V_{DS} and g_m/I_{DS} vs $I_{DS}/(W/L)$ curves of the DSM (α=90°) and CSM counterpart (3DNS results).

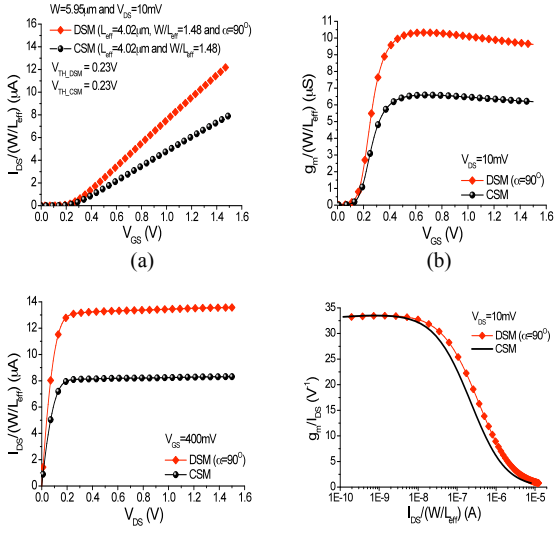

Fig. 1. *$I_{DS}/(W/L)$ vs V_{GS} (a), $g_m/(W/L)$ vs V_{GS} (b), $I_{DS}/(W/L)$ vs V_{DS} (c) and g_m/I_{DS} vs $I_{DS}/(W/L)$ (d) curves of DSM (α=90°) and CSM counterpart.*

Notice that, DSM $I_{DS}/(W/L)$, $g_m/(W/L)$, $I_{DS}/(W/L)$ in the saturation region and g_m/I_{DS} in the moderate inversion regime are always higher than those found in the CSM counterpart considering the same A_G, W and bias conditions. Table II compares the values of the g_m/I_{DS} in the moderate inversion regime ($I_{DS}/W/L$=130 nA), V_{EA} and A_{V0} of the DSM (α=90°) and CSM counterpart.

Table II. *g_m/I_{DS}, V_{EA} and A_{V0} of the DSM (α=90°) and CSM counterpart.*

#	g_m/I_{DS} (V^{-1})	V_{EA} (V)	$A_{V0}=(g_m/I_{DS}).V_{EA}$
CSM	20.8	55.5	1154
DSM	23.9 (+14.9%)	51.2 (-7.7%)	1224 (+6.1%)

Observe that, in the moderate inversion region, although V_{EA} DSM is smaller than the one verified in the CSM counterpart due to its higher $\vec{\varepsilon}_{//}$, the DSM A_{V0} is even higher (6.1%) than the one found in CSM counterpart due to the higher contribution (14.9%) of the g_m/I_{DS} (Fig. 1.d) in the determination of the DSM A_{V0}. Based on this analysis, the Diamond layout style can be used to improve the performance of the analog ICs. Besides that, knowing that the OTA A_{V0} is directly proportional to the product of the g_m/I_{DS} and equivalent V_{EA} of the output stage transistors [1], the DSM can also be as an alternative device to implement the differential pair to further improve the OTA voltage gain. Furthermore we do not recommend to its used in the output stages of the amplifiers, due to its smaller V_{EA} in comparison to the CSM counterpart.

3. Experimental Results

Knowing that Diamond layout style can be implemented in any CMOS technology of the ICs, we are also presenting some additional experimental results by using the conventional CMOS manufacture process (AMI, On-Semiconductor, MOSIS) in order to verify the benefits that the Diamond structure can bring to further enhance the performance of a single stage amplifier as compared to the conventional nMOSFET counterpart. Table III presents the dimensions of the nMOSFETs: two Diamond with α equal to 37° (DM1) and 53° (DM2) and their respective conventional nMOSFETs (CM1 and CM2) counterparts.

Table III. *CMs and DMs (α=37°) counterparts Dimensions.*

#	W (µm)	L_{eff} (µm)	W/L	B (µm)	b (µm)
CM1	5.95	9.98	0.596	-	-
DM1 (α=37°)	5.95	9.98	0.596	18.90	1.05
CM2	5.95	7.00	0.850	-	-
DM2 (α=53°)	5.95	7.00	0.850	12.95	1.05

The circuit used to measure the A_V as a function of the frequency (f) is showed in Figure 2 and Table IV presents the bias conditions of the transistors and the drain resistance (R_D) value that defines the low frequency voltage gain ($A_{V0} \cong g_m.R_D$) [1].

Table IV. *Bias conditions and the used R_D value, respectively.*

#	I_{DS}	V_{GS}	V_{DS}	R_D
CM1, 2	7.1 µA	1.15 V	1.41 V	83.3 KΩ
DM1, 2	7.1 µA	0.98 V	1.41 V	83.3 KΩ

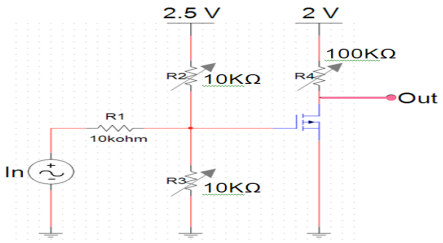

Fig. 2. *Circuit used to measure the A_V vs f.*

Figure 3 presents the curves of the voltage gain (A_V) as a function of the frequency of the DM with α equal to 37° (a) and 53° (b), respectively and their CMs counterparts and Table V presents the values of the A_{V0} and f_T that are extracted from Figure 3.

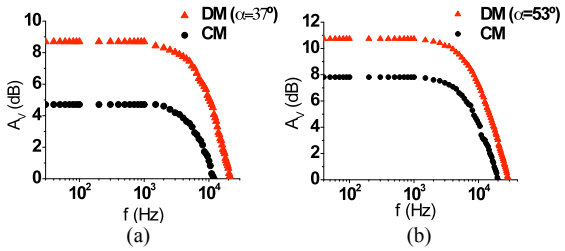

Fig. 3. *A_V vs f experimental curves of the CM and DM counterparts with α equal to 37° (a) and 53° (b), respectively.*

Table V. *A_{V0} and the f_T of the CMs and DMs.*

#	CM1	DM1 (α=37°)	Gain1 (%)	CM2	DM2 (α=53°)	Gain2 (%)
A_{V0} (dB)	5	9	+80	8	11	+37.5
f_T (kHz)	11	21	+91	20	29	+45

Observe that, the DM A_{V0} in dB and the DM f_T are practically two times higher than those found in the CMs counterparts. Besides that, while α is being increased (L_{eff} is reduced), the A_{V0} and f_T gains are being reduced, i.e., when α changes from 37° to 53°, the DM A_{V0} gain in dB diminishes from 80% to 37.5% and the DM f_T gain drops from 91% to 45%. These remarkable results can be explained due to higher DM g_m than the one observed in the CM counterpart.

5. Conclusions

Remarkable improvements in the A_{V0} and f_T can be reached by the use of the Diamond layout style when we compare to the analog ICs implemented with the conventional geometry. In conclusion, Diamond structure proves to be another device option for to further improve the frequency response of the analog ICs.

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DFT Simulation of SOI Devices: Semiconductor/Oxide Interfaces

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1. Abstract

We present a Density Functional Theory (DFT) study of the electronic properties of the interface between thin silicon films and SiO_2 in SOI devices. DFT provides an accurate description of materials at the atomic scale, where a fully quantum mechanical description is essential. Understanding and controlling defects at the interface between the silicon layer and the oxide is crucial when devices reach the ultimate level of miniaturization, since such defects affect the electronic transport and might critically degrade the device performance.

2. DFT simulation of Si/SiO_2 interfaces

The semiclassical tools successfully used until now to model traditional semiconductor devices are no longer adequate to address the quantum effects that arise in nanoscale devices such as ultra-thin body (UTB) silicon-on-insulator (SOI) devices. DFT is a quantum mechanical theory that enables the modeling of point defects such as missing atoms, dopants, etc., and other issues such as strain or surface reconstruction. It is thus an extremely useful tool to model the most-likely reconstructions of ideal and defected Si(001)/SiO_2 interfaces, which is the goal of this work. All our calculations have been performed with the SIESTA code [1], using the optimized basis and pseudopotentials described in [2].

2.1 SiO_2 modeling

The first stage is the modeling of the SiO_2 layer. Actual devices are fabricated with amorphous SiO_2, but such non-crystalline materials are hard to model from an atomistic point of view. We have then as a first approach described the oxide in its crystalline alpha-quartz (α-quartz) phase. α-quartz is well known to be the most stable phase of crystalline quartz. On a further step a more realistic description of the oxide will be tackled by the use of amorphous -instead of crystal- quartz. This complex approach requires performing a statistical analysis of different amorphous configurations in order to extract some trends in the oxide behavior beyond the particularities of each SiO_2 layer studied.

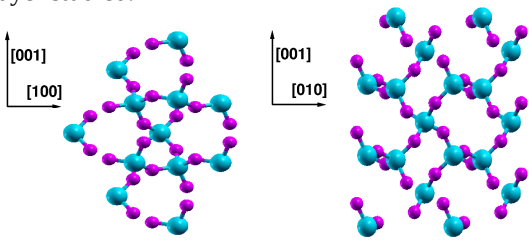

Fig. 1: *Ball-and-stick models of the front and lateral views of the SiO_2(001) layer. Silicon atoms are shown in cyan, oxygen atoms in pink.*

2.2 The Si/SiO_2 interface in SOI devices

We have next studied the electronic properties of the interface between a Si(001) slab and a top α-quartz layer, as a first stage towards the full atomistic

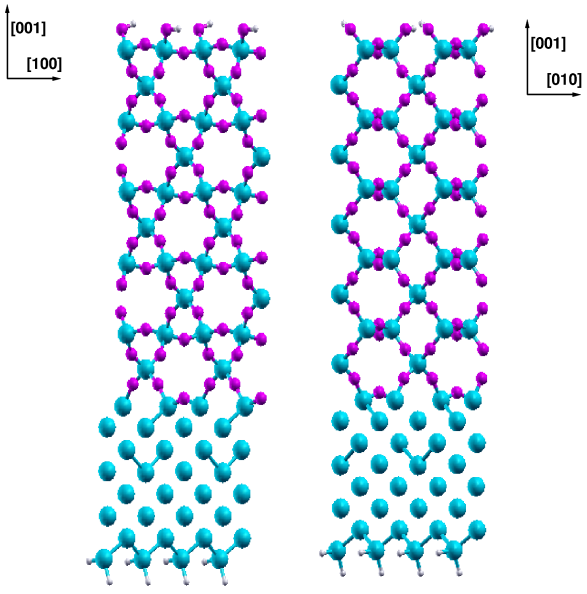

Fig. 2: *Front and lateral views of the Si(001)/SiO_2 interface after relaxation. Small white atoms represent hydrogen atoms passivating the dangling bonds at the surfaces.*

simulation of the whole device. Our self-consistent DFT simulation enables redistribution of ions and electronic charge, leading to the formation of new bonds that build the energetically most stable geometry. Special attention must be paid to the mismatch in the lattice constants of both crystals. We have worked with different thickness

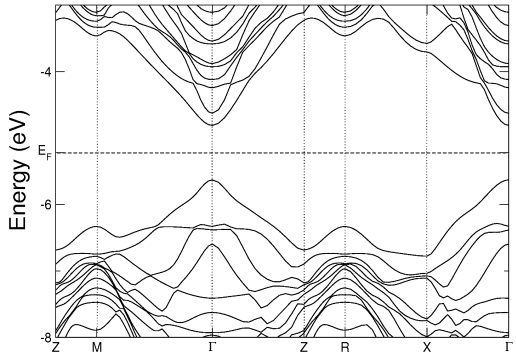

Fig. 3: *Band structure along high-symmetry k-points of the relaxed Si(001)/SiO_2 structure shown in Fig. 2.*

of silicon and oxide layers (between 1 and 3 nm) and have focused on how the actual sizes modify the band dispersion and the bandgap value for these nanostructures (see Fig. 3). After relaxation, and induced by the geometry of the Si layer, the SiO_2 layer

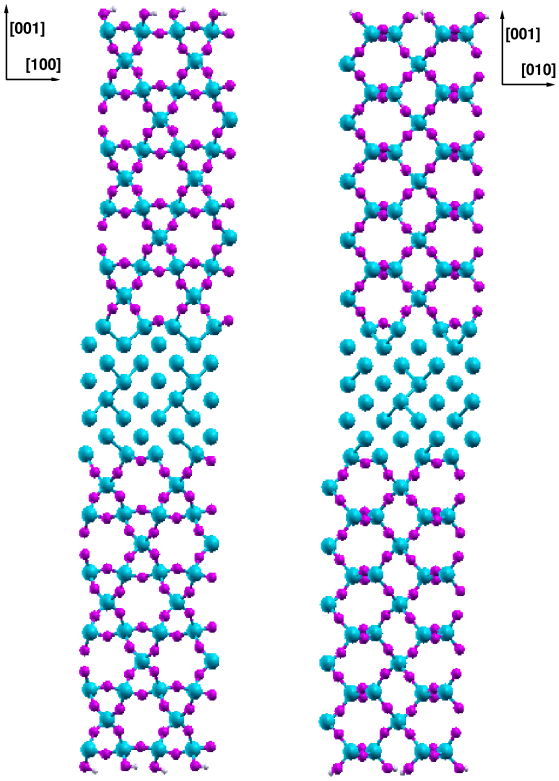

Fig. 4: *Schematic ball-and-stick models of the relaxed double-gate Si(001)/SiO_2 interface (lateral and front view).*

suffers a transition from the alpha to the beta (β) phase (see Fig. 2), a higher-symmetric but less stable phase of quartz when isolated.

The electronic structure of the oxide/silicon interface in double-gate SOI devices, shown in Fig. 4, has been also analyzed and compared to those of bulk Si and isolated Si slabs (see Fig 5). The reduced dimensions of these nanometer-scale systems have an immediate impact on the bandstructures, which can no longer be modeled as the bulk one. Parameters employed for transport simulations, such as effective masses and scattering rates, can be fitted to DFT bandstructure calculations in order to accurately reproduce the impact of interface imperfections and reduced device sizes. Vacancies, dopants and other point-like defects can also greatly impact the electronic properties of the Si/SiO_2 interface [3]. At the atomic scale, the presence of these defects at the interface might lead to a strong degradation of the device performance. We will address this analysis in a future work.

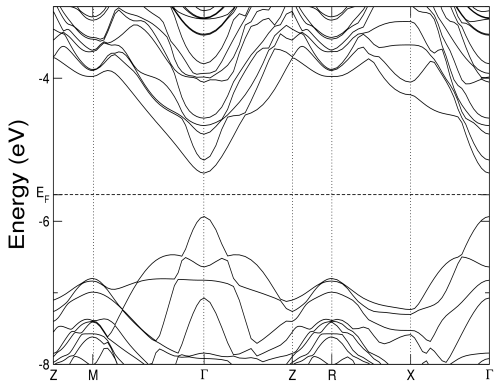

Fig. 5: *Band structure along high-symmetry k-points for the relaxed double-gate Si(001)/SiO_2 interface shown in Fig. 4.*

3. Conclusions

In order to understand and control the influence of reduced dimensions and point defects on the new generation of electronic devices, accurate simulations at the atomic-scale are needed. DFT provides a valuable tool to characterize the effect of defects such as vacancies, dopants, etc. We have addressed here the effect of confinement on the electronic structure of the Si(001)/SiO_2 interfaces. Our results show the influence of reduced device sizes on the band dispersion and the bandgap values, which points towards the need for a careful fitting of parameters such as effective masses to non-bulk device bandstructures.

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Multi-Subband Monte Carlo Simulation of Oxide Thickness Fluctuation on SGSOI MOSFETs

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1. Abstract

The oxide thickness fluctuation (OTF) is an important source of variability in the fabrication of MOSFETs devices due to the scaling of the transistors [1,2]. In this paper we study the influence of the OTF impact on a Single Gate Silicon on Insulator (SGSOI) MOSFET when a random fluctuation is introduced in the HfO_2/SiO_2 interface.

2. Benchmark Devices

In this work we have analysed the effect of the oxide thickness fluctuations for a 32 nm gate length SGSOI MOSFET. The length of the source and drain regions is 60 nm and they are uniformly doped with $N_D = 5 \times 10^{19}$ cm^{-3}. The channel thickness is 6 nm and it is lightly doped with $N_A = 1.2 \times 10^{15}$ cm^{-3}. The top oxide is formed by a stack of 4.12 nm of HfO_2 and 0.7 nm of SiO_2 (EOT=1.4 nm). The value of the buried oxide thickness is 10 nm.

The HfO_2/SiO_2 interface was modified considering a random fluctuation of the HfO_2 position which penetrates into the SiO_2 interface. This penetration produces an oxide thickness fluctuation of ±3.5 Å.

In order to compare the effects of the silicon oxide fluctuations we have simulated two different configurations without roughness. The first one without penetration of the HfO_2 into the oxide silicon and the second one with a homogeneous penetration of the HfO_2 of 3.5 Å, such as is shown in Fig.1. These two configurations were considered as the limit cases of the roughness in the interface between the two oxides.

The necessary simulations to perform this study were carried out with a Multi-Subband Monte Carlo simulator [3].

3. Simulation Results

Fig.2 shows the potential distribution in the SGSOI MOSFET without OTF when $V_D = V_G = 1V$. The potential difference between this case and a SGSOI MOSFET with random penetrations of the HfO_2 is depicted in Fig.3. In this figure we can observe higher values of the potential in the SiO_2 region as a consequence of the higher electronic permittivity of the HfO_2 introduced in the SiO_2. Consequently, the potential of the channel is decreased, in the region close to the gate oxide, as an electrostatic response of the higher oxide potential.

The influence of the OTF over the drain current is shown in Fig. 4 and Fig. 5. These figures show four different configurations, with and without OTF. Simulations with OTF (OTF1 and OTF2) have different random interfaces with several HfO_2 elements penetrating 3.5 Å into the SiO_2. These elements were placed in random locations of the oxide interface. Simulations without OTF consider homogeneous interfaces with different oxide thicknesses 0.7 and 0.35 nm for SiO_2, and 4.12 and 4.47 nm for HfO_2 respectively. Fig. 4 shows the drain current behaviour versus the gate voltage for different configurations of the oxide interface when $V_D = 1$ V. This figure shows the results of OTF simulations are very similar to the simulation without OTF with an equivalent HfO_2 penetration of 3.5 Å. The same behaviour is obtained for I_D & V_{DS} when $V_G = 1$ V. Both figures seem to show a better performance of the drain current when the top SiO_2 layer is thinner.

4. Conclusions

In this work we have analysed the impact of oxide thickness fluctuations (OTF) in the HfO_2/SiO_2 interface of a SGSOI using a Multisubband Monte Carlo simulator. The OTF interfaces take into account a 3.5 Å penetration placed in random locations of the HfO_2/SiO_2 interface. Simulation results show the considered interfaces with OTF can affect the drain current performance, obtaining a very similar behaviour to a homogeneous interface with an equivalent HfO_2 penetration. These results have to be studied with more detail in a future work, considering more realistic data of the HfO_2 penetration into the SiO_2 layer and comparing with experimental results.

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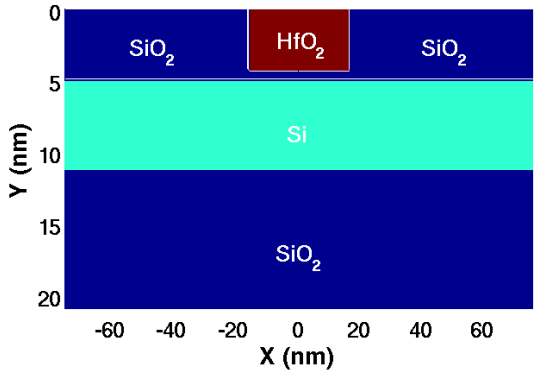

Fig.1: *Representation of the SGSOI MOSFET structure. The random HfO_2 fluctuation was simulated as a 3.5 Å penetration into the top SiO_2.*

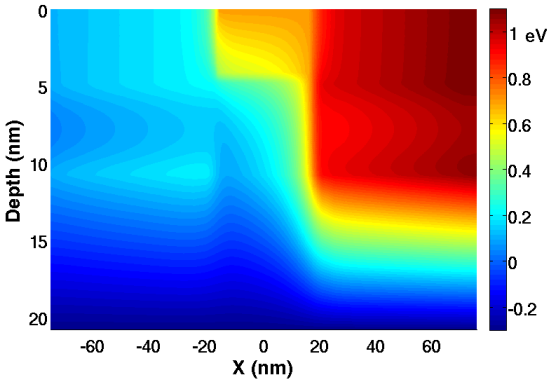

Fig.2: *Potential distribution of the SGSOI MOSFET with a homogeneous interface between the HfO_2 and SiO_2. The values of the oxide thickness for the HfO_2 and SiO_2 are 4.2 nm and 0.7 nm respectively. $V_D = V_G = 1V$.*

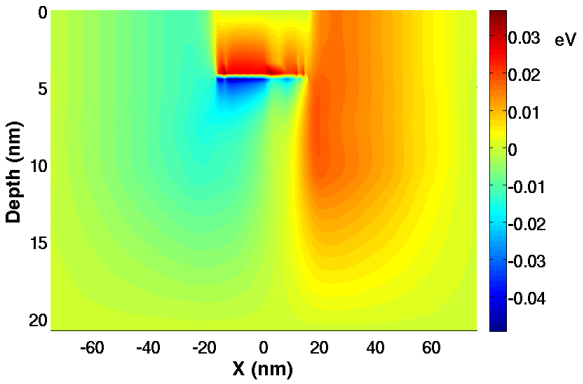

Fig.3: *Distribution of difference between the potential of the SGSOI MOSFET without OTF and with OTF. The values of the oxide thickness for the HfO_2 and SiO_2 are 4.2 nm and 0.7 nm respectively. $V_D = V_G = 1V$.*

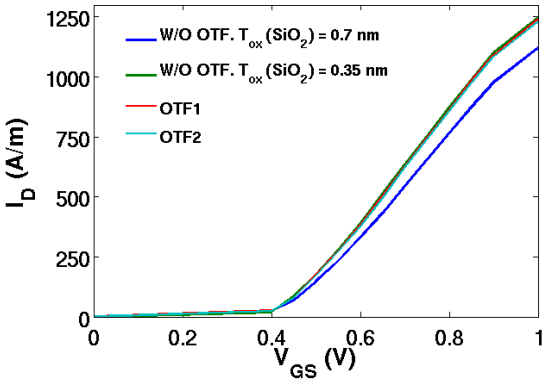

Fig.4: *I_D & V_{GS} curves for a SGSOI with $V_D = 1$ V and with different configurations of the oxide interface. OTF1 and OTF2 depict the influence of random oxide thickness fluctuations for the SiO_2 thickness between 0.35 and 0.7 nm.*

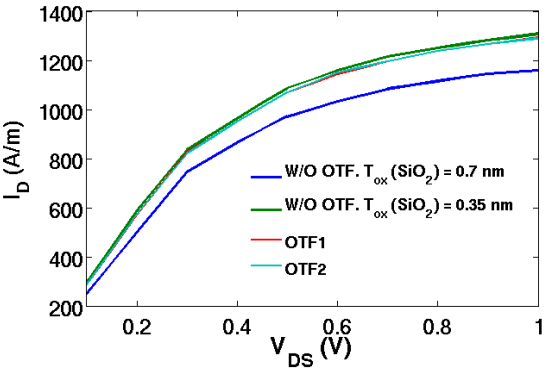

Fig.5: *I_D & V_{DS} curves for a SGSOI with $V_G = 1$ V and with different configurations of the oxide interface. OTF1 and OTF2 depict the influence of random oxide thickness fluctuations for the SiO_2 thickness between 0.35 and 0.7 nm.*

Universal relationship between substrate current and history effect in SOI MOSFETs and its importance for physical compact modeling

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1. Abstract

A surface-potential-based SOI-MOSFET model capable of reproducing dynamic history effects [1-2] as well as dc floating-body kinks is presented. The history effect is modelled by using essentially the same idea as that used for modelling of non-quasistatic (NQS) effects. The relaxation time required therein is derived from a recently found device-size-independent universal relationship between the dc steady-state substrate current I_{sub} and the drain-current relaxation time of floating-body devices in response to a voltage pulse.

2. Modelling of dc floating-body effect

Accurate modeling of the dc floating-body effects [3-6] is a prerequisite for modeling of the history effect. The kinks that appear in dc I_d-V_{ds} curves are caused mainly by accumulation of holes generated by impact ionization taking place near the drain. Let Q_h be the charge thus accumulating in the floating body. Our compact model, HiSIM-SOI, adopts a surface-potential-based formulation and iteratively solves the Poisson equation for three surface potentials at the source and the drain ends [5]. To model the dc floating-body effect appropriately, Q_h must be included in the Poisson equation. HiSIM-SOI relates I_{sub} with Q_h by determining the body-source junction voltage ΔV_{bs} (Fig. 1) with Eq. (1) shown on the next page, obtained by solving for the diode current together with the I_{sub} current. Fig. 2 shows that the Q_h-I_{sub} characteristics from HiSIM-SOI agree well with those from 2D device simulation.

3. Modelling of dynamic history effect

We are now in a position to model the dynamic behavior of Q_h. Looking back at the equivalent circuit in Fig. 1, it is reminiscent of a model for NQS effects in MOSFETs. We, therefore, choose to model the history effect using essentially the same formulation as that for the NQS model in HiSIM2 [8]. The transient $Q_h(t)$ is thus calculated with Eq. (2) on next page. The relaxation time constant t_d in Eq. (2) could be estimated by looking at the responses of a device to wide input pulses. Some measurement results are shown in Fig. 3. While the measured t_d depends on L/W, it turns out that $t_d = q_1 I_{sub}^{-1}$ holds independent of L/W, as shown in Fig.4 [7], with q_1 being a constant. This universal relationship motivates us to assume that I_{sub}-based universal modeling of the history effect is also possible. We apply the universal relationship to determine t_d in Eq. (2), with q_1 left as a fitting parameter to secure fitting capability. As shown in Fig. 5, HiSIM-SOI successfully reproduced the pulsed-V_g measurement of Fig. 3(a) for a wide variety of bias conditions. Fig. 6 shows that the sweep-rate-dependent I_d-V_{ds} curves are also well reproduced. Transient simulation results in Fig. 7 show that the device reaches a switching steady state at different rates depending on the width and cycle of the applied pulses, as it should.

4. Conclusions

We have demonstrated that the dc steady-state substrate current I_{sub}, which would flow in a body-tied device, can be used to model dynamic history effects as well as dc I_d-V_{ds} kinks of a floating-body device. The successful history effect modelling was made possible by a recently found device-size-independent universal relationship between I_{sub} and the relaxation time t_d of floating-body devices in response to a voltage pulse [7].

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Table 1: Equations used in HiSIM-SOI.

Body-source junction voltage

$$\Delta V_{\rm bs} = \mathbf{PARAM} \cdot \frac{kT}{q} \cdot \ln\left[1 + \frac{I_{\rm sub} L_{\rm p} L_{\rm n}}{q t_{\rm Si} W_{\rm eff}^{*} e^{-qV_{\rm bi}/(kT)} (D_{\rm n} n_{\rm n0} L_{\rm p} + D_{\rm n} p_{\rm p0} L_{\rm n})}\right] \quad (1)$$

PARAM: model parameter
$L_{\rm n}$: electron diffusion length
$L_{\rm p}$: hole diffusion length
$D_{\rm n}$: electron diffusion coefficient
$D_{\rm p}$: hole diffusion coefficient
$V_{\rm bi}$: body-source junction built-in potential
$t_{\rm Si}$: Si film thickness
$W_{\rm eff}$: effective channel width
$n_{\rm n0}$: equilibrium electron density in source
$p_{\rm p0}$: equilibrium hole density in body

Incremental change in transient $Q_{\rm h}$

$$Q_{\rm h}(t_i) = Q_{\rm h}(t_{i-1}) + \frac{\Delta t}{\Delta t + t_{\rm d}} [Q_{\rm h,dc}(t_i) - Q_{\rm h}(t_{i-1})] \quad (2)$$

$\Delta t = t_i - t_{i-1}$: time step
$t_{\rm d}$: relaxation time for $Q_{\rm h}$
$Q_{\rm h,dc}(t_i)$: dc steady-state value of $Q_{\rm h}$ under biases at t_i

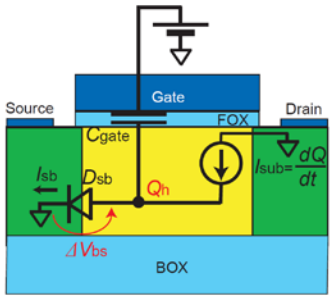

Fig.1: *An equivalent circuit representation of the relation between the accumulated charge $Q_{\rm h}$ and the substrate current $I_{\rm sub}$.*

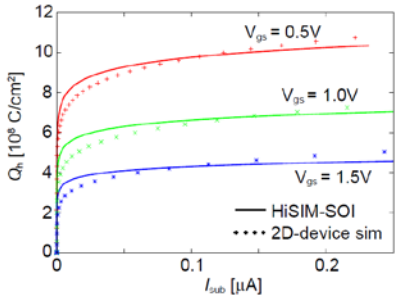

Fig.2: *$Q_{\rm h}$ in a floating-body device versus substrate current $I_{\rm sub}$ in a body-tied device. $t_{\rm ox}$ = 2.5 nm, $t_{\rm Si}$ = 50 nm, $t_{\rm box}$ = 110 nm, L = 1 μm, W = 1 μm.*

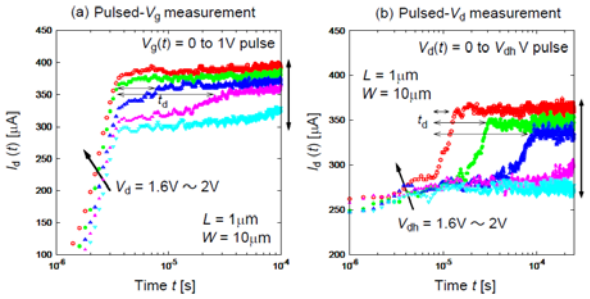

Fig.3: *(a) Measured transient response of $I_{\rm d}$ to a voltage pulse applied to the gate under different values of $V_{\rm d}$. The pulse height is 1 V. $I_{\rm d}$ reaches a steady state after $t_{\rm d}$. The rise time of the input pulse is 4 μs and the pulse width is long enough (200 ms) for reaching a steady state. (b) When a pulse is applied to the drain.*

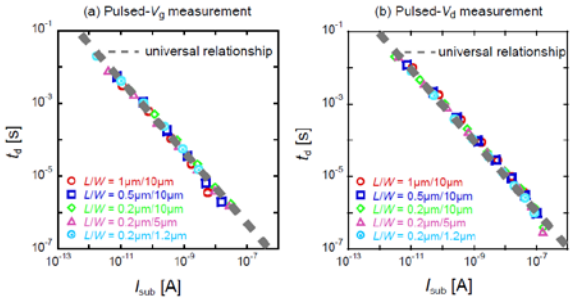

Fig.4: *(a) Measured relationship between the $t_{\rm d}$ of floating-body devices and the $I_{\rm sub}$ of body-tied devices when a pulse is applied to the gate. (b) When a pulse is applied to the drain.*

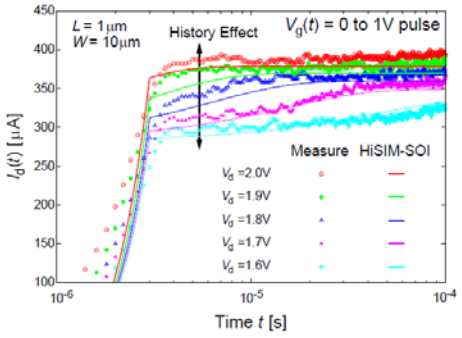

Fig.5: *Transient simulation results with HiSIM-SOI reproducing the measurement date in Fig. 3(a).*

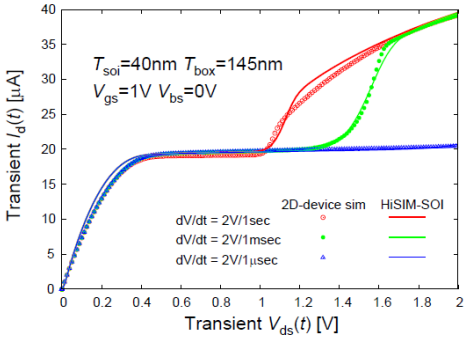

Fig.6: *Sweep-rate-dependent $I_{\rm d}$-$V_{\rm ds}$ curves.*

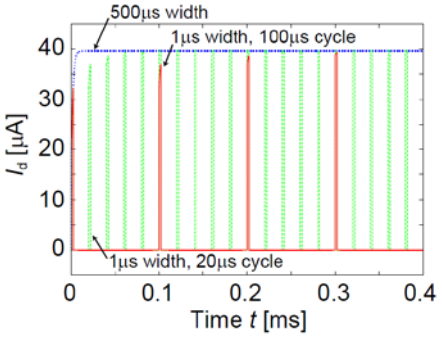

Fig.7: *Transient simulation results showing history effects when pulses with different widths and cycles are applied to the drain. $V_{\rm gs}$ = 1 V. $V_{\rm ds}$ = 2 V (pulse height).*

Session 5: Device Physics

Chair: Sigfried Mantl

Confinement-Induced Mobility Increase in p-type [110] and [111] Silicon Nanowires

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1. Abstract

The $sp^3d^5s^*$-spin-orbit-coupled (SO) atomistic tight-binding (TB) model is coupled to Boltzmann transport formalism for calculation of the low-field mobility in Si nanowires (NWs). We show that the phonon limited mobility of p-type NWs in the [110] and [111] transport orientations largely increases by more than 7X as the diameter is scaled from D=12nm down to D=3nm. This effect is attributed to dispersion modifications due to confinement that largely improve the carrier velocities and reduce scattering rates in these type of NWs.

2. Approach

Silicon NWs have recently attracted significant attention as candidates for high performance transistor channels. NW devices with channel lengths down to L_G=15nm and diameters down to D=3nm have already been demonstrated [1, 2].

Low-dimensional materials offer the capability of improved performance due to additional degrees of freedom in engineering their properties: i) the cross section size, ii) the transport orientation, iii) the orientation of the confining surfaces.

We calculate the phonon-limited mobility of p-type Si NWs using the $sp^3d^5s^*$-SO TB model for the electronic structure [3], and Boltzmann theory for transport [4, 5], for NWs up to 12nm in diameter (~5500 atoms in the unit cell). The conductivity is evaluated from:

$$\sigma = q_0^2 \int_{E_0}^{\infty} dE \left(-\frac{\partial f_0}{\partial E} \right) \Xi(E) \qquad (1),$$

where $\Xi(E)$ is defined as:

$$\Xi(E) = \sum_{k_x,n} v_n^2(k_x)\,\tau_n(k_x)\,\delta\left(E - E_n(k_x)\right) \qquad (2).$$

Here $v_n(k_x)$ is the bandstructure velocity and $\tau_n(k_x)$ is the momentum relaxation time for a hole with momentum k_x in subband n. The mobility is defined as:

$$\mu_p = \frac{\sigma}{q_0 p} \qquad (3),$$

where p is the hole concentration in the channel.

3. Results

Figure 1 shows the heavy-hole energy surface of bulk silicon. Confinement in the [110] direction will produce channels with light subbands picked alone the 45° lines in the figure. In a (110) ultra-thin-body (UTB) channel, this will result in lighter subbands in the [110] direction as the confinement increases. This is shown in Fig. 2a and 2b for this (110) UTB channel for body thicknesses W=3nm and W=15nm, respectively. In a NW, this effect will also result in lighter subbands with confinement, as shown in Fig. 3a and 3b for cylindrical [110] p-type NWs of D=3nm and D=12nm respectively.

The increase in the dispersions' curvature with confinement will result in increased carrier velocities and conductivity in the NWs. Figure 4 shows the carrier velocity in the p-type [110] (triangle-red) and [111] (circle-green) NWs. As the diameter decreases from D=12nm down to D=3nm, a ~2X increase in the velocity is observed. Figure 5 shows the conductivity in these NWs as a function of the carrier concentration for D=12nm (dotted) and D=3nm (solid). The conductivity largely increases for smaller diameters. This increase reflects in the mobility of the NWs as a function of the diameter as shown in Fig. 6. Here the mobility increases by 9X and 7X for the [110] and [111] NWs respectively as the diameter scales. We mention that only phonon scattering is considered in the calculations. Surface roughness scattering can change the results for very small diameters, but even so, mobility improvements with confinement can still be achieved [5].

4. Conclusions

The $sp^3d^5s^*$-SO atomistic tight-binding model is coupled to linearized Boltzmann transport for the calculation of mobility in silicon NWs. We show that the phonon-limited low-field mobility in p-type [110] and [111] NWs increases by 9X and 7X, respectively, as the diameter is reduced from D=12nm down to D=3nm.

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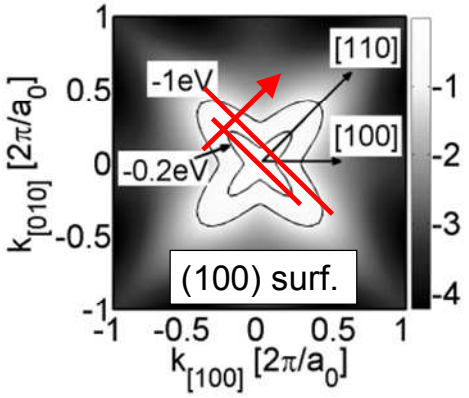

Fig.1: *The Si bulk (100) energy surface. The 45° inclined lines show the relevant energy regions for devices with physical surface confinement along the direction of the red arrow.*

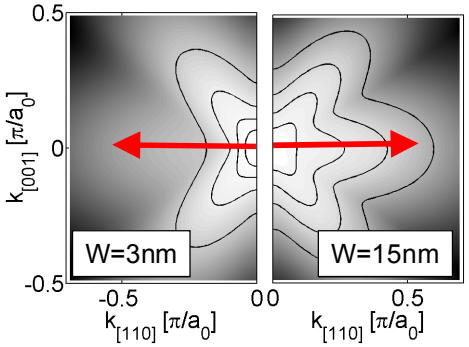

Fig.2: *The energy surfaces of (110) UTB layers for different thicknesses (W).Left:W=3nm. Right: W=15nm.The subbands are lighter in [110] (arrow) for the thinner body channel (the energy contours point towards the center).*

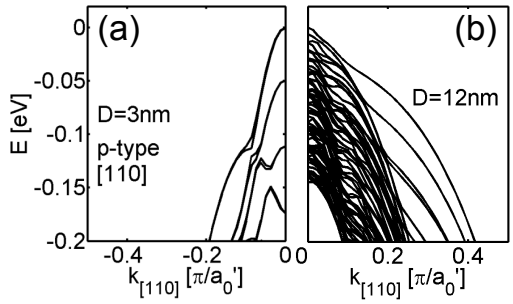

Fig.2: *Dispersions of p-type [110] NWs of diameters D=3nm (left) and D=12nm (right).*

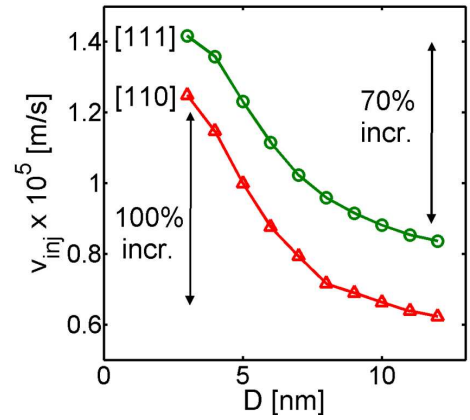

Fig.2: *The carrier velocities of p-type NWs in [110] (triangle-red) and [111] (circle-green) transport orientations vs. diameter under non-degenerate conditions.*

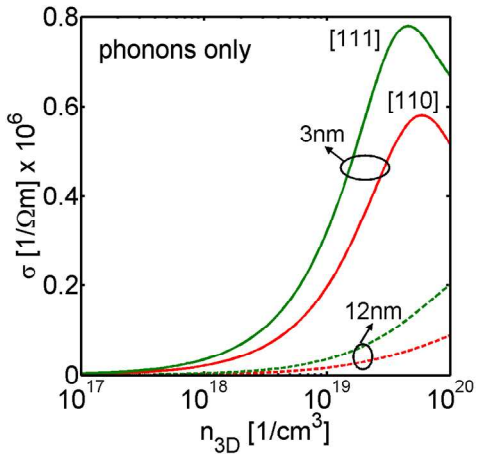

Fig.2: *The conductivity of p-type NWs in [110] (red) and [111] (green) transport orientations vs. the carrier concentration. Solid lines: D=3nm. Dashed lines: D=12nm.*

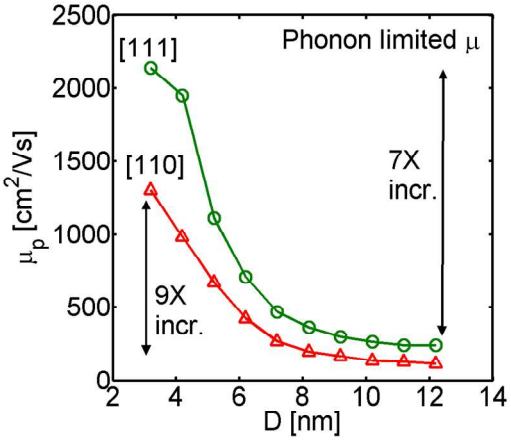

Fig.2: *Phonon-limited mobility for p-type NWs in [110] (triangle-red) and [111] (circle-green) transport orientations as a function of the NWs' diameter. Large increases are observed with diameter scaling.*

Transport mass of holes in ultra-thin DGSOI devices

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1. Abstract

We study ultra-thin p-channel double-gate silicon-on-insulator devices employing a self-consistent simulator based on the six-band ***k·p*** model. Transport properties of such devices are analyzed for different surface and channel orientations; bandstructure effects can be significantly summarized by the effective transport mass, provided that a proper averaging is performed.

2. Introduction

Improvement of carrier mobility, especially in the case of holes, is one of the fundamental goals of present research, with the aim of guaranteeing the performance of electronic devices within the scaling roadmap. In this perspective, it has been found that in devices fabricated on (111) or (011) surfaces, hole mobility is larger than on the usual (001) one [1], [2]. On the other hand, device scaling also requires a strong control of short channel effects, and this can be achieved through the use of silicon-on-insulator (SOI) devices and multiple gates. The aim of this paper is to study hole properties in ultra-thin SOI devices with symmetric double gate (DG) structures and to compare the properties obtained when different surface orientations and channel directions are considered. To this end, we employ a self-consistent simulator [3] based on the 6-band ***k·p*** method [4] for bandstructure calculation and the Kubo-Greenwood formula to compute hole mobility [5].

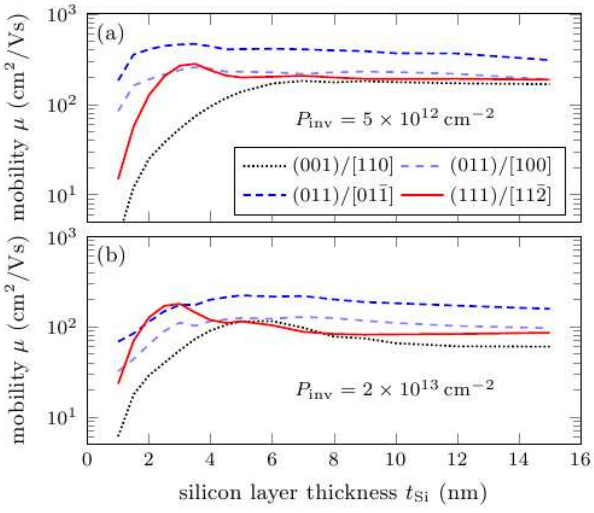

Fig.1: *Hole mobility as a function of t_{Si} for different surface and channel orientations.*

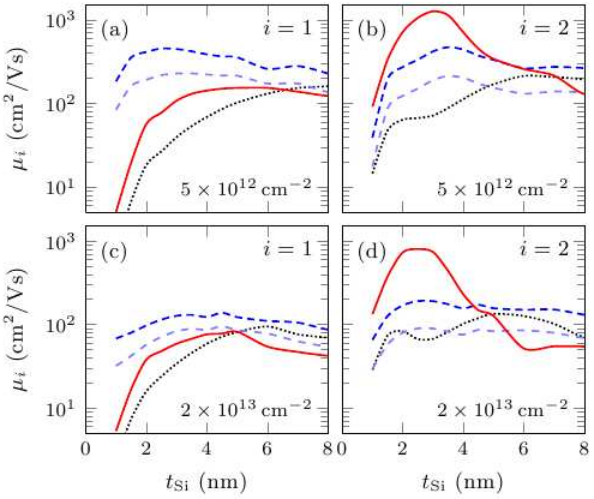

Fig.2: *Mobility of holes in the first and second subbands. Line types and colors represent surface and channel orientations as in Figure 1.*

3. Results

We consider DG SOI structures with silicon layer thicknesses, t_{Si}, ranging from 1 to 15 nm; the channel is essentially undoped ($N_D=10^{14}$ cm^{-3}), the thickness of both oxide layers is t_{ox}=1 nm, and a midgap metal is considered as gate material. Hole mobility, μ, is computed by Kubo-Greenwood formula [5], employing the subband dispersion and wavefunctions obtained with the band ***k·p*** model, taking into account phonon (optical and acoustic) and surface roughness (SR) scattering mechanisms [6].The dependence of hole mobility on t_{Si} is shown in Figure 1, for different values of inversion carrier density P_{inv}. We only represent one curve for (001) and (111) surface orientations, because in these cases μ shows a very small dependence (up to 1–2%) on channel orientation. On the contrary, a large mobility difference is observed between different channel orientations for (011) devices. It is clear that for very thin channels μ is always strongly reduced; however, it is important to emphasize that there are large quantitative differences between curves corresponding to different surface and channel orientations. The most important observation is that hole mobility is severely degraded for (001) devices below 6nm, while this happens at smaller values of t_{Si} for (011) and (111) devices. Therefore, the mobility enhancement of alternative orientations not only persists for ultra-thin devices; on the contrary, it increases and can be quite large, especially at small values of P_{inv}. To study the

origin of such enhancement we separate the mobility of the first two subbands, as shown in Figure 2. The important mobility decrease can be attributed to the increase of both phonon and SR scattering at small Si thicknesses; however the different behavior corresponding to different surface orientations cannot be explained by differences in the scattering rates. The effective transport mass m_i^{α} is defined as:

$$\frac{1}{m_i^{\alpha}(k)} = \frac{1}{\hbar^2}\frac{\partial^2 E_i(k)}{\partial k_{\alpha}^2}$$

where $E_i(k)$ is the energy of i-th subband as a function of momentum k, and k_α is the momentum component in the transport direction α. As we can see in Figure 3, m_i^{α} varies heavily as a function of k, and the value at k=0 [7,8] cannot be taken as a single value to summarize transport properties. We define an average effective transport mass M_i^{α} by:

$$\frac{1}{M_i^{\alpha}} = \int \frac{f(E_i(k))}{m_i^{\alpha}(k)}\,\mathrm{d}k \Big/ \int f(E_i(k))\mathrm{d}k$$

where $f(E)$ is the Fermi-Dirac distribution. Figure 4 shows $m_1^{\alpha}(0)$ and M_1^{α} as functions of t_{Si}; while the former has a weak dependence on t_{Si} for all orientations, the latter shows a strong decrease at small t_{Si} for (011) surface orientation, especially for [01-1] direction.

This fact compensates, to a certain extent, the large increase of scattering rates (both phonon and SR ones) occurring at very small thicknesses, giving rise to the mobility behavior shown in Figures 1 and 2. Such a decrease of M_1^{α} is not caused by a corresponding decrease in $m_1^{\alpha}(0)$ but, as we can see in Figures 3(c), (d), and (e), by a flattening of the surface of $m_1^{\alpha}(k)$.

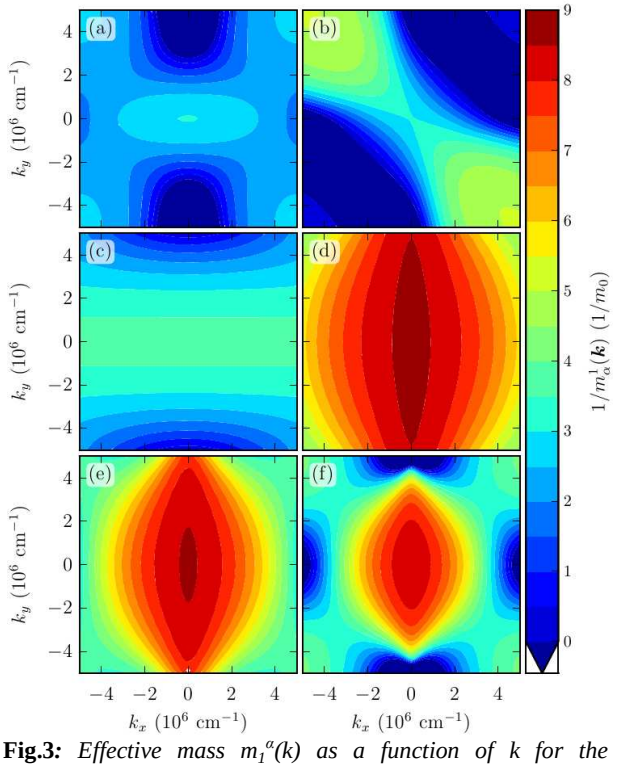

Fig.3: *Effective mass $m_1^{\alpha}(k)$ as a function of k for the following devices: t_{Si}=2nm with (001) surface orientation and k_α parallel to [100] (a), (001)/[110] (b), (011)/[100] (c), (011)/[01-1] (d); (e) and (f) are the same as (d) but with t_{Si}= 3nm and 5nm, respectively. For (001) orientation k_x and k_y are directed along [100] and [010], while for (011) orientation they are directed along [100] and [01-1].*

4. Conclusions

We studied the effect of surface and channel orientations on hole mobility in ultra-thin double gate structures. The largest mobility is observed for (011) surface orientation and [011] channel direction, in almost the whole range of silicon layer thicknesses and inversion densities considered; moreover, the enhancement with respect to the classic (001)/[110] case is larger for ultra-thin devices than thick or bulk ones. Mobility was shown to be related to a properly averaged value of the effective transport mass, rather than to its value at k=0.

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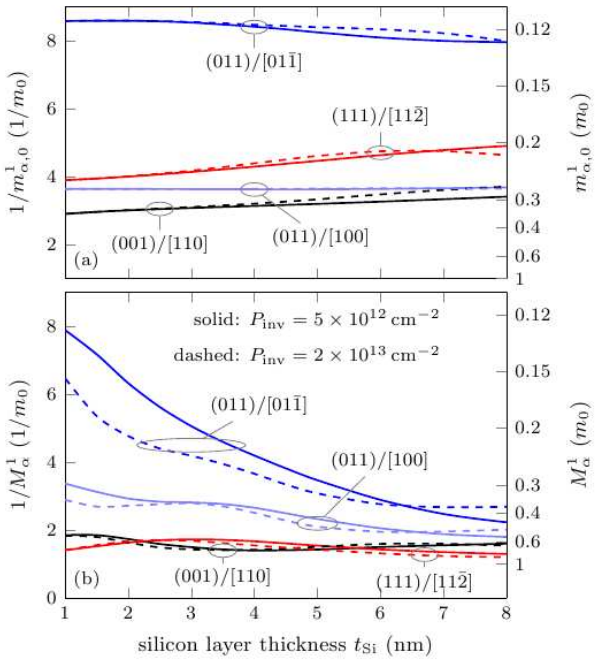

Fig.4: *Effective masses m_1^{α} and M_1^{α} as a function of t_{Si}.*

Electron-Hole Bi-Layers in Ultra-Thin SOI-Devices

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1. Abstract

We have investigated the properties of an electron-hole bi-layer in a double gate SOIFET with a 22 nm-thick channel. We have measured the drag resistance as a function of temperature and carrier density. We have also observed activated hysteretic behaviour in electron and hole currents in certain temperature and carrier density ranges.

2. Introduction

Electron-hole bi-layers provide an interesting system for investigation of interactions between two carrier distributions, one example being drag resistance between the two carrier systems. These effects have been investigated in III-V devices [1] and in silicon-on-insulator (SOI) devices [2]. The high dielectric strength of silicon dioxide in double gate SOI devices allows for a high asymmetric electric field that can overcome the energy gap of Si, facilitating the formation of 2D electron and hole gases simultaneously inside the thin Si channel. With the double gate geometry the densities, distributions and location of carrier gases can be tuned to investigate the interactions in a very wide parameter window. Here we report on fabrication of double gate SOI devices. We have measured e-h drag resistance as a function of temperature and carrier density. Also, we have found interesting bistable behaviour in a coupled e-h system.

3. Experimental

The SOI devices were fabricated on commercially available bonded SOI wafers. The fabrication follows closely the process for the n-type double gate FETs described in Ref. [3]. The major difference in comparison with standard n-type FET is that instead of having only n^+ contacts the present devices also have p^+ contact regions, which provide galvanic contact to the hole gas inside the 22-nm-thick Si well. Figure 1 shows an optical micrograph of the Hall bar device explored in this work. The bistability effect was investigated in cross-bar device geometry with the effective bi-layer area of 1.4x1.4 μm^2. The devices were characterised at room and low temperatures at balanced bias conditions where the electron and hole concentrations in the channel are equal.

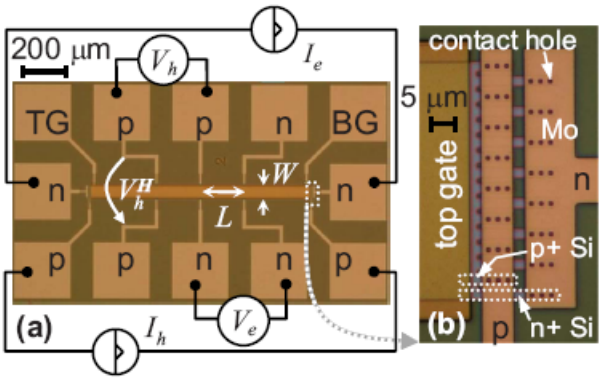

Fig.1: *Optical micrograph of a Hall bar device used in the drag resistance measurements. The left panel shows a magnification of the p+/n+ contacts to the channel.*

4. Results

In Figure 2 is shown the drag sheet resistance as a function of carrier density and temperature. The measurements are carried out at balanced charge densities, n_e=n_h. The drag resistance decreases as a function of carrier density at any temperature. In the intermediate temperature range and at high carrier densities the dependence follows the T^2 dependence, as expected for Coulomb drag in systems of low disorder.

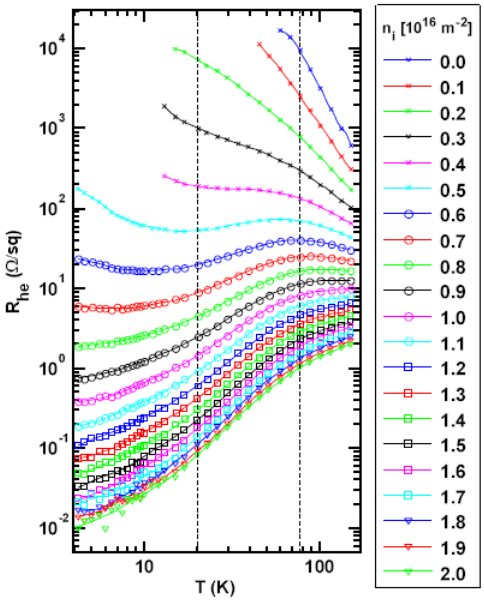

Fig.2: *E-H drag sheet resistance as a function of temperature at various carrier densities, n_e=n_h.*

At temperatures below 110 K the bi-layer showed interesting bistable behaviour at certain carrier densities. The effect is reproducible and thermally activated. An example of the bistability is shown in Figure 3.

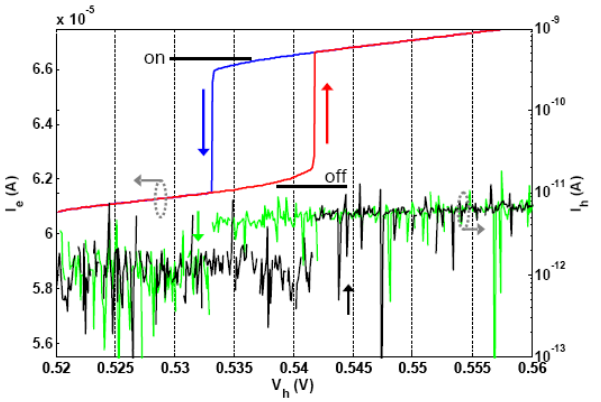

Fig.3: *Electron and hole layer currents as a function of hole layer gating bias (Note the current scales). Up and down arrows indicate the sweeping direction. T=77 K.*

5. Conclusions

By providing a highly asymmetric gate bias in a double gate SOIFET, both electron and hole gases can exist simultaneously in the Si channel. In this configuration the interaction between 2D electron and hole gases can be investigated. The measured e-h drag resistance shows Coulombic behaviour in the intermediate temperature range of 20-80 K when the electron and hole layers are in "metallic" regime. At low temperatures and low carrier densities also other coupling processes start to play a role. Below 100 K a reproducible bistable effect emerges. The origin of this effect needs further investigation.

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Dispersion of Confined Acoustic Phonons in Ultra-Thin Silicon Membranes.

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1. Abstract

The acoustic phonon dispersion curves of ~10 and ~30 nm Si membranes were measured using Brillouin Light Scattering (BLS) spectroscopy. The dispersion relations of the confined phonons were calculated from a semi-analytical model based on continuum elasticity theory. Green's function simulations were used to simulate both the phonon density of states and Brillouin spectra of the membranes. The effect of the native oxide layer was also considered, and found to affect significantly the dispersion of the higher order modes.

2. Motivation

The acoustic properties of ultra-thin Si layers are important for many areas of nanofabrication, impacting on both structural integrity and thermal transport. The effect of phonon confinement is particularly important, affecting both heat dissipation and charge carrier mobility [1]. The goal of this work is to obtain a deeper understanding of phonon confinement and propagation in materials with dimensions comparable to thermal phonon wavelengths. Previous studies have investigated confined acoustic phonons in 30 nm Si membranes by inelastic light scattering at normal incidence, with use of a triple grating Raman spectrometer [2,3]. In this work the in-plane propagation of these modes is investigated as a function of the parallel component of the wavevector, using a high-resolution Tandem Fabry-Perot Interferometer. The effect of the ~1 nm native oxide layer in such thin systems was also calculated using a three-layer model.

3. Methods

Brillouin Light Scattering (BLS) spectroscopy is an inelastic light scattering technique, which can directly measure acoustic phonon dispersion in a non-destructive manner. Using an angle-resolved approach, out-of-plane confined phonons as well as flexural, dilatational, and shear modes propagating in the plane of the membrane were investigated. The dispersion curves were calculated from numerical solutions to the analytic equations for the acoustic modes in a membrane, based on a continuum elasticity model [4]. Green's function simulations were also used to calculate the density of states of the phonon modes and to simulate the Brillouin spectra [5]. The membranes of area 500 x 500 □m2 were fabricated on nominally undoped 150 mm thin SOI wafers using Si MEMS processing techniques. The thin SOI wafers were produced by bonding the standard SOI wafers from SOITEC company [5] with a Si oxidized wafers.

4. Results

The BLS spectra of the membranes corresponded to calculated thicknesses of 12 and 28 nm. Calculations for the 12 nm membrane showed that mode frequencies exhibit a detectable shift of 8% with changes in the thickness of the membrane of 1 nm, which is of the order of the uncertainty in the thickness measurement (Figure 2) The ultra-thin nature of the membranes resulted in a slow phase and group velocity for the first order flexural (A0) modes, with a phase velocity down to 320 m s^{-1} recorded for the 12 nm membrane. This is 15 times smaller than the comparable bulk value (Rayleigh Wave) v_{RSAW} = 4921 m s^{-1}. This resulted in a large phonon density of states, as evidenced by an enhanced acousto-optic interaction and therefore a strong scattered signal. It was observed that the experimental data agree with the dispersion curves

calculated from continuum elasticity theory to within experimental error, apart from the dilatational mode of the 12 nm membrane (Figure1), which is under further investigation.

Calculations for a three layer system were also performed to take account of the native oxide layer, which was found to cause a detectable change in the dispersion of the higher order (n>0) acoustic modes. (Figure 3)

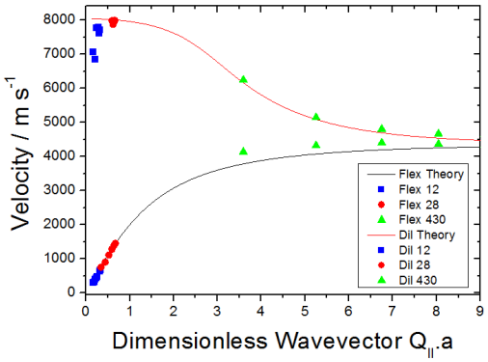

Fig. 1: *Phase velocity vs. dimensionless parallel wavevector for 12 nm (blue squares), 28 nm (red circles) and 430 nm (green triangles) membranes, with theoretical calculations for the first order flexural (black line) and dilatational (red line) modes of a Si membrane.*

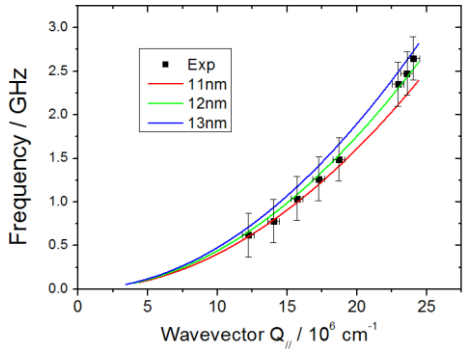

Fig. 2: *Experimental data for the 12 nm membrane and calculations of the first order flexural mode for different thicknesses. The measurements are sensitive to changes in thickness on the order of 1 nm.*

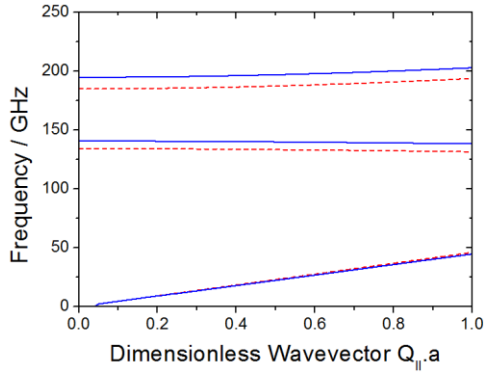

Fig.3: *Dispersion curves of the dilatational modes of a 30 nm Si membrane, (blue solid line) and 28.4nm Si with 1.6 nm SiO_2 on the top and bottom surfaces (red dashed line).*

5. Conclusions

The acoustic dispersion relations of confined phonons in ultra-thin Si membranes, with thicknesses of 12 and 28 nm, were measured. The experimental results were compared with semi-analytic and Green's function calculations with satisfactory agreement, confirming a small phase and group velocity for the first order flexural mode. Calculations show that the spectra are sensitive to changes in thickness of the membrane on the order of 1 nm. The higher order acoustic modes were also shown to be sensitive to the presence of the thin native oxide layer. This work provides a basis to investigate the effect of acoustic phonon confinement on thermal transport in systems with sub- 50 nm dimensions.

6. Acknowledgements

The authors are grateful for financial support from the FP7 projects ICT FET TAILPHOX (grant nr. 233883, NMP NAPANIL (grant nr. 214249) and the MICINN project ACPHIN (FIS2009-10150). J.C. gratefully acknowledges financial support under an Irish Research Council for Science, Engineering, and Technology (ICRSET) scholarship.

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Session 6: Advanced Simulation

Chair: Massimo V. Fischetti

Reaching sub-32nm nodes: SGSOI optimization

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1. Abstract

This work presents a MSB-EMC study of the impact of downscaling on V_{th} and DIBL for different configurations of sub-32nm SGSOI devices. The simulations show that the combination of Extremely-Thin BOX combined with ground plane is necessary in order to reach the 11nm node.

2. Introduction

The continuous efforts of the Semiconductor Industry in order to keep Moore's Law still valid, imply the search of new solutions to face the implementation of future technological nodes [1]. Bulk MOSFETs will be still the main actor for the 32nm node. However, as the channel length is reduced, short channel effects (SCEs) and variability problems arising from a highly doped channel make necessary the use of SOI devices. Among the different possibilities, Extremely-Thin (ET) single gate devices (SGSOI) and, multigate transistors (MuGFETs) will compete to substitute Bulk-based technology. This work presents a Monte Carlo study of different ETSOI devices including SGSOI and DGSOI transistors to explore the possibilities of such devices to be used for sub-32nm nodes.

3. Model and Calibration

The electrostatic and transport performance of the proposed devices have been analyzed with a Multi-Subband Ensemble Monte Carlo simulator (MSB-EMC). The code, presented elsewhere [2], has been successfully used in previous studies of SOI [2] and bulk devices [3]. The model considers the quantum problem decoupled from the transport plane. Therefore, the Schrödinger equation is solved in the confinement direction (Z) for each slice corresponding to the grid defined from source to drain (Fig. 1). The Boltzmann Transport Equation (BTE) is solved in the transport plane (XY) by the Monte Carlo method. Self-consistency is kept by solving Poisson's equation in the XZ plane. In this way, the evolution of the eigen-energies, $E_{i,\upsilon}(x)$, and the wave functions, $\zeta_{i,\upsilon}(x,z)$ are obtained along the transport axis, X, for the i-th valley and the υ-th subband. Non parabolic analytical conduction band is considered. Concerning scattering mechanisms, phonon, surface roughness and ionized impurities effects are included.

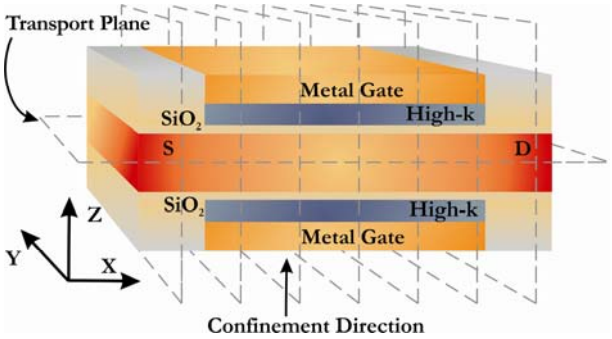

Fig.1: *Simulated structure for an ET-SGSOI with ground plane. 1D Schrödinger equation is solved for each grid point in the transport direction whereas Boltzmann Transport Equation is solved by the Monte Carlo method in the transport plane.*

The results obtained from the MSB-EMC code have been compared to those measured in [4] for a SGSOI with T_{Si}= 8nm, L_G= 33nm, Ultrathin-BOX (10 nm) and ground plane (GP). The gate stack is formed by TiN (10nm), HfO_2 (2.2 nm) and SiO_2 (1.6nm). I_D-V_{GS} curves for V_{DS}= 1.1V (red) and 100mV (blue) are shown in Figure 2. Our simulations (symbols) show a good agreement with experimental data (lines).

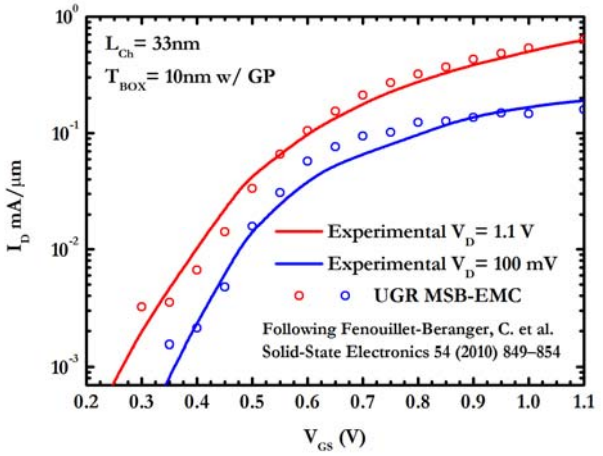

Fig.2: *I_D vs. V_{GS} curves for a 33nm SGSOI with ground plane. Experimental results from [4] (lines) are compared to the MSB-EMC simulator (symbols).*

4. SGSOI for sub-32nm nodes

As the channel length is reduced below 32nm, DIBL and V_{th} roll-off control demand a careful design of the device. A set of devices including different SGSOI and DGSOI have been compared to establish the impact of different device configurations on the aforementioned parameters. For SGSOI devices, channel lengths of 18 and 11nm with 6nm Si thickness have been considered. The gate stack structure includes midgap metal and HfO_2/SiO_2 dielectric bilayer giving an EOT= 2nm. Concerning the BOX, three configurations are studied; a standard thick BOX (145nm), an UT-BOX (10nm) and the same UT-BOX but including ground plane contact (GP). Source and drain regions are doped with $5\times10^{19}cm^{-3}$ with a Gaussian transition profile into the channel. For DGSOI devices, an identical structure than in the SGSOI case is considering but substituting the BOX by a gate stack identical than the previously described. The geometries have been chosen to obey one of the standard design rules for FDSOI, $L_{Gmin}\approx2T_{Si}$, and check for which of the BOX structures can be applied to the 11nm device. The impact of different BOX configurations on the drain current for SGSOI devices with L_G= 18nm is shown in Figure 3. As can be observed, the impact on the transfer characteristic highly depends on the BOX configuration. For the Thick BOX device the variation of the I_D-V_{GS} curves for low and high drain bias is too big. As a consequence, such configuration cannot be addressed for 18nm devices, even when the aspect ratio is high enough ($L_G=3T_{Si}$) following the standard recommendations for electrostatic integrity in SGSOI.

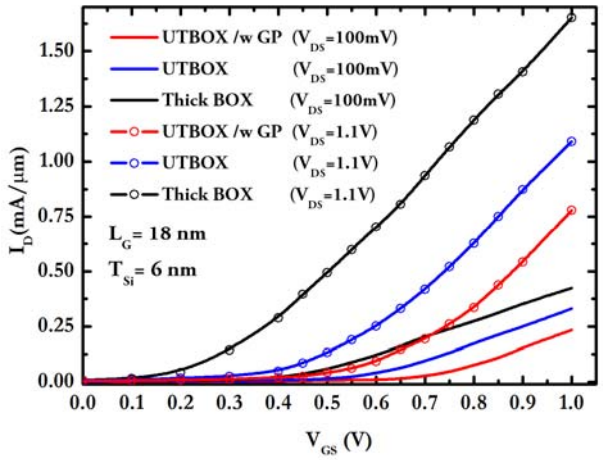

Fig.3: *Drain current curves for the 18 nm SGSOI devices calculated at V_{DS}=100 mV (solid line) and 1.1 V (solid with symbols).*

The V_{th} roll-off for each configuration when the channel length is reduced from 18 down to 11nm is presented in Table 1. Moderate variations are observed as the devices are scaled down, however, and thanks to the midgap metal gate, the threshold voltage remains in an acceptable range.

L_G (nm)	V_{th} (mV) @ V_D=100 mV			
	UTBOX GP	UTBOX	Thick BOX	DGSOI
18	700	600	420	500
11	580	520	400	440

Table.1: *V_{th} calculated at V_D=100 mV for the different configurations of SGSOI and DGSOI. For all the considered channel lengths, V_{th} remains in a reliable range.*

From the point of view of DIBL, defined at V_D=1.1V as DIBL≡($V_{th@100mV}-V_{th@1.1V}$)/ΔV_D, the behavior of each device is different. For the 18nm transistors, the simulations reveal that the use of UTBOX is mandatory. Even more, if the channel length is reduced to 11nm, UTBOX is not enough and must be combined with ground plane. In the case of DGSOI devices, the electrostatic integrity is kept. As a consequence, the standard design rule for FDSOI devices is not valid in general for sub-32nm nodes and specific rules must be redefined taking into account the BOX characteristics.

L_G (nm)	DIBL (mV/V) @ V_D=1.1V			
	UTBOX GP	UTBOX	Thick BOX	DGSOI
18	130	180	300	45
11	190	380	450	50

Table.2: *DIBL calculated at V_D=1.1V. In order to fabricate reliable transistors, UTBOX is mandatory for sub-32 nm nodes.*

4. Conclusions

This work presents a MSB-EMC study of electrostatic integrity for sub-32nm nodes. The simulations show that the main limiting factor for downscaling is the DIBL and UTBOX-GP configuration is the only valid to downscale SGSOI to 11nm keeping the standard aspect ratio design rules.

5. Acknowledges

This work has been supported by the EU (EUROSOI+ CA and NANOSIL) and the Spanish Government (FIS2008-05805, TEC2008-06758-C02-01) and Junta de Andalucía P09-TIC4873.

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3D Monte Carlo simulations of a 25 nm gate length SOI FinFET using unstructured tetrahedral grids

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1. Abstract

A parallel 3D Monte Carlo (MC)/Drift-Diffusion (DD) simulator designed to work on unstructured tetrahedral elements has been developed for the simulations of nano-MOSFETs. Quantum corrections are introduced using the density gradient approach. The simulator is applied to the simulation of a 25 nm gate length FinFET with a HfO_2 gate stack fabricated on a SOI substrate.

2. Introduction

Various novel thin-body architectures have been proposed to tackle the degradation in performance observed in the conventional, bulk 22 nm technology and beyond. FinFETs are among the strongest contenders to satisfy the requirements imposed by ITRS and continue the scaling. Accurate physical modelling of the carrier transport as well as a correct description of complex 3D geometry of these architectures is needed in order to predict their behaviour and optimise their design. Such physical modelling can be achieved via the ensemble Monte Carlo (MC) method. However, this technique is computationally very expensive for complex 3D geometries as shown in the example of Fig. 1 [1], [2]. Therefore, the use of efficient algorithms and parallel computing in order to save simulation time is imperative. The main computational burden is the self-consistent solution of the Poisson equation. Each iteration time step in self-consistent simulations depends on the geometry and doping of the device and it can be as small as 0.05 fs [3] leading to tens of thousands of iterations per bias point until the steady-state is reached. Therefore, there is a need for a 3D MC device simulator which uses an optimal mesh and can discretise the simulation domains using non-rectangular meshes. In this work, we describe such a 3D finite element MC simulator based on tetrahedral elements and present results of the simulations for a 25 nm gate length SOI FinFET designed following the guidelines in Ref. [4].

3. Simulation approach

The optimisation of device geometry details for the best performance but mostly the assessment of the suitability

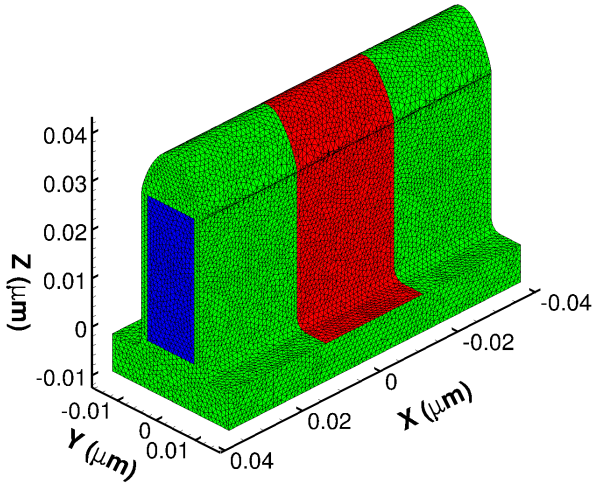

Fig.1: *Mesh of the simulated FinFET geometry with a fin height of 30 nm and width of 12 nm.*

of selected SOI FinFET candidates cannot be based exclusively on the evaluation of the performance of ideally fabricated devices. A proper study of the characteristics of particular design has also to assess variability including the resistance to random variability induced by intrinsic parameter fluctuations. In order to study statistical samples and, at the same time, maintain the predictive power of the simulations, trade-offs must be made between efficiency and accuracy. We have chosen the analytic nonparabolic anisotropic model for the dispersion relation in the valleys of the conduction band of silicon [5] which allows very efficient MC simulations while retaining much of its accuracy for expected values of supply voltages. Also, quantum corrections are used "frozen" taking the value of the quantum potential from DD simulations and adding it to the self-consistent electrostatic potential updated every 0.05 fs [6]. Finally, to obtain subthreshold characteristics, the results of the DD simulations are used, since they are free of the statistical noise present in the MC simulations and the transport in this region is well reproduced.

4. Simulation results

The simulated device, shown in Fig. 1, is a fully depleted 25 nm gate length FinFET which has a silicon

body with a height of 30 nm and a width of 12 nm [4]. Dimensions and shape of the oxide layer were modelled from data in [7]. The doping profile was defined analytically with constant values of 10^{20} cm^{-3} in the source and drain regions and background channel doping of 10^{17} cm^{-3}. Fig. 2 shows the I-V characteristics, in linear and logarithmic scales, using the DD and MC transport models. MC simulations were carried out using both self-consistent (SC) and frozen field (FF) approaches for the electrostatic potential. The quantum corrections were included in "frozen way" in the both cases. DD simulations naturally underestimate the drain current at high gate voltages. Both sets of MC simulations show a good agreement at low drain bias as expected but FF MC exhibits a "saturation behaviour" in the sub-threshold region while SC MC is still able to reproduce a very small current. Fig. 3 shows the average electron density at V_D=50mV and V_G=0.8V. Due to the increased oxide thickness on the top of the device, the most important transport channels are on the sides of the silicon body, producing effectively a double gate MOSFET behaviour.

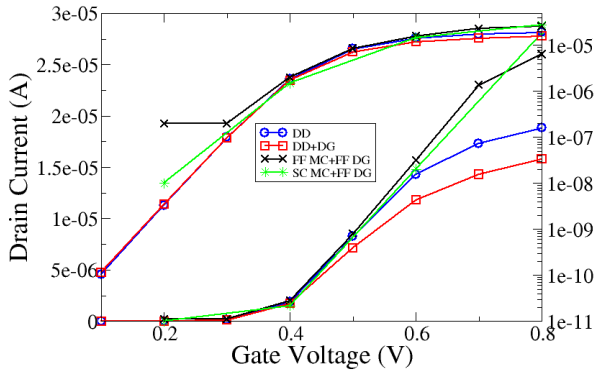

Fig. 2: *I_D-V_G characteristics at V_D=50mV of the simulated SOI FinFET using DD (circles), DD+DG (squares), FF MC + FF DG (crosses) and SC MC + FF DG (stars).*

4. Conclusions

We have presented some preliminary results of the simulation of a 25 nm gate length SOI FinFET using a 3D DD and MC device simulator based on the finite element method including quantum corrections through the density gradient model. Simulations with DD and MC transport models were compared at a low drain bias of 50 mV showing, as expected, a good agreement at low (bearing in mind difficulties with a noise in the MC at very small currents) and moderate gate biases. At large applied voltages even and the small drain volatge of 50 mV, the MC simulations will predict a large current due to the starting impact of non-eqilibrium carrier transport in these nanoscale transitors. We have proven that 3D finite element DD and MC simulation tools can successfully reproduce the comlex geometry of the 25 nm gate length SOI FinFET and that the tools can be applied to study the effects of fluctuations combining both transport models to increase the efficiency of the simulations.

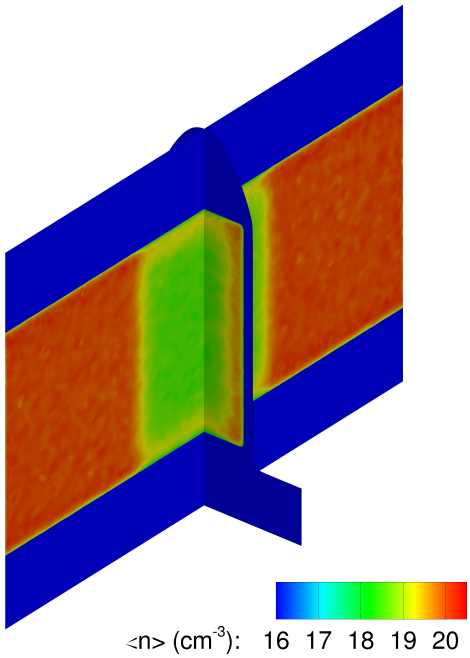

Fig. 3: *Average electron concentration in the cross sections of the device parallel and perpendicular to the source-drain direction in the middle of the device (y=0 and x=0 planes).*

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Comprehensive Simulation Study of Statistical Variability in 32nm SOI MOSFET

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1. Abstract

We have studied the statistical variability (SV) in thin-body silicon-on-insulator (TBSOI) MOSFETs with high-κ/metal gate stacks. We have considered the impact of the gate workfunction variation (WFV) in conjunction with random discrete dopants (RDD) and trapped interface charges. The simulations were carried with the Glasgow 3D 'atomistic' simulator GARAND. Results for both threshold voltage and on current variability are presented.

2. Introduction

Statistical variability (SV) in the MOSFET parameters, due to discrete charges and granularity of matter is a big challenge to nano-CMOS scaling and integration [1]. SV in devices degrades circuit and system performance, and increases the power dissipations in chips. SV in bulk MOSFETs is dominated by random discrete dopants (RDD) in the channel [2]. Fully depleted (FD) TBSOI devices, without channel doping, promise to reduce SV, as is crucial for further gate length reduction. However, with the introduction of high-κ/metal gate technology at the 45nm technology generation, WFV associated with different gate grain orientations becomes an extremely important source of SV for gate-first process [3, 4].

We study the impact of WFV on the threshold voltage (V_T) variability of a 32nm n-channel FD TBSOI transistor with high-κ/metal gate stack with various grain sizes (from 5 to 30 nm) and orientation, using 3D physical device simulations, on a statistical scale. Further, we compare the WFV-induced V_T variability with that due to RDD, LER, and PBTI-induced trapped charges [5].

3. Device Structure

The investigated device is a 32nm physical gate length TBSOI template nMOSFET developed by the EU PULLNANO consortium. This device features a TiN metal gate with a high-κ dielectric with equivalent oxide thickness of 1.2nm, and silicon body thickness of 7nm. The background channel doping concentrations is 1.2×10^{15} cm^{-3}. The buried oxide (BOX) thickness is 20nm. All other device specifications are following the ITRS requirement.

4. Simulation Methodology

The Glasgow 3D 'atomistic' device simulator has been used in this study on statistical samples of 1000 microscopically different, but macroscopically identical transistors. WFV arises from the different surface density in grains of different orientation [4], and is modeled in the simulator by creating a random metal gate grain pattern for each simulated device. Such a pattern is imported into the simulator following a procedure similar to that used previously to investigate polysilicon granularity [6]. We simulate two possible metal grain orientations in the gate, with 40% probability, for the grain orientation with a work function of 4.48eV, and 60% for the grain orientation with a work function of 4.68eV [3]. The modeling of RDD and LER follows a well-established procedure, the parameters for LER being 1.3nm RMS amplitude and 25nm correlation length. The PBTI-induced trapped charge sheet density (TCD) are chosen to be 1×10^{11}, 5×10^{11}, 1×10^{12} cm^{-2} representative of early, intermediate and later aging stages respectively, with the assumption that the charges are trapped at the Si/SiO_2 interfaces [7].

5. Results and Discussion

V_T extraction is based on sub-threshold current criterion of 1 μA/μm, at high drain bias V_D=1V, and for the uniform, continuously doped device results in V_T= 329 mV. Fig. 1 shows the dependency of σV_T on the average grain diameter of the metal gate for two simulation scenarios – with and without RDD and LER.

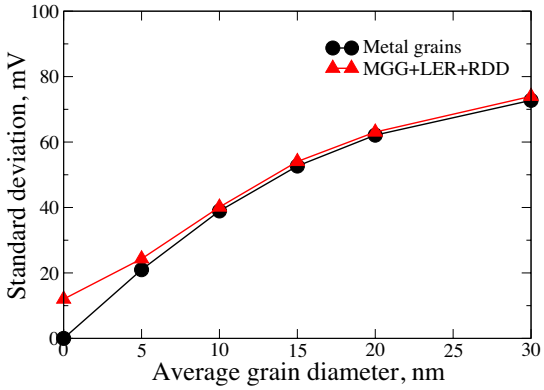

Fig.1: Dependence of σV_T on the metal gate grain size

Due to low channel doping, RDD on its own leads to the smallest V_T fluctuations (σV_T= 5 mV), and combined with LER results in σV_T of 12 mV. It is clear from Fig.1 that even at a relatively small average grain diameter of 5 nm,

MGG dominates the variability in this device. However, another important source of V_T variability is the trapped charge at the Si/SiO_2 interface, accumulated as a result of aging associated with N/PBTI [7]. Fig. 2 shows the dependency of σV_T on TCD for traps on their own and for two different average grain diameters of the metal gate. The highest simulated trap density leads to large V_T fluctuations in the traps-only case (~20 mV), but its contribution when metal gate granularity is considered is moderate (less than 10 mV). This is easily understood from Fig. 3, showing the conduction band landscape where the maximum charge density in the channel is. The effect of the traps (seen as spikes in the potential) is too localized, compared to the potential shifts due to different grains (identified as plateaus at different levels).

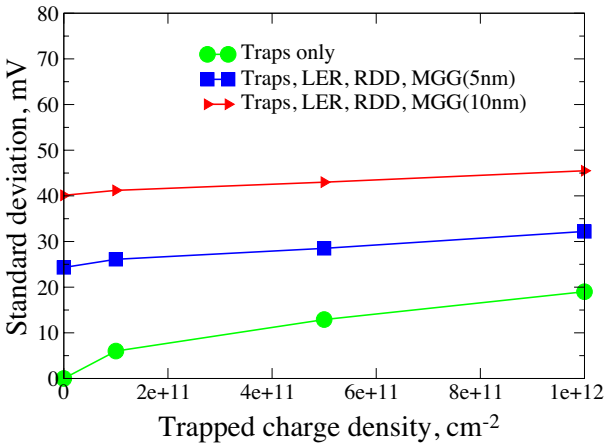

Fig.2: Dependence of σV_T on trapped charge density

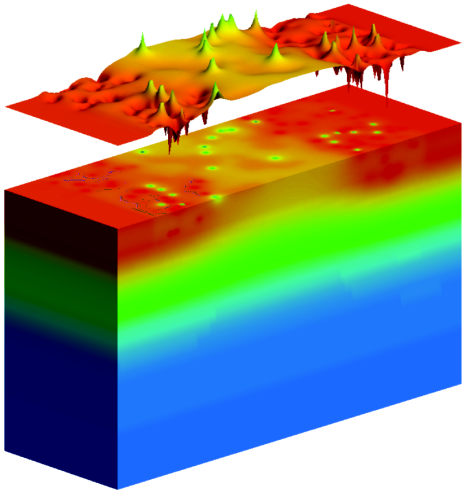

Fig. 3. The potential landscape where maximum electron density in the channel is, and potential distribution in the substrate. RDD,LER,MGG(5nm) and TCD($10^{12}cm^{-2}$).

Although RDD have small influence on V_T in FD-TBSOI devices, it has an important effect on the on-current (I_{ON}) variability, since such devices are very sensitive to the random dopant fluctuations in the source/drain access regions. This is obvious from Fig. 4, showing the linear transfer characteristics of the device sample. The curves fan out after maximum transconductance (~V_G of 0.6V), which is not typically observed in bulk, planar MOSFETs. This leads to a decorrelation between V_T and I_{ON}, most clearly illustrated with the scatter plot in Fig. 5. Since propagation delay in circuits is directly influenced by I_{ON}, any inference about its variability on the basis of V_T fluctuations alone may be misleading.

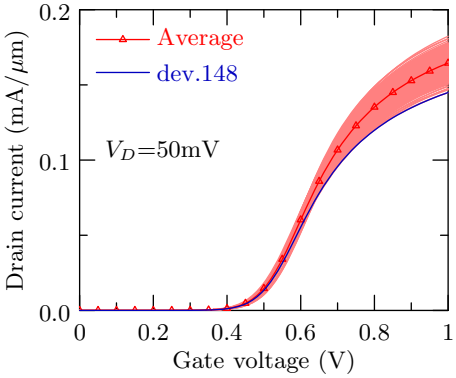

Fig. 4 Linear transfer characteristics of 1000-device sample.

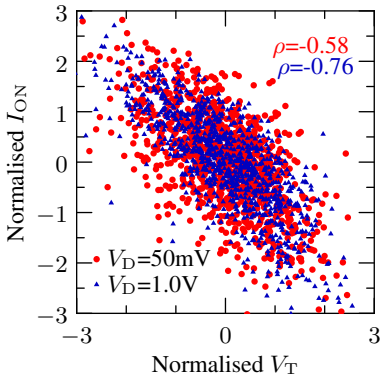

Fig. 5 Scatter plot of V_T vs. I_{ON} at low and high V_D

6. Conclusions

We present a statistical simulation investigation of the statistical variability in a 32nm TBSOI MOSFET, emphasizing the dominant impact of WFV on threshold voltage fluctuations. The impact of RDD and LER is successfully mediated in the simulated device structure. However, PBTI is still important at moderately large average grain diameter. RDD in the source and drain start to effect a decorrelation between threshold voltage and on-current, and have to be further investigated with advanced scaling of TBSOI devices.

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Quantum simulation of an UTB FD SOI FET with channel imperfections

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1. Abstract

The program for all-quantum simulation of a nanometer field-effect transistors was elaborated. The model is based on Landauer-Buttiker approach. The efficient calculation of transmission coefficients employs T-matrix technique involving an arbitrary (multiprecision) arithmetic to cope with evanescent modes. The results of simulation demonstrate the impact of realistic channel imperfections on transistor characteristics.

2. Introduction

The continuing progress in silicon VLSI technology motivates the transition to silicon-on-insulator (SOI) wafers. Just these structures definitely suppress short channel effects which substantially impair bulk MOSFET performance. The ultrathin body (UTB) (1-5nm) fully depleted (FD) silicon on insulator (SOI) will be a structure to take an ultimate advantage of SOI wafers and to provide an advancement of silicon technology to the extreme channel length. This also results in higher frequency and lower power consumption.

As a carrier wave length becomes commensurable with a channel size the all-quantum simulation of such small devices becomes challenging.

2. Efficient T-matrix method for quantum simulation

The efficient T-matrix method for solution of a scattering problem for the stationary Schrödinger equation in a transistor channel of nanometer length with an arbitrary potential relief was developed [1, 2]. The method allows fulfilling a simulation of a field effect transistor based on Landauer-Buttiker approach. It has a distinct physical sense clearly based on the conception of a transistor channel as a quantum wire or quantum wave-guide. The necessary transmission coefficients are determined via a self-consistent solution of Schrödinger and Poisson equations.

To cope with the well-known encumbrance caused by evanescent modes in a nonuniform wave-guide we employed an arbitrary (multiprecision) arithmetic. It allows to sustain accuracy when one manipulates at the same time with very small and very large numbers corresponding to exponentially decaying and exponentially growing evanescent modes [3, 4]. Then T-matrix technique turned out to be much faster than that of S-matrix. It is quite comprehensible because S-matrix method implies a solution of eigen-value problem in any cross-section of a channel with an arbitrary potential. We employ an expansion over eigen-functions of an ideal wave-guide and matrix elements of a potential describing mode coupling.

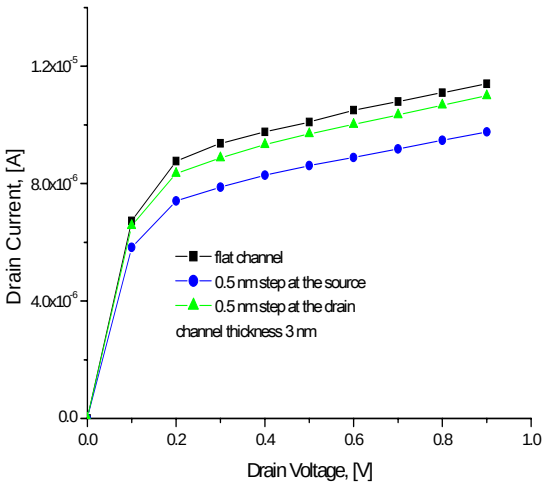

Fig.1: *Drain current vs. drain voltage: a perfect channel (squares) and a corrugated channel with a step near the source (dots) and the drain (triangles).*

3. Results of simulation: imperfections and stress in a channel

The results of simulation demonstrate the impact of realistic channel inhomogeneities and stress on transistor characteristics. The FD ETSOI FET in simulation is as follows: a gate length 10nm, spacers 5nm, channel thickness 2nm, channel width 5nm, equivalent gate oxide thickness 1.5nm, and source/drain contact doping 10^{20}cm^{-3}.

A fairly high and steep potential barrier originating at the junction of a heavily doped S/D contact and

undoped channel justifies a supposition of equilibrium distribution function for particles coming to the channel from S/D contacts and makes the Landauer-Buttiker approach to be valid although it does not incorporates a very strong scattering in contacts.

A step-like corrugation of a channel wall diminishes ON-state current (Fig. 1). A positively charged center augments ON-state current (Fig. 2). Merely, it means a shifted threshold voltage. A charged center may originate in a random impurity inside the channel, or in interface defect, or in defect inside the gate dielectric.

All kinds of inhomogeneities have much stronger effect on the current when they are located by the source contact compared with that located by the drain contact. The preliminary estimation of dispersion caused by realistic imperfectness of transistors in a circuit gives rise to 10-20%. In spite of former intuitive suspicions, it is not dramatic. However, some improvements of technology and materials for ultra-large integrated circuits may become necessary.

The program was also adopted to account for a strained silicon body. A stress leads to a deformed band structure with split valleys and changed effective masses. Parameters are the same as above. There is a redistribution of electrons among valleys due to stress. For upper curves in Fig. 3 electrons mostly occupy two [100] valleys, for lower curves electrons occupy four [010] and [001] valleys, therefore, the Fermi energy is smaller. The intermediate curve corresponds to an unstrained body. We attribute the main influence of stress to a change in Fermi energy leading to a shifted threshold voltage.

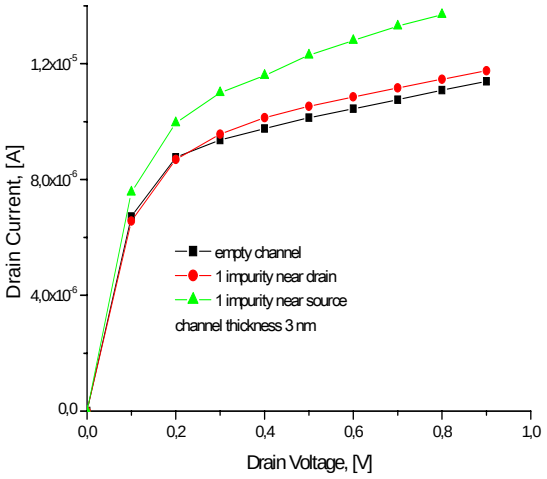

Fig.2: *Drain current vs. drain voltage: an empty channel (squares) and a channel with a single positively charged impurity near the source (triangles) and the drain (hearts).*

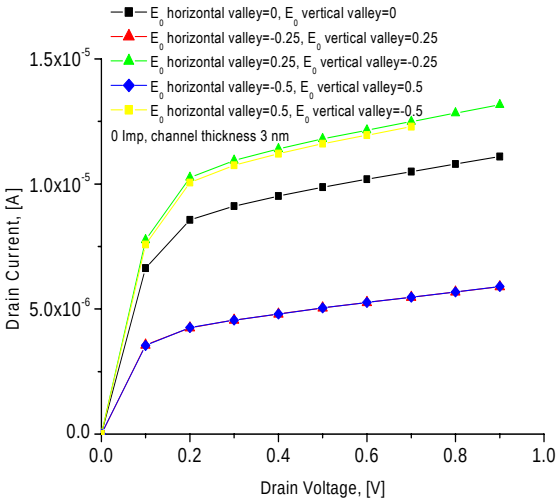

Fig.3: *Drain current vs. drain voltage: strained silicon channel with different kind of stress.*

4. Conclusions

The efficient program for all-quantum simulation of nanometer field-effect transistors was elaborated and employed for the estimation of an impact of realistic channel imperfections and stress on transistor characteristics.

Acknowledgement

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Session 7: Analog Performance & Circuits

Chair: João Antonio Martino

65nm Partially Depleted SOI Output Buffer with Active Body-Biasing Control

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1. Abstract

This paper proposes a specific high speed Input/Ouput interface which takes advantage of the Partially Depleted Silicon-on-Insulator technology while avoiding its drawbacks related to floating body effects, such as history effect and higher static leakage current compared to bulk technology. The proposed technique based on a dynamic control of the threshold voltage through active body biasing circuit achieves 10% speed improvement, while keeping same jitter and static power consumption as standard body contacted circuits.

2. Introduction

Partially Depleted Silicon-on-Insulator (PD-SOI) technology is attractive for its performance improvement at same supply voltage when using Floating Body (FB) devices [1]. Such performance gain in core digital design is also effective in Input/Output (I/O) circuits. Furthermore, another main motivation for using SOI technology is the immunity to latch-up effect which brings the opportunities to get transistors closer from one another and to remove guard rings.

On the other hand, due to the floating body effects, drawbacks emerge such as history effect and higher static power consumption, which are respectively non-existent and less significant in bulk technology. Within high speed I/O interface design, timing uncertainty due to history effect could be non-negligible as jitter is a key parameter in I/O design.

One simple solution is to use Body Contacted (BC) devices, with bodies tied to either Vdde (PMOS) or Gnde (NMOS), in order to suppress those unwanted effects but at the cost of a loss of performances and a larger silicon area.

A more advanced solution, called Active Body-biasing Control (ABC) [2], consists in dynamically modulating the threshold voltage (V_T) of transistors. However, the existing solution offers a limited control of the transistor to be body biased since during one half-period, the body remains floating which induces additional static leakage current and jitter. Let us notice that this solution was not specifically designed for I/O interface.

On the contrary, the ABC circuit proposed in this paper takes into account I/O concerns by providing a better body control in order to diminish jitter and to reduce static leakage current.

3. I/O Scheme

The I/O cell topology is divided in two parts, as shown in Fig. 1. The upper one is dedicated to the PMOS drive whereas the lower one is dedicated to the NMOS drive of the output buffer. It aims at transmitting the logic data coming from the core toward an external load. First, the input signal path is split and level-up shifted with respect to the external supply voltage (Vdde). The resulting signal is rise time and fall time controlled respectively for NBuffer and PBuffer so as to make sure that both transistors are not turned on simultaneously. Hence, a waste of power consumption is avoided during switching time of the output buffer where a large current has to be provided to the large load. Finally, buffer provides output impedance control.

For comparison purpose, level shifters and pre-drivers are body contacted with bodies tied to Vdde or Gnde accordingly. In this work, only the output buffer will be subject to modification, as further detailed in Section 6.

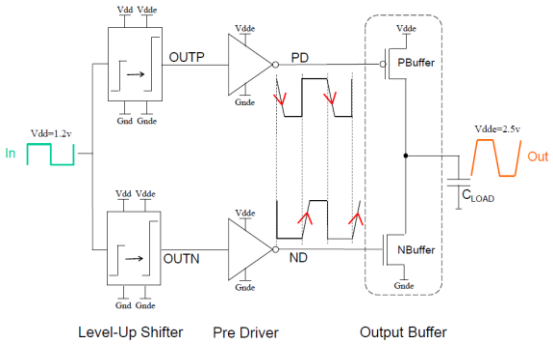

Fig. 1: *Output cell topology.*

Within I/O design, output jitter is one of the main parameters to be considered. As bit time is continuously lowered with speed increase of data communication, total jitter, including random and deterministic jitter, has to be taken into account in order to keep high signal integrity. Deterministic jitter can be divided into three categorizes: periodic jitter, duty-cycle-dependant jitter and Data-Dependant (DD) jitter [3]. In this paper, the jitter analysis will only be focused on DD jitter.

4. Floating Body Impact on I/O Design

Due to floating body effect, history effect arises which leads to timing uncertainty depending on the body potential fluctuation that occurred during the past history. Therefore, history effect is expected to impact

the output DD jitter of FB-based I/O circuits. To analyze the history effect impact, FB transistors are used for the output buffer depicted in Fig. 1.
1st/2nd switch method [4] yields in good enough timing characterization taking into account this effect. It consists in carrying out two simulations: a first one with logic '0' on the input as initial condition (DC0) and the second one with logic '1' (DC1). However, to achieve proper DD jitter calculation, all edges have to be taken into account within one simulation. Hence, the input signal considered for DD jitter calculation is shown in Fig. 2. A first data type signal is transmitted with DC0 condition. Then, logic '1' is held for 10s before starting the second data type transmission based on DC1 condition.

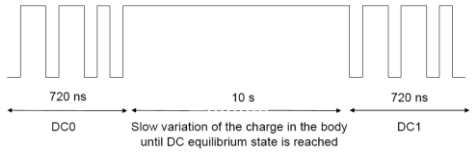

Fig. 2: *Input data type signal allowing jitter calculation considering history effect impact.*

The self body biasing of FB transistors also induces higher static current impact due to lowered V_T and junction diode current.
In order to cope with both the history effect and the high static current impact, the simplest solution is the use of BC transistors, equivalent to bulk transistors behaviour, by biasing the body to Gnde (NMOS) and Vdde (PMOS). This makes V_T rise but at the expense of a loss of dynamic performance.

5. Proposed ABC Circuit

The aim of ABC circuit is to modulate V_T through body biasing so as to improve transition time by lowering V_T during switching time and in order to reduce static current impact by increasing V_T during steady state.
In Fig. 3, only the NMOS part of the output buffer is shown since the PMOS part is symmetrically the same. The proposed ABC circuit allows a better control of V_T as opposed to FB transistors and as compared to the previous ABC solution where the body is floating for one half-period [2].

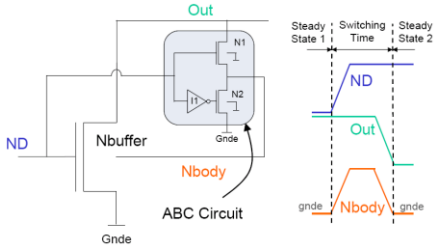

Fig. 3: *Pull down transistor and the proposed ABC circuit.*

The ABC circuit controlling Nbuffer consists of two NMOS N1 and N2, and one inverter I1. At steady state 1, when ND signal is low, N1 is turned off and N2 is turned on. Thus, Nbody is low. During switching time, while Nbuffer is being turned on, N1 is turned on which makes current flow through N1. Hence, Nbody tends to be high as Out is initially high. Then, Out goes low which consequently brings Nbody to low. In this phase, during the switching time, V_T has been lowered and Ion current has increased. Consequently, Nbuffer switches faster from off-state to on-state. At steady state 2, when ND signal is high, N1 is on and Nbody is pulled down to the Out node potential. Thus, Nbody is grounded.
At I/O cell level, one additional improvement consists in connecting the signals triggering both ABC circuits of Pbuffer and Nbuffer, to previous stages in order to anticipate the switching of the corresponding buffer transistor [5].

6. Simulation Results

Simulations were performed to compare four different output buffer structures based on: BC devices, FB devices, previous ABC circuit and proposed ABC circuit. Level-Up Shifters and Pre Drivers are body contacted whatever the output buffer structure. A comparative result is shown in Table 1. DD jitter is calculated with a capacitive load of 50pF and T_{BIT}=5ns.

Table 1: *Comparative result*

	BC	FB	Previous ABC [2]	Proposed ABC
Perf	X	-7%	-10%	-10%
DD Jitter	5.9 ps	20 ps	15 ps	3.8 ps
Istatic	4.7 nA	375 nA	430 nA	5.1 nA

BC-based output buffer is appointed as reference structure for performance evaluation. One can say that FB-based output buffer is quite faster than BC-based output buffer. Nevertheless, this structure is consuming extra static power and has a greater DD jitter, respectively due to heightened V_T and history effect impact. Previous ABC-based output buffer offers only mitigated improvement as compared to FB-based output buffer, essentially due to still floating body effect during one half-period. Finally, proposed ABC-based output buffer offers 10% performance gain while improving static leakage current and reducing DD jitter in the same order as BC-based output buffer.

7. Conclusion

An active body-bias control circuit has been proposed within I/O interface design. This solution offers both the advantages of the FB and the BC transistors. It brings higher performance and low static power consumption along with controlled history effect, only by adding a small circuitry as compared to the large transistors of the last I/O stage .

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A circuit level 65nm node bulk and SOI technologies comparison for analog amplifiers.

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1. Abstract

This work aims at demonstrating the effectiveness of advanced SOI CMOS technologies from an analog circuit designer point of view. After a quick review of the compared analog figures of merit of bulk and SOI technologies of the same 65nm node, we will present an automated sizing tool developed to target given specifications and deduce the remaining degrees of freedom. With this tool, we can fairly compare the SOI and bulk designs of a test amplifier.

2. Technologies main differences

Two twin CMOS technologies, bulk and partially depleted (PD) SOI, of the same 65nm node are considered. Size constraints and doping profiles are very similar [1]. The analog figures of merit of the three transistor types (high, standard and low V_{th}) were extracted from ELDO simulations with BSIM foundry models. The threshold voltages were calculated using the $I_D/sqrt(g_m)$ method. Their levels and behavior against length (L) or drain-source voltage (V_{DS}) appear very close.

Several analog improvements of SOI over bulk transistors are noted. The thin SOI layer and related shallow junctions lead to a better gate control on the channel, especially for low doped devices. The resulting body factor (n) gets closer to 1, thereby increasing the maximum g_m/I_D by about 10%. The Early voltage (V_{EA}, Fig. 1) is rather independent on the doping level for SOI, whereas it significantly drops for standard and low V_{th} bulk transistors, resulting in a SOI improvement of 50% for standard V_{th} and of a factor of three for low V_{th}.

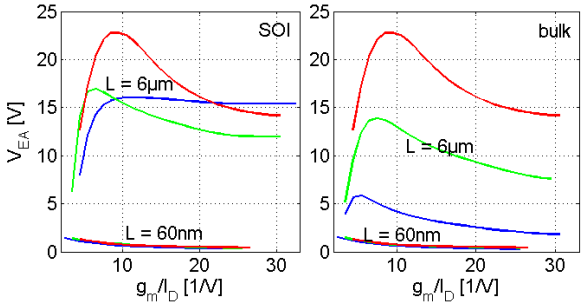

Fig. 1 : *Early voltage vs. g_m/I_D for different L @ V_{DS} = 0.5V , red: high V_{th}, green : standard V_{th}, blue : low V_{th}.*

Finally, the intrinsic capacitances show comparable values, while the extrinsic drain and source to substrate capacitance is three times smaller in SOI.

3. Automated sizing technique

Starting from a circuit level specification, the objective of the analog automated sizing technique is to find for each transistor, either a DC, a large signal or a small signal characteristic that will be used to find all values of the following matrix [2] satisfying the specification.

$$\begin{bmatrix} i_D \\ i_G \\ i_S \\ i_B \end{bmatrix} = \begin{bmatrix} C_{dd} & -C_{dg} & -C_{ds} & -C_{db} \\ -C_{gd} & C_{gg} & -C_{gs} & -C_{gb} \\ -C_{sd} & -C_{sg} & C_{ss} & -C_{sb} \\ -C_{bd} & -C_{bg} & -C_{bs} & C_{bb} \end{bmatrix} \cdot \begin{bmatrix} v_D \\ v_G \\ v_S \\ v_B \end{bmatrix} \cdot s + \begin{bmatrix} g_d & g_m & g_{ms} & g_{mb} \\ 0 & 0 & 0 & 0 \\ -g_d & -g_m & -g_{ms} & -g_{mb} \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_D \\ v_G \\ v_S \\ v_B \end{bmatrix}$$

Equ. 1 : *Small signal quadripole equivalent of a transistor.*

In other words, from a DC bias (V_{GS} and V_{DS}), a large signal swing or common mode range (V_{Dsat}), or a small signal gain or bandwidth (g_m/g_d or g_m/C), we can estimate the required g_m/I_D, L and V_{DS} for each transistor, from which we can calculate all its other characteristics from their SPICE model or measurements versus the three above-mentioned key design parameters (as in Fig. 1 for the Early voltage).

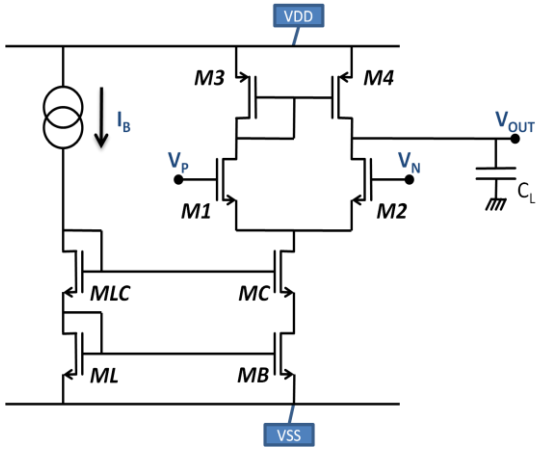

Fig. 2 : *Test structure schematic.*

Subsequently, any small-signal circuit level characteristic can be inferred (gain, bandwidth, PSRR, CMRR, phase margin). Large signal specifications can be approximated using the drain-source saturation voltage of each transistor (swing, input range), bias currents (slew rate) and DC attributes from all V_{GS} (systematic offset, bias voltages).

A simple differential pair with cascoded current source will be considered as a test structure for the analog performance comparison (Fig. 2). The developed sizing script starts from the output DC voltage, set at the middle of the 1.0V supply voltage. To lower the systematic offset, the matched transistors M3 and M4 need the same DC V_{DS}, that is $V_{DS3} = V_{GS3} = V_{DS4} = V_{DD}/2$. From V_{GS} and V_{DS} for M3, setting L to an arbitrary first-guess value, the three central figures of those two transistors are found. In order to maximize the output swing, as V_{Dsat} lowers in weak inversion, M3 and M4 are high-V_{th} type PMOS.

To maximize the input common mode range, V_{DsatC} and $V_{DSB} = V_{GSB}$ need to be minimized. V_{GS1} needs to remain low as well; therefore only low-V_{th} NMOS transistors were used. The V_{Dsat} versus g_m/I_D relationship is depicted in Fig. 3 for two L, showing a slight SOI advantage.

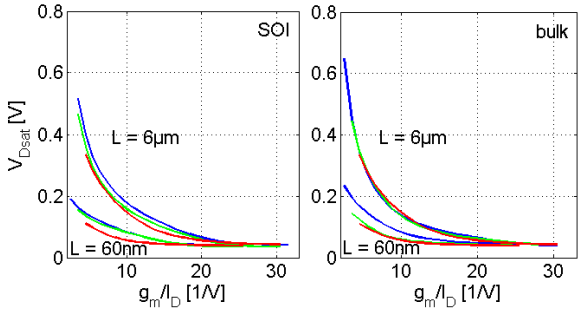

Fig. 3 : *Drain-source saturation voltage voltage vs. g_m/I_D for different L, left : SOI, right : bulk; red line : high V_{th}, green : standard V_{th}, blue : low V_{th}.*

The differential pair transistors characteristics are then found from the specified output swing, through their maximum V_{Dsat}.

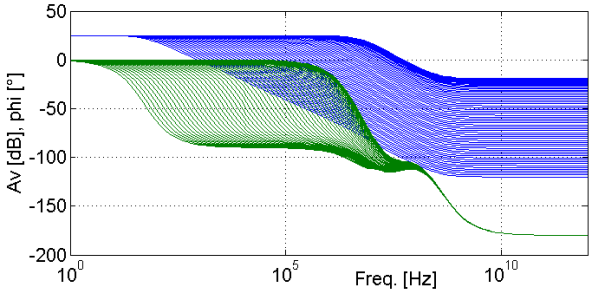

Fig. 4 : *Bode diagram of the SOI amplifier for 1nW to 0.1W power consumption.*

At this point, all calculated values are independent of the bias current. Setting its value will give the final size of each transistor, then its transconductance and capacitance values. The Bode diagram of the amplifier can be plotted for several values of power consumption, allowing the designer to minimize the consumption for a given gain bandwidth (Fig. 4).

4. Performance comparison

With this tool, amplifiers were designed on the twin SOI and bulk technologies, guaranteeing a fair comparison of the optimum achievable results for identical specifications.

For identical output swing (0.6V for a 1.0V power voltage), power consumption (1µW), and same channel lengths specifications, the result of the Bode diagram is plotted in Fig. 5.

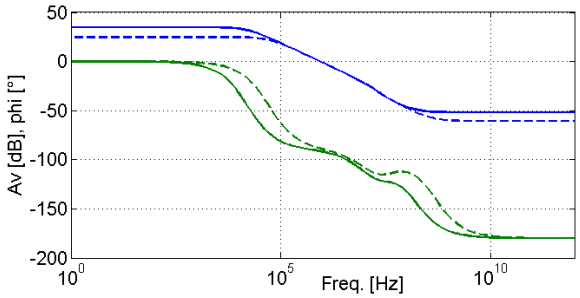

Fig. 5 : *Bode diagram of an amplifier designed on 65nm bulk (dashed) and SOI (line) technologies. Gain in blue, phase in green.*

The active area is about the same (31µm²), as well as the gain-bandwidth (0.9MHz), while the main SOI improvement actually appears on the DC gain, i.e. 35dB instead of 25dB, thanks to the better SOI V_{EA}.

To achieve higher bandwidth, the output transistors were shortened, and the power consumption raised to 1mW (Tab. 1). The SOI technology then shows better performances than bulk in terms of DC gain, bandwidth, and especially die active area, i.e. cost.

	SOI	*Bulk*
Av0 [*dB*]	27	23
GBW [*GHz*]	0.18	0.15
Phase margin [°]	75	78
Power cons. [*mW*]	1.00	1.00
Active surface [*µm²*]	12 000	40 000

Tab. 1 : *Comparison of high bandwidth OTA designs.*

4. Conclusion

Automated designs of SOI and bulk operational amplifiers were performed and compared. The better SOI V_{EA} and gm/Id permit significant improvements on the optimal gain, bandwidth, or active area for identical power specifications.

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Ultra-thin body and BOX SOI Analog Figures of Merit

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1. Abstract

In this paper, we analyze, for the first time to our best knowledge, the perspectives of ultra-thin body and BOX (UT2B) SOI CMOS technology for analog applications. We show that UT2B is a promising contender for analog applications, exhibiting high transconductance maximum, drive current, intrinsic gain and achievable cut-off frequencies in the range of 150-200 GHz. Effect of substrate bias, temperature, channel width and orientation on Analog Figures-of-Merit (FoM) is analyzed.

2. Introduction

Ultra-thin body (UTB) FD SOI MOSFETs are widely considered as one of the most promising candidates for ultimate device scaling requested by ITRS thanks to their immunity to short channel effects (SCE). Ultra thin BOX then allows suppression of fringing electric fields through the BOX thus further improving SCE control. Moreover, simulations predict a reduction of self-heating effects (SHE) in MOSFETs with thin-BOX. Additionally, ultra-thin BOX allows the use of back-gate control schemes. Electrostatics, scalability and variability issues in UT2B MOSFETs as well as their perspectives for low power digital applications are widely discussed in the literature [1-5]. However, till now no attention has been paid to their analog features. In this work we make a first assessment of UT2B technology for analog applications, paying particular attention to drive current, transconductance maximum, Early voltage and Intrinsic Gain as well as their variation with substrate bias, channel width and orientation and in a temperature range up to 250°C.

3. Experimental details

The devices were processed at CEA-LETI on UNIBOND (100) SOI wafers with 10-nm-thick BOX. In the channel region, the Si body was thinned down to about 7 nm. Elevated source-drain structures were employed to reduce parasitic resistance. No channel doping was used. The gate stack consisted of HfSiON with EOT of 1.3 nm, and TiN gate electrode. The measured devices were n-channel MOSFETs with the channel length L of 30 to 100 nm and the channel width W of 80 nm to 10 μm. Devices with 0° and 90° channel orientation were studied. I_dV_g and I_dV_d curves at different substrate bias, V_{sub}, were measured in a temperature range from room-temperature up to 250°C. Then, analog FoM were calculated, such as transconductance maximum, G_{mmax}, transconductance over drain current ratio, G_m/I_d, normalized drain current, $I_d/(W/L)$ taken at constant G_m/I_d of 10 and 5 V^{-1}, Early voltage, $V_{EA}=I_d/g_d$ and Intrinsic gain, $A_v=g_m/g_d=G_m/I_d \cdot V_{EA}$. Multi-fingers devices were used and embedded in coplanar waveguide access pads for performing RF characterization. RF measurements were performed in the frequency range from 100 kHz to 4 GHz.

3. Results and discussion

Table 1 summarizes analog FoM of UT2B devices with different channel lengths, widths, orientation and compares them with respect to previous technology "generations". UT2B devices feature improved analog FoM comparing to the counterparts from other technologies with the same L of about 100 nm. This results from the improved control of SCE, lower body factor and undoped silicon body in these UT2B devices. It can be seen that even 30 nm-long device exhibits rather high G_{mmax} and I_d values as well as Intrinsic gain as high as ~35 dB. Additionally, these values seem to be higher than previously reported for 50 nm-long UTB MOSFETs [8], possibly as a result of improved SCE control in these UT2B devices comparing to UTB ones. One can see that channel narrowing allows a further improvement of I_d and G_{mmax},

Table 1. *Summary of analog FoMs for different technologies.*

	$I_d/(W/L)$ $G_m/I_d=10V^{-1}$	$I_d/(W/L)$ $G_m/I_d=5V^{-1}$	$G_{mmax}/(W/L)$, S	Gain dB
FD SG SOI 120nm [6]	$3.5\cdot10^{-6}$ A	$9\cdot10^{-6}$ A	$5.5\ 10^{-5}$	10-15
FinFETs [7] L=100nm		$1.\cdot10^{-5}$ A	$6\ 10^{-5}$	30
UT2B,W=10μm 0° orientation				
L=100nm	$4.\cdot10^{-6}$ A	$1.3\cdot10^{-5}$ A	$8.4\cdot10^{-5}$	45-50
L=30nm	$1.7\cdot10^{-6}$ A	$5.3\cdot10^{-6}$ A	$3\cdot10^{-5}$	30-36
UT2B,W=80nm 0° orientation				
L=100nm	$5.3\cdot10^{-6}$ A	$1.2\cdot10^{-4}$ A	$1.2\cdot10^{-4}$	45-52
L=30nm	$2.5\cdot10^{-5}$ A	$4.8\cdot10^{-5}$ A	$4.8\cdot10^{-5}$	30-37
UT2B,W=10μm 90° orientation				
L=100nm	$2.8\cdot10^{-6}$ A	$8.5\cdot10^{-6}$ A	$5.4\cdot10^{-5}$	42-47
L=30nm	$8.5\cdot10^{-7}$ A	$2.5\cdot10^{-6}$ A	$1.5\cdot10^{-5}$	30-36

while intrinsic gain stays almost invariant. Contrarily, 90° channel orientation, which is unfavorable for n-channels, indeed results in I_d and G_{mmax} degradation, keeping Intrinsic gain again almost unchangeable.

Fig.1 shows variation of Intrinsic gain as a function gate and drain applied biases. It can be seen that the highest values are achieved when V_g=0.4V, i.e. at about threshold voltage (V_T=0.38V for L=30nm) which is profitable for low voltage/low power applications.

When investigating analog FoM, one should care that self-heating and substrate [9] effects cause device conductance, G_d, and hence V_{EA}, degradation with frequency. Indeed, G_d vs. frequency curves (Fig. 2) clearly exhibit transitions due to both SH (in MHz range) and substrate (in Hz, due to minority carrier, and GHz, due to majority carriers, ranges) effects. Moreover, it is clearly seen that substrate-related G_d degradation can become as strong as (and even stronger than) SHE-related one (especially at lower V_g) in UT2B devices without ground plane, as was previously predicted in [9].

Regarding RF performance, cut-off frequency as high as ~150 GHz and ~200 GHz can be obtained in 50nm- and 30nm- long UT2B devices, respectively.

Considering back-bias control schemes, we, then, analyzed effect of substrate bias on analog FoM. Effect of V_{sub} is two-fold: from one hand, it is known, that application of negative substrate bias will increase V_T, thus improving I_{on}/I_{off}, improve both subthreshold slope and DIBL [2,5] (i.e. profitable for digital applications); from another hand, application of positive substrate bias will improve I_d/I_g ratio (i.e. profitable for low power application) and will move charge centroid to the bottom film interface featured higher mobility [10]. So, below we analyze which effect will dominate in analog FoM. G_m/I_d vs. $I_d/(W/L)$ curve is very useful tool for such analysis since being V_T independent it allows to discard effect of strong V_T vs V_{sub} shift. We observed that drain current, taken at fixed G_m/I_d, increases slightly (5-10%) when V_{sub} moves to positive values, which is most probably a sign

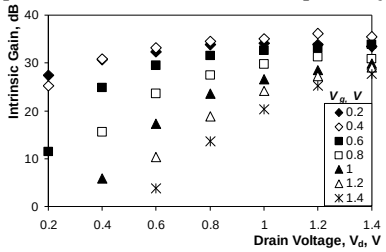

Fig.1: *Intrinsic gain vs. V_d at different V_g. L=30nm. W=10µm.*

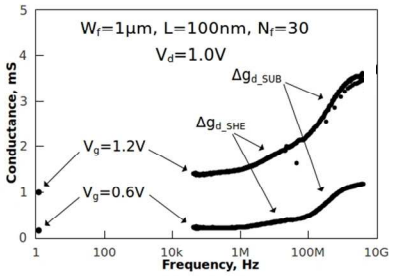

Fig.2: *Conductance vs. frequency at different bias conditions.*

of beneficial effect of mobility. Contrarily, negative V_{sub} seem to be slightly preferable for V_{EA} and G_m/I_d taken at fixed V_g=V_d. As a result some ~5 dB improvement in the Intrinsic gain can be expected for the case with negatively biased V_{sub}, while dominant mechanism is not so evident in the weak inversion region (Fig. 3).

Finally, we assessed the perspectives of UT2B devices for high-temperature applications. UT2B devices featuring thin Si body exhibit extremely small variation of threshold voltage of 0.6 mV/dec and subthreshold slope variation close to that predicted by kT/q ln(10) dependence. V_{EA} stays quasi-constant in the temperature range up to 250°C. As result, devices keep fairly "correct" both analog and digital performance in a wide temperature range. Degradation of intrinsic gain is limited to 5-8 dB, notwithstanding G_m/I_d degrades almost twice at T=250°C. Table 2 summarizes temperature evolution of different UT2B parameters.

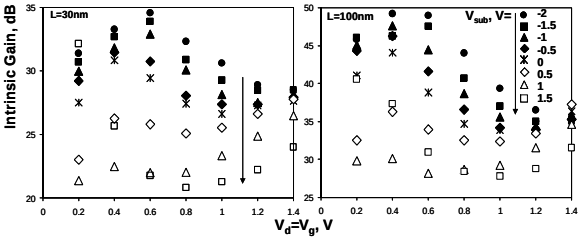

Fig.3: *Intrinsic gain vs. applied bias, V_g=V_d at different V_{sub}.*

Table 2: *Temperature evolution of UT2B figures. L = 100 nm.*

T, °C	I_{dnorm} G_m/I_d= 10 V^{-1}	I_{dnorm} G_m/I_d= 10 V^{-1}	I_{on}/I_{off}	G_{mmax} norm	G_m/I_d max	Gain Vg=Vd =0.4V
25	4µA	13.2µA	10^5	81µS	$34V^{-1}$	42 dB
125	2.8µA	10.6µA	$8·10^5$	71µS	$25V^{-1}$	38 dB
250	1.9µA	8.6µA	$2·10^4$	65µS	$19V^{-1}$	34 dB

4. Conclusions

Perspectives of UT2B SOI technology for analog applications were extensively studied. Influence of substrate bias, channel orientation and temperature on analog FoM was assessed. It was demonstrated that UT2B has a great potential for analog applications featuring high drive current, transconductance maximum and intrinsic gain. Negative substrate biasing allows for further about 5dB increasing of intrinsic gain. Very limited degradation of device parameters in temperature range up to 250°C was observed.

Acknowledgements:
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Temperature Influence on the Analog Performance of 45º Rotated Triple-Gate nFinFETs

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1. Abstract

This work presents the analog performance of n-type triple-gate FinFETs with high-κ dielectrics and TiN gate material fabricated in 45º rotated SOI substrates. Different fin widths are studied for temperatures ranging from 250 K up to 400 K.

2. Introduction and Device Fabrication

FinFETs are attractive devices for the CMOS nanometer era due to the improved gate control on the channel charges resulting in excellent short-channel immunity. Also relevant improvements against planar devices have been demonstrated for the analog operation of FinFETs, exhibiting reduced drain output conductance (g_D) and higher open-loop voltage gain (A_V)[1]. These improvements are obtained by using narrow fins [2]. In this case, the majority of the drain current flows through the sidewalls in the (110) plane and not in the traditional (100) plane as in planar devices. The problem associated with this change in the conduction direction is that the mobility of electrons is degraded in the (110) crystal orientation with respect to (100) whereas the mobility of holes is improved [3]. In order to overcome the electron mobility degradation due to crystal orientation for sidewall conduction, the substrate can be rotated in 45º such that all the conduction planes will be (100) [4]. Although the improvements of substrate rotation have been discussed in the literature, its impact on the analog parameters of FinFETs in a wide temperature range has not been presented yet. This paper studies the influence of the substrate rotation on the analog parameters of n-type triple-gate FinFETs with HfSiON gate dielectric, TiN gate material and undoped body.

Tall triple-gate n-type FinFETs were fabricated in 45º rotated SOI wafers with 150 nm thick buried oxide, following the same process of ref. [5]. The fin height (H_{Fin}) is 65 nm for all devices. After the fin patterning a 1 nm thick interfacial thermal oxide is grown followed by the deposition of 2.3 nm HfSiON. A 5 nm thick TiN layer is then deposited and a 100 nm thick amorphous silicon capping completes the gate stack. No channel doping or halo implantation is applied during the processing, keeping the p-type doping level in the order of 10^{15} cm^{-3}. Nickel silicidation is used to reduce the access resistance. Devices composed by 5 parallel fins with L=1 µm and variable fin width (W_{Fin}) were used.

3. Results and Discussion

Figure 1 presents extracted transconductance normalized by the device channel width (g_m/W, $W=2*H_{Fin}+W_{Fin}$) as a function of W_{Fin} for the measured FinFETs in linear region with a drain bias of V_{DS}=50 mV and variable temperature.

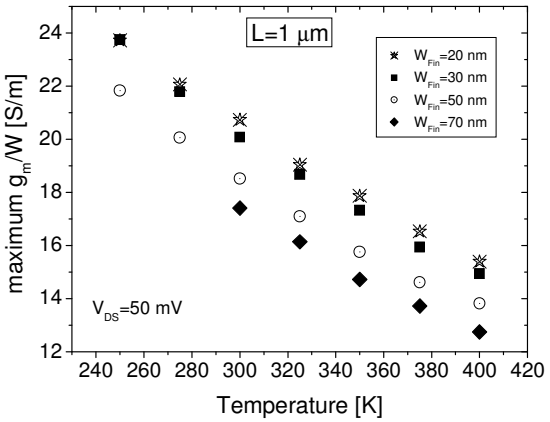

Fig. 1 – *Measured maximum g_m/W as a function of temperature at V_{DS}=50 mV for FinFETs with variable W_{Fin}.*

From the results of Figure 1 one can see that the narrower is the FinFET the larger is the normalized transconductance as the better coupling between the sidewalls improves the carrier mobility with respect to wider ones. Also the transconductance (and hence the carrier mobility) increases linearly with the temperature reduction independently of W_{Fin} under consideration. This linear increase of maximum g_m indicates that the dominant mobility degradation factor is the phonon scattering [6] in this temperature range. The $|dg_m/dT|$ rate varies in the range of 56.5 nS/µmK for a 20 nm wide FinFET to 53.8 nS/µmK and 46.9 nS/µmK for W_{Fin}= 50 nm and 70 nm, respectively. It indicates that

narrower fins present a larger g_m increase with T reduction than wider ones.

To investigate the impact of fin width and substrate rotation on the analog properties of FinFETs, the devices have been measured in saturation at a drain bias of 0.85 V and gate voltage overdrive ($V_{GT}=V_{GF}-V_{TH}$, V_{GF} being the gate voltage and V_{TH} the threshold voltage) of 0.20 V. Figure 2 presents the output conductance per channel width (g_D/W) plotted for different W_{Fin} and temperatures.

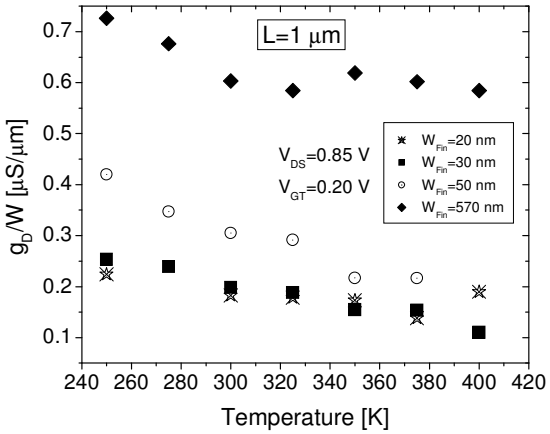

Fig. 2 – *Measured g_D/W as a function of W_{Fin} at several temperatures with V_{DS}=0.85 V and V_{GT}=0.2 V.*

The g_D is smaller for narrower FinFETs in the whole temperature range and degrades as the W_{Fin} is increased. This phenomenon is associated with the higher coupling between the two lateral gates as W_{Fin} is reduced, which contributes to minimize the channel length modulation effect due to the drain bias. In addition, the temperature reduction promotes g_D degradation. Using the extracted g_D results and the measured I_{DS} the Early voltage ($V_{EA}\approx g_D/I_{DS}$) has been calculated and the results are presented in Figure 3.

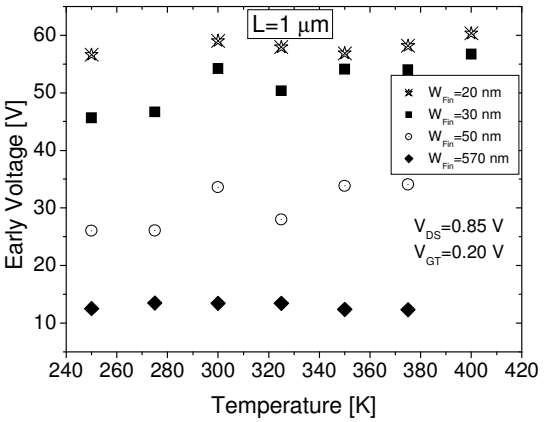

Fig. 3 – *Extracted V_{EA} as a function of W_{Fin} at several temperatures with V_{DS}=0.85 V and V_{GT}=0.2 V.*

The results of Figure 3 show that the Early voltage is larger in narrower FinFETs and degrades as the W_{Fin} is increased. As for g_D the less effective coupling between the sidewall gates with larger W_{Fin} diminishes the V_{EA}.

Using the extracted values for g_m/W and g_D/W at V_{GT}=0.2 V and V_{DS}=0.85 V the intrinsic voltage gain ($A_V=g_m/g_D$) has been calculated and the results are plotted in Figure 4.

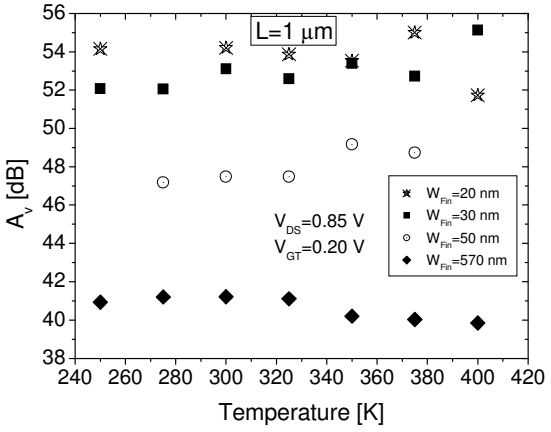

Fig. 4 – *Calculated A_V as a function of W_{Fin} at several temperatures with V_{DS}=0.85 V and V_{GT}=0.2 V.*

The W_{Fin} increase from 20 nm to 570 nm causes a degradation of A_V by 14 dB because of the larger g_D in wider FinFETs. Among the several W_{Fin} under study one can see that the maximum A_V variation with temperature is in the order of 2 dB, indicating that the improvement on g_m with temperature reduction is being compensated by the g_D degradation in all cases.

4. Conclusions

This work studied the temperature variation influence on the performance of triple-gate FinFETs built on 45° rotated substrate in a temperature range from 250 K to 400 K. It has been demonstrated that the narrower is the fin the larger is the normalized transconductance per channel width, both in linear or in saturation region. The increase of fin width degrades the output conductance due to the larger channel length modulation leading to a reduction of 14 dB in the intrinsic voltage gain when the fin width increases from 20 nm to 570 nm. In the temperature range and fin widths under study the intrinsic voltage gain variation is not larger than 2 dB.

Acknowledgments

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Session 8: SOI Devices

Chair: Jouni Ahopelto

TiN/$GdScO_3$/strained $Si_{0.5}Ge_{0.5}$/SSOI stack for high mobility short channel *p*-MOSFETs

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1. Abstract

Long and short channel *p*-MOSFETs with compressively strained $Si_{0.5}Ge_{0.5}$ channels on tensely strained SOI substrates are demonstrated with a novel high-κ gate stack, comprising of $GdScO_3$ and TiN. 100 nm gate length devices exhibit an I_{on}/I_{off} current ratio of 4×10^5 and a threshold voltage of V_T=585 mV. The low field hole mobility, 265 cm^2/Vs (extracted from long channel MOSFETs), is about 100% higher than the universal hole mobility in Si. The transistor performance will be discussed regarding the <110> and <100> channel orientations.

2. Introduction

Currently, uniaxial compressively strained Si is the dominant technology for high performance *p*-MOS devices. In order to achieve further mobility improvement in nanoscaled devices, it is important to examine novel channel materials such as strained/relaxed SiGe and Ge [1]. Hole mobility is known to be higher in SiGe than in Si. Even more, a compressive strain splits the light hole (LH) and heavy hole (HH) bands. This, in combination with confinement effect, results in reduced scattering, and subsequently, increased hole mobility. Significantly performance enhancements compared to Si devices have already been demonstrated in p-type MOSFETs with strained SiGe channels [1]. However, the integration of strained SiGe or Ge channels requires the use of high-k dielectrics as gate oxides and thus low temperature processes in order to conserve the elastic strain and reduce Ge (inter)diffusion. Although ternary rare earth high-κ dielectrics such as $LaLuO_3$, $LaScO_3$ or $GdScO_3$ are promising candidates for gate-first processed transistors, the scalability of such stacks has not been demonstrated yet [2,3]. We will assess here the hole mobility and electrical performances of short gate length strained $Si_{0.5}Ge_{0.5}$ / strained SOI (SSOI) *p*-MOSFETs with TiN/$GdScO_3$ gate stacks. Different channel orientations are compared regarding the carrier mobility and device performances.

3. Device fabrication

The devices were fabricated on 5 nm strained Si / 25 nm $Si_{0.5}Ge_{0.5}$ layers pseudomorphically grown on 12 nm biaxially tensile strained SOI substrates by reduced pressure – chemical vapor deposition (RPCVD) [4]. The Si cap was thinned from 5 down to approximately 3 nm thanks to a RCA wet cleaning before $GdScO_3$ deposition. 10 nm of amorphous $GdScO_3$ films, with a dielectric constant κ = 24 [5], were deposited by e-gun evaporation at a substrate temperature of 300°C, followed by TiN sputter deposition. The low temperature gate-first process flow used for device fabrication is schematically shown in Fig.1 (a)-(c). The gate was then patterned, with lengths ranging from 100 nm to 1.5 µm (a). Source and drain (S/D) areas were then formed by 16 keV BF_2^+ implantation to 2×10^{15} ions/cm^2, and forming gas anneal (1:10 H_2/N_2) at 650°C for 1 minute (b). A SiO_2 passivation layer was deposited over the structures and the S/D and gate windows were opened for Al metal contacts deposition (c).

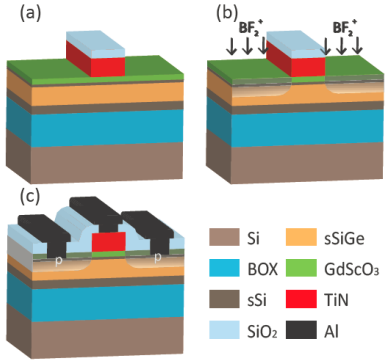

Fig.1: *(a)-(c) Schematic of the gate first process flow used to fabricate strained SiGe/SSOI MOSFETs with TiN/$GdScO_3$ gate stacks.*

4. Results

Fig.2(a) depicts the degree of relaxation of strained $Si_{0.5}Ge_{0.5}$ layers as a function of the annealing temperature and layer thickness. The 25 nm thick $Si_{0.5}Ge_{0.5}$ layer remains fully strained up to an annealing

temperature of 850°C. The Raman spectra of the S/D regions of a processed MOSFET indicate no relaxation as seen in Fig. 2b. TEM analyses of the gate stack demonstrate that the $GdScO_3$ dielectric is amorphous (Fig. 2c).

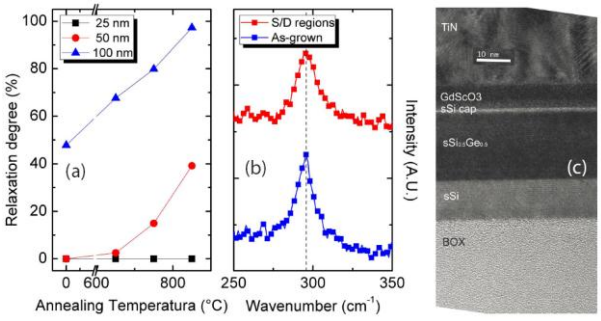

Fig.2: *(a)* $Si_{0.5}Ge_{0.5}$ *relaxation degree as a function of the annealing temperature (various layer thicknesses probed). Annealing time: 5 minutes, (b) Raman spectra of an as-grown SiGe layer and S/D areas of a MOSFET; and (c) cross-sectional TEM image of the channel region.*

The transfer-characteristics of the strained SiGe device with 500 nm gate length are presented in Fig. 3(a). The subthreshold slope (SS) of the transistor is 90 mV/dec, and the threshold voltage V_T= - 670 mV. The transistor exhibits a maximum I_{on}/I_{off} current ratio of 10^6 (10^5 if I_{off} is taken at zero gate bias). The short channel transistors with 100 nm gate length show an I_{on}/I_{off} ratio of 4×10^5. The relatively low I_{on} of 105 µA/µm at V_d= - 1.5 V is due to the high S/D resistance. The S/D resistance can be improved by optimization of SiGe doping activation and by forming silicided S/D. For the short channel transistor the subthreshold slope degrades to 134 mV/dec.

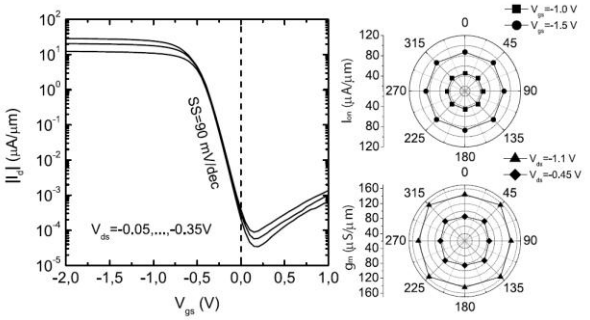

Fig.3: *(a) Transfer-characteristics of a 500 nm channel length device; and (b)* I_{on} *(top right) and transconductance (bottom right) dependence on the channel orientation, where 0° and 45° represents the <100>and <110> crystal directions, respectively.*

With our fabrication process, the short channel devices are defined by the gate patterning, with the SiGe channel being under biaxial strain. Fig. 3(b) indicates identical I_{on} and transconductance for transistors with <100> and <110> channel orientation. This is consistent with the simulation results of Krisnamohan *et al.* [1] for strained SiGe *p*-MOSFETs, where the channel direction dependence appears only under uniaxial strain. In order to evaluate the hole mobility, long channel devices were fabricated. Fig. 4(a) displays the effective hole mobility extracted using the split *C-V* method from a 1.5 µm gate length transistor. The device exhibits a peak mobility of 265 cm^2/Vs at low inversion charge density. The relative mobility enhancement compared to Si universal mobility falls from 90% at low fields to about 40% at high fields. In our heterostructure, the transport at high electric fields takes place both in the strained Si cap and the SiGe layer underneath. Dual channel formation is illustrated in Fig. 4 by a 2D SILVACO simulation [6] of the potential well created in the heterostructure device for two different gate voltages. At higher gate voltages (V_g), a channel in Si with a higher density of holes is created, with consequently a mobility decrease.

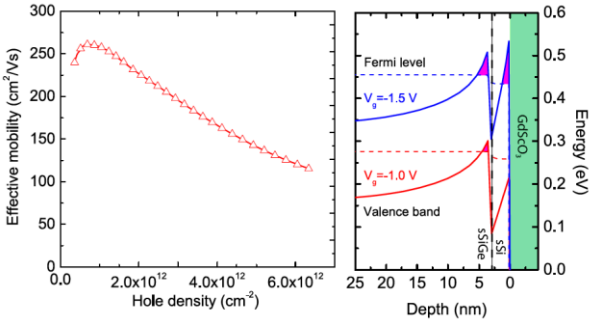

Fig.4: *(a) Hole mobility and mobility enhancement relative to universal Si results extracted from the strained SiGe channel MOSFET with* $GdScO_3$ *gate dielectric; and (b) 2D simulation of the potential well created in the transistor at gate voltages of -1.0 and -1.5 V. The dashed and solid lines represent the Fermi level for holes and the valence band edges, respectively.*

5. Conclusions

We present a high performance strained SiGe channel *p*-MOSFET using $GdScO_3$ /TiN gate stack. We show that both channel and gate dielectric conserve their integrity after a low thermal budget gate-first process. The 500 nm long channel transistor exhibits a subthreshold slope of 90 mV/dec and an on-off ratio of 10^5 for I_{off} at V_g=0. The hole mobilities, I_{on} and g_m are independent of the channel orientation due to biaxial strain. The device shows 90% improved mobility at low inversion compared to the universal Si mobility curve.

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2D Analytical Calculation of the Current in Lightly Doped Schottky Barrier Double-Gate MOSFET

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1. Abstract

Here we present a new way to predict the tunneling and thermionic current of Schottky barrier Double-Gate MOSFETs (SB-DG-MOSFET) in subthreshold operation region. 2D solutions of the electrostatic potential and electric field are used to calculate the tunneling current with the Wentzel-Kramers-Brillouin (WKB) approximation. A comparison with data simulated by TCAD Sentaurus for channel lengths down to 65nm and several barrier heights was made and is in a good agreement to this simulation results.

2. Introduction

In the last years, the research for sub-20nm devices focuses on new SOI-type structures. With these structures downscaling to the sub-10nm range is possible with so called DG-MOSFETs, FinFET and GAA (Gate-all-around) FETs. These alternative designs on SOI substrate reduce dramatically short channel effects (SCE) [1]. Another issue becomes more and more significant, the parasitic resistances of the highly doped source/drain (S/D) regions. Therefore, the Schottky barrier (SB) MOSFET is one of the promising structures because of its metallic source/drain (S/D) electrodes with low specific resistances [2]. Further advantages are high scalability even down to the sub-10nm region and good process compability with current standard Si technologies.

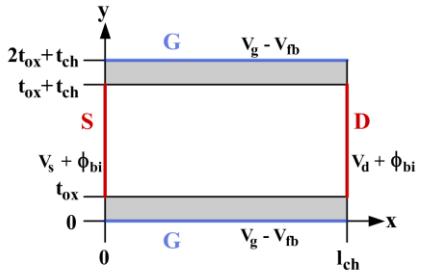

Fig.1: *Simplified geometry and boundaries of a SB-DG-MOSFET. Thick lines define the S/D metal contacts and gate contacts, respectively.*

Compact models for SB-DG-MOSFETs require an analytical calculation of the channel current. This paper shows a new way to predict the tunneling and thermionic current for Schottky barrier Double-Gate MOSFETs (Fig. 1) in subthreshold operation region including 2D effects from the electrostatic potential and the electric field. Subthreshold currents and the ambipolar behavior depend on those potentials and fields. In [3], [4] we already presented analytical closed-form models for the potential and electric field based on the conformal mapping technique. The barrier height ϕ_{Bn} is included in the built-in potential ϕ_{bi} as part of the boundaries is defined in Fig. 1 [3].

A first approach for the tunneling current with respect to the energy has been presented in [5]. Here we show an improvement of this approach. The approach is shown for electron tunneling at the source and can be used in similar way for calculation of hole tunneling at the drain.

3. Calculation of the Tunneling Thermionic Current

For the calculation of the tunneling current it is necessary to estimate the tunneling probability of the charge carriers. Therefore, we use the enhanced WKB model presented in [6], which assumes a triangular potential profile. It follows

$$T(\vec{E},x,y) = \exp\left(\frac{-4\sqrt{2m\cdot m_0}\left(|\vec{E}(x,y)|\cdot x\right)^{3/2}}{3q\hbar|\vec{E}(x,y)|}\right). \quad (1)$$

Here m describes the effective mass, m_0 the electron rest mass, q the elementary charge, $\hbar$ the reduced Planck constant and $\vec{E}$ the electric field at the point of interest on the position y (Fig. 2). The tunneling current density is predicted with

$$J_{tun}(y) = \frac{A^*T}{k}\int_0^{l_{ch}} T(\vec{E},x,y)\cdot f_m(\xi(x))\cdot[1-f_s(\xi(x))]\frac{\partial\xi}{\partial x}dx. \quad (2)$$

In contrast to [5], [7], here we integrate with respect to position x along the channel instead of the energy ξ. Here A^* is the Richardson constant, T the temperature in K and k the Boltzmann constant. The tunneling current results from the integration over dimensions y and z

$$I_{tun} = \int_0^{w_{ch}}\int_{t_{ox}}^{t_{ox}+t_{ch}} J_{tun,M\to S}(y)\cdot dy\cdot dz. \quad (3)$$

The integration takes place along the boundary for the channel thickness t_{ch} and the channel width w_{ch} of the device. The contribution of the thermionic current is calculated as presented in [7].

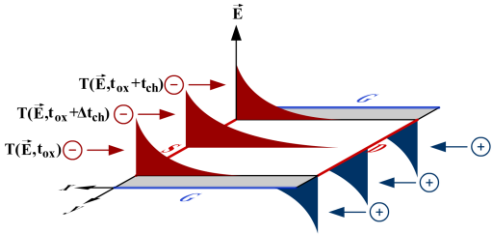

Fig.2: *The schematic tunneling probability for inversion mode is calculated at the boundaries depending on the position y.*

Charge carriers with energies larger than the top of the barrier contribute to the current, while the shape of the barrier is ignored. It follows for the thermionic current density

$$J_{therm}(y) = A^* T^2 \exp\left(-\frac{q\phi_B(y)}{kT}\left[\exp\left(\frac{qV_{ds}}{kT}\right) - 1\right]\right). \quad (4)$$

Here $\phi_B(y)$ describes the maximum barrier the carriers have to surmount which is calculated using the analytical model presented in [3]. Finally the thermionic current is expressed

$$I_{therm} = \int_0^{w_{ch}} \int_{t_{ox}}^{t_{ox}+t_{ch}} J_{therm,M\to S}(y) \cdot dy \cdot dz. \quad (5)$$

4. Discussion

In Fig. 3 we present the result of the tunneling probability for the electrons at the source electrode. We observe from this plot a two dimensional influence on the tunneling probability from the two gates on top and bottom.

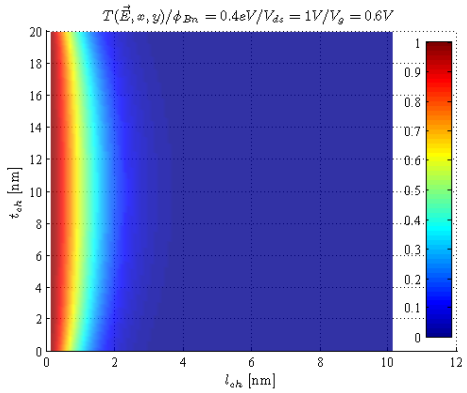

Fig.3: *Tunneling probability of electrons at the source electrode in inversion for $\phi_{Bn} = 0.4eV$, Device geometry: l_{ch}= 65nm, t_{ch}= 20nm, t_{ox}= 2nm, ϵ_{ox}= 7. Bias conditions: $V_{ds} = 1V$, $V_g = 0.6V$.*

We compared the results of our model with numerical device simulations of TCAD Sentaurus [8]. Fig. 4 shows us the summarized current of quantum mechanical tunneling and thermionic emission compared to the overall current extracted from TCAD Sentaurus. The masses of electrons and holes have been fitted in the model, we use for $m_n = 0.22$ and for $m_p = 0.19$. As we can observe our results differ from the simulated data in the accumulation and inversion regions, because additional charge carriers take influence (which are currently not considered in our model), and also because we did not consider drift-diffusion transport (the effects of which dominate in the strong inversion region) nor a varying Fermi level between source and drain (also, an important effect in strong inversion). Nevertheless, the behavior of our model is close to the behavior of the simulated curves from TCAD Sentaurus in the subthreshold regime where tunneling/thermionic transport effects dominate.

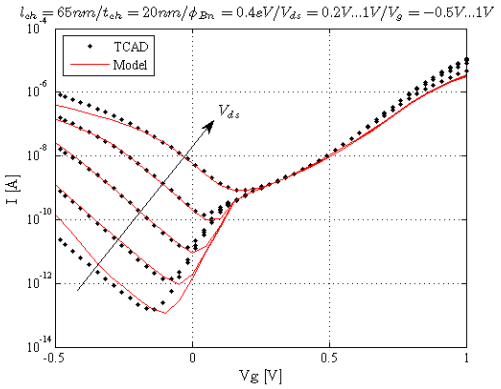

Fig.4: *Tunneling and thermionic current of a SB-DG-MOSFET for $\phi_{Bn} = 0.4eV$ compared to TCAD Sentaurus. Device geometry: $l_{ch} = 65nm$, $t_{ch} = 20nm$. Bias conditions: $V_{ds} = 0.2V$ to $1V$ with $0.2V$ steps, $V_g = -0.5V$ to $1V$ with $0.01V$ steps.*

5. Conclusions

We presented an approach to calculate the tunneling and thermionic current in SB-DG-MOSFETs. This approach shows a good agreement with the simulation results down to 65nm channel lengths in the subthreshold region. The model presented here is able to predict the current well for several barrier heights and several geometries and can therefore contribute to the definition of a compact model for SB-DG-MOSFETs including 2D effects.

6. Acknowledgment

This project was supported by the German Federal Ministry of Education and Research under contract No. 1779X09 and by the European Commission under FP7 Projects ICT-216171 (NANOSIL) and IAPP-218255 (COMON), by the Spanish Ministerio de Ciencia y Tecnologa under Projects TEC2008-06758-C02-02, and also by the PGIR/15 Grant from URV and by the ICREA Academia Prize.

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LDMOS transistors on 150 mm silicon-on-polycrystalline-silicon carbide hybrid substrates

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1. Abstract

Silicon based RF and power devices need a substrate that conducts heat better than conventional SOI-substrates. Here, the silicon dioxide insulator and the silicon substrate as in a SOI-wafer, are replaced by silicon carbide (SiC) which has higher thermal conductivity and is semi-insulating. Successful LDMOS-transistors were processed on the 150 mm Silicon-on-polycrystalline-Silicon carbide (Si-on-poly-SiC) substrates with improved or equal electrical performance compared to a RF-optimized SOI substrate.

2. Introduction

Our group has previously presented a new Si-on-poly-SiC hybrid substrate which reduces substrate RF losses and improve the thermal properties compared to a conventional SOI wafer [1-4, 7]. In previous works [1-4], 50 mm single-crystalline SiC or 100 mm poly-crystalline SiC (poly-SiC) was used while in this study, the substrates are fabricated with 150 mm poly-SiC [7]. The buried oxide and silicon substrate is replaced by a thin polycrystalline silicon layer (originally deposited as amorphous silicon) and a poly-SiC substrate (Fig. 1). By wafer bonding and simple MOS-processing techniques, the substrates were realized and thermal and electrical characterization was performed to evaluate the substrate. Initial electrical and thermal measurements are found in [7]. For comparison, low resistivity SOI-wafers (Okmetic) were used, which are optimized to reduce substrate losses in high power RF-transistors. For the first time, we will here present electrical and RF-measurements of LDMOS transistors on the hybrid Si/SiC-substrate.

3. Experimental

150 mm poly-SiC wafers (Saint Gobain) were mechanically lapped followed by a low pressure CVD deposition of 1 µm amorphous silicon. The silicon layer was polished by chemical mechanical polishing to a thickness of 0.5 µm for a high quality bond surface. For the crystalline silicon device layer, SIMOX wafers (Ibis) were used with a device layer thickness of 5 µm. The device layer was thinned down to 3 µm by oxidation and etching to match the thickness of the SOI reference wafers. The wafers were rendered hydrophilic in acid solution, megasonically rinsed in de-ionized water and brushed, and spin-dried. They were then contacted in a wafer bonder. A novel rapid thermal annealing step was applied before the furnace anneal in order to reduce stress and breakage. After the following furnace anneal the silicon handle and the buried oxide was etched away in tetramethyl ammonium hydroxide (TMAH) and hydroflouric acid solution. LDMOS-transistors and other electrical and thermal test structures were processed on the Si/SiC hybrid substrate and on the SOI reference substrate. The process included LOCOS isolation, n+-poly gates and a gate oxide thickness of 300 Å. Diodes were characterized (IV) as well as capacitance-voltage (CV) on MOS-capacitors [7], while IV and RF-behaviour was characterized for the LDMOS-transistors.

4. Results and discussion

Photographs of a final hybrid Si-on-poly-SiC wafer and another processed wafer are shown in Fig. 2. Previous results [6] from Raman spectroscopy and XRD showed that the silicon device layer on the hybrid substrate is stress-free. Diodes and capacitors were measured to characterize the device layer which indicated some recombination and lifetime issues but a good oxide interface with a low density of traps [7].

Measurements of MOSFET output characteristics (Fig. 3) show that the substrates are similar in electrical performance emphasizing that the effective gate length only affected the transconductance for shorter gate lengths. Ideal long channel behaviour was observed which indicate good surface quality and inversion mobility for both substrates. LDMOS transistors were also measured on both substrates and the output characteristics can be seen in Fig. 4. Short channel effects are represented by constant transconductance and high linearity. The transconductance is almost 2x higher for the Si/SiC hybrid although the saturation threshold voltage is similar at 2.42 V for the SOI reference and 2.31 V for the Si/SiC hybrid.

RF-behaviour can be seen in Fig. 5, where the equivalent parallel resistance extracted from the admittance parameters is plotted for the substrates as well as an ordinary commercial SOI-wafer (Soitec) and our old BaSiC-substrate [1]. The results show lower losses for the 150 mm Si/SiC hybrid wafer compared to the LR-SOI.

4. Conclusions

We have presented a method to form 150 mm Si-on-poly-SiC substrates without any intermediate oxide layers [5]. The substrates are void-free and the device layer is stress-free.

For the first time, LDMOS transistors has successfully been fabricated on our Si-on-poly-SiC hybrid substrate with improved or equal electrical performance compared to a low resistivity SOI wafer. Since the transconductance is similar for the MOSFETs and not for the LDMOS transistors, the p-base doping may differ between the substrates giving the Si/SiC hybrid a shorter effective gate length.

From the RF-measurement in can be concluded that trenches need to be incorporated between the devices and pads to reduce the losses in the silicon device layer so that only the losses in the substrate can be measured.

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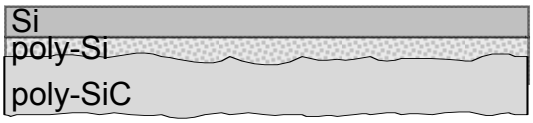
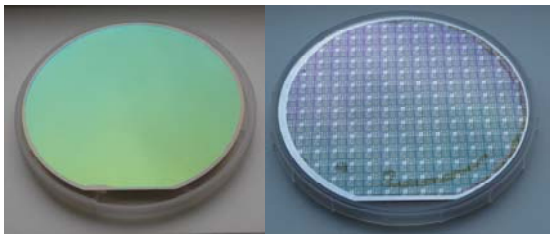


Fig.1: *Schematic cross-section of the hybrid wafer.*



(a) (b)

Fig.2: *(a) Photograph of a 150 mm Si–on-poly-SiC wafer and (b) the fully processed wafer.*

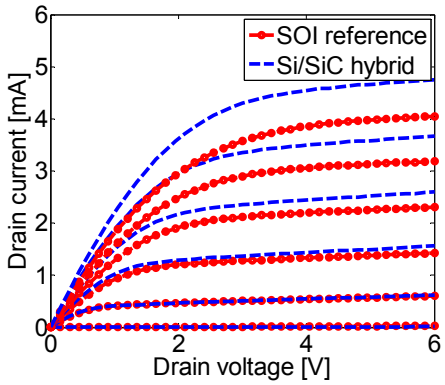


Fig.3: MOSFET *output characteristics for the SOI reference and Si/SiC hybrid substrate. Gate voltage is applied from 0 to 5 V, 1 V/step. L_g=2 µm and L_w=20 µm.*

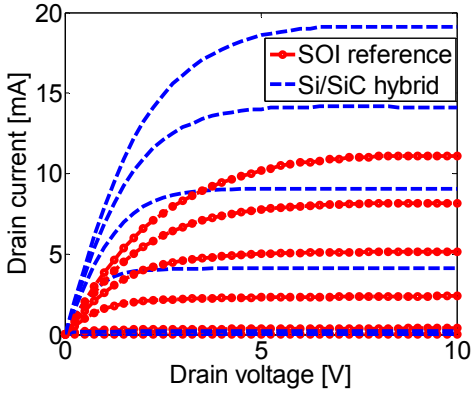


Fig.4: *LDMOS output characteristics for the SOI reference and Si/SiC hybrid substrate. Gate voltage is applied from 0 to 10 V, 2 V/step. L_g=2 µm and L_w=50 µm.*

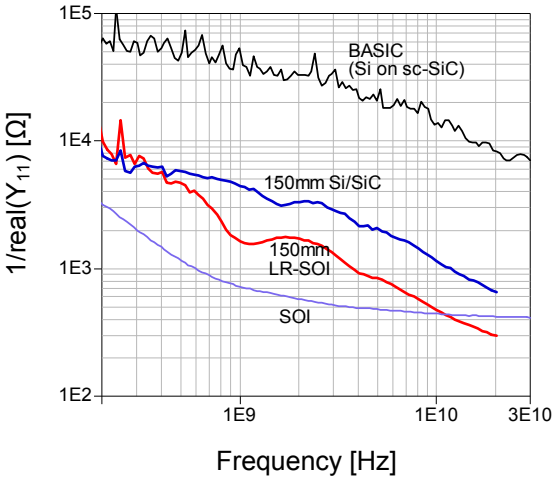


Fig.5: *Equivalent parallel resistance versus frequency for various substrates. Device layer thicknesses are d_{BASIC}=0.3 µm, $d_{Si/SiC}$=3 µm, $d_{LR\text{-}SOI}$=3 µm and d_{SOI}=0.3 µm.*

Lateral Transient Voltage Suppressor for SOI Technologies

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1. Abstract

The study of the behaviour of a lateral punch-through TVS (Transient Voltage Suppressor) device addressed to on chip protection against ESD (ElectroStatic Discharge) in SOI technology is reported in this paper. The improvement of the TVS electrical performances inherent to SOI technologies is described. The inclusion of a field plate, connected to the collector for better control of the breakdown voltage is analysed and compared with Bulk counterparts. Low voltage breakdown values achieved by implementing the field plate are less sensitive to technology fluctuations than the equivalent TVS devices integrated on Bulk substrates.

2. Introduction

Due the reduction of the minimum feature size and the voltage supply of the integrated circuits, new isolation techniques based on dielectric material have been deeply studied. The use of Silicon-on-Insulator (SOI) substrates provides a vertical dielectric isolation and a lateral isolation with the implementation of shallow trenches deep enough to contact the buried layer. Today SOI substrates are used in most of the microelectronics fields, especially in low voltage applications where protections against voltage transients are mandatory. Zener diodes are commonly used in power supply values higher than 5 V. However, the leakage current of Zener diodes dramatically increases for power supply values in the range of 2-5 V. Transient Voltage Suppressor (TVS) devices based on a punch-through breakdown where introduced to cover these voltage range. Although the first TVS devices were integrated in a vertical architecture, their lateral version (LTVS) has to be implemented in advanced deep submicron technologies. A study of the LTVS device performances to be integrated on Ultra-Thin SOI technologies is carried out in this paper.

3. SOI LTVS structures

The schematic cross-section of a four layer LTVS device integrated on Ultra-Thin SOI technology is shown in Fig. 1. The voltage capability of the LTVS is determined by the punch-through between anode and collector as a consequence of the depletion of the low doped P-type layer and the P^+ buffer. Simulations performed with Silvaco have shown that the behaviour of LTVS structures in Thick and Thin SOI substrates is similar than in Bulk LTVS. On the contrary, LTVS structures implemented on Ultra-Thin SOI substrates exhibit a significantly different behaviour. This can be observed in Fig. 2, where the I-V characteristics as a function of D_{epi} of four layer LTVS structures implemented on different active layer thickness. It can be clearly inferred from Fig. 2 that the breakdown voltage value decreases with the thickness of the active layer. The implementation of a polysilicon field plate, as shown in Fig. 3 allows a breakdown voltage reduction. As a consequence, the bipolar base width can be wider since the punch-through voltage will be mainly determined by the field plate length according to the modification of the depletion region at the Silicon surface. Thus, the punch-through voltage value decreases with the increase of the field plate length, at a given bipolar base width, as it can be inferred from Fig. 4. The comparison between Bulk LTVS structures (three and four layers) and four layer SOI LTVS structures without field plate is shown in Figs. 5 and 6. Identical relationship between Clamping and Breakdown voltages has been imposed in order to compare devices with protection capability as similar as possible (Fig. 5). These three and four layer LTVS devices with identical protection capability have to be implemented by using different buffer doping level, to tune the V_{cl} value, and also with different bipolar base width (W_{eff}), to tune the V_{bd} value. In these conditions, Fig. 6 shows that SOI LTVS structures exhibit less sensitivity against W_{eff} variations, leading to a less complex process technology when LTVS devices are integrated on SOI substrates.

4. Conclusions

The simulated electrical characteristics of four layer punch-through TVS structures in SOI substrates have been analysed and compared with their Bulk counterparts. This analysis reveals that punch-through TVS structures in Ultra-Thin SOI technology exhibit better performances than in Thick and Thin SOI, reducing both leakage current and breakdown voltage. The insertion of a field plate, connected with the collector, allows a reduction of the breakdown voltage. Therefore, a wide range of breakdown voltage values can be obtained just varying the length of the field plate

while maintaining the doping profiles. Finally, a reduction of the complexity in the fabrication process is achieved due to the minimised sensibility of the breakdown voltage against W_{eff} variations in SOI substrates.

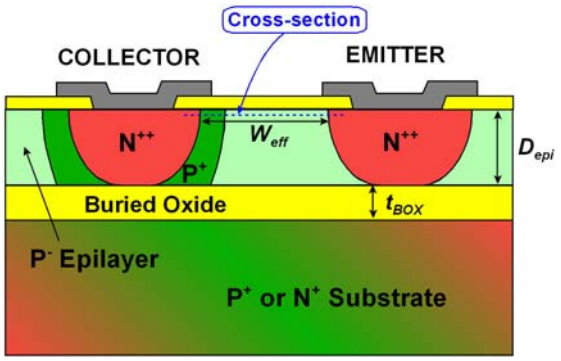

Fig. 1. *Lateral 4-layer TVS Structure on SOI technology.*

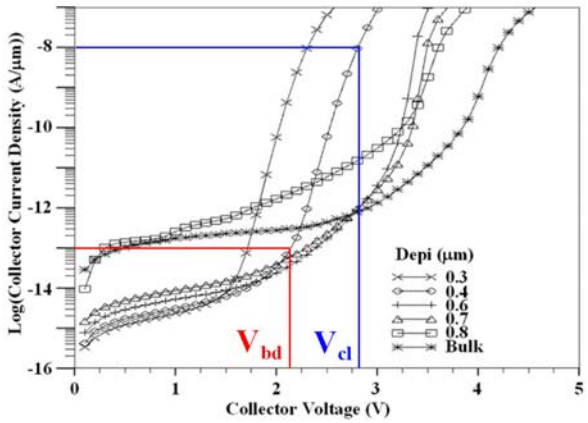

Fig. 2. *I-V characteristics as a function of D_{epi} of lateral four layers TVS devices in SOI technology. W_{eff} = 1.7 μm, N_{epi} = 5e15 cm^{-3}, N_b=5.2e16 cm^{-3} and T_{box} = 1μm*

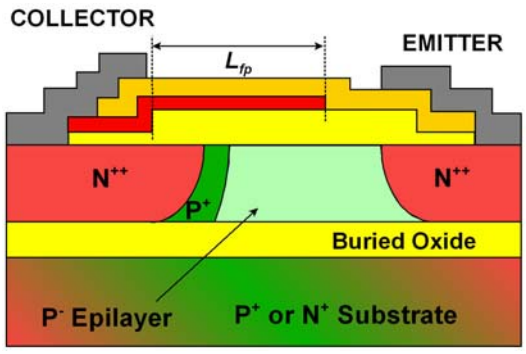

Fig. 3. *Lateral TVS structure with field plate.*

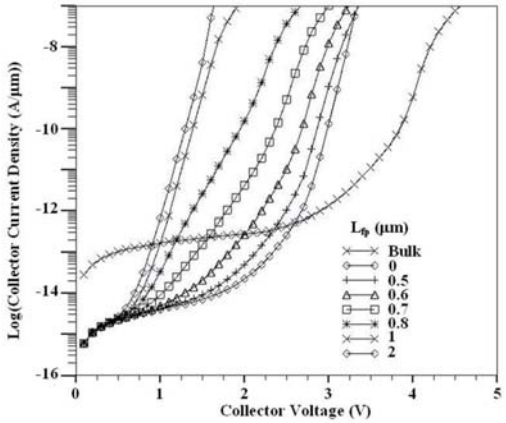

Fig. 4. *I-V characteristics as a function of L_{fp}. W_{eff} = 1.4 μm, N_{epi} = 5e15 cm^{-3}, N_b = 5.2e16 cm^{-3}, D_{epi} = 0.5 μm and T_{box} = 1 μm.*

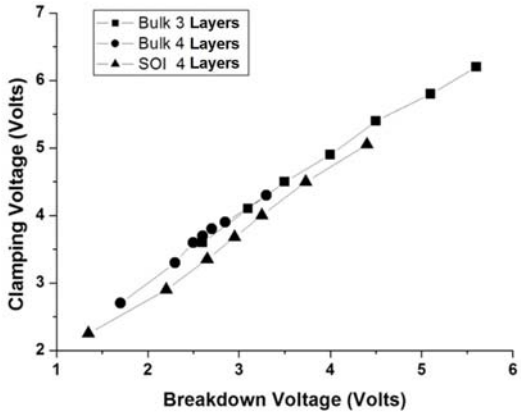

Fig. 5. *Clamping voltage vs. Breakdown voltage of different LTVS structures.*

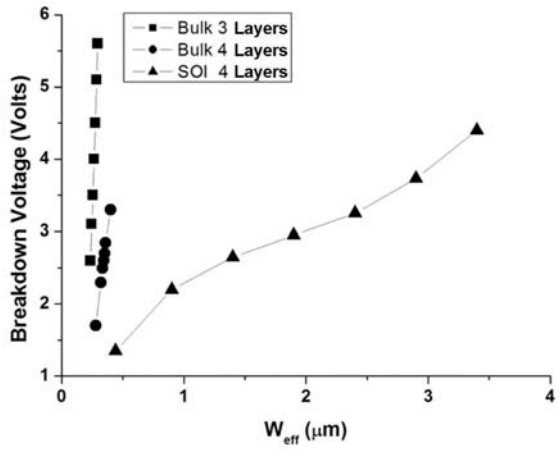

Fig. 6. *Breakdown voltage vs. W_{eff} of different LTVS structures.*