INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

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D4.13. First motivated list of selected topics for future research on SOI technology. Outcome of the panel discussion held during the 6th EUROSOI Workshop Grenoble, 25-27 January, 2010

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PP	Restricted to other programme participants (including the Commission Services)	
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1.- Introduction.

One of the goals of EUROSOI+ project is the promotion of industrial participation in EUROSOI activities and the coordination of the initiatives so that European Industry successfully faces Roadmap-identified challenges

In the first stage of EUROSOI network (2003-2006), we have carefully studied the situation of SOI technology in Europe, we have identified the current status, where we want to go, and what is the best approach ("road") to follow. Now it is time for movement. SOI community has to face and successfully achieve, in the following years, the challenges identified in the Roadmap.

EUROSOI+ will not duplicate works and actions undertaken in other projects, but will, through a forum linking technologists, scientists, designers and industry:

1. Promote industrial participation in the Network activities, informing industry about relevant progress in SOI technology worldwide and providing a feedback loop for industrial mid and long-term interests to academic and research centres.
2. Organize annual workshops, scientific meetings and discussion panels with industry experts (Tyndall-2008, Chalmers-2009, Grenoble-2010 and Granada-2011)
3. Upgrade the EUROSOI State-of-the-Art Report.
4. Upgrade the European SOI Roadmap: Identify scientific priority areas, and formulate research and development strategies.
5. Promote the interaction between existing SOI projects at national and European level (FP6-IST, FP7-ICT, EUREKA/MEDEA/CATRENE, ENIAC), and facilitate the coordination of their work. Organization of Workshops and scientific meetings.
6. Foster the initiatives to face the challenges already identified in EUROSOI Roadmap, by selecting and creating the research consortium from the best European actors already identified at EUROSOI "Who is Who" guide. Co-ordinate activities at national and European level.
7. Co-ordinate activities with other FP7 instruments: NoEs, IPs, Marie-Curie initiatives.
8. Address and foster initiatives beyond CMOS: take advantage of the SOI knowledge to develop platforms for further technological development in nanotechnology, such as to prepare the transition from microelectronics to nanoelectronics.
9. Propose a list of highly desirable topics of advanced research on SOI by analyzing the future trends in industry and research.

To fulfill this goal, EUROSOI will organize panel discussions with different specialists on SOI technology to identify hot topics in SOI research. These discussion panels will be held simultaneously with each EUROSOI workshop. As outcome of these panel discussions, a report with a list of selected topics in SOI research will be elaborated.

The third Workshop and Scientific meeting organized by EUROSOI+ project was held on January 25-27, 2010 in MINATEC, Grenoble, France. During this Workshop, the panel discussion, chaired by Prof. Raphael Clerc, was held on Tuesday, January 26th. The following five SOI experts were invited to participate in the discussions:

1. Dr. Horacio Mendez, SOI Industry Consortium, USA
2. Dr. Christophe Tretz, IBM, USA
3. Dr. Frederic Boeuf , STMicroelectronics, Crolles, France
4. Dr. Jan Hoentschel, GlobalFoundries, Dresden, Germany
5. Prof. Jean-Pierre Colinge, Tyndall, Cork, Ireland
6. Prof. Krishna Saraswat, Stanford University, Stanford, USA

Each expert presented his point of view and position on the SOI technology, future applications, and the European situation. The leading thread of this year's debate was "**SOI Technologies: What kind of research for what kind of products?"**

After the initial positioning, there was a long and live debate among the panellists and the rest of the audience. This debate was useful to identify the hot topics and concerns of European researchers and how we could contribute to improve the situation.

The details of the Panel are described in the next sections.

2.- Panel discussion participants.

1) Dr.Horacio Mendez − SOI Industry Consortium, (USA)

Prior to joining the SOI Industry Consortium as the Executive Director, Horacio Mendez was most recently the Director of New Product Development at Freescale Semiconductor. He is one of the industry's key experts in SOI technology with broad experience in manufacturing as well as technology roadmap development and strategic planning. Prior to Freescale, he held various positions at Motorola, including Director of Device Engineering Wireless Technologies where he was responsible for the development and successful commercialization of all RF and Analog/Mixed Signal technologies.

2) Dr. Christophe Tretz − IBM, San Jose (USA).

Christophe Tretz received the B.Sc. degree from the Ecole Nationale Superieure d'Electronique, Electrotechnique, Informatique et Hydraulique de Toulouse (ENSEEIHT), France, in 1991, and the M.S. and Ph.D. degrees in electrical engineering from the Columbia University, New York, in 1992 and 1997, respectively. In 1997, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, and contributed to the design of several microprocessors for servers and workstations both with bulk and SOI processes. In 2000, he joined Advanced Micro Devices with the California Microprocessor Division, as a Member of the Technical Staff, contributing to the design of the Hammer microprocessor family, and establishing design guidelines for microprocessor using SOI technologies. In mid 2003, he went back to IBM Engineering & Technology Services as a Senior Development Engineer. He is currently in charge of the development and business strategy of a developer's platform using Cell. He has authored or coauthored about 33 papers and 3 U.S. patents in the field of circuit-design techniques using SOI, circuit optimization, and low power design. His current research interests remain in optimizing circuit design for SOI and in improving design choices for SOI. Dr. Tretz has been part of the organizing committees of the IEEE International SOI Conference since 1998 and was the Conference General Chair for 2006.

3) Dr. Frederic Boeuf − STMicroelectronics, Crolles (France)

4) Dr. Jan Hoentschel − Global Foundries, Dresden (Germany)

Jan Hoentschel received the Dipl.-Ing. degree and the Ph.D. degree in electrical engineering in 2000 from the University of Applied Sciences Dresden and in 2004 from the Technical University Dresden, Germany, respectively. During his research, from 2000 to 2004 at the University of Applied Science Dresden, he was engaged in simulations of quantum-sized devices, III-V semiconductors as well as the modeling of quantum transport phenomena in nanostructures. From 2004 to 2008 he was working for Advanced Micro Devices and served several

PD-SOI-CMOS device integrations from 130nm down to 45nm technologies for high performance microprocessors. Since 2009 he is with Globalfoundries and currently responsible for 32/28nm low power technologies. His research interests include strain engineering, asymmetric implantations and low power technologies on CMOS devices. Mr. Hoentschel is author and co-author of numerous technical papers and patents in the semiconductor field. He holds the 2000 VDE award of the German Association for Electrical, Electronic and Information Technologies (VDE) for an excellent diploma thesis.

5) Prof. Jean Pierre Colinge − Tyndall National Institute, Cork (Ireland)

Prof. Colinge is head of the Ultimate Silicon Devices Research Group at Tyndall National Institute in Cork. He was professor of Electrical Engineering at the University of California, Davis (USA) from 1997 to 2006. He received a BS degree in Philosophy, the Electrical Engineer degree, and the Ph.D. degree in Applied Sciences from the Université Catholique de Louvain, Louvain-la-Neuve, Belgium, in 1980, 1980, and 1984, respectively.

From 1981 to 1984 he was Researcher at the Centre National d'Etudes des Télécommunications (CNET), Grenoble, France, where he developed early for the fabrication of SOI films and developed the "Stacked CMOS" technique (one of the first 3D structures). From 1985 to 1988 he was member technical staff of the Hewlett-Packard Research Labs, Palo Alto, CA, where he carried out research and development work on thin-film SOI devices and discovered many of the properties of fully depleted SOI devices (sharp subthreshold slope, absence of kink effect, properties of transconductance, etc.) From 1988 to 1991 he was project leader for the SOI research at IMEC (Inter University Microelectronics Center) in Leuven, Belgium. He designed and fabricated novel SOI devices, including radiation-hard devices and the first double-gate SOI transistors. From 1991 to 1997 he was Professor at the Université Catholique de Louvain, heading research in the areas of SOI device physics and technology, high-temperature SOI integrated circuits, radiation-hard integrated SOI circuits, quantum effects (2D,1D) in SOI devices, microwave SOI devices, and low-power SOI circuits. He is currently carrying research in advances multiple-gate SOI MOSFET device physics.

He has been on the committee of several conferences, including IEDM and SSDM, has been General Chairman of the IEEE SOS/SOI Technology Conference in 1988, and is a Fellow of IEEE. He has published over 250 scientific papers and three books on the field of SOI as well as two books on semiconductor device physics and four book chapters on SOI. Dr. Colinge has given lectures on SOI at short courses offered by various conferences, including IEDM, NSREC and the IEEE International SOI Conference.

6) Prof.Krishna Saraswat, Standford University (USA)

Prof. Saraswat received his B.E. degree in Electronics in 1968 from the Birla Institute of Technology and Science, Pilani, India, and his M.S. and Ph.D.

degrees in Electrical Engineering in 1969 and 1974 respectively from Stanford University, Stanford, CA. Professor Saraswat stayed at Stanford as a researcher and was appointed Professor of Electrical Engineering in 1983. He serves on the leadership council of the MARCO/DARPA-funded Focus Center for Materials, Structures, and nano-Devices. He also has an honorary appointment of an Adjunct Professor at the Birla Institute of Technology and Science, Pilani, India since January 2004 and a Visiting Professor during the summer of 2007 at IIT Bombay, India.

Professor Saraswat research interests are in new and innovative materials, structures, and process technology of silicon, germanium and III-V devices and interconnect for VLSI and nanoelectronics. Special areas of his interest are: new device structures to continue scaling MOS transistors, DRAMs and flash memories to nanometer regime, 3-dimentional ICs with multiple layers of heterogeneous devices, ultrathin MOS gate dielectrics, and metal and optical interconnections.

During 1969-70, he worked on microwave transistors at Texas Instruments. Returning to Stanford in 1971, he did his Ph.D. on high voltage MOS devices and circuits. After graduating he joined Stanford University as a Research Associate in 1975 and later became a Professor of Electrical Engineering in 1983. For the next 15 years, Prof. Saraswat worked on modeling of CVD of silicon, conduction in polysilicon, diffusion in silicides, contact resistance, interconnect delay and 2-D oxidation effects in silicon. He pioneered the technologies for aluminum/titanium layered interconnects, CVD of tungsten silicide MOS gates, CVD tungsten MOS gates and tunable workfunction SiGe MOS gates. During the late 80's he became interested in the economics and technology of single wafer manufacturing. He developed equipment and simulators for single wafer thermal processing, deposition and etching and technology for the in-situ measurements and real-time control. Jointly with Texas Instruments a microfactory for single wafer manufacturing was demonstrated in 1993. Since the mid 90's Prof. Saraswat has been working on new materials, devices and interconnects for scaling MOS technology to sub-10 nm regime. He has pioneered several new concepts of 3-D ICs with multiple layers of heterogeneous devices. His group has recently demonstrated the first high performance germanium MOSFETs with high-k dielectrics and high efficiency optical detectors in germanium integrated on silicon. During 2000-2008 he also did research on Environmentally Benign Semiconductor Manufacturing.

Prof. Saraswat has graduated 70 doctoral students and has authored or co-authored over 620 technical papers, of which six have received Best Paper Award. He is a Fellow of the IEEE, and a member of both The Electrochemical Society and The Materials Research Society. He received the Thomas Callinan Award from The Electrochemical Society in 2000 for his contributions to the dielectric science and technology, the 2004 IEEE Andrew Grove Award for seminal contributions to silicon process technology, Inventor Recognition Award from MARCO/FCRP in 2007 and the Technovisionary Award from the India Semiconductor Association in 2007. He is listed by ISI as one of the 250 Highly Cited Authors in his field.

3.- Panel Discussion ideas – SOI technologies: What kind of research for what kind of products?

The panel discussion was organized with the following scheme. The Chair had previously asked the panellists to list key issues in SOI technology from two points of view:

a) What products will be the next SOI market?
b) What kind of research is needed in the short and long term related to SOI?

Each panellist introduced his point of view about SOI technology in 5−6 slides during 10 minutes. They explained and documented their feelings from their own experience, by focussing on the following points: what is needed to improve the current situation, what is being done well, what is not being done so well, and what we need to improve.

The chair of the Session, Dr. Clerc, distributed among the panellists and the attendants the following poll:

1) What is going to be the next big SOI market?

    a. Fully depleted SOI for high performance applications?
    b. Fully depleted SOI for low power applications?
    c. SOI for 3D integration?
    d. SOI for RF circuits?
    e. SOI for Microsystems?
    f. SOI for power electronics?
    g. SOI for LED?
    h. Wave Guide on SOI?
    i. Organization of conference for SOI experts?
    j. Others (specify)

2) What kind of research for SOI next big market?
    a. Massive industrial technological R&D ?
    b. Smart circuit design?
    c. Academia creativity?
    d. Innovative marketing?
    e. Other (specify)

Christophe Tretz's answers:

1) Working on high performance processors. Design of computing blocks within the processors of gaming applications (e.g.: Xbox 360)

2) Research has to be cheap, highly efficient and practical, and very innovative to accommodate the needs for optimum performance.

Frederic Bouef's answers:

1) System-on-chip (SoC) age: wireless and mobility. So the needs are:
   a. High speed at lower power consumption.
   b. RF/analog capability

2) Research on circuit design is strongly required for the following years, but it must fulfil high performance and low stand-by power. UTBSOI has a very interesting future for 22nm and below. Hence, Extra-Thin SOI and Hybrid SOI are topics of interest.

Horacio Mendez's answers:

1) SOI Markets:
   a. **Short term**: Mobile internet computing is the next big market. The traffic of mobile video is growing dramatically. The profits can be huge for the winners. It also means a technology challenge (increasing memory capacity and fulfilment of mobile power specifications) due to the increasing integration of applications. It will be necessary:
      i. Lots of memory (embedded DRAMs).
      ii. Much lower power consumption at the same supply voltage to keep up with the density.
      iii. Heterogeneous integration of technologies (sensors, digital, RF).

   b. **Long term**: Convergence of Electronics and Medicine to provide non-invasive assessment or corrective procedures.

2) Research on circuit design on SOI. Full integration of Sensors+Processors+RF at very low power is the market for future.

Jan Hoentchel's answers:

1) Low power devices and applications will be 80% of the market for mobile and low cost applications. At the same time high performance is important and should be maintained.

2) Research on circuit design. Keep scaling trend and packaging different applications and process in the same chip.

Jean-Pierre Colinge's answers:

1) SOI Markets:
   a. Killer application is something changing. Currently SOI represents 34.8% of the total logic market. Entertainment applications (gaming consoles, TVs, etc.). The main advantage of SOI comes from LP performance, and that is its biggest potential.

b. Next SOI market: Mobile, low-power systems (maybe using solar cell as single power supply).
c. SOI Industry consortium survey:
Why is SOI important for your business?
i. Power savings (46%)
ii. Higher performance (21%)
iii. More reliable (2%)
iv. All the above (23%)
v. Other (8%)

2) More education to support SOI adoption.

Krishna Saraswat's answers:

1) SOI Markets:
a. Different applications need different devices (bulk, single-gate SOI or double-gate SOI) with specific characteristics (Ion, Ioff, delay, high CV/I, etc).
b. Some areas of interest in short term: 1T-DRAM for embedded memories is an interesting topic, 3D-ICs, SOI technology is key to both bonding and monolithic 3D technologies.

2) Academic creative is the research needed. An example: Tunnel transistors, IMOS, nanomechanical switch - can they beat the MOSFET subthreshold-swing-limit of 60mV/decade?

4. Conclusions and list of topics

After the initial positioning, there was a long and very live debate among the panellists and the rest of the audience. Prof. James B. Kuo from National Taiwan University manifested that the main problem of “SOI for business” is yield, and he wondered how we could improve the yield of SOI compared to bulk devices. Horacio Mendez answered that there’s no difference between SOI and bulk with regards to yield, and he cited the ARM1176 experience. Finally, he added that mobile Internet devices will create one of the largest semiconductor demands in history. To successfully face these demands, technology will have to provide stable high-density memory and very low power consumption. SOI technology provides viable solutions to these challenges:

1. Partially-Depleted SOI with a proven +40% power reduction (ARM 1176 data). This power reduction is important for Networking applications.
2. The significantly reduced variability of FD SOI is a practical solution for mobile (low-power) applications.

However, the main drawbacks are

1. the lack of available IP for SOI foundry offerings,
2. the lack of education on SOI design.

These problems become a barrier to broad adoption of SOI.

In summary, SOI technology can provide significantly higher chip performance improvement and extraordinary power reduction compared to standard bulk silicon technology, and is used broadly today in applications ranging from enterprise servers to consumer game consoles. But, more importantly, SOI is now moving to other markets dedicated to low-power and mobile Internet applications. For the success of these new markets two important tasks have to be addressed:

i) Make public already available existing IP on SOI.

ii) Train designers on how to design with SOI but also on how they can access the IP and the advantages of SOI.