INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

Grant Agreement nº 216373

D5.9 Report on promotional activities for the use of EUROSOI design and prototyping platform during second reporting period

Due date of deliverable: 28-02-2010
Actual submission date: 28-02-2010

Start date of project: 01-01-2008 Duration: 39 months

Project coordinator: Prof. Francisco Gámiz, UGR
Project coordinator organisation: University of Granada, Spain Rev.1

Table of contents

Project co-funded by the European Commission within the Seventh Framework Programme (FP7)		
Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

1.- Introduction.

2.- Promotion of the FDSOI technology.

1.- Introduction.

Technical promotion of SOI technologies is clearly one of the biggest goals of EUROSOI+. As the FDSOI platform is also a main achievement of this project, CEA-LETI and possibly other partners from EUROSOI+ will visit European IC and Fabless companies in order to promote the FDSOI technology and the work done in the frame of EUROSOI+. Such promotion will outline the potentialities of this technology, as well as the new circuit design opportunities and applications that will be raised during the meetings. Target companies are ARM, AMD, ST, Qimonda, Innovative Silicon, Nokia, etc... Two visits per year are programmed and budgeted (A total budget of 3600€ (600€ per visit) are allocated to cover travel costs and subsistence expenses of visitors). At the end of every year, a report explaining the activities developed during the visits, the companies visited and the outcomes of the visits will be delivered (D5.8, D5.9 and D5.10).

2.- Promotion of the FDSOI technology.

According to Task 5.1 LETI has provided already processed Fully Depleted SOI devices (fabricated on ultra-thin SOI films and coupled with high-K and metal gates) to EUROSOI partners.

In addition to the already provided wafers by LETI (to UCL, IMEP and UGR), FDSOI wafers with functional devices have been provided to the following EUROSOI+ partners during 2009:

- R. Ritzentaler and B. Iniguez (Tarragona University). Two Wafers with various SOI thicknesses.

- Sorin Cristoloveanu (IMEP, Grenoble). Additional wafers.

Promotion of the FDSOI technology is one of the most important goals of EUROSOI+. During 2009, several events and workshops have been organized by CEA-LETI in order to promote this technology:

- During the LETI annual review (in June 2009), a specific presentation has been made by Olivier Faynot in order to make a status of this technology at LETI and present the state of the art of the Research dedicated Design Kit.
- In the frame of the 2009 VLSI symposium, held in Kyoto, Olivier Faynot had the opportunity to participate to the evening rump session. The rump session was focussed on 'The Key technology options for sub 20nm nodes'. Panel members were: Raj Jammy from SEMATECH, Wilfried Haensch from IBM, Dr; Kita from University of Tokyo, Dr. Uchida from TITECH, Clement Wann from TSMC and Olivier Faynot from LETI. This was a good opportunity for LETI to highlight the advantages of FDSOI for sub-20nm nodes.
- A FDSOI workshop has been co-organized in Leuven from October 15-16th 2009, by the SOI Consortium and IMEC. This workshop was dedicated to the promotion of the FDSOI technology for the industrial companies that are more focussed on Bulk and FinFET technologies. Several international speakers were invited. For Europe, the contributors were: Pierre Fazan (from Innovative Silicon), Daniel Delprat (from SOITEC) and Olivier Faynot (from LETI). The agenda of this meeting was:

FD SOI ARCHITECTURE, TECHNOLOGY PLATFORM FOR LOW POWER APPLICATIONS FOR 22nm AND BEYOND

When/Where: Friday Oct 16, Leuven, Belgium
9:00-17:00 - WORKSHOP SESSIONS - IMEC auditorium
17:00-20:00 - NETWORKING RECEPTION - IMEC entrance hall

Agenda	Speaker	Topic	Affiliation
9:00 - 9:10	Luc Van den hove	Opening remarks	IMEC
9:10 - 9:40	Ghavam Shahidi	Fully Depleted SOI Technology for 22 nm and beyond	IBM
9:40 -10:10	Nobuyuki Sugii	Hybrid SOI and bulk integration	Hitachi
10:10 - 10:40	Daniel Delprat	UTSOI and UTBOX wafer readiness	Soitec
10:40 - 11:00	coffee break		
11:00 - 11:30	Tsu Jae King	SRAM yield enhancement with FDSOI	UCB
11:30 - 12:00	Pierre Fazan	ZRAM for embedded and stand alone applications	ISi
12:00 - 12:30	Horacio Mendez	FinFET case study: SOI vs. bulk	SOI Consortium
12:30 - 14:00	Lunch		
14:00 - 14:30	Olivier Faynot	Planar FDSOI technology: performance and perspectives	CEA-LETI
14:30 - 15:00	Bora Nikolic	Porting designs to FDSOI	UCB

15:00 - 15:30	ARM Representative	ARM 1176 implementation in SOI 45 nm and outlook	ARM
15:30 - 15:50	coffee break		
15:50 - 16:20	Mike Jacob	Signal integrity analysis in a cell based SOI design	Cadence
16:20 - 16:50	Phil Watson	Design methodology and tools for SOI based products	Synopsys
16:50 - 17:00	Horacio Mendez	Closing remarks	SOI Consortium

- After IEDM conference in Baltimore, a second FDSOI workshop has been co-organized (on December 9th) by the SOI Consortium and LETI. The goal was the same as the previous workshop. This meeting was a good opportunity to expose ARM company to the recent FDSOI results. ARM was one of the company targeted to be exposed to the FDSOI results. The agenda was the following:

  6:00pm Reception
  6:40pm Opening remarks (Dr. C. Mazure, Soitec)
  6:45pm FDSOI Highlights of the IEDM 2009 (Dr. O. Faynot)
  7:00pm ETSOI substrate readiness for FDSOI (Dr. B. Doris, IBM)
  7:15pm Models for FDSOI: BSIM, SPICE (Prof. C. Hu, UCB)
  7:35pm FDSOI Benefits for SRAM at the 22nm Node (Prof. T.J. King, UCB)
  7:55pm ARM 1176 implementation in SOI 45nm technology and silicon measurement and outlook towards FDSOI (Dr. Greg Yeric, ARM)
  8:15pm SOI Digital Implementation & Electrical Signoff (M. Jacobs, Cadence)
  8 :35pm Wrap up (H. Mendez, SOI consortium)
  8:40pm Discussion, networking and drinks, ends at 9:15 pm

From Europe, the speakers were Carlos Mazure from SOITEC, Greg Yeric from ARM and Olivier Faynot from LETI.

- In the frame of the DECISIF project, the most recent FDSOI technology developments have been presented in Dresden (Global Foundries site), in front of the project partners: ST, SOITEC, SILTRONIC, MPI Halle, Juelich. This was a good opportunity to expose Global Foundries (ex AMD) to the FDSOI results. Compared to AMD, Global Foundries is now interested in Low Power technology and in this objective, they were interested in the presented results.
- During the EUROSOI 2010 workshop, a working group meeting has been organized and Carlo Reita (LETI) presented the status of the FDSOI platform. Outcomes of this meeting are summarized in deliverable D5.3.
- Technology and electrical results have been also presented to ST Microelectronics and SOITEC in order to highlight the interest of such technology for Low Power applications. No travel expenses are related to this promotion.
- An article has been written in ‘Advanced Substrates News’, in the Spring 2009 edition. The title is: ‘Leti, Soitec and ST have discovered the sources of threshold voltage variation in undoped, ultrathin FD-SOI

architectures.' It can be read using the following website: http://www.advancedsubstratenews.com/index.php?newsletter=4

The promotion of the technology is also done through the accessibility of the Design Kit developed by LETI. The status of the Design Kit and its associated documentation are summarized in deliverable D5.3, D5.4 and D5.5.

In 2009, the design Kit and its associated doscumentation has been provided to ISEP (in Paris) and UC Berkeley. UCL (Louvain La Neuve) and Innovative Silicon should receive it in the next weeks.
During the EUROSOI 2010 worskhop, LETI announced to the partners the possibility to design some small circuits in the upcoming new LETI testchip called SNOW (see following slide). This new testchip is planed for the end of June 2010.