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COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

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D4.12. Second motivated list of selected topics for future research on SOI technology. Outcome of the panel discussion held during the 5th EUROSOI Workshop Chalmers, 20-21 January, 2009

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1.- Introduction.

One of the goals of EUROSOI+ project is the promotion of industrial participation in EUROSOI activities and the coordination of the initiatives so that European Industry successfully faces Roadmap-identified challenges

In the first stage of EUROSOI network (2003-2006), we have carefully studied the situation of SOI technology in Europe, we have identified the current status, where we want to go, and what is the best approach ("road") to follow. Now it is time for movement. SOI community has to face and successfully achieve, in the following years, the challenges identified in the Roadmap.

EUROSOI+ will not duplicate works and actions undertaken in other projects, but will, through a forum linking technologists, scientists, designers and industry:

1. Promote industrial participation in the Network activities, informing industry about relevant progress in SOI technology worldwide and providing a feedback loop for industrial mid and long-term interests to academic and research centres.
2. Organize annual workshops, scientific meetings and discussion panels with industry experts (Tyndall-2008, Chalmers-2009, Grenoble-2010 and Granada-2011)
3. Upgrade the EUROSOI State-of-the-Art Report.
4. Upgrade the European SOI Roadmap: Identify scientific priority areas, and formulate research and development strategies.
5. Promote the interaction between existing SOI projects at national and European level (FP6-IST, FP7-ICT, EUREKA/MEDEA), and facilitate the coordination of their work. Organization of Workshops and scientific meetings.
6. Foster the initiatives to face the challenges already identified in EUROSOI Roadmap, by selecting and creating the research consortium from the best European actors already identified at EUROSOI "Who is Who" guide. Co-ordinate activities at national and European level.
7. Co-ordinate activities with other FP7 instruments: NoEs, IPs, Marie-Curie initiatives.
8. Address and foster initiatives beyond CMOS: take advantage of the SOI knowledge to develop platforms for further technological development in nanotechnology, such as to prepare the transition from microelectronics to nanoelectronics.
9. Propose a list of highly desirable topics of advanced research on SOI by analyzing the future trends in industry and research.

To fulfill this goal, EUROSOI will organize panel discussions with different specialists on SOI technology to identify hot topics in SOI research. These discussion panels will be held simultaneously with each EUROSOI workshop. As outcome of these panel discussions, a report with a list of selected topics in SOI research will be elaborated.

The second Workshop and Scientific meeting organized by EUROSOI+ project was held on January 20-21, 2009 in Chalmers, Sweden. During this Workshop, the first panel discussion, chaired by Prof. Cristoloveanu, was held on Tuesday, January 20th. The following five SOI experts were invited to participate in the discussions:

1. Dr. Cor Claeys, IMEC, Belgium
2. Dr. Olivier Faynot, CEA-LETI, Grenoble France
3. Prof. Jerry Fossum, University of Florida, Gainesville, USA
4. Dr. Stephen Monfray, STMicroelectronics, France
5. Prof. Francis Balestra, IMEP, Grenoble France
6. Prof. Jean-Pierre Colinge, Tyndall, Cork, Ireland

Each expert presented his point of view and position on the SOI technology, future applications, and the European situation. After the initial positioning, there was a long and live debate among the panellists and the rest of the audience. This debate was useful to identify the hot topics and concerns of European researchers and how we could contribute to improve the situation.

The details of the Panel are described in the next sections.

2.- Panel discussion participants.

1) Dr. Cor Claeys − IMEC (Belgium).

Cor Claeys was born in Antwerp, Belgium. He received the M.S. degree in electrical engineering and the Ph.D. degree from the Katholieke Universiteit Leuven (KU Leuven), Belgium, in 1974 and 1979, respectively. His dissertation focused on the field of process-induced defect characterization for very large scale integration technologies. During 1974–1984, he was a Research Assistant and then a Staff Member of the ESAT Laboratory, KU Leuven, and has been a Professor since 1990. In 1984, he joined IMEC, Leuven, as the Head of the Silicon Processing Group. Since 1992, he has been responsible for technology business development. He coedited the book *Low Temperature Electronics* and authored the book *Radiation Effects in Advanced Semiconductor Materials and Devices*. He has also authored and coauthored six book chapters and more than 600 technical papers and conference contributions. His research interests are general silicon technology for ultralarge scale integration, device physics including low temperature operation, low-frequency noise phenomena and radiation effects, and defect engineering and material characterization.
Dr. Claeys was elected Academician and Professor of the International Information Academy in 1999. He was the Founder of the IEEE Electron Devices Benelux Chapter and elected AdCom Member (1999–2005), of the Electron Devices Society. Presently he is an EDS Distinguished Lecturer and President-Elect of EDS. He is also a member of SEMI and the European Material Research Society, Fellow of the Electrochemical Society, and an Associate Editor for the Journal of the Electrochemical Society.

2) Dr. Olivier Faynot − LETI, Grenoble (France)

Olivier Faynot received the M.Sc and Ph.D. degrees from the Institut National Polytechnique de Grenoble, France in 1991 and 1995, respectively. His doctoral research was related to the characterization and modeling of deep submicron Fully Depleted SOI devices fabricated on ultrathin SIMOX wafers. He joined LETI (CEA-Grenoble, France) in 1995, working on simulation and modeling of deep submicron fully and partially depleted SOI devices. His main activity was the development of a dedicated Partially Depleted SOI model, called LETISOI. Since 2000, he is involved in the development of sub 0.1µm fully and partially depleted technology and other very advanced SOI devices. He is author and co-author of more than 30 scientific publications on SOI in journals and international conferences. Since 2001, Dr. Faynot is on the IEEE International SOI conference Committee.

3) Prof. Jerry Fossum − University of Florida Gainesville, USA

Prof. Fossum was born in Phoenix, AZ. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Arizona, Tucson. His doctoral research was in the area of semiconductor device and integrated circuit (IC) modeling and simulation. During his graduate program, he was a NASA

Predoctoral Trainee, a Graduate Teaching and Research Associate, and an industrial consultant. In 1971, he joined the Technical Staff of Sandia Laboratories, Albuquerque, NM, where he was engaged in various semiconductor device design and modeling activities, including the development of silicon solar cells. In 1978, he moved to the University of Florida, Gainesville, where he is now Professor of electrical and computer engineering. His general area of interest is semiconductor device theory, modeling, and design; his current research concerns physical, process-based device modeling for IC simulation and technology CAD, with emphasis on SOI, double-gate, and bulk-Si CMOS. He is the author or coauthor of more than 200 papers published in technical journals and conference proceedings.
Dr. Fossum is a member of the Honorary Editorial Advisory Board of *Solid-State Electronics*. He was an Associate Editor for the IEEE Transactions on Computer-aided Design from 1988 to 1991, and a Guest Editor for the IEEE Transactions on electron Devices in 1998. In 1983, he was elected a Fellow of the IEEE for “contributions to the theory and technology of silicon solar cells and transistors.” In 1992, he and two of his students received the Best Paper Award at the IEEE International SOI Conference. He served on the Executive Committee of that conference from 1994 to 1997.

4) Dr. Stephen Monfray, STMicroelectronics (France)

Dr. Monfray was born in Lyon, France, in 1975. He received the M.Eng. degree in physics and the postgraduate diploma in microelectronics in 1999 from the Institut National des Sciences Appliquées, Lyon, France, and the Ph.D. degree from the Université de Provence Aix-Marseille I, Marseille, France. He has eight years of experience in the field of advanced device integration. He joined France Telecom R&D in 1999 and worked in collaboration with STMicroelectronics, Crolles, France, on the development and characterization of the silicon-on-nothing technology. After his Ph.D. studies, he was with the Advanced Devices Group, STMicroelectronics, as the Disruptive Devices Project Leader. He was involved in European projects (Nanocmos and Pullnano), and he is driving and managing collaborations with universities and research laboratories and supervises Ph.D. dissertations. He is the author or a coauthor of more than 28 publications in major conferences and journals and of a book chapter. He is the holder of more than 20 patents. Dr. Monfray had multiple participations and paper presentations in the International Electron Devices Meeting in 2001, 2002, 2004, and 2007. He was a corecipient of the Paul Rappaport Award in 2000.

5) Prof. Francis Balestra, IMEP, Grenoble (France)

Prof. Balestra was born in Digne, France, in 1960. He received the B.S. degree from the University of Provence, Marseille, France, in 1981, and the M.S. and Ph.D. degrees in electronics from the Institut National Polytechnique, Grenoble, France, in 1982 and 1985, respectively. In 1989, he received the Habilitation diploma from the INPG, authorizing him to supervise Ph.D. dissertations. He joined the Laboratoire de Physique des Composants a Semiconducteurs

(LPCS), INP Grenoble, in 1982, where he has been involved in research on the characterization, modeling, and simulation of silicon-on-sapphire MOS transistors. He became Charge de Recherche C.N.R.S. (Centre National de la Recherche Scientifique) in 1985. From 1993 to 1994, he was with the Research Center for Integrated Systems, Hiroshima University, Higashi-Hiroshima, Japan, as a Visiting Researcher, and worked on sub-0.1-_m MOSFET's and SIMOX devices. Since 1996, he has been Deputy Director of the LPCS. He led several research teams on deep submicron MOSFET's, silicon-on insulator devices, low-temperature electronics, and polysilicon emitter bipolar transistors for BiCMOS technology. He has supervised 12 research projects.
He has coauthored more than 60 publications in international scientific journals and 100 communications at national and international conferences. Dr. Balestra was the organizer of the 1st European Workshop on Low-Temperature Electronics (WOLTE), Grenoble, France, June 1994.

6) Prof. Jean Pierre Colinge − Tyndall National Institute, Cork (Ireland)

Prof. Colinge is head of the Ultimate Silicon Devices Research Group at Tyndall National Institute in Cork. He was professor of Electrical Engineering at the University of California, Davis (USA) from 1997 to 2006. He received a BS degree in Philosophy, the Electrical Engineer degree, and the Ph.D. degree in Applied Sciences from the Université Catholique de Louvain, Louvain-la-Neuve, Belgium, in 1980, 1980, and 1984, respectively.

From 1981 to 1984 he was Researcher at the Centre National d'Etudes des Télécommunications (CNET), Grenoble, France, where he developed early for the fabrication of SOI films and developed the "Stacked CMOS" technique (one of the first 3D structures). From 1985 to 1988 he was member technical staff of the Hewlett-Packard Research Labs, Palo Alto, CA, where he carried out research and development work on thin-film SOI devices and discovered many of the properties of fully depleted SOI devices (sharp subthreshold slope, absence of kink effect, properties of transconductance, etc.) From 1988 to 1991 he was project leader for the SOI research at IMEC (Inter University Microelectronics Center) in Leuven, Belgium. He designed and fabricated novel SOI devices, including radiation-hard devices and the first double-gate SOI transistors. From 1991 to 1997 he was Professor at the Université Catholique de Louvain, heading research in the areas of SOI device physics and technology, high-temperature SOI integrated circuits, radiation-hard integrated SOI circuits, quantum effects (2D,1D) in SOI devices, microwave SOI devices, and low-power SOI circuits. He is currently carrying research in advances multiple-gate SOI MOSFET device physics.

He has been on the committee of several conferences, including IEDM and SSDM, has been General Chairman of the IEEE SOS/SOI Technology Conference in 1988, and is a Fellow of IEEE. He has published over 250 scientific papers and three books on the field of SOI as well as two books on semiconductor device physics and four book chapters on SOI. Dr. Colinge has given lectures on SOI at short courses offered by various conferences, including IEDM, NSREC and the IEEE International SOI Conference.

3.- Panel Discussion Ideas

What is the killing advantage of multiple-gate SOI MOSFETs: electrostatics and scalability, transport or functionality?

The panel discussion was organized with the following scheme. The Chair had previously asked the panellists to list 3 key issues in SOI technology. After compilation, each panellist was invited to address one particular issue, in a lively and provocative way. Each panellist introduced his point of view about SOI technology during 10 minutes. They explained and documented their feelings from their field of experience, by focussing on the following points: what is needed to improve the situation, what is being done well, what is not being done so well, and what we need to improve.

Dr. Cor Claeys, IMEC, Belgium

Dr. Olivier Faynot, CEA-LETI, Grenoble France

Prof. Jerry Fossum, University of Florida, Gainesville, USA

Dr. Stephen Monfray, STMicroelectronics, France

Prof. Francis Balestra, IMEP, Grenoble France

Prof. Jean-Pierre Colinge, Tyndall, Cork, Ireland

Cor Claeys, IMEC:

- FinFET architecture is a way to relax constraint on T_{ox}, N_{doping} to alleviate the problems with leakage and mobility at short gate length.
- But mobility is also impacted by smaller Fin dimensions.
- The increasing impact of parasitic capacitances & resistances when reducing dimensions will influence on the device architecture.
- Other factors to deal with are cost substrate material & self-heating.
- The 16nm node will require double gate (FinFET).
- Intel pointed out that one does not need SOI FinFET; bulk FinFET results look very good (VLSI 2008)
- It seems clear that 3D integration is the future, but which one??

Olivier Faynot, LETI:

- There is a huge offer on SOI device architectures, but most of them in CMOS.
- The main target of the European research in SOI is to do publications.
- SOI is very promising. We have many excellent SOI devices (SOI Zoo); candidates to build circuits and applications. Many possibilities, but very few practical circuits on SOI yet.

- "If you want to convince a company about the use of SOI, you have a problem because there is a large offer in terms of devices, but few solutions in term of circuit design".
- Requirements to fulfil:
    - Demonstration of real application
    - Reproducibility
    - Processing of billions of transistor
    - Yield >90%
    - Low cost
- Key advantage of Multigate devices
    - Process: No, too complicated
    - Electrostatic, scalability: To be demonstrated
    - Transport: No
    - Functionality: No breakthrough

The advantage: Ensure the researchers activities for the next 15 years.

Jerry Fossum, University of Florida

- Bulk (or volume) inversion is not a beneficial effect.
- Lower gate capacitance and midgap gate implies lower current Conclusion: A 3rd dimension is necessary.
- The use of thee or even four gates is limited to very restricted design space.
- From all the MuG devices pragmatic DG-FinFET CMOS can be good, as well as scalable.
- 32% speed improvement can be achieved with pragmatic FinFET design.

Stephen Monfray, STMicroelectronics

- Planar Multigate devices propose the best tradeoff between scalability & performance.
- But what means planar when the device tends to be nanowire/nanodot?
- In any case, the killing advantage is electrostatics control with surrounding gates.
- Main challenges will be cost/yield
- However we should keep in mind that:
    - With a normalization by circumference, none MuG device has already outperformed bulk
    - The intrinsic gain in transport has not been really observed on small devices

Francis Balestra, IMEP

- Multi-gate SOI MOSFETs with volume inversion are needed for ultimate CMOS scaling down to sub-5nm.
- The killing advantages of multiple-gate SOI MOSFETs are:
- They provide better control of charges and electrostatics

  - o I_{on} increase (higher number of gates, ballisticity)
  - o I_{off} decrease due to a better control of SCEs
  - o Gain in performance in a loaded environment → HP/LOP/LSTP
  - o Best subthreshold slope → low voltage/low power
- New design flexibility/architectures can be introduced to control the number of channels. Possibility of independent gate operation.
- Lower Low Frequency noise analog and RF ICs.
- High immunity in Threshold Voltage variability due to the possible use of undoped ultra-thin SOI.
- More tolerant to line edge roughness induced variability and therefore higher scalability.
- NVM/DRAM/SRAM performance improvements and scaling.

Jean Pierre Colinge, Tyndall

- The main advantage of multiple-gate MOSFETs is the electrostatic control.
- A decrease of T_{Si} can be substituted for a decrease of T_{ox} or an increase of ε_{ox} .
- There are not significant differences in terms of SCEs among different well designed multigate devices.
- More research should be focused on the functionality of these devices taking advantage of the independent operation of the different gates.

4. Conclusions and list of topics

After the initial positioning, there was a long and lively debate among the panellists and the rest of the audience. As a final conclusion we can highlight the following three points:

1. There are plenty of multiple-gate SOI MOSFETs which could be potential solutions for the 22nm node and below (SOI Zoo). At this moment is difficult to designate a single SOI candidate among all of them to substitute the traditional planar bulk MOSFET.
2. It will be essential to take advantage of their unique characteristics in terms of SCE control for very low channel length.
3. The key difference could come from the possibility of 3D integration (increasing the density of integration) or specific designs that employ the gates independently achieving new circuits functionalities.

In summary, the topics which need to be promoted and studied at short term are mainly related to device design issues.

1.- Assess the transport properties of multiple-gate MOSFETs compared to traditional planar devices

2.- Evaluate the possibilities of 3D integration of multiple-gate MOSFETs to increase the device density.

3.- Design of circuits that employ the gates independently to get new applications.

Some actions are being taken in this sense:

- A big training event will be held at Grenoble on June 2009 from 20th to 26th dedicated to SOI Concepts: from materials to devices and applications. This event will be organized by Prof. Sorin Cristoloveanu and Dr. Olivier Faynot and several specialists will present the state of the art on SOI technology. In this course all these topics will be presented and discussed in depth.