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COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

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D4.11. First motivated list of selected topics for future research on SOI technology. Outcome of the panel discussion held during the 4th EUROSOI Workshop Cork, 23-25 January, 2008

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PP	Restricted to other programme participants (including the Commission Services)	
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1.- Introduction.

One of the goals of EUROSOI+ project is the promotion of industrial participation in EUROSOI activities and the coordination of the initiatives so that European Industry successfully faces Roadmap-identified challenges

In the first stage of EUROSOI network (2003-2006), we have carefully studied the situation of SOI technology in Europe, we have identified the current status, where we want to go, and what is the best approach ("road") to follow. Now it is time for movement. SOI community has to face and successfully achieve, in the following years, the challenges identified in the Roadmap.

EUROSOI+ will not duplicate works and actions undertaken in other projects, but will, through a forum linking technologists, scientists, designers and industry:

1. Promote industrial participation in the Network activities, informing industry about relevant progress in SOI technology worldwide and providing a feedback loop for industrial mid and long-term interests to academic and research centres.
2. Organize annual workshops, scientific meetings and discussion panels with industry experts (Tyndall-2008, Chalmers-2009, Grenoble-2010 and Granada-2011)
3. Upgrade the EUROSOI State-of-the-Art Report.
4. Upgrade the European SOI Roadmap: Identify scientific priority areas, and formulate research and development strategies.
5. Promote the interaction between existing SOI projects at national and European level (FP6-IST, FP7-ICT, EUREKA/MEDEA), and facilitate the coordination of their work. Organization of Workshops and scientific meetings.
6. Foster the initiatives to face the challenges already identified in EUROSOI Roadmap, by selecting and creating the research consortium from the best European actors already identified at EUROSOI "Who is Who" guide. Co-ordinate activities at national and European level.
7. Co-ordinate activities with other FP7 instruments: NoEs, IPs, Marie-Curie initiatives.
8. Address and foster initiatives beyond CMOS: take advantage of the SOI knowledge to develop platforms for further technological development in nanotechnology, such as to prepare the transition from microelectronics to nanoelectronics.
9. Propose a list of highly desirable topics of advanced research on SOI by analyzing the future trends in industry and research.

To fulfill this goal, EUROSOI will organize panel discussions with different specialists on SOI technology to identify hot topics in SOI research. These discussion panels will be held simultaneously with each EUROSOI workshop. As outcome of these panel discussions, a report with a list of selected topics in SOI research will be elaborated.

The first Workshop and Scientific meeting organized by EUROSOI+ project was held on January 23-25, 2008 in Cork, Ireland. During this Workshop, the first panel discussion, chaired by Prof. Cristoloveanu, was held on Friday, January 25th. The following five SOI experts were invited to participate in the discussions:

1. Dr. Damien Bretegnier, SOITEC, France
2. Prof. Denis Flandre, UCL, Louvain-la-Neuve, Belgium
3. Dr. Sergei Okhonin, Innovative Silicon, Switzerland
4. Dr. Olivier Faynot, CEA-LETI, Grenoble France
5. Prof. Jean-Pierre Colinge, Tyndall, Cork, Ireland

Each expert presented his point of view and position on the SOI technology, future applications, and the European situation. After the initial positioning, there was a long and live debate among the panellists and the rest of the audience. This debate was useful to identify the hot topics and concerns of European researchers and how we could contribute to improve the situation.

The details of the Panel are described in the next sections.

2.- Panel discussion participants.

1) Prof. Sorin Cristoloveanu − IMEP Grenoble (France)

Sorin Cristoloveanu received the PhD (1976) in Electronics and the French Doctorat ès-Sciences in physics (1981) from the National Polytechnic Institute, Grenoble (INPG), France. He joined the Centre National de la Recherche Scientifique (CNRS) and became a Senior Scientist in 1982 and a Director of Research in 1989. In 1989, he joined the University of Maryland, College Park, as an Associate Professor for one sabbatical year. He also worked at JPL (Pasadena), Motorola (Phoenix), and the Universities of Florida (Gainesville), Nashville and Western Australia (Perth). From 1993 to 1999, he served as the director of the LPCS Laboratory of INPG. Between 1999—2000, he was in charge of the creation of the Center for Advanced Projects in Microelectronics (CPMA Grenoble), initial seed of the Minatec center. He is the author or co-author of more than 600 technical journal papers and communications at international conferences (including 100 invited contributions). He is the author or the editor of 17 books, and he has organized 16 international conferences. His expertise is in the area of the electrical characterization and modeling of semiconductor materials and devices, with special interest for silicon-on-insulator structures. He has supervised more than 60 PhD completions. With his students, he has received 5 Best Paper Awards, an Academy of Science Award (1995), and the Electronics Division Award of the Electrochemical Society (2002). He is a Fellow of IEEE, a Fellow of the Electrochemical Society, and Editor of Solid-State Electronics.

2) Dr. Damien Bretegnier − SOITEC, Bernin (France).

Dr. Bretegnier is electrical & electronic engineer by ISEP (L'Institut Supérieur d'Electronique de Paris). Since his graduation, Dr.Bretegnier has been working for different European Semiconductor Companies such as Infineon in the development of SRAMs circuits. During the last years, he has created and developed a Circuit Design Center in India. He is actually Project Manager at Silicon-On-Insulator Technologies (SOITEC).
SOITEC was initially founded in the early 1990s as a commercial spin-off of the Laboratoire d'Electronique, de Technologie et d'Instrumentation (LETI), the premier French technology and instrumentation laboratory for semiconductor research. Today, SOITEC is the world's leading manufacturer and supplier of SOI wafers. SOITEC provides a broad range of advanced thin-film substrates for IC manufacturing, including bonded SOI (UNIBOND®) and silicon-on-quartz/glass wafers. Originally, a SIMOX-driven company, SOITEC has shifted its production to a thin-film bonded technique using the unique Smart Cut® technology. The Smart Cut technology is an implantation technique, which requires only one wafer to form a bonded product. The application of this unique concept enables SOITEC to produce a low-cost, high-volume product using standard manufacturing equipment. The use of standard equipment is a tremendous advantage in reducing the lead time for capacity increases and ensuring that SOI material will profit from the mainstream advances in

semiconductor manufacturing equipment, such as the transition to 300 mm wafer production. In April 1997, SOITEC signed a long-term alliance with Shin-Etsu Handotai (SEH), headquartered in Tokyo, Japan, the leading manufacturer of bulk silicon wafers. The alliance involves technology cooperation for advanced SOI research and development, cross licensing, joint marketing and increased production capacity. Since SOITEC and SEH have extensive experience in SOI technology, the goal was that each company will be able to maximize its strengths through this strategic technology agreement. SOITEC cross-licensed its patented technology to SEH in order to establish Smart Cut® as the worldwide standard technology for SOI wafer manufacturing as it continues to move into mainstream applications. Due to the increased demand for SOI material and the success of UNIBOND, SOITEC has constructed a new $50 million manufacturing and headquarters facility in Bernin, France, near Grenoble. This new production plant, opened in 1999, is located in the same industrial zone as ST Microelectronics new 8-inch wafer facility and newly announced 12-inch facility. Since then, a second phase to the new Bernin facility has been built to increase capacity and address 300mm SOI wafers. Together with SEH, more than 1million wafers/year are being fabricated. In addition to SOI wafers, SOITEC has undertaken significant diversification's, applying the Smart-Cut process for the realisation of unique composite substrates (Anything On Anything concept). Major examples concern the development of strained-Si (sSOI), GeOI, monocrystalline Silicon On Quartz, etc.

3) Prof. Denis Flandre − DICE, Universite catholique de Louvain (Belgium)

Prof. Denis Flandre received the Electrical Engineer degree, the Ph.D. degree and the Post-doctoral thesis degree from the Université catholique de Louvain (UCL), Louvain-la-Neuve, Belgium, in 1986, 1990 and 1999, respectively. His doctoral research was on the modelling of Silicon-on-Insulator (SOI) MOS devices for characterization and circuit simulation, his Post-doctoral thesis on a systematic and automated synthesis methodology for MOS analog circuits. In 1985, he was a summer student trainee at NTT Headquaters, Tokyo, Japan. From October 1990 to September 1991, he was with the Centro Nacional de Microelectrònica, Barcelona, Spain, working on the characterization and numerical simulation of SOI MOS process and devices. He was then at the Laboratoire de Microélectronique (DICE), Louvain-la-Neuve, Belgium, as Senior Research Associate of the National Fund for Scientific Research (FNRS, Belgium). Since 2001, he is full-time Professor at UCL. Since 2003, he has been the Head of the UCL Microelectronics Laboratory. He is currently involved in the research and development of SOI MOS devices, digital and analog circuits, as well as sensors and MEMS for special applications, more specifically high-speed, low-voltage low-power, microwave, rad-hard, high-temperature electronics and microsystems. Prof. Flandre has been recipient of the 1992 Biennial Siemens - FNRS Award for an original contribution in the fields of electricity and electronics, the 1997 Wernaers Prize for innovation in pedagogical presentation of advanced research work and the 1999 CEN•SCK Prize for innovation in nuclear science instrumentation. He has authored or co-authored more than 400 technical papers or conference contributions. He holds 6 patents. He participated in many short courses on SOI technology in

universities, industrial companies and conferences, as well as organized and lectured several courses on SOI technology, devices and circuits. He has been a member of the Advisory Board of the EU Network of Excellence for High-Temperature Electronics (HITEN), of the Scientific Board of the "Microserv" large infrastructure EU program of the CNM-Barcelona, of the Executive Boards of « NANOSIL» (the new EU Network of Excellence in Silicon Nano-devices) and of SINANO (a new EU institute), and of the Director Board of the Cyclotron Research Center (CRC, Louvain-la-Neuve, Belgium). He is an IEEE member, a founding member of the CERMIN (Centre de Recherche en Dispositifs et Matériaux Electroniques Micro- et Nanoscopiques of UCL) and chairs the Users commitee of the UCL Micro/nano-technology facility. Prof. Flandre is a co-founder of CISSOID S.A., a start-up company, spun-off of UCL in July 2000, focusing on SOI circuit design services.

4) Dr. Serguei Okhonin − Innovative Silicon Inc, Laussane (Switzerland)

Dr. Okhonin received his M. Sc. in Physics from Novosibirsk State University in 1980, and his PhD degree from the Swiss Federal Institute of Technology (EPFL) in 2001. From 1980 to 1993, he worked as Research Associate at the Institute of Semiconductor Physics, Novosibirsk, Russia, focusing on semiconductor device physics. From 1994 to 2003, he worked as Research Associate at l'Institut de Micro et Optoelectronique (IMO) and Laboratoire d'Electronique Generale (LEG) at Ecole Polytechnique Federale de Lausanne (EPFL). He took part in several European projects focused on advanced CMOS technology development. In 2002 he co-founded Innovative Silicon, developing a new SOI single transistor memory technology. He has authored or co-authored more than 50 papers and filed more than 30 patents. Dr. Okhonin has served as member in program committees of the ASDAM and ESSDERC international conferences.

Innovative Silicon Inc. (ISi) delivers ultra high density memory IP for embedded SoC, MPU, and portable consumer applications. Endorsed by IEEE Spectrum Magazine in 2007 as one of five 'winning' technologies, ISi's Z-RAM[R] memory provides up to twice the density of embedded DRAM and is five times denser than embedded SRAM, making it the world's lowest-cost semiconductor memory solution. The company closed its first round of VC funding in 2003, completed its first 90nm megabit Z-RAM memory designs in 2004, its first 65nm designs in 2005 and its first 45nm designs in 2006. The company is incorporated in the USA with R&D in Lausanne, Switzerland.

5) Dr. Olivier Faynot − LETI, Grenoble (France)

Olivier Faynot received the M.Sc and Ph.D. degrees from the Institut National Polytechnique de Grenoble, France in 1991 and 1995, respectively. His doctoral research was related to the characterization and modeling of deep submicron Fully Depleted SOI devices fabricated on ultrathin SIMOX wafers. He joined LETI (CEA-Grenoble, France) in 1995, working on simulation and modeling of deep submicron fully and partially depleted SOI devices. His main activity was the development of a dedicated Partially Depleted SOI model, called LETISOI.

Since 2000, he is involved in the development of sub 0.1µm fully and partially depleted technology and other very advanced SOI devices. He is author and co-author of more than 30 scientific publications on SOI in journals and international conferences. Since 2001, Dr. Faynot is on the IEEE International SOI conference Committee.

6) Prof. Jean Pierre Colinge − Tyndall National Institute, Cork (Ireland)

Prof. Colinge is head of the Ultimate Silicon Devices Research Group at Tyndall National Institute in Cork. He was professor of Electrical Engineering at the University of California, Davis (USA) from 1997 to 2006. He received a BS degree in Philosophy, the Electrical Engineer degree, and the Ph.D. degree in Applied Sciences from the Université Catholique de Louvain, Louvain-la-Neuve, Belgium, in 1980, 1980, and 1984, respectively.

From 1981 to 1984 he was Researcher at the Centre National d'Etudes des Télécommunications (CNET), Grenoble, France, where he developed early for the fabrication of SOI films and developed the "Stacked CMOS" technique (one of the first 3D structures). From 1985 to 1988 he was member technical staff of the Hewlett-Packard Research Labs, Palo Alto, CA, where he carried out research and development work on thin-film SOI devices and discovered many of the properties of fully depleted SOI devices (sharp subthreshold slope, absence of kink effect, properties of transconductance, etc.) From 1988 to 1991 he was project leader for the SOI research at IMEC (Inter University Microelectronics Center) in Leuven, Belgium. He designed and fabricated novel SOI devices, including radiation-hard devices and the first double-gate SOI transistors. From 1991 to 1997 he was Professor at the Université Catholique de Louvain, heading research in the areas of SOI device physics and technology, high-temperature SOI integrated circuits, radiation-hard integrated SOI circuits, quantum effects (2D,1D) in SOI devices, microwave SOI devices, and low-power SOI circuits. He is currently carrying research in advances multiple-gate SOI MOSFET device physics.

He has been on the committee of several conferences, including IEDM and SSDM, has been General Chairman of the IEEE SOS/SOI Technology Conference in 1988, and is a Fellow of IEEE. He has published over 250 scientific papers and three books on the field of SOI as well as two books on semiconductor device physics and four book chapters on SOI. Dr. Colinge has given lectures on SOI at short courses offered by various conferences, including IEDM, NSREC and the IEEE International SOI Conference.

3.- Panel Discussion – Key Issues in SOI: Solutions and Ideas

The panel discussion was organized with the following scheme. The Chair had previously asked the panellists to list 3 key issues in SOI technology. After compilation, each panellist was invited to address one particular issue, in a lively and provocative way. Each panellist introduced his point of view about SOI technology in 5−6 slides during 10 minutes. They explained and documented their feelings from their field of experience, by focussing on the following points: what is needed to improve the situation, what is being done well, what is not being done so well, and what we need to improve.

Damien Bretegnier, SOITEC:

- "For mobile systems, bulk-Si era is ending and SOI is coming"
- "SOI is the solution to answer mobile market key drivers:
    - SOI enables 30% to 40% reduction on dynamics power consumption. (Increase battery lifetime)
    - Higher performance
    - More memory
    - Improved reliability
    - Cost
    - SOI merits for SoC noise immunity.
- Fully-depleted SOI technology will be the choice technology for 22nm node.
- To improve the situation, SOITEC will reduce the price of SOI wafers in the following years.
- **Conclusion:** "We will see very cheap mobile telephones with SOI inside in the following years"

Denis Flandre, UCL:

- Prof. Flandre is pessimistic about SOI future in the More than Moore domain.
- "More than Moore applications are very well suited for SOI. However, having a glance to The International Solid-State Circuits Conference program (ISSCC is the foremost forum for presentation of advances in solid-state circuits and systems-on-a-chip) we cannot find any papers on SOI related to these topics.
- "SOI is out of business in More than Moore, right now"
- Maybe the field of sensors and MEMS can be a good ground play for SOI technology applications.

Sergei Okhonin, Innovative Silicon, Inc:

- "Is SOI the only solution for 22nm technology node?"
- The answer to this question has to take into account the following parameters:
    - Manufacturability
    - Performance
    - On overall, COST. (The price of the wafers is critical !!!)

Olivier Faynot, LETI:

- There is a huge offer on SOI device architectures, but most of them in CMOS.
- The main target of the European research in SOI is to do publications.
- SOI is very promising. We have many excellent SOI devices (SOI Zoo); candidates to build circuits and applications. Many possibilities, but very few practical circuits on SOI yet.

- "If you want to convince a company about the use of SOI, you have a problem because of the too large offer in term of devices, but very few solutions in term of circuit design"

- We have to think differently as we did in the past:
    - New actors: Foundries, Fabless
    - New markets: Low power, memory, MEMS, automotive.

Jean Pierre Colinge, Tyndall

- We should focus our research efforts in different fields to Logic.
- AMD has based its microprocessors on SOI wafers for the 130, 90 and 65 nm generations. However, they are still mulling whether to use silicon on insulator (SOI) or bulk silicon technology for its future high-end and mobile products.
- IBM has been touting SOI as a means of reducing junction capacitance, in contrast with Intel and Texas Instruments, which have shied away from SOI for cost and design complexity reasons. Even Freescale Semiconductor has a stake, with its high-end networking chips committed to SOI.
- Cell Broadband Engine chips used in the Playstation3 systems have been produced on SOI wafers. However, Toshiba may modify the Cell processor to Toshiba's bulk CMOS process, moving away from the silicon on insulator (SOI) process.

Sorin Cristoloveanu, IMEP

- The actual problem is not the technology. We have a large offer of SOI devices. We need to agree in one candidate (FDSOI?, FinFET?) and then try to involve design companies to develop design libraries and design kits around the chosen candidate to be used in low-power and mobile applications.

4. Conclusions and list of topics

After the initial positioning, there was a long and very live debate among the panellists and the rest of the audience. As a final conclusion we can highlight the following three points:

1. There are plenty of “SOI species” which could be potential solutions for 22nm and below (*SOI Zoo and Botanic Garden*) but we need to designate a single SOI candidate among all of them. Otherwise it is impossible to advance our position much more from where we are now: we have excellent devices (LETI FDSOI, IMEC FinFETs), but very few circuits applications.
2. It is becoming urgent to involve/convince design people in next future to work using this only device.
3. The announcement of SOITEC about a strong reduction of SOI wafer price is important. This will be essentially beneficial for the development of communication applications: “rather cheap mobile telephone with SOI inside”.

In summary, the topics which need to be promoted at short term are mainly related to design issues. Some actions are being taken in this sense:

-IMEC is organizing a two-days course about SOI for analog, digital and RF SOCs and microsystems applications (May-15-16, 2008 IMEC Microelectronics Training Center) with the participation of Profs. Denis Flandre, Jean Pierre Raskin, Nadine Collaert and Piet Wambacq.

-The training course to be organized in January, 2009 in the framework of EUROSOI-2009 Workshop will be devoted to design issues on SOI technology.