Contract N° 257964

NANO-TEC

Ecosystems Technology and Design for Nanoelectronics

Coordination Action

Information and Communication Technologies

Deliverable D 5.2

Report on benchmarking exercise and table of selected devices

Due date of deliverable: M16

Actual submission date: M19

Start date of project: 1 September 2010 Duration: 30 Months

Organisation name of lead contractor for this deliverable:

VTT Technical Research Centre of Finland

Revision [1.1]

Approval

WP Leader ☒	**Coordinator** ☒

Partner	Please, give a short description (1-3 sentences) of partners contribution to this deliverable
VTT	VTT is the work package leader and compiles all of the results regarding nano-electronic devices benchmarking to arise from the 2nd NANO-TEC Workshop. Contributed the Benchmarking criteria set table to be used in the 2nd NANO-TEC workshop.

Table of contents

1. Introduction

This Deliverable describes the benchmarking exercise for the emerging Beyond CMOS devices. The benchmarking is the outcome of the second workshop in the series of the four workshops to identify the potential emerging devices for data processing for the post CMOS era. This topic is defined in the DOW as the following:

Task 5.2: Benchmarking and selection
Benchmarking is based on characterisation of devices with the emphasis on the properties defined in Task 5.1. Measurements such as I-V curves, noise margins, impedance levels etc. will be performed to define the critical parameters, and not only one but several devices will be characterised to obtain a picture of the device property and fabrication tolerances. The best candidates for future ICT devices will be identified.

A similar exercise was carried out in the USA in 2010 [1] with the focus on strictly benchmarking the emerging devices against to state of the art CMOS devices. The benchmarking was performed by Semiconductor Research Corporation (SRC) and Nanoelectronics Research Initiative (NRI). For the benchmarking a relative large number of emerging devices were selected. Inverters, NANDs and adders were built and the performance was compared with 15 nm CMOS circuits. An example of the outcome is shown in Fig. 1 in which the energy-delay product of NANDs constructed using different devices is compared. According to this investigation the emerging devices are performing surprising well.

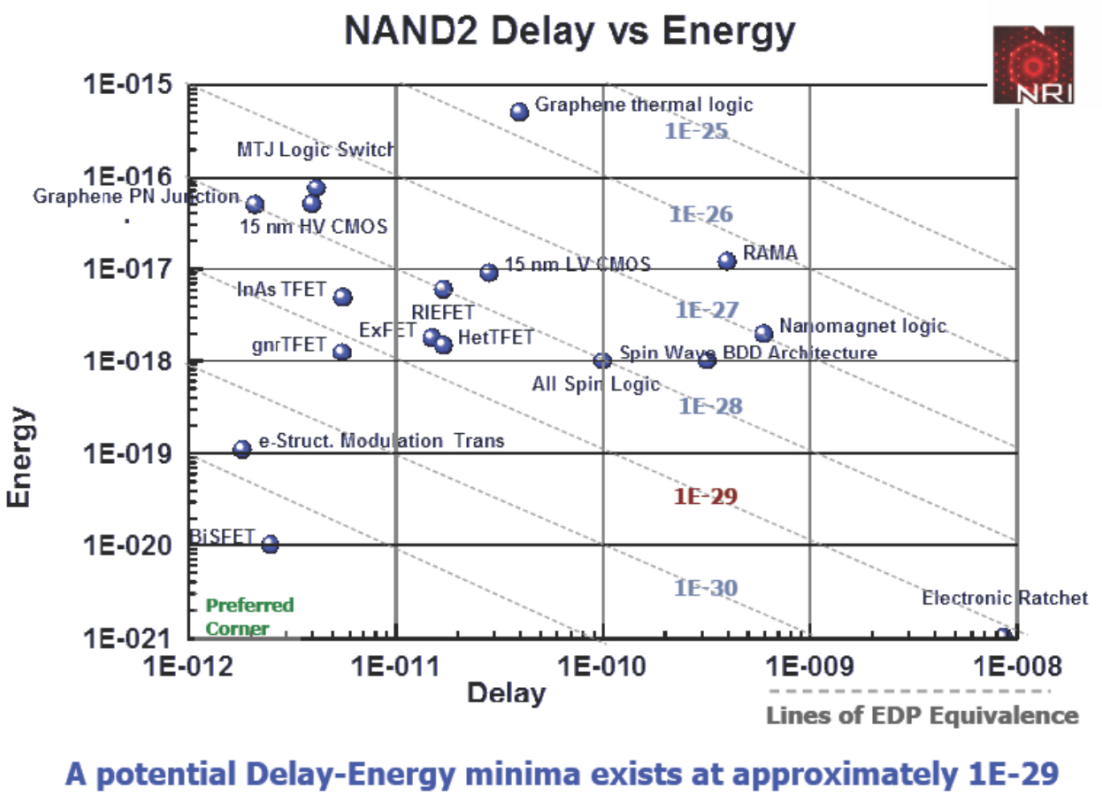


Fig. 1 Energy-delay product for NANDs with fan-out of 4 constructed using various device technologies. [After Bernstein et al., Device and Architecture Outlook for Beyond CMOS Switches, Proc. IEEE 98 (2010) 2169.]

2. NANO-TEC approach for benchmarking

In the NANO-TEC project a little bit broader scope for the benchmarking was selected. The idea was not to directly compare the performance with CMOS devices but also to allow for concepts with other functions than just digital Boolean switches. One of the targets was to collect information and parameters relevant for the design community to identify the potential of the emerging devices for useful data processing. One of the results seem to be that there still is a rather large gap between the approaches providing new functionalities and the design tools available., A more detailed report of the outcome is given in the Appendix 1.

3. Conclusions

It is clear that there is a gap between the emerging device concepts and the design approaches. Diederik Verkest in his introduction for the panel discussion in the 2nd Workshop.briefly described the design tools and challenges in scaling of CMOS circuits. Regarding the Beyond CMOS devices, he stressed the importance of systemability, meaning "The ability to economically design and manufacture reliable systems from the interaction of devices fabricated in a given technology" with system standing for "computation, storage, interconnects and input/output". The big challenge to the Beyond CMOS devices arises from the lack of understanding of the physics of the operation, large variance of the properties and in reproducibility. This means that multi-scale modelling approaches are essential for the emerging devices. It also became evident that it is very difficult to make definitive decisions on the candidates for the next generation data processing devices. Some of the potential candidates have been identified during the benchmarking but the final conclusions and recommendations should be left for the SWOT practise to be carried out in the Workshop 3 of the NANO-TEC project.

References

[1] Bernstein et al., Device and Architecture Outlook for Beyond CMOS Switches, Proc. IEEE 98 (2010) 2169.

Appendix 1

Contract N° 257964

NANOTEC
Ecosystems Technology and Design for Nanoelectronics

Coordination Action
Information and Communication Technologies

Start date of project: 1 September 2010 Duration: 30 Months

Report on Workshop 2:
Benchmarking of New Beyond CMOS device/design concepts
13-14 October 2011, Divani Caravel Hotel, Athens, Greece

Report submission date: 1.2.2012….. Revision: [v2]

Author: Jouni Ahopelto - VTT Technical Research Centre of Finland

Project co-funded by the European Commission within the Seventh Framework Programme (2007-2012)		
Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

Partner	**Contribution**
ICN	Rapporteur for Memristors
VTT	Compiled, edited and submitted the Workshop 2 report, rapporteur for Molecular Electronics
ECN	
CTHA	
ITE	
TU Delft	Rapporteur for Spintronics
NCSR	Rapporteur for Nanowires
Tyndall-UCC	Rapporteur for Solid-State Quantum Computing

Juelich	
EPFL	
CNRS	

Table of contents:

1. Introduction

In Europe the interaction between the design and the technology research communities working in nanoelectronics, and especially in the Beyond CMOS area, is characterised by a diversity of terminology, modus operandi and the absence of a consensus on main priorities.

In the project NANO-TEC, the relationship between technology and design in nanoelectronics is seen as a mutually dependent two-block partnership. Consider a function of relevance to Beyond CMOS, which comes out of the myriad of possibilities arising from the fast progress in material sciences, coupled to developments in the control of morphology and or the nanostructuring of these materials. A crucial next step is to find a way to link this function to an established, or a new, logic. For this logic to work, ideas on design and architecture are needed. In this basic frame of analysis, design plays a key enabling role in the latter two steps, as well as in the consideration of the way the information-related function, based on the properties of these new materials and (nano) structures, is linked to a logic system.

The 1st NANO-TEC workshop entitled "Identification of the main requirements for future ICT Devices" was held in Granada, Spain from 20 to 21 January 2011 with over 70 participants from academia, research organisations and industry. It was the first of four planned workshops as part of the NANO-TEC project strategy to reach its aim of identifying the next generation of emerging device concepts and technologies.

The 2nd NANO-TEC workshop "Benchmarking of new beyond CMOS device/design concepts" was held in Athens, Greece October 13-14, 2011. In this report the main points, trends, specific discussion points and recommendations are summarised. The text has been compiled by the rapporteurs, aided by the speaker presentation and the discussant brief presentations. The compilation and editing is the responsibility of the partner VTT.

The workshop presentations can be found in https://www.fp7-nanotec.eu/node/499 .

2. Methodology of Workshop 2

Following the outcome and recommendations of the 1st workshop, the topics for the 2nd workshop were selected and the focus was more on devices than on technology. To reach some level of comparability and to empower the discussion on the relevant design related issues, the following guidelines were provided in advance to the speakers, discussants and rapporteurs:

Guidelines for the Second NANO-TEC Workshop, "Benchmarking Beyond CMOS Devices",

The aim of this workshop is to shed light on the potential of the technologies claimed for the "Beyond CMOS" era. The aim is not to directly compare, to "benchmark", the performance of the emerging devices against the current state-of- the-art CMOS devices. It is rather more like mapping and identifying the potential for future ICT applications, bearing in mind that some relevant properties are required to be fulfilled. The challenges include, among others, power consumption, speed, integration prospects, flexibility for new architectures and manufacturability. The attached slide contains a Table which should be used for summing up the relevant properties of the emerging technology. Personal opinions and institutional views are encouraged.

The USA Semiconductor Research Corporation (SRC) carried out a benchmarking study a few years ago of emerging devices. The approach was to realise a few digital devices, such as inverters, NAND gates and 32 bit adders, using the emerging devices and to compare the performance, i.e., energy vs. delay and required surface area, with current CMOS devices. Interestingly, the outcome was that the

emerging devices in general had a little larger delays but smaller power consumption, not lagging much behind of the SoA CMOS circuits.

Speakers

The time allocated to your presentation is 35 minutes. A talk covering the device and/or design concepts, the state of the art, future trends, main scientific, technological and design challenges in the next 10 years or beyond in your field, would be much appreciated. Please use the attached slide in your presentation. In the slide are summarised some generic issues that are relevant for information technology devices. The list is not at all exhaustive and other relevant issues, potentially typical to the technology in question should be addressed.

Your discussant will need a copy of the power point presentation a week in advance (October 6), even if it is in draft form, to prepare his/her part. Please send your slides directly to your discussant with cc to Noemi Baruch (see email address below). When registering we would ask you for a public version of your presentation in pdf for the Workshop web site. Your talk can of course be different. We simply need some form of records to feed into the next workshops (see figure at the end of this document).

Discussants

The main role of the discussant is to ensure the discussion is lively and that the information and opinions we need for benchmarking are identified and clarified. There are 25 minutes allocated for the discussion.

When you receive the draft presentation from the speaker in your session, consider the aims of the workshop and prepare some questions for the speaker and for the audience. The idea is not for you to prepare another talk, but *well formulated questions, which could be illustrated with figures and shown in a slide or two, together with your main questions.* Would you bear in mind that one thing is to identify, and another is to benchmark (compare) with respect to current and future performance and requirements. Please make your slides with your questions available to Noemi Baruch before the end of the workshop.

Rapporteurs

The key role of the rapporteurs is to prepare a summary of the session (talk and discussion) to be shown in a few ppt slide in the 5 minutes you have in the Wrap up sessions. It would be helpful if you have some rough text, which can later (within a week?) be prepared in a 1- or 2-page summary for internal workshop participants' use, on which the two summary slides are based. We would be grateful if you could send the two Summary slides and 2-page text summary to Noemi Baruch as soon as possible after the workshop.

Benchmarking Beyond CMOS Devices

Technology	[Wires, graphene, MEMS etc… please insert name]
Gain **Signal/Noise ratio** **Non-linearity**	
Speed **Power consumption**	
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	
Other specific properties	
Manufacturability **(Fabrication processes needed, tolerances etc.)**	
Timeline **(When exploitable or when foreseen in production)**	

3. Topic 1: Molecular Electronics

Speaker: Dominique Vuillaume
Discussant: Clivia M Sotomayor Torres
Rapporteur: Jouni Ahopelto

3.1. Working group report

In the presentation molecular electronics was divided in three different categories based on different dimensions: i) single molecule electronics, ii) self-assembled molecular electronics and iii) thin-film molecular electronics. The presentation focused on self-assembled molecular electronics with lateral dimensions from a few tens of nm to mm and vertical dimensions of a few nm as the most relevant device structure for the purpose of the NANO-TEC benchmarking. For the single molecule electronics no applications was foreseen in a reasonable time-scale and thin-film molecular electronics was regarded as plastic electronics with some products already commercialised and not as a candidate for Beyond CMOS devices. Self-assembled molecular electronics was further divided into device families in which the self-assembled monolayers (SAM) act as dielectric, as an active channel or as a non-linear switch. Finally, tunnel magnetoresistance (TMR) devices for molecular spintronics and concepts for neuro-inspired devices were described.

The most straightforward application for SAMs is to use them as gate dielectrics combined with organic conducting polymers. Transistor behaviour has been demonstrated at reasonable drain voltages. The drain current levels are still small, leading to requirement of relatively wide devices. Simple logic gates have also been demonstrated with reasonable gain and low switching energy.

In a SAMFET the SAMs form the channel of the FET. This type of device is schematically shown in Fig. 1. It seems that true saturation is difficult to reach with this type of device. Anyhow, Ion/Ioff ratios close to 2000 has been reached and a 15 bit code generator by integrating 300 SAMFETs has been demonstrated.

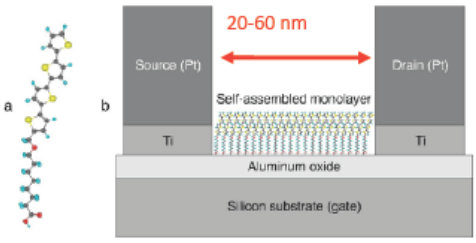


Fig. 1. Cross section of a SAMFET in which the channel is formed from self-assembled 4T-MEOA polymer.

[M. Mottaghi et al., Adv. Funct. Mater. 2007, 17, 597–604.]

Memory cells have been realised using redox molecules in which the charge density can be very high, of the order of 19 mC/cm2. Write times of 10 ms and retention times of a few hundred of seconds have been demonstrated.

Conformation changes triggered by light can be used to switch the conductance and on/off ratios from about 100 to 1500 have been obtained.

There are several experimental results on electrical molecular switches based on hysteretic behaviour of the molecules, e.g., in cross-bar configuration. The role of the molecules is not yet fully clear.

Tunnel magnetoresistance through a SAM junction was first demonstrated in 2004. Since then TMR up to 300 % has been demonstrated. The reproducibility of the devices is still questionable.

Finally, an interesting new development is based on nanoparticle-organic molecule FET (NOMFET) which combines conducting polymer with metallic nanoparticles. The NOMFETs have shown neuron-like behaviour by mimicking plasticity found in human synapses, potentially leading to learning behaviour.

Open issues

Several questions were raised during the discussion and some of these are included in the benchmarking table attached. The questions included issues such as potential routes to integration, interconnects and, consequently, potential problems related to design and architecture. Although there is a wide variety of molecules with different functions available, providing almost infinite number of combinations, the question arouse, how to combine the molecules to achieve the desired set of functions. Also, the impedance levels are relatively high and the current drive capability low, leading to low speed and, potentially, problems in integration due to restricted fan-out.

Fabrication is another open issue. Although the synthesis of the molecules can be controlled, the reproducibility in device fabrication remains an open question.

Recommendations

Although single molecule devices were omitted in the presentation, it would be important to continue the research to gain insight on the behaviour and potential of molecules as building blocks for information processing devices. Also, the design community should start to advance approaches for architectures for the molecular devices, switches and memories, not to mention the neuron inspired devices.

Conclusions

The research in the field of molecular electronics, maybe excluding plastic electronics, has been driven so far by academic push. The topic is very interesting, although one cannot expect this technology to replace current CMOS, as was commented during the discussion. For information processing new paradigms will be needed for molecular electronics, single switches and their integration may not be the right way to exploit molecules in electronics. For this reason benchmarking against CMOS technology may not be fully fair. For sensing applications and, especially in flexible electronics the current maturity level may provide new possibilities. It can be expected that in the long term new interesting developments will emerge, but much more research will yet be needed.

3.2. Benchmarking table

Benchmarking Beyond CMOS Devices

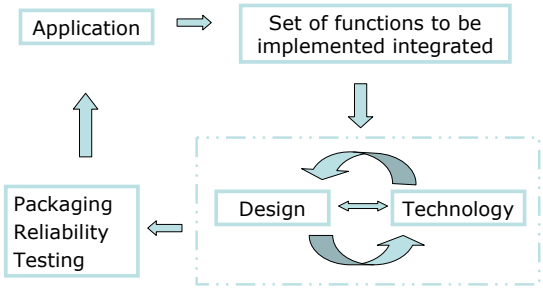
Technology	Molecular Electronics D. Vuillaume, CNRS & University of Lille
Gain **Signal/Noise ratio** **Non-linearity**	Ok with SAMFET (to be optimized), 2-terminal junction: low current Noise not yet studied (a few publications) Molecular junctions are mainly non-linear
Speed **Power consumption**	Low Low (50 zJ/mol switching energy)
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	Molecule-nanoparticle 2D and 3D arrays could implement some functions (e.g. reconfigurable logic, neuro-inspired functions)
Other specific properties	Almost infinite combination of molecules, adjustable by chemistry, specific design (1 molecule = 1 function)
Manufacturability (Fabrication processes needed, tolerances etc.)	Solution processing, compatible with flexible substrate. Defect control? Large variability (but not a problem if we envision artificial neural networks)
Timeline (When exploitable or when foreseen in production)	> 5 – 10 years (if ever?)

4. Topic 2: MEMS

Speaker: Lina Sarro
Discussant: Piotr Grabiec
Rapporteur: Danilo de Marchi

4.1. Working group report

Strength and weaknesses of presented technology
Generally MEMS are produced using modified integrated circuit (IC) fabrication techniques and materials. This is done not having as first goal the miniaturization, but it is more important for MEMS to put more functions per chip area. The role of MEMS/NEMS in ICT can be seen as integrating sensors, functionalities etc. with ICT. MEMS are strongly application driven, in fact from the application is individuated the set of functions to be implemented and integrated, then the design and the realization are carried out (see figure).



The use of the third dimension is one of the most important characteristics and must be exploited as much as possible. The main advantages of the use of 3D are the possibility (i) to integrate specific functions, (ii) to enhance performances, (iii) to miniaturize a complete system.

With MEMS it is possible to mimic the reality, mixing movement, forces, electrical stimulation. And this gives a possibility of testing for example cells in conditions very close to the real environment. An example can be the test of cardiomyocytes plated on a stretchable multi-electrode array, miming the heartbeat.

Open issues

In MEMS/NEMS almost all the domains of physics are present, so the functionalities to be realized are very different. For this reason they are mainly application driven. They are new technologies that can have a strong impact on normal life, and nowadays they have yet to bet completely accepted by the users. They are very complex, but in the same time they must be reliable and low power, because most of their application fields are related to portability, so they have to have an autonomous management of power.

The most important challenges for MEMS technologies can be summarized as:

- Miniaturization related to size matters. Technology advances are on-going and the design tools and simulation programs must be upgraded to the new solutions
- For integration the most important point is to manage complexity. Monolithic vs heterogeneous solutions must be considered. Performances have to be considered vs costs and vs volume. Integration is a key point, because the “user” wants a system
- They must be autonomous, with a long life
- New applications are needed to integrate new functionalities, increase reliability and give to the products the requested “multiple” applicability

The actual technology trends are:

- Top down & Bottom up BMM & SMM ”merge”
- Functional multi-layers and heterogeneous integration
- System approach
- Harsh environment: SiC, Diamond, Graphene

- Biocompatibility
- Flexibility

Recommendations

It is important to exploit the third dimension in the devices and to focus to the user needs and to the applications. System integration level needs special attention. In fact it controls performance and forms more than the 70% of costs, and it has more than the 90% of impact to size and reliability.

Conclusions

MEMS development has come through fundamental research moving towards applications. Advanced micro and nanotechnologies offer many opportunities for improved performance and reduced costs in a wide range of applications and emphasis is on improved functionality and reducing the size of the system rather than reduced size of individual components. For this reason scaling of components is only necessary where functional benefits can be obtained. Health, Environment and Energy are the main areas seen for the technology, thus the applications require multi-disciplinary approach.

4.2. Benchmarking table

Not available. The speaker said that the table, as it is, it is not correct for the MEMS. In fact the diversity of MEMS technology and applications would require a specific and more complex table.

5. Topic 3: Solid-State Quantum Computing

Speaker: Jaw-Shen Tsai
Discussant: Wolfgang Porod
Rapporteur: Isabelle Ferain,

5.1. Working group report

The prospects of solid-state quantum computing were debated by Prof. Jaw-Shen Tsai. Quantum computing relies on the coupling of switching quantum bits (qubits). The emphasis of the talk was set on issues related to de-coherence states/rate and integration schemes for quantum computing. According to Prof. Tsai, Josephson junction (JJ) qubits might be the most promising way to approach supercomputing and break the thermodynamical limit encountered in MOSFETs caused to thermal distribution of electrons in the energy bands. The main advantage of quantum computing is that it consumes no energy at the qubit level. However no super computer involving more than a hundred qubits have been achieved so far, which shows that there's still a long way to go before it can compete with present CMOS logic circuits. In theory, quantum computing is expected to increase the number of qubits (functionality density) as compared to conventional solid-state devices, which will allow significant computational time decrease. The current standard used for quantum computing is SSL128 (Rsa1024). Physical implementation of Qubits can be done with superconductor JJ (where phase, flux, charge are the degrees of freedom) or with semiconductor quantum dot (where the degrees of freedom are the spin (preferred, for its larger retention time) and the charge). In his talk, Prof. Tsai mentioned that JJ qubits are compatible with Silicon MOS processing.

The applications can be found in quantum mechanics simulations where computation of huge matrix is involved. Quantum computing intends to solve simplification issues currently required in order to simulate quantum effects in a reasonable amount of time. This is meant to speed up simulations and to limit power consumption.

Main challenges arise from de-coherence rate and implementation of correction. Interfacing for read-out is straightforward (the current direction is used to identify 1 or 0) but the question on how to read the data during computing without introducing thermal noise remains unanswered. A few solutions were cited during the discussions, such as niobium-Rapid Single Flux Quantum circuits but it requires cryogenic cooling in order to allow for quantum non-demolition measurements and maintain phase coherence. Another possibility relies on Bayesian quantum feedback.

Open issues

It is not clear which will be the "winning" technology for qubits : It probably needs to be solid-state but should it be Josephson junctions? Quantum dots? Single spins? Robustness is another issue: Qubits need to be isolated from external noise sources, yet interactions are needed to control them. At least 100 of qubits are needed for computing to be useful. Very few algorithms are available at this stage, and the need for error correction may consume most resources as error corrections will be handled by qubits

Session summary

The main issue addressed in the talk was the scheme to integration for quantum computing. Physical implementation of qubits is more likely to happen in a solid-state technology, be it with superconducting Josephson Junctions or quantum dots. How quantum computing works has been presented (coupling between 2 switching qubits) and the integrability of such computing scheme has been addressed. It was briefly mentioned that JJ-based chips have been achieved and demonstrated full compatibility with silicon MOS-technology. The discussant/audience tried to identify key applications for QC and how to implement error correction with qubits. QC might present better

power consumption figures than conventional MOS switches-based computing; however this is achieved at a cost of increased hardware complexity. Key applications remain to be clearly identified to justify to effort invested in the development of quantum computing.

Conclusions

Increasing the number of qubits while maintaining the current decoherence rate should be considered as the key indicator for monitoring progresses in quantum computing.

5.2. Benchmarking table

Benchmarking Beyond CMOS Devices

Technology	Solid-state –superconducting - Qubits
Gain, Signal/Noise ratio, Non-linearity	n/a
Speed **Power consumption**	~2^N from gate standpoint is almost 0 but the energy required to run cryogenic equipment (for ultra-low noise) is fairly high → Qubits is not the replacement for CMOS
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	- Maintain current de-coherence rate and implement correction witha reasonable increase in number of Qubits - Integration/Interfacing: read-out is straightforward (current direction is used to identify 1 or 0) but strategy on how to open the system w/o introducing noise is challenging (during computing).
Manufacturability **(Fabrication processes needed, tolerances etc.)**	- Al tunnel junctions (best coherence), involves EBL. - No obvious material-related issue as it operates at very low T and Qubits are not stressed.
Timeline	10 to 100 Qubits quantum computing in less than 10 years from now (doesn't include error correction?).

6. Topic 4: Spintronics

Speaker: Johan Åkerman
Discussant: Christian Pithan
Rapporteur: Mart Graef

6.1. Working group report

The historic drive for spintronics originates from the hard disk drive industry. Within the domain of spintronics, the following topics were discussed:

- MRAM
  - Toggle MRAM
  - Spin Transfer Torque MRAM (STT-MRAM)
  - Thermally Assisted Switching MRAM (TAS-MRAM)
  - Thermally Assisted STT-MRAM (TAS+STT-MRAM)
  - Thermagnonic STT-MRAM
- Spin Torque Oscillators
- Spin Torque Microwave Detectors
- Magnonics, spin caloritronics

Benchmarking tables were presented for all these options, except magnonics and spin caloritronics, which are not yet suitable for benchmarking. Applications can be found in non-volatile memories in which it will be hard to beat flash NVM (now at 19 nm) in device density, but for power consumption and speed, spintronics will be advantageous. Gate arrays (FPGA) is obvious application for spin torque. This enables integration of logic & memory. Examples are video tracking and imaging.

Open issues

The reliability issue of thermally assisted MRAMs was raised (noise, fluctuations, scaling limits?). There is no single answer possible, since this issue is associated with the "electromagnetic recording trilemma". Another interesting question was could spintronics be an option for spatial computing (rather than in time domain)? This was considered to be a rather "esoteric question", which would require substantial exploratory research.

Conclusions

Spintronics hold high potential for memory applications (i.e. the HDD market). This is very close to industrialization (timeline 1-3 years), and as such it does not qualify for 'beyond CMOS'. Today, most resources go to STT-MRAM. Spin torque will not replace conventional memories, but is a suitable option for some (large) niches, e.g. applications requiring flash/DRAM combinations. Spintronics can be considered as a 'tool box' that provides an entry point for other spin transfer device options.

Within the domain of spintronics, novel devices such as magnonics and spin caloritronics have a high potential for various applications (e.g. microwave detectors). Benchmarking for these devices has yet to be done.

6.2. Benchmarking table

Toggle MRAM

Technology	Toggle MRAM – Commercially Available
Gain Signal/Noise ratio Non-linearity	N/A N/A N/A
Speed Power consumption	40 MHz Zero stand-by power, ~120 pJ per switching event
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	CMOS compatible, embeddable, modular
Other specific properties	Radiation hard, High Reliability, Temperature range
Manufacturability (Fabrication processes needed, tolerances etc.)	CMOS compatible
Timeline (When exploitable or when foreseen in production)	Commercialized

STT-MRAM

Technology	Spin Transfer Torque MRAM (STT-MRAM)
Gain Signal/Noise ratio Non-linearity	N/A N/A N/A
Speed Power consumption	40 MHz Zero stand-by power, ~0.02 - 2 pJ per switching event
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	CMOS compatible, embeddable, modular
Other specific properties	Radiation hard
Manufacturability (Fabrication processes needed, tolerances etc.)	CMOS compatible
Timeline (When exploitable or when foreseen in production)	1-3 years

TAS-MRAM

Technology	Thermally Assisted Switching MRAM (TAS-MRAM)
Gain Signal/Noise ratio Non-linearity	N/A N/A N/A
Speed Power consumption	40 MHz Zero stand-by power
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	CMOS compatible, embeddable, modular
Other specific properties	Radiation hard
Manufacturability (Fabrication processes needed, tolerances etc.)	CMOS compatible Reliability?
Timeline (When exploitable or when foreseen in production)	1-3 years?

TAS+STT-MRAM

Technology	Thermally Assisted STT-MRAM (TAS+STT-MRAM)
Gain Signal/Noise ratio Non-linearity	N/A N/A N/A
Speed Power consumption	40 MHz Zero stand-by power, 2-3 pJ per switching event
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	CMOS compatible, embeddable, modular
Other specific properties	Radiation hard
Manufacturability (Fabrication processes needed, tolerances etc.)	CMOS compatible Reliability?
Timeline (When exploitable or when foreseen in production)	1-3 years?

Thermagnonic STT-MRAM

Technology	Thermagnonic STT-MRAM
Gain Signal/Noise ratio Non-linearity	N/A N/A N/A
Speed Power consumption	40 MHz Zero stand-by power, <1 pJ per switching event
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	
Other specific properties	Radiation hard
Manufacturability (Fabrication processes needed, tolerances etc.)	CMOS compatible? Functionality demonstrated?
Timeline (When exploitable or when foreseen in production)	3-5 years

Spin Torque Oscillators (STO)

Technology	Spin Torque Oscillators (STO)
Gain Signal/Noise ratio Non-linearity	N/A Low to moderate signal, high phase noise Mostly linear
Speed Power consumption	0.1 - 50 GHz demonstrated, >100 GHz expected Low to moderate depending on technology
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	CMOS compatible, embeddable, modular
Other specific properties	Ultra wide band, Ultra high modulation rates, Nano size
Manufacturability (Fabrication processes needed, tolerances etc.)	RF CMOS compatible GMR based STOs show good wafer uniformity
Timeline (When exploitable or when foreseen in production)	3-5 years

Spin Torque Microwave Detectors

Technology	Spin Torque Microwave Detectors
Gain Signal/Noise ratio Non-linearity	N/A High signal, noise reasonably good Mostly linear
Speed Power consumption	Very fast, >1 GHz expected Low
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	CMOS compatible, embeddable, modular
Other specific properties	Ultra wide band, Nano size, Good spectral resolution
Manufacturability (Fabrication processes needed, tolerances etc.)	RF CMOS compatible
Timeline (When exploitable or when foreseen in production)	3-5 years

7. Topic 5: Nanowires

Speaker: Heike Riel
Discussant: Isabelle Ferain
Rapporteur: Androula Nassiopoulou

7.1. Working group report

The current MOSFET technology evolved through miniaturization. Further scaling down is limited by several factors:

- By reducing the gate length, the fraction of charge controlled by the gate decreases.
- The finite number of dopants in source-drain region increases device variability
- Reduction of the oxide thickness increases the gate leakage current
- V_T shift, DIBL and increased inverse sub-threshold slope are observed. The minimum inverse sub-threshold slope S is limited by thermally broadened source Fermi function, so as thermal emission imposes a limit to the present transistor/switch technology.
- Power consumption per chip increases by scaling down and leakage power dominates in advanced technology nodes. V_T scaling is saturated by the 60mV/dec physical limit and voltage scaling is slowed (1.2V at 90nm technology node, 1V at 45nm, 0.8V at 22nm etc.).

Since the electrostatic control of the channel depends on the gate architecture, alternative architectures are currently investigated. The electrostatic control of the channel is higher and geometrical scaling is improved when passing successively from the planar FET to the FinFET and the nanowire transistor (NW FET). In NW FETs extreme scaling of the dielectric is not necessary and reduced leakage current is obtained with thicker oxide.
Examples are the gate-all-around (GAA) NW FET and the tunnel FET. In the GAA NW FET the scaling behavior is improved compared to planar fully depleted devices. With the GAA geometry there is ~ $2{,}5xL_{eff}$ benefit at constant short channel effects. The GAA FET is considered as the ultimately scaled device.
The dynamic power dissipation of a FET device is proportional to the third power of the applied voltage: $P_{dynamic} \sim V^3$. Steep turn-on characteristics S are essential for low power devices. In an ideal switch $S \approx 0$mV/dec. In a MOSFET S is limited to $S \approx 60$mV/dec., while a steep sub-threshold slope switch has to slow $S<<60$mV/dec. Towards decreasing S, the following devices were investigated so far: ferro-FET, electromechanical FET, tunnel FET and impact ionization FET. Tunnel FET (T-FET) is considered to be the most promising small switch for V_{dd} scaling. The first T-FET with $S<60$mV/dec is a carbon nanotube T-FET (demonstrated S~40mV/dec). The disadvantage of T-FET is that the on-current depends on the tunneling probability.

Open issues

Theoretical understanding of the underlying physics, material science, etc. is necessary. The interplay of the physical properties of nanowires (electronic, optical, thermal, mechanical e.g. strain, Interfaces, interface states, Surface chemistry etc) still needs investigation and the effect of those on device operation and mechanism. The effect of variability on integration is an open question.
Fabrication is another issue, top-down versus bottom-up, catalyzed or non-catalyzed growth, contacts, etc.
Metrology, testing and modelling of nanowires are also partially open issues.

Conclusions

Material/device strengths and challenges can be summarized as follows: Grown Si NWs possess severe limitations for logic applications. Top-down gate-all-around Si NW FET is the ultimate-scaled FET, and on the other hand T-FET is currently the best candidate for steep slope switch. In fabricated

only using silicon, all-Si Tunnel FETs are limited by large bandgap and III-V heterostructure Tunnel FETs seem to be the best device option.
T-FET strengths are in low voltage – low power and architecture compatibility. The challenges are in experimental verification which is needed for optimized devices and in theoretical modeling which needs to be improved in order to enable prediction of the device performance. Combined circuit and device optimization is needed, since the best discrete device may not give best circuit performance.

7.2. Benchmarking table

Table I – Tunnel FET

Technology	**Tunnel FETs**
Gain **Signal/Noise ratio** **Non-linearity**	Similar functionality than MOSFET but promises lower voltage and lower power consumption, I_{on} may be smaller, Potentially better noise margin and high gain at extremely low current/voltage
Speed **Power consumption**	Depends on the I_{on} that can be achieved, probably not faster, maybe a little bit smaller Lower power consumption
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	Similar architecture, some circuit changes needed, may have density penality but there is room for new clever circuit designs.
Other specific properties	
Manufacturability **(Fabrication processes needed, tolerances etc.)**	SiGe TFET CMOS compatible, Integration of III-V heterojunction TFETs need more work but should be possible, junction quality, interface states, self-alignment critical, variability may be more critical due to exponential dependence of tunneling, V_T variation, doping tails and stochastic behavior of doping, high-k gate stack…
Timeline **(When exploitable or when foreseen in production)**	On the roadmap after GAA and conventional III-V → 5-10 years

Junctionless NW FET (JNT)

Technology	Junctionless Nanowire Field Effect Transistor (JNT)
Gain, Signal/Noise ratio **Non-linearity**	Not investigated yet (single-device characterization)
Speed **Power consumption**	CV/I: lower Miller capacitance than inversion mode FETs, SS~60mV/dec at V_{dd}=1V, I_{on} similar to IM FETs (contact resistance is the main issue!)
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	Same as FinFETs/GAA NW: high density required SOI is the substrate of choice (thermal dissipation issues?) Bulk Si OK
Other specific properties	
Manufacturability **(Fabrication processes needed, tolerances etc.)**	Fully CMOS compatible, no need for ultra- shallow junction engineering. Need for SOI thickness and LER control
Timeline **(When exploitable or when foreseen in production)**	Outperforms bulk Si GAA IM FETs at gate lengths < 25nm (in terms of SCE control), σ_{VT} being addressed,

8. Topic 6: Memristors

Speaker: Julie Grollier
Discussant: Dag Winkler
Rapporteur: Clivia M Sotomayor Torres

8.1. Working group report

Characteristics of Memristors:

- It exhibit a pinched or zero-crossing I-V loop as necessary but not sufficient condition.
- A resistive component the operation of which is via Spike Timing Dependence Plasticity (STDP), like artificial synapsis with potential for Hebbian learning..
- Array of devices form an artificial neural network. A possible architecture is based on a 2-bar approach with potential for huge interconnectivity.
- Main mechanism is via motion of atoms and ions, i.e., motion of "defects" in, eg, oxides (electromigration). However, there are purely electronic versions of memristors.
- Low energy operation expected in parallel analogue computation, e.g., neuromorphic computing. So far local heating is a problem.
- Interest due to expectation that each device can learn in unsupervised manner.
- Device manifestations: non-volatile memories, logic functions
- There are organic MRs and operation is via resistive switching

1) Key questions raised

o Considering the materials and physical changes required for operation, how reproducible is, e.g., electromigration? What defect tolerances are acceptable?

o Given the predominance of transport mechanisms, how reversible is the thermodynamical process involved?

o States are perhaps affected when Reading them. How many readings are possible?

o Concerning switching, concerns include:

- I-V loops indicate large dissipations and therefore local heating impacting on energy consumption.
- Extent of co-firing and fan out
- Scalability bounds
- Cooling strategies

o What new architecture will be needed, considering that each device will vary and therefore can learn a different thing. A suitable architecture will need to handle these variations, especially if they exceed 100 nA-1 uA. A possible architecture is a 2-bar technology going from 2- to 3-dimensions.

o What is the killer application? Is its pattern recognition (CMOS "neuron" + memristor "synapses"?

2) Degree to which benchmarking criteria were met: Memristors were benchmarked for two kind of devices (see tables).
It was mentioned that if massive parallel architecture became possible then speed would not be important. The same would apply to retention time.
The organic MRS are seen as Beyond beyond CMOS in terms of time scales.

3) Strength and weaknesses of presented technology/ies.
Memristors are controversial in terms of definitions and the claim of being the 4th element in electronic circuits. It seems that much remains to be understood among memrisitros experts themselves. Once agreement on definitions is reached, clarity will emerge with respect to the claims of main functions enabling comparison and benchmarking to the two types odf devices benchmarked here.

One of the main strengths is the prospect for neuromorphic computing.

Open issues

Those raised in the benchmarked tables to prioritise functions and reach agreement on a killer application.

Recommendations

Support device- or function-oriented research. A strong candidate presented was the spintronic memristor but much needs to be understood.

Conclusions

The topic is clearly one that generates lively debate both in terms of definitions and relative merits of prospective applications. Given that one of the potential avenues heavily depends on architectures and design, memristor technologies may be good candidates for a SWOT analysis combining design and technology.

8.2. Benchmarking table

Technology	**DIGITAL MEMRISTORS**			
	Phase Change Memories	Red-ox	Ferroelectric Tunnel Junction RAM	Spin Torque RAM (STT)
Gain **Signal/Noise ratio** **Non-linearity**	N/A			
Speed **Power consumption**	50 ns 6 pJ	10 ns < 1 pJ	10 ns 10 fJ	25 ns 0.02-5 pJ
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	6 F^2	5/8 F^2	5/8 F^2	20/40 F^2
Other specific properties: • **prototypes** • **forming step** • **switching** • **good theoretical understanding**	Commercial No Unipolar yes	Some Some Both No	-- No Bipolar Yes	Yes No Bipolar Yes
Manufacturability (Fabrication processes needed, tolerances etc.)	CMOS compatible			

Timeline (When exploitable or when foreseen in production)	Available	< 5 years	?	< 3 years

Technology	**ANALOGUE MEMRISTORS**					
	PCM	Thermal Chemical Mechanism Red-Ox	Valency Change Mechanism Red-Ox	Electrochemical Metallisation Red-Ox	Spin Torque RAM	Organic
Gain **Signal/Noise ratio** **Non-linearity**	N/A					
Speed **Power consumption**	5 ns 6 pJ	10 ns < 1 pJ			25 ns 0.02-5 pJ	Ms ?
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	6 F^2	5/8 F^2			20/40 F^2	?
Other specific properties: • **Forming step** • **R_{off}/R_{on} (crossbar)** • **Operation : bipolar makes STDP synaptic change easier** • **Retention time** • **good theoretical understanding**						
	No	No	Yes	No	No	No
	> 50	?	$>10^3$	$>10^7$	>6	?
	unipolar	unipolar	bipolar	bipolar	bipolar	bipolar
	10 years					1 hr
	Yes	No			Yes	No
Manufacturability (Fabrication processes needed, tolerances etc.)	CMOS compatible					
Timeline (When exploitable or when foreseen in production)	Still in basic R&D					

9. Topic 7: Graphene

Speaker: Jari Kinaret
Discussant: Dimitris Pavlidis
Rapporteur: Lars Hedrich

9.1. Working group report

Graphene is a material, emerging very few years ago. The research is rapidly evolving, the properties and applications become more and more visible. In our workshop we had a lively presentation of Jari Kinaret on graphene preceded by an overview talk from the same person about the European flagship pilot action on graphene. Started and motivated by Dimitris Pavlidis, the discussion focuses on manufacturing and transistor performances topics. The subsequent workshop discussed and formulated the properties of graphene technologies with respect to the benchmark questions from the Nanotech project. In the following you will find a summary of the talk, discussions and workshop-benchmark results.

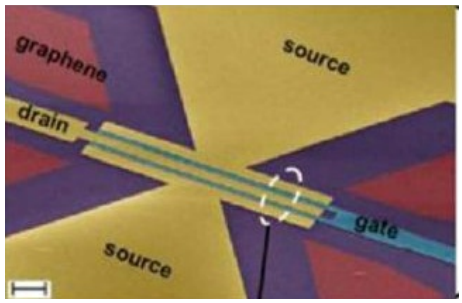


Figure 9.1: Possible Graphene FET-Layout

Graphene is a mono-layer material with very good mobility (up to 200000 cm²/Vs, a high velocity saturation ($4*10^5$ m/s) and in unmodified state an ambipolarity. The ambipolarity has a strong impact on **gain** being very small, if no bandgap is opened with additional techniques. These techniques, e.g. chemical modification, nano ribbons or bi-layer graphene, are now under investigation. It is not clear, which will be the best without leading to a large degradation of other properties like the advantageous mobility. The resulting Ion/Ioff ratio in the pure case is in the range of 2..10. On the other hand, the good mobility offers high **speed** devices which have been already demonstrated in the 300 GHz area and are expected to go up to 1 THz. This opens applications in RF-analog range. Due to the poor gain, but high conductivity, the **power** consumption can be assessed twofold: The low off current would lead to excessive leakage currents, while the good conductivity would result in low power dissipation of the active device (e.g. quite helpful for analog RF).

The **integrability** and **manufacturability** of the devices are in principle shown with demonstrators (see Figure 9.1). It is planar friendly and compatible with CMOS. However, there are issues with mobility degradation depending on the substrate and the gate oxide. The latter is under strong investigation and research. Possible gate materials are BN (today: transfer technique) and suspended gates. Another candidate for optimization is the deposition of graphene on the substrate: Today, many techniques with different influences on the final graphene structure exists, e.g. exfoliation, CVD, SiC and chemical synthesis.

Graphene is seen to have its much strength in special **applications,** which are discussed here together with **timeline** estimations**.** Optical applications range from ITO replacement (absorption 2.3% per layer), solar cells to lasers. They can make use of the very good conductivity of a very thin layer of material. Introduction of first prototypes are expected to start in 2013-14. Another wide application

field will be printable electronics. An ink will be commercial available 2012, while first transistors fabricated with oxidized graphene could be expected in 2013. Applications can take advantage from the ambipolarity like RF-mixers. General analog electronics will need better gain and can be expected in 2020, while digital standard-cell based electronics will be done the latest (2025) due to substantial research requirement of an improved off state of the device.

Conclusions and recommendations

Graphene has a very high potential in being used in optical applications. Industrial applications are seen in the very near future. However for a replacement of the standard digital FET the timeline is even longer due to up to know not realizable low off currents. Hence the research and development of graphene should definitely be pushed due to advantages - very good conductivity - in optical applications combined with the hope, that further investigation leads to solutions for the existing challenges for the use in analog and digital applications.

9.2. Benchmarking table

Technology	Graphene
Gain **Signal/Noise ratio** **Non-linearity**	Poor, would benefit from gap Unclear which way is best to open the gap. Candidates are: Chemical modification, Nano Ribbons, Bilayer Graphene or live without a gap
Speed **Power consumption**	High up to THz (fT, fMax little bit lower) Off state is problematic; On state is good; Ion/Ioff: 2..10; Analog RF quite good
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	Planar friendly, Have been demonstrated, Issues: Mobility dependent on substrate, Gate oxide Contacting > Si
Other specific properties	Optical appl.: ITO replacement, solar cells, lasers ; printable electronics, Ambi-polarity, BISFET
Manufacturability (Fabrication processes needed, tolerances etc.)	In general compatible to CMOS: Issues: Deposition, gate oxides: BN (transfer), suspended gate
Timeline (When exploitable or when foreseen in production)	Prototypes: Printable electronics (Transistors) 2013, Optoelectronics 2013-14 , Electronics: Analog 2020 , Digital 2025 Ink commercial available 2012

10. Panel Discussion on Design

Chair person: Dan Herr
Introduction speaker: Diederik Verkest
Discussants: Paolo Lugli, Sandip Tiwari, Lars Hedrich

In his introduction Diederik Verkest briefly described the design tools and challenges in scaling of CMOS circuits. Regarding the Beyond CMOS devices, he stressed the importance of systemability, meaning "The ability to economically design and manufacture reliable systems from the interaction of devices fabricated in a given technology" with system standing for "computation, storage, interconnects and input/output". The big challenge to the Beyond CMOS devices arises from the lack of understanding of the physics of the operation, large variance of the properties and in reproducibility. Also, interconnects and contacting nanoscale objects, not to speak about other variables than charge, pose a huge challenge both for design and technology. According to Dr. Verkerst out of the benchmarked topics nanowires, spintronics, memristors and graphene can be integrated within the current CMOS, MEMS, molecular devices and graphene "on top" and quantum computing is clearly beyond the CMOS platform.

Dan Herr put forward the idea of learning from nature, both for design and fabrication and for signal processing. In all these fields nature is orders of magnitude more efficient than the best processes in semiconductor industry today. "Nature's ability to leverage miniaturization and functional diversification provides clues for developing convergent nature aware design and fabrication options" was one of the key messages.

In their comments the panelists stressed the importance of the easiness of the use of the designing tools and, again, the importance of understanding the underlying physics. The phenomena arising from the decreasing dimensions need more complex physical models, moving from continuum models to quantum mechanics to ab-initio models, and combining these with design tools is not straightforward.

11. Recommendations

The series of NANO-TEC workshops, workshop 1 to identify the main requirements for future ICT devices, workshop 2 for Benchmarking of new beyond CMOS device/design concepts and workshop 3for SWOT analysis of the benchmarked devices form a unique exercise in advancing the research of future emerging devices in Europe.

During the Workshop it became evident that the Beyond CMOS devices span from medium term to long term and even longer term with examples, such as nanowires which may be implemented into current CMOS platform to single molecule approaches which may never become viable. Devices building on non-charge based variables form another interesting, yet unexplored, field, possibly with the exception of spintronics.

Recommendations arising from the 2nd NANO-TEC Workshop

- In general, there is a need to refine the benchmarking methodology to cover a wider range of Beyond CMOS technologies and design approaches. This became clear in the case of technologies that are apparently more suitable to application in specific devices as opposed to those specific to a given state variable and a new communications paradigm. An approach solely based on the switching function of FET-like devices is too restrictive, as is one exclusively based only on memory functions. An extension of the benchmarking method is therefore a clear research need for Beyond CMOS devices and architectures.

With to specific technologies the recommendations arising from the 2nd NANO-TEC workshop are:

- Continue research in *molecular electronics* to gain insights in the behaviour and potential of molecules as building blocks for information processing devices accompanied by efforts in design. In this way advances will be made in architectures for molecular devices, switches and memories, as well as in neuron inspired devices.

- With respect to *MEMS/NEMS* with the use of the third dimension is one of the most important characteristics with a large exploitation potential since it would make possible (i) to integrate specific functions aided by design tools and simulations designed to manage complexity with a systems approach, (ii) to enhance performance with respect to cost and volume (iii) to miniaturize a complete autonomous and long-lived system. The application specificity of MEMS/NEMS requires a device specific benchmarking.

- In *quantum computing* it is not clear which will be the "winning" technology for qubits: Josephson junctions, quantum dots or single spins? Robustness, method of isolation from external noise sources and at least 100 of qubits are needed for quantum computing to be useful. New algorithms are needed for, e.g., error correction, which may consume most of the computing resources. Increasing the number of qubits while maintaining the current decoherence rate should be considered as the key indicator for monitoring progresses in quantum computing. The integration on Si platforms is viewed as an essential step for quantum computing.

- For *spintronics*, the reliability issue of thermally assisted MRAMs was perceived as essential (noise, fluctuations, scaling limits) but.there is no single answer since this issue is associated with the "electromagnetic recording trilemma".

- With respect to *nanowires*, theoretical understanding of the underlying physics, material science is necessary. The interplay of the physical properties of nanowires (electronic,

optical, thermal, mechanical, e.g., strain, Interfaces, interface states, surface chemistry, and associated metrology) still require investigation their effect on device operation and on variability, both of which impacting on architectures and integration prospects.

- Concerning *memristors* the material and physical changes required for operation need to studied with respect to defect tolerances and the reversibility of the thermodynamic processes involved. For switching functions the I-V loops indicate large dissipations and therefore local heating impacting on energy consumption needs to be address as well as co-firing and fan-out. New architecture will be needed, considering that each device will vary and therefore can learn a different thing. A killer application needs to be found and one possible example is pattern recognition based on a CMOS "neuron" together with memristor "synapses".

- In *graphene* research, reliable techniques to open a gap are high in the agenda as otherwise gain is too low. Such techniques should degrade other advantageous properties. Due to the poor gain, but high conductivity, the power consumption can be assessed two-fold: The low off current would lead to excessive leakage currents, while the good conductivity would result in low power dissipation of the active device. This is a clear case where benchmarking needs to be refined for specific applications.at this stage given that for a replacement of the standard digital FET, the timeline is perceived as being too long.

- The design tools for the beyond CMOS devices have to have multiphysics and multiscale characters. Without proper tools the true exploitation of the emerging devices in ICT will become extremely difficult or even impossible.

12. Annex I: Workshop Program

Workshop 2 Program

Thursday 13 October 2011

08.30-09.00 Registration

09.00-09.05 Introduction to day 1

Jouni Ahopelto - VTT Technical Research Centre of Finland, and Mart Graef - Technical University of Delft

09.05-10.05 Session 1 – Molecular Electronics
Speaker: Dominique Vuillaume – CNRS, Lille, France (35 minutes)
Discussant: Clivia M Sotomayor Torres - Catalan Institute of Nanotechnology,Barcelona, Spain (5 minutes)
Rapporteur: Jouni Ahopelto - VTT Technical Research Centre of Finland,
Group discussion (20 minutes)

10.05-11.05 Session 2 – MEMS
Speaker: Lina Sarro - Technical University of Delft, The Netherlands (35 minutes)
Discussant: Piotr Grabiec - Institute of Electron Technology, Warsaw, Poland (5 minutes)
Rapporteur: Danilo de Marchi -Politechnic Univerity of Turin, Italy
Group discussion (20 minutes)

11.05-11.30 Snapshot poster introduction
Speakers: all attendants presenting a poster

11.30-12.00 Coffee Break & Posters

12.00-13.00 Session 3 – Solid-State Quantum Computing
Speaker: Jaw-Shen Tsai - NEC &The Riken Institute f. Phys. and Chem. Research, Ibaraki, Japan (35 min.)
Discussant: Wolfgang Porod - University of Notre Dame, IN, U.S.A. (5 minutes)
Rapporteur: Isabelle Ferain, Tyndall National Institute-University College Cork, Ireland
Group discussion (20 minutes)

13.00-14.00 Session 4 – Spintronics
Speaker: Johan Åkerman - University of Gothenburg & NanoSC, Sweden (35 minutes)
Discussant: Christian Pithan - Forschungszentrum Juelich GmbH, Germany (5 minutes)
Rapporteur: Mart Graef - Technical University of Delft, the Netherlands
Group discussion (20 minutes)

14.00-15.20 Lunch and Networking

15.20-16.20 **Session 5 – Nanowires**
Speaker: Heike Riel - IBM, Zurich, Switzerland (35 minutes)
Discussant: Isabelle Ferain- Tyndall National Institute at University College Cork, Ireland (5 minutes)
Rapporteur: Androula Nassiopoulou - National Centre f. Scientific Research "Demokritos", Athens, Greece
Group discussion (20 minutes)

16.20-17.20 **Session 6 – Memristors**
Speaker: Julie Grollier - Centre National de la Recherche Cientifique-Thales, Palaiseau, France (35minutes)
Discussant: Dag Winkler - Chalmers University of Technology, Gothenburg, Sweden (5 minutes)
Rapporteur: Clivia M Sotomayor Torres - Catalan Institute of Nanotechnology, Barcelona, Spain
Group discussion (20 minutes)

17.20-17.50 **Coffee Break & Posters**

17.50-18.00 **Guardian Angels" - a short introduction to the Flagship pilot coordination action**

Speaker: Heike Riel - IBM, Zurich, Switzerland

18.00-18.10 **Graphene-CA" - a short introduction to the Flagship pilot coordination action**

Speaker: Jari Kinaret - Chalmers University of Technology, Gothenburg, Sweden

18.10-19.10 **Session 7 – Graphene**
Speaker: Jari Kinaret - Chalmers University of Technology, Gothenburg, Sweden (35 minutes)
Discussant: Dimitris Pavlidis - Centre National de la Recherche Cientifique, IEMN Universite de Lille, France (5 minutes)
Rapporteur: Lars Hedrich - University of Frankfurt, Germany
Group discussion (20 minutes)

19.10-19.30 **Wrap-up and conclusion of the day. All rapporteurs (5 minutes each)**

20.30 **Workshop Dinner**

Friday 14 October 2011

09.00-10.30 **Panel Discussion on Design**
Chair person: Dan Herr, Semiconductor Research Corporation, Research triangle Park, NC, U.S.A.
Introduction speaker: Diederik Verkest, Interuniversity Microelectronics Center – Leuven, Belgium
Discussants: Paolo Lugli - Technical University of Munich, Germany

Sandip Tiwari - University of Cornell, NY, U.S.A
Lars Hedrich- Johann Wolfgang Goethe-Universität, Frankfurt am Main, Germany

10.30-11.30 Parallel working groups on Molecular Electronics, MEMS, and Solid State Quantum Computing

Three separate rooms, maximum 15 participants per session, chair persons to be confirmed

11.30-11.50 Coffee Break & Posters

11.50-12.50 Parallel working groups on Spintronics and Nanowires

Three separate rooms, maximum 15 participants per session, chair persons to be confirmed

12.50-13.50 Parallel discussion on Memristors and graphene

Three separate rooms, maximum 15 participants per session, chair persons to be confirmed

13.50-14.20 Conclusions of working groups by rapporteurs (5 minutes each)

14.20 Closing remarks of workshop 2, Next steps and announcement of Workshop 3

Jouni Ahopelto - VTT Technical Research Centre of Finland, and Mart Graef - Technical University of Delft