spin Orbit torque memory for cache & multicore processor applications

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D1.1 Project Presentation

Responsible Toplink Innovation (C. BREMOND)

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Particip.	Participant organization name	Short name	Country
1 RES 1	CNRS Spintec	CNRS	France
2 RES 2	Catalan Institute of Nanotechnology	ICN	Spain
3 RES 3	Karlsruher Institut für Technologie	KIT	Germany
4 RES 4	National Center for Scientific Research Demokritos	NCSR D	Greece
5 RES 5	CEA LETI	LETI	France
6 IND 1	In Silicio	INSIL	France
7 IND 2	Singulus	SING	Germany
8 OTHER 1	Toplink Innovation	TLI	France
No.	**Advisory Board member**	**Short name**	**Country**
TAB 1	Micron Technology	MICRON	Italy
TAB 2	Tower Semiconductor	TOWER	Israel
TAB 3	European Nanoelectronics Infr. for Innovation	ENI2	Europe

Work programme topics addressed

Objective ICT-2011.3.1: Very advanced nanoelectronic components: design, engineering, technology and manufacturability

a) "Beyond CMOS technology"

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Abstract

This Project Presentation is a short description of spOt objectives, goals, approach, expected results and participants. The purpose of this document is to use it for dissemination of spOt and all the information included here is also included in the project web site: www.spot-research.eu

spOt STREP Project 318144 “spin Orbit torque memory for cache & multicore processor applications”, was selected to be funded by the European Commission within the ICT-2011-8 call of the Seventh Framework Program.

This project addresses the sub-objectives 3.1: Very advanced nanoelectronic components: design, engineering, technology and manufacturability and more particularly a) “Beyond CMOS technology”. The total budget of the project is 4 420 768 €. The project has an expected duration of 36 months, starting on October 1st 2012.

Strategic objectives addressed

- ✓ Demonstrate the relevance of SOT-MRAM for low power and ultra high speed non-volatile memory applications.
- ✓ Explore the potential of embedded SOT-MRAM for normally off / instant on advanced micro processors, paving the way towards green electronics.
- ✓ Propose a novel hybrid embedded processor architecture with hybrid memory hierarchy to show systemability of the technology.
- ✓ Implement a stand-alone memory test chip to show integrability and manufacturability of the technology.

Background

The microelectronics industry will face major challenges related to power dissipation and energy consumption in the next years. Both static and dynamic consumption (already dominated by the leakage power) will soon start to limit microprocessor performance growth. Multicore processors e.g. will not be able to afford keeping more than a very small fraction of all cores active at any given moment and their scaling will soon hit a power wall. A promising way to stop this trend is integration of non-volatility as a new feature of memory caches, which would immediately minimize static power as well as paving the way towards normally-off/instant-on computing. The development of an electrically addressable non volatile memory combining high speed and high endurance is essential to achieve these goals. Among the recent emerging memories, Spin Transfer Torque Magnetic Random Access Memory – STT-MRAM – has been identified by the ITRS as the most credible candidate. However STT-MRAM still suffers from a lack of speed for cache application and from potential endurance issues due to the large current densities injected through the tunnel barrier for switching the magnetization.

The goal of the project is to introduce non-volatile fast memories in the core of the processors in order to develop a new class of power efficient and scalable microprocessors. To accomplish this aggressive goal, limitations of present non-volatile memories in terms of speed and endurance must be overcome and new architectures taking full benefit of these new functionalities must be developed. Would it succeed, it would imply a comprehensive modification of the memory hierarchy leading to a large reduction of power consumption and thermal dissipation. To tackle these issues the consortium will base its research on a recent discovery achieved jointly by SPINTEC and the Catalan Institute of Nanotechnology, which is called “Spin Orbit Torque” (SOT). This disruptive technology, which can be viewed as the ultimate evolution of STT, offers the same non-volatility and compliance with technological nodes below 22nm, with the addition of lower power consumption, cache-compatible high speed, and truly infinite endurance. Proof of principle has already been demonstrated on isolated cells with switching speed <0.5ns. In order to demonstrate its viability for cache, a number of identified technology roadblocks must be addressed: A magnetic stack presenting both large SOT (for write) and large Tunnel Magneto-Resistance (for read) must be developed; Writing current needs to be lowered to match advanced transistor outputs. The cell architecture must be optimized to accommodate the 3-terminal geometry. With this in hand, novel system level architectures combining logic and memory can be developed, in particular with an increased granularity of the memory within the processors.

The spOt project intends to pave the way to improved processors capabilities in terms of energy consumption and thermal dissipation allowing for example many more active cores under a fixed power budget than a pure CMOS implementation could afford.

Objectives of the project

spOt has 4 intermediate goals:

i) the realization of a fast write, low power, high read signal single memory cell
ii) the development of a single cell architecture (standard cell) with minimal footprint
iii) A stand-alone memory test chip with full functionality
iv) The full chip simulation of a low-power/normally-off multicore processor.

Would it succeed, it would imply a complete modification of the memory hierarchy leading to high performance and power efficient processors. The project is prospective and risky but with outstanding potential. When completed, it will lead to viable disruptive and highly competitive technologies for the next decade products.

Several demonstrators will validate the RTD results:

- ✓ A SOT memory test chip will be fabricated in order to demonstrate the integrability and manufacturability of this new technology (T0+36),
- ✓ The full chip simulation of a novel multicore processor integrating embedded SOT memory will be carried out, in order to demonstrate the systemability of such approach (T0+36),
- ✓ A complete key device SOT simulation software will de developed, to enable the growing spintronics industry (T0+36).

Consortium description

The consortium we have gathered is composed of 8 leading European players, coordinated by the Spintec laboratory. Synergies between partners are high and field of competences clearly established. In parallel, an Advisory Board comprising major European-based players representing IDMs (Independent Device Manufacturers) and foundries is put together to ensure optimal exploitation. The partnership is composed with:

A high level R&D team: SPINTEC (France), ICN (Spain), KIT (Germany) and NCRS-D (Greece) are four research institutions with a wealth of experience in European projects and new magnetic application developments. ICN and SPINTEC jointly discovered (and patented) the spin orbit torque effect which is at the basis of this project. The main expertise of KIT in this project revolves around robust system design, and emerging architectures for computing whilst NCSR D is a major research centre in Greece, with expertise on magnetic materials

A top CMOS technology transfer platform; LETI (France) has a longstanding expertise in the integration of magnetic materials for spintronics application using integration routes for 100 and 200mm magnetic nano-device fabrication. LETI has set-up over the years a flexible R&D clean room for the microfabrication of 100mm wafers that will be used in the project.

A close partnership with focused Small and Medium Size Companies: Social and economic cohesion will be particularly enhanced by 3 SMEs with a unique expertise in their respective business fields: magnetic simulation softwares for In-Silicio (France), magnetic deposition equipment for Singulus (Germany) and project management for Toplink (France). The project represents for those SMEs a great business opportunity and that will allow them to become reference companies in the field.

Spintec, the catalyst: Most of partners and advisory board members have a successful bilateral experience with Spintec through several European projects and are used to work efficiently together since their respective role is clearly identified. Indeed, Spintec is leading for many years strong cooperation with: ICN (on materials and magnetization dynamics), KIT (on design & architectures), Singulus and LETI (for fabrication aspects) and TLI (for projects set up and coordination). All those successful long term collaborations will benefit to the project easing a strong and efficient implementation and project management.

Detailed partners presentations

CNRS SPINTEC (Fr) : Spintec is a laboratory jointly operated by CEA, CNRS and UJF, in partnership with G-INP. It is fully dedicated to spintronics research, with the aim to bridge the gap between fundamental research and applications. It was created in 2002 and rapidly expanded to currently reach ~60 people (~25 permanent). It is located in the MINATEC campus, close to LETI facilities. Spintec brings together expertise in fundamental physics such as theory and modelling, new materials, spin-transfer torque, spin current-induced domain-wall motion and magnetization dynamics, as well as in device-oriented technologies such as CAD tools and circuit design, technology integration and functional testing. This synergy has placed SPINTEC at the forefront of spintronics research. Consistent with its mission at the crossroad of research and technology, Spintec has many connections with international laboratories and companies. Spintec has also been developing a strong collaboration with LETI for technology development and transfer to third parties. This joint effort has led to the creation of a start-up company, Crocus Technology, in 2006.

Catalan Institute of Nanotechnology (Sp) : The Catalan Institute of Nanotechnology (ICN) is a research centre of the Generalitat de Catalunya established in 2005. ICN is part of the Nanocluster of the Universitat Autonoma de Barcelona, which brings together also the Institut de Ciencia de Materials de Barcelona (ICMAB), and the Centro Nacional de Microelectrónica (CNM). This partnership constitutes one of the largest concentrations of nanotechnology institutes in southern Europe and provides access to a great number of nanofabrication and characterization facilities. ICN employs presently 140 people, of which 72% are scientific staff and 38% women, working in key aspects of nanotechnology involving magnetic materials, spintronics, quantum electronics, and chemistry. ICN has a successful track record of participation in European research programmes (18 projects) and has leveraged these collaborations to build a solid research and management infrastructure that enables it to support large-scale projects.

Karlsruhe Institute of Technology (Ge) : Karlsruhe Institute of Technology (KIT) is a higher education and research organisation established on 01/10/2009 as merger of Universitat Karlsruhe (founded in 1825), one of Germany's leading research universities, and Forschungszentrum Karlsruhe (founded in 1956), one of the largest research centers in the Helmholtz Association. Higher education, research, and innovation are the three pillars of KIT's activities. The Chair of Dependable Nano Computing (CDNC) headed by Prof. Tahoori, investigates emerging technologies for computing as well as dependability aspects in design and implementation of computing schemes using emerging nanotechnologies. The main expertise of this group revolves around design of robust system design, testing aspects of

computing systems, emerging technologies for computing, and hardware design automation.

NCSR DEMOKRITOS (Gr) : The Institute of Materials Science (IMS) and the Institute of Microelectronics, of the NCSR D (www.demokritos.gr), were established in 1987 as the key institutes of the NCSR 'Demokritos', the major research centre in Greece, related to materials preparation, processing and nanostructuring. Areas of interest are magnetic thin films for magnetic recording, sensors for memories (MRAM, STT-MRAM), semiconductor materials and micro-nanofluidics, advanced ceramics for sensors, microelectronics and energy related applications. The activities are supported by a powerful infrastructure in terms of expertise and equipment in areas such as synthesis (Thin Film using MBE, e-beam, laser ablation and sputtering and screen printing), electron spectroscopy (SEM, TEM, AFM, MFM), spectrometry (Mossbauer, EPR, NMR, FT-ERP, ICP, NQR), magnetotrasport characterization from 4.2-400 K and nanopatterning using a new VISTEC-EBPG5000plus system and device characterization.

CEA-LETI (Fr): LETI is a large organization (>800 people) with a department focused on silicon-based technology. LETI currently owns and operates a high-tech 200/300mm clean-room fully equipped with state of the art tools, which enables the fabrication of real devices on large scale wafers. This gives access to a complete line for fabrication and characterization of devices from silicon to chips. LETI brings expertise in spinelectronics nano-device fabrication and RF components materials development. It has a longstanding expertise in the integration of magnetic materials for spintronics application using integration routes for 100 and 200mm magnetic nano-device fabrication, process flow and circuits conception, above IC integration and structural and electrical characterization. To this adds a newly available 200 mm IBS deposition tool for spin electronics materials, with focus on the realization MgO based magnetic tunnel junction of low RA and high TMR. The laboratory successfully lead the European project "NEXT" to the demonstration of the feasibility of Thermally Assisted MRAM on 200mm line with international recognition.

In Silicio (Fr) : In Silicio (2004) is an Independent Software Vendor (ISV) company with the ambition to build up into a high value provider of simulation software technology and solutions for Technology Computer Assisted Design (TCAD), specially focusing on spintronics related applications, to enable equipment and device vendors to better design and manufacture innovative equipments, processes and products involving nano-scale manufacturing and/or device operation. In Silicio has already developed and is selling worldwide two highly regarded software products addressing some of the most pressing

challenges in this context (Proteus 2D & Spinflow 3D). In Silicio which has been awarded the national prize for high tech start-up company creation (French ministry of research, 2004), is rapidly growing a customer base worldwide (Europe, US and Asia/Pacific) for its software products and services offering.

SINGULUS TECHNOLOGIES AG (Ge): Singulus' Nano Deposition Technologies group was established to offer thin film vacuum deposition tools specifically for MRAM and semi-conductor technology and to be a development partner for new cell concepts. Singulus is manufacturing now the 2nd generation TIMARIS PVD bridge tool, capable of handling all wafers sizes up to 300 mm diameter. Besides producing cluster tools for all types of MRAM technology (conventional, STT-MRAM and TAS-MRAM), Singulus has shipped systems to the hard drive industry for production of thin film heads. Singulus is the only European maker of deposition tools which demonstrates high performance for STT-MRAM applications, as the unique production concept allows an efficient production with a low cost of ownership. Singulus participated together with Crocus in the NEXT-MRAM (IST-2001-37334) EU project, which provided the MRAM concept demonstration leading to the creation of Crocus – and was awarded an FP6-DESCARTES 2006 Finalist Prize for Excellence In Collaborative Research. Singulus is also a partner in the MAGWIRE-Project for the development of Magnetic Nanowires for High Density Non Volatile Memories (FP7-ICT-2009-7).

Toplink Innovation (Fr): Ideally located nearby Toulon, between Sophia-Antipolis and Aix-Marseilles famous technology areas, TOPLINK Innovation is French Private Company, delivering High-Tech Consulting Services to innovative Organizations. Its Mission consists in promoting Innovation while experiencing excellence, in order to strengthen its customers Positioning and Competitiveness, which are the European players for tomorrow (High-tech Industries and SMEs, Laboratories and Universities, Governmental Institutions). TOPLINK Innovation is staffed with expert consultants and R&D project managers, skilled in signal processing, microelectronics/nanotechnologies, embedded computing systems and information technologies. Its know-how is to facilitate Innovation and financial process during the 3 major Innovations steps: 1) Strategic Development (assessment of marketing positioning, technology and competition survey, Business planning…) 2) Innovation Management (R&D innovative projects set-up and management in partnership, skills networking) 3) Outcomes Valuation (technology licensing agreements, Industrial Partnerships, Sales Strategy).

How spOt project will change the International Play

SOT-MRAM is a new technology with the potential to impact the whole "device to system" food chain and as such we intend to cover all aspects from design tools, architectures, methodologies and paradigm. The spOt project will propose a disruptive memory targeting 2 distinct markets:

- ✓ The embedded memory applications,
- ✓ The embedded and server processors applications (as an example of high-end multicore platforms).

The consortium has therefore elected not to seek for one or several selected industrial partner within the project, but to create an advisory board with the major players covering the whole spectrum of exploitation. The board will be formed of one leading Independent Devices Manufacturer (IDM) involved in MRAM and with a strong presence in Europe (**Micron**), covering both the DRAM and microprocessor markets, the leading European specialty foundry already involved in MRAM (**Tower Semiconductors**), and the leading European semiconductor research groups (**ENI2 / Sinano Institute**).

The consortium is eager to have a strongly involved board through discussions and meetings. The Advisory Board will partner this project to:

- ✓ evaluate the work (WP1, WP4, WP5),
- ✓ give directions of where to go market-wise (WP1),
- ✓ prepare future exploitations of the project results (WP1),
- ✓ define new areas for industrial outcomes valuation (WP1),

And more generally ensure “manufacturability”, “integrability” and “systemability” of the developed solutions through WP4 and WP5.

Once the project is completed, it is expected that the technology will be licensed to one or several manufacturers. Access to the technology to SME’s and research organizations may also be possible through the use of the Eurobroker initiative. This will be evaluated near the end of the project by the Advisory Board.