



**ICT - Information and Communication Technologies**



## **Merging Plasmonic and Silicon Photonics Technology towards Tb/s routing in optical interconnects**

**Collaborative Project**

**Grant Agreement Number 249135**

# **Fabrication of SOI RF circuitry and complete SOI motherboard**

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## 1 Executive Summary

This document provides a detailed overview of the complete process flow for the fabrication of the PLATON SOI motherboard and preliminary characterization results from the evaluation of the RF lines and the IC circuit.

The description of the process flow is described in two parts; a) silicon photonics waveguides with grating couplers and b) formation of plasmonic waveguides. The co-integration of silicon photonics and plasmonics on the same chip required the development of novel "2.5D" masks that were patented by UB. The complete process flow has effectively resolved all problems that came up during the difficult task of co-integrating thermally tunable silicon photonics and plasmonic components on the same chip. Results from the latest PLATON chip reveal that the Si-part chip insertion losses are now reduced by more than 20dB compared to the first chips produced two years ago, taking advantage of a "new" grating coupler design and of improvements applied in the fabrication process. Additionally, the first results from the unpackaged SOI multiplexers are reported, showing clear resonance peaks and good uniformity of the ring resonator dimensions.

Furthermore, progress of the integrated photodiode is described. Experimental results from the responsivity and the speed of the monolithic integrated photodiodes verify that both parameters fulfill the original router specifications set in D2.4.

Finally, the results from the performance evaluation of the IC circuit and the SOI RF lines are presented. The IC is able to produce very narrow pulses, exceeding by far the specifications. In terms of output current for safety reasons, since the Cyclomer loaded plasmonic switches are not yet fully characterized, an amplifier has been added to the circuit so as to ensure enough power for optimum switching. Moreover, RF signal propagation losses over the RF lines at various frequencies are reported. In the KHz range, which is mainly of interest for PLATON RF signals, the propagation losses are lower than 2.5dB/cm, a value that is tolerable for the power budget between the IC and the plasmonic switches.

## **2 Introduction**

### ***2.1 Purpose of this document***

This document provides a detailed overview of the PLATON 2x2 router and the step-wise fabrication process that has been followed for the integration of the router's Si and plasmonic parts. Optical characterization of silicon test waveguide structures has been carried out in order to evaluate their performance and functionality. The results from the latest PLATON chip reveal that the insertion losses of the router have been reduced by more than 20dB by using an improved design of new TM grating coupler and continuous advances in the fabrication process. Besides, both static and dynamic characterization of the fabricated silicon implanted photodiodes has been performed and assessed. Moreover, results from the latest chip generations with lower-loss Si grating couplers and waveguides are reported. Finally, the performance of the IC circuit as well as of the RF interconnect lines is presented.

To this end, this deliverable aims to provide the final fabrication process needed for the integration of silicon, plasmonic and electrical components that have to be integrated for the 2x2 routing platform.

### ***2.2 Document structure***

The present deliverable is split into 4 chapters:

- Executive Summary
- Overview of the SOI motherboard:
  1. Layout of PLATON 2x2 and 4x4 router
  2. Fabrication process of the 2x2 router's Si part
  3. Fabrication process of the 2x2 router's plasmonic part
  4. Progress in PLATON's Si technology
  5. Preliminary results from unpackaged chips containing SOI multiplexers
  6. RF characterization of the monolithic Si photodiodes
  7. Performance evaluation of the IC circuit

8. Performance evaluation of the RF lines for the interconnection of the IC with the plasmonic based switch and the PDs

- Conclusions

### ***2.3 Audience***

This document is public.

### 3 Overview of PLATON's Silicon-On-Insulator (SOI) motherboard

#### 3.1 Layout of PLATON 2x2 and 4x4 router

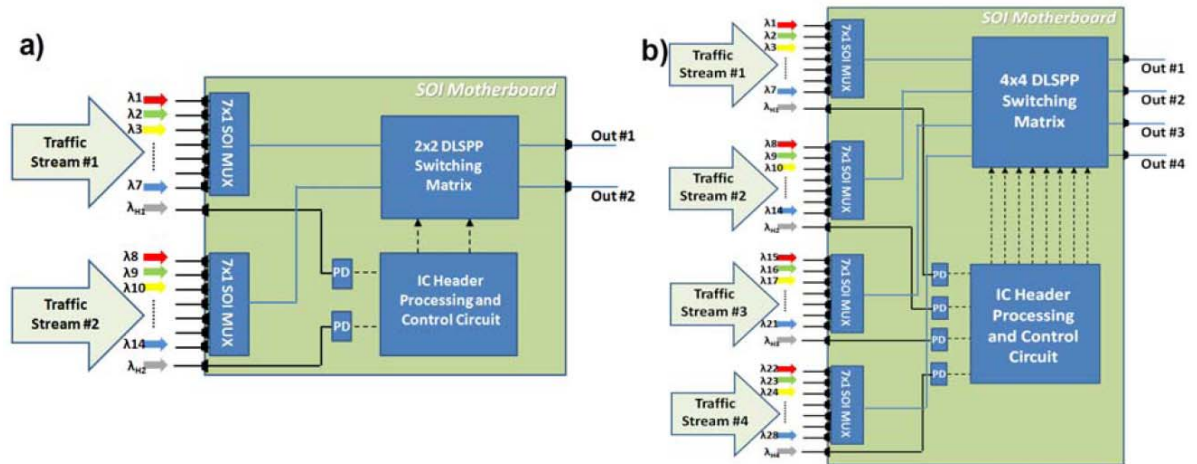


Figure 3.1: PLATON's a) 2x2 and b) 4x4 router block diagram.

Figure 3.1(a) and (b) show the block diagrams of the PLATON 2x2 and 4x4 router system, respectively, as these have been already described in detail in D2.1. Both routing platforms operate with optical data line-rates of 40 Gb/s and reside on a Silicon-on-Insulator Motherboard that hosts all the heterogeneous technologies, namely SOI-based components, Dielectric Loaded Surface Plasmon Polariton (DLSP) switches, and Integrated Circuit Microcontrollers. The 2x2 router offers an aggregate switching throughput of up to 560 Gb/s, whereas the 4x4 router provides a total throughput of up to 1.12 Tb/s.

PLATON's Silicon-on-Insulator (SOI) motherboard chip will contain silicon nanophotonic elements as waveguides, grating couplers, multiplexing circuitry, and photodetectors and will be capable to host the plasmonic switching elements and the IC control circuitry. To this end, the non-plasmonic (sub-) systems and configurations to be employed on the SOI motherboard will include the following monolithically integrated devices:

- a. **Silicon waveguides and Si-to-DLSP couplers** for guiding light in the SOI chip and interposing to the plasmonic part, respectively.



- b. **Fiber coupling structures** for allowing optical fibers to be interfaced with the PLATON routers.
- c. **Optical 7x1 MUX circuitry** capable of multiplexing up to 7 optical data wavelengths with 100GHz channel spacing into a single waveguide.
- d. **Monolithically integrated photodiodes** that will be used for the optoelectronic conversion of the packet-rate header pulses in order to drive the IC micro-controller circuit with the electrical header information.

In addition the following components have to be taken into account for the integration process

- e. **A gold lift-off chip area** to enable subsequent DLSPP waveguide writing processes, so as to allow for the incorporation of the DLSPP-based switching matrix.
- f. **An IC microcontroller circuit** to be hybridly integrated on the SOI motherboard, being responsible for processing the packet header information and for generating the appropriate electrical control signals to drive the DLSPP switching matrix
- g. **Metal interconnects** for guiding the electrical-RF signals inserted into or generated by the IC circuit and for thermal tuning of the SOI MUX circuitry.

A schematic representation of these building blocks and their positioning on the SOI motherboard is provided in Figure 3.2.

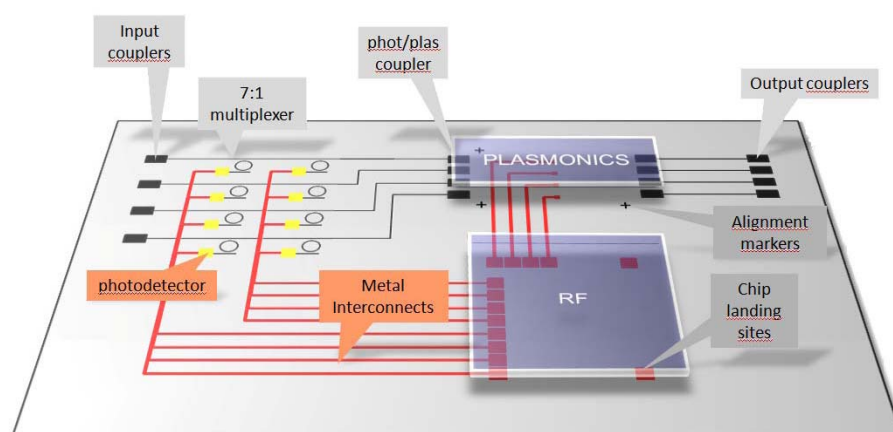


Figure 3.2: PLATON's SOI motherboard and its various building blocks.

### ***3.2 Fabrication process of the 2x2 router's Si part***

As the developed routing platform employs three different technologies, namely silicon photonics, plasmonics and electronics, compatibility between the various components and sub-systems has to be ensured in order to allow for their seamless interfacing and interoperability.

Figure 3.3 gives an overview of the realized Plasmonic Router layout, where plasmonic switches, SOI multiplexers and process control structures are highlighted. Taking this into account a special process flow, which fulfills these requirements, has been developed within the PLATON project. The overall silicon motherboard fabrication process can be performed using a so-called Mix&Match technology, which represents a combination of electron beam lithography and photolithography on 6" SOI wafers. The developed process flow is schematically depicted in Figure 3.4. The overall SOI nanophotonic motherboard foresees the integration of all necessary components such as waveguides, grating couplers, multiplexing circuits with metal heaters, RF and DC metal interconnects, and landing sites for the plasmonic and IC integration. In the following an overview of the employed process flow for the realization of the routing platform is presented.

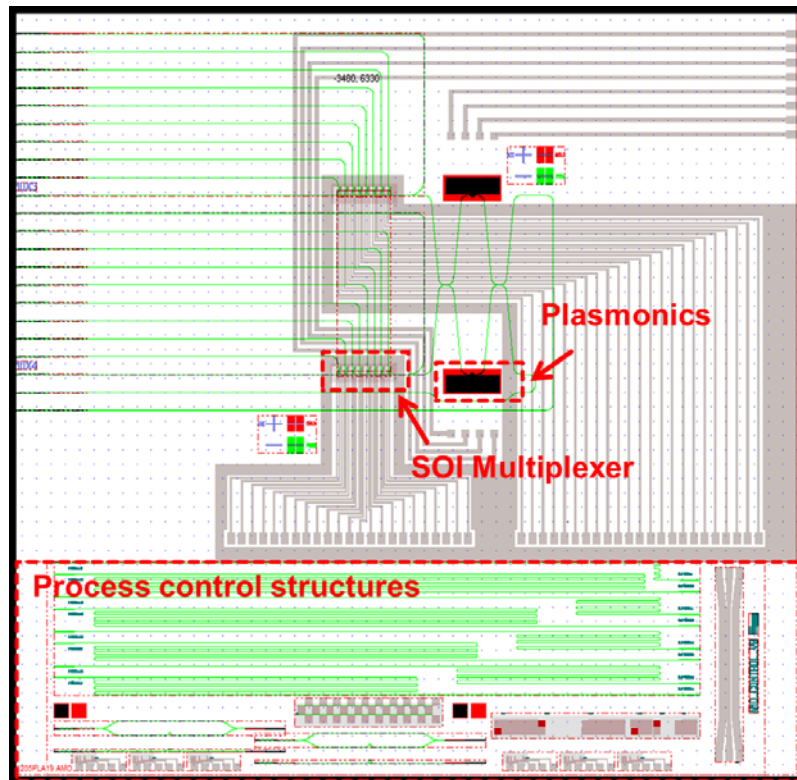


Figure 3.3: *Overview Layout Plasmonic Router: Plasmonic switches, SOI multiplexers including thermally tunable microrings and process control structures are highlighted.*

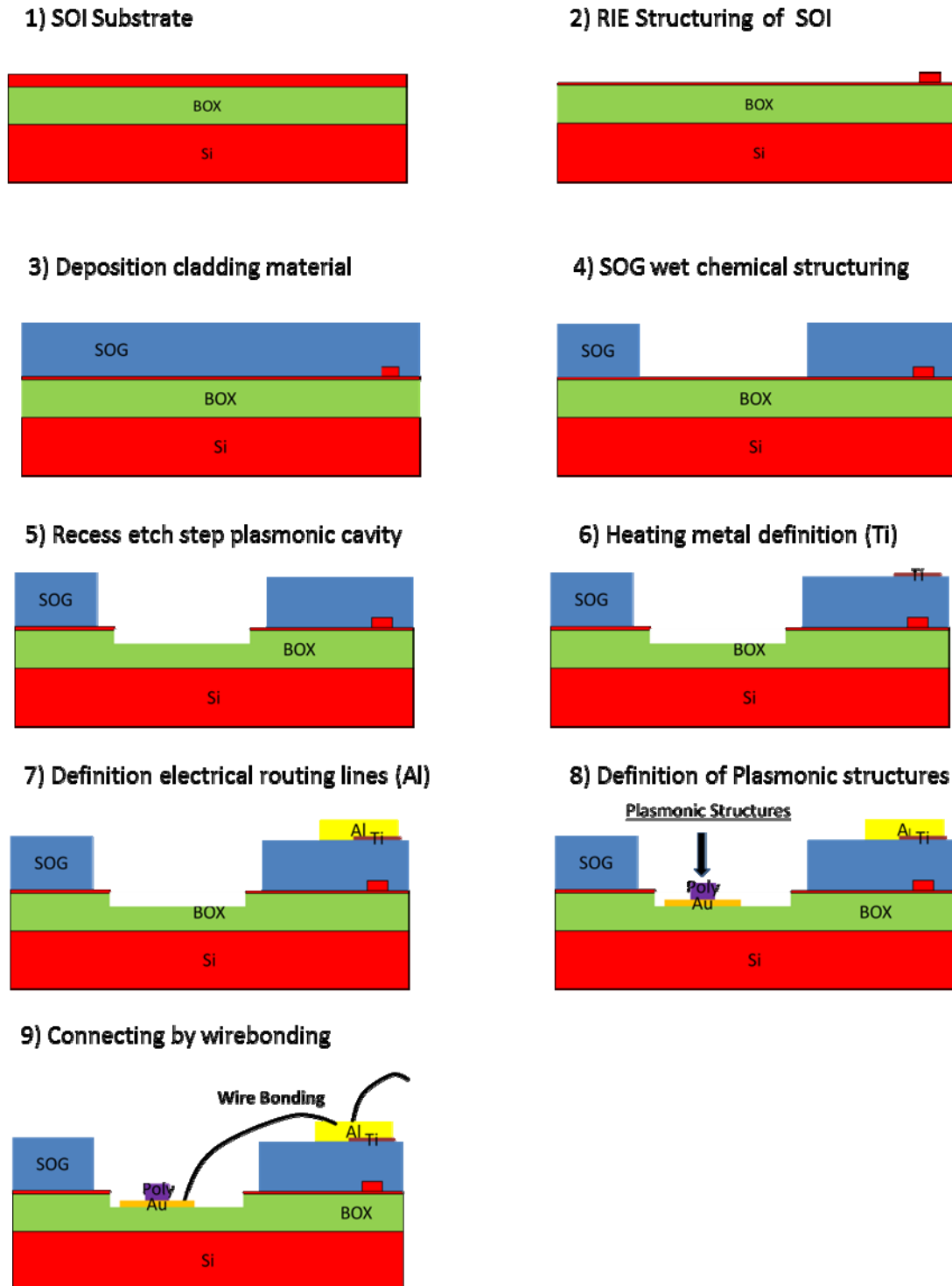


Figure 3.4: Schematic process flow for the fabrication of the Terabit plasmonic router hosted on a silicon motherboard. Connection of the different heights on the chip is carried out by wire-bonding.

The plasmonic router relies on nanophotonic rib-waveguides defined by e-beam lithography. Waveguides with 340 nm height, 50 nm slab height, and 400 nm width as a single-mode waveguide structure for TM polarization has been chosen. AMO has developed a reliable and low-loss fabrication process for SOI nanophotonic structures which guarantees excellent reproducibility. Additionally, process quality parameters such as surface roughness are optimized with respect to their influence on optical performance of the devices. The electron beam lithography (EBL) processes used to fabricate waveguides, multiplexing devices and grating couplers for fibre-chip-coupling is based on the use of hydrogen silsesquioxane (HSQ) as a negative tone resist material. An optimized high contrast development process is necessary to achieve high resolution, a step resist profile and a smooth resist surface. HSQ allows a good control of the gap width between the ring resonator and the waveguides. A reactive ion etching (RIE) process based on HBr chemistry is used for device fabrication. This process shows a high selectivity to the underlying buried oxide, smooth waveguide and resonator surfaces and a high degree of anisotropy (s. Figure 3.4(1-2)).

After patterning the SOI structures (s. Figure 3.4(3)) a 500 nm thick dielectric Spin-On-Glass (SOG) as a cladding material has been deposited. Structuring of the cladding material has been carried out by wet chemical etching (s. Figure 3.4(4)).

In order to integrate the plasmonics in a seamless way Si-to-DLSPP coupling structures have been developed to match the mode profile between the SOI and the DLSPP waveguides and thereby minimizing optical losses. For a successful integration of these structures recess etch step based on a combination of reactive ion and wet chemical etching, which defines a cavity for placing the plasmonic waveguides is necessary (Figure 3.4(5-6)).

In the next step a titanium layer is deposited and patterned to form the heating electrodes for controlling the resonance wavelength of the SOI multiplexer. Titanium is a very stable metal and serves as an efficient heater (Figure 3.4(6)). Next RF and DC metal routing lines out of aluminum are deposited and structured using a combination of RIE and wet chemical etching (Figure 3.4(7)). After definition and structuring the plasmonic part at project partner UB (see section 3.3; Figure 3.4(8)) the two different heights on the substrate are interconnected using wire-bonding by project partner SDU (Figure 3.4(9)).

In the following a detailed description of the process flow is given. After the fabrication of the nanophotonic waveguides using e-beam lithography and RIE based on HBr chemistry

a cladding material has been applied to allow the optical and electrical functionalization of the chip. The cladding material of choice is the spin-on-glass (SOG) material 512B from Honeywell. It has excellent optical and electrical properties and provides the necessary film thickness of 500nm. To enable the manufacturing of the plasmonic cavity the SOG has been structured using wet chemical etching in Buffered Oxide Etch (BOE) from Honeywell to ensure a high selectivity to the underlying silicon (see Figure 3.5).

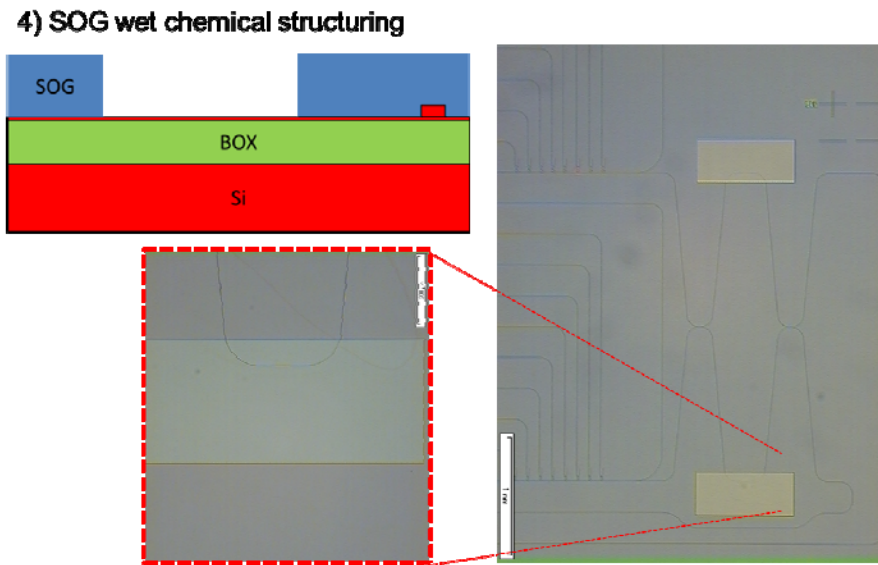


Figure 3.5: *Schematic view and microscope image of the wet chemical structuring of SOG. The SOG has been deposited on the wafer using spin-coating with a target thickness of 500nm. The SOG has then been etched selectively to the silicon by wet etching in BOE.*

In the next step of manufacturing the plasmonic cavity the top silicon layer and a part of the photonic waveguide structures have been removed. This has been done by a specifically developed RIE process based on SF<sub>6</sub> chemistry that etches both the thin silicon slab and the silicon waveguide simultaneously. The etch process has been optimized for a high selectivity to the underlying Buried Oxide (BOX) layer enabling the complete removal of the silicon without transferring the structures in the BOX layer. To finalize the plasmonic cavity the BOX layer has been under etched using wet chemical etching in BOE to satisfy the required cavity depth of 200 nm (see Figure 3.6). The etch depth has been controlled and verified using contact free ellipsometric measurements.

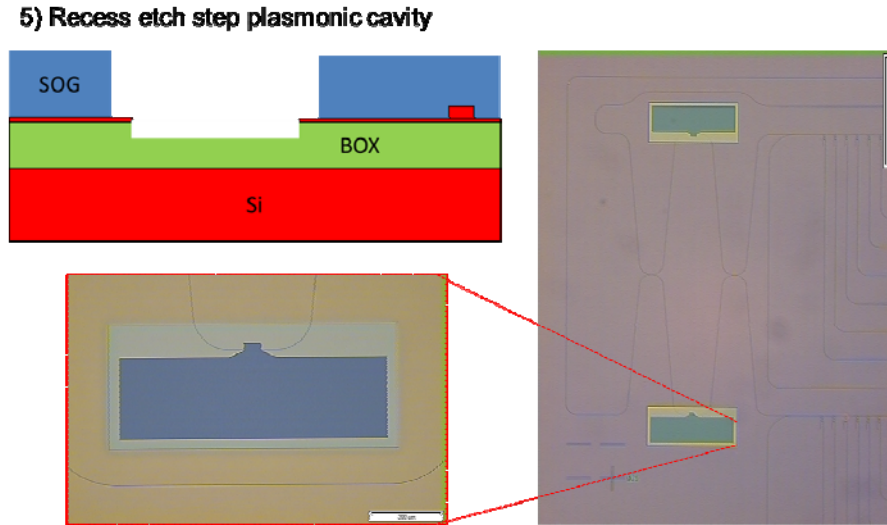


Figure 3.6: *Schematic view and microscope image of the recess etch step and the final plasmonic cavity. In the recess etch step the silicon with a part of the nanophotonic waveguide has been removed by a specifically developed RIE process based on SF<sub>6</sub> chemistry. The definition of the cavity depth in the BOX has been realized by wet chemical under etching with BOE and controlled by contact free ellipsometric measurements.*

The following definition of the heater layer has been realized by a special processing procedure to not affect the already defined plasmonic cavity. First a 110 nm thick layer of titanium (Ti) has been deposited using sputter deposition. The deposited Ti layer covers the whole wafer, including the silicon waveguide structures in the cavity region. The structuring of the heaters has been realized with two separate etch steps. In the first etch step the Ti has been pre-structured using a wet chemical solution of water (H<sub>2</sub>O), hydrogen peroxide (H<sub>2</sub>O<sub>2</sub>) and hydrofluoric acid (HF). With this etch solution Ti is etched with a high selectivity to the silicon and BOX layer which allows complete removal of the Ti from the photonic waveguides. This prevents high optical losses due to a metal contamination of the waveguides in the plasmonic structure. Because the processing tolerances of the wet chemical etching of Ti can't match the necessary critical dimensions to manufacture the final heater structures a second etch step is necessary. For this second etch step a RIE process based on chlorine chemistry (BCl<sub>3</sub>, Cl<sub>2</sub>) has been employed to define the final heater structures on the pre-structured Ti layer (see Figure 3.7). One important requirement for this process step is that the plasmonic cavity is completely covered by the photomask to prevent damage to the photonic waveguides by the etch plasma.

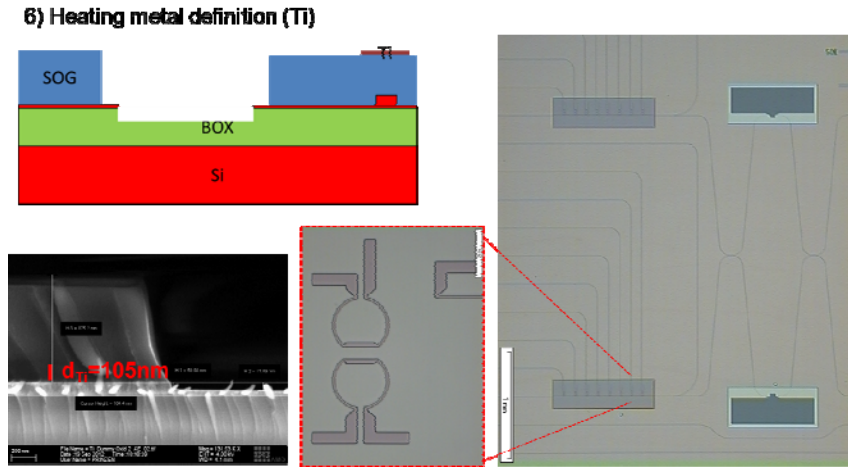


Figure 3.7: Schematic view and microscope image of the heating metal definition. The sputtered Ti has been structured in two etch steps. In the first step the Ti has been pre-structured by a wet chemical etching with an etch solution of  $H_2O$ ,  $H_2O_2$  and  $HF$ . The second RIE etch step based on  $Cl_2$  and  $BCl_3$  has been applied to define the final heater geometry.

In the final processing step the aluminum (Al) RF and DC conducting paths have been manufactured. A  $1\mu m$  thick Al layer has been deposited using a sputter deposition process optimized for smooth surfaces. Similar to the Ti deposition during the heater definition the Al is sputtered all over the wafer, also covering the photonic waveguides in the plasmonic cavity. For this reason and because of the large thickness of the Al layer the structuring of the conducting paths has been carried out with two separate etch steps. In a first RIE etch step based on  $BCl_3$  and  $Cl_2$  chemistry the Al layer has been partially etched to an etch depth of 700 nm (see Figure 3.8). The remaining 300 nm of Al have then been etched in a second wet chemistry etch step using an aluminum etch solution from Honeywell that mainly consists of phosphoric acid and provides a high selectivity to silicon.



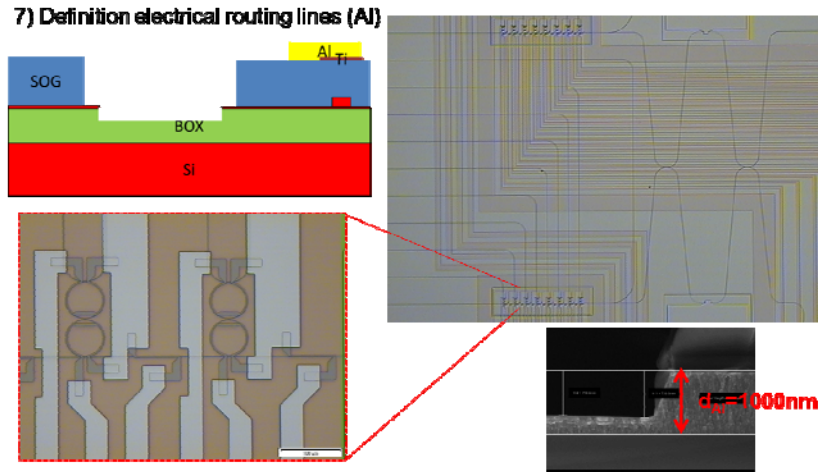


Figure 3.8: Schematic view and microscope image of the definition of the electrical routing lines. First a  $1\mu\text{m}$  thick Al layer has been deposited on the wafer using sputter deposition. The structuring of the Al layer has been done by two etch steps. First a RIE etch step has been used to partially etch the Al to a depth of 700 nm. In a subsequent wet chemical etching using an aluminum etch solution that mainly consists of phosphoric acid the remaining Al has been etched.

This processing ensures that the Al is completely removed from the photonic waveguides to prevent optical losses due to a metal contamination. The initial pre-structuring using the RIE process is necessary to ensure the critical dimension of the conducting lines and to reduce the wet etch time to prevent under etching of the photomask and damage to the structures.

After the final processing the wafers (see Figure 3.9) have been diced in  $3\times 3\text{mm}^2$  chips.

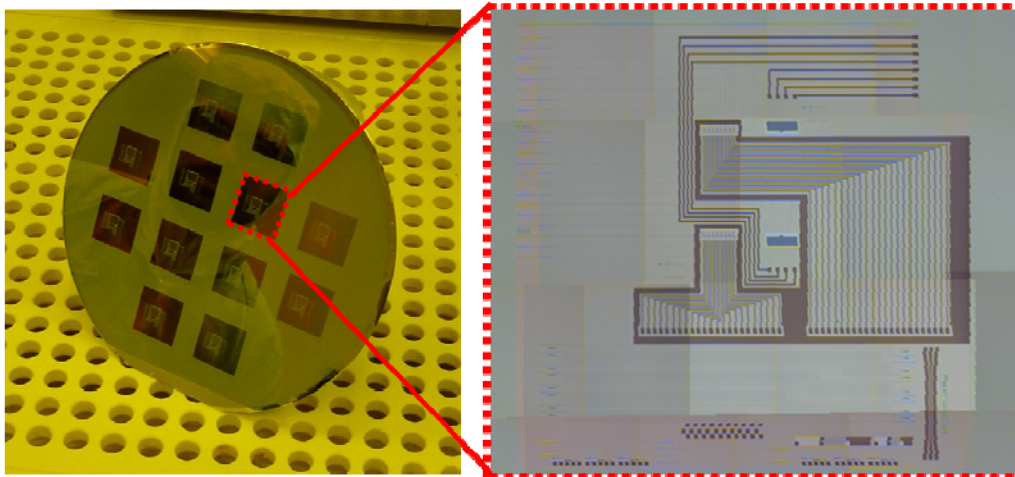


Figure 3.9: Picture and microscope image of the final wafer and chip showing the decoration of the wafer with a total of 12 dies (nanophotonic structures may only be present on several chips) and the final structures on the chip.

After completing AMO's fabrication part of the plasmonic router an optical characterization of the process control structures to analyze the performance and functionality of the silicon nanophotonic devices have been carried out. Optical test structures consist out of SOI rib waveguides of different lengths, which allow the analysis of grating coupler performance and linear waveguide losses by using the cutback method. Geometrical parameters of waveguide cross-sections and the grating couplers of these test structures are the same as for the overall realized router concept and thus can be used for a first estimation of the performance of the plasmonic router.

In Figure 3.10 the measured optical transmission as a function of waveguide length for various samples from two fabricated wafers are shown. Measurements have been carried out in the cleanroom facilities of AMO by using a conventional optical characterization setup. TM-polarized light at a wavelength of 1550nm has been coupled to and from the chip by using optical fibers. In Figure 3.10 the measurement results of 6 router samples (black) and the corresponding mean values (red) are depicted. A linear fit to these measured values results in a mean linear waveguide loss of  $\alpha_{\text{MEAN}}=5.14\text{dB/cm}$  and a mean fiber-to-chip coupling efficiency of  $\kappa_{\text{MEAN}}=14.7\%$ .

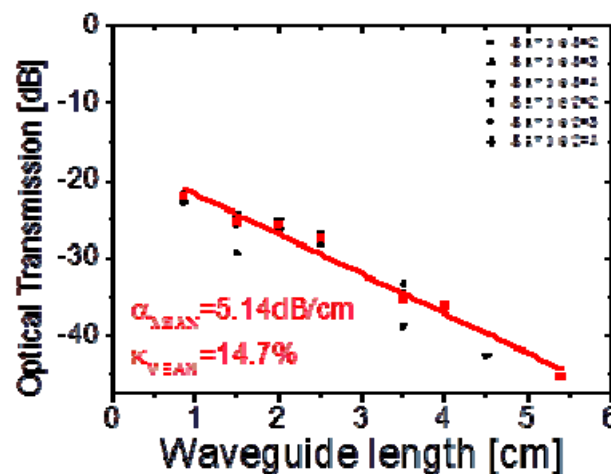


Figure 3.10: Results of optical measurements of process control structures carried out in AMO's clean room facilities. Obtained mean linear waveguide losses and fiber-to-chip coupling efficiencies are 5.14dB/cm and 14.7%.

This good optical functionality of the fabricated coupling structure and SOI nanophotonic rib waveguides proves the compatibility of the used process modules for the overall router concept and the successful fabrication of the SOI motherboard for the targeted plasmonic router.

### ***3.3 Improvements in PLATON's Si technology***

One of the major PLATON achievements throughout the duration of the project is the improvement in Silicon Photonic elements for TM polarized signals. The first generation of PLATON structures as it is illustrated in Figure 3.11(a), were exhibiting propagation losses in the Si waveguides shaped with 340x400nm<sup>2</sup> cross section and 50nm height slab in the order of ~3.5dB/cm. Also from the same figure it can be deduced that the grating couplers employed for coupling the signals in and out of the hybrid switches were imposing more than 12dB of losses. Considering that a router chip could be as long as 2cm so as to integrate the multiple switches for the formation of the higher order switching matrix, it is anticipated that the device's insertion losses just for the Si part would be ~ -33dB. This fact has imposed several problems in the applicability of PLATON technology in datacom environments where optical amplification is prohibited.

PLATON consortium anticipated this problem very early and throughout the duration of the project is constantly trying to fabricate Si waveguide with lower propagation losses through improvements in the whole process. Also it has started a research effort to design and fabricate TM grating couplers with coupling losses similar to the ones exhibited by TE ones. The results from these efforts are depicted in Figure 3.11(b) where cut-back measurements from the last PLATON chips are presented. The propagation losses in the straight Si waveguides are now reduced to ~1.5dB/cm while the coupling losses of the "new" TM grating coupler design is 4.3dB. Therefore, for the same 2cm long device, the insertion losses in the Si part of the router are reduced by more than 20dB and render feasible the error free communication between two computer nodes or servers without any need for signal amplification.

The new TM grating coupler design was developed based on a fully etched approach with a filling factor of 0.8. The grating period was 0.71 $\mu$ m, the groove width 0.13 $\mu$ m and the incident angle of the light 10 degrees. The grating was filled with Spin-on-Glass (SOG) with 800nm height. Figure 3.11(c) presents a layout of the new grating coupler's schematic cross section and Figure 3.11(d) depicts the SEM image of the fabricated one. Figure 3.11(e) presents the spectral response measured from the last batch of samples and the minimum coupling loss was recorded at 3.25dB at 1557nm, while the 3-dB bandwidth was around 32nm. The blue line in Figure 3.11(e) presents also the results obtained from simulation that indicate very good agreement between theory and experiment and that fabricated the grating couplers are only 0.5dB from their theoretical

limit. This 1-dB lower loss compared to the previous grating couplers is coming from the simpler fabrication process as for these chips only Si components were placed on the dies.

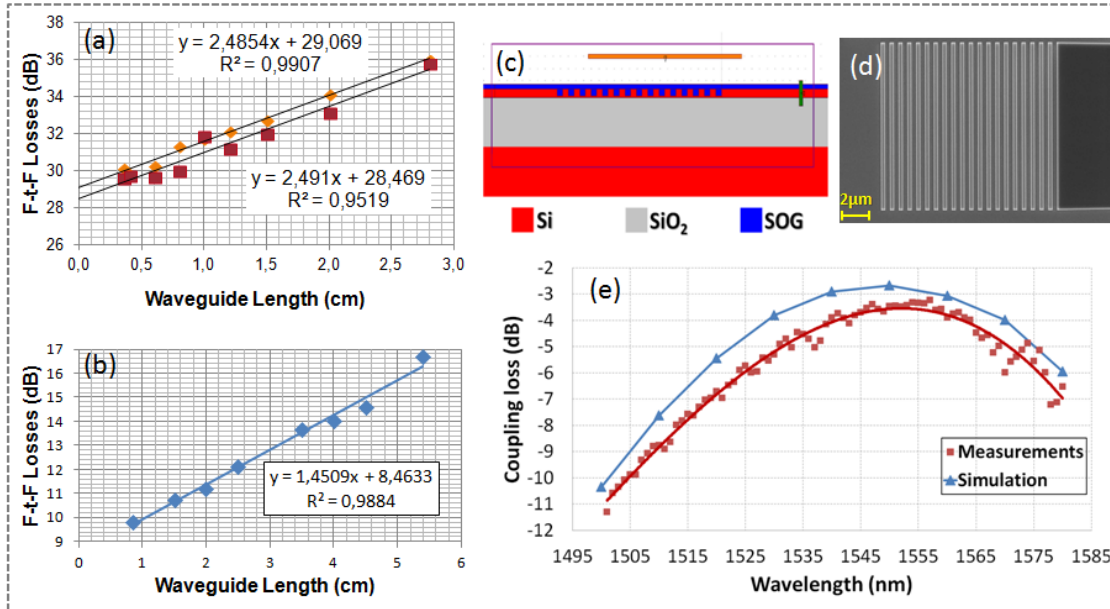


Figure 3.11: (a) and (b) Cutback measurements of TM supporting Si waveguides and Grating Couplers from the first and the last fabricated chips, respectively. "New "TM grating coupler: (c) Schematic cross sectional view, (d) SEM image, (e) Spectral responses extracted from the simulation studies and experimental results.

### 3.4 Preliminary results from unpackaged SOI Multiplexer Chips

The finalization of the fabrication process has enabled the fabrication of the first complete PLATON router chips that have been subsequently sent for packaging at IZM. However, these chips allowed for the first time due to their low losses, a preliminary characterization and performance evaluation of the two SOI-MUX circuits. The results were obtained between the input port and the 10% monitor placed at the output of the MUX that will be used at the final form of the chip for monitoring of the signal condition and MUX alignment.

Figure 3.12(a) and (b) illustrate the transfer function of Through port for both MUX1 and MUX2 designs, respectively. The resonance peaks are not spaced in a 100GHz grid and exhibit this non ideal shape with the double deeps due to the non packaged form of the chip that would allow independent access and thermal tuning of each MUX's element so

as to reach its targeted spectral position. However, the analysis of Figure 3.12(a) reveals peaks with 7 and 6.8 nm Free Spectral Range (FSR) corresponding to 12 and 11.7 $\mu$ m radius RRs, respectively, indicating a very good uniformity in the eight second order rings' dimensions and in very good agreement with the targeted radii. In the transfer function it is also evident the parabolic envelope from the grating couplers with more than 30nm 3-dB bandwidth and minimum loss at 1535 nm, consistent with Figure 3.11(e). The Fiber-to-Fiber losses of the chip were measured -25.6dB and were higher than the expected -20.5dB. These 5dB extra losses are coming from non ideal fiber array alignment and design error in the 90:10 coupler.

Figure 3.12(b) displays the spectral response of MUX2 design. The resonance peaks now have 9.17 and 9nm FSR corresponding to 9 and 9.2nm radius RRs, inline again with design specifications. The Q-factor of these peaks is not as high as in the MUX1 chips and most likely this is due to the smaller RR radius. Any slight deviation from the targeted dimensions cause now higher separation between the resonance peaks that appear as Q-factor degradation. The overall response is again dictated by the transfer function of the grating couplers centered at 1537nm with more than 30nm 3-dB bandwidth. The Fiber-to-Fiber loss was -24.5dB, while the calculated value was estimated to be again -20.5dB.

The two MUXs will be evaluated in terms of signal quality after the chip will be wire bonded and fully packaged. The connection of the 32 RRs and the 14 straight sections to external power supplies will allow to fine tune each RR's spectral position and form the 100GHz grid with the desired specifications.

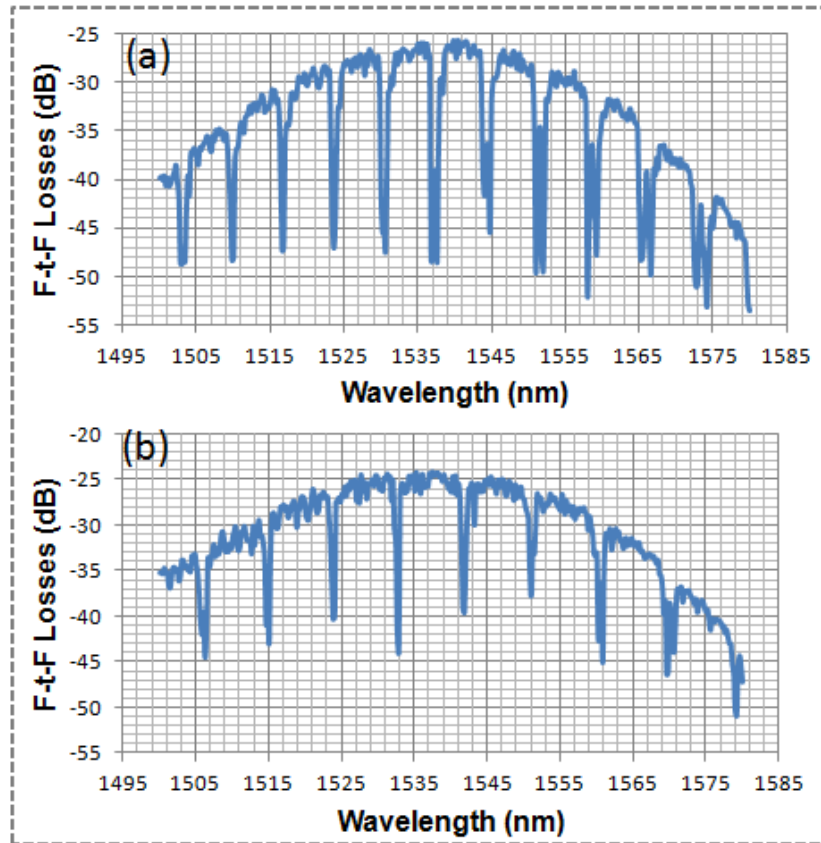


Figure 3.12. Preliminary experimental results derived from the non packaged (a) MUX1 and (b) MUX2 chips, respectively.

### ***3.5 Fabrication process of the 2x2 router's plasmonic part***

We describe here the fabrication process for the integration of plasmonic part. It consists first in processing the Gold structure using a lift-off UV lithography process and secondly the Cyclomer waveguides by deep UV lithography.

#### ***Development of Etched Recess (2.5D) Photomask for Plasmonic part integration into 2x2 router chips.***

The challenge in the integration of the plasmonics part into the PLATON router chips is that it comes in last position in the process and that structures have to be placed into a relatively deep (1 to 1.5 $\mu\text{m}$ ) cavity etched into BOX+SOG+Al, as shown in the Figure 3.13 below.

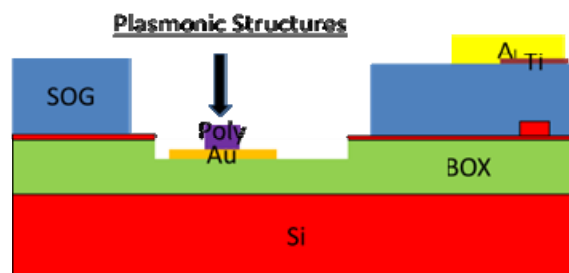


Figure 3.13: *Side view of PLATON router.*

To address this challenge, while keeping the previously developed cyclomer process based on Deep UV (250nm) lithography, we have introduced a novel type of mask, the recess etched photomask, or "2.5D photomask", whose topography is specially designed to match the chip's topography, as depicted in Figure 3.14. This is necessary to keep the intimate contact between the Cr mask and the resist absolutely needed to achieve the 500nm resolution required for the polymer waveguides. This 2.5D photomask technique was used only for the cyclomer step because the gold level requirements were not as strict as the polymer one. This novelty is currently the subject of an enquiry for patent application by UB.

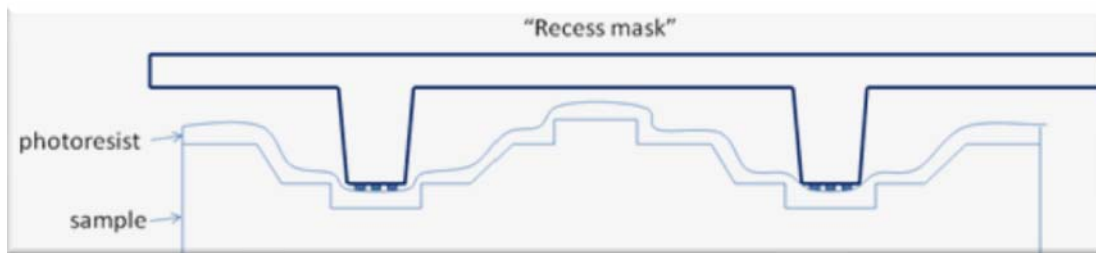
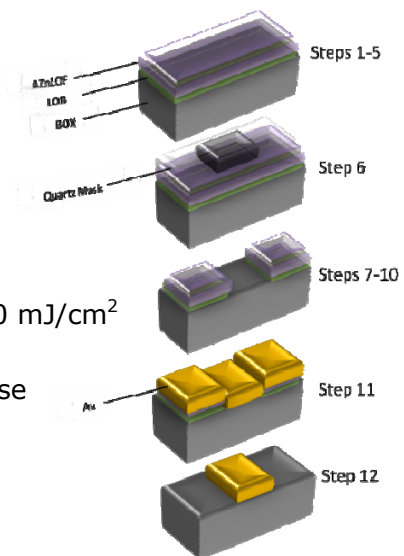


Figure 3.14: Side view of PLATON router.

### ***First step: Gold structure integration***

For the gold level fabrication a bi-layer photoresist lithography process is applied followed by thermal metal evaporation and subsequent lift-off. The lithography mask used was the standard one as it does not need to be a recess mask in that case. The main advantages of the bilayer lift-off process compared to single layer lift-off are a lower line edge roughness and sharper edges and a quick and efficient lift-off without any use of ultrasounds. A brief summary of this part of the process flow is described below and Figure 3.15 displays the resulting Au electrodes of the MZI switch.

1. Spin – coat LOR 07A:20A / 3:1 @3,000rpm for 40s
2. Soft bake @195° C for 3min
3. Spin – Coat AZnLOF 1:04 (AZ:EBR) @ 3,000 rpm for 40s
4. Soft bake @110° C for 3min
5. EBR 10 sec
6. UV 365nm exposure @vacuum mode; dose: 40-50 mJ/cm<sup>2</sup>
7. Post exposure bake @112° C for 4 min
8. Development with AZ826 MIF for 2min max, rinse with DI water
9. Flood exposure; dose: 370mJ
10. Hard bake @110° C for 3 min
11. Evaporate 5nm of Ti and 60nm of Au
12. Lift-off in NMP @ 90° C for 1h max



The following picture in Figure 3.13 displays the Au electrodes of the MZI switch:



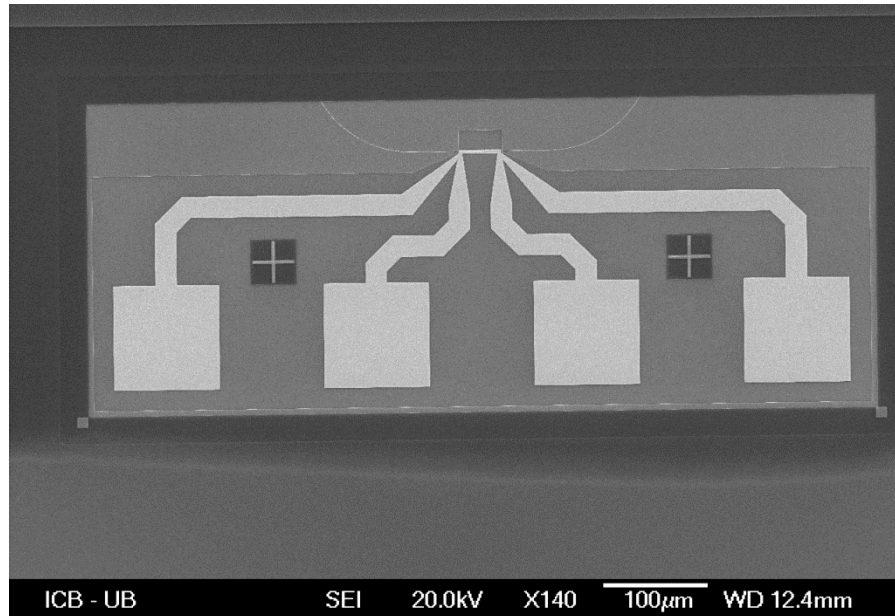
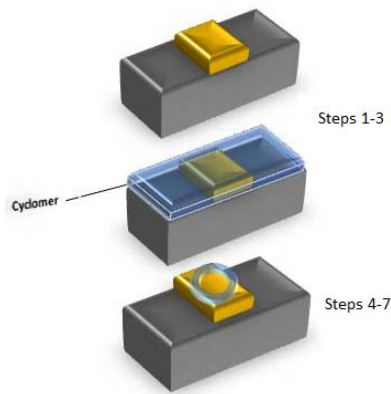


Figure 3.15: SEM micrograph of the MZI switch after the gold level fabrication.

### ***Second step: Cyclomer waveguide integration***

The specially designed recessed photomask described in the beginning of this section was applied during cyclomer UV exposure. The last step of the process flow is a hard bake at @60° for 5 min follows to ensure maximal thermal stability of the resin, as well as a precise TOC value of  $-2.1 \times 10^{-4}/^{\circ}\text{C}$ . The process flow is summarized below:

1. Spin – coat Cyclomer:EBR / 2:3 @1,600rpm for 40s => thickness of 600nm
2. Soft bake @110° C for 5min
3. Edge Bead Removal for 10 sec
4. UV 250nm exposure@vacuum mode; dose: 600-800 mJ/cm<sup>2</sup>
5. Development @ethyl lactate for 45sec max, rinse with IPA
6. Flood exposure; dose: 700mJ/cm<sup>2</sup>
7. Hard bake @60° for 5 min



The table presented below summarizes the structural characteristics of the 2x2 MZI routing structure according to their design and as found by characterization. AFM characterization was employed in order to define the vertical dimensions of the fabricated structures.

**Table 1:** Comparison between designed and actual MZI structural characteristics

Feature	Nominal	Actual	Variation %
Arms length ( $\mu\text{m}$ )	40 or 20	$40 \pm 0.4$ or $20 \pm 0.2$	$\approx 1$
Gold thickness (nm)	60	59-61	2
Cyclomer thickness (nm)	600	570-630	5
Cyclomer width (nm)	500	480-520	4
Asymmetric Part width (nm)	700	670-700	4

The variation between the nominal and the actual values is less than 5%. Concerning the alignment accuracy, all our results were better than the machine's specs of  $0.25\mu\text{m}$ . In conclusion, taking into account the difficulty of the processing and the risk introduced by the novel 2.5D mask processing, the plasmonics integration into the router chips must be considered as a major accomplishment within our facilities.

### ***3.6 RF characterization of the monolithic Si photodiodes***

Silicon-based integrated photonic devices rely on the transparency of bulk silicon at wavelengths longer than  $1.1\mu\text{m}$ . On the contrary, this transparency for photon energies

below the indirect electronic bandgap is a major drawback for conventional linear absorption based silicon photodetectors at telecommunication wavelength of 1.55  $\mu\text{m}$ .

As reported before an all-silicon concept as an alternative approach to Germanium photodetectors is targeted within the PLATON project. In this approach, the IR photogeneration in silicon is enhanced by linear absorption at midgap energy states introduced by silicon ion implantation. This approach is expected to significantly reduce the fabrication costs compared to hybrid detector concepts.  $\text{Si}^+$ -implanted photodetectors appear to provide the performance required within PLATON whilst keeping the overall integration complexity relatively low.

In our experiments we have followed the recently reported way of  $\text{Si}^+$ -ion implantation to generate defect states inside silicon [1]. This generation of midgap states leads to a drastic increase in linear absorption. Figure 3.16 shows the investigated rib-waveguide structure of the detector in a side and a top view. The active length of the investigated detector structure was  $L_{\text{PD}}=1.0$  mm and an ion implantation dose of  $1\text{e}13\text{cm}^2$  at an acceleration voltage of  $U=130\text{keV}$  has been used, masked with an implantation window defined by electron beam lithography centered to the silicon waveguide.

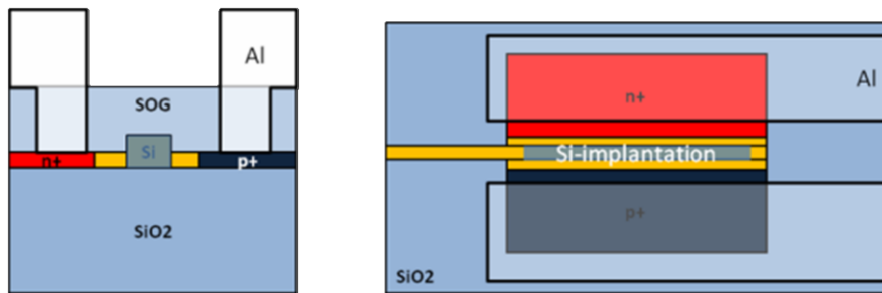


Figure 3.16: Schematic drawing of integrated Si-implanted photodiodes. (Left) cross sectional view, (right) top view.

Figure 3.17 summarizes the results of the static electro-optic characterization of the fabricated photodiode. Shown is the resulting photocurrent as a function of optical power inside the SOI waveguide at a reverse bias voltage of  $U=-5\text{V}$ . The photodiode shows a linear characteristic resulting in a sensitivity of  $S \approx 0.1\text{A/W}$ .

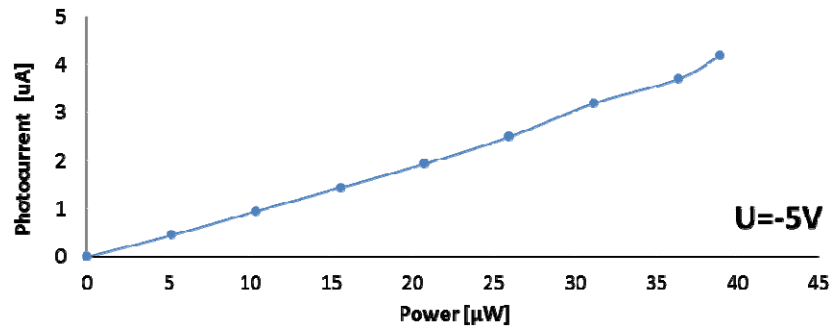


Figure 3.17: Results of the static characterization of silicon implanted photodiode. Shown is the resulting photocurrent as a function of optical power inside the SOI waveguide at a reverse bias voltage of  $U=-5\text{V}$ .

For the analysis of the dynamic behavior of the silicon implanted photodiode the measurement setup, which is schematically shown in Figure 3.18 has been used. The photodiode is analyzed by coupling a modulated optical signal at a wavelength around  $\lambda \approx 1550\text{nm}$  to the detector. The resulting electrical signal from the photodiode is transformed and amplified by a transimpedance amplifier (TIA) and detected by an oscilloscope. The silicon implanted photodiode is operated at a reverse bias voltage of  $U=-5\text{V}$ , which is applied to the device via a bias tee.

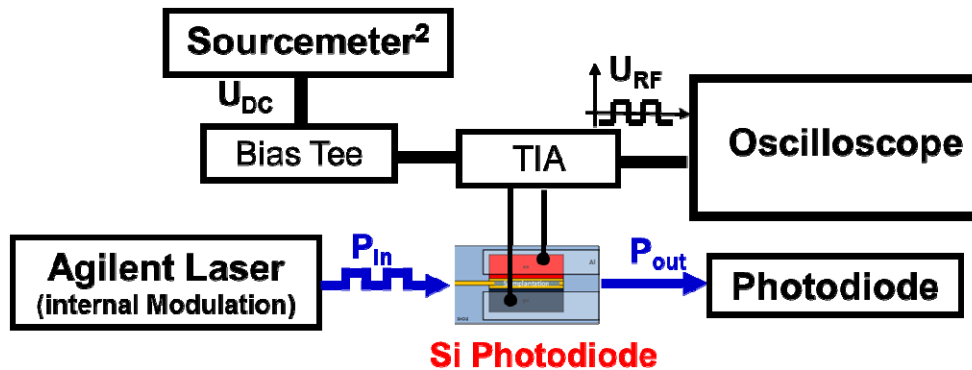


Figure 3.18: Measurement setup for the dynamic characterization of the silicon implanted photodiode.

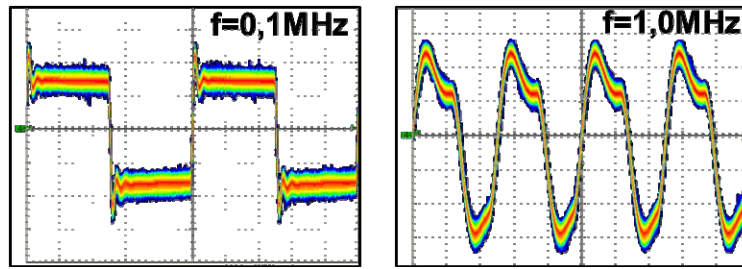


Figure 3.19: *Photodetector signals at  $f=0.1\text{MHz}$  and  $f=1.0\text{MHz}$  from silicon implanted photodiodes at a reverse bias of  $U=-5\text{V}$ .*

In Figure 3.19 the photodetector signals received at the oscilloscope for modulation frequencies of  $f=0.1\text{MHz}$  and  $f=1.0\text{MHz}$  are shown, where for the  $f=0.1\text{MHz}$  the square like modulation format can be clearly identified, while a more distorted signal is visible for  $f=1.0\text{MHz}$ . This distortion is due to the already distorted modulated optical signal from the laser source, which is operated at its maximum bandwidth of internal electrical modulation.

In summary the applicability of the all silicon photodiode approach for the goal of the PLATON project has been successfully demonstrated. A sensitivity of the analyzed photodiode of  $S=0.1\text{A/W}$  and the ability to detect modulated optical signals up to  $1\text{MHz}$  has been shown. As within PLATON, the role of the photodiode is to detect the header signal on the order of  $1\mu\text{s}$  the measured bandwidth of  $f=1\text{MHz}$  of the photodiode is sufficient for the targeted routing application.

### **3.7 Performance evaluation of the IC circuit**

The IC was fabricated by Austria Microsystems using a  $0.35\mu\text{m}$  CMOS process. The process features four metal layers for interconnects, two polysilicon layers for gate electrodes and interconnects, high resistivity polysilicon structures and output buffers with output voltage up to  $3.3\text{V}$  and current of  $12\text{mA}$ . After fabrication the ICs were delivered to IZM for assembly, packaging, testing and system integration.

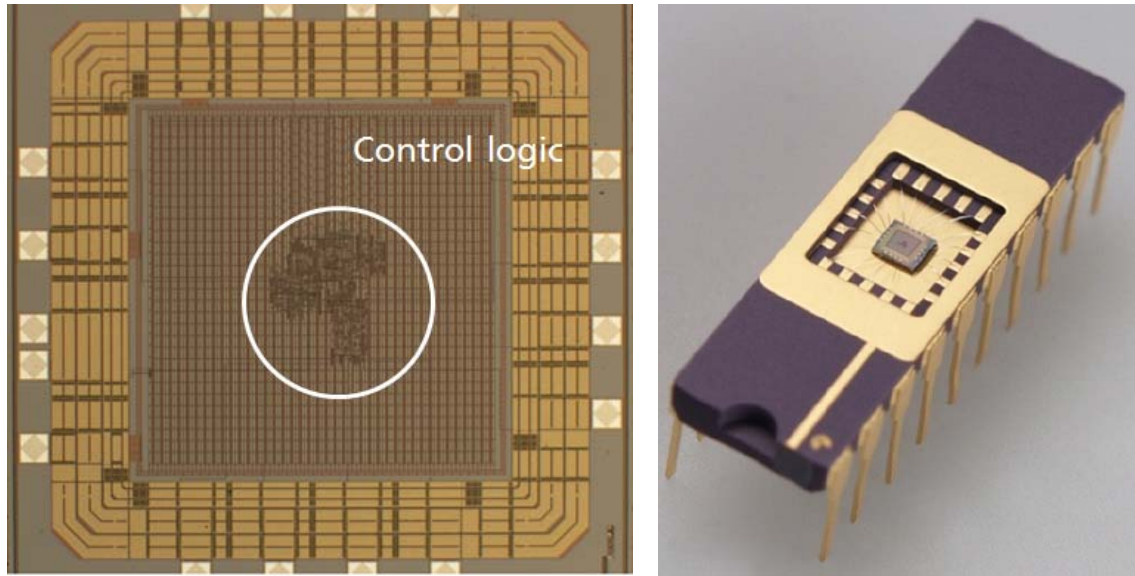


Figure 3.20: *Photography of control IC (Left), Packaged control IC for testing (Right).*

For testing the IC was mounted into a leadless ceramic chip carrier (CERDIP) package (Figure 3.20, left). The actual logic cells use only a small part in the center of the IC as there is a minimum die size.

The electrical interconnects were done using wire-bonds from the chip pads to the leads of the package (Figure 3.20, right). The electrical input signals were supplied by a FPGA board. For the verification of the digital logic the output signals were measured by the FPGA and visualized on a PC. The timing and the output levels were measured using an oscilloscope.

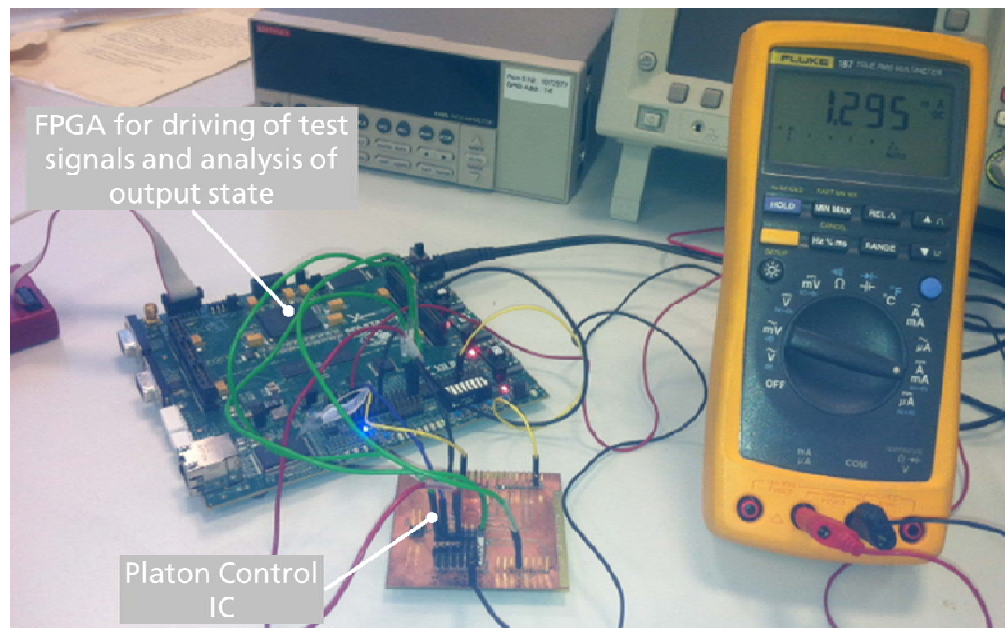


Figure 3.21: *Measurement setup for PLATON control ASIC.*

Figure 3.21 shows the measurement setup with the PCB for the PLATON-ASIC, the FPGA board and the measurement instruments. The generation of the input signals is controlled by a PC via the FPGA. In addition to the mentioned devices a power supply and a signal generator for the generation of the clock signal are required.

The results of the bit pattern measurements are shown in Figure 3.22. The plots show the output patterns (rows 4-11) for three different input bit patterns (rows 2 and 3). For all bit pattern it can be seen that the outputs change 1  $\mu\text{sec}$  after the inputs have changed.



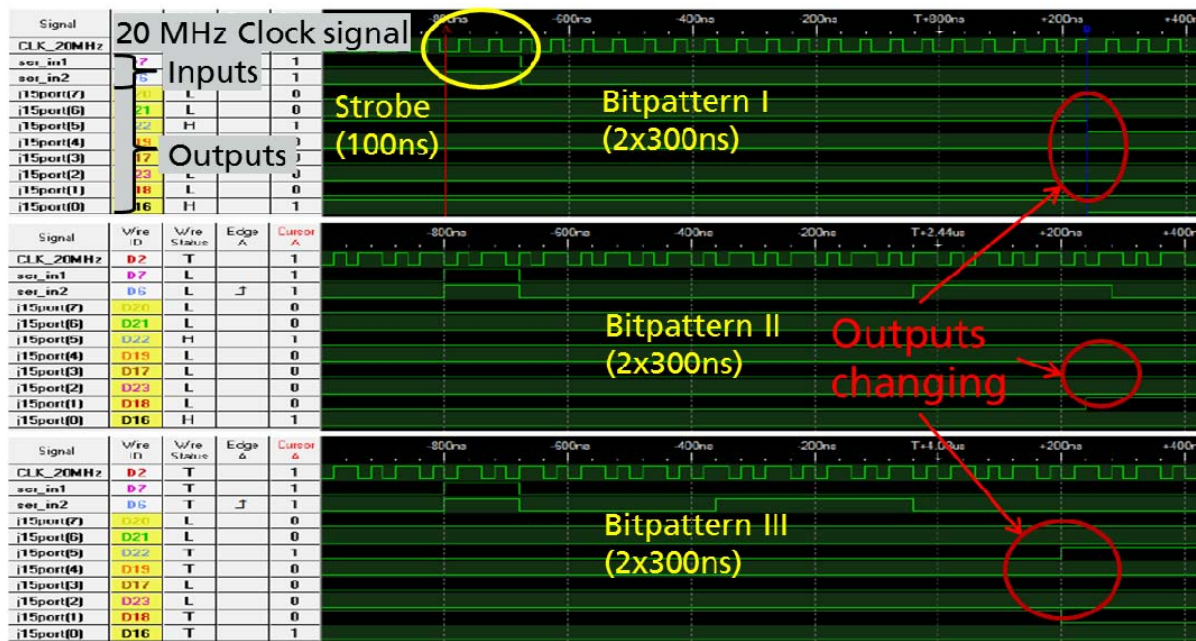


Figure 3.22: Bit-pattern measurements of PLATON ASIC.

Figure 3.23 shows current and voltage oscilloscope measurements at the output of the PLATON IC. In order to increase the output current two output buffers have been cascaded in parallel to drive a  $137\ \Omega$  load resistor. The plots show the transition from the low to the high state.

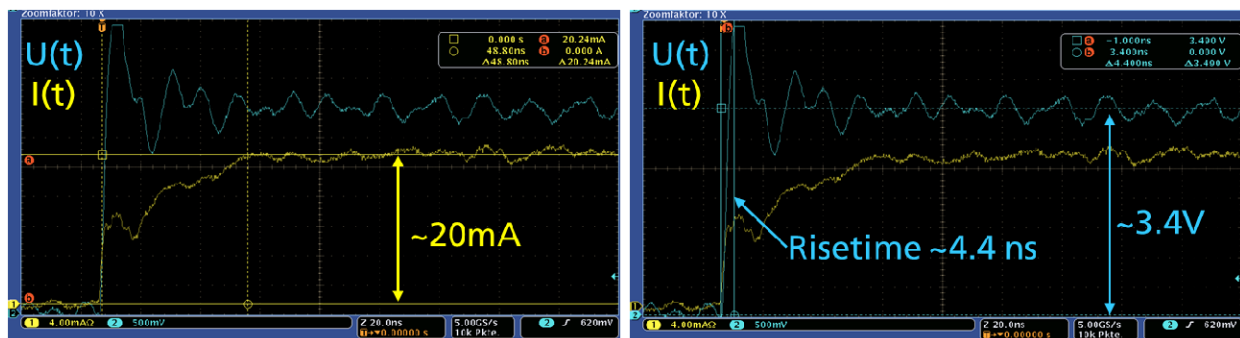


Figure 3.23: Oscilloscope measurements of PLATON's control IC output buffer characteristics.

The total output current of the buffers is approximately 20 mA, which is slightly lower than the predicted maximum of 24 mA ( $2 \times 12$  mA), while the voltage is about 3.4 V with a rise time of approximately 4.4 ns.

As it has not been specified yet the current required for achieving full switching with the cyclomer based plasmonic switches, an additional current amplifier has been developed and integrated in the circuit. The amplifier is based on a MOSFET transistor with the



output current controlled by a variable resistor at the drain. A schematic layout of the whole IC circuit that is going to be used for the PLATON router is depicted in Figure 3.24.

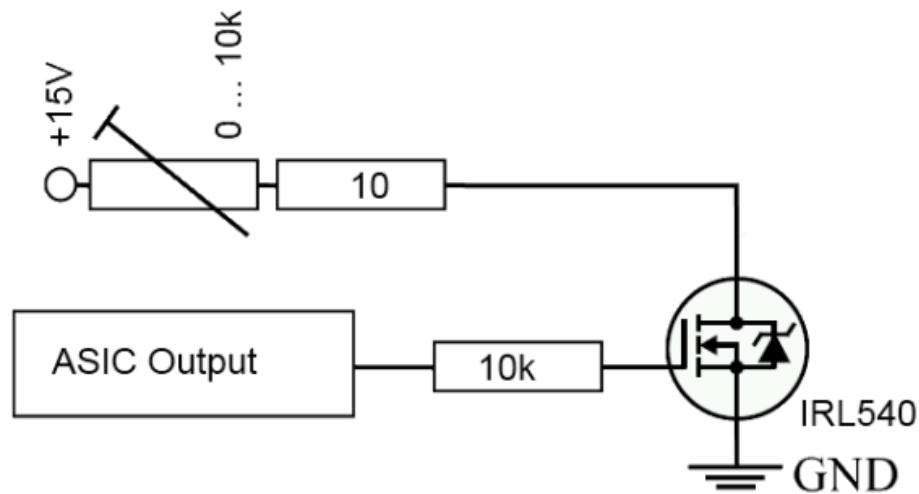


Figure 3.24: Electronics schematic of the current amplifier used to drive the PLATON plasmonic heating switch.

### 3.8 Performance evaluation of the RF lines for the interconnection of the IC with the plasmonic based switch and the PDs

The control signals from the photodiodes (PD) are fed into the control ASIC and after being processed drive the DLSP switch (Figure 3.25).

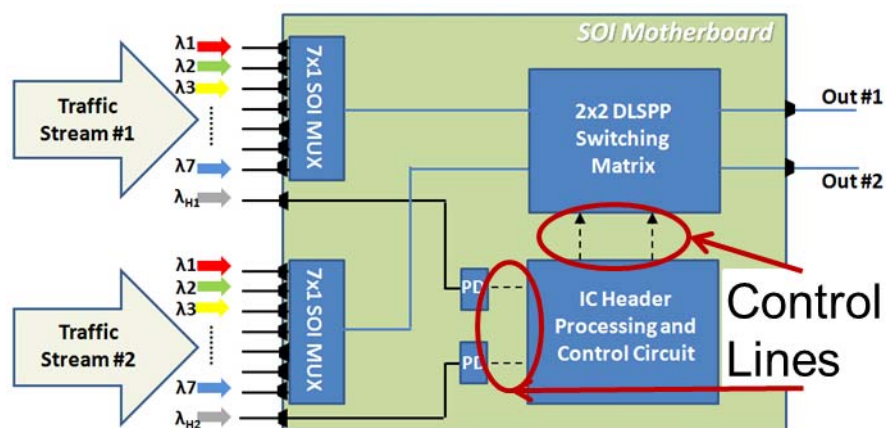


Figure 3.25: Schematic of signal flow in PLATON router.

The control IC generates digital signals with a clock frequency of 20 MHz and rise times in range of some ns. In order to assess the feasibility for high switching speeds, an analysis of high frequency signal transmission properties was done.

In order to characterize the electrical properties of the interconnects, test structures were fabricated and measured. Figure 3.26 shows a sample of the transmission line test structures. The transmission line is made up of a signal line which is surrounded by a reference metal structure.

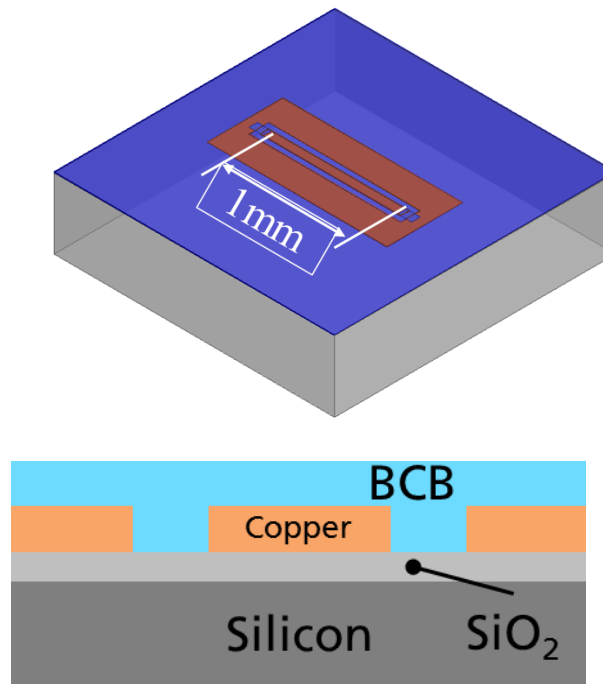


Figure 3.26: 3D view and cross section of test structure.

The structures were analyzed using 3D electromagnetic field simulations and compared to network analyzer measurements. Figure 3.27 shows a comparison of the measurement with simulations for different Si-conductivities. The simulations for 10 S/m show good correlation to the measurement. The extracted attenuation characteristics are shown in Figure 3.28. The trace shows a non-linear behavior frequency dependency in the region 1-10 GHz. However, as the IC will operate in the sub MHz range, this behavior is not expecting to distort the electrical signal that will pass through these lines. Actually, below the 300MHz range the frequency dependent losses are quite flat in the order of 2.5dB/cm and thus there is no need for pre-emphasis.

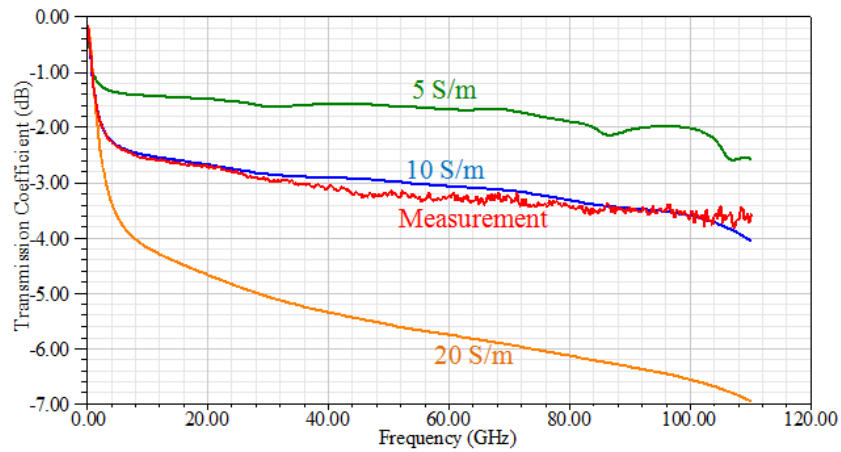


Figure 3.27: Comparison of simulation and measurements of transmission lines on Si/SiO<sub>2</sub> substrate with different spec. conductivities.

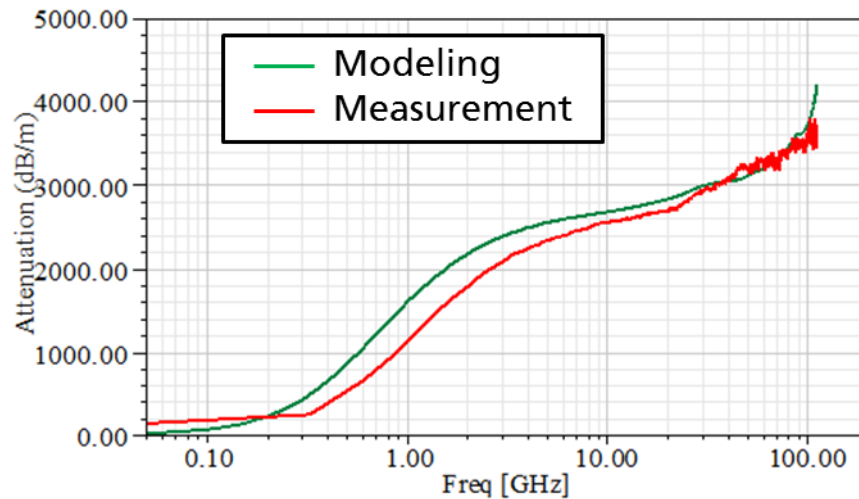


Figure 3.28: Extracted attenuation from simulation and measurement.

## 4 Conclusions

This deliverable presents an overview of the complete process flow that has been developed and finalized towards the integration of the silicon, plasmonic and electronic sub-systems in the same routing platform, allowing for the first time their seamless interoperability. The process flow of the Si and the plasmonic parts of the router is described in detail with first experimental results indicating great quality for the Si waveguides. The first chips produced by this method have demonstrated lower losses in the order of 20dB compared to the first generation of chips produces two years ago. These chips allowed also due to their low loss, to conduct for the first time a preliminary characterization of the two SOI-MUXs placed at the frontend of the PLATON router with very encouraging results. Full characterization of the SOI-MUX was not feasible due to the non packaged form of the chip that prohibited access to the 32 ring resonators and 7 thermally tunable straight sections forming each MUX. Moreover, results from the fabricated monolithic silicon photodiodes are presented. Their performance evaluation verified that their performance is within the specifications set in D2.4.

Furthermore, the performance evaluation of the IC circuit that is going to be used in the PLATON router for packet routing decision making and control signal generation has been reported. The speed of the IC is well beyond the specification, but the output current might be probably low. For safety reasons, since there is not yet an experimental characterization of the Cyclomer based plasmonic switch that would reveal the required driving current, an additional MOSFET transistor is placed at the output of the IC circuit for amplifying the current. The amplitude of the output current is controlled by a variable resistor at the drain. Finally, the performance of the RF lines on the Si substrate is presented. In the sub MHz range, where the electrical signals of the router will operate, the propagation losses are quite low and frequency independent revealing that there is no need for pre-emphasis of the signals.

## References

[1] M. W. Geis, S. J. Spector, M. E. Grein, J. U. Yoon, D. M. Lennon, and T. M. Lyszczarz, "Silicon waveguide infrared photodiodes with >35 GHz bandwidth and phototransistors with 50 A/W response," *Optics Express* 17 (2009) 5193-5204.