ICT - Information and Communication Technologies

Merging Plasmonics and Silicon Photonics Technology towards Tb/s routing in optical interconnects

Collaborative Project

Grant Agreement Number 249135

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1 Executive Summary

This document provides detail for the packaging and fiber-pigtailing of the 2x2 optical interconnect router based on the PLA19 chips, where the design of silicon photonic components, SOI motherboard and microcontroller IC based preliminary specifications of PLATON's 2x2 and 4x4 routing platforms both at component- and at system-level had been provided in the deliverable D2.1.

To this end, it includes the specifications for all specific PLATON router sub-blocks, like:

- Silicon-on-Insulator (SOI) platform
- Waveguides (Silicon waveguides and Dielectric Loaded – Surface Plasmon Polariton (DLSPP) waveguides)
- Interfaces (fiber-to-Silicon, Silicon-to-DLSPP, electrical)
- Silicon-on-Insulator Multiplexing (MUX) circuit
- IC electronic control circuitry
- 2x2 Dielectric Loaded – Surface Plasmon Polariton (DLSPP) switching element

2 Introduction

2.1 Purpose of this document

The objective of this deliverable is to provide design and details of packaging and fiber-pigtailing of the 2x2 PLA19 optical interconnect router. The 2x2 PLATON optical interconnect router is based on the PLA19 chips and rely on silicon photonic components, SOI motherboard and microcontroller IC based preliminary specifications of PLATON's 2x2 routing platforms both at component- and at system-level (D2.1).

2.2 Document structure

The present deliverable is split into six major chapters:

- Overview of PLATON 2x2 routing concept
- Components ad specifications of the 2x2 routing concept
- Interfaces of 2x2 routing platform
- Packaging concept
- Driver circuit
- Details of the 2x2router package
-

2.3 Audience

This document is public.

3 Overview of PLATON 2x2 router concept

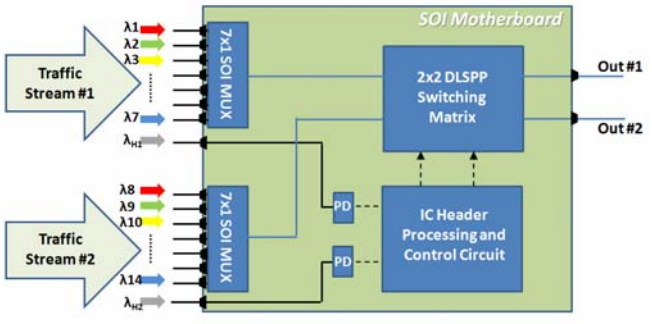

Figure 3-1*: PLATON's 2x2 router* ***block diagram***

Figure 3-1 shows the block diagram of the PLATON 2x2. Routing platform operates with optical data line-rates of 40Gb/s and reside on a Silicon-on-Insulator Motherboard that hosts all the heterogeneous technologies, namely SOI-based components, Dielectric Loaded Surface Plasmon Polariton (DLSPP) switches, Photodiodes and Integrated Circuit Microcontrollers. The 2x2 router offers an aggregate switching throughput of 560 Gb/s. Briefly the role of each router sub-unit is as follows:

1. 7x1 SOI MUX (Multiplexer): This subsystem is used to multiplex the 7 incoming 40Gb/s data traffic carrying wavelengths into a common, single optical traffic stream that is considered to follow the same route throughout the network. Two 7x1 SOI multiplexers will be employed in the 2x2 PLATON. The SOI MUX will rely on silicon-based photonic integration technologies.

2. PD O/E Conversion Stage: Photodiodes integrated on the SOI motherboard will form the O/E conversion stage of the routing platform. PDs will be used for converting the optical header information into respective electrical header pulses to be subsequently processed by the IC Header Processing and Control Circuit. One PD will be employed for every header wavelength, which in turn implies that in the case of the 2x2 router a total number of 2 PDs will be used.

3. IC Header Processing and Control Circuit: This subsystem is used for processing the incoming header information and generating the proper electrical control signals to drive the DLSPP switching matrix. For the 2x2 router, the IC circuit will have two input ports for receiving the respective electrical header pulse streams and will provide two electrical output signals for controlling the state of the 2x2 switching matrix.

4. DLSPP switching matrix: The DLSPP switching matrix routes the incoming traffic streams towards the different outputs depending on the header information. PLATON's switching matrix will comprise Dielectric Loaded Surface Plasmon Polariton (DLSPP)-based thermo-optic switching elements. A 2x2 switching matrix will be used for the 2x2 routing platform.

A schematic representation of these building blocks and their positioning on the SOI motherboard is provided in Figure 3-2.

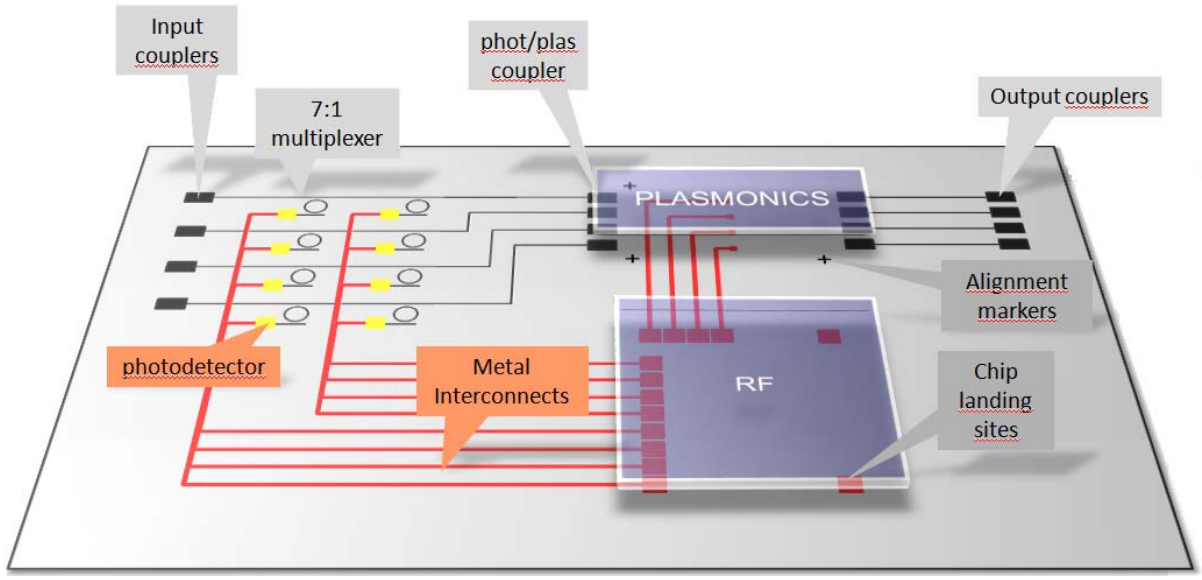

Figure 3-2*: PLATON's SOI motherboard and its various building blocks*

4 PLATON 2x2 router component specifications

4.1 Silicon-on-Insulator Multiplexing (MUX) circuit

MUX circuitry will rely on an interconnected arrangement of 7 microring-based SOI structures. Seven respective heating structures relying on electrical current driving circuitry will be employed for enabling fine-tuning of the MUX resonating frequencies so as to optimally align them to the incoming data wavelengths.

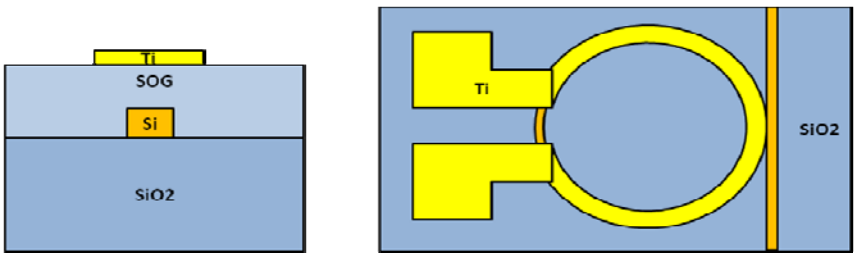

Figure 4-1*: a) Cross-sectional and b) Top view of the integrated micro-heaters*

An overview of the targeted specifications is provided below:

Table 1: 7x1 SOI MUX specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
No# of Input ports			7		
No# of Output ports			1		
SiWire Width	W		400		nm
SiWire Height	H		340		nm
Si waveguide Top-Cladding			SOG		

			Accuglass T512B		
Material for electrical contacts			Titanium		
Thickness of electrical contacts	W_{Ti}		100		nm
Operating Wavelength Range		1500		1600	nm
Center Wavelength			TBD		nm
Channel spacing	Δf		100		GHz
Channel 3-dB bandwidth	$\Delta\lambda$		0.32		nm
Footprint / Chip size (w)x(L) (without the electrical contacts)			20x250		μm^2
Footprint / Chip size (w)x(L) (including electrical contacts)			40x250		μm^2
Power loss per channel	α		0.5	1	dB
Channel Crosstalk		-25	-20	-18	dB
Power consumption per temperature deviation			1		mW/K
Maximum Heating power per heating element		10		100	mW

The optical characteristics of the ring resonators and the switching matrix will be controlled by the control IC circuit using heating resistors. The heating resistors will be realized by applying thin resistive layers to the devices that can be heated using an electrical current. The Heating resistors will optionally be driven by buffer amplifiers. In order to change the temperature the control IC generates a square-wave signal. The temperature can be controlled by changing the duty-cycle as well as the frequency.

4.2 Header detection / photodiode

Two alternative photodiode solutions will be investigated:

- Monolithically integrated Ge photodiodes using two different integration techniques, namely butt coupling and evanescent coupling. These configurations are expected to provide outstanding performance values well beyond the requirements of PLATON's routing platforms, coming, however, at the expense of increased fabrication complexity.
- Si+-implanted photodetectors, that seem to be the most appropriate compromise for matching the requirements of PLATON whilst keeping the overall integration complexity relatively low. In that type of photodetectors, generation of charge carriers relies on linear absorption at incorporated defect states which constitute inter-band energy levels caused by silicon ion implantation.

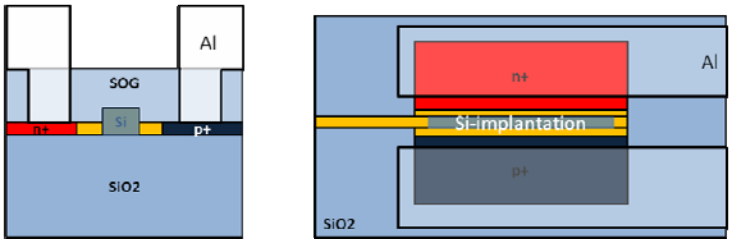

Figure 4-2: *a) Cross-sectional and b) Top view of the Si+-implanted photodetectors*

The targeted specifications for the photodetector option used in the final 2x2 and 4x4 router platforms are summarized in the following table:

Table 2: Header O/E Conversion: Photodiode specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Footprint			0.1		mm²
Photodiode Reverse Voltage	V_{PD}		3		V
Maximum average optical input power (NRZ signal)	P_{opt}		TBD		
Maximum output peak voltage	V_{PEAK}		TBD		
Operating Wavelength Range	λ	1500		1600	nm
DC Responsivity @1550nm	R		0.2		A/W
Polarization Dependent Loss	PDL		TBD		
3-dB cut-off frequency	f_{3dB}		1		GHz
Photodiode Dark Current	I_{dark}			100	nA

4.3 IC electronic control circuitry

The digital control IC has to evaluate the header information and control the output DLSPP switches according to the a pre-defined routing look-up table.

The block diagram of the digital control IC for the case of the 2x2 routing platform is illustrated in Figure 4-3. A similar design will be used also for the 4x4 PLATON router employing however a total number of 4 input and 8 output ports. The control IC will be a synchronous design. The clock signal will be generated by an internal oscillator.

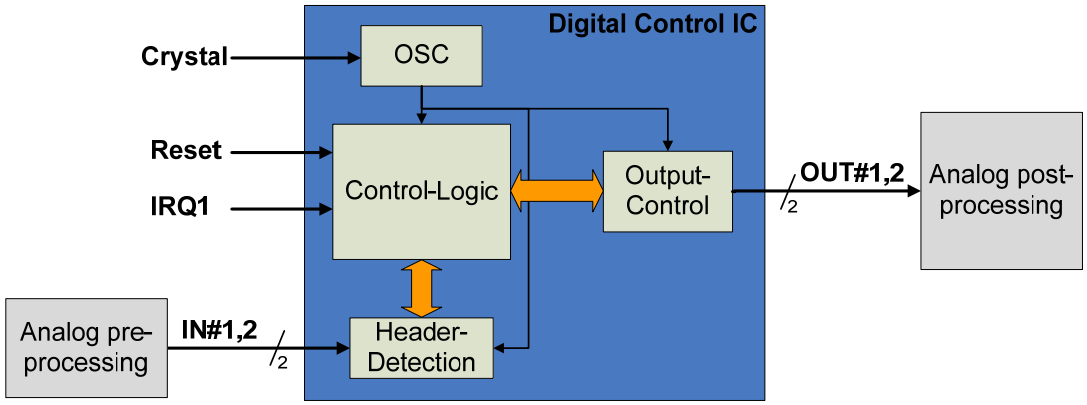

Figure 4-3: Block diagram of the control IC

A summary of the IC microcontroller specifications is provided below:

Table 3: Specifications of digital control IC

Parameter	Description/Value
Technology	Austriamicrosystems C35B4C3
Clock Speed	up to 20 MHz
Input/Output - Options	3.3V (supply voltage - VDD) digital CMOS signals
	0.7 VDD input high level
	0.7 VDD input low level
	2 inputs/2 outputs for 2x2 router
	4 inputs/8 outputs for 4x4 router
	Bidirectional CMOS buffers up to 24mA
	Bidirectional Schmit-Trigger buffers up to 24mA
	Bidirectional TTL buffers up to 24mA
	Tri-State output buffers up to 24mA
Footprint/Dimensions	4x4 mm^2
Latency	TBD
Assembly	Wire bonding / Flip-chip

It has to be evaluated, whether the DLSPP switching elements will be able to be controlled directly by the digital CMOS output signals that offer a driving strength up to 24mA. In case this does not prove sufficient for the purposes of thermo-optic switching by means of the DLSPP switch modules, a separate external driving stage will be implemented.

4.4 Metal Interconnects

The metal interconnects will provide signal and power distribution between the components. The interconnects will be designed impedance controlled so as to maximize the power delivered to the modulators and control the timing of the header signaling for the IC Microcontroller. In order to reduce the number of required metallization levels single metallization layer configurations will be employed. Initial designs for different TML configurations (Coplanar Waveguide, Coplanar Strips) and substrate build-ups (metal layer on BOX, metal layer on redistribution layer RDL) have been done based on numerical simulations. The electrical characteristics are compiled in Table 4. The designs take into account the different geometrical features of the processes.

Table 4: Specifications for PLATON's electrical interconnects

Parameter	Symbol	TML on BOX	TML on RDL	Unit
CPW width of center conductor	Wcpw	15	100	um
CPW gap signal to ground	Gcpw	1	5	um
CPS width of signal conductors	Wcps	15	45	um
CPS gap between signal lines	Gcps	5	10	um

The metal interconnects will be deployed using:

- Alu metallization with thickness ranging between 300-1000 nm (~ $3x10^{-6}$ Ohmcm)

- top-cladding with thickness between 100-1500 nm
- Via etching down to the silicon layer
- Via etching down to the heater layer

For chip scale fabrication, photolithography with ~5 μm alignment accuracy and ~ 5 μm minimum feature size will be used.

4.5 2x2 Dielectric Loaded – Surface Plasmon Polariton (DLSPP) switching element

Preliminary simulation-based results have identified two alternative DLSPP switch architectures as the most promising designs for the 2x2 switching matrix: the Mach-Zehnder Interferometric (MZI) layout and the Waveguide Ring Resonator (WRR) setup. The specifications for both of them operating as a 2x2 switching matrix are summarized in Table 5:

Table 5: 2x2 DLSPP Switching Matrix Specifications

Parameter	Symbol	MZI	WRR	Unit
No. of ports (input x output)		4 (2/2)	4 (2/2)	
No. of switching elements		1	1	
Waveguide Type		DLSPP-W	DLSPP-W	
Operating Wavelength Region	λ	1500-1600	1500-1600	nm
Free Spectral Range	FSR	>100	50	nm
Channel Bandwidth	$\Delta\lambda_{3dB}$	>60	>4	nm
Crossection (waveguide mode) dimensions		0.5x0.6	0.5x0.6	μm^2
Footprint / Chip size (w)x(L)		15x40	15x15	μm^2
Total power consumption	P_{elec}	8	8	mW
Optical Power Losses (input/output)	α	5	<8	dB
Latency	$t_{latency}$	220	<100	fsec
switching time	Δt_{speed}	1	1	μsec
Optical Crosstalk	ER	<-20	-10	dB

5 PLATON 2x2 router interfaces

The optical layout of PLATON 2x2 router silicon integration platform is depicted in the Figure 5-1.

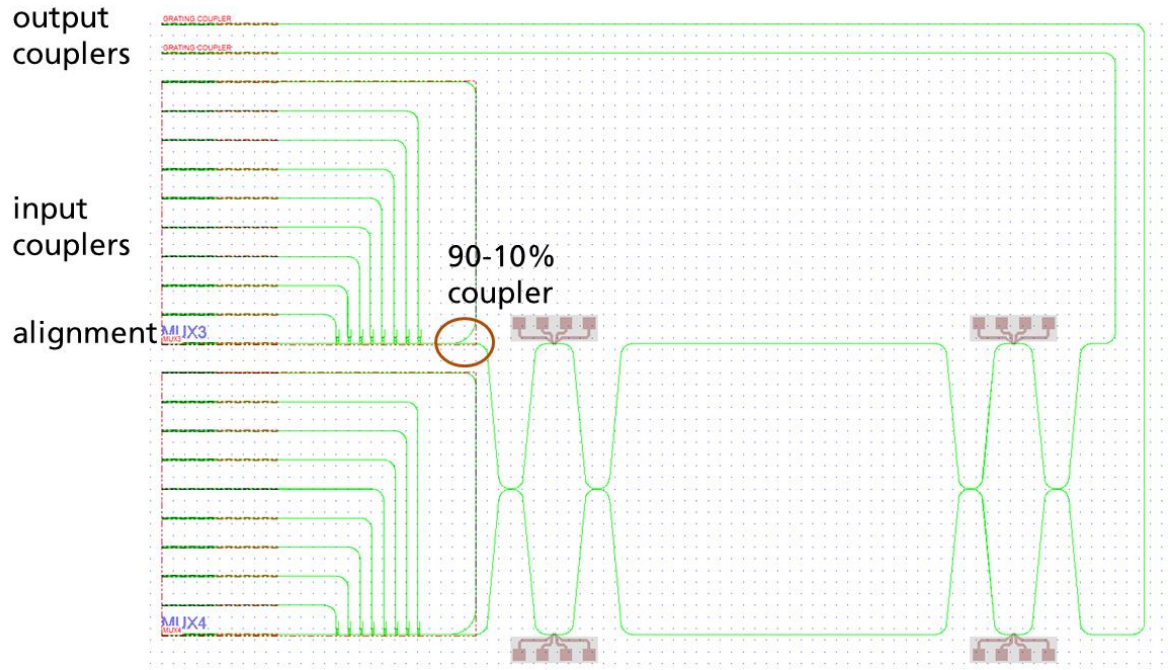

Figure 5-1: Optical layout of PLATON 2x2 router

The 2x2 router consists of 2 1x8 MUX blocks and a cascaded 2MZIs for 2x2 switching function. Each MUX block has 10 optical I/Os to be used for multi-fiber alignment and also MUX inputs. The enable the alignment the trough port MUX have been chosen and the output of the MUX has been tabbed using 10:90 coupler to be coupled back the alignment out port. Further 2 additional ports have been considered to couple out the 2x2 switching matrix output signals. Considering all these optical I/Os, the 2x2 router has 22 optical ports to be coupled to the outside of the router, which is possible using only multi-fiber arrayed structures.

The grating coupler to be used in the optical I/Os had been discussed in detail in D2.2 based on their tolerances and TM coupling performances.

Beyond the optical interfaces the 2x2 router consists of several DC electrical I/Os in order to bias the double ring resonator structures of the 1x8 MUX and also the biasing pins for the DLSPP based MZI switches in the 2x2 switching matrix. Further in order to trim the phase between the multiplexed signals the 1x8 MUX consists of phase sections to be tuned. In the figure 5.2 also the electrical signal paths are included, the figure shows entire layout of the 2x2 PLATON routers with its MUX and 2x2 switching matrix.

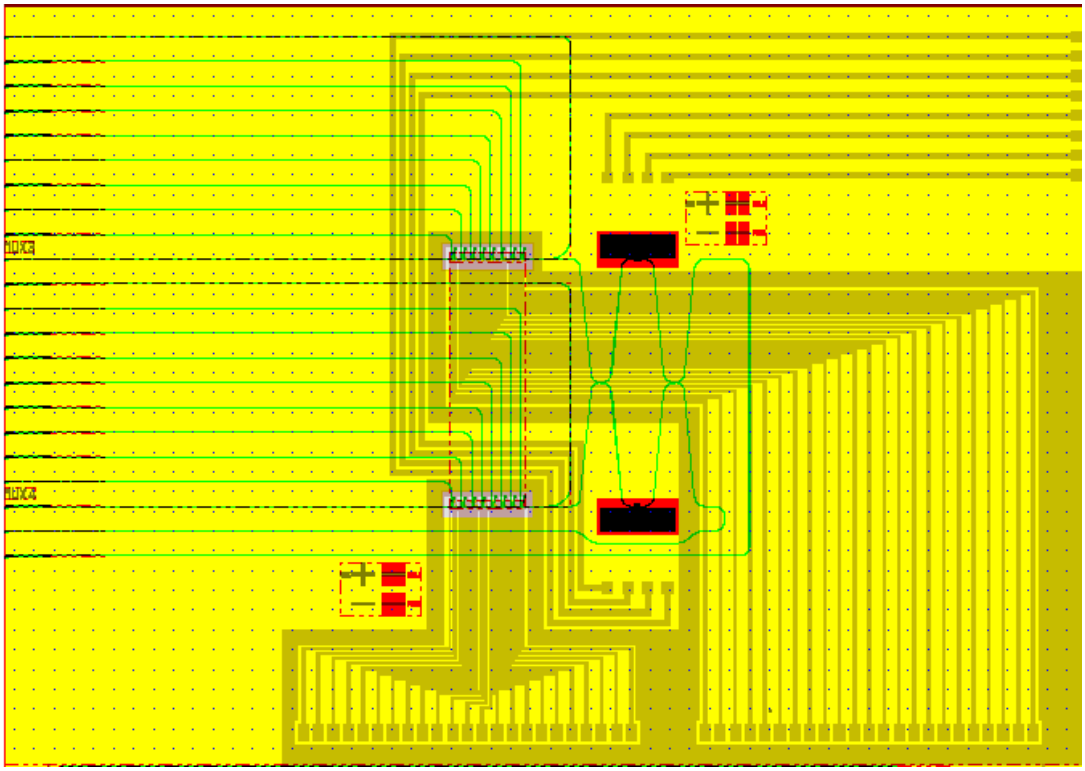

Figure 5-2: GDS layout of the 2x2 PLATON router

A closer view of the double ring resonator based MUX and DLSPP based MZI switching element is depicted in Figure 5-3, including also the side views of the MUX and switching elements.

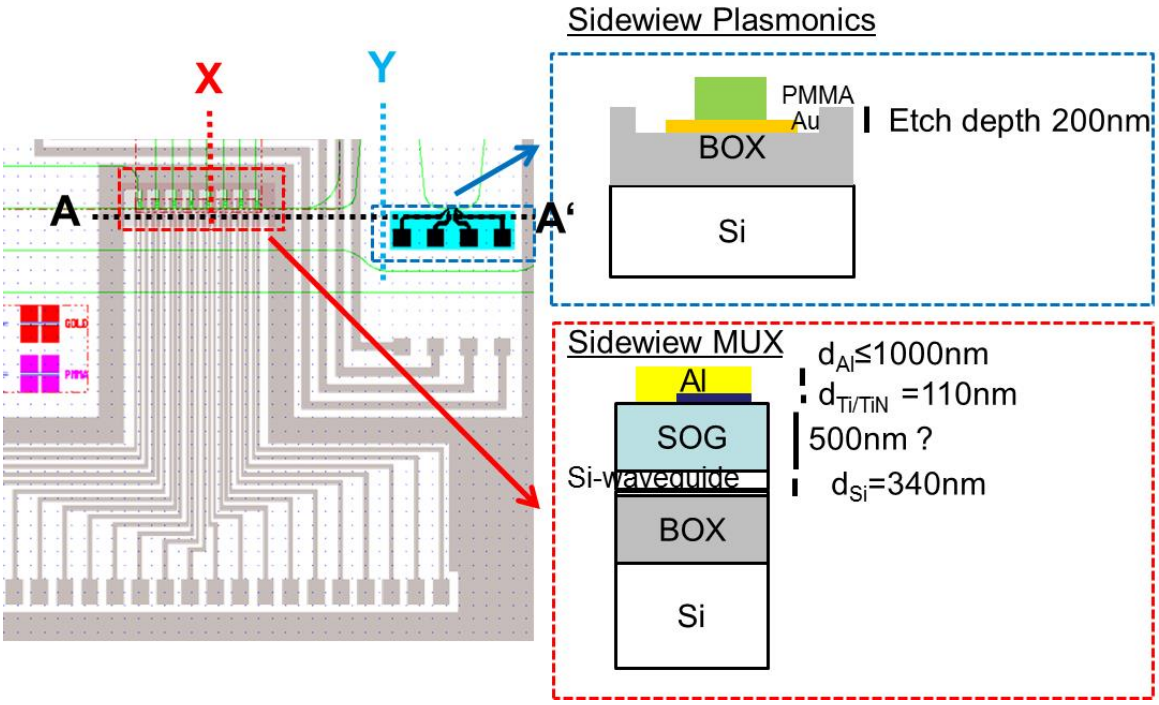

Figure 5-3: Side views of the MUX and switching elements

Here the main challenge is to bring the required contacts over the entire chip to the borders of the entire 2x2 router in order to contact them using wire bonding schemes to the periphery of the router. That enables to control each of the required component separately the double ring resonators and DLSPP based switching elements (Figure 5-4). Here the Au metallization layers for the DLSPP elements and used Al signal layer metallization are providing the process incompatibility which has to solve.

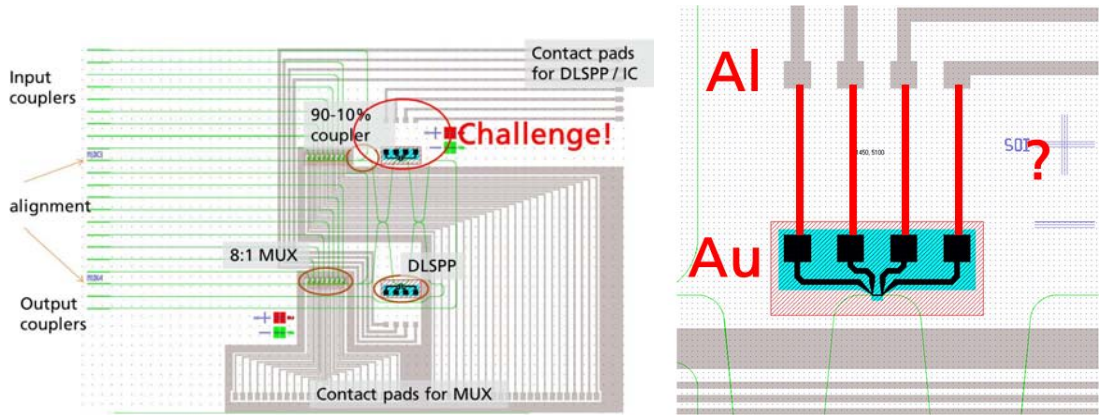

Figure 5-4: Challenge of heteronomous integration, compatibility issues related to AU and Al

Due to the process complexity a straight forward solution of separately processing the Al signal paths on silicon integration platform has been chosen and then further interfacing the DLSPP switching elements using wire bonding scheme as depicted in the Figure 5-5.

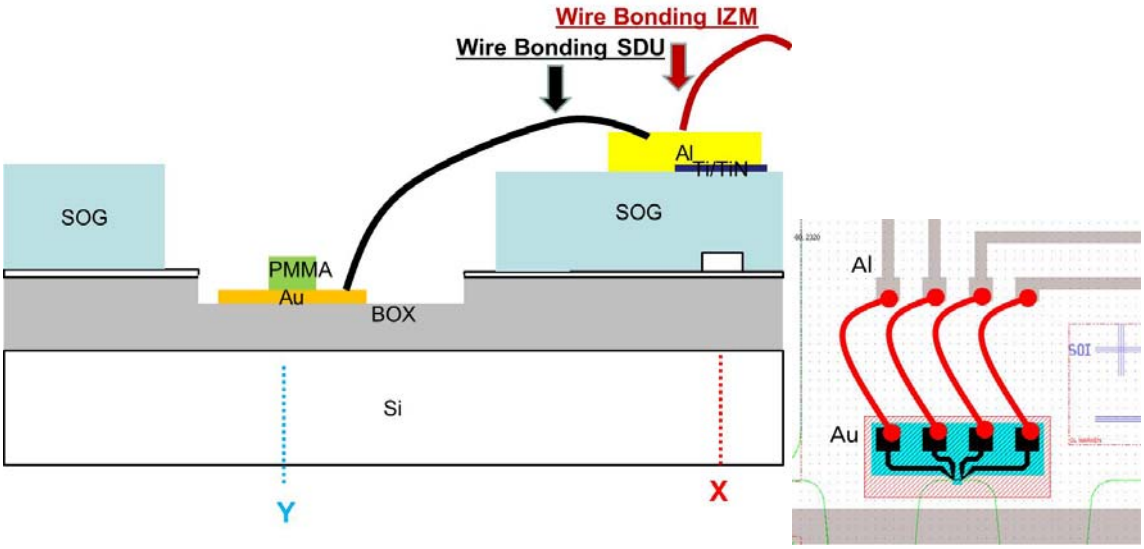

Figure 5-5: Wire bonding approach to overcome the challange

Figure 5-5 indicates also the process flow to be considered in order to get the DLSPP switching elements to be contacted: after finalizing the silicon photonics integration platform processing with the required cavity for the DLSPP elements the plasmonics components to be fabricated to be contacted to the Al contact pads which have been

already processed within the silicon platform. Using those required signal paths to be contacted the periphery.

Further a complex process flow and advanced integration concept has been developed to be considered heterogeneous integration of all PLATON components in a 3D integration scheme taking care on the interfaces using planar signal distribution layers. This concept is depicted in the Figure 5-6

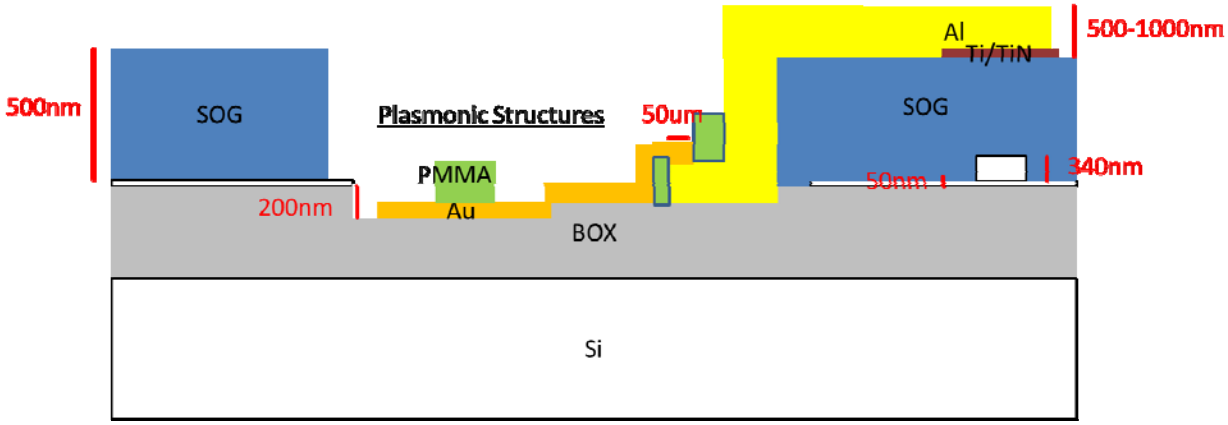

Figure 5-6 Bridging approach providing a heterogeneous integrated solution

Due to the complex process and logistic involved the implementation of this concept has been not considered in the PLATON runs.

Further interfaces to be considered are related to the functionality of PLATON 2x2 router the ASIC and photodiode integration on the router platform. All have been considered in the Figure 5-7.

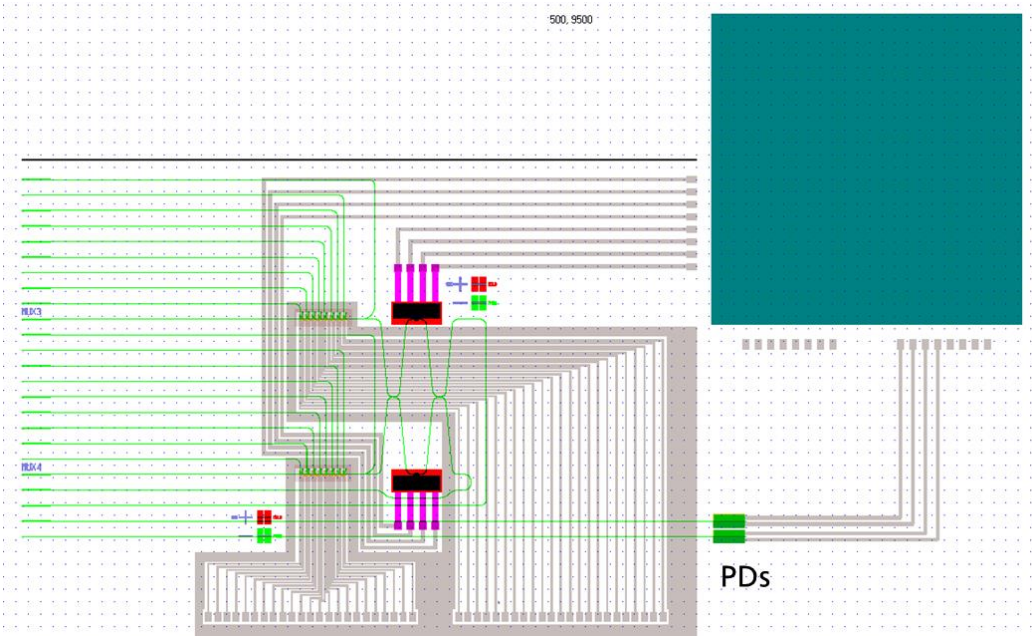

Figure 5-7: PLATON 2x2 silicon photonics and ASIC integration layout

The layout includes the 2 1x8 MUX blocks 2x2 switching matrix and also photo diodes for header recognition and ASIC to logic control of the switching matrix based on the lockup tables.

6 PLATON 2x2 router packaging concept

The principle of PLATON 2x2 router packaging concept developed is shown in Figure 6-1, consider its components to be connected to the periphery.

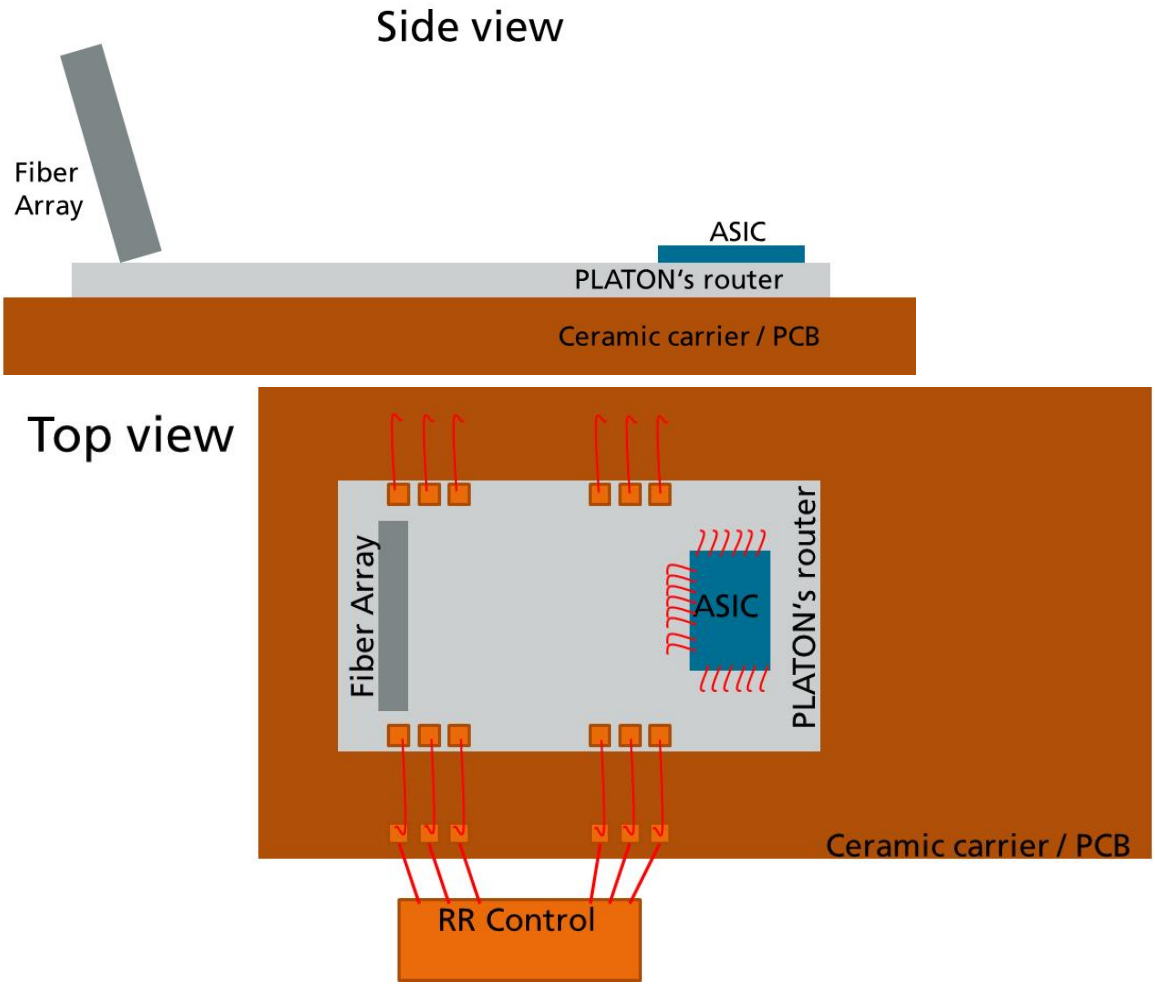

Figure 6-1: Principle of PLATON 2x2 router package

This principle allows PLATON 2x2 router components effectively be assembled. After considering the dimensions of the entire building blocks a more detailed schematic has been designed in order to select the sufficient packaging platform of the 2x2 router as in Figure 6-2.

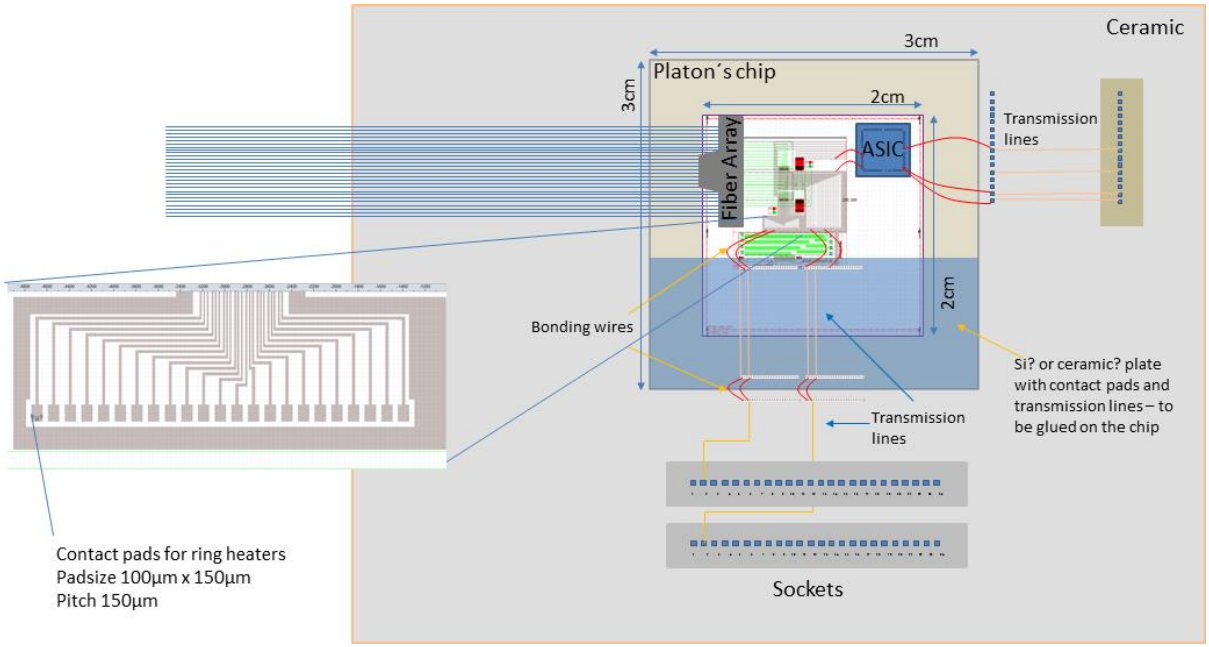

Figure 6-2: Detailed plan of PLATON 2x2 router package integration

Figure 6-2 shows the 2cmx2cm PLATON 2x2 router chip with corresponding ASIC chip to be integrated on the silicon photonics platform hybrid and to interfaced optically and electrically. Although the dimensions of the silicon photonics 2x2 router chip are small since a dense integration is possible due to the silicon photonics nanowire concepts, the interfaces to the periphery defines the dimensions of the package. Here standard multi fiber arrays and standard electrical pin arrays to be implemented to the router, which are defined in sub millimeters and millimeters.

Due to the wire bonding considerations and boundaries the landing pads for wire bonds have been selected to be pad sizes dimensioned 100µmx100µm with a pitch of 50µm.

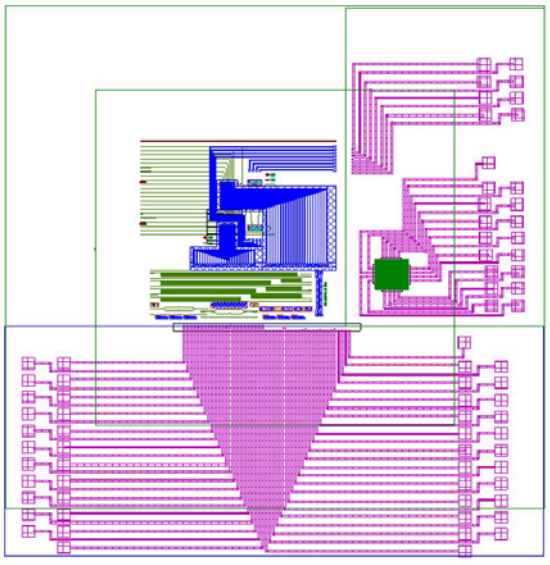

Figure 6-3: Dimensioned plan of PLATON 2x2 router package integration

A more detail layout of the integration platform is shown in in Figure 6-3, with real dimensions considered for the 2x2 router chip, ASIC and corresponding wiring. A ceramic based platform have been chosen in order to provide the required mechanical and thermal stability and easy structure material.

The corresponding housing is depicted in the Figure 6-4. Here Gleanair compact connectors have been used to provide the required 75 connections. Further temperature stabilization will be provided by using AD590 and Peltier based cooling component.

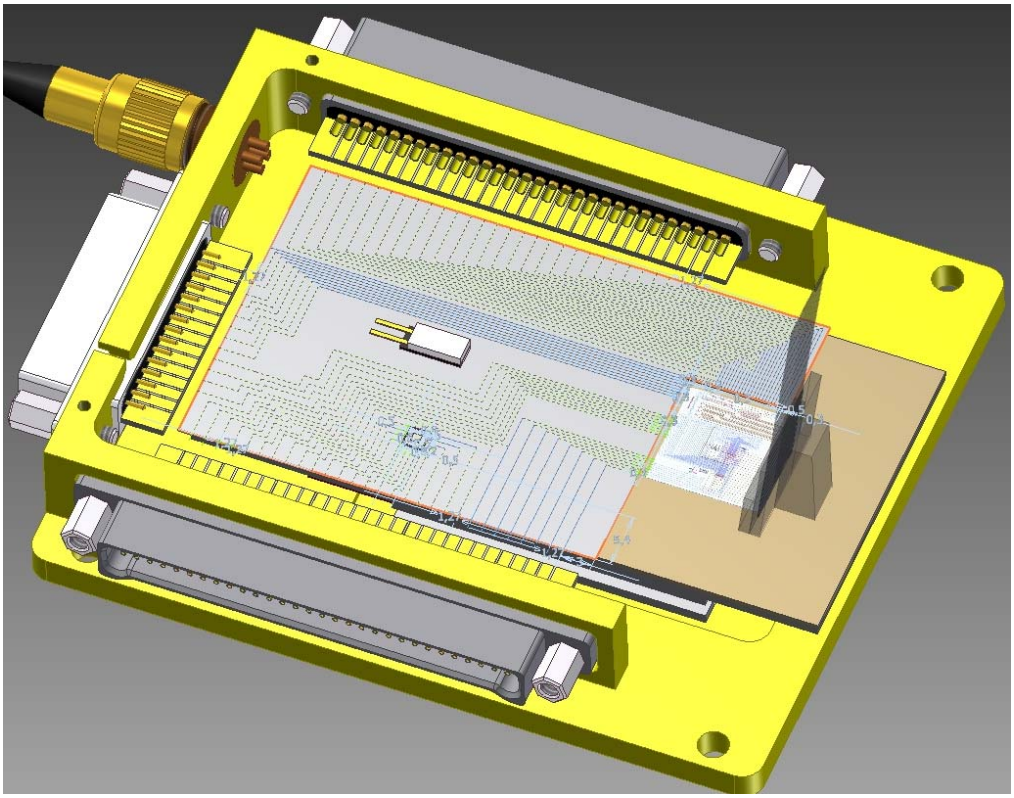

Figure 6-4: PLATON 2x2 router package

7 Driver circuit

Due to the required signal level of the DSPP based switches and standard MPW based control ASIC output signal level an additional amplification of signal is needed. For this purpose an external driver circuit have been design and reported earlier. This driver circuit has been tested using discrete packaged ASIC as shown in the Figure 7-1. The developed evaluation board enables rapid control of the driver circuitry as well as the verification of the ASIC which have been designed using the look table parameters in two step first on FPGA board to and later using MPW services an standard CMOS foundry especially for the needs of PLATON 2x2 router.

The test environment of the evaluation board is depicted in the Figure 7-2, consisting of an FPGA board to ensure in several steps the required input signal data stream is given, and also to provide the clock enabler signals. With the testing phase also the power consumption of such ASIC have been tested where supply voltage is 3.3V and the current in range of 1.4mA, corresponding to 4.62mW.

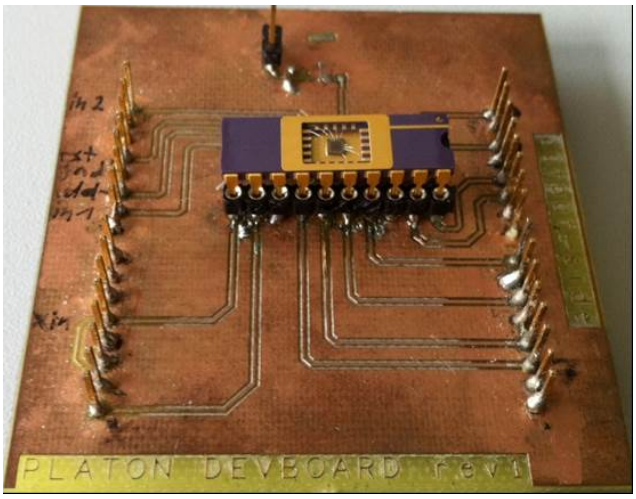

Figure 7-1: ASIC evaluation board.

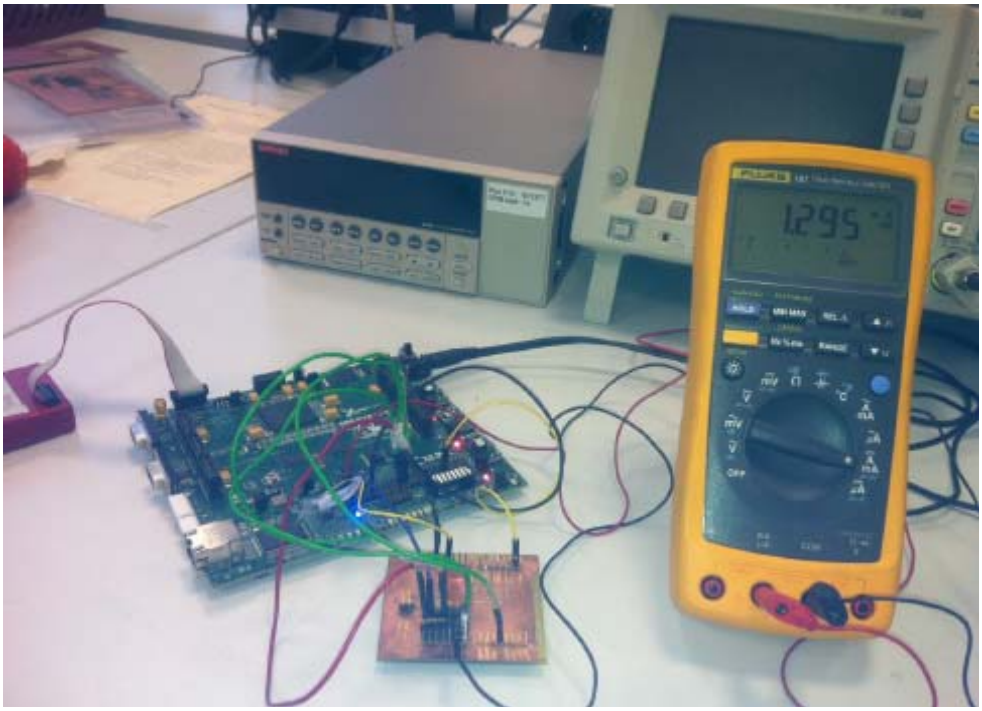

Figure 7-2: ASIC evaluation environments.

The developed driver circuit is depicted in Figure 7-3, which provides the needed signal level in order to enable the switching using the DLSPP based elements within 2x2 switching matrix. It consists the amplification of the ASIC output signals, since the supply voltage of the ASIC is limited the output signal level cannot be greater of the bounded ASIC, further it includes also limitation due to the current flow in order to avoid the overload of DLSPP based switching elements.

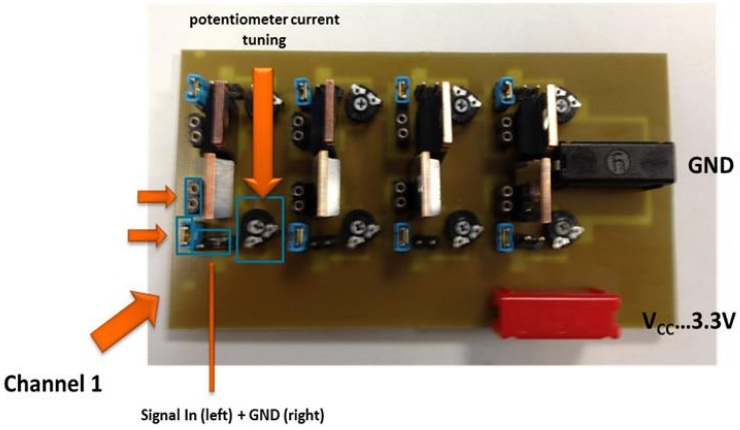

Figure 7-3: Driver circuit between ASIC DLSPP switch

8 PLATON 2x2 router package details

The silicon photonics based PLATON 2x2 router consisting of two 1x8 MUX stages, 2x2 switching matrix based on DLSPP switching elements, corresponding control ASIC have been assembled in an brass module on a ceramic platform with dedicated signal paths using standard microsystem integration technologies such as wire bonding. In order to keep housing dimensions as small as possible compact Glenair connectors have been considered to provide the required 75 electrical connections to the periphery. Here the details of the PLATON 2x2 router connections are provided. In Figure 8-1 all the PLATON 2x2 router module connectors are depicted and labeled accordingly.

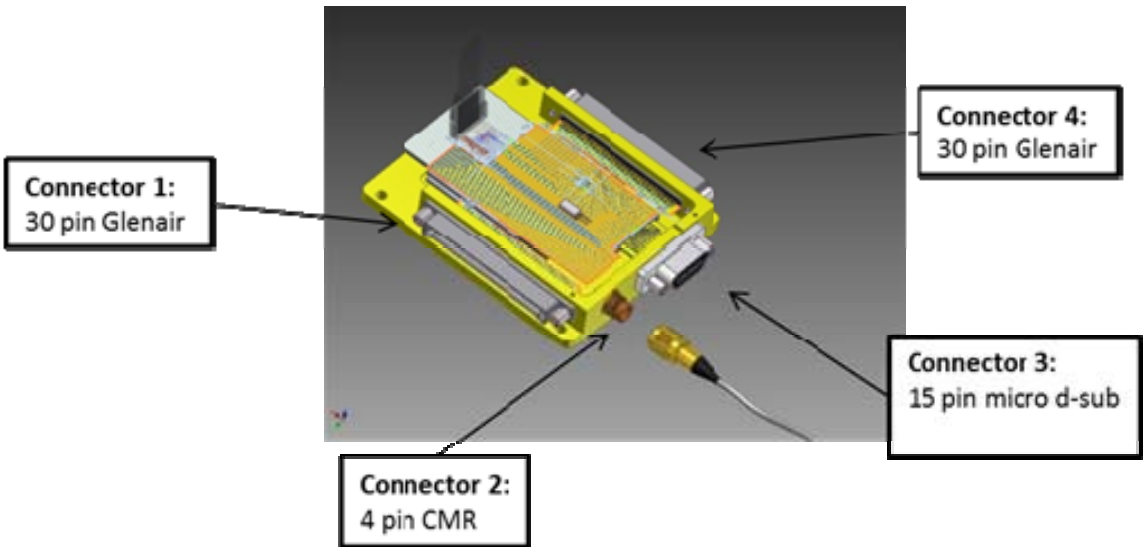

Figure 8-1: PLATON 2x2 router module connectors

In Figure 8-2 the overall signal paths within the PLATON 2x2 router have been labeled and taken as reference for the pin allocation for each of the connector.

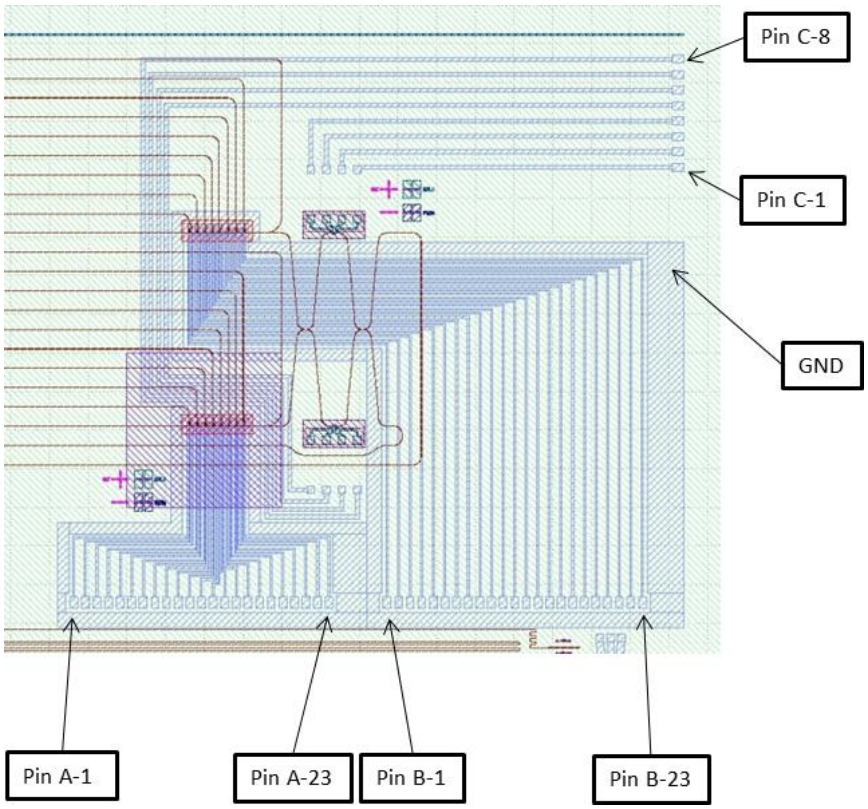

Figure 8-2: PLATON2x2 router overall electrical connections

In Figure 8-3 connector 1 , the 30pin Glenair connector depicted, the corresponding pin allocation is given in Table 8.1.

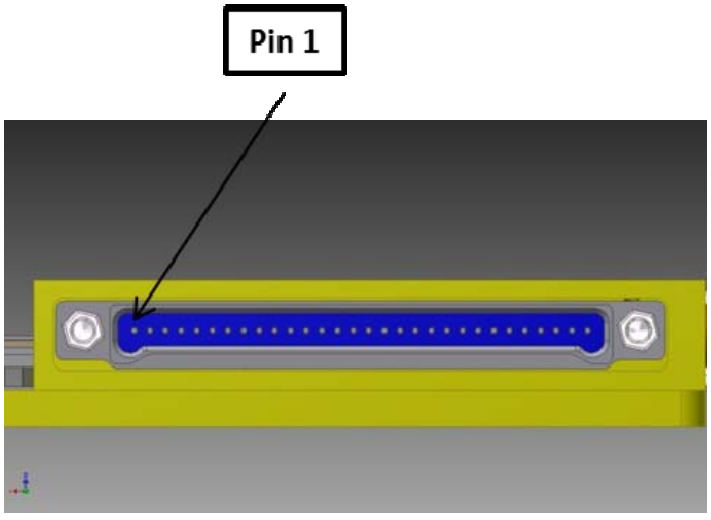

Figure 8-3: Connector 1(Glenair)

Table 8.1: Connector1 pin allocation

Connector 1	Routerchip	Cable color
1	Pin A-1	white
2	Pin A-2	grey
3	Pin A-3	violett
4	Pin A-4	blue
5	Pin A-5	green
6	Pin A-6	yellow
7	Pin A-7	orange
8	Pin A-8	red
9	Pin A-9	brown
10	Pin A-10	black
11	Pin A-11	white
12	Pin A-12	grey
13	Pin A-13	violett
14	Pin A-14	blue
15	Pin A-15	green
16	Pin A-16	yellow
17	Pin A-17	orange
18	Pin A-18	red
19	Pin A-19	brown
20	Pin A-20	black
21	Pin A-21	white
22	Pin A-22	grey
23	Pin A-23	violett
24	Pin B-1	blue
25	Pin B-2	green
26	Pin B-3	yellow
27	Pin B-4	orange
28	Pin B-5	red
29	Pin B-6	brown
30	Pin B-7	black

Figure 8-4 shows the four pin CMR connector to enable the interfaces to the AD590 temperature sensor and Peltier cooling element. The corresponding pin allocation is given in the Table 8.2 for the CMR 4 pin connector.

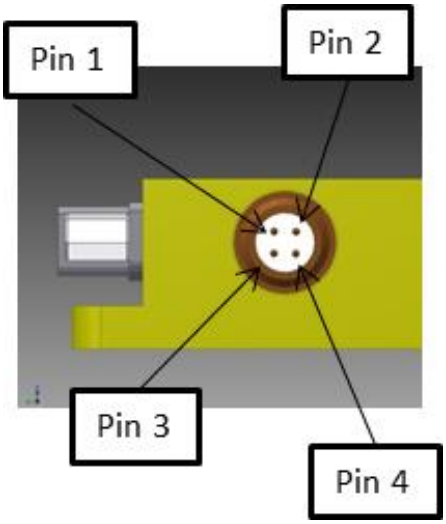

Figure 8-4: Connector 2 (4 pin CMR)

Table 8.2: Conector2 pin allocation

Connector 2	TEC/AD590
1	AD590 +
2	AD590 -
3	TEC -
4	TEC +

The Figure 8-5 provides the schematic of 15 pol Glenair connector and numbering of its pins. The related pin allocation can be found in the Table 8.3.

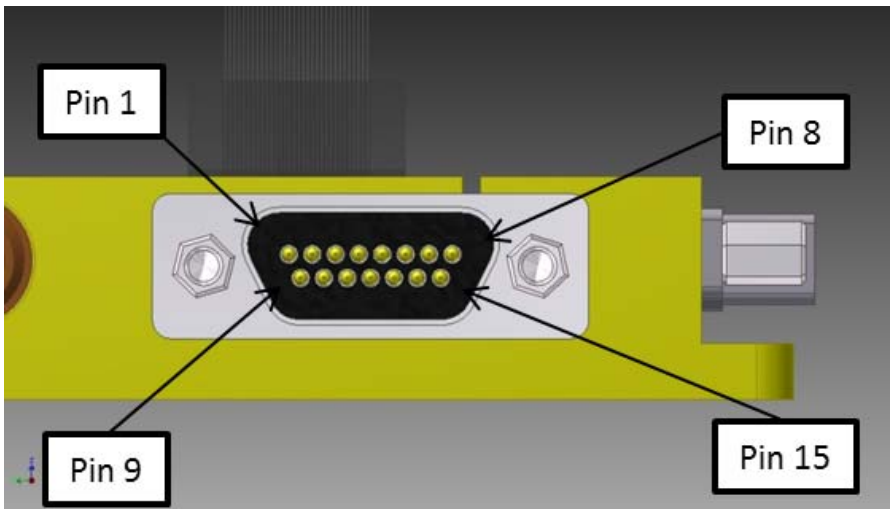

Figure 8-5: Connector3 15 pol connector

Table 8.3: Cnnector3 in allocation

Connector 3	Routerchip
1	Pin B-10
2	Pin B-11
3	Pin B-12
4	Pin B-13
5	Pin B-14
6	Pin B-15
7	Pin B-23
8	Pin B-22
9	Pin B-8
10	Pin B-9
11	n.c.
12	n.c.
13	n.c.
14	Pin B-21
15	Pin B-20

In Figure 8-6 the connector4 30 pin Glenair) is depicted with labeling to be used to contact the ASIC circuitry which has been hybrid integrated on the PLATON 2x2 router platform. Further the pin details of the ASIC is given in the figure 8.7.

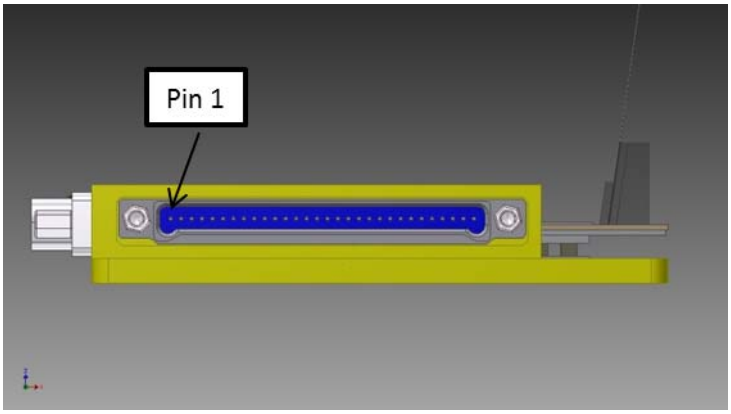

Figure 8-6: Connector4 30 pin Glenair

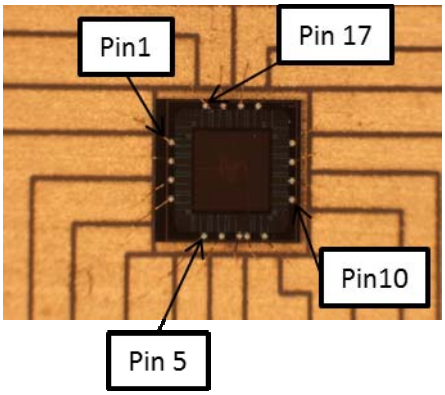

Figure 8-7: ASIC contact pads numbering

The corresponding pin allocation of the connector4 is listed in the Table 8.4, considering also the connections for ASIC.

Table 8.4: Connector4 pin allocation

Connector 4	Routerchip/Asic
1	Pin B-19
2	Pin B-18
3	Pin B-17
4	Pin B-16
5	GND
6	Asic 16
7	Asic 17
8	Asic 1
9	Asic 2
10	Asic 3
11	Asic 4
12	Asic 5
13	Asic 6
14	Asic 7
15	Asic 8
16	Asic 9
17	Asic 10
18	Asic 11
19	Asic 12
20	Asic 13
21	Asic 14
22	Asic 15
23	Pin C-1
24	Pin C-2
25	Pin C-3

26	Pin C-4
27	Pin C-5
28	Pin C-6
29	Pin C-7
30	Pin C-8

Finally Figure 8-7 illustrates the final form of the packaged 2x2 PLATON PLA19 router chip.

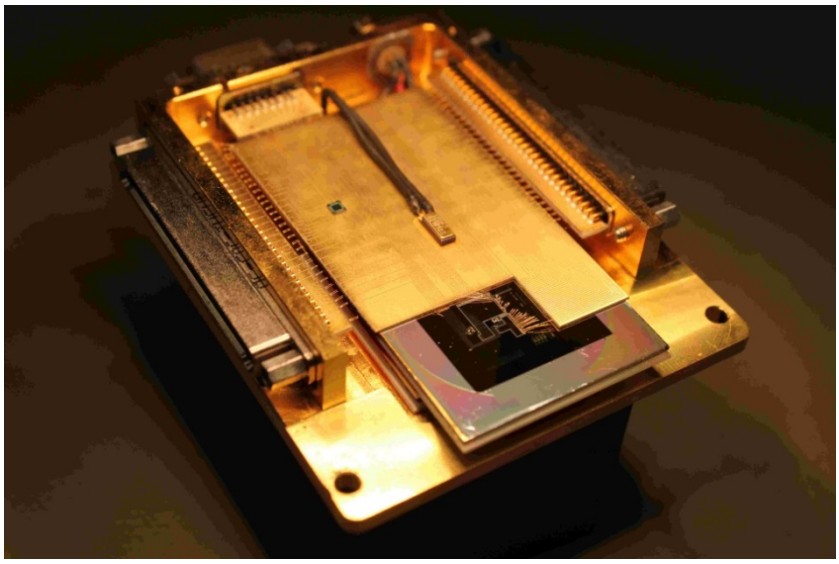

Figure 8-7: The completely packaged 2x2 PLATON router

9 Conclusions

This deliverable is reporting on packaging and fiber-pigtailing details of the PLA19 PLATON 2x2 optical interconnect router based on the PLA19chips. PLATON 2x2 router have been designed and fabricated based on silicon photonics platform consisting of 2 1x8MUX stages a 2x2 switching matrix based on DLSPP switching elements and control ASIC which have been assembled and pigtailed using established microsystem integration techniques and technologies in order to provide 79 electrical connections 22 optical I/Os. For this purpose a special housing has been developed using brass module with commercial available connectors and fiber arrays. This module includes also the driver circuit to enable the needed signal level for the switching functionality of the 2x2 DLSPP based switching matrix.