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**Merging Plasmonics and Silicon Photonics Technology
towards Tb/s routing in optical interconnects**

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TABLE OF CONTENTS

1	EXECUTIVE SUMMARY	4
2	INTRODUCTION.....	5
2.1	PURPOSE OF THIS DOCUMENT	5
2.2	DOCUMENT STRUCTURE.....	5
2.3	AUDIENCE.....	5
3	2X2 PLATON OPTICAL INTERCONNECT ROUTER	6
3.1	OVERVIEW OF THE 2X2 PLATON ROUTING CONCEPT	6
3.2	INTEGRATED 2X2 PLATON PLA19 ROUTER CHIP	8
4	EVALUATION TESTBED OF THE 2X2 PLATON OPTICAL INTERCONNECT ROUTER.....	10
5	EXPERIMENTAL EVALUATION OF THE 2X2 PLATON OPTICAL INTERCONNECT ROUTER (PLA19)	12
5.1	CUTBACK SECTION.....	12
5.2	REFERENCE STRUCTURES.....	13
5.3	2x2 PLATON OPTICAL ROUTER.....	15
5.3.1	<i>Regular fiber-array alignment.....</i>	<i>15</i>
5.3.2	<i>Alternative Characterization Solutions.....</i>	<i>16</i>
5.3.3	<i>Metal-induced loss simulations.....</i>	<i>19</i>
6	CONCLUSIONS	21

1 Executive Summary

This document reports on the experimental results obtained by the characterization and system-level evaluation of the 2x2 PLATON optical interconnect router. The 2x2 router is considered to be a crucial step towards the implementation of the entire 4x4 PLATON router chip, as it requires the seamless consolidation of all the fabrication techniques that were developed within the frames of the PLATON project.

The concept of the 2x2 PLATON router is based on the integration of various photonic, plasmonic and electronic components on the same SOI motherboard enabling the realization of a fully functional hybrid chip that will be able of accommodating and switching 560Gbps aggregate data traffic. The fabrication process was based on the mask layout of the router chip that describes in detail all the individual structures and building blocks of the 2x2 PLATON router, together with the necessary cutback waveguides and reference optical and electrical structures.

The optical testbed to be used for the system-level evaluation of the 2x2 router chip was assembled in NTUA premises and it comprises multi-wavelength optical and high speed electrical equipment capable of generating and assessing 40Gbps WDM data traffic both in signal visualizers and high-rate BER testing equipment. It also comprises an out-of-plane probe station that was utilized during the initial characterization of the chip.

The initial characterization measurements include measurements on the cutback waveguides and silicon reference structures, as well as the evaluation of the static performance of the SOI MUX and the 2x2 MZI-based plasmonic switch employing a 16-channel V-groove assembly (fiber array) as optical input. In the current document, alternative characterization solutions are also described utilizing single fibers (instead of fiber array) in various alignment arrangements.

Finally, the document presents a study on the detrimental effect of the reduced gap between the silicon waveguides and the metal layers on the optical propagation losses that hindered the system level evaluation of the 2x2 router, leading to valuable conclusions for the subsequent PLATON fabrication runs.

2 Introduction

2.1 Purpose of this document

The objective of this deliverable is to present the results on the characterization and system-level evaluation of the 2x2 PLATON optical interconnect router. It aims also to summarize the difficulties encountered by the consortium as well as the contingency plans and solutions that were developed and will be incorporated in future fabrication runs.

2.2 Document structure

The deliverable is organized into the following chapters:

- Overview of the 2x2 PLATON Routing Concept
- Integrated 2x2 PLATON Router Chip
- Evaluation test-bed of the 2x2 PLATON Optical Interconnect Router
- Experimental evaluation of the 2x2 PLATON Router Chip

2.3 Audience

This document is confidential.

3 2x2 PLATON Optical Interconnect Router

3.1 Overview of the 2x2 PLATON Routing Concept

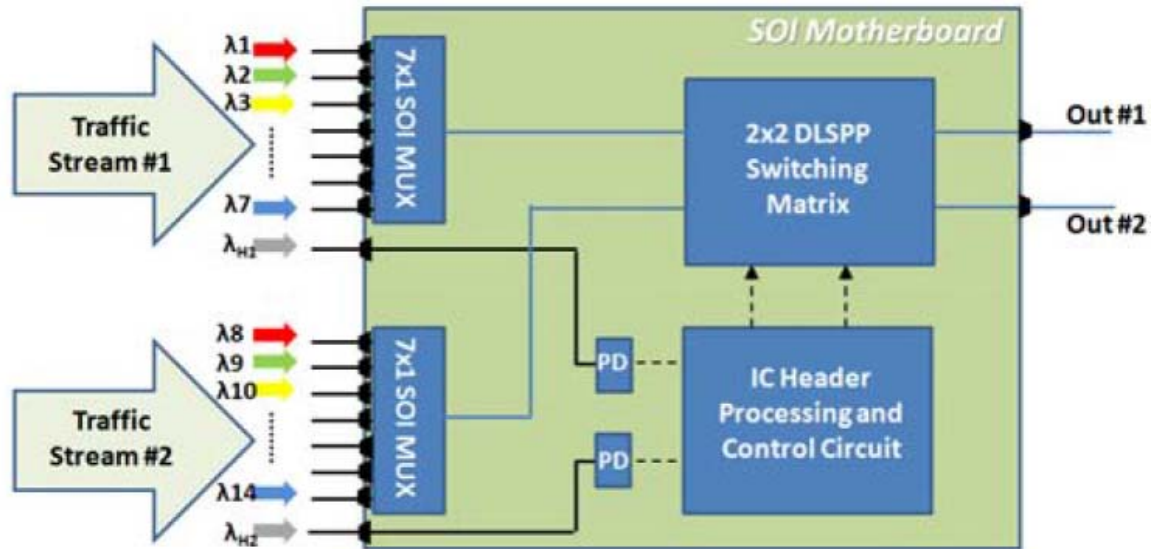


Figure 1: 2x2 PLATON Routing Concept

Figure 1 shows the block diagram of the PLATON 2x2 router system that operates with optical data line-rates of 40Gb/s and resides on a Silicon-on-Insulator Motherboard that hosts all the heterogeneous technologies, namely SOI-based components, Dielectric Loaded Surface Plasmon Polariton (DLSP) switches, Photodiodes and Integrated Circuit Microcontrollers, offering an aggregate switching throughput of 560 Gb/s. Briefly the role of each router sub-unit is as follows:

- **7x1 SOI MUX (Multiplexer):** This subsystem is used to multiplex the 7 incoming 40Gb/s data traffic carrying wavelengths into a common, single optical traffic stream that will follow the same route through the network. Two 7x1 SOI multiplexing modules will be employed in the 2x2 PLATON router platform while the SOI MUX will rely on silicon-based photonic integrated components.
- **PD O/E Conversion Stage:** Photodiodes integrated on the SOI motherboard will form the O/E conversion stage of the routing platform. PDs will be used for converting the optical header information into respective electrical header pulses to be subsequently processed by the IC Header Processing and Control Circuit. One PD will be employed for every header wavelength, which in turn implies that in the case of the 2x2 router a total number of 2 PDs will be necessary.
- **IC Header Processing and Control Circuit:** This subsystem is used for processing the incoming header information and for generating the appropriate electrical control signals that will drive the DLSP switching matrix. For the 2x2 router, the IC circuit

will have two input ports for receiving the respective electrical header pulse streams and will provide two electrical output signals for controlling the state of the 2x2 switching matrix.

- DLSPS switching matrix: The 2x2 DLSPS switching matrix routes the incoming traffic streams towards the different outputs depending on the header information. PLATON's switching matrix will rely on Dielectric Loaded Surface Plasmon Polariton (DLSPS)-based thermo-optic switching elements. A 2x2 switching matrix will be used for the 2x2 routing platform.

3.2 Integrated 2x2 PLATON PLA19 Router Chip

Figure 2 illustrates the gds mask layout of the 2x2 PLATON router chip that was generated by IZM in collaboration with AMO, UB, ICCS/NTUA and CETH.

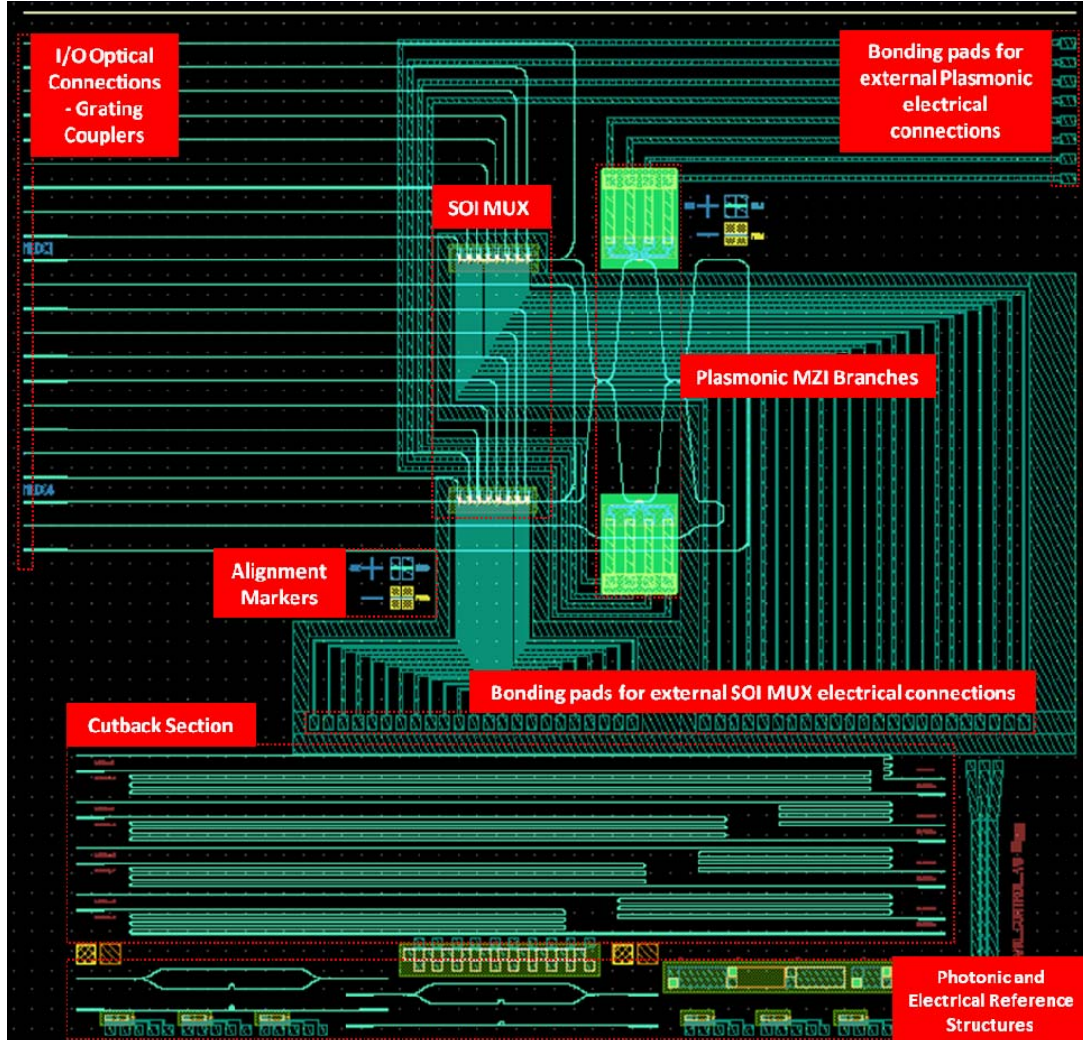


Figure 2: GDS mask layout of the 2x2 PLATON Router Chip

The mask comprises two different sections:

- ✓ **the actual 2x2 router structure.** The router structure consists of two 8:1 SOI multiplexers, one for each input port, that are optically connected, via a bus waveguide, to the hybrid MZI interferometer switch that is equipped with two plasmonic branches. The inputs of the multiplexers, as well as the output of the MZI switch, are connected to an array of grating couplers that enable the efficient coupling of light with optical fibers (arrayed in a V-groove assembly). In order to facilitate the tuning and biasing of the structure, a 90/10 coupler has been incorporated in the bus waveguide, allowing for individual operation of the multiplexers. The tap waveguide is also connected to the

grating coupler array. The thermal tuning of the multiplexers' ring resonators is enabled by heating elements that are placed on top of the WRRs. The heating elements are connected to an array of contact/bonding pads for external current injection. The thermo-optic switching operation of the plasmonic MZI is also based on the conductive connection of the underlaying gold layer of the Dielectric Loaded Plasmon Polariton waveguide with an external electrical signal source through the respective contact/bonding pads as shown in the figure.

- ✓ **the reference and cutback structures.** The cutback section comprises 8 silicon waveguides, equipped with grating couplers, with lengths varying from 8500 μm to 54000 μm . This section can be used so as to determine the propagation losses in the silicon waveguides as well as the coupling losses of the grating couplers. The reference structures include two all-silicon MZI interferometers exhibiting slightly different optical paths between the upper and the lower branches, and two WRRs with 20 μm radius, 0.25 μm and 0.35 μm gap respectively. The performance of the MZIs will dictate how close is the splitting ratio of the 3dB-couplers to the optimum 50:50 while the extinction ratio of the resonators will depend on the coupling efficiency between the straight and the bend waveguide as well as the propagation losses inside the ring cavity. Both reference structures together with the cutback section will provide valuable information on the fabrication quality of the 2x2 router chip.

4 Evaluation Testbed of the 2x2 PLATON Optical Interconnect Router

Figure 3 depicts a schematic of the optical testbed that has been assembled in NTUA premises so as to evaluate the performance of the 2x2 PLATON router in realistic, high-rate WDM data traffic conditions.

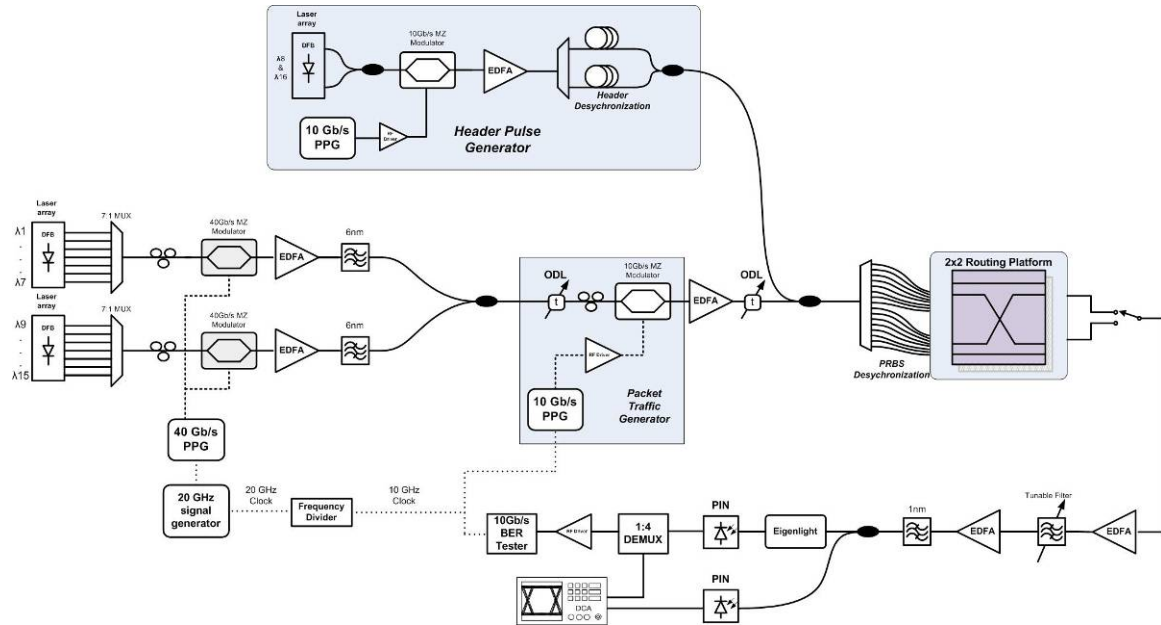


Figure 3: Evaluation testbed of the 2x2 PLATON optical interconnect router

The 7-channel WDM input optical signals are generated by two laser arrays each one consisting of 7 lasers of different wavelengths (in accordance with the ITU grid). Each 7-channel signal is consolidated in a single WDM stream through a WDM multiplexer and modulated with 40Gbps data through a LiNbO₃ amplitude modulator that is driven by a 40Gbps Pulse Pattern Generator (PPG) producing a 31st order Pseudo Random Bit Sequence (PRBS) electrical signal. Each WDM 40Gbps stream is then amplified by an EDFA, filtered by an optical bandpass filter and launched into the packet traffic generator through a 3dB coupler that combines the two streams into a single 14-channel data stream. The packet generation is based on the slow (kHz scale) ON-OFF operation of a 10Gbps LiNbO₃ modulator that is driven by a programmable PPG. The synchronization between the input 40Gbps data and the low rate packets is ensured through the use of an optical delay line (ODL) prior to the 10Gbps modulator. In all cases, optimum optical operation of the modulators is achieved through the utilization of polarization controllers at their inputs. After the packet generator, the 40Gbps WDM packet traffic is amplified in an EDFA and combined with the low-rate header signals through a 3dB-coupler. The header optical signals are produced by two laser modules, modulated in a common LiNbO₃ modulator and desynchronized using a WDM demultiplexer that feeds them into different optical fiber paths prior to their recombination. The proper time alignment between the 40Gbps WDM packet traffic and the header signals is ensured by the use of an ODL before the 3dB coupler.

The 16-channel WDM signal is entered into a 1:16 WDM demultiplexer and each tributary (channel) is launched into the respective input of the 2x2 router. The desynchronization of the 40Gbps PRBS channels is achieved at the input of the 2x2 routing platform using slightly different fiber lengths between the WDM demultiplexer and the chip. It should be also mentioned that in the experimental evaluation (that will be described in the following chapters) the header signals are applied directly in the electrical domain, since the current version of the under-test chip does not support on-chip optical header extraction and processing.

In the receiver part, manual selection between the output ports is performed so as to evaluate one output stream at a time. The selected 40Gbps stream is amplified and fed into a quite steep tunable optical band pass filter that is used so as to pick one out of the 7 WDM center wavelengths of the stream. The respective channel is then amplified again, filtered, and divided into two different tributaries. The one is fed into a photodiode that is connected to a 70GHz oscilloscope while the other is entered in the Bit-Error-Rate measurements setup. The setup consists of an Eigenlight attenuator/power-meter connected to a 40GHz photo-receiver. After the photo-receiver an 1:4 optical demultiplexer has been employed so as to down-convert the 40Gbps signal into 4 individual 10Gbps streams enabling the evaluation of the power penalty, induced by the switch, with the 12.5Gbps BER tester that is available in NTUA. The high-frequency clock that is necessary in order to synchronize the PPGs and the BER tester is provided by a high-precision signal generator.

5 Experimental Evaluation of the 2x2 PLATON Optical Interconnect Router (PLA19)

Before proceeding to the system-level evaluation of the 2x2 routing platform the chip was optically characterized in the out-of-plane probe station that is available in NTUA laboratory. The following figure shows an impression of the probe station with the 2x2 router chip placed on the vacuum chuck.

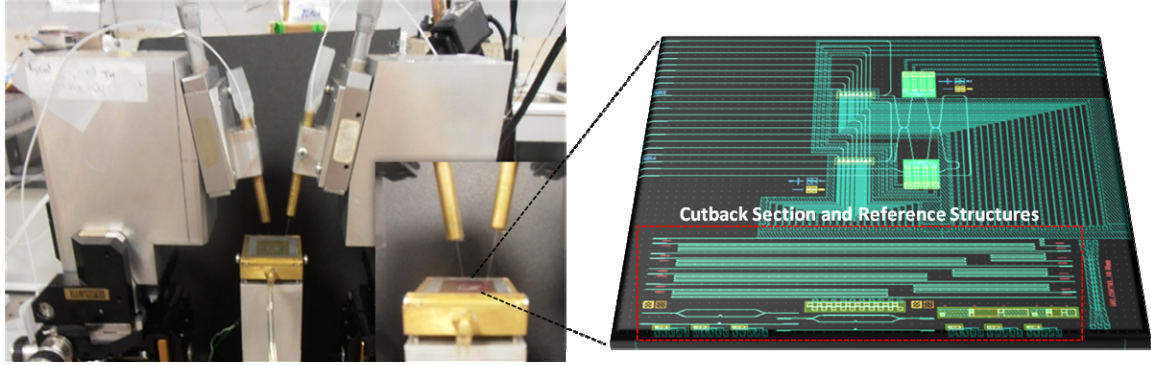


Figure 4: Out-of-plane probe station

The chip that was used in the characterization process described in the current document was part of the PLA19 fabrication round (chip PLA19_W3S1) which was the first 2x2 router fabrication attempt. It should be mentioned that at the time of the characterization the plasmonic branches were not connected to the electrical circuitry of the chips. According to the project plan the conductive connection between the gold (plasmonic) and aluminium (electrical circuitry) layer would be realized by means of on-chip wire-bonding.

5.1 Cutback Section

The cutback section was characterized using the regular out-of-plane probe station setup employing two opposite 10 degrees tilted cleaved fibers. The input signal was provided by a CW tunable laser while the output was measured in a power meter and monitored in an Optical Spectrum Analyzer (OSA). The necessary (for the DLSP waveguides) TM polarization was ensured by the use of a polarization controller between the laser and the probe station while spectrum measurements were obtained by sweeping the tunable laser across the 1500 nm to 1580 nm spectrum range.

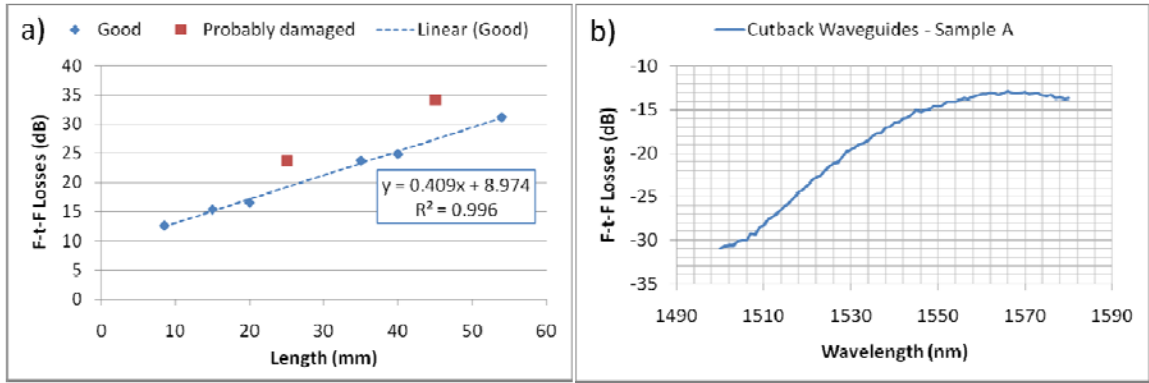


Figure 5: (a) Cutback measurements and linear fitting, (b) Spectral response of the first cutback waveguide

Figure 5 (a) depicts the fiber-to-fiber loss measurements (in dB) that were taken in the cutback section, plotted against the waveguide length. Linear fitting reveals that the propagation losses in the silicon waveguides were 4.1 dB/cm while the coupling losses were approximately 4.5 dB/grating. Two waveguides (red markers) were considered as damaged and excluded from the linear regression because of their unexpectedly high losses (taking the cutback measurements several times led us to the conclusion that there is a systematic error relating to the fabrication quality of those two individual samples).

Figure 5 (b) reveals the spectral behavior of the first cutback waveguide. As it can be seen, the response is quite smooth exhibiting a 48 nm 3dB-bandwidth centered around the 1566 nm wavelength. Approximately the same spectral results were also obtained for the rest of the cutback waveguide samples.

5.2 Reference Structures

During the characterization of the 2x2 router chip the first set of the reference structures, including an MZI interferometer and a WRR, as shown in Figure 6 (a), was evaluated.

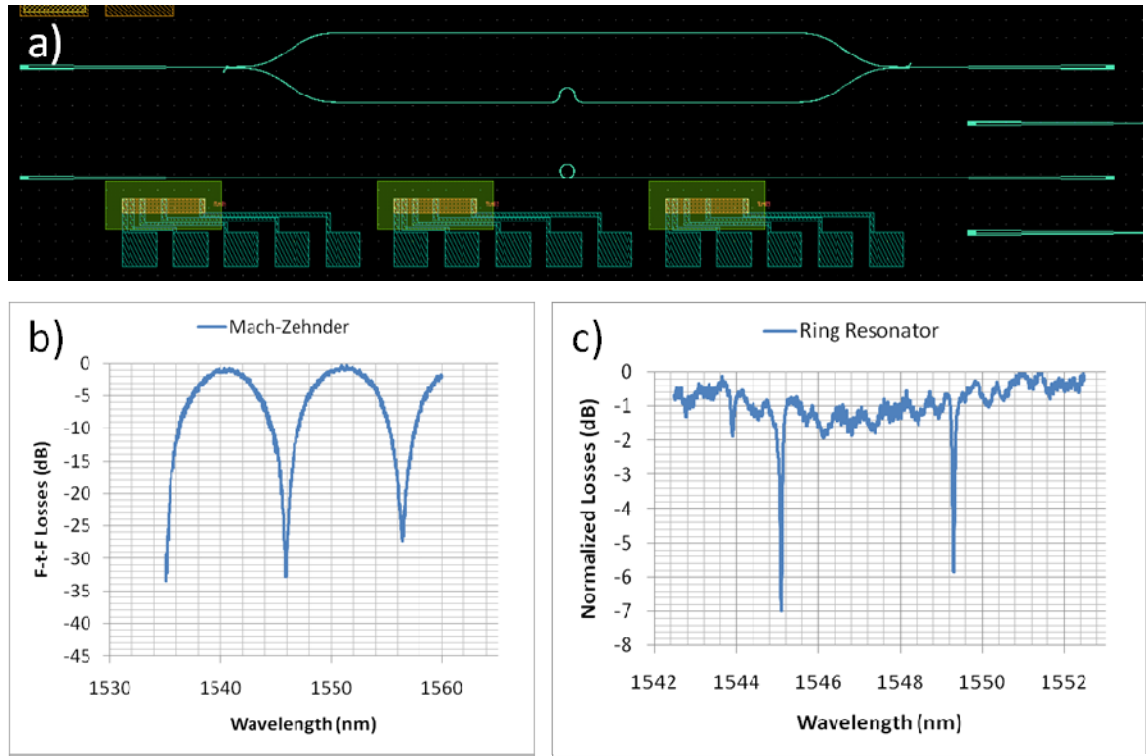


Figure 6: (a) Mask layout of the reference MZI and WRR structures, (b) Spectral response of the MZI and (c) Spectral response of the WRR

Figure 6 (b) shows the spectral response of the MZI that was obtained by sweeping a tunable CW laser across the 1535-1560 nm spectral window. It can be seen that the static extinction ratio of the filter is more than 30 dB dictating negligible loss difference between the two MZI branches as well as adequate performance of the 3dB couplers.

The spectral response of the ring resonator, also obtained with the tunable CW laser, is presented in Figure 6 (c). The extinction ratio of the ring filter is sufficiently high whereas the notches are quite steep, indicating good coupling between the straight waveguide and the ring cavity and low-loss light propagation inside the ring cavity.

Both results verify the advanced fabrication quality of the silicon optical circuitry.

5.3 2x2 PLATON Optical Router

5.3.1 Regular fiber-array alignment

As described in the previous paragraphs, the input and output optical connections of the 2x2 router are realized through grating couplers that are placed in a 1D array arrangement. To this end, the in and out light coupling is based on the use of a V-groove assembly comprising 16 fibers placed in 250µm spaced v-grooves (Figure 7 (a)) which is also the pitch of the grating coupler array. The end facet of the V-groove assembly was polished at 10 degrees (top-to-bottom) so as to comply with the optimum operation angle of the grating couplers.

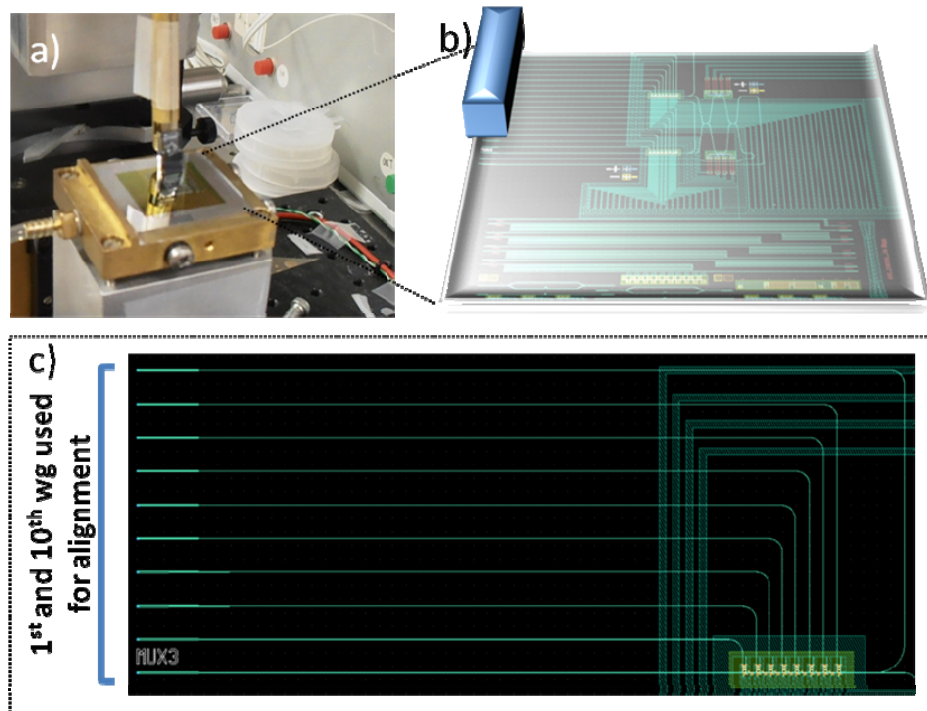


Figure 7: (a) Impression of the actual V-groove assembly alignment process, (b) 3D representation of the V-groove alignment process and (c) Waveguides that were employed during the alignment process

The chip was lacking alignment grating couplers, therefore the alignment of the fiber array relied on the use of the optical path connecting the common (bus) waveguide of the SOI MUX and the 10% tap waveguide as shown in Figure 7 (b) and (c). More specifically, the ASE produced by a high power EDFA was launched into the common (10th waveguide) and the output power and spectrum was monitored at the 10% tap waveguide (1st waveguide). Theoretically, the power measured at the output of the tap waveguide should be approximately 40 dB lower than the input because of the coupling and propagation losses, the spectrum that is sliced by the SOI MUX and the effect of the 10:90 coupler. Considering 17 dBm noise power at the input, the output power levels should be high enough to be measured by a regular optical power meter and monitored in an optical spectrum analyzer. However,

despite the several characterization attempts, the output levels were negligible, prohibiting the fiber-array alignment on top of the grating couplers. As a result, alternative characterization solutions were pursued so as to both characterize the 2x2 router chip and identify the reason of the aforementioned fiber-array alignment issue.

5.3.2 Alternative Characterization Solutions

- 1st Setup: Two approximately parallel fibers

The first solution that was followed included the replacement of the fiber array with two cleaved SMF fibers in order to ease the alignment process. In order to be able to place the fibers on top of the 1st and the 10th waveguide of the grating coupler array, the mechanical setup of the vertical probe station had to be re-arranged so as to introduce the same (and not opposite) angle to the fiber holders and the chip had to be rotated by 90 degrees. The respective configuration is shown in Figure 8 (a-f).

As it can be seen in Figure 8 (a) and (b), it was possible to achieve a θ_y angle of 10 degrees, as required by the grating coupler design, however, due to certain equipment limitations, it was unfeasible to bring the fibers close enough keeping them parallel at the same time. A small θ_x angle had to be introduced to each fiber as a compromise between fiber proximity and coupling efficiency. The effect of this angle was evaluated using the already characterized cutback section, revealing more than 10 dB additional coupling losses per coupler.

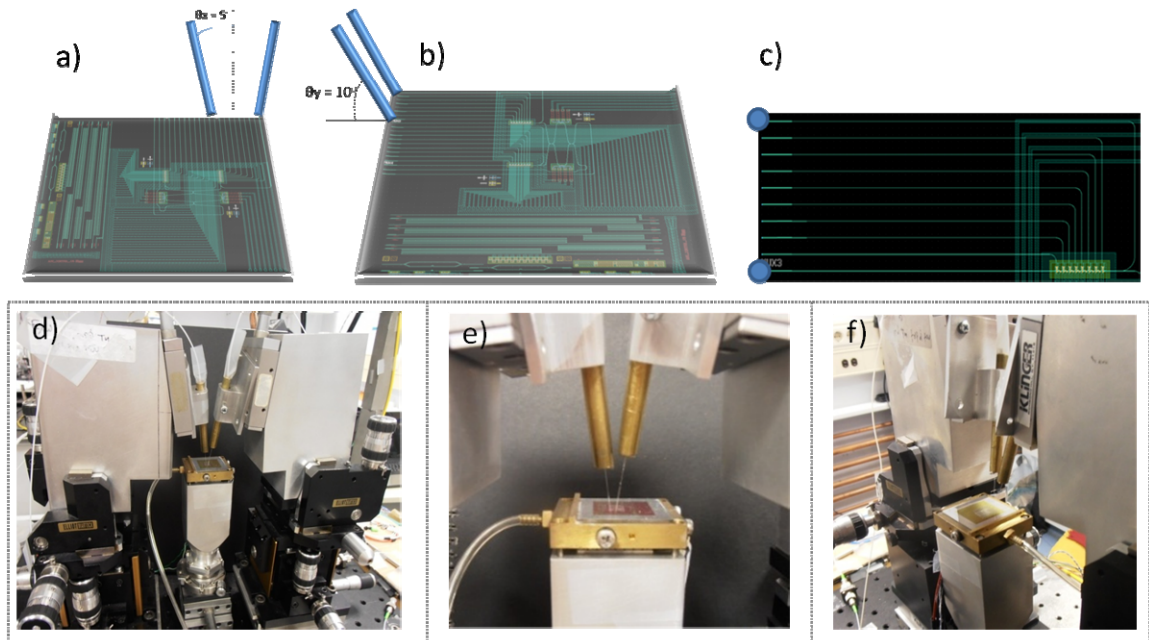


Figure 8: (a), (b) Graphical representation of the approximately parallel fibers, (c) Waveguides that were used during the alignment process, (d) – (f) Impression of the modified probe station

The characterization attempt led again to negligible power levels at the tap waveguide output (using the aforementioned ASE noise as input). Consequently, a different approach should be followed allowing for single fiber (not fiber-array) alignment and considerably lower impact on the coupling losses.

- 2nd Setup: Two opposite fibers

The 2nd alternative solution is based on the attribute of the grating coupler to emit/receive radiation in more than one angles due to higher orders of diffraction. Following that, one could use the regular probe station (the one used during the cutback and reference structures characterization) bringing the fiber holders close to each other and attempt to couple light from a negative angle in the common (bus) SOI MUX waveguide, as shown in Figure 9. This way, in contrast with the first alternative solution, the output fiber will still be optimally aligned on top of the grating coupler yielding minimum coupling losses, overcoming at the same time the equipment limitations imposed by NTUAs probe station configuration.

Since the grating coupler design, though, has been optimized so as to maximize its performance for the 1st order of diffraction, any angle different than +10 degrees would lead to increased coupling losses. In this case, the effect of putting the fibers in -10 degrees was calculated by performing measurements on the cutback waveguides and comparing the outcome with already obtained results. To this end, the probe station configuration shown in Figure 10 (a) and (b) was utilized.

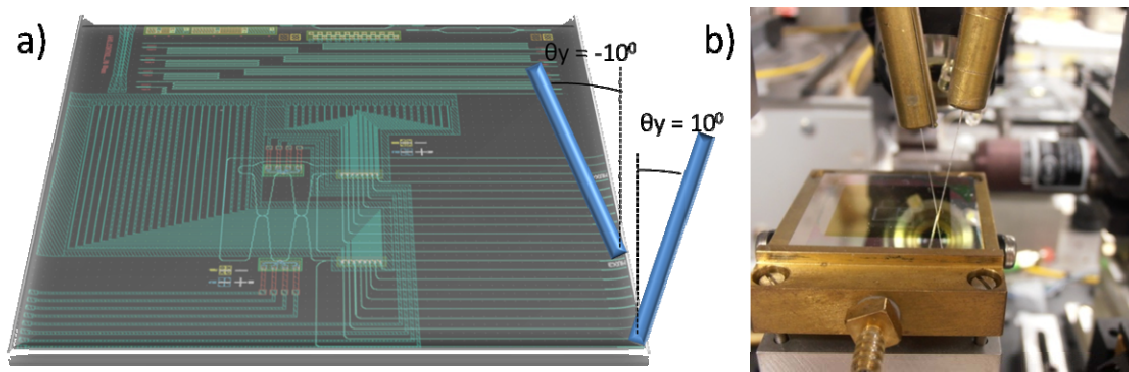


Figure 9: (a) Proposed concept with two opposite fibers, (b) Realization of the concept

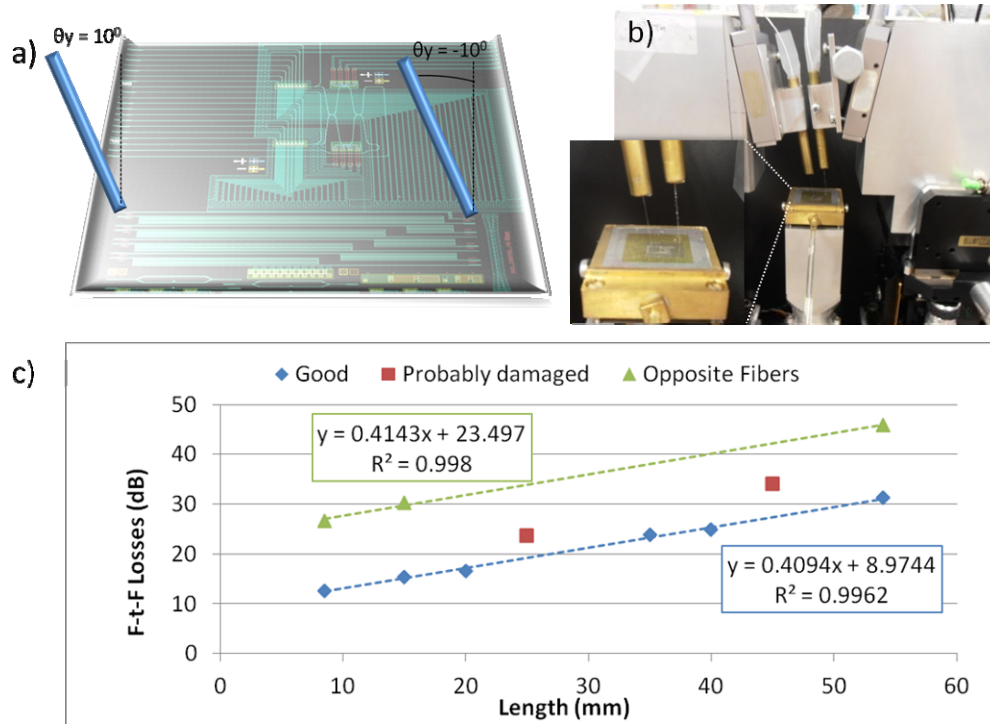


Figure 10: (a) Verification of the proposed concept on the cutback section, (b) Probe station configuration and (c) Comparison between the performance of the cutback waveguides for regular and opposite fibers.

Figure 10 (c) depicts the comparison between the regular cutback results and some indicative measurements that were taken using the opposite-fibers configuration. It can be seen that the operation of the input grating coupler at -10 degrees leads to 15dB additional coupling losses. Given the 17dBm noise input power and the -80dBm sensitivity of the power meter, the available power budget was more than enough to enable the characterization of, at least, the SOI MUX structure. However, even though all the SOI MUX inputs and the common MUX waveguide were tested, the power levels were negligible in all cases. It should be noted at this point that the correct alignment of the optical fibers on top of the grating couplers was verified by launching light in the fibers and monitoring the reflection spectrum using a circulator between the ASE noise source and the fiber. When the fiber was on top of the grating coupler the filtering characteristics of the latter appeared in the spectrum.

5.3.3 Metal-induced loss simulations

According to the measurements that were performed on the cutback section and the reference structures, the propagation and coupling losses of the silicon waveguides fall well within the acceptable limits whereas the directional couplers and ring gaps exhibit adequately good performance. Therefore, the negligible power levels that are obtained at the output ports of the 2x2 router cannot be explained by the optical part of the 2x2 router chip.

A more detailed look at the mask layout of the integrated chip, reveals that a large part of the optical circuitry of the silicon multiplexer is covered with an aluminium layer due to the on-chip electrical connections. Furthermore, the ring resonators themselves are equipped with Ti heaters as shown in Figure 11. It is well known that the high imaginary part of the refractive index of metals could have detrimental effect on the propagation of optical signals if the metal layer is placed close to the photonic waveguide. For the 2x2 Platon Router chips the distance between the top of the waveguide and the bottom of the Al/Ti layer is determined by the thickness of the protective Spin-on-Glass layer that has been spin-coated on top of the silicon chip. In the case of the PLA19 chip, the thickness was decided to be reduced from 850 nm down to 500 nm in order to facilitate subsequent fabrication steps that, however, fall out of the scopus of the current document. Taking into consideration the 400x340nm rib waveguide platform configuration (50 nm slab) , one can readily calculate that the distance between the waveguide and the metal layer was only 210 nm.

In order to estimate the effect on the propagation of the field, an FD solver (available in NTUA), capable of calculating the metal induced losses in high-index contrast structures, was employed. Figure 12 (a) and (c) illustrate the index profile of the electromagnetic problem that was imported in the mode solver for 850 nm SOG and 500 nm SOG, while Figure 12 (b) and (d) show the respective field distributions that were calculated. It is clear that in the case of 500 nm the field distribution is

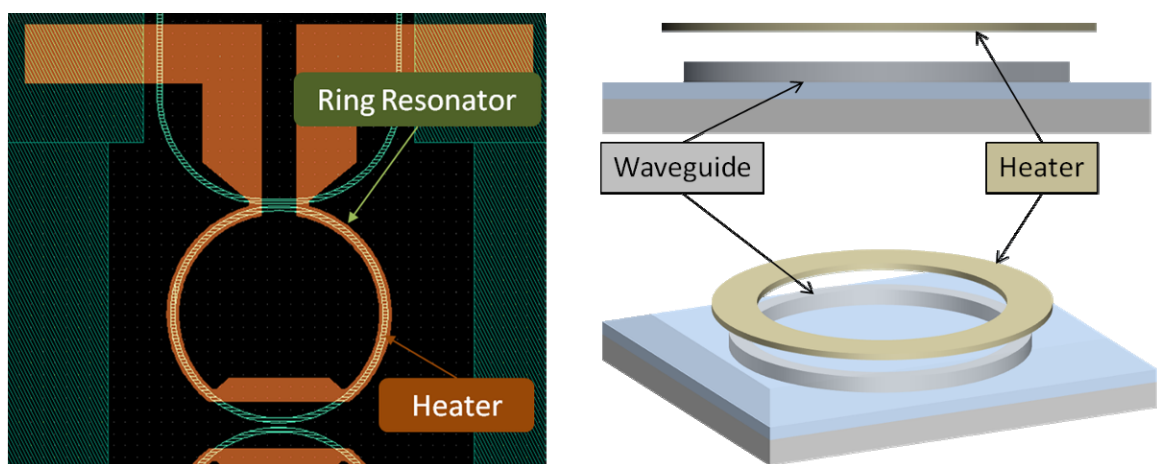


Figure 11: Waveguide Ring Resonator with Heater

severely affected by the presence of the metallic layer. By processing the imaginary part of the effective refractive index of the calculated modes, the following propagation losses are derived:

- SOG height 850 nm, metal-waveguide distance 560 nm : **0.67dB/cm**
- SOG height 500 nm, metal-waveguide distance 210 nm : **266 dB/cm**

These results, lead seamlessly to the conclusion that the reduced distance between the waveguide and the metal interface induces prohibitively high losses, severely degrading the performance of the silicon optical circuitry. This issue has been addressed by the consortium in future fabrication runs, namely PLA20 and PLA22. The characterization results obtained by those chips will be reported in D6.3.

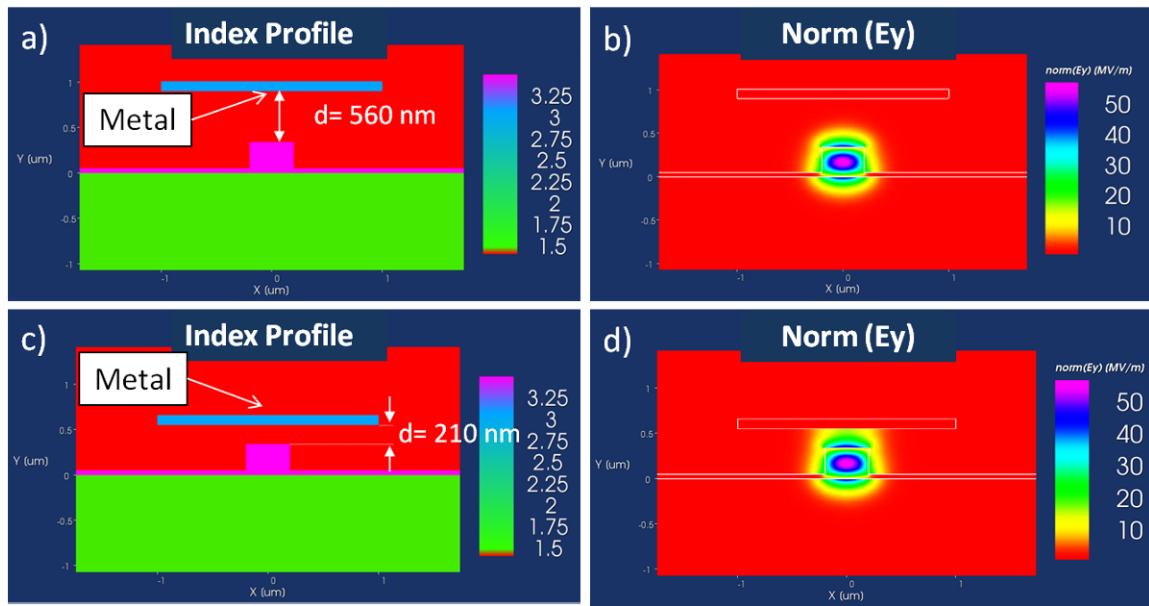


Figure 12: (a) Index profile imported in the mode solver for 850 nm SOG, (b) Calculated fundamental TM mode – field distribution for 850 nm SOG, (c) Index profile imported in the mode solver for 500 nm SOG and (d) Calculated fundamental TM mode – field distribution for 500 nm SOG

6 Conclusions

This deliverable summarizes the experimental results that were obtained during the characterization of the 2x2 PLATON optical interconnect router as well as the optical test-bed that has been assembled for the system-level evaluation. The successful convey of the 2x2 router concept to an integrated photonic circuit, exhibiting also plasmonic and electrical functionality, has been demonstrated through the description of the generated (.gds format) mask layout, while several characterization attempts, including light coupling with V-groove assembly and single cleaved SMF fibers were presented, all leading, however, to negligible power levels at the output. Finally, an investigation on the effect of the metal layer on the performance of the silicon waveguides revealed that the reason of the unsuccessful characterizations is highly related to the small gap between the waveguides and the electrical circuitry of the chip.