ICT - Information and Communication Technologies

Merging Plasmonic and Silicon Photonics Technology towards Tb/s routing in optical interconnects

Collaborative Project

Grant Agreement Number 249135

D3.2 Fabrication of passive SOI components and integration of Ge photodiodes

Due Date of Deliverable: 30/09/2011

Actual Submission Date: 03/11/2011

Revision: Final

Start date of project: January 1st 2010 **Duration:** 36 months

Organization name of lead contractor for this deliverable: AMO

Authors: M. Baus (AMO), M. Karl (AMO), T. Tekin (IZM), A. Suna (IZM), S. Papaioannou (CERTH), K. Vyrsokinos (CERTH), G. Kalfas (CERTH), N. Pleros (CERTH), D. Kalavrouziotis (NTUA) , G. Giannoulis (NTUA), I. Lazarou (NTUA), D. Apostolopoulos (NTUA), H. Avramopoulos (NTUA).

Project Information

PROJECT	
Project name:	Merging Plasmonic and Silicon Photonics Technology towards Tb/s routing in optical interconnects
Project acronym:	PLATON
Project start date:	01/01/2010
Project duration:	36 months
Contract number:	249135
Project coordinator:	Nikos Pleros – CERTH
Instrument:	STREP
Activity:	THEME CHALLENGE 3: Components, Systems, Engineering
DOCUMENT	
Document title:	Fabr. of passive SOI comp. and integr. of Ge photodiodes
Document type:	Report
Deliverable number:	D3.2
Contractual date of delivery:	30/09/2011
Calendar date of delivery:	03/11/2011
Editor:	Matthias Baus (AMO)
Authors:	M. Baus (AMO), M. Karl (AMO), T. Tekin (IZM), A. Suna (IZM), S. Papaioannou (CERTH), K. Vyrsokinos (CERTH), G. Kalfas (CERTH), N. Pleros (CERTH), D. Kalavrouziotis (NTUA) , G. Giannoulis (NTUA), I. Lazarou (NTUA), D. Apostolopoulos (NTUA), H. Avramopoulos (NTUA)
Workpackage number:	WP3
Workpackage title:	SOI platform and RF/IC circuitry development
Lead partner:	AMO
Dissemination level:	CO - Confidential
Date created:	30/09/2011
Updated:	02/11/2011
Version:	V10
Total number of Pages:	39
Document status:	Final

Table of contents

1 Executive Summary

This document provides a detailed overview of the progress on the fabrication of PLATON's silicon-on-insulator (SOI) photonic components. This includes several passive components, partially equipped with integrated heating elements, and a photodiode for header detection.

Photonic waveguides, fiber couplers and multiplexing (MUX) circuits are the main passive components realized here in SOI. Their fabrication is reported and supplemented by the final design that has been considered and their simulation-based performance evaluation.

Furthermore, progress of the integrated photodiode is described. There is a deviation in the kind of photodiode for header detection: Already at an early stage it has been figured out that an all-silicon photodiode is much simpler to incorporate into the complex process flow for chip fabrication than the originally envisaged germanium diode. This route has been followed for monolithical integration and progress is reported.

Moreover, the process flow for the complete SOI motherboard towards the integration of the final PLATON 2x2 and 4x4 routing platforms has been defined and included in this document. This document also includes confidential details for the design and fabrication of the above mentioned components in the annex.

2 Introduction

2.1 Purpose of this document

This document provides a detailed overview of the fabrication of passive SOI components and photodiodes and summarizes their optical performance. To this end it reviews the specifications and design issues and includes the description of the processes for the fabrication of the overall SOI platform.

The deliverable aims to provide the basic fabrication process needed for the integration of all components that have to be integrated for the routing platform. It provides also the basis for the integration of SOI multiplexing circuits including tunable microring resonators and photodiodes.

2.2 Document structure

The present deliverable is split into 9 chapters and an annex:

- Executive Summary
- Overview of the SOI motherboard
- Nanophotonic Waveguides
- Fiber-to-chip coupling
- MUX with metal heaters
- Integrated photodiodes
- Overview of the full motherboard integration process
- Conclusions

2.3 Audience

This document is confidential. A public version will be created to make it available on PLATON's website.

3 Overview of PLATON´s Silicon-On-Insulator (SOI) motherboard

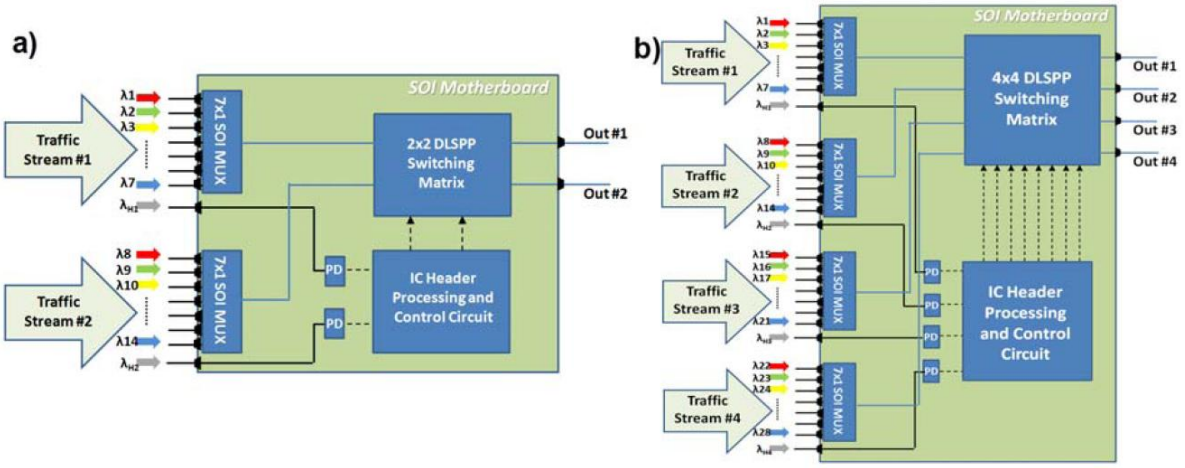


Figure 3.1: PLATON's a) 2x2 and b) 4x4 router block diagram.

Figure 3.1(a) and (b) show the block diagrams of the PLATON 2x2 and 4x4 router system, respectively, as these have been already described in detail in D2.1. Both routing platforms operate with optical data line-rates of 40 Gb/s and reside on a Silicon-on-Insulator Motherboard that hosts all the heterogeneous technologies, namely SOI-based components, Dielectric Loaded Surface Plasmon Polariton (DLSPP) switches, and Integrated Circuit Microcontrollers. The 2x2 router offers an aggregate switching throughput of 560 Gb/s, whereas the 4x4 router provides a total throughput of 1.12 Tb/s.

PLATON's Silicon-on-Insulator (SOI) motherboard chip will contain silicon nanophotonic elements as waveguides, grating couplers, multiplexing circuitry, and photodetectors and will be capable to host the plasmonic switching elements and the IC control circuitry. To this end, the non-plasmonic (sub-)systems and configurations to be employed on the SOI motherboard will include the following monolithically integrated devices:

a. **Silicon waveguides and Si-to-DLSPP couplers** for guiding light in the SOI chip and interposing to the plasmonic part, respectively.

b. **Fiber coupling structures** for allowing optical fibers to be interfaced with the PLATON routers.

c. **Optical 7x1 MUX circuitry** capable of multiplexing up to 7 optical data wavelengths with 100GHz channel spacing into a single waveguide.

d. **Monolithically integrated photodiodes** that will be used for the optoelectronic conversion of the packet-rate header pulses in order to drive the IC micro-controller circuit with the electrical header information.

In addition the following components have to be taken into account for the integration process

e. **A gold lift-off chip area** to enable subsequent DLSPP waveguide writing processes, so as to allow for the incorporation of the DLSPP-based switching matrix.

f. **An IC microcontroller circuit** to be hybridly integrated on the SOI motherboard, being responsible for processing the packet header information and for generating the appropriate electrical control signals to drive the DLSPP switching matrix

g. Metal interconnects for guiding the electrical-RF signals inserted into or generated by the IC circuit and for thermal tuning of the SOI MUX circuitry.

A schematic representation of these building blocks and their positioning on the SOI motherboard is provided in Figure 3.2.

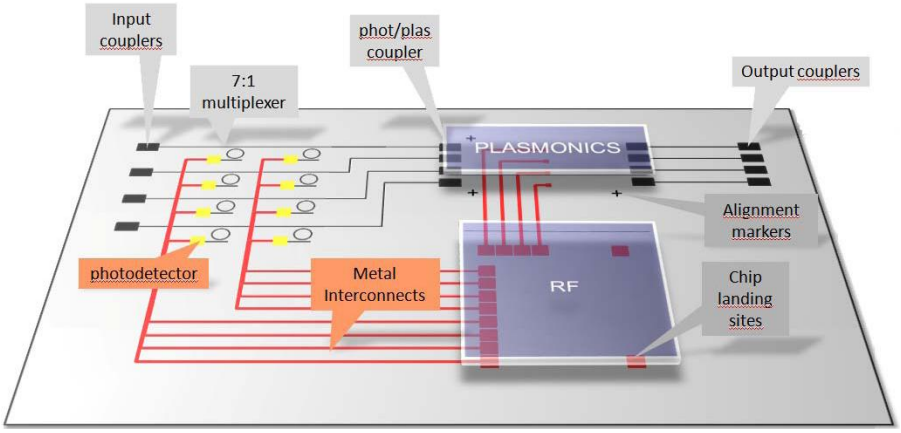


Figure 3.2: PLATON's SOI motherboard and its various building blocks.

4 Silicon Nanophotonic Waveguides

4.1 Introduction, Design, Simulation

As PLATON's routing platforms employ three different technologies, namely silicon photonics, plasmonics and electronics, compatibility between the various components and sub-systems has to be ensured in order to allow for their seamless interfacing and interoperability. Regarding the Silicon waveguide structures, their compatibility operational framework enforced mainly by the plasmonic elements incorporated in PLATON is the following:

- Requirement for single-mode operation in order to avoid enhanced power losses due to power coupled to more than one modes, since the Dielectric-Loaded Surface Plasmon Polariton waveguides are capable of supporting only the TM mode.
- Requirement for TM mode operation, again in order to keep the power losses at the minimum possible level due to the strictly TM-supporting plasmonic waveguides.
- Requirement for nanometer waveguide dimensions, so as to ensure optimal waveguide dimension matching conditions between silicon and DLSPP structures. The DLSPP waveguide structures have a dielectric loading of 500x600 nm^2 placed on top of a 60nm thick gold film (see D2.3, D2.4).
- Requirement for process compatibility for the integration of the photodiodes electrical contacts.

These conditions indicate the nano rib-waveguides with 340nm height, 50 nm slab height, and 400 nm width as a single-mode waveguide structure for TM polarization. The choice of 340 nm for the Si waveguide core height has been made on the basis of using commercially available SOI wafers (220nm and 340nm SOI thicknesses are available) as well as on its properties for guiding TM polarization (better guided in 340nm thick SOI). This will be confirmed in the following sections that describe simulation results obtained for strip waveguides, providing also calculations about their light coupling losses when direct butt coupled to an optical fiber.

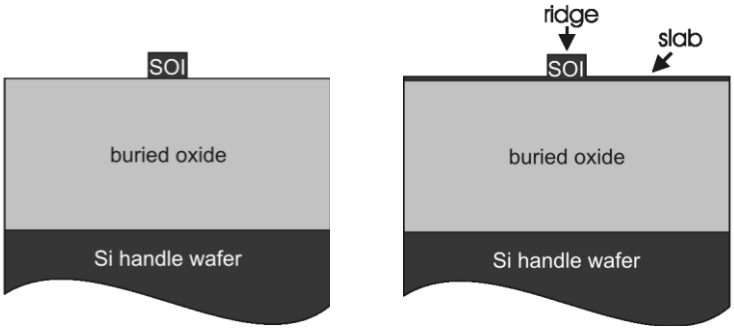


Figure 4.1: Comparison of the cross-section of Strip (left) and Rib (right) waveguides.

For the integration of active silicon structures the Rib waveguide approach offers significant advantages. In the following table we show that Rib waveguides (in contrast to Strip waveguides) are compatible to all processing modules required to integrate the overall PLATON routing platform.

	Strip	Rib
MUX	No etch stop for top-dielectric	Silicon slab = etch stop
PD	Integration of electrical contacts not possible	Easy integration of electrical contacts
DLSPP	OK without top dielectric	OK

Table 4.2: Comparison of integration issues of Strip and Rib waveguides.

4.2 Fabrication: SOI nanophotonic waveguide technology

AMO has developed a reliable fabrication process for SOI nanophotonic structures that is based on an exact control of the critical lateral dimensions of the photonic nanodevices. The process technology guarantees excellent reproducibility. Additionally, process quality parameters such as surface roughness are optimized with respect to their influence on optical performance of the devices.

The electron beam lithography (EBL) processes used to fabricate waveguides and resonator devices is based on the use of hydrogen silsesquioxane (HSQ) as a negative tone resist material. An optimized high contrast development process is necessary to achieve high resolution, a step resist profile and a smooth resist surface. HSQ allows a good control of the gap width between the ring resonator and the waveguides. An reactive ion etching (RIE) process based on HBr chemistry will be used for device fabrication. This process shows a high selectivity to the underlying buried oxide, smooth waveguide and resonator surfaces and a high degree of anisotropy.
The available EBL processes have proven to guarantee high CD accuracy, low sidewall roughness and good chip-to-chip reproducibility. Therefore, an EBL based fabrication is suitable for fast prototyping and exploration of the potential of different design variations.

As an example, the process for rib waveguide patterning has been optimized by tuning the relevant parameters of the RIE etching process, mainly as gas pressure and plasma power. Using this optimized process the trenching effect – a well known effect in anisotropic etching processes – is suppressed.

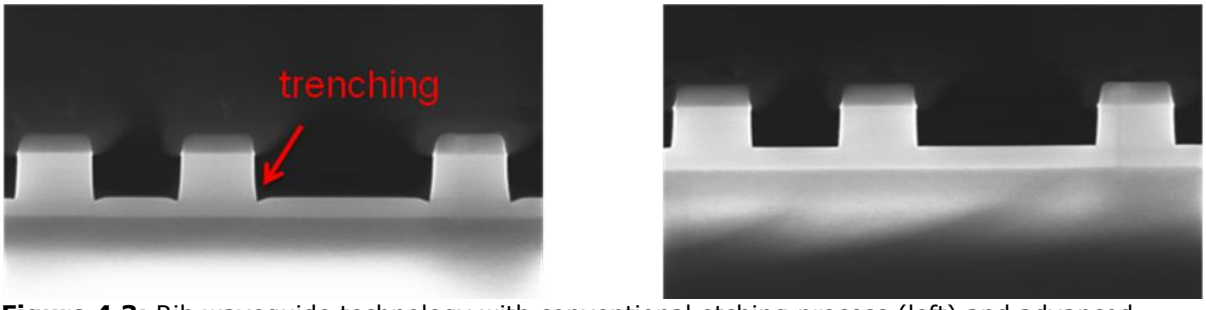


Figure 4.3: Rib waveguide technology with conventional etching process (left) and advanced etching process (right).

4.3 Characterization: Propagation losses in SOI waveguides

The optical losses of the silicon nanophotonic platform have been characterized in order to evaluate its influence on the performance of PLATON´s overall routing platform. Cut-back structures have been fabricated that comprise waveguides with a cross section of 340 x 400 nm², a slab height of 50 nm, and different lengths ranging from 0.3 to 2.8 cm. Both ends of the waveguides are equipped with grating couplers (non-optimized in this case).

When drawing the overall losses of each waveguide structure in dB over the waveguide length a linear behaviour is clearly evident (see Fig. 4.4). The linear losses given by the slope are in the order of 2.5 dB/cm for TM polarization.

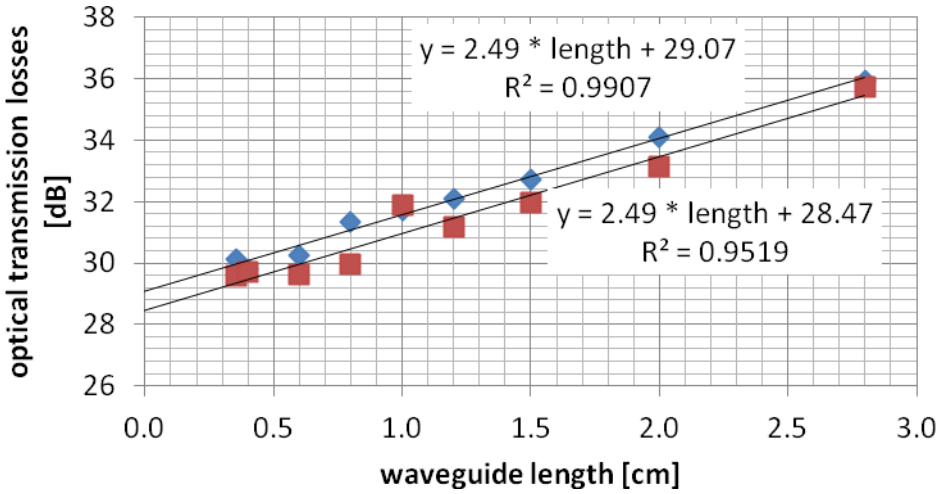


Figure 4.4: Waveguide losses: Rib waveguides 340 x 400 nm² (with non-optimized grating couplers).

The measured propagation loss of 2.5dB/cm is difficult to compare to other publications since TM polarization and an individual rib geometry has been chosen for PLATON´s purposes. TM polarization is less commonly used because propagation losses tend to be higher. Nevertheless, some comparison can be done to published data: The thin slab thickness used here make the waveguides comparable with completely etched strip waveguides. Such waveguides show propagation losses in the range of 3.6dB/cm for TM modes with a 445x220nm² cross-section [1] - for 340nm SOI lower losses are expected.

4.4 Si-to-DLSPP coupling structures

In order to integrate the plasmonics in a seamless way, Si-to-DLSPP coupling structures have been developed to match the mode profile between the SOI and the DLSPP waveguides and thereby minimize the optical losses. In the pure SOI platform, this Si-to-DLSPP coupling structure consists of an inverted taper with nominal width of 175nm at the end. Consciously the Si-to-DLSPP coupling structure has been designed in a way that no additional fabrication steps are required, i.e., it is defined by the same process the SOI waveguides are structured. This is possible because EBL is used for the photonic SOI layer and feature sizes of 175nm are not a problem at all. Details on the specification of the Si-to-DLSPP coupling structure can be found in Deliverables 3.1, 2.4.

5 Fiber Coupling Structures

5.1 Introduction

Grating couplers are the best solution for testing nanophotonic circuits. The main benefit is that they allow access via an optical fiber from the top and therefore there is no need to dice the chip and prepare the facets crucially. In PLATON, grating couplers have to be designed to couple TM mode into and out of the SOI waveguides.

5.2 Design and Simulation

Recent simulations performed at IZM came up with a grating coupler layout capable of coupling losses less than -3dB for 1550nm in TM configuration. The layout has been optimized for a simple integration scheme which is in the focus of PLATON since all components are integrated into one chip finally. The methodology used here is described in Deliverable 2.2. More details on geometry and performance of the TM grating coupler are given in the annex.

In order to optimize the grating coupler structure for TM polarization, 3 different approaches or structures were considered, namely:

- **shallow etched grating**, with etch depths initially supposed to be smaller than one third of the total Si core height (=340 nm).
- **fully etched grating** with an etch depth of 290 nm. This etch depth was not equal to the whole Si core height due to fabrication tolerances, which would not allow to totally etch the Si layer and leave a layer of 50 nm on top of the SiO_2.
- **fully etched grating** with an etch depth of 290 nm as well. In this case, a variation of the filling factor (ratio between the tooth width and the total period) of the grating was performed to improve the coupling.

A series of simulations was performed for every structure in order to compare their performance characteristics and choose the best one.

Shallow etched structure

A parameter scan was performed for the period, the etching depth and the incidence angle, showing an optimal coupling of about -3 dB (0.49857) for the following values:

Period = 0.8 µm, Etch depth = 0.17 µm and Angle = 10°

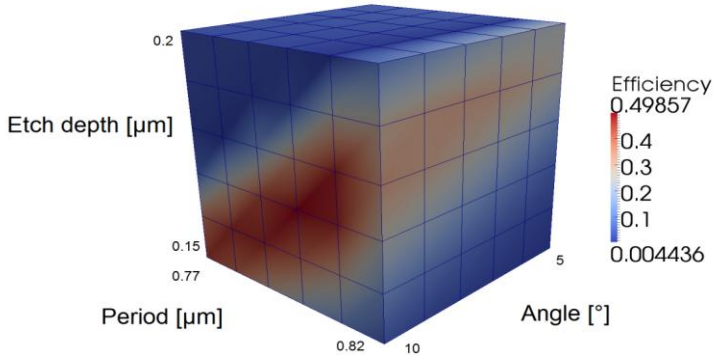


Figure 5.1: Shallow etched grating parameter scan.

The etching depth that was taken is bigger than the initial supposition of 1/3 of the Si core height, because the coupling values in this range were not as good. This structure offers good theoretical performance, but due to simplified fabrication processes, a fully etched structure was also investigated.

Fully etched structure without filling factor

A grating coupler with an etching depth of 290 nm was simulated and its optimal period for an angle of 9° was found to be 0.9 μm. The theoretical coupling efficiency was around -3 dB at the central wavelength. The spectral response of this optimized structure was found as well, having a -3dB bandwidth of almost 60 nm.

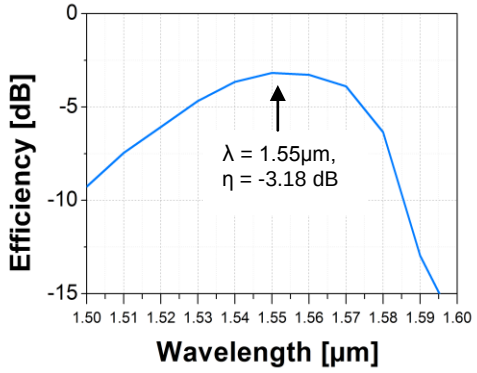


Figure 5.2: Simulated spectral response of the fully etched grating coupler without filling factor.

The designed structure was fabricated at the AMO facilities and the preliminary characterization showed an efficiency of -7.5 dB for an angle of 5°. The angle measurements were limited to this angle due to the set-up at the laboratory.

Fully etched structure with filling factor

In this case the optimal period is 0.7 μm for a filling factor of 0.8 (equivalent to a gap width of 0.14 μm) and an incidence angle of 10°. The coupling efficiency at the central wavelength is -2.68 dB. The following figure shows the simulated spectral response of the structure, which has a bandwidth of around 55 nm.

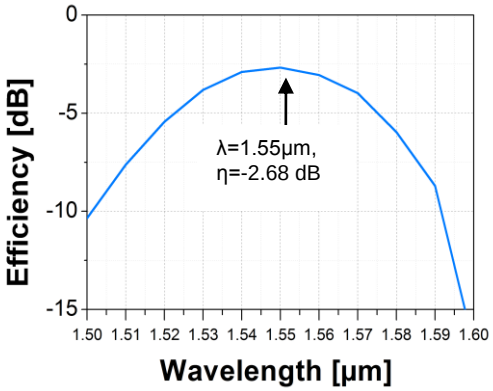


Figure 5.3: Simulated spectral response of the fully etched grating coupler with filling factor.

This structure was fabricated and characterized at the AMO facilities as well, and a measured coupling efficiency of around -5 dB was obtained for an angle of 10°. These results show a good agreement with the theoretical ones.

Conclusion

Based on the results presented above, the fully etched structure with filling factor variation has been selected for implementation in the mask.

5.3 Fabrication

Figure 5.4 shows a SEM image of PLATON's first TM grating coupler. The grating couplers are fabricated on the same layer used for the photonic waveguides.

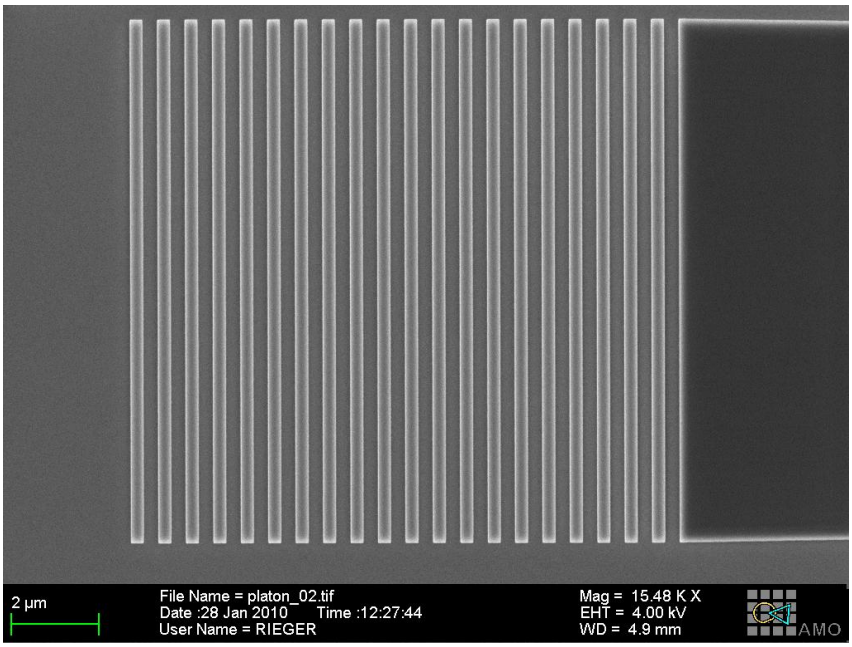


Figure 5.4: TM grating couplers designed by IZM and fabricated by AMO.

Grating couplers are very sensitive to even small variation in critical dimension (CD). Here significant effort to improve the CD control has been undertaken in the German national project MISTRAL. In this project 220 nm thick waveguides and TE grating couplers have been investigated. These results can be directly transferred to PLATON´s 340 nm thick SOI platform for TM, since grating coupler gaps are in the same geometrical range.

During the definition of the grating couplers by EBL, the proximity effect can cause variation in CD and therefore can lead to large variations in the coupling performance. The accidental deviation of the gap widths at different positions has been investigated using a dedicated automated SEM analysis tool [2]. CD deviations in the gap widths of about ~3 nm as shown in Figure 5.5 (hollow circles) have been found. This translates into a significant measurement error when using the cut-back method which requires highly reproducible coupling efficiencies. The effect of strong variations is demonstrated in Figure 5.6 (hollow circles), where optical transmission losses of waveguides fabricated without proximity effect correction (PEC) are plotted against the respective waveguide lengths. The error bar for the linear optical losses extracted from this plot is ±1.95 dB/cm. This value demonstrates a non-reproducible coupling efficiency when grating couplers are fabricated without PEC.

When PEC is used for EBL, variations are significantly reduced [3]. Using this technique the CD deviations within each block have been reduced to less than 2 nm, (see Fig. 5.5, full squares). This directly leads to a reduction of the measurement error by a factor of four to less than ±0.5 dB/cm (see Fig. 5.6, full squares). Devices fabricated using this technique show a uniform coupling efficiency for all couplers and are therefore well-suited for all applications that require stable fiber-to-chip coupling.

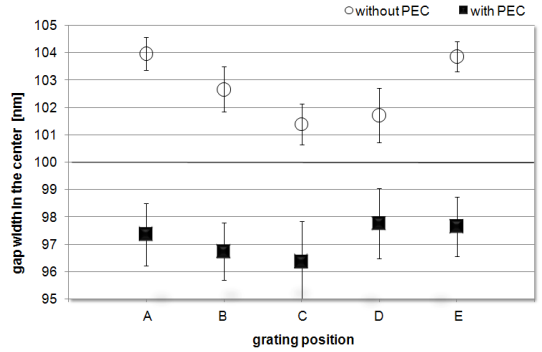


Figure 5.5: Measured gap width of grating couplers for TE at a wavelength of λ=1310nm at different grating positions without and with PEC.

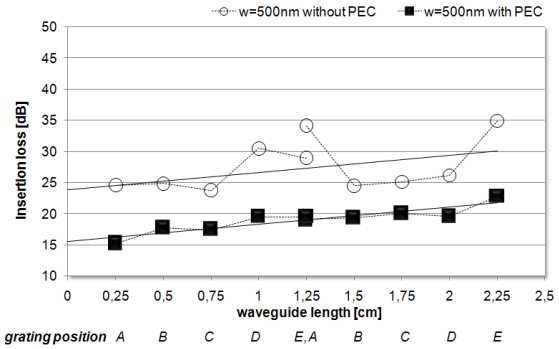


Figure 5.6: Measured optical TE loss of 500nm wide Si strip waveguides at λ=1310nm, with and without PEC.

5.4 Characterization

5.4.1 Experimental setup

The experimental setup that was used for the characterization process is depicted in Figure 5.7(a). A tunable Continuous Wave (CW) laser with a tuning range of 1500 to 1580 nm was used as input signal into the SOI chip via a polarization controller, ensuring TM polarization state of the propagating light. The output of the chip was split, using a 50:50 coupler, and monitored on both an Optical Spectrum Analyzer and an Optical Power Meter. Spectral response as well as coupling loss measurements were performed by scanning along the tuning range of the CW laser while monitoring the power level of the chip's output. A zoomed mask of the cutback sections included in the SOI chip is presented in Figure 5.7(b).

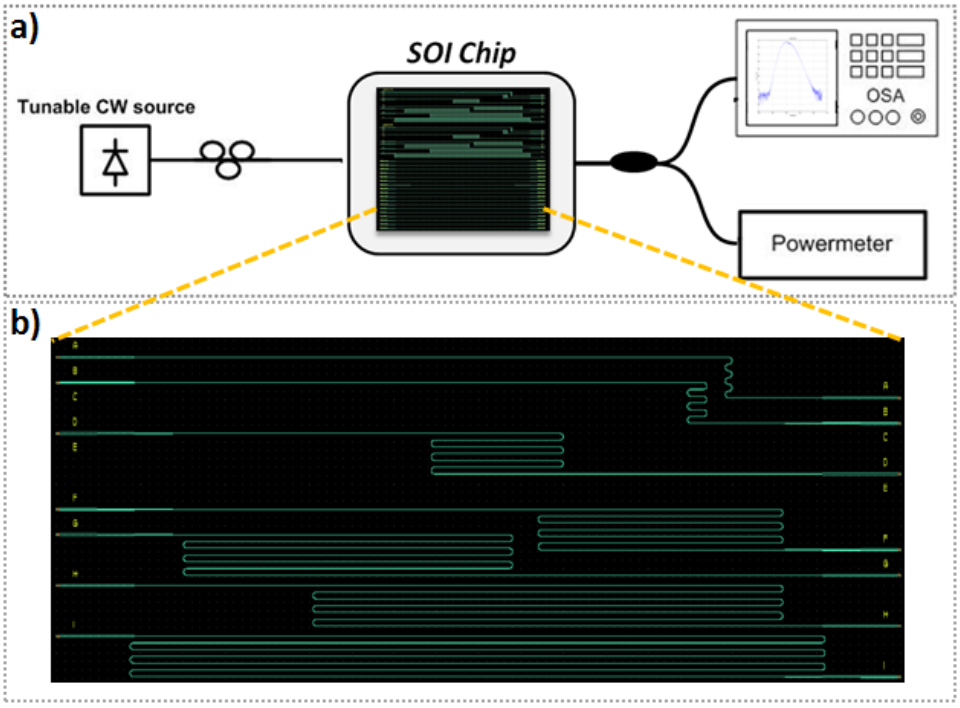


Figure 5.7: a) Experimental setup, b) Cutback sections in SOI chip.

5.4.2 Measurements results for Si TM grating couplers

The initial step of the characterization process was the assessment of the coupling efficiency of the Λ=700nm period grating coupler with respect to the angle of the incident beam. For this purpose, the CW laser source was replaced by an Erbium Doped Fiber Amplifier (EDFA), which served as a broad Amplified Spontaneous Emission (ASE) noise source, and fiber-to-fiber losses measurements of the 070_014 straight Si waveguide were performed for incident beam angle varying from 5 to 15 degrees with 2 degrees step. Figure 5.8 shows the coupling losses plotted against the incident beam angle and normalized to the lower loss value. The graph reveals optimum coupling at 10^0 degrees with less than 3dB output power variation across the total angle range.
Following this result, the incident beam angle was fixed at 10 degrees, in order to optimize the characterization process.

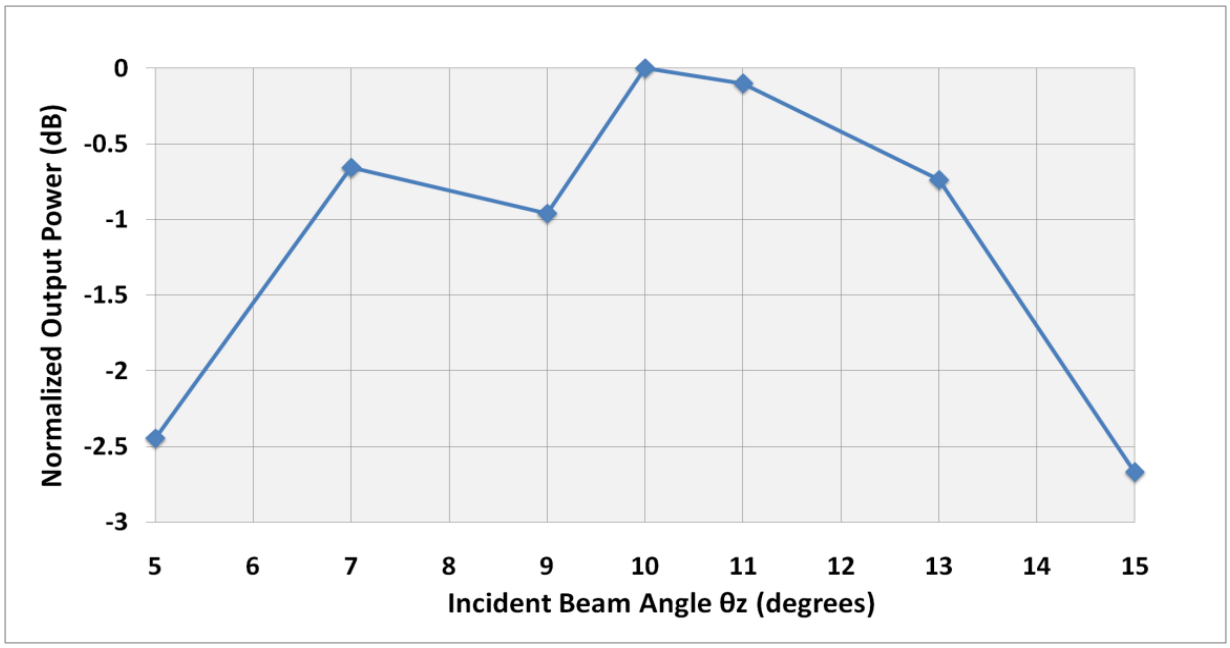


Figure 5.8: Normalized output power of the 700nm period grating coupler with respect to the angle of the incident beam.

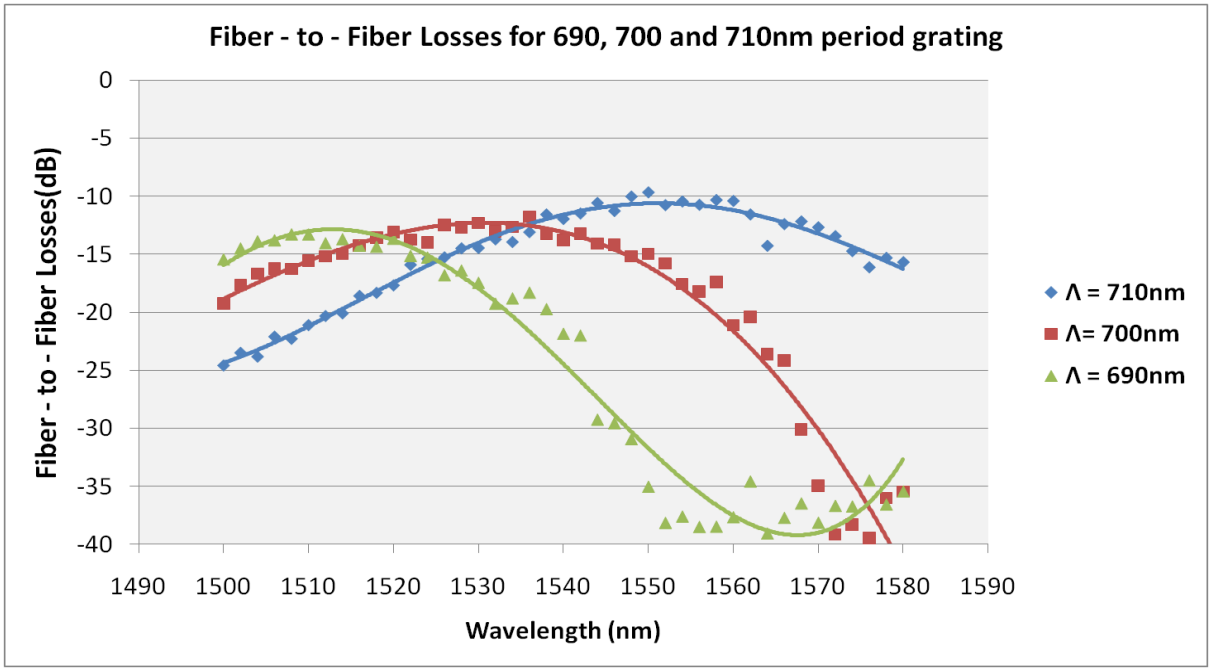


Figure 5.9: Spectral dependence of the fiber-to-fiber losses of the straight Si waveguides equipped with 690,700 and 710nm period grating couplers.

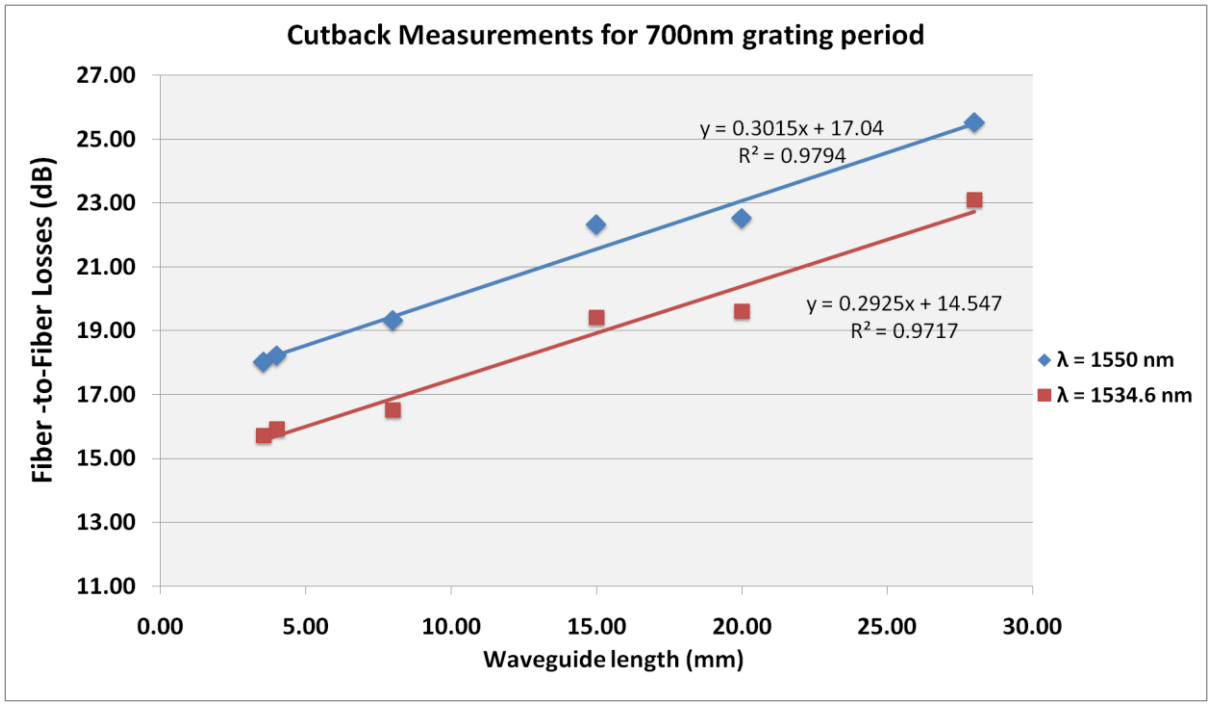


Figure 5.10: Cutback measurements for the 700nm period grating coupler at 1550nm and 1534.6nm center wavelength.

The spectral response of the structures was measured by tuning the CW laser from 1500 to 1580nm with 2nm step and measuring the fiber-to-fiber losses of three straight waveguides equipped with 690, 700 and 710nm grating couplers. The transfer function of

each waveguide, and therefore of each grating coupler type, was reconstructed by plotting the measured losses against the wavelength, as it is shown in Figure 5.9. It is evident that the transfer function of the grating coupler is shifting to longer wavelengths as the period of the grating increases. Moreover, the 710nm period grating exhibits adequate coupling performance of ~ 5dB per coupler at 1550nm, consisting therefore the most promising design.

Coupling and propagation losses were measured utilizing a cutback section consisting of seven waveguide samples of various lengths. Since the cutback waveguides were equipped with 700nm period gratings, the center wavelength of the CW was initially set to 1534.6nm so as to ensure optimum coupling losses, according to Figure 5.9. However, cutback measurements were also taken at 1550nm center wavelength for reference purposes. Figure 5.10 shows the measured fiber-to-fiber losses plotted against the waveguide length. Linear fitting revealed coupling losses of 17.04dB at 1550 nm and 14.5dB at 1534.6nm, while the propagation losses were found to be approximately 3.0dB/cm in both cases. Previous measurements, though, performed on similar cutback waveguides, have shown that the coupling losses are overestimated owing to the increased propagation losses taking place in the semicircle parts of the silicon waveguides. Therefore, in order to estimate the coupling losses of the grating couplers without taking into account the additional bending losses, the propagation losses corresponding to the 0.33cm long straight Si waveguide were calculated, according to the 3dB/cm given by the cutback measurements, and subtracted from the measured fiber-to-fiber losses shown in Figure 5.9. Table 5.11 summarizes the fiber-to-fiber as well as the calculated coupling losses of the grating coupler structures at the spectral region around 1550nm. In the case of 690 and 700nm, the losses corresponding to 1510.198nm and 1534.6nm wavelength, respectively, are also shown.

It is clearly demonstrated that the TM grating couplers, fabricated according to the fully etched design provided by IZM, present low coupling loss for all the three different grating periods. Furthermore, 710nm grating period seems to meet PLATON requirements for low coupling loss in the spectral region around 1550nm.

Structure ID	Si grating period (nm)	Si rib waveguide length (cm)	Fiber-to-fiber losses (dB)	Coupling efficiency-losses per coupler (dB)	Wavelength (nm)
070_014	700	0.336	13.82	6.36	1550.043
070_014	700	0.336	11.44	5.18	1534.601
071_013	710	0.336	9.91	4.42	1550.025
069_014	690	0.336	25.92	12.41	1549.237
069_014	690	0.336	12.92	5.43	1510.198

Table 5.11: Fiber-to-fiber and coupling losses of the fabricated grating couplers.

6 Optical 7:1 MUX circuitry

6.1 Introduction

The front end of PLATON's router is an optical multiplexing circuitry comprising cascaded 2nd order SOI waveguide ring resonators (WRRs) that enable the multiplexing of 100 GHz spaced 40 Gb/s channels into a common waveguide, according to the requirements that were described in D2.4. The generic 8:1 SOI MUX design employs two different radii clusters (R_1 and R_2), with each cluster having four 2nd order thermo-optically tunable ring structures of the same radius (see Fig. 6.1). This configuration meets AMO's fabrication limit to single lines (50nm in resist) and can perform successfully for a thermo-optically induced wavelength tuning of less than 3 nm (see D2.2). Besides, it can fulfill PLATON's signal specifications, namely the 100 GHz channel (resonance) spacing and the 0.32 nm (40 GHz) 3-dB bandwidth of each resonant peak.

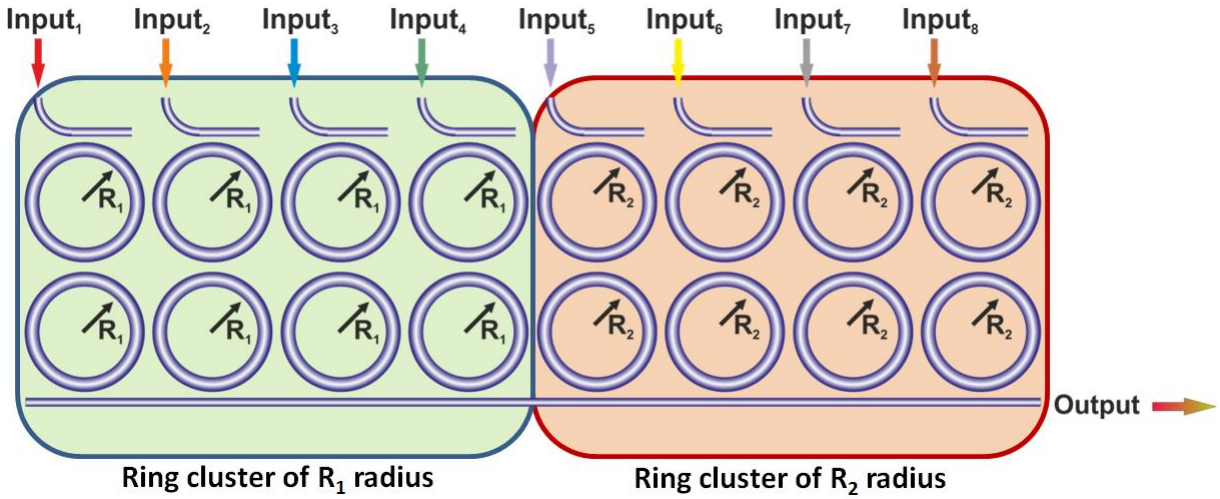


Figure 6.1: 8 cascaded 2nd order WRR consisted of two different radii clusters.

6.2 Fabrication

Figure 6.2 depicts the cross-sectional view of the fabricated MUX structures. First the SOI layer has been patterned according to the description in chapter 4. With these processing steps all passive components like waveguides, grating couplers and ring resonators have been fabricated. Even though the CD control is very accurate (see chapter 5), tiny deviations can have significant effect on the resonance frequency of each ring resonator. As these small deviations cannot be avoided during fabrication, adequate possibilities for trimming and tuning are needed in the final devices. For this reason, metal heating elements will be integrated on top of each ring.

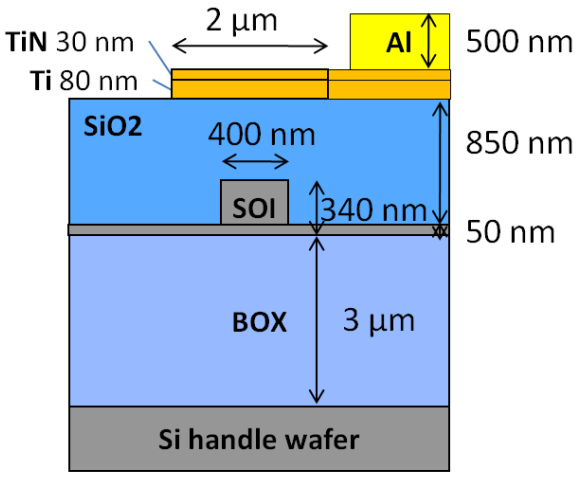


Figure 6.2: Cross-sectional view of a 1st order WRR with micro-heaters.

After patterning the SOI structures (see chapter 4) the whole substrate is spin-coated by a 850 nm thick dielectric Spin-On-Glass (SOG). This material is very similar to SiO_2 after curing, is easy to process, and is able to fill the tiny gaps in the grating couplers without any bubbles, so-called voids. In the next step, a titanium/ titanium nitride sandwich is deposited and patterned to form the heating electrode on top of the SOI waveguides and ring resonators. Titanium is a very stable metal and serves as efficient heater. The titanium nitride serves as diffusion barrier to avoid a reaction between the titanium and the following aluminum interconnect.

The first SOI MUX devices capable of 1:1, 2:1 and 4:1 multiplexing have been fabricated. In particular, AMO fabricated a batch consisting of 3 wafers each with dies (i.e., chips after dicing the wafer) using different types of Proximity Effect Correction (PEC) for EBL, namely PEC32 and PEC08. One of 3 wafers was taken out of the process flow before putting the microheaters on top of the sensitive microrings. From this wafer two chips have been diced out (one exposed with PEC08 and the other one with PEC32). Both chips were delivered directly to NTUA for preliminary characterization without microheaters. For these chips only 1:1 MUX structures with 5.4 μm, 9 μm, 12 μm and 14.85 μm ring radii could be evaluated in terms of resonant peaks' shape and wavelength, free spectral range (FSR) and 3-dB bandwidth. The specifications of the fabricated multiplexing structures are summarized in Table 6.5.

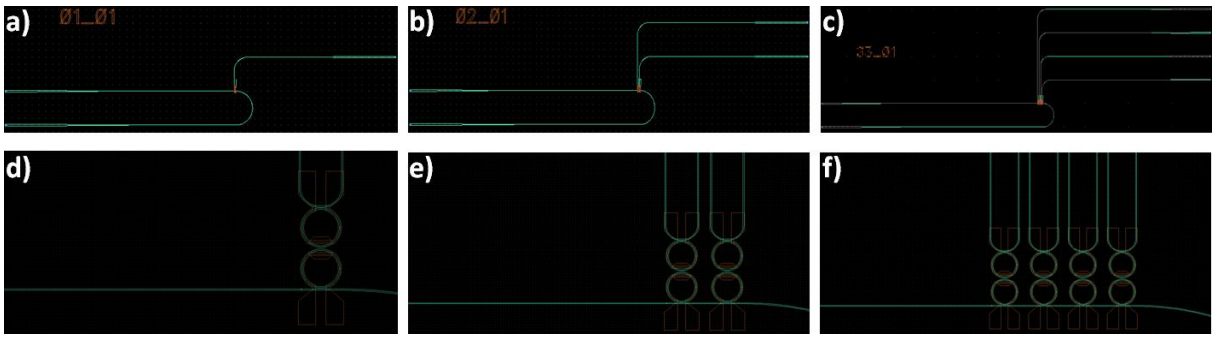


Figure 6.3: Mask layouts of a a) 1:1, b) 2:1, c) 4:1 multiplexing structure and the respective zoomed views (d-f).

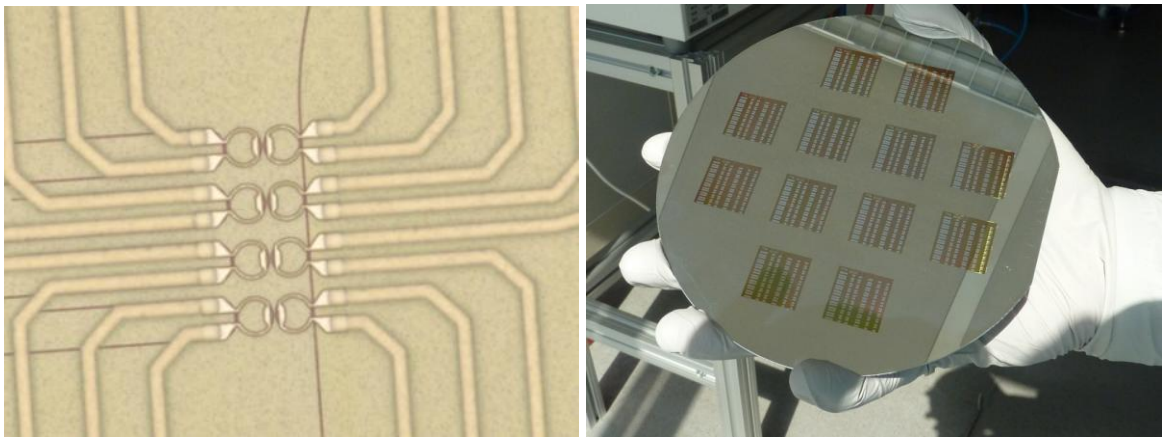


Figure 6.4: Images of the multiplexing circuitry: left: 4:1 MUX device with heaters and interconnects, right: photograph of a full 6-inch wafer containing hundreds of MUX circuits for testing purposes.

Parameter / MUX device (μm)	Ring radius (R)	Bus-to-ring (B2R) gaps (gap_1)	Ring-to-ring (R2R) gaps (gap_2)
1:1	5.4	0.19, 0.2, 0.21	0.44, 0.46, 0.48
	9	0.19, 0.2, 0.21	0.36, 0.38, 0.4
	12	0.16, 0.17, 0.18	0.28, 0.3, 0.32
	14.85	0.165, 0.17, 0.175	0.26, 0.28, 0.3
2:1	5.4	0.19, 0.2, 0.21	0.44, 0.46, 0.48
4:1	5.4	0.19, 0.2, 0.21	0.44, 0.46, 0.48

Table 6.5: Specifications of fabricated SOI MUX devices.

6.3 Static Characterization

NTUA characterized both PEC32- and PEC08-exposed chips. Since these chips have not been equipped with microheaters, preliminary characterization was carried out for all 1:1 ring structures of first chip (PEC32). The 1:1 9μm-ring devices of the other chip (PEC08) were also characterized in order to have a comparative study of the two types of PEC. Considering all possible combinations of the gaps for each radius (see Table 6.5), 45 devices were characterized in total (36 structures correspond to PEC32 chip and the remaining 9 belong to PEC08 chip).

Figure 6.6 (a, b) depicts the representative spectra of four 1:1 fabricated ring structures with 5.4 μm, 9 μm, 12 μm and 14.85 μm radii, respectively. Within the 1530-1560 nm region, two resonant peaks at 1534.1 nm and 1549.5 nm arise from the 5.4μm-radius structure, resulting in 15.4 nm FSR (Fig. 6.6(a)). At the same spectral window, three peaks (1534.2 nm, 1543.4 nm, 1552.7 nm) are observed for the 9μm-radius device that features now a FSR of ~9.25 nm. Regarding the 2^{nd} order ring of 12 μm radius, 4 resonances (1534 nm, 1540.7 nm, 1547.6 nm, 1554.7 nm) are present in the 1530-1560 nm band and the respective FSR value is ~6.9 nm (Fig. 6.6(b)). As concerns the ring structure with 14.85 μm radius, six resonant peaks (1531.9 nm, 1537.2 nm, 1543.1 nm, 1548.4 nm, 1554.4 nm, 1559.8 nm) are appeared within the same spectral band, leading to ~5.6 nm FSR.

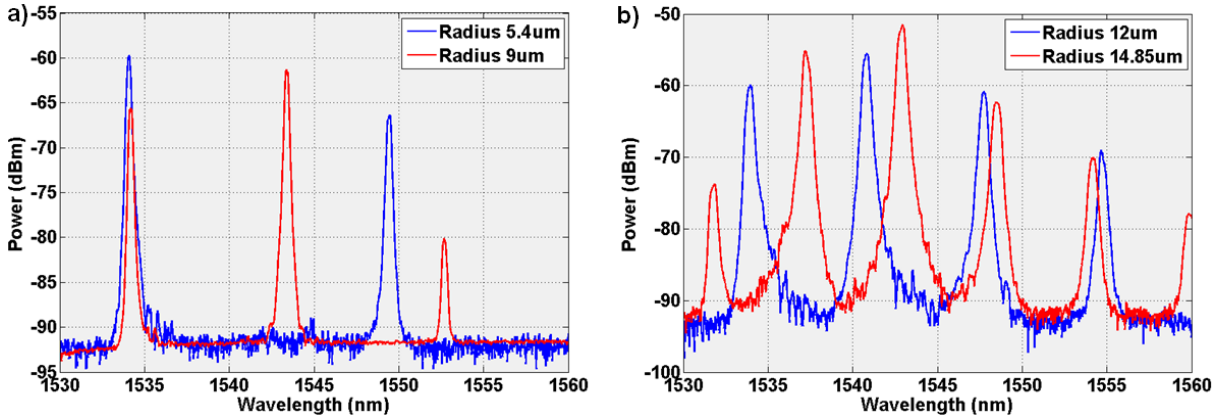


Figure 6.6: Spectra of 1:1 fabricated devices with a) 5.4 μm and 9 μm, b) 12 μm and 14.85 μm ring radii.

Figure 6.7(a) illustrates the wavelengths of resonances that appear within the 1530-1537 nm range and correspond to the 1:1 ring structures of PEC32-exposed chip. For each radius the resonances tend to shift to longer wavelengths as the gap values are getting larger. This trend is shown by the dashed line on the same figure. On the contrary, no such trend with respect to gap size increase is observed for the 9μm-radius ring devices that are included in the other chip (Fig. 6.7(b)). Consequently, the type of PEC for EBL seems to affect (in terms of wavelength shifting) the WRRs' spectral responses.

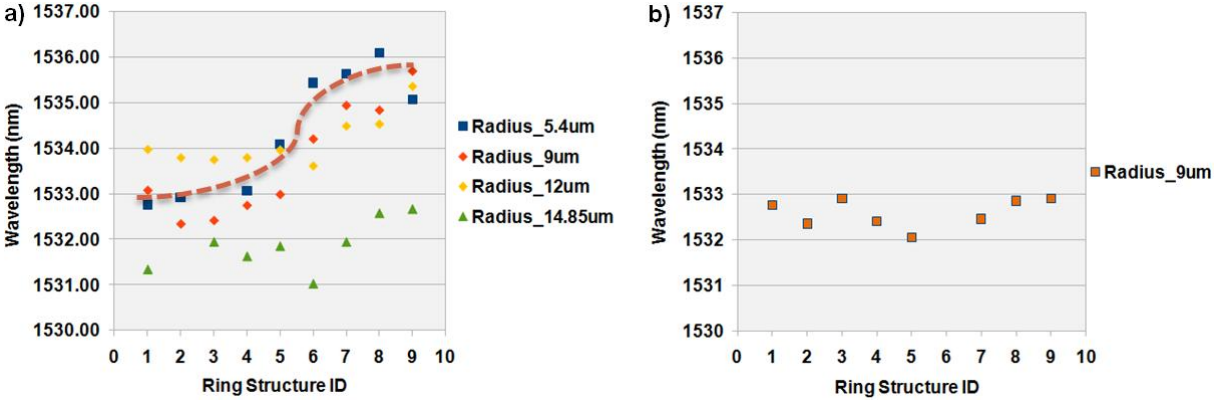


Figure 6.7: Wavelengths of resonant peaks around 1533 nm for the fabricated ring structures with a) 5.4 μm, 9 μm, 12 μm and 14.85 μm (PEC32), b) 9 μm (PEC08) radii.

The reproducibility of the characterized devices has been checked by calculating the mean of standard deviation of the resonances' wavelengths in 1530-1560 nm for each ring radius. As depicted in Figure 6.8(a), regarding the PEC32 chip, standard deviation decreases for large radii, exhibiting a range from 1.47 nm to 0.51 nm. Compared with the respective value (1.28 nm) for 9 μm ring radius, PEC08 chip reveals lower standard deviation (0.73 nm). Figure 6.8(b) presents the 3-dB bandwidth of representative ring structures for both chips. The dashed line marks the 40 GHz threshold that is required for 40 Gb/s data transmission. Therefore, the ring devices with 12 μm and 14.85 μm radii from PEC32 chip and some others with 9 μm radii from PEC08 chip are suitable for the required line rates. These structures result in 3-dB bandwidth values of their resonant peaks that ranges from 40 GHz to 70 GHz. Table 6.9 summarizes the mean values of resonances' standard deviation and FSR for each ring radius on both chips.

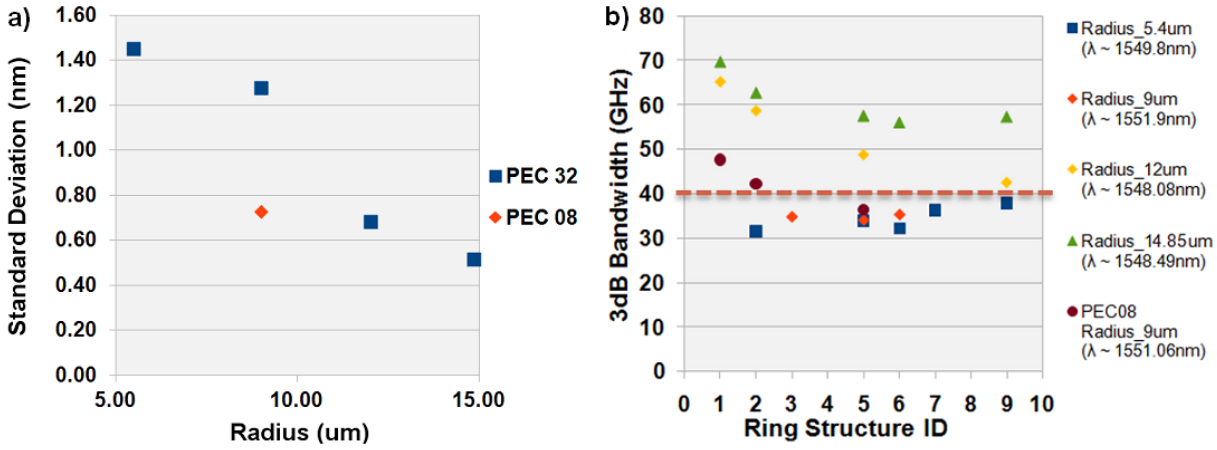


Figure 6.8: a) Resonances' standard deviation and b) 3-dB bandwidth of the characterized ring structures.

PEC	Ring radius R (μm)	Resonances' standard deviation (nm)	FSR (nm)
32	5.4	1.47	15.35
	9	1.28	9.21
	12	0.68	6.91
	14.85	0.51	5.79
08	9	0.73	9.22

Table 6.9: Characterization of the fabricated ring structures in terms of resonance's standard deviation and FSR.

The characterization without heaters revealed that the 5.4 μm-radius structures cannot be utilized to support the required data traffic format due to their narrow resonant peaks. The structures with 14.85 μm radius were also rejected since they exhibited too small FSR values (5.6 nm) prohibiting the multiplexing of 8 wavelengths at 100 GHz spacing (requiring 6.4 nm). On the contrary, MUX circuits with 9 μm and 12 μm radii appeared to comfort with PLATON's signal specifications. In particular, S05_02 (PEC08) and S09_05 (PEC32) structures led to the most promising results. The first structure refers to a 2nd order ring with 9 μm radius (R), 190 nm gap for the bus-to-ring (B2R) parts (gap_1) and 380 nm for the ring-to-ring (R2R) part (gap_2). The values of the respective quantities for the other structure are R=12 μm, gap_1=170 nm and gap_2=300 nm.

6.4 Thermo-optic Characterization

Following the static characterization, the SOI MUX structures were also evaluated in terms of their thermo-optic tuning properties. For this purpose a third SOI MUX chip, equipped with microheaters and electrical contact pads was delivered to ICCS/NTUA premises for testing. During the characterization process a broad ASE signal was used as input into the chip while a variable DC voltage was applied to the contact pads using a precision power supply. The DC voltage was applied only to the lower ring of each dual ring structure allowing for, simultaneously, testing the thermo-optic tuning properties of the individual ring while evaluating the thermal crosstalk between the cascaded rings. Step-by-step voltage measurements were performed with the output of the chip being monitored on an Optical Spectrum Analyzer. Figure 6.10 summarizes some preliminary results obtained during the characterization of the 1x1 SOI MUX structures incorporated in the chip.

The thermo-optic tuning of structure 01_05 is depicted in Figure 6.10(a) revealing 4.05nm tuning for 8.6mW supplied power, while 3.2nm tuning was achieved for 05_04 structure with 13.8mW power, as shown in Figure 6.10(b). Less efficient tuning was obtained for larger radii with 09_04 structure exhibiting 2.52nm for 15.2mW power (Fig. 6.10(c)) and 13_04 structure 3.12nm for 17.3mW respectively (Fig. 6.10(d)). Furthermore, in Figure 6.10(b-d) the resonance corresponding to the second ring, that is not heated, is also shown. Apparently, this resonance is also slightly shifting to longer wavelengths when current is injected into the adjacent ring, indicating the existence of thermal crosstalk between the cascaded rings of the dual ring structure.

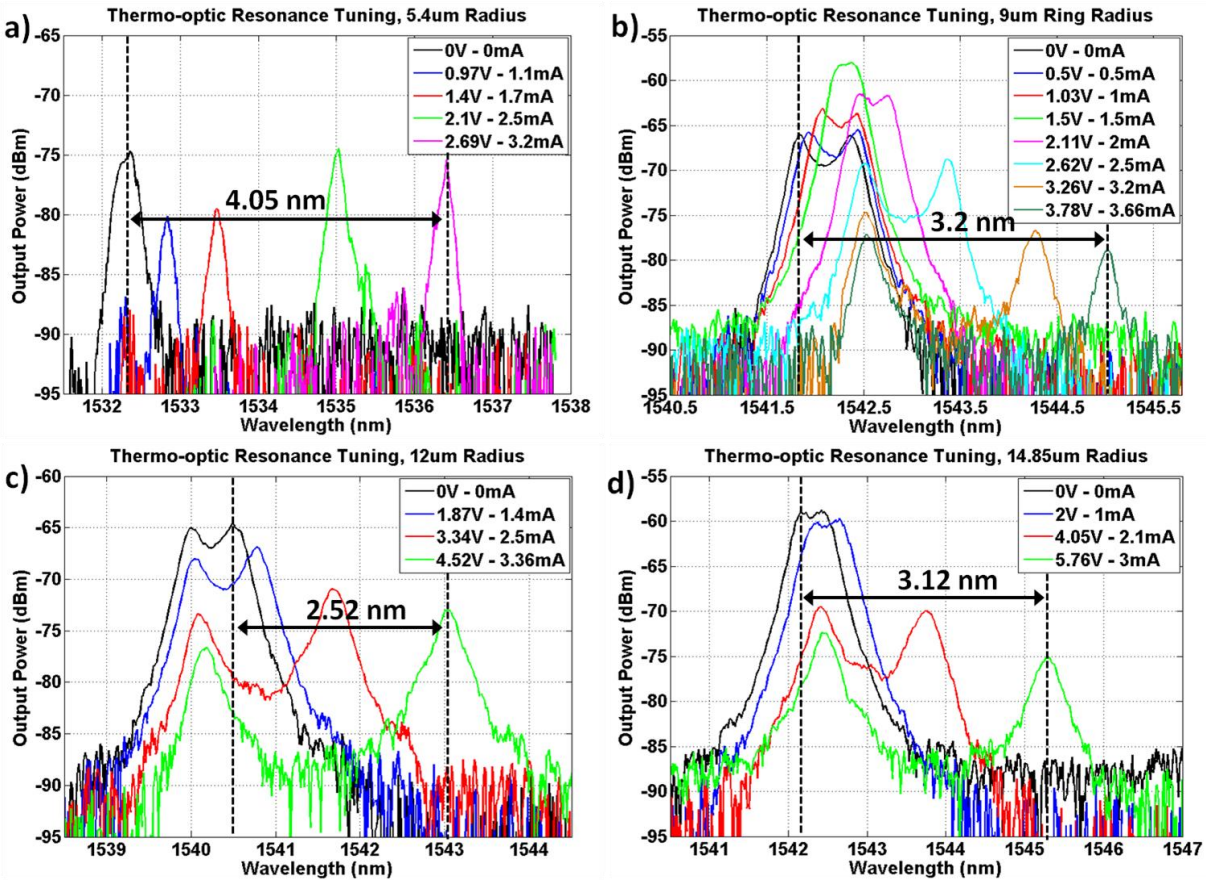


Figure 6.10: Thermo-optic tuning of dual ring structure a) 01_05 with 5.4um radius, b) 05_04 with 9um radius, c) 09_05 with 12um radius and d) 13_04 with 14.85um radius.

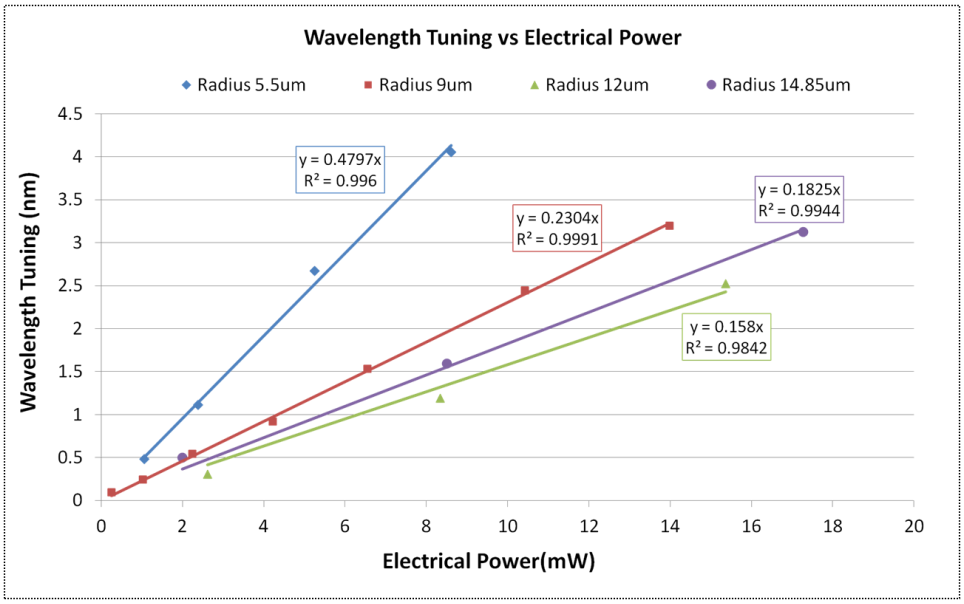


Figure 6.11: Wavelength tuning plotted against the required electrical power.

However this resonance shift was found to be at least 13 times lower than the first one, even in worst case, implying nearly negligible effect of the crosstalk. Furthermore, the absolute maximum current was found to be 4mA, since above this threshold the heating element was rapidly degrading.

Figure 6.11 presents the wavelength tuning plotted against the supplied electrical power for each one of the aforementioned dual ring structures. The tuning sensitivity can be extracted by performing linear regression on each data series and calculating the slope of the respective fitting lines, as shown in the figure. The outcome of the fitting process (blue markers) as well as the total measured resistance (red markers) of each structure are depicted in Figure 6.12. It is clear that the tuning sensitivity decreases as the radius of the ring increases whilst the opposite, as expected, stands for the resistance of the heater.

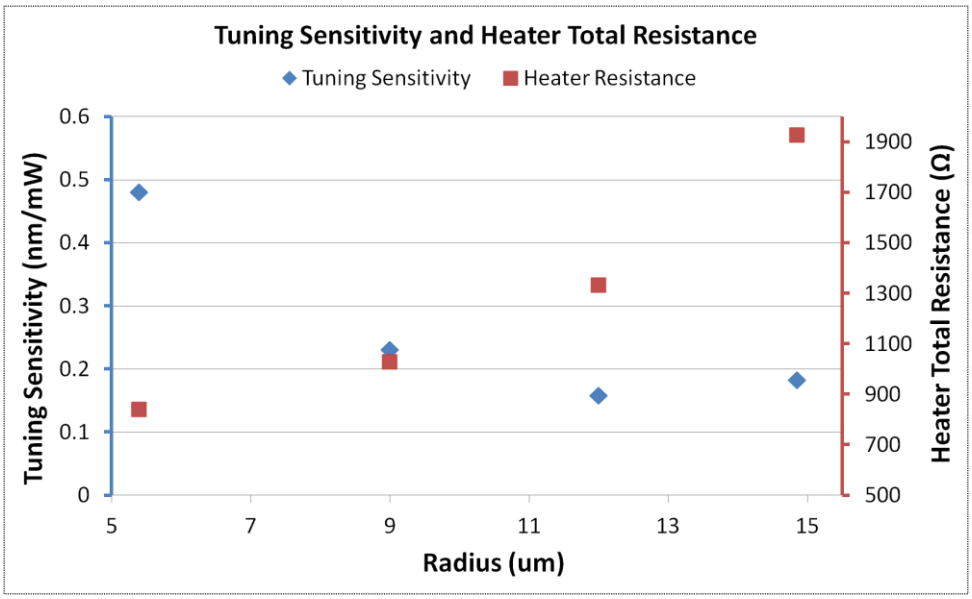


Figure 6.12: Tuning sensitivity (left vertical axis) and Heater Total Resistance (right vertical axis) plotted against the ring radius of the structure.

6.5 Final designs

The experimental outcomes of the preliminary characterization described in section 6.3 can be reproduced satisfactorily by our developed simulation tool (see D2.2). The simulation parameters that determine the spectral response of a 2nd order ring structure are listed in Table 6.13. Since the ring radii and the SOI propagation losses are fixed (see Table 6.13), the remaining parameters namely the refractive index and the power coupling coefficients had to be adjusted for optimal matching. Matching the resonant peaks with respect to FSR was achieved by using a group refractive index value of ~4.55 [4,5]. The power coupling coefficients related to the bus-to-ring and ring-to-ring waveguides were also altered appropriately to fit the shape and 3-dB bandwidth of the experimental resonances.

Ring radii (R)	Refractive index (n_{gr})	Losses (a)	B2R power coupling coefficient (C_a)	R2R power coupling coefficient (C_b)
5.4 μm 9 μm 12 μm 14.85 μm	~4.55	3 dB/cm	Varying between 0 and 1	Varying between 0 and 1

Table 6.13: Simulation parameters.

Figure 6.14(a) shows the transmission spectrum of the 9μm-radius S05_02 (PEC08) structure in comparison with that derived from the simulation after the matching process. Blue line represents the experimental results whereas the red one corresponds to the simulation. The FSR is easily perceivable within C band and equals 9.3 nm in both cases. Nevertheless, misalignments are observed regarding the power levels of the resonant peaks owing to the ASE gain profile of the employed EDFA. However, these deviations do not affect the reliability of the matching process as the shape of the resonant peaks is almost perfectly reproduced for more than 17 dB power region. The insertion losses of the simulation model were adjusted to fit the resonance at ~1551 nm. A more detailed view of this resonance that exhibits 0.34 nm 3-dB bandwidth is depicted in Figure 6.14(b). This resonant peak was reproduced by the simulation model of a 2nd order ring with R=9 μm, n_{gr}=4.5522, bus-to-ring power coupling coefficient (C_a) equal to 0.17 and ring-to-ring power coupling coefficient (C_b) equal to 0.007. Respective results are illustrated in Figure 6.15 for the 12μm-radius S09_05 (PEC32) structure. In this case the FSR and 3-dB bandwidth values are 6.9 nm and 0.39 nm, respectively. The resonant peak at ~1548 nm was matched by utilizing the simulation parameters R=12 μm, n_{gr}=4.5571, C_a=0.33 and C_b=0.01. Table 6.16 summarizes the specifications of the above structures and presents the selected simulation parameters for optimal matching in terms of FSR and 3-dB bandwidth.

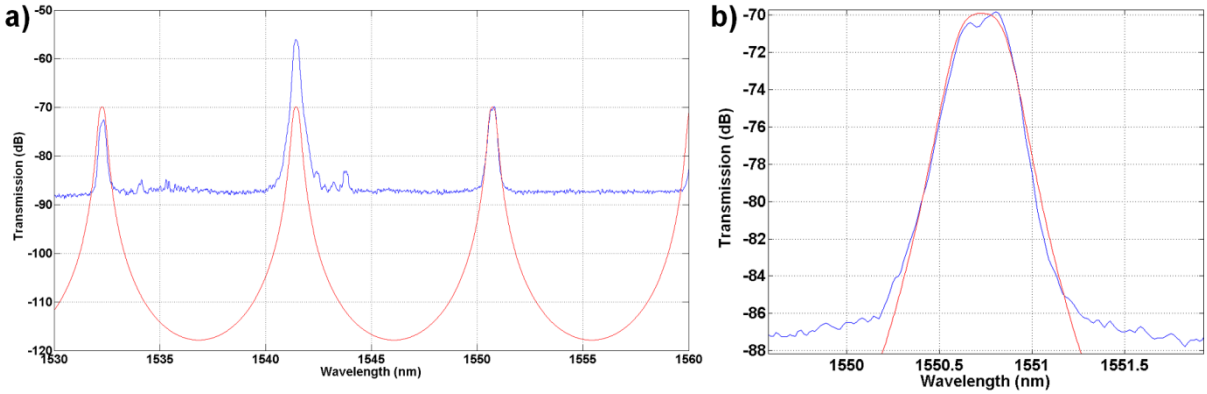


Figure 6.14: Experimental (blue) and simulation (red) transmission spectra of a 2nd order WRR with R=9 μm a) in a wavelength range of 30 nm and b) around 1551 nm.

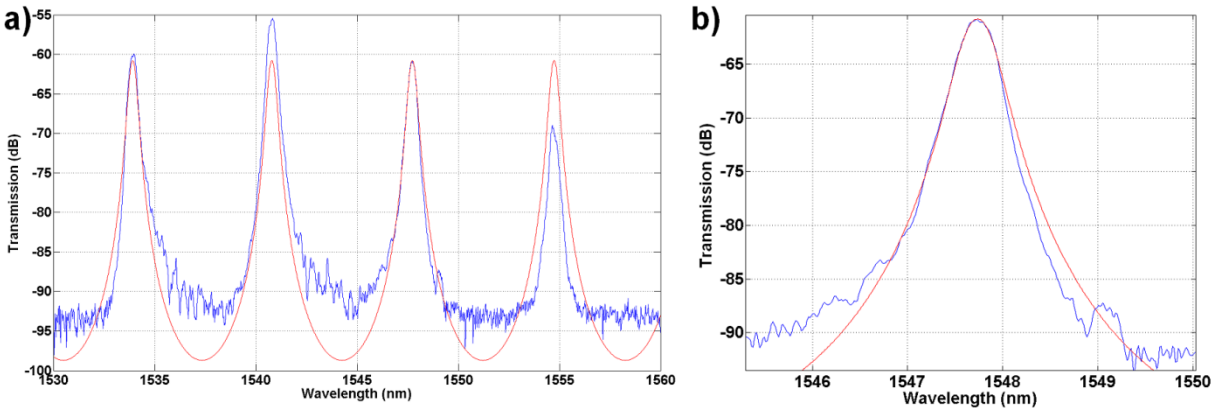


Figure 6.15: Experimental (blue) and simulation (red) transmission spectra of a 2nd order WRR with R=12 μm a) in a wavelength range of 30 nm and b) around 1548 nm.

Parameter / Ring Structure	Radius R	B2R gaps (gap_1)	R2R gap (gap_2)	B2R power coupling coefficient (C_a)	R2R power coupling coefficient (C_b)	n_{gr}	FSR	3-dB BW
S05_02 (PEC08)	9 μm	0.19 μm	0.38 μm	-	-		9.23 nm	0.34 nm
Model_1	9 μm	-	-	0.17	0.007	4.5522	9.23 nm	0.34 nm
S09_05 (PEC32)	12 μm	0.17 μm	0.3 μm	-	-		6.9 nm	0.39 nm
Model_2	12 μm	-	-	0.33	0.01	4.5571	6.9 nm	0.39 nm

Table 6.16: Specifications of the fabricated ring structures, simulation parameters of their models and the matching results.

PLATON's MUXs have been redesigned for adoption in the final routing platform based on the experimental results obtained from the fabricated structures. Figure 6.17 presents the layouts of the 8:1 multiplexers where the first 4 cascaded rings have larger ($R_1>R_2$) (Fig. 6.17(a)) or smaller ($R_1<R_2$) (Fig. 6.17(b)) radius compared to the rest of them. This design meets the fabrication limit and the maximum variation of refractive index that can be induced by the permissible applied voltage.

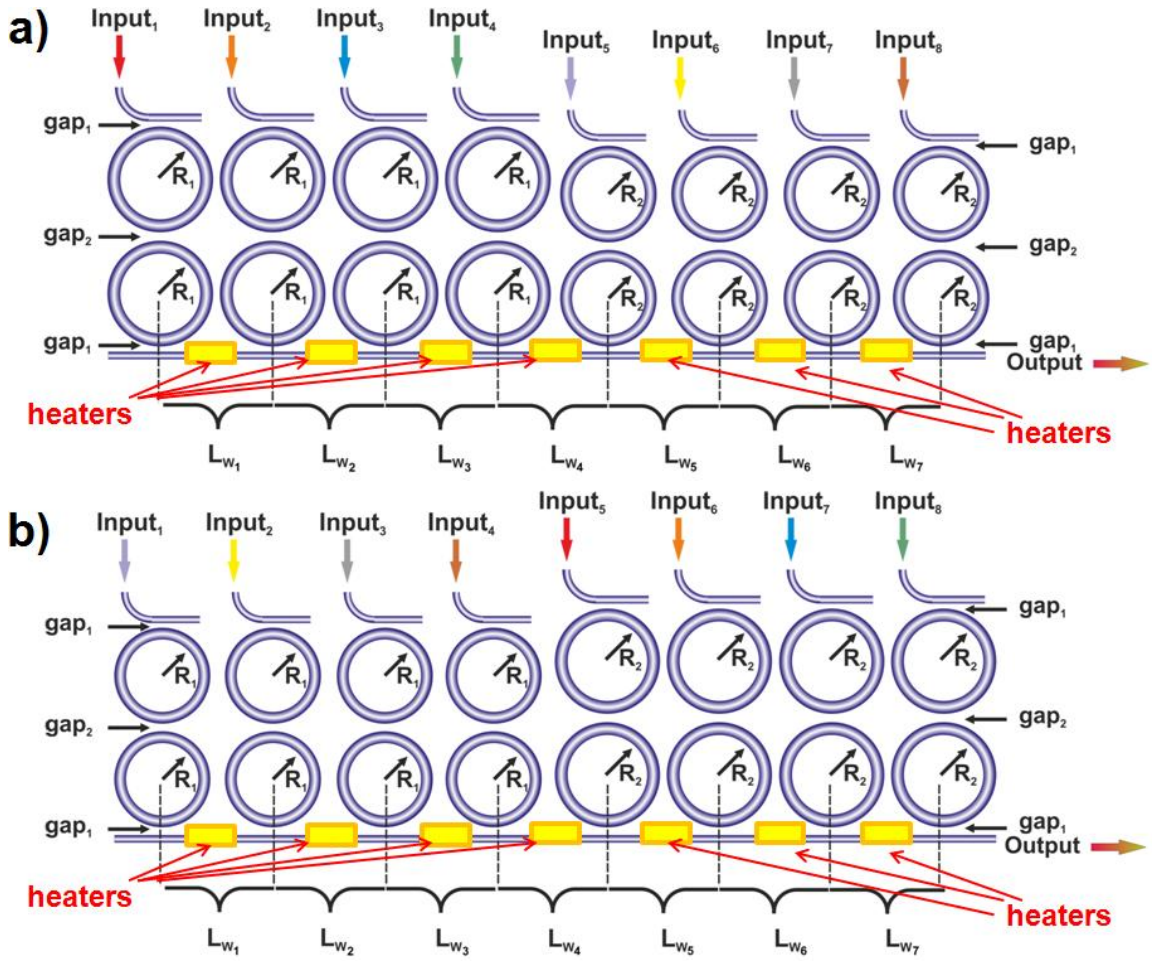


Figure 6.17: 8 cascaded 2nd order WRR with a) R_1=12 μm, R_2=11.7 μm, b) R_1=9 μm, R_2=9.2 μm.

Apart from 100 GHz channel spacing and at least 0.32 nm 3-dB bandwidth of each resonance, lower than -15 dB crosstalk for the adjacent resonant peaks of each multiplexer is required. During the design it was observed that the lengths (L_{Wi}) of the straight waveguides connecting successive 2nd order rings greatly affect the crosstalk between adjacent channels. Their slightest length alteration can lead to extremely low crosstalk values degrading the desirable multiplexing operation. To this end, heaters have to be included in the straight inter-ring waveguide sections. These sections should be long enough to prevent thermal crosstalk to the interconnected rings. The heaters will be placed in the middle of every straight waveguide, occupying 30x1 μm^2 area, as depicted in Figure 6.17.

The final 4x4 router also requires four different spectral bands within the 1530-1565 nm wavelength window. This specification can be satisfied by choosing different combinations for the ring radii and the straight waveguides. The first three designs are based on the 12

μm radius S09_05 (PEC32) layout of the already tested structures. These designs employ four 12 μm and four 11.7 μm radius rings as illustrated in Figure 6.17(a). The fourth design relies on the 9 μm radius S05_02 (PEC08) layout and comprises four rings with 9 μm and four rings with 9.2 μm radius, as shown in Figure 6.17(b). The exact values of the ring radii, gaps and straight waveguide sections for all MUX designs are presented in Table 6.18.

Parameter / MUX design (μm)	R_1	R_2	gap_1	gap_2	L_{w1}	L_{w2}	L_{w3}	L_{w4}	L_{w5}	L_{w6}	L_{w7}
1	12	11.7	0.17	0.3	123	118	112	105	104	100	95
2	12	11.7	0.17	0.3	108	106	102	120	116	112	109
3	12	11.7	0.17	0.3	101	99	96	93	107	105	102
4	9	9.2	0.19	0.38	104	102	100	104	99	97	95

Table 6.18: Final SOI MUX specifications.

Figure 6.19(a-d) depicts the transmission spectra corresponding to the four MUX designs. The crosstalk is at least -20 dB for the adjacent channels in all cases. The 3-dB bandwidth and the channel spacing are also in agreement with PLATON requirements. Moreover, multiplexers 1-4 operate in (1534-1540 nm), (1540-1547 nm), (1547-1554 nm) and (1557-1563 nm) regions, respectively. All these results are summarized in Table 6.20.

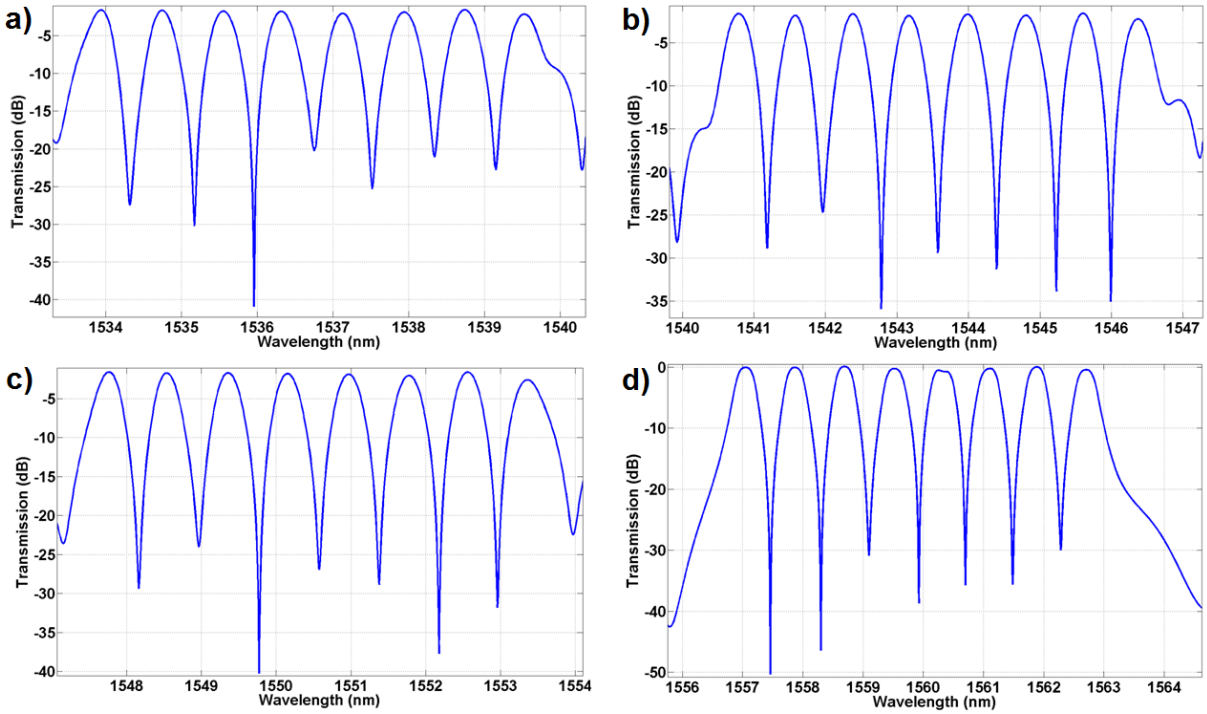


Figure 6.19: Spectral responses of the a) first (1534-1540 nm band), b) second (1540-1547 nm band), c) third (1547-1554 nm band) and d) fourth (1557-1563 nm band) 8:1 multiplexing designs.

Parameter / MUX design	Crosstalk	Channel spacing	3-dB bandwidth	Spectral band
1	<-20 dB	0.8 nm (100 GHz)	0.32 nm (40 GHz)	1534-1540 nm
2	<-25 dB	0.8 nm (100 GHz)	0.32 nm (40 GHz)	1540-1547 nm
3	<-24 dB	0.8 nm (100 GHz)	0.32 nm (40 GHz)	1547-1554 nm
4	<-30 dB	0.8 nm (100 GHz)	0.32 nm (40 GHz)	1557-1563 nm

Table 6.20: Simulated results of the final SOI MUX designs.

7 Monolithically integrated Photodiodes

7.1 Introduction, Design, Simulation

Silicon-based integrated photonic devices rely on the transparency of bulk silicon at wavelengths longer than 1.1 µm. On the contrary, this transparency for photon energies below the indirect electronic bandgap is a major drawback for conventional linear absorption based silicon photodetectors at telecommunication wavelength of 1.55 µm.

Germanium photodetectors have been initially targeted for employment as they provide adequate performance for the required optical interconnection routing platform, well beyond the requirements of PLATON's routing platforms, coming, however, at the expense of increased fabrication complexity.

As an alternative approach, an all-silicon concept based on micro ring resonators consisting of rib-waveguides with laterally incorporated p-i-n diodes has been developed by AMO within the European project "Circles of Light" and the results obtained during this activity have been evaluated by AMO with respect to the detector performance required within PLATON.

In this approach, the IR photogeneration in silicon is enhanced by linear absorption at midgap energy states introduced by silicon ion implantation. This approach is expected to significantly reduce the fabrication costs compared to hybrid detector concepts. Si^+-implanted photodetectors appear to provide the performance required within PLATON whilst keeping the overall integration complexity relatively low.

Defect states inside silicon are known for a long time to generate significant absorption in the infrared wavelength region. One prominent example for such a defect state is the silicon divacancy [6].

In PLATON, the role of the photodiode is to detect the header signal. As reported in D2.4 the duration of the header pulses are in the range of 333-500 ns which corresponds to a minimum photodetector bandwidth speed of 2 Mb/s.

7.2 Fabrication

In our experiments we have followed the recently reported way of Si^+-ion implantation to generate defect states inside silicon [7]. This generation of midgap states leads to a drastic increase in linear absorption. Figure 7.1 shows the investigated rib-waveguide structure of the detector in a side view. Geometries of the detector are identical to the waveguide cross-section. The active length of the detector structure was varied between L_{CAV}=0.2 mm and 3 mm and the doped areas of the rib waveguide were separated by 750 nm from the silicon waveguide. An ion implantation in the order of 1e13/cm² has been used, masked with an implantation window defined by electron beam lithography centered to the silicon waveguide. Figure 7.2 depicts different Si-implanted photodiodes integrated on a test chip.

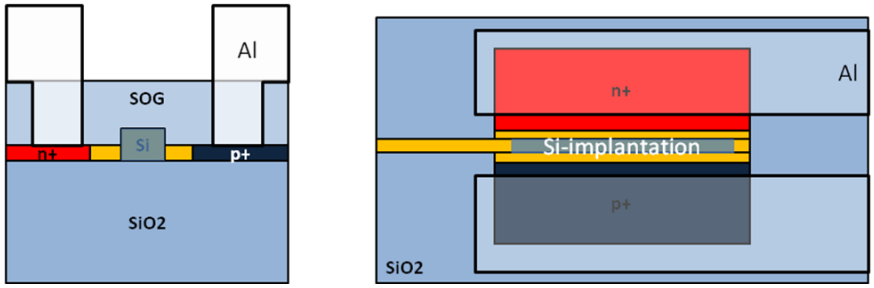


Figure 7.1: Schematic drawing of integrated Si-implanted photodiodes. (Left) cross sectional view, (right) top view.

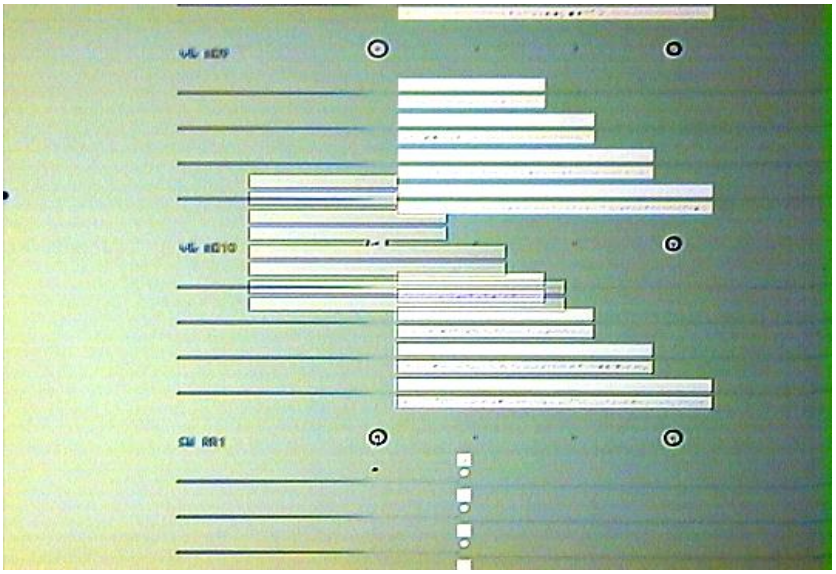


Figure 7.2: Test chip of the integrated Si-implanted photodiodes.

7.3 Characterization

After silicon ion implantation detector devices have been characterized in a linear electro-optic measurement setup. Fiber-to-chip coupling was achieved via grating couplers and electrical properties of the built-in PIN diodes have been investigated by metallic contact probes. Extracted photocurrents of the detector devices have been measured for various reverse bias voltages and optical input powers.

Analysis of the experimental data reveals a clear linear behavior between the optical power and the detected photocurrent of the Si-implanted photodiode. The linearity confirms the underlying effect of optical absorption at mid-bandgap states. Further details on the DC characterization can be found in the annex.

Si-implanted defect state photodetectors exhibit sensitivities that are in the same order of magnitude as their heterogeneous counterparts if a sufficient length of a few millimeters is used. This of course limits the detection speed that has to be considered in the project. As in PLATON only low-rate photodiodes are required for opto-electronically converting the low-rate header pulses, these detectors appear to be the optimum

candidates as they promise adequate performance values fully satisfying the PLATON platform requirements and easy and cost-effective integration.

	Ge-on-Si photodetectors					III-V-on-Si photodetectors				defect state photodetectors		
	 LUXTERA	 MIT	 INTEL	 UPS-IEF & LETI	 UPS-IEF & LETI	 EU- PICMOS project	 INTEL	 IMEC	 EU- PICMOS project	 Geis et al	 AMO COL project	 PLATON project
Year	~ 2007	2007	2007	2008	2009	2006	2007	2007-09	2009	2007	2009	2010-12
structure	PIN	PIN	PIN	PIN	PIN	PIN	PIN	MSM	PIN	PIN	PIN	PIN
Dark current at -1V	~10 µA	~1 µA	~170 nA	~ 20 nA	~ 1 µA	~1 nA	~50 nA	~1 nA	~1 nA	TBD	10 nA	100 nA
Responsivity	~ 0.85 A/W	~1.08 A/W	~0.9 A/W	~ 1 A/W	~0.8 A/W	~0.45 A/W	~0.31 A/W	~1 A/W	~0.7 A/W	0.8 A/W	0.23 A/W	0.1 A/W
Bandwidth	20 GHz	7.2 GHz	31 GHz	42 GHz	~ 90 GHz	33 GHz	0.5 GHz	-	25 GHz	~20 GHz	TBD	1 GHz

Table compiled by Vivien et al. (IEF) for EU Helios project

Figure 7.3: Comparison of various hetero-integrated photodiode approaches from literature and pure silicon solutions jointly developed by AMO and RWTH Aachen University.

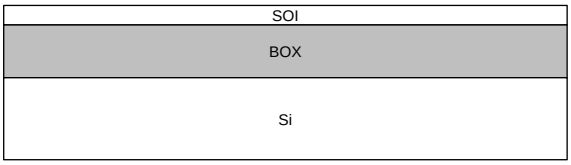
8 Full SOI Motherboard integration process

Based on the results of Workpackage 3, an integration scheme for the overall SOI nanophotonic motherboard has been set up. The process foresees the integration of all necessary components such as waveguides, grating couplers, multiplexing circuits with metal heaters, photodiodes, RF and DC metal interconnects, and landing sites for the plasmonic and IC integration

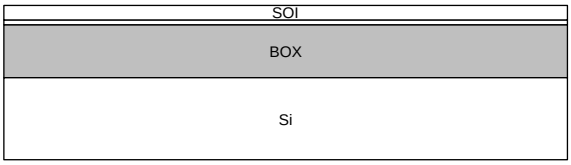
The overall motherboard fabrication process will be performed using a mix&match technology with electron beam lithography and photolithography. The process flow is schematically depicted below. The integration process foresees 13 subsequent lithography steps where electron beam lithography has to be used for #2 and #3 only. All other lithography steps can be performed using conventional photolithography. This allows for ultra-high accuracy during fabrication of the nanophotonic structures and reliable and cost-effective fabrication of the peripheral structures.

The overall integration process is compatible with all building blocks needed for the integration of PLATON´s routing platform.

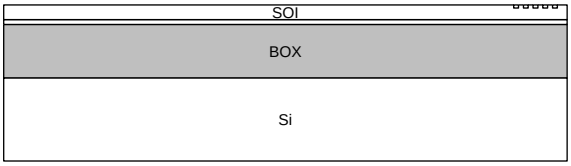
Overall Platon Process Flow



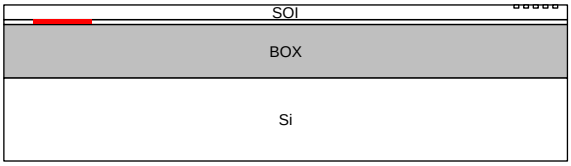
1) Patterning of Alignment markers



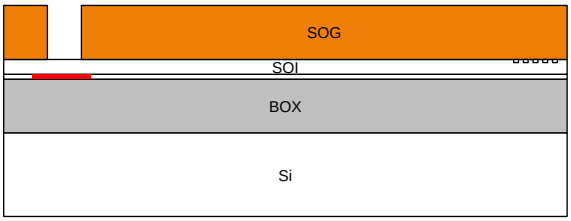
2) Rib waveguide patterning (EBL)



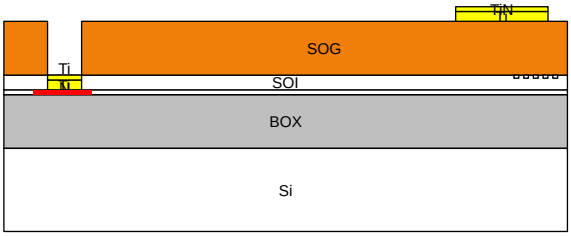
3) Grating coupler patterning (EBL)



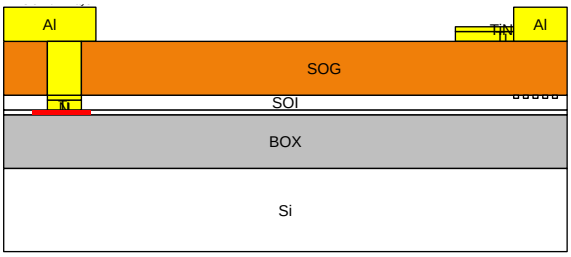
4, 5, 6) Implantation of As, B, Si



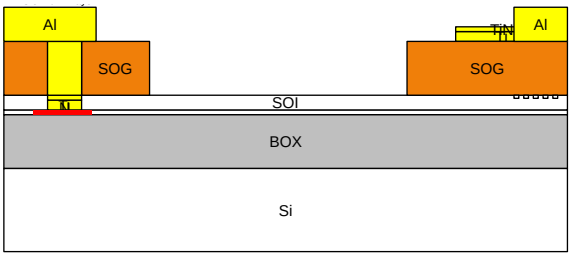
7) SOG deposition and contact patterning



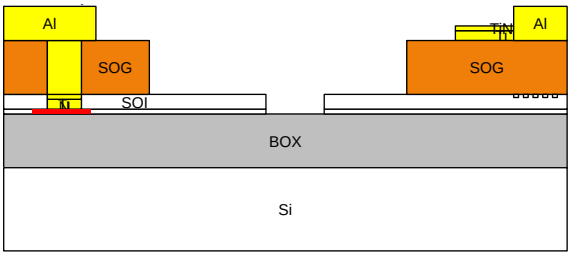
8) Ti/TiN metal deposition and patterning



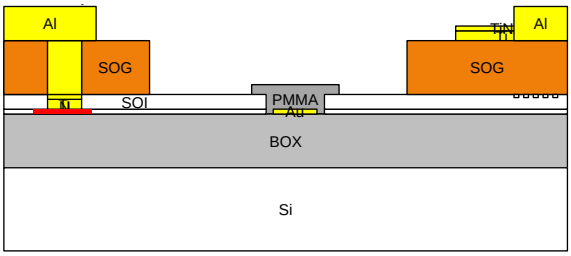
9) Al metal deposition and patterning



10) SOG patterning 2



11) Plasmonic landing site patterning



12, 13) Plasmonic integration

9 Conclusions

This deliverable presents an overview of the progress carried out so far on the fabrication of the silicon photonic components for the integration of the SOI motherboard. All elements to be employed in the 2x2 and 4x4 PLATON routing platforms have now been fabricated and characterized and their performance has been evaluated towards the project´s objectives. The non-plasmonic building blocks that were fabricated and analyzed within this deliverable involve:

- Silicon waveguides
- Fiber couplers (grating couplers)
- Silicon-on-Insulator Multiplexing (MUX) circuit
- Photodiodes for Header Detection

These components are exploited as the basis for launching the first fabrication run for PLATON's SOI motherboard. Following the fabrication runs and their experimental characterization, optimized designs will be implemented so as to conclude to improved layouts utilizing the feedback gained from the experimental procedures. Silicon nanophotonic fabrication is a stable and reproducible process at AMO. Waveguide structures are well defined and no technological limits or problems are expected.

10 References

[1] Y. Vlasov et al., Optics Express **12** (2004) 1622.

[2] J. Bolten, T. Wahlbrink, M. Schmidt, H.D.B. Gottlob, H. Kurz, Microelec. Eng., doi:10.1016/j.mee.2010.12.047.

[3] J. Bolten, T.Wahlbrink, N. Koo, H. Kurz, S. Stammberger, U. Hofmann, N. Ünal, Microelec.Eng. **87** (2010) 1041-1043.

[4] W. Bogaerts et al., IEEE J. Sel. Top. Quantum Electron. **12**(6) (2006) 1394–1401.

[5] W. Bogaerts et al., IEEE J. Sel. Top. Quantum Electron. **16**(1) (2010) 33–44.

[6] J. W. Corbett, and G. D. Watkins, "Silicon divacancy and its direct production by electron irradiation," Physical Review Letters **7** (1961) 314.

[7] M. W. Geis, S. J. Spector, M. E. Grein, J. U. Yoon, D. M. Lennon, and T. M. Lyszczarz, "Silicon waveguide infrared photodiodes with >35 GHz bandwidth and phototransistors with 50 A/W response," Optics Express 17 (2009) 5193-5204.

11 ANNEX – Parameters and Specifications

11.1 Waveguides

Parameter	Symbol	Design			Fabrication			Unit
		Min	Typ	Max	Min	Typ	Max	
Polarization			TM			TM		
Waveguide type			rib			rib		
Waveguide height			340		318	340	362	nm
Waveguide width			400		390		410	nm
Slab height			50		23	45	60	nm
Propagation losses			3		2.5	3	5	dB/cm

11.2 Grating Coupler

Parameter	Symbol	Design			Fabrication			Unit
		Min	Typ	Max	Min	Typ	Max	
Polarization			TM			TM		
Central wavelength	λ		1550			1550		nm
Bandwidth (3dB)			55			40		nm
Period	Λ		700			710		nm
Filling factor			0.8			0.8		
Etching depth			290			290		nm
Coupling angle			10			10		°
Coupling loss			-2.7		-4.4	-5	-6	dB

11.3 Si-to-DLSPP

Parameter	Symbol	Design			Fabrication			Unit
		Min	Typ	Max	Min	Typ	Max	
Cavity etching depth		180		200	190		230	nm
Space between waveguide end and metal			500		200		800	nm
Si-taper tip width			175	200		180		nm
Si-taper length			10	500		10		μm
Coupling losses			2.5		2.4		5.4	dB

11.4 MUX

Parameter	Symbol	Design			Fabrication			Unit
		Min	Typ	Max	Min	Typ	Max	
Spacing			100			100		GHz
Data rate/channel			40		10	40		Gb/s
3dB bandwidth			0.32 (40)		0.32 (40)	0.34 (42.5)	0.39 (48.75)	nm (GHz)
Most promising 2nd order rings:								
I: ring radius			9			9		µm
I: gap_1 (bus-ring)			190			190		nm
I: gap_2 (ring-ring)			380			380		nm
I: Free Spectral Range			9.23			9.23		nm
II: ring radius			12			12		µm
II: gap_1 (bus-ring)			170			170		nm
II: gap_2 (ring-ring)			300			300		nm
I: Free Spectral Range			6.9			6.9		nm

11.5 Photodetector

Parameter	Symbol	Design			Fabrication			Unit
		Min	Typ	Max	Min	Typ	Max	
Footprint			0.1				0.1	mm²
Reverse bias	V_{PD}		3			8	20	V
Max. average optical input power (NRZ)	P_{opt}		TBD					
Max. output peak voltage	V_{peak}		TBD					
Operating wavelength	λ	1500		1600		1550		nm
Length		0.2	0.75	1	0.2		1.6	mm
Initial current			50	90				mA
Sensitivity (DC) @1550nm	S		0.2		0.014	0.1	0.3	A/W
Polarization dependent loss	PDL		TBD					
3db cutoff frequency	f_{3dB}		1		0.001			GHz
Dark current	I_{dark}			100	1			nA

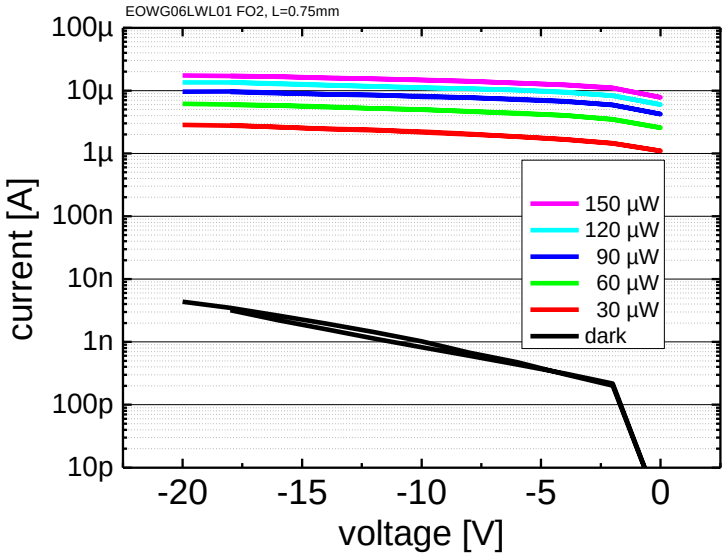


Figure 11.1: I-V characteristics of the photodiode at various optical power levels.

Figure 11.1 shows the current-voltage characteristics of the photodiode at various optical power levels inside the silicon waveguide. Plotting the photocurrent versus the optical power inside the waveguide for a fixed bias voltage a clear linear behavior can be found. The device with a length of 0.75 mm exhibits a sensitivity of 0.09 A/W and 0.11 A/W for 6V and 20V, respectively. With increased device length the sensitivity can be further increased. On this scale the sensitivity is approximately linear to the device length, i.e., for a sensitivity of S ≈0.3 A/W a detector length of 2.5mm would be sufficient. These results are comparable to state of the art [7]. In addition the dark current is by far below the specified maximum value of 100nA, even if the length of the plotted device (0.75mm) would have to be doubled or tripled to achieve the targeted sensitivity.

The Si-implanted photodetector has also been characterized dynamically. For this experiment a modulated optical NRZ signal was coupled into the detector device and the current response was measured at a fixed reverse bias voltage. Due to the limitations of the measurement setup the modulation speed of the laser diode was limited to 1 MHz. At this frequency no significant distortion was observed thus the detector is expected to be suitable for 10 Mb/s data recognition. However this data rate has to be proven experimentally in an alternative measurement setup.

11.6 Motherboard

Parameter	Symbol	Design			Fabrication			Unit
		Min	Typ	Max	Min	Typ	Max	
Patterned area	a			10				mm
Patterned area	b			7				mm