SEVENTH FRAMEWORK PROGRAMME
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[FET Proactive 1: Concurrent Tera-device Computing]

Project acronym: EURETILE
Project full title: European Reference Tiled Architecture Experiment
Grant agreement no.: 247846

WP9 – Training, Exploitation and Dissemination
D9.2 – Second Report on Training, Exploitation and Dissemination

Lead contractor for deliverable: INFN
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<th>Dissemination Level</th>
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1. **CASTNESS’12 WORKSHOP** on Computing Architectures Software tools and nano-Technologies for Numerical Embedded and Scalable Systems

During 2012, an important WP9 action has been the contribution to the organization of the CASTNESS’12 Workshop (Computer Architectures, Software tools and nano-Technologies for Numerical and Embedded Scalable Systems).

Twenty speakers, representing the four Teradevice Computing projects (EURETILE, TERAFLUX, TRAMS and SooS) presented their activities.

The CASTNESS’12 workshop has been collocated with the HIPEAC’12 conference (Paris, Jan 23-25th).

This year, according to the TERACOMP plan, the organizational leadership has been assumed by the TERAFLUX project (coordinator Prof. Roberto Giorgi, Università di Siena) and the workshop has been chaired by Rosa Badia (Barcelona Supercomputing Center).

**CASTNESS’12 AGENDA**

8:00-8:25 Registration
8:25-8:30 **Opening and Welcome**, Rosa M. Badia
8:30-10:45 **TRAMS project**
   
   - **Overview of the TRAMS Project in the second year**, Antonio Rubio (UPC)
   - **FinFET variability - TCAD based PDK development**, Si-Yu Liao (UOG)
   - **Variability Assessment for 10nm FinFET SRAM**, Miguel Miranda (Imec)
   - **Quantitative comparison of proactive and reactive variability compensation technique**, S. Ganapathy, (UPC)
   - **System Reconfiguration to Face Multicore Reliability and Variability Challenges**, Tanausu Ramirez (Intel)

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Panel discussion
10:45-11:00 Break
11:00-12:45 EURETILE project
- Brain Inspired Many-Tile Experiment: second year overview of EURETILE, Pier S. Paolucci (INFN)
- Peer-to-peer GPGPU-APENet+connectivity on HPC EURETILE platform, Piero Vicini (INFN)
- Management of process network dynamism in the distributed application layer, Iuliana Bacivarov (ETHZ)
- Simulation-based software debugging in many-tile systems, Luis Murillo (RWTH)
- The use of communication path formalization for driver synthesis in the context of hierarchical heterogeneous systems, Frederic Rousseau (UJF-TIMA)
- Application-Specific Instruction-set Processors (ASIPs) and related design tools for tiled systems, Gert Goossens (TARGET)
- EURETILE Specific Questions & Answers
- Panel discussion
12:45-14:00 Lunch Break
14:00-15:45 TERAFLUX project
- TERAFLUX: exploiting dataflow parallelism in teradevice computing - Year 2, Roberto Giorgi (UNISI)
- Teraflux Architecture, Skevos Evripidou (UCY)
- Reliability aspects in Teraflux, Theo Ungerer (U. Augsburg)
- Teraflux, from the programming model to the execution model Antoniu Pop (INRIA)
- Panel discussion
15:45-16:15 Break
16:15-18:00 SoOs project
- Overview & Status of S(o)OS (HLRS)
- New approaches to annotating & identifying concurrency and parallelism on code level (HLRS/UT)
- Description of resource capabilities using CIASH (UT)
- Characterization and analysis of pipelined applications on the Intel SCC (SSSA)
- Rethinking Transactional Memory in the Manycore Context (EPFL)
- Communication & migration in many-core systems (IT)
- Panel Discussion

2. Papers - Posters - Technical Press – Newsletters
Here after the list updated to the reporting date.

2.1 ETHZ

2013

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2012


2011


2010


2.2 RWTH

2012

- Schumacher, J. H. Weinstock, R. Leupers, G. Ascheid, L. Tosoratto, A. Lonardo, D. Petras, T. Groetker. *IegaSCi: Legacy SystemC Model Integration into Parallel...
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- SystemC Simulators”. 1st Workshop on Virtual Prototyping of Parallel and Embedded Systems (ViPES), 2013, Boston, USA (accepted for publication).

2011

2010

2.3 TIMA

2011

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### 2.4 INFN

**2012**

- The EURETILE Consortium - Brain Simulation Benchmark: Inspiring and benchmarking the scalability and fault-tolerance of future many-tile systems - Poster at HIPEAC12 - Jan 2012 Paris, France

**2011**


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• APEnet+ project status - XXIX International Symposium on Lattice Field Theory - July 2011 Squaw Valley, Lake Tahoe, CA

2010
• Pier Stanislao Paolucci - *FP7 EURETILE Project: EUropean REference TILed architecture Experiment* - HipEacInfo, Quarterly Newsletter, Number 24, page 11, October 2010 (http://www.Hipeac.net/newsletter)
• R. Ammendola et al. - *High speed data transfer with FPGAs and QSFP+ modules* - Nuclear Science Symposium Conference Record (NSS/MIC) 2010 IEEE, Publication Year: 2010, Page(s): 1323 1325, November 2010, Knoxville, Tennessee. DOI: 10.1109/NSSMIC.2010.5873983

3. Presentations

3.1 ETHZ

2012

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2011


2010


3.2 RWTH

2012

- R. Leupers. Design Technologies for Wireless Multiprocessor Systems-on-Chip, PhD course, University of Pisa, Jul 2012, Pisa, Italy
- R. Leupers, H. Meyr. Embedded Processor Design, Block lecture ALaRI, Feb 2012, University of Lugano, Lugano, Switzerland
- Luis Murillo. Simulation-based software debugging in many-tile systems. CASTNESS 2012, January 26, 2012, Paris, France

2011

- Juan Eusse. Hybrid Simulation Technology for Extensible Cores and Full System Simulation of Complex MPSoCs. Presentation at HiPEAC Computing Systems Week, Nov 2011, Barcelona, Spain
- S. Yakoushkin. Advanced Simulation Techniques, Joint RWTH/TU Tampere Seminar, June 2011, Tampere, Finland
- R. Leupers (organized by). ICT Technology Transfer Workshop targeting Horizon 2020, Apr 2011, Brussels, Belgium
- R. Leupers and G. Martin (organized by). Special session at DATE 2011: Virtual Manycore Platforms: Moving Towards 100+ Processor Cores, March 2011, Grenoble, France
- R. Leupers, H. Meyr. Embedded Processor Design, Block lecture ALaRI, Feb 2011, University of Lugano, Lugano, Switzerland
- Jovana Jovic, Simulation Challenges in the EURETILE Project, CASTNESS 2011, January 17-18, 2011, Rome, Italy

2010

- Christoph Schumacher, Virtual Platform Technologies for Multi-core Platforms, UMIC Day, 19 October, 2010, RWTH Aachen, Germany
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- Rainer Leupers, HiPEAC Cluster Meeting (Design and Simulation Cluster), October 2010, Barcelona, Spain
- Christoph Schumacher, Stefan Kraemer and Rainer Leupers, demonstration at DAC 2010 exhibition: parSC: parallel SystemC simulation, deterministic, accurate, fast, June 14-16, 2010, Anaheim, USA
- Rainer Leupers, MPSoC Design for Wireless Multimedia, Tutorial, MIXDES, June 2010, Wroclaw, Poland
- Stefan Kraemer, Advanced Simulation Techniques for Virtual Platforms, May 26, 2010, Imperial College London, London, United Kingdom
- Rainer Leupers, Cool MPSoC Design, ASCI Winter School on Embedded Systems, March 2010, Soesterburg, Netherlands
- Rainer Leupers, Embedded Processor Design and Implementation, course in MSc in Embedded Systems track at ALaRI Institute, March 1-4, 2010, University of Lugano, Switzerland

3.3 **INFN**

2012
- D. Rossetti, Leveraging NVIDIA GPUDirect on APEnet+ 3D Torus Cluster Interconnect - GTC 2012 - GPU Technology Conference - May 2012 - San Jose, CA, [[8]]
- R. Ammendola, Comunicazioni Peer to Peer tra GPU remote con APEnet+ - E4 Workshop 2012 - Sept 2012 - Bologna, Italy [[9]]
- D. Rossetti, Multi GPU simulations: status and perspectives - New Frontiers in Lattice Gauge Theory, GGI Firenze, Italy - [[10]]
- Davide Rossetti, Breadth First Search on APEnet+ - talk at IA^3 Workshop on Irregular Applications at SC12 conference, 10 Nov 2012. Presentation available here
- Pier Stanislao Paolucci, Brain Inspired Many-Tile Experiment: second year overview of EURETILE, CASTNESS’12, 26 January 2012, Paris, France
- P. Vicini, Peer-to-peer GPGPU-APEnet+connectivity on HPC EURETILE platform, CASTNESS’12, 26 January 2012, Paris, France

2011

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### 3.4 Target

**2012**

**2011**
- G. Goossens, “Building Multicore SoCs with Application-Specific Processors”, Electronic Design and Solutions Fair, Yokohama (Japan), November 16-18, 2011.
- G. Goossens, “Building Multicore SoCs with Application-Specific Processors”, Intl. Conf. on IP-Based SoC Design (IP-SoC-2011), Grenoble (France), December 7-8, 2011.
2010