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WP9 – Training, Exploitation and Dissemination
D9.3 – Third Report on Training, Exploitation and Dissemination

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Third Report on Training, Exploitation and Dissemination

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1. CASTNESS’13 WORKSHOP on Computing Architectures
   Software tools and nano-Technologies for Numerical Embedded and Scalable Systems

During 2013, an important WP9 action has been the contribution to the organization of the
CASTNESS’13 Workshop (Computer Architectures, Software tools and nano-Technologies
for Numerical and Embedded Scalable Systems).

Twenty speakers, representing the four Teradevice Computing projects (EURETILE,
TERAFLUX, TRAMS and SooS) presented their activities.

The CASTNESS’13 workshop has been held in Barcellona (28th June 2013).

This year, according to the TERACOMP plan, the organizational leadership has been
assumed by the TRAMS project (coordinator Prof. Antonio Rubio, Universitat Politècnica
de Catalunya (UPC)) and the workshop has been chaired by Antonio Rubio and Lutz
Schubert (Universität Ulm).

1.1 CASTNESS 2013 Agenda

   9.00 Welcome and introduction

   9.10 90 MINUTES SLOT FOR TRAMS PROJECT
   • “Overview of the TRAMS project”, Antonio Rubio
   • “Controlled Degradation Stochastic Resonance in Future Nanoarchitectures”, Nivard
     Aymerich
   • "New cells and reliability mechanisms for next generation memories", Ramon Canal
   • “Performance, power and reliability aware designs for tera-scale processors”, Intel
   • “Dynamically Capturing Vulnerability Variation for Caches”, Intel

   10.40 Coffee break

   11.20 90 MINUTES SLOT FOR S(o)Os PROJECT

   12.50 Lunch time

   14.30 90 MINUTES SLOT FOR EURETILE PROJECT
   • “The EURETILE parallel simulation environment”, Jan H. Weinstock, RWTH Aachen
   • "Distributed application layer: mapping dynamic applications on many-core systems”,
     Iuliana Bacivarov, ETH Zurich
   • "Full Methodology of a Lightweight Task Migration in Embedded Multi-Tiled
     Architecture Using Task Code Replication”, Ashraf ELANTABLY, TIMA
   • "The EURETILE hardware experimental platform" - Andrea Biagioni, INFN - TARGET
   • "Fault and critical event awareness: a no single point of failure approach for
distributed systems" - Laura Tosoratto, INFN-TARGET

   16.00 90 MINUTES SLOT FOR TERAFLUX
CONCLUSIONS; ROUND TABLE and CLOSING

2. Papers - Posters - Technical Press – Newsletters

Hereafter the list updated to the reporting date.

2.1 ETHZ

2013


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2012


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2011


2010

2.2 RWTH

2013


2012

Project: **EURETILE** – European Reference Tiled Architecture Experiment  
Grant Agreement no.: **247846**  


**2011**

- S. Kraemer, Design and analysis of efficient MPSoC simulation techniques, dissertation, 2011, Aachen, Germany.

**2010**


**2.3 TIMA**

**2013**


**2012**


**2011**


**2.4 INFN**

**2013**


Project: **EURETILE** – European Reference Tiled Architecture Experiment
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- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Davide Rossetti, Francesco Simula, Laura Tosoratto and Piero Vicini, "Design and implementation of a modular, low latency, fault-aware, FPGA-based Network Interface" IEEE Xplore, track on International Conference on Reconfigurable Computing and FPGAs (ReConFig) 2013, to be published.


**2012**

- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Davide Rossetti, Francesco Simula, Laura Tosoratto, Piero Vicini. APEnet+: a 3-D Torus network optimized for GPU-


2011


2010
3. Presentations

3.1 ETHZ

2013

- Iuliana Bacivarov, How model-based design simplifies the debugging of many-core systems. 1st International Workshop on Multicore Application Debugging (MAD 2013). Nov. 2013, Munich, Germany.
- Iuliana Bacivarov, Distributed Application Layer - Run-time mapping of streaming applications on heterogeneous many-core systems. DAC CHANGE - Computing in
Heterogeneous, Autonomous 'N' Goal-oriented Environments, June 2013, Austin, TX, USA.

2012


2011

- Iuliana Bacivarov, Distributed Application Layer – Towards Seamless Programming of Many-Tile Architectures, CASTNESS 2011, 17 and 18 January 2011, Rome, Italy

2010

- Iuliana Bacivarov, Distributed Operation Layer: An Efficient and Predictable KPN-Based Design Flow, invited talk at Workshop on Compiler-Assisted System-On-
Chip Assembly 2010, in conjunction with Embedded Systems Week, Scottsdale, AZ, US, October 2010

- Iuliana Bacivarov, Efficient Execution of Kahn Process Networks on CELL BE, invited talk at Summer School on Models for Embedded Signal Processing Systems at Lorentz Center, Leiden, Netherlands, 30 Aug - 3 Sep 2010
- Iuliana Bacivarov, Distributed Operation Layer: A Practical Perspective, tutorial at Summer School on Models for Embedded Signal Processing Systems at Lorentz Center, Leiden, Netherlands, 30 Aug - 3 Sep 2010
- Iuliana Bacivarov, invited talk at Efficient Execution of Kahn Process Networks on MPSoC, Mapping Applications to MPSoCs 2010, June 29-30, 2010, St. Goar, Germany.

### 3.2 RWTH 2013

- R. Leupers. Keynote at Sabanci Univ, Oct 2013, Istanbul, Turkey
- R. Leupers. HiPEAC boot at DATE’13, Mar 2013, Grenoble, France
- R. Leupers. System-Level Design Technologies. Joint RWTH/Intel Lab seminar, Mar 2013, Aachen, Germany
- R. Leupers. Embedded Processor Design, Block lecture ALaRI, Jan-Feb 2013, University of Lugano, Lugano, Switzerland.
Asia and South Pacific Design Automation Conference (ASP-DAC), Jan 2013, Yokohama, Japan
- R. Leupers. Joint RWTH/U Ghent Seminar, Jan 2013, Aachen, Germany
- R. Leupers. Embedded Processor Design, course. Thai-German Graduate School (TGGS), Jan 2013, Bangkok, Thailand

2012

- R. Leupers. Design Technologies for Wireless Multiprocessor Systems-on-Chip, PhD course, University of Pisa, Jul 2012, Pisa, Italy
- R. Leupers, H. Meyr. Embedded Processor Design, Block lecture ALaRI, Feb 2012, University of Lugano, Lugano, Switzerland
- Luis Murillo. Simulation-based software debugging in many-tile systems. CASTNESS 2012, January 26, 2012, Paris, France

2011

- Juan Eusse. Hybrid Simulation Technology for Extensible Cores and Full System Simulation of Complex MPSoCs. Presentation at HiPEAC Computing Systems Week, Nov 2011, Barcelona, Spain
- S. Yakoushkin. Advanced Simulation Techniques, Joint RWTH/TU Tampere Seminar, June 2011, Tampere, Finland
- R. Leupers (organized by). ICT Technology Transfer Workshop targeting Horizon 2020, Apr 2011, Brussels, Belgium
R. Leupers and G. Martin (organized by). Special session at DATE 2011: Virtual Manycore Platforms: Moving Towards 100+ Processor Cores, March 2011, Grenoble, France

R. Leupers, H. Meyr. Embedded Processor Design, Block lecture ALaRI, Feb 2011, University of Lugano, Lugano, Switzerland

Jovana Jovic, Simulation Challenges in the EURETILE Project, CASTNESS 2011, January 17-18, 2011, Rome, Italy

2010

Christoph Schumacher, Virtual Platform Technologies for Multi-core Platforms, UMIC Day, 19 October, 2010, RWTH Aachen, Germany

Rainer Leupers, HiPEAC Cluster Meeting (Design and Simulation Cluster), October 2010, Barcelona, Spain


Christoph Schumacher, Stefan Kraemer and Rainer Leupers, demonstration at DAC 2010 exhibition: parSC: parallel SystemC simulation, deterministic, accurate, fast, June 14-16, 2010, Anaheim, USA

Rainer Leupers, MPSoC Design for Wireless Multimedia, Tutorial, MIXDES, June 2010, Wroclaw, Poland

Stefan Kraemer, Advanced Simulation Techniques for Virtual Platforms, May 26, 2010, Imperial College London, London, United Kingdom

Rainer Leupers, Cool MPSoC Design, ASCI Winter School on Embedded Systems, March 2010, Soesterburg, Netherlands

Rainer Leupers, Embedded Processor Design and Implementation, course in MSc in Embedded Systems track at ALaRI Institute, March 1-4, 2010, University of Lugano, Switzerland

3.3 INFN

2013

Roberto Ammendola - Virtual-to-Physical address translation for an FPGA-based interconnect with host and GPU remote DMA capabilities - 2013 International Conference on Field-Programmable Technology (ICFPT) 2013 - 9-11 dec - Kyoto, Japan

Alessandro Lonardo - Building a Low-latency, Real-time, GPU-based Stream Processing System - GTC 2013 - March 20, 2013 - San Jose (California)

Andrea Biagioni - The EURETILE hardware experimental platform - CASTNESS 2013 - 28 June 2013 - Barcelona, Spain

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Laura Tosoratto - Fault and Critical Event Awareness: a no-single-point-of-failure approach for distributed systems - CASTNESS 2013 - 28 June 2013 - Barcelona, Spain


Francesco Simula - From GPU-accelerated computing to GPU-accelerated data acquisition for physics experiments; the QUonG cluster, the APEnet+ network card and the APE project evolution - X Seminar on Software for Nuclear, Subnuclear and Applied Physics 2013 - Alghero, Italy

Piero Vicini - Analysis of performance improvements for host and gpu interface of the APEnet+ 3D Torus network - XV International Workshop on Advanced Computing and Analysis Techniques in Physics (ACAT)- Beijing, China - May 2013

Piero Vicini - GPU for Real Time processing in HEP trigger systems - XV International Workshop on Advanced Computing and Analysis Techniques in Physics (ACAT)- Beijing, China - May 2013

Davide Rossetti - GPU Techniques Applied to a Cluster Interconnect - Parallel and Distributed Processing Symposium Workshops PhD Forum (IPDPSW) 2013 - Boston, MA.

Alessandro Lonardo - Architectural improvements and 28 nm FPGA implementation of the APEnet+ 3D Torus network for hybrid HPC systems - International Conference on Computing in High Energy and Nuclear Physics (CHEP) 2013, 14-18 Oct 2013, Amsterdam, Nederlands.

Ottorino Frezza - Design and implementation of a modular, low latency, fault-aware, FPGA-based Network Interface - ReConFig 2013 - Dec 2013 - Cancun, MEX.

2012

R. Ammendola, apeNET+: a 3D toroidal network enabling petaFLOPS scale Lattice QCD simulations on commodity clusters, Lattice 2010, THE XXVIII INTERNATIONAL SYMPOSIUM ON LATTICE FIELD THEORY, Villasimius, Italy, June 2010

D. Rossetti, Leveraging NVIDIA GPUDirect on APEnet+ 3D Torus Cluster Interconnect - GTC 2012 - GPU Technology Conference - May 2012 - San Jose, CA

R. Ammendola, Comunicazioni Peer to Peer tra GPU remote con APENet+ - E4 Workshop 2012 - Sept 2012 - Bologna, Italy

D. Rossetti, Multi GPU simulations: status and perspectives - New Frontiers in Lattice Gauge Theory, GGI Firenze, Italy

Davide Rossetti, Breadth First Search on APEnet+ - talk at IA^3 Workshop on Irregular Applications at SC12 conference, 10 Nov 2012

Pier Stanislao Paolucci, Brain Inspired Many-Tile Experiment: second year overview of EURETILE, CASTNESS’12, 26 January 2012, Paris, France

P. Vicini, Peer-to-peer GPGPU-APEnet+connectivity on HPC EURETILE platform, CASTNESS’12, 26 January 2012, Paris, France
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2011

- D. Rossetti, apeNET+ Project Status, Lattice 2010, THE XXIX INTERNATIONAL SYMPOSIUM ON LATTICE FIELD THEORY, Squaw Village, Lake Tahoe, CA, USA, July 2011
- P. Vicini, QUonG: A GPU-based HPC System Dedicated to LQCD Computing - Symposium on Application Accelerators in High-Performance Computing, Knoxville, TN - USA, July 2011
- D. Rossetti, Remote Direct Memory Access between NVIDIA GPUs with the APEnet 3D Torus Interconnect - SC11 - International Conference for High Performance Computing, Networking, Storage and Analysis - Seattle, WA
- Pier Stanislao Paolucci, EURETILE: Brain-Inspired many-tile SW/HW Experiment, CASTNESS 2011, 17 and 18 January 2011, Rome, Italy,
- P. Vicini, EURETILE: The HPC and Embedded Experimental HW Platform, CASTNESS 2011, 17 and 18 January 2011, Rome, Italy,

3.4 Target

2011

- G. Goossens, “Building Multicore SoCs with Application-Specific Processors”, Electronic Design and Solutions Fair, Yokohama (Japan), November 16-18, 2011.
- G. Goossens, “Building Multicore SoCs with Application-Specific Processors”, Intl. Conf. on IP-Based SoC Design (IP-SoC-2011), Grenoble (France), December 7-8, 2011.
2010


3.5 TIMA

2013

- Ashraf Elantably, Frédéric Rousseau. Lightweight task migration in embedded multi-tiled architectures using task code replication, CASTNESS 2013, Barcelona, Spain.

2012

- Frédéric Rousseau, presentation of the EURETILE project in front of the Board of directors of the University Joseph Fourier, March 2011, Grenoble, France (in French)
- Frédéric Rousseau, Communication Synthesis in Low Level Software for Hierarchical Heterogeneous Systems, CASTNESS 2011, January 17-18, 2011, Rome, Italy

4. Books

4.1 ETHZ

4.2 RWTH


4.3 TIMA


4.4 Joint reports
2013