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SiNAPS

Semiconducting Nanowire Platform for Autonomous Sensors

Collaborative Project

FP7-ICT-2009-5: Future and Emerging Technologies

“Towards Zero Power ICT” Proactive Scheme



Deliverable D4.4: Charging and sensor demos, targets for final platform and integration

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Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

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1 Executive Summary (publishable)

This report describes the integration & packaging concepts of the SiNAPS sensor system and is referred in the project proposal as deliverable 4.4 “charging and sensor demos, targets for final platform and integration”.

The report describes on the integration process of a charging, a sensing demonstrator and the final platform for demonstration of the project results.

WP4 has no delays; in the next months minor delays could occur due to late delivery of parts and some problems in the wire bonding process. These delays are expected to stay within two months.

2 Introduction

This is the report on deliverable D4.4 as defined in the SiNAPS Project Proposal.

D4.4: Charging and sensor demos, targets for final platform and integration (Nanosens M30)

This report describes:

- 1. Design Considerations for Issue 2 & 3*
- 2. Assessment of the Thermoplastic Chip Bonding Process for Die Placement*
- 3. Feasibility Tests of the Wire Bonding Process*
- 4. Planning Towards Final Deliverable D4.5*

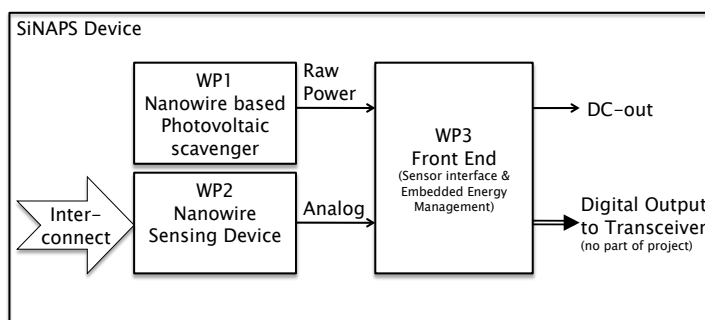
3 Design Considerations for Issue 2 & 3

3.1 Substrate Layout

Deliverable 4.3 in month 15 of the SiNAPS Project was finalised with a comparison between a passive substrate and a patterned conductive substrate. Basically, the Issue 3 is a miniaturized version of the Issue 2. Design options that are made for Issue 2 count also applies for Issue 3, though only the options with highest integration performance can be applied for Issue 3. A trade off between the two options was made and has led to a preferred solution with a fully passive substrate. This however was conditional; it needed a matching bonding method for the assembly of the Dies on the substrate. This bonding method should be able to place the Dies with small gaps in between, as little as 50 micron. This is not possible with a standard soldering process, therefore alternatives are investigated.

3.2 Interconnections

In the early stage of the project, the number of interconnections has been inventoried (Deliverable 4.2). This inventory is still up to date, though the Digital Output to the transceiver, the transceiver being no part of the project, will be implemented in Issue 3.



Inventory of the internal and external interconnections

The interconnections are to be divided into two categories:

- The interconnections for the power circuitry;
- Interconnections for the sensor data path (analogue as well digital).

3.2.1 Power circuitry

The power circuitry will be fully implemented in the Issue 2 and the Issue 3 design and connects the PV cells with the EPFL power chip and the power chip to the outside world. Interconnections can be realised with die-to-die wire bonds, however, the power dies need to be bonded using a Au wire. This is different from e.g. the PV cell.

3.2.2 Sensor data path

The sensor data path connects the sensor output with the power die (which also contains the ADC) with the RF transceiver (outside world).

Due to the lead times of the fluidic sensor of WP2 the planning for integration cannot be reached when implementing a fluidic sensor and a hydrogen sensor Die (based on pre-existing demonstrators) will be integrated in the designs for Issue 2 and 3. The current, first generation, power Die is not equipped with a suitable ADC yet, and as such cannot complete the sensor data path. For this reason, a fully functional sensor data path will not be applied in the Issue 2 design. At a later stage, in the Issue 3 design, it will be implemented based on the second generation Power Management Die, designed and made by EPFL.

3.3 Placement and Bonding of the Dies

Initial designs of Issue 2 and 3 have indicated that the effective use of substrate area is respectively 62% and 55%. The application of an enhanced bonding method could increase this level to more than 70%, being limited by the tolerances of the parts. Reduction of the gap size and also the distance to the board edges requires state of the art positioning of the dies. Commercial pick and place equipment is able to realise the required die accuracies fairly easy; however, bonding the dies without movement of the parts during the curing process is more difficult. For this reason two alternatives for this process were investigated, Snap-Cure and Thermoplastic bonding:

1/ Snap Cure:

Snap Cure is a method where an adhesive bond layer is activated, gets (sticky) and starts curing. During a certain time window, varying from seconds to minutes, the product can be placed in the adhesive. Due to the sticky behaviour, the component stays in place.

2/ Thermoplastic Chip Bonding:

The second alternative is a thermoplastic way of bonding. In this case the substrate is covered with a layer of thermoplastic material that can be used as an adhesive layer. The chip is heated to a certain temperature and placed in the adhesive layer. The heat shock on the component is comparable to the process of soldering.

3.4 Selection of the Process of Die Bonding

UV Snap cure (eg Delo, Loctite) is a standard process where the substrate is heated quickly after placement of the parts. The process takes, depending on chosen materials, between 30 and 90 seconds. Parts and substrate are both heated to cure the adhesive, which requires a thermally matching substrate. Since the thermal expansion of the Si Dies is low this limits the option for the choice of substrate material; some ceramic materials, glass or carbon fibre substrates can be used.

The second bonding method, heated Die thermoplastic bonding, is a proved but not a broadly used industrial process. It suffers from the shortcoming that the thermal conductance to the substrate is not optimal. Except for this, the Dies could come off of the substrate when heated up during its functional performance (CPU's Power electronics). In the case of the SiNAPS project however, the thermal load of the interconnection is minimal, since the project deals with low power electronics. The general shortcoming of the process is not a shortcoming for SiNAPS due to the low power usage of the SiNAPS system.

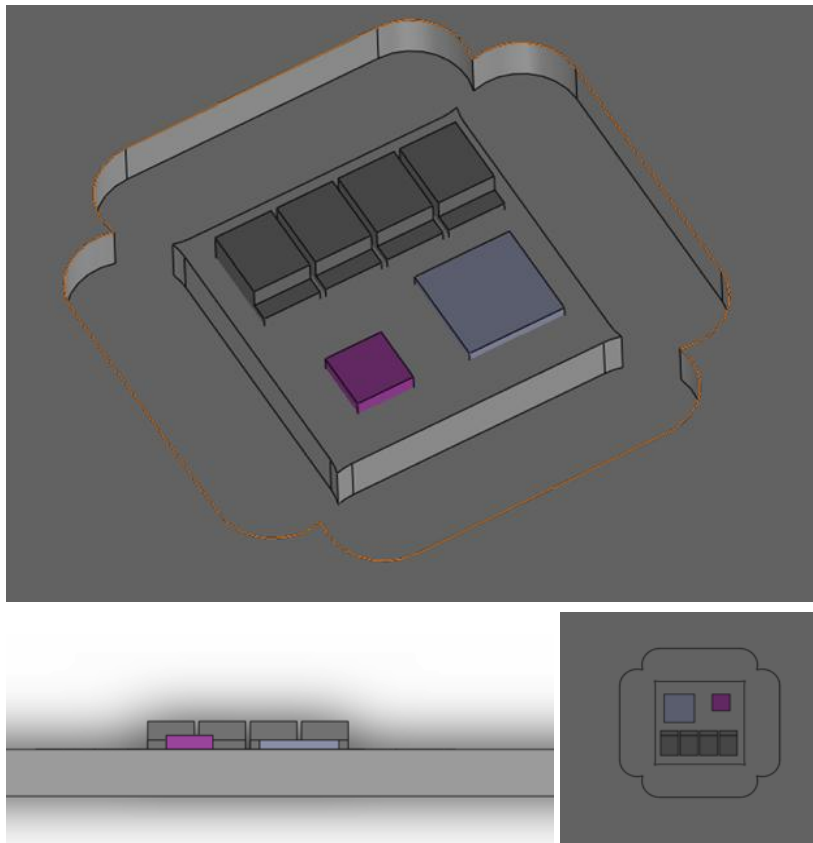
The positive quality of the thermoplastic bonding is the capability of using a broad scope of plastics for the substrate. In the process the Die is heated but the substrate remains cool. For this reason there is limited thermal expansion of the substrate when the heated Die is placed. The substrate remains cool and in combination with the limited thermal expansion of the Si Dies, the connection is reliable as long as the Die stays cool ($<100^{\circ}\text{C}$).

A second positive attribute of the process is that it enables integration of housing and substrate, this is an extra space saver when real products, that need a protective package for the (harsh) environments where they are applied.

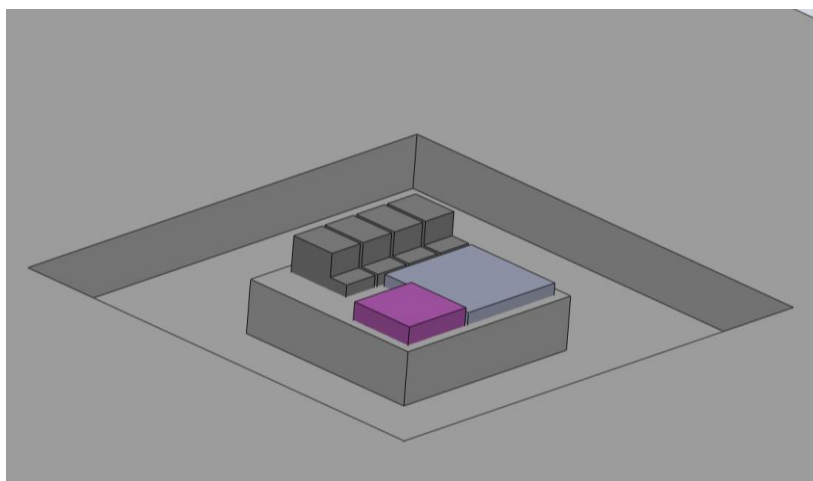
Thermoplastic bonding is considered a very suitable process for SiNAPS and has been chosen for as bonding method for both Issue 2 and 3.

3.5 Layout and Geometrical design of Issue 2 and 3

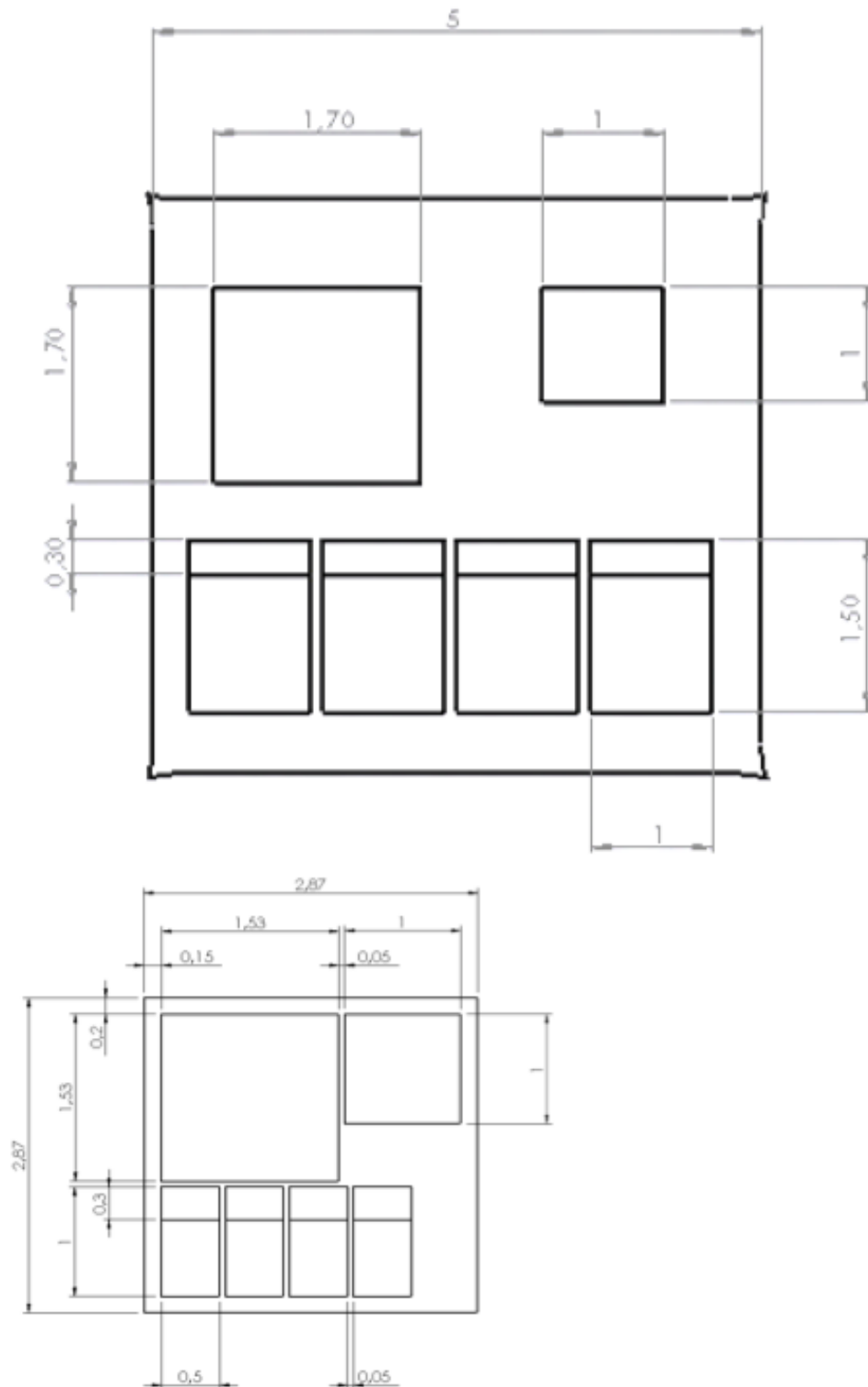
The number of PV-Cells has been unsure since the beginning of the project, not knowing the exact voltage that would be generated by the Cells. Based on measurement at EPFL and recent evaluation of the quality of the last batched produced, the number has been determined and set to four PV cells. This has some changes for the design. However, since the substrate has no conducting elements left, these changes in the design could be carried through easily. This has led to the following geometrical design of Issue 2 and 3:



Layout in 3D, Side View and Top View of Issue 2



Top View of Issue 3



Geometry of Issue 2 in comparable scaling

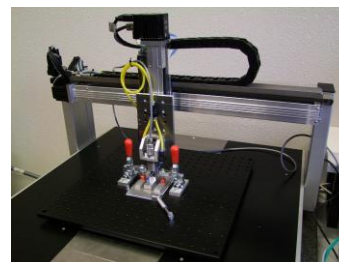
4 Assessment of the TC-Bonding Process for Die Placement

4.1 Die Placement

For the manufacturing of SiNAPS devices, an industrial Pick & Place process will be used. This choice enables the use of high-end but standard industrial equipment.

Pick & Place is a 2½D process; it is performed in a two-dimensional plane, the third dimension is used for handling. A Pick & Place process consists of a number of sequential actions; the basic order is:

- Feeding the part from a tray, tape or other storage system;
- Grasping the part with a gripper that is able to hold the part firmly without damaging it (in this case the nanowire structure);
- Mount the part to the substrate.



Standard Pick&Place equipment is available in the industry

The mounting process can be divided into three sub-actions:

- Collide; mate the part and the substrate;
- Fixate; this is an optional step that is frequently used. It takes care of a temporary (secondary) connection if the final bonding cannot be applied instantly;
- Cure; the functional adhesive is cured or a solder connection is cooled down.

In case of the bonding of the SiNAPS device, little problems are to be expected with the Feeding & Grasping processes, but for the bonding process, *an instant bond is needed since there is too little room for a secondary connection.*

4.2 Process Development

4.3 General

The positive quality of the thermoplastic bonding is the capability of using a broad scope of plastics for the substrate. In the process the Die is heated but the substrate remains cool. For this reason there is limited thermal expansion of the substrate when the heated Die is placed. The substrate remains cool and in combination with the limited thermal expansion of the Si Dies, the connection is reliable as long as the Die stays cool (<100 °C).

A second positive attribute of the process is that it enables integration of housing and substrate, this is an extra space saver when real products, that need a protective package for the (harsh) environments where they are applied.

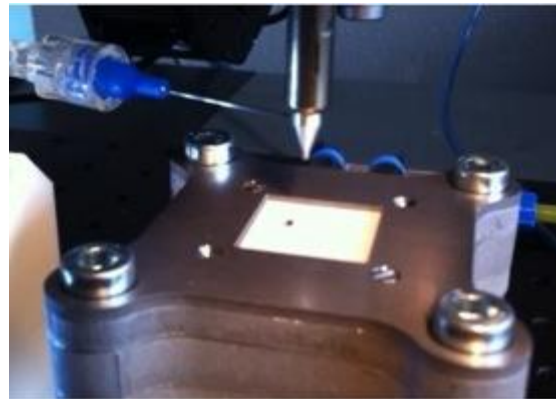
Thermoplastic bonding is a very suitable process for SiNAPS and has been chosen for as bonding method for Issue 2 and 3.

4.3.1 Equipment

The process of thermoplastic bonding can be applied on standard Pick & Place equipment. This equipment is available to Nanosens, however some process specific tooling needs to be designed. The main topic is a heated vacuum gripper that holds the Die and is able to heat it to a certain, adjustable, temperature. For this a dedicated gripper was developed.

4.4 Equipment for Die Placement

- Equipment was installed and site-accepted;
- Heated gripper designed, built & tested;
- Developed vacuum table for fixed positioning of the substrate;
- Designed spring loaded stage to prevent part being over constrained during placement;
- Installed top and bottom cameras to track position of parts;
- Software development to support semi-automated placement of dies.



4.5 Thermoplastic Bonding Process (SMD's)

- Started with Polystyrene (PS) Substrates;
- Operating windows were scanned with Surface Mounted Devices (SMDs, see figure);
- Tuned settings and software;
- Performed preliminary shear tests to measure bond strength;
- Operating window OK for SMD's.

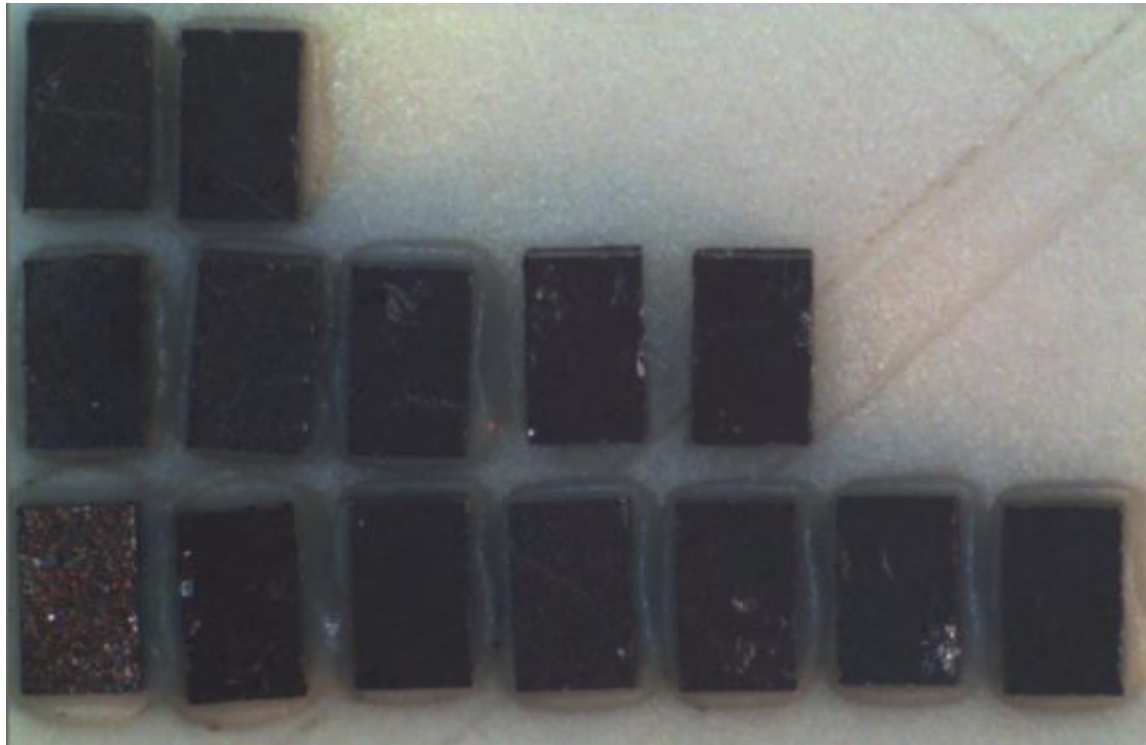


4.6 Bonding of IPHT-Dies

- Larger operating window with Si dies due to better heat conductance of Si;
- Minimal intrusion depth on substrate
- Low deformation enables close positioning of dies → Important for Issue 3 that needs minimal gap size
- Initial bond strength OK (to be characterised further).



4.7 Placement test



- Process seems feasible; reliable bond;
- Placement is still done semi automated → small errors in placement → adding computer vision system;
- Machine has been characterised.

4.8 Optimisations of the Thermoplastic Bonding Process

So far, the thermoplastic bonding process and related equipment is brought to a basic starting level:

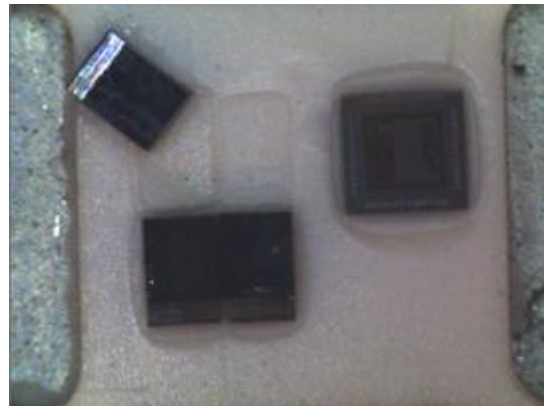
- One material tested so far: Polystyrene (PS);
- Reasonable results have been achieved with placement of dummy parts;
- Investigations have focussed on the gap size between parts, 50 micron seemed feasible;
- Equipment was up and running well;
- Many parameters still to be investigated: time, pressure, Temperature, Placement speed, etc.

Last months have been spent to characterise the bonding process and find a tolerant working area within the many parameters to vary. This working area is found with the following settings. Tolerances on settings seem ok to be varied within +/- 10% (except placement height +/- 0,1 mm), thus forming a working area around the following settings:

Temperature	300	°C
Speed	2	mm/s
Placement height z	-93.58	EPFL-module in mm
	-93.42	Pd-sensor in mm
	-93.1	PV-cell in mm
Mate time	0.8	s
Release time	0.1	s
Release distance Z	10	mm
Placement Force	35.7	gram

Initial tests indicate that the assembled devices survive at least 10G. For most domestic applications this seems enough. Shear tests have not been performed yet due to prioritisation.

Though there has not been sufficient ground to prove it, assemblies seem to degrade in time. Available testing methods for bonding strength are destructive. Bond quality seems to fluctuate as well. In some cases, slight colouration, from white to brownish, of the PS substrate was detected. The preliminary assumption is that some thermal degradation of the PS occurs. Though the decrease in bonding strength does not seem problematic, this effect should be investigated to bring the process up to the industrial level.



Some mechanical issues have not been explained yet. The moment of impact seems to strongly influence the strength of the bond. This can be explained because the temperature of the Si part drops quickly after impact of the part on the substrate. Parasitic contact during placement influences this process due to a strong decrease in temperature. Placement speed seems the parameter to investigate. This research should be prioritised before industrialisation.

4.9 Alternative Substrate material

In order to have at least one additional option as a substrate material, PET-G was tested for bonding characteristics. PET, the same material as used for recyclable bottles, has higher temperature stability than PS. Given the colouration of the PS, less thermal degradation was expected, which



would overcome the problem of degradation. PET, being a transparent material also enables inspection from the backside of the substrate. In this way, information about material flow and air inclusions can be gathered.

Results of the PET bonding tests were substantially better than for PS:

- The parameters that were optimized for PS, appeared to work for PET as well, though the heat infected zones around the dies seem smaller. Expectations confirm that PET can withstand higher thermal load. No colouration of the PET was perceived;
- Bonding strength was substantially higher, up to the point that the parts were mechanically hard to remove from the substrate;
- Neighbouring parts do not seem to suffer from the heat infected zones of the previously bonded part;
- Little difference was seen with varying size and thicknesses of the different parts. Even the substantially thinner EPFL Die could be bonded with same settings.

4.10 Placement test

- Process seems feasible; reliable bond;
- Placement is still done semi automated → small errors in placement → adding computer-vision system;
- Machine has been characterised.

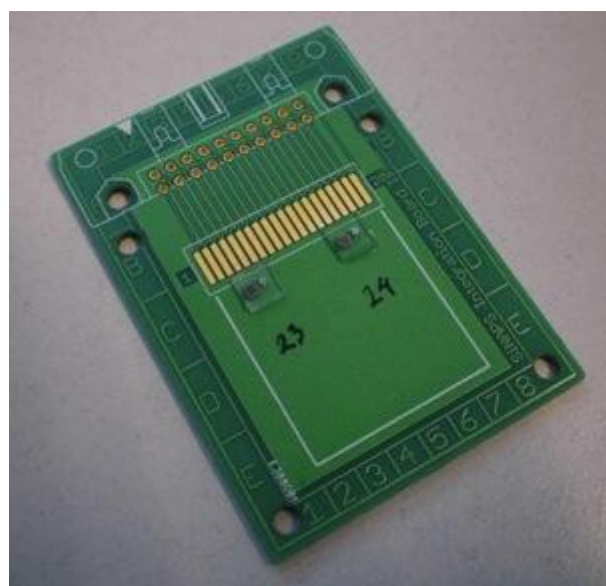


Charging and Sensing demonstrators for Issue 2

4.11 External interconnection

For the interconnection to the outside world, the Issue 1 Printed Circuit Board (60 x 45mm) will be applied.

Equipment for testing will be connected through the wire bond pads and the connector on the PCB (connector not shown in picture).

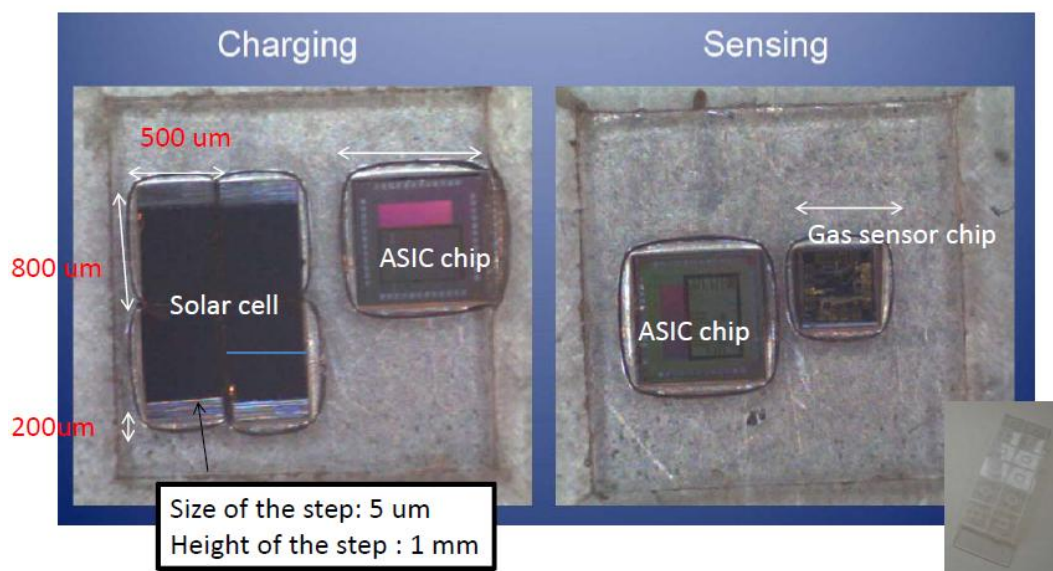


Using the Issue 1 Board for connections to the outside world. The secondary function of the board is to

enable easy handling while the functional testing is done. It protects the fragile wire bonds and dies while on the test bench

5 Feasibility Tests of the Wire Bonding Process

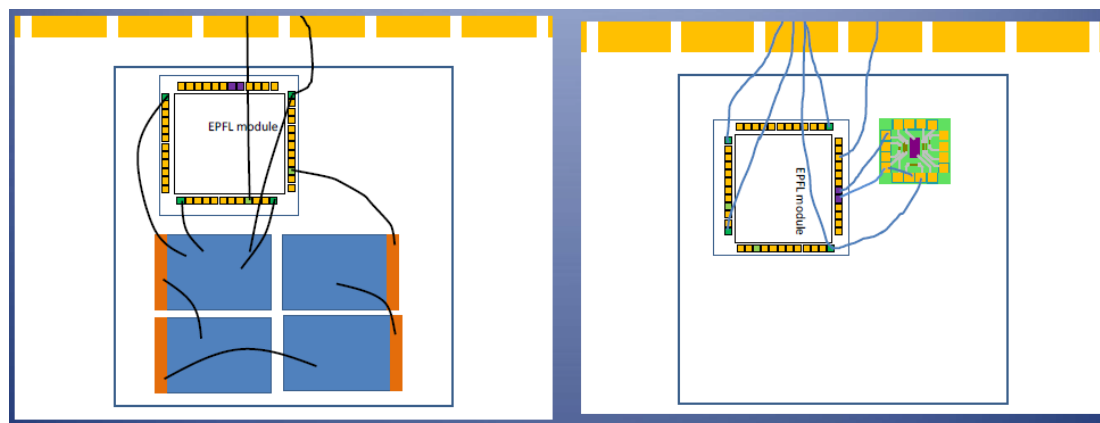
Combining the issue 1 board and Issue 2 dies the wire bonding of the sensing and charging modules was attempted and tested. Two modules were created as shown in the figure below. The figure on the left is the charging module and the figure on the right is the sensing module.



Charging module (left) and Sensing module (right) Substrates

5.1 Wire Bonding Schematics.

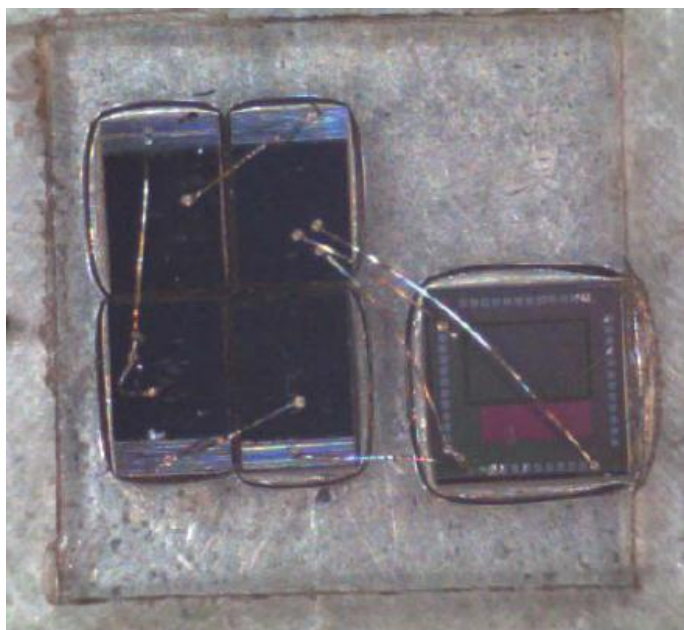
Wire bonding schematics for the charging and sensing module are shown in Figure 3. The wire bonding schematics were defined as per the chip layout design given by EPFL and Nanosens. E.g. the solar cells were connected in series and the “Lo” (p-type – top TCO layer) was connected to the ground of the EPFL chip as shown in the Figure below. For the sensing chip as shown in Figure, the reference NW and sensing NW were connected with one of the contacts grounded to “Lo”. For future use, the in-situ temperature sensor on the Pd NW chip could be used to calibrate and sense temperature changes on the chip.



Wire bonding schematics of the charging module. Right, wire bonding schematics of the sensing module

5.2 Wire bonding the Charging Module

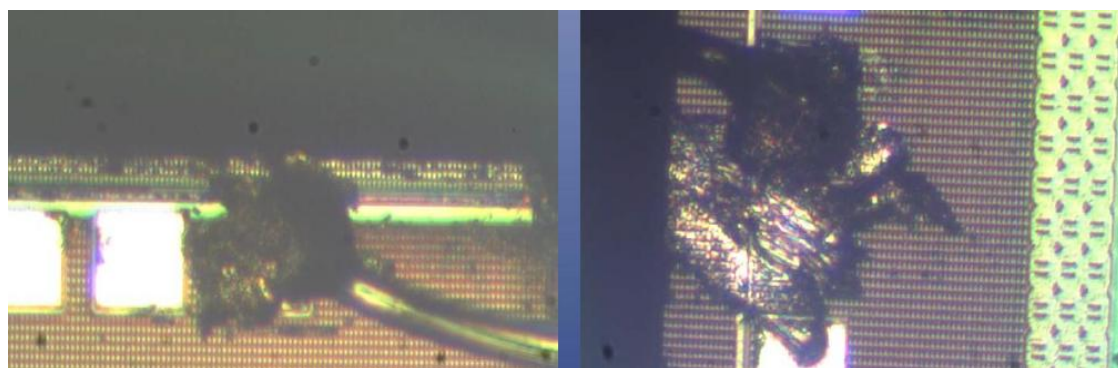
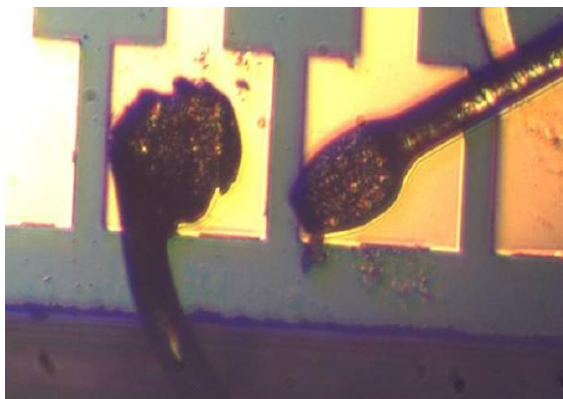
For the charging module, consisting of the solar cell and EPFL chip, the bonding on the solar cells chips were made after repeated attempts. This is shown in figure at the right. Wire bonding improved after cleaning with acetone-IPA and increasing the power settings.



Prior to the wire bonding, the solar chips were subjected to cleaning procedures by acetone. The cleaning procedure was not so rigorous as the traditionally followed at IPHT (Jia Guobin). Normally, he subjects the cleaning of the solar cells to acetone and Isopropylalcohol (IPA) for 10 minutes [followed by a 1~2 sec dip in diluted HF (2%) and rinsing in deionized water direct before the wire bonding (recommended)]. Wire bonding attempts from the solar cells to the EPFL chips were not successful because the contact pads on the EPFL chip were too small for the 32-micron bond wire. The Al EPFL bond pads have a size of 69x69 micron. The footprint of a bonded wire is typically 2,5 times the wire thickness.

5.3 Wire bonding the Sensing Module

For the sensing module, it was a combination consisting of the Pd Nano-wire chip and the EPFL chip. While the wire bonding for Pd sensing chip works, the wire bonding could not be applied on EPFL chip. The Pd NW chips had Au contact pads and the size of the pads was quite large (150 μm , figure right). The smaller pad size of the EPFL chips gave the same problems as the charging module (figure below).



Contact pads and wirebonding on the EPFL chip

5.4 Physical Adhesion of the Dies

None of the modules that were wire bonded came off the substrate during the bonding process. The modules thermally bonded onto the PET substrates were able to withstand the high power and force settings used for wire bonding.

Wire bonder settings used at IPHT:

	Normal settings	Settings used for
Power	400	800
Force	250	450

5.5 Conclusions of the Wire Bonding Tests

Based on the wire bonding tests the following conclusions were drawn:

1. Connection between the parts and the PET substrate appears sufficient.
2. Bonding is reliably possible with PET as a substrate.
3. Bonding on PV cells remains tricky but is possible using 32 μ m aluminum wire and doubled bonding force and power.
4. Bonding on the EPFL chip is very weak and must be considered not feasible with the 32 μ m aluminum wire (also no-chain bonding possible).
5. Bonding on the Pd Nano-wire chip is feasible.

5.6 Solution and Workaround to the Wire Bonding Process

So far, the wire bonding has only been partially successful due to the following difficulties:

1. The EPFL Dies need to be wire bonded with thin Au wire;
2. It is unsure if this needs to be a hot process;
3. It is unsure if the PV cells can be wire bonded with Au wire, but expectations are low. No successful reference is found in literature.

5.6.1 Workaround for the Issue 2 Sensing Demonstrator

This solution is straightforward, the sensing demonstrator will be realised with the Au wire bond process. Tests if this is possible, and if the substrate really needs to be heated will be planned.

5.6.2 Workaround for the Issue 2 Charging demonstrator

The charging demonstrator will be realised with the Al bond process. The PV cells will be bonded to the Au PCB substrate using the soft Al wire at IPHT. The EPFL die will be bonded using Au wire to the PCB. Both will be connected using the PCB.

5.6.3 Solution for the fully functional device (Issue 2 and Issue 3)

For a fully operational system, the PV cell will need to be provided with a bondable Au layer. In discussion with IPHT the possibilities for this have been discussed in the recent past. The Priority on these discussions will be increased.

The goal still is to realise a fully operational demonstrator in the project.

6 Demonstrator Specifications

Quantity	Issue 2	Issue 3
<i>Dimensions in x-y plane [μm]</i>	<i>(+/-50 unless stated otherwise)</i>	
- External Substrate	5000 x 5000	2870 x 2870
- Effective Device	4300 x 3300	2530 x 2530
- PV Cell	1500 x 1000	1000 x 500
- Power Die	1700 x 1700	1525 x 1525
- Sensor	1000 x 1000	1000 x 1000
- Gap size	100	50
<i>Dimensions Thickness [μm]</i>	<i>(+/-25 unless stated otherwise)</i>	
- Substrate	1000 +/-50	1000 +/-50
- PV Cell	700	700
- Power Die	300	300
- Sensor	400	400
<i>Device Area [mm^2]</i>	<i>(+/-0,25)</i>	
- Substrate	25,00	8,24
- Device Area	14,19	6,40
<i>Device Volume [mm^3]</i> <i>(Bond Wire Height 0,200)</i>	<i>(+/-1,5)</i>	
- Including Substrate	47,50	15,66
- Without Substrate	26,96	12,16

Specifications of electronics circuit for Issue 2 & Issue 3	
Technology	Europractice UMC180nm
Active die area	670 X 370 μm^2
Chip Area, including pads	1525X1525 μm^2
Pad Size	69 X 69 μm^2
Pad-to-Pad distance	99 μm
Specifications of Varta V6HR as energy storage option	
Technology	NiMH battery
Nominal Operating Voltage	1.2V
Size	D: 6.8mm, H: 2.15mm

Energy Capacity	6,200 μ Ah
Peak Discharge Current	18mA
Cycle life	1,000
Specifications of TZ1053 as external wireless transceiver	
Supply Voltage	1-1.5V (NiMH-compatible)
Size	5x5mm ²
Current consumption during data transmission	3mA
Current consumption during data reception	2.8mA
Current consumption during standby time	5 μ A

7 Planning Towards Final Deliverable D4.5

	March (M32)	April (M33)	May (M34)	June (M35)	July (M36)	Sept (M38)	Oct (M39)
Realisation Sensing & Charging Demonstrator on PCB							
Testing Sensing Demonstrator							
Realisation Issue 2 & Issue 3							
Testing Issue 2 & Issue 3							