Public

FP7-ICT-2013- 10 (611146) **CONTREX**

Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties

Project Duration 2013-10-01 – 2016-09-30 Type IP

	WP no.	Deliverable no.	Lead participant
	WP6	**D6.1.2**	**ECSI**

CONTREX Training Delivery Report

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Issued by	**ECSI**
Document Number/Rev.	**CONTREX/ECSI/R/D6.1.2/1.0**
Classification	**CONTREX Public**
Submission Date	**2016-09-30**
Due Date	**2016-09-30**

Project co-funded by the European Commission within the Seventh Framework Programme (2007-2013)

History of Changes

ED.	REV.	DATE	PAGES	REASON FOR CHANGES
AM	0.1	2016-09-30	10	Initial version
KG	0.2	2016-09-30	23	Integrated training activities from D6.1.1 and consortium level training activities
WF, JF	0.3	2016-09-30	24	Update of the POLIMI courses and Intecs update
AM	0.4	2016-09-30	28	Update and integration of contributions
KG	1.0	2016-09-30	28	Final release

Contents

1 Introduction

This deliverable describes the CONTREX consortium training delivery. The consortium envisaged developing four types of training activities; they were undertaken by a set of CONTREX partners or individually by some partners:

- Specific training on tools and methods (prepared and delivered by individual partners or set of partners)
- Tutorial material
- Training courses
- Web training material comprising e.g. videotaped tool demonstrations, tutorials
- Consortium training (at workshops and conferences)

The document is organised as follows: Section 2 describes joint partner and consortium-level training activities, while Section 3 focuses on partner-level training activities.

2 Joint Partner and Consortium-Level Training Activities

2.1 DATE 2016 Tutorial

Virtual Platforms in the Internet-of-Things Era – State of the Art and New Perspectives

Date 2016 Monday Tutorial, March 14th, 2016

Smart embedded systems are the building blocks of the so-called Internet-of-Things (IoT). They communicate each other and interact with the physical environment. In embedded system design, it is well known that the software development effort has overtaken the hardware effort. Virtual platforms can address this mismatch by parallelizing software and hardware development. Verification and testing of applications based on IoT and smart embedded systems require a continuous evolution of virtual platform methodologies:

- the ever more powerful MPSoCs allow exploiting concurrency which must be handled in platform simulation;
- executing multiple applications on the same chip could lead to interferences and impact on extra-functional properties (e.g., time, power and temperature) which must be analyzed;
- new operating systems and hypervisors, for improved control of the system and for improved security and safety, must be ported and tested;
- smart systems are ever more connected with components or external environment with continuous-time behavior that must be simulated together with discrete-time models;
- interaction among systems is becoming a crucial aspect to be verified in a full realistic network scenario;
- integration of legacy RTL components into abstract virtual platform is desired to further reduce the time-to-market.

This tutorial gives insights into which changes to expect in new virtual platforms regarding efficient CPU simulation, analog-mixed-signal modeling, simulation of extra-functional properties and network simulation. Speakers are expert in such topics; they ported research ideas into successful tools and therefore they can provide a scientific and industrial perspective supported by real case studies. Researchers and practitioners learn how these changes can help to design tomorrow's embedded systems more efficiently.
The tutorial aims at explaining the following concepts:

- virtual platform concept and architecture
- execution and verification of embedded software by using virtual platforms
- simulation of extra-functional properties of embedded platforms
- simulation of analog-mixed-signal behavior in virtual platforms
- simulation of realistic network scenarios
- integration of legacy components in standard virtual platforms

Agenda and speakers

Session 1

14:30 Welcome and Overview (Kim Grüttner – OFFIS, Davide Quaglia – EDALab)

14:45 Introduction to virtual platforms: Embedded software development, debugging, analysis, and verification with virtual platforms supporting today's MPSoCs (Simon Davidmann – Imperas)

15:30 The notion of time in virtual platforms and extraction of extra-functional properties (Kim Grüttner – OFFIS)

16:00 Coffee Break

Session 2

16:30 Modelling complex analog and digital systems: COSIDE – The design environment for heterogeneous systems (Karsten Einwich – COSEDA)

17:15 Generation and integration of components into virtual platforms: RTL-to-TLM abstraction, simulation of analog components, network scenario, extra-functional properties (Davide Quaglia – EDALab)

18:00 End

Organizers:

Dr. Kim Grüttner
OFFIS – Institute for Information Technology, Germany
kim.gruettner@offis.de

Dr. Davide Quaglia
EDALab s.r.l. and University of Verona, Italy
davide.quaglia@edalab.it

For more details, see: https://www.date-conference.com/date16/conference/tutorial-m08

2.2 HiPEAC 2016 Conference Tutorial

Title: Virtual Integration Testing for Mixed-Criticality Systems under Consideration of Power and Temperature Constraints –A highly integrated Avionics and Payload Computing Use-Case

Organizers: Kim Grüttner (OFFIS, Germany), Eugenio Villar (University of Cantabria, Spain), William Fornaciari (Politecnico di Milano, Italy), Davide Quaglia (EDALab, Italy)

Modern Multi-Core System on Chips enable the implementation of new performance hungry applications that previously could not be realized on single core processors. Furthermore, they enable integration of many embedded applications on a single chip that have previously implemented on several devices. In addition, mixed-criticality systems, which integrate a mixture of safety and non-safety relevant applications on the same computer, aim to profit from these multi-core benefits. The main new challenges that arise for a mixed-criticality system implementation on multi-core architectures are unpredictable sources of interference between safety-relevant and non-safety-relevant applications. They originate from e.g. timing

anomalies due to shared resource usage, power and thermal induced coupling due to shared power supply nets and high integration density.

To prevent the failure of such a highly integrated mixed-criticality system, the system engineer should be aware of any possible cross-application interferences with respect to timing, power and thermal properties as soon as possible in the design flow. For this reason, the extra-functional properties need to be modelled and analyzed at the system level, because they can strongly affect the overall quality of service (performance, battery lifetime) or even cause the system to fail meeting its real-time and safety requirements.

This tutorial addresses the challenges of power and thermal control of a mixed-criticality multi-rotor system in which a Xilinx Zynq MPSoC integrates safety-critical flight control and non-safety-critical high-demanding video processing. It covers new concepts of UML/MARTE based specification for mixed-criticality systems, the specification of platform properties (extra-functional model) as well as the dynamic capturing, processing, and extraction of power/temperature information during the simulation in a virtual platform. Furthermore, the presented concepts and tools will be applied to the design flow of the mixed-criticality multi-rotor system. In particular, the run-time optimization and management techniques to control the power consumption and waste heat discharge will be presented.

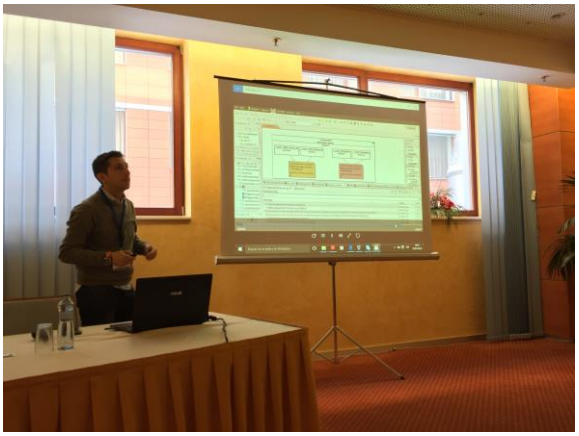
Covered topics: UML/MARTE for the design of mixed-criticality systems; MPSoC power and thermal simulation; Run-Time Resource Management; Multi-Rotor Avionics and Payload processing Mixed-Criticality MPSoC implementation; use of virtual platforms for verification.

Presentations and demos (with names of speakers):

1. Sören Schreiner (OFFIS, Germany): A Mixed-Criticality MPSoC Case-Study: The Multi-Rotor Avionics and Payload Computer System (30 min)
2. Fernando Herrera (University of Cantabria, Spain): UML/MARTE modelling for mixed-criticality systems (30 min)
3. Giuseppe Massari (Politecnico di Milano, Italy): Barbeque Run-Time Resource Management in Mixed-Criticality Systems (30 min)
4. Kim Grüttner (OFFIS, Germany): Virtual Integration Testing for Power and Temperature using Virtual Platforms (30 min)
5. Davide Quaglia (EDALab, Italy): Tools for Virtual Platform Integration Supporting Extra-Functional Properties (30 min)

For more information and proceedings:
https://www.hipeac.net/events/activities/7330/contrex/


Mixed-Criticality
Contrex
System components and their associated requirements have different "importance"
Modelling and Design has to be Mixed-Criticality




Contrex

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[3] K. Grüttner, P. A. Hartmann, T. Fandrey, K. Hylla, D. Lorenz, S. Stattelmann, B. Sander, O. Bringmann, W. Nebel and W. Rosenstiel: *"An ESL Timing & Power Estimation and Simulation Framework for Heterogeneous SoCs"*, International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS XIV), 2014

[4] P. A. Hartmann, K. Grüttner and W. Nebel: *"Advanced SystemC Tracing and Analysis Framework for Extra-Functional Properties"*, The 10th International Symposium on Applied Reconfigurable Computing (ARC), 2015

[5] Patrick Bellasi, Giuseppe Massari, William Fornaciari: Effective Runtime Resource Management Using Linux Control Groups with the BarbequeRTRM Framework. ACM Trans. Embedded Comput. Syst. 14(2): 39:1-39:17 (2015).

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[7] Simone Libutti, Giuseppe Massari, William Fornaciari *"Addressing Task Co-scheduling on Multi-core Heterogeneous Systems: An Energy-Aware Perspective"* HIPEAC Workshop on Energy Efficiency with Heterogeneous Computing (EEHCO), Jan. 19 2015, Amsterdam, The Netherlands

[8] F. Herrera, P. Peñil, H. Posadas, E. Villar *"Model-Driven Methodology for the Development of Multi-level Executable Environments"*J. Haase (Ed.): "Models, Methods and Tools for Complex Chip Design", Lecture Notes in Electrical Engineering, V.265, Springer. 2014-01

[9] F. Herrera, H. Posadas, P. Peñil, E. Villar, F. Ferrero, R. Valencia, G. Palermo"The COMPLEX methodology for UML/MARTE modeling and design-space exploration of embedded systems"Journal of Systems Architecture, V.60, N.1, Elsevier, pp.55–78. 2014-01

[10] Emad Ebeid, Franco Fummi, and Davide Quaglia, *"Model-Driven Design of Network Aspects of Distributed Embedded Systems"*, IEEE Transactions on Computer-Aided Design of IntegratedCircuits and Systems, vol. 34, n. 4, April 2015, pp. 603-614, DOI 10.1109/TCAD.2015.2394395.

[11] Parinaz Sayyah, Mihai T. Lazarescu, Sara Bocchio, Emad Ebeid, Gianluca Palermo, Davide Quaglia, Alberto Rosti, Luciano Lavagno, Virtual Platform-based Design Space Exploration of Power-Efficient Distributed Embedded Applications, ACM Transactions on Embedded Computing Systems, vol. 14, n. 3, April 2015, pp. 49:1-49:25, DOI 10.1145/2723161.

3 Partner-Level Training Activities

3.1 OFFIS E.V.

3.1.1 Specific training on tools and methods

OFFIS has trained Intecs on the usage of the Xilinx Zynq virtual platform through multiple video conferencing sessions. Content of the training:

- Usage of the Zynq virtual platform for software testing
- Integration of the Intecs telecom use-case on the Xilinx Zynq virtual platform
- Usage of the power and temperature models in the Xilinx Zynq virtual platform

OFFIS has trained UC on the HW/SW model of the multi-rotor demonstrator to represent it as a UML/Marte model. This training has been conducted through video conferences. Content of the training:

- Overview of the HW/SW architecture of the OFFIS multi-rotor system
- Code walkthrough of the flight control and video processing algorithms

3.1.2 Tutorial material

3.1.2.1 HiPEAC 2016 Conference Tutorial

OFFIS has prepared the following material for the HiPEAC 2016 tutorial (see Section 2.2):

1) Presentation slides and handouts "A Mixed-Criticality MPSoC Case-Study: The Multi-Rotor Avionics and Payload Computer System", available at https://www.hipeac.net/assets/private/events/subactivity/hipeac16_slides_sschreiner_final_unroll.pdf (HiPEAC login required)

2) Presentation slides and handouts "Virtual Integration Testing for Power and Temperature using Virtual Platforms", available at https://www.hipeac.net/assets/private/events/subactivity/contrex-hipeac16-tutorial-vit-power-temp_no_video_1HqCmOS.pdf (HiPEAC login required)

Video material use in this tutorial is available at the following YouTube channel: https://www.youtube.com/channel/UCnVUYR-FfD_zhhk1XbuGmJQ

- CONTREX Project Video: https://www.youtube.com/watch?v=udu-KPKbyKk
- CONTREX Project Video (with subtitle): https://www.youtube.com/watch?v=UJs6ZUwCHJs
- CAMeL-View - OVP Co-Simulation of a Quadrocopter: https://www.youtube.com/watch?v=Rjyj1YmtSBg

- OVP based virtual platform running video processing algorithm (object detection): https://www.youtube.com/watch?v=sdEdAwV1jbs

3.1.2.2 DATE 2016 Conference Tutorial

OFFIS has prepared the following material for the DATE 2016 tutorial (see Section 2.1):

Presentation slides and handouts "The notion of time in virtual platforms and extraction of extra-functional properties", available at https://www.date-conference.com/date16/system/files/private/date16/tutorials/DATE16-Tutorial-M08-Handouts.zip (DATE conference login required)

3.1.3 Training courses

OFFIS co-organized and participated at the following trainings:

- HiPEAC 2016 Conference Tutorial: Virtual Integration Testing for Mixed-Criticality Systems under Consideration of Power and Temperature Constraints –A highly integrated Avionics and Payload Computing Use-Case (see https://www.hipeac.net/events/activities/7330/contrex/)

- DATE 2016 Conference Tutorial: Internet-of-Things: Virtual Platforms in the Internet-of-Things Era – State of the art and perspectives (see https://www.date-conference.com/date16/conference/tutorial-m08)

3.1.4 Lectures & University Courses

3.1.4.1 Project Group Avionic Architecture

Course offered at: Carl von Ossietzky University Oldenburg
Course interval: It is offered every two years
Data of 1st pass: April 2014 – March 2015
Link: http://www.uni-oldenburg.de/avionic-architecture/

Figure 3-1 Project Group Avionic Architecture 2014/15

Organization:
Wolfgang Nebel - Carl von Ossietzky University Oldenburg
Achim Rettberg - Carl von Ossietzky University Oldenburg
Malte Metzdorf – OFFIS
Henning Schlender - Carl von Ossietzky University Oldenburg
Sören Schreiner – OFFIS

Description:

The master degree program in computer science of the Carl von Ossietzky University Oldenburg contains the obligatory visiting of a project group. This university lecture gives 6-12 students over 12 month an overview of performing a task in a best practice, industrial way. It covers state-of-the-art methods for planning, implementing and testing today's systems. The range of the task and amount of overall work is chosen by the number of students who are signed on the lecture. The lecture covers the following topics in detail:

- Phases of an industrial workflow
- Project management techniques
- Requirements engineering
- Process models
- Testing methods
- Implementation of a prototype
- Documentation and presentation

CONTREX related contents:

In the project group Avionic Architecture 12 students developed an avionics for a multi-rotor system, which is based on a Xilinx ZYNQ Multiprocessor System-on-Chip (MPSoC). The postulated result of the course was to get a stable flying system, which uses the processing power of the MPSoC not only for the flight algorithms but also for another performance needing on-board task. The students decided to implement an on-board video processing task. With the use of a 3-axes camera gimbal the camera tracks a coloured football, while the multi-rotor is flying and piloted remotely. In that way the students implemented an architecture for the used MPSoC, which is able to serve a mixed-critical system. In summary, the lecture covers the following project related contents:

- Methods to build architectures which are capable to process tasks of mixed-criticality
- Building a flying demonstrator
- Model-driven development
- Handling with extra-functional properties

3.1.4.2 Low Energy System Design

Course offered at: Carl von Ossietzky University Oldenburg
Course interval: It is offered every winter semester.
Date of 1st pass: October 2013 - February 2014
Date of 2nd pass: October 2014 - February 2015
Date of 3rd pass: October 2015 - February 2016
Link: http://www.uni-oldenburg.de/?id=35149

Organization:
Ralf Stemmer - Carl von Ossietzky University Oldenburg
Domenik Helms – OFFIS
Malte Metzdorf – OFFIS
Patrick Knocke – OFFIS
Lars Kosmann – OFFIS
Reef Eilers – OFFIS

Description:
This lecture gives an introduction to the topics of power estimation and power optimization for integrated circuits. During this course students will:

- get insight into the general problem of power dissipation (dynamic and static) and its main sources in today's transistor technology
- acquire a deep knowledge of requirements-driven design of embedded systems
- get knowledge of state-of-the-art power analysis and power optimization techniques
- get practical experience using design and analysis tools for power
- get practical experience with low power design flow

CONTREX related content:
Beside a general introduction of power estimation and optimization, the lecture presents CONTREX relevant topics:

- software-power estimation basics
- model generation and data abstraction techniques
- modelling and estimation of temperature for ICs
- modelling and estimation of reliability for ICs

3.1.4.3 System-Level Design

Course offered at: Carl von Ossietzky University Oldenburg
Course interval: It is offered every summer semester.
Date of 1st pass: April 2014 – July 2014
Date of 2nd pass: April 2015 – July 2015
Date of 3rd pass: April 2016 – July 2016
Link: http://www.uni-oldenburg.de/?id=35150

Organization:
Kim Grüttner – OFFIS
Philipp A. Hartmann – OFFIS
Ralph Görgen – OFFIS
Daniel Lorenz – OFFIS
Philipp Ittershagen – OFFIS
Maher Fakih – OFFIS
Ralf Stemmer - Carl von Ossietzky University Oldenburg
Henning Schlender - Carl von Ossietzky University Oldenburg

Description:
This master course extends the basic courses on embedded system that give an overview on the design of hardware/software systems. It covers state-of-the-art methods and tools for the design of today's systems. In a practical part, an introduction to SystemC is given, which is otherwise not covered in depth at the University of Oldenburg. Based on SystemC, the modelling of virtual prototypes at Transaction-Level is given. The course covers the following topics in detail:

- Phases of a System-Level Design Flow
- Refinement and Transformation of an initial specification towards a real implementation
- Current design methods and tools
- (Formal) Models of Computation used for specification and analysis
- Partitioning and parallelization of applications
- Evaluation and exploration of design decisions
- Modelling if system components and architectures based on system-level design languages (SpecC, SystemC)

CONTREX related content:
Besides a general introduction to system-level design in general, the lecture presents CONTREX relevant topics. Furthermore, project results are directly integrated into the lecture. In summary, the lecture covers the following project related content:

- Transaction-level modelling of applications and architectures
- Modelling and abstraction of extra-functional properties of a system
- Design-Space Exploration techniques and tools
- Virtual prototyping in SystemC

3.2 INTECS

3.2.1 Specific training on tools and methods

Context of training: Intecs worked together in particular with OFFIS in WP2, supplying the CHESS system, integrated with the OCRA tool and with the FoReVer extensions for contract specification associated with system components. The purpose was to integrate the existing work of OFFIS on structural contracts for structural reasoning. Intecs modelled power contracts in CHESS, thereby providing a validation context to be able to check for valid hardware component checking.

In online, hands-on training sessions, Intecs introduced OFFIS personnel to the CHESS technology and approach, including as well the FoReVer extensions and indications for application of the OCRA language.

These online training sessions were supplemented by subsequent follow-up support for specific questions arising during the work of integrating the structural contracts.

3.2.2 Tutorial material

The material used in the training described in the above section was based upon standard presentations of CHESS that are available in the CHESS project site (https://www.polarsys.org/chess/index.html) and through its membership in the Polarsys consortium (https://www.polarsys.org/), and therefore available openly to all. As mentioned above, this formal material was supplemented by hands-on demonstrations within the training sessions themselves.

3.2.3 Web training material comprising e.g. videotaped tool demonstrations, tutorials

There are videotaped demonstrations of the CHESS tool available in the CHESS project site; the user manual providing also demonstration of the CHESS tool capabilities is also freely available through its membership in Polarsys, together with examples of CHESS models.

3.3 iXtronics GmbH

iXtronics gave several trainings for the model based development for the members of the CONTREX consortium.

3.3.1 Specific training on tools and methods

The model based development training is performed with CAMeL-View. CAMeL-View is a design tool that facilitates the modelling, analysis and synthesis of mechatronic systems within a comprehensive development environment. It provides domain specific component parts, e.g. rigid bodies and joints. Systems are modelled on the physical level.

Mathematical equations are derived automatically, in case of multibody systems even based on the minimal representation, allowing the real-time processing of many technical systems. CAMeL-View automatically generates, compiles and links program code for analysis. In

addition to a variety of analysis techniques known from control engineering, CAMeL-View provides interfaces for third-party design tools.

CAMeL-View is composed of several modules, each providing a specific function. Part classes can be filed in and made available through catalogues. The modeller (Modelling Workbench) is used to create and modify models. It also allows the inclusion of measuring data. The analysis module offers non-linear simulation, linearisation of linear systems, and calculation of eigenvalues resp. frequency response. Other modules provide graphical visualization (3d animation, 2d plot) and support automatic documentation of models.

The model browser provides an easy way to modify parameters, select outputs to be visualized during simulation, and connect inputs to external data.

3.3.2 Tutorial material

The tutorial material for CAMeL-View is very extensive and consists of five main chapters:

Chapter 1: Modelling with Objective-DSS

- Elements of Language Definition in Objective-DSS
- Structure of the Refence Guide

Chapter 2: Structure of Objective-DSS Description Elements

- Model Classes in Objective-DSS
- Class Definition
- Interface Definition
- Parametrization (ParametrizationOdss)

Chapter 3: Mathematical Classes and Equations

- Definition of Variables
- Mathematical Operators and Evaluation Sequence
- Functions
- Assignments
- Access to Variables
- Conditioned Instructions and Code Blocks

Chapter 4: Part Metaclasses of Equation-Oriented Control Engineering Systems

- Nonlinear State Space Description (StateSpaceOdss)
- Linear State Space Description (LinearStateSpaceOdss)
- Linear Transfer Function (TransferFunctionOdss)

- Linear z Transfer Function (ZTransferFunctionOdss)
- Characteristic Curves and Look-Up Tables (Table2dOdss, Table3dOdss and TableNdOdss)
- Table2dOdss and Table3dOdss
- TableNdOdss
- C-Code description (CCodeElementOdss)

Chapter 5: Hierachical elements

- Topology diagrams (MechatronicHcsOdss)
- Block diagrams (MathematicHcsOdss)

3.3.3 Web training material comprising e.g. videotaped tool demonstrations, tutorials

The full version of CAMeL-View on the complete tutorial can be downloaded and performed on http://www.ixtronics.com/31/index.html

3.3.4 Consortium training (at workshops and conferences)

Trainings in CAMeL-View for the consortium were performed

- in Oldenburg within the technical consortium meeting,
- in Oldenburg for the Project Group Avionic Architecture (1st training)
- in Paderborn for the Project Group Avionic Architecture (2nd training)
- via telephone and online meeting for individual members of the CONTREX consortium.

3.4 INTEL

3.4.1 Specific training on tools and methods

The Intel Docea team regularly delivers hands-on and live support sessions to its customers. The team delivers no formal courses.

3.4.2 Tutorial material

The Intel Docea products (namely Intel® Docea™ Thermal Profiler, Intel® Docea™ Power Simulator and Intel® Docea™ Power Analytics) come with a full set of documents (user guide, quick start guide, technical notes…) and examples. This material is used to train new users and update existing ones with new features.

3.5 POLITECNICO DI MILANO

3.5.1 Specific training on tools and methods

PoliMi trained Vodafone on the N2Sim Node level simulator and BBQLite and EFP-Monitoring framework. Moreover, Polimi has trained OFFIS on the usage of BBQ-RTRM for the integration in the UC1.

3.5.2 Tutorial material

POLIMI has prepared the following material for the HiPEAC 2016 tutorial on "Barbeque Run-Time Resource Management in Mixed-Criticality Systems". (https://contrex.offis.de/home/images/downloads/hipeac2016/HIPEAC16_Tutorial_RTRM_v1.1.pdf)

3.5.3 Training courses

PoliMi participated at HiPEAC 2016 Conference Tutorial organized at consortium level at HiPEAC 2016 "Virtual Integration Testing for Mixed-Criticality Systems under Consideration of Power and Temperature Constraints" focusing on the run-time resource management part.

3.5.4 Web training material comprising e.g. videotaped tool demonstrations, tutorials

3.5.4.1 Online Training Material for BBQ-RTRM

The BBQ web page (http://bosp.dei.polimi.it/) offers training material for the usage and porting of BBQ run-time resource manager within applications and platforms. In particular, the following tutorials are relevant for CONTREX:

- BBQ: A quick start from source code to build.
- Run-Time Adaptivity and Monitoring Library
- Using MOST-DSE tool to characterize applications for Run-Time Management
- Cross-compilation for ARM multicore architecture
- Tutorial presented during HiPEAC 2016 Conference

3.5.5 Lectures & University Courses

3.5.5.1 Advanced Operating Systems

Course offered at: Politecnico di Milano
Course interval: It is offered every winter semester.
Date of 1st pass: October 2013- January 2014
Date of 2nd pass: October 2014- January 2015
Date of 3rd pass: October 2015- January 2016

Date of 4rd pass: October 2016- in progress

Level: MSc Level

Organization:
William Fornaciari – Politecnico di Milano

Description:
The goal of the course is to provide the necessary knowledge on design methodologies and tools necessary to develop system and application software for embedded applications. During the course some hands-on sessions will be to show how to put in practice the topics covered during the course. The goal is to make the students familiar with STM/ARM development boards provided by the lectures for the realization of small projects. Given their widespread availability, Linux and Android will be the reference for most of the examples. The course Advanced Operating Systems (AOS) focus on the development of the system and application software, including real-time aspects,

CONTREX related content:
- Application development for critical embedded systems
- Scheduling, Allocation and resource management
- Interfacing with sensors and accelerometers on STM/ARM platforms
- Usage of the Wireless sensor nodes developed at POLIMI, HANDS toolchain for extrafunctional property simulation and BBQ-RTRM

3.5.5.2 Embedded Systems

Course offered at: Politecnico di Milano
Course interval: It is offered every winter semester.
Date of 1st pass: October 2013- January 2014
Date of 2nd pass: October 2014- January 2015
Date of 3rd pass: October 2015- January 2016
Date of 4rd pass: October 2016- in progress

Level: MSc Level

Organization:
William Fornaciari – Politecnico di Milano

Description:
The goal of the course is to provide competencies and design methodologies tailored to realize embedded applications including the management of the design flow and the selection of the toolchain.
Such applications range from Cyber Physical Systems to industrial control; in general any consumer electronics product is an embedded systems. Their design requires the coordination of cross competencies to identify the optimal solution under a number of aspects including flexibility, standardization, cost, size, energy and power, performance, etc.
The course will provide and enhance the competencies regarding: architectures for PCB and SoC based embedded systems which currently are many-core and integrate MEMS sensors; communication and interfacing standard popular in the embedded system market, energy aware design of software and hardware, including run-time management of the resources.

Hands-on labs are proposed to the students (participation in optional) to show how to use STM/ARM development boards to interface external sensors and peripherals.

CONTREX related content:
- Building and using embedded HW platforms including extra-functional awareness
- Software Power Optimization for embedded systems
- Usage of HANDS toolchain for extrafunctional property simulation, BBQ-Run Time Resource Management, SWAT toolchain and MOST-DSE tool

3.5.5.3 Energy-Aware Computing

Course offered at: Politecnico di Milano
Course interval: It is offered every year.
Date of 1st pass: May-June 2014
Date of 2nd pass: May-June 2016

Level: PhD Level

Organization:
William Fornaciari – Politecnico di Milano
Giovanni Agosta – Politecnico di Milano
Gianluca Palermo – Politecnico di Milano
Carlo Brandolese– Politecnico di Milano
Davide Zoni – Politecnico di Milano

The course covers topics in energy aware computing, from the architecture, application design methodology and system software points of view. It aims at providing an holistic view of energy efficiency across the computing continuum, from ultra-low power embedded systems to low-power servers and green computing. Popular tools and flows will be also presented. Syllabus: (1) Introduction: motivations and topics overview; (2) Architectures: power/energy/thermal viewpoint; (3) Monitors and knobs, policies; (4) Software development; (5) Design Methodology; (6) RunTime adaptive management of resources; (7) Application case studies. The following in-house developed open source tools will be used: BBQ, SWAT, MOST, HANDS, PoliNode/Miosix, MEET, SDFA.

CONTREX related content:
- Energy-aware architecture design
- Energy-aware software development and optimization
- Energy-aware resource Management
- Usage of HANDS tool-chain for extra-functional property simulation, BBQ-Run Time Resource Management, SWAT tool-chain and MOST-DSE tool

3.6 POLITECNICO DI TORINO

3.6.1 Lectures & University Courses

3.6.1.1 Energy Management of Mobile Systems
Course offered at: Politecnico di Torino

Course interval: It is offered every year (1st semester).
Date of 1st pass: May-June 2014
Date of 2nd pass: May-June 2015

Level: Master Level

Organization:
Massimo Poncino - Politecnico di Torino
Sara Vinco - Politecnico di Torino

The course addresses the main issue involved in the design of energy-efficient electronic systems. The main learning outcomes of the course include:

- Understanding of the energetic issues of modern embedded mobile systems;
- Analyzing the energy consumption sources and skills in the design of energy-reduction solutions.
- Evaluating quantitatively the effectiveness of the design solutions;
- Understanding of the fundamental features of non-fixed power supply sources such as batteries, fule cells, photovoltaic cells or scavenging-based sources.
- Skills in the design of power supply systems

The course covers the following specific topics

- Technological and architectural trends and relative energetic implications
- Dynamic power management (DPM) and its variants applied to various types of components (cores, memories, devices)
- Other non-DPM based optimizations: information compression and coding;
- Quality/energy tradeoff in mobile systems: approximate and error-resilient computations
- Energy storage: types of energy storage devices (batteries, fuel cell, photovoltaic cells) and their relation with power management
- Energy generation: energy scavenging solutions and their energetic implications
- Energy conversion: types of converters and their efficiency.
- Simulation and design of the energy distribution sub-systems in an embedded device.

CONTREX related content:
The course presents many concepts that have been included in some CONTREX deliverables of WP3 and that have been tested during students' lab, in particular:
- development of battery models (including power conversion) and their validation
- SystemC/AMS simulation of an entire system (from power source to loads)
- IP-XACT modeling of system component interfaces.

3.7 UNIVERSIDAD DE CANTABRIA

3.7.1 Specific training on tools and methods

UC has provided training on the modelling methodology to the consortium in former internal meetings.

UC has generated specific training material for the single-source UML/MARTE modelling methodology, and for all the tools developed (CONTREX Eclipse Plug-in, VIPPE and CamelView Stub). The material has been developed as user-guides, as videos, and also in the

shape of pre-installed software and examples in virtual machines. Most of this material has been already used in specific events and training actions during CONTREX and it has been also made available on the web. Further details are given below.

3.7.2 Tutorial material

In CONTREX the documentation regarding the UML/MARTE modelling methodology has been re-structured. The documentation has been adapted to methodology enhancements (specification of periodic tasks, simplification of views, and adaptation of the specification for the DSE to a more standard style). The documentation has been enhanced with the extensions for Mixed-Criticality and for network modelling. Given the richness and extension of this documentation, a main achievement has been the restructuring; such there is an introductory document, a core document to introduce the modelling methodology, and then documents to describe the modelling for specific design activities, e.g. how to specify a DSE parameter for DSE. This material has been publically available within the UML/MARTE methodology website. Moreover, some small modelling examples have been developed for the introduction to the methodology (material to be published on the CONTREP website).

Regarding the CONTREX Eclipse Plug-in, UC has generated tutorial and training material based on the Quadcopter use case (due to the possibility to make this material open). This has been already used in tutorials and demos.

Regarding VIPPE, the main result is the VIPPE user guide, made available in the VIPPE website. A Virtual Machine has been also generated and used for training.

A Virtual Machine specifically oriented to the avionics use case (CONTREX UC1 VM) has been also developed. This CONTREX UC1 VM contains working installation of the UC tools used in the avionics use case, and other partner tools, e.g. MOST from PoliMi, integrated as back-end tools by CONTREP.

Figure 2. Login window of the CONTREX Use Case 1 Virtual Machine.

For the CamelView Stub, a specific and detailed manual has been generated and enabled to the partners internally to the consortium. This manual was accompanied with examples directly integrated in the examples folder of VIPPE. This material has served to enable OFFIS a successful connection between the OVP-based model of the quadcopter controller with the of the physical model of the quadcopter and of its environment in CamelView (OFFIS only required one e-mail to clarify the supported platforms).

3.7.3 Training courses

UC introduced the UML/MARTE model of the Quadcopter (use case 1a) to OFFIS in a F2F meeting (Hipeac'16).

UC has provided training to GMV on the UML/MARTE methodology, on CONTREP environment and on the VIPPE tool via several telcos abd webconf. meetings (relying on the updated versions of the CONTREX Virtual Machine). This has been crucial for the remote but tight collaboration between the use case 1 partners.

UC has shown the generation of a VIPPE performance model from the Quadcopter UML/MARTE model and the validation of the performance requirements in a University Booth in DATE'16. For it, UC relied on the CONTREX UC1 VM.

UC has provided training to IRT-Saint Exupery, as they have signed a NDA with UC for trying and using VIPPE. They have been introduced to VIPPE tool in two telcos and in a webconf meeting by relying on a specific *VIPPE VM*.

3.7.4 Web training material comprising e.g. videotaped tool demonstrations, tutorials

UC has developed three new websites for the UML/MARTE methodology (http://umlmarte.teisa.unican.es), for the CONTREX Eclipse Plug-in (http://contrep.teisa.unican.es) and for VIPPE (http://vippe.teisa.unican.es). Final dissemination report (D6.3.4), provides the details on the home site content of this sites.

As mentioned above, UC has made publically available most of the developed training material so far in these sites.

Figure 3 shows the documentation page of the single-source modelling&design methodology site. The page let access to the introductory and core modelling guides, as well as the "design activity specific" documents. Thus, the site aims to make visible and accessible this information to the user also in a structured way.

Figure 4 shows the documentation page of the VIPPE tool. There, the VIPPE user guide can be download without restrictions. Moreover, information regarding related publications is given.

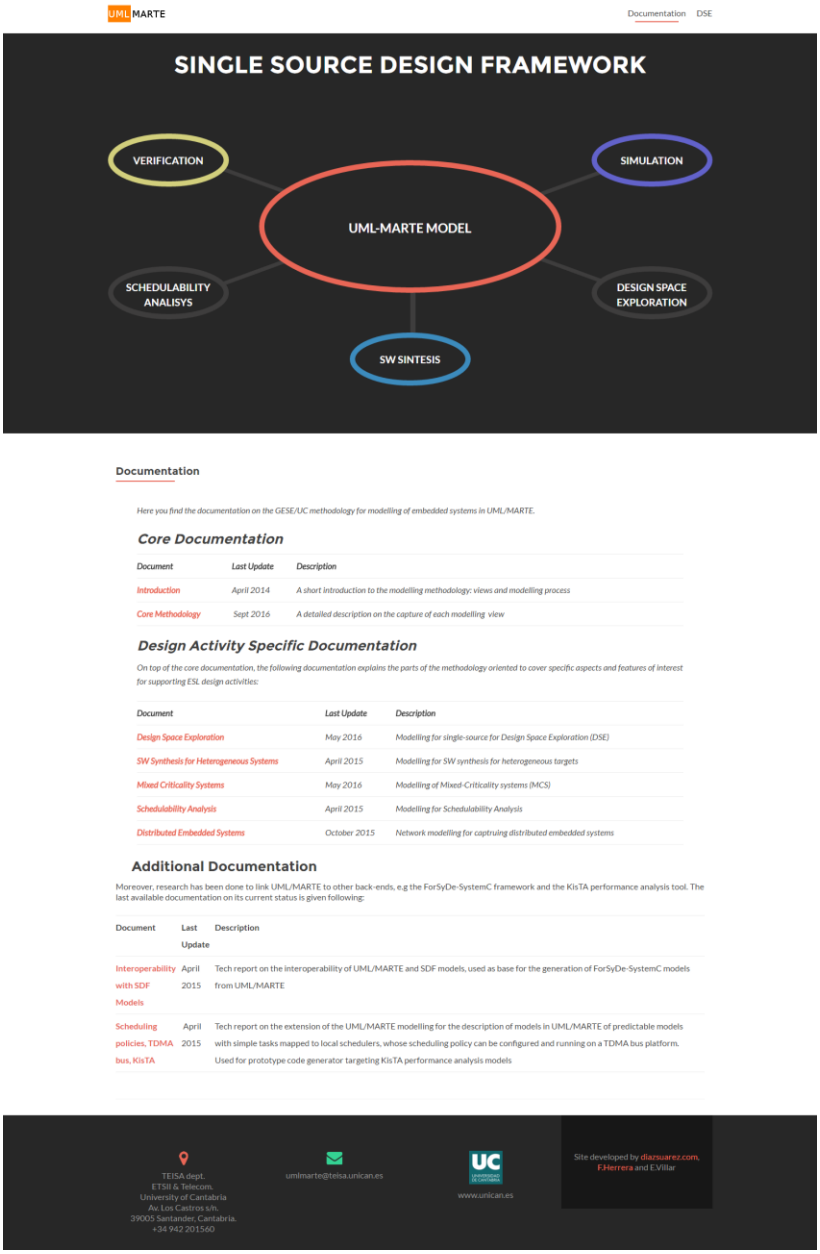

Figure 3. The documentation page of the single-source modelling&design methodology site of UC provides access to all the documentation on the UML/MARTE modelling methodology.

Figure 4 shows the documentation page of the CONTREP website. There, the material presented in HIPEAC'16 and in DATE'16 can be accessed. Among them, links to presented videos. The page also provides access to an additional set of videos showing how to use and exploit the tool.

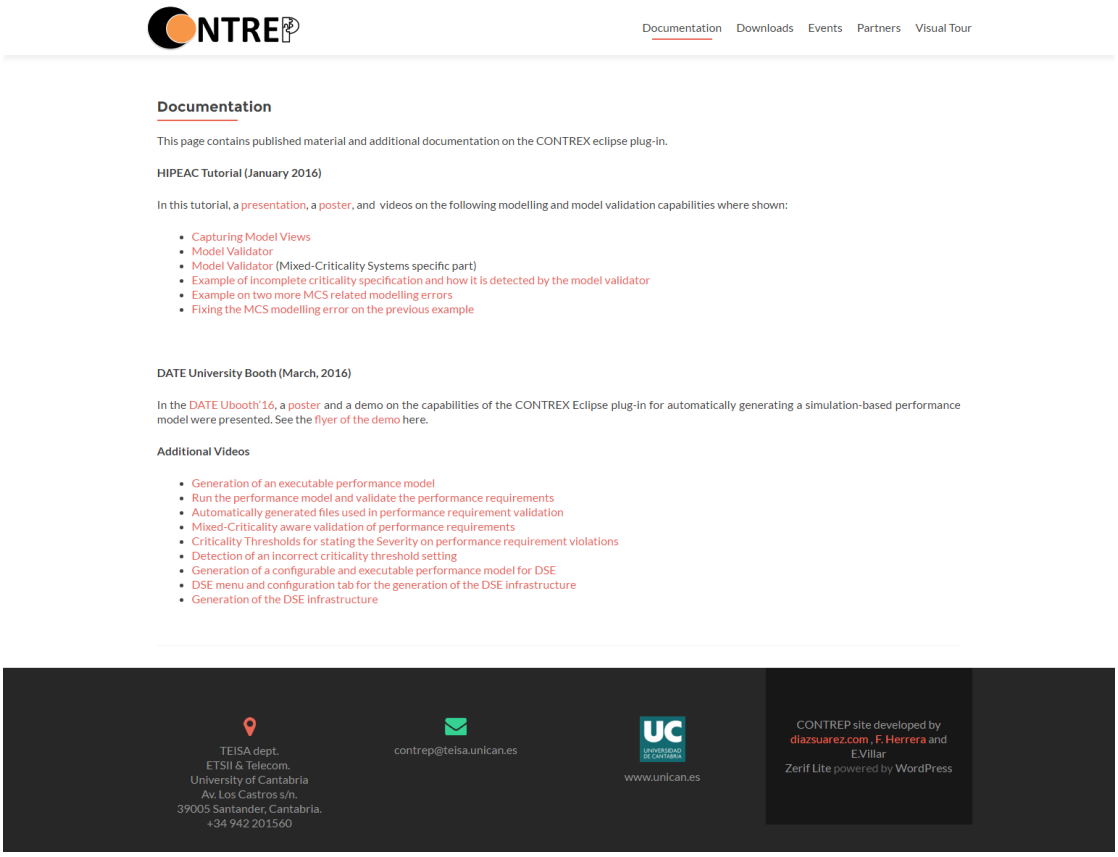

Figure 4. The download page of the CONTREX Eclipse Plugin in site enables accessing to the material presented in HIPEAC'16 tutorial, in DATE'16, and to additional material. Much of it is in the shape of tutorial videos uploaded to the Internet.

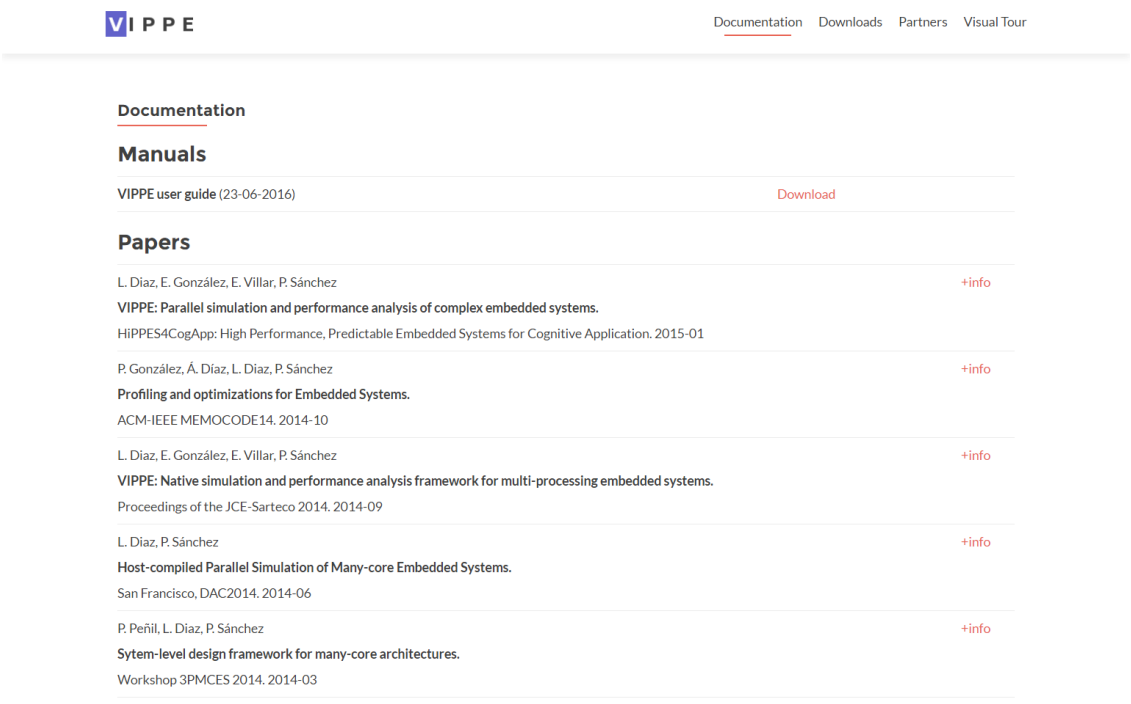

Figure 5 Excerpt of the documents page of the CONTREX Eclipse Plug-in website.

3.7.5 Consortium training (at workshops and conferences)

UC presented the modelling needs and the former version of the MARTE extension in the first MCS workshop of the project cluster in July, 2nd 2014 in Brussels.

In the second MCS workshop UC has participated by presenting the UML/MARTE modelling methodology.

UC also presented the UML/MARTE modelling methodology to the CONTREX partners in the Oldenburg technical meeting in December 2014, including the advances in CONTREX.

UC has shown the generation of a UML/MARTE model of the Quadcopter (Use Case 1a) and the model validation features of CONTREP in a tutorial in HIPEAC'16.

Prof. E. Villar gave a tutorial entitled "Electronic System Modeling, Analysis and Design beyond Moore's Law: A forecast" in Nanoelectronics, Applications, Design & Technology Conference Highlights from CATRENE, PENTA, ECSEL and H2020 projects. Grenoble, France, 21-22th June, 2016. http://tima.imag.fr/sls/dtc .

3.7.6 Lectures & University Courses

Relying on the CONTREX results, UC has also developed training material for its Master and Degree courses. Being UC an academic partner, this training for students is considered exploitation, and so this is reported in D6.5.3.

3.8 KUNGLIGA TEKNISKA HOEGSKOLAN

3.8.1 Specific training on tools and methods

KTH has trained Intecs in using the SystemC modelling libraries for ForSyDe to be able to model parts of their use case in SystemC ForSyDe. The training has been conducted in two training sessions online using a web conference system, and by self-studies of the Intecs employees using the online tutorials of ForSyDe.

3.8.2 Tutorial material

The ForSyDe web page offers training material for the ForSyDe modelling libraries, which are available for the languages SystemC and Haskell. In particular the following tutorials are relevant for CONTREX and have also been used by Intecs inside the CONTREX-project:

ForSyDe-SystemC:

- Installation and Setup
- Synchronous MoC Tutorial
- Synchronous Dataflow MoC Tutorial
- Continuous-Time MoC Tutorial

ForSyDe-Haskell:

- Getting Started with ForSyDe tutorial: which is more suitable for beginners with more emphasis on modelling with shallow embedded ForSyDe.
- ForSyDe tutorial: with a more emphasis on deep embedded models.

All tutorials are available via the ForSyDe web page: https://forsyde.ict.kth.se

The tutorial on the analytical design space exploration tool (DeSyDe) is available at: https://github.com/forsyde/DeSyDe

Publicly available ForSyDe tools:

Several tools and their corresponding documentations are available at the ForSyDe github webpage: https://github.com/forsyde. For instance, ForSyDe shell provides a set of scripts to set up the ForSyDe SystemC ecosystem for the demonstrator applications and create a shell environment with the necessary commands: https://github.com/forsyde/forsyde-shell. All the tools are distributed as open source tools with a permissive license.

3.8.3 Lectures & University Courses

3.8.3.1 IL2206 Embedded Systems

Course offered at: KTH Royal Institute of Technology
Course interval: It is offered every winter semester.
Credits: 7.5 ECTS credits
Number of students: 100
Link: https://www.kth.se/social/course/IL2206/

Organization:
Ingo Sander – KTH Royal Institute of Technology
Kathrin Rosvall – KTH Royal Institute of Technology
Hosein Attarzadeh – KTH Royal Institute of Technology
George Ungureanu – KTH Royal Institute of Technology
Nima Khalilzad – KTH Royal Institute of Technology
Mohamed Tagelsir Mohamed Elhussein – KTH Royal Institute of Technology

Description:
The course IL2206 Embedded Systems is given at master level at KTH Royal Institute of Technology. The course addresses the design of embedded systems with a focus on real-time. The course has the following main topics:

- Embedded computing platform
- Memory system
- Inter-process communication
- Introduction to real-time systems
- Software acceleration

CONTREX related content:
Although the main objective of the course is to give an introduction to embedded system design, the course aims to provide the necessary information, why it is so difficult to design real-time systems with guaranteed performance on state-of-the-art processors and multi-processor. Special focus is put on the sources for unpredictability in the memory system (cache) and communication architecture (shared bus and shared memory). Thus the course gives the foundation for a more elaborate discussion of real-time software design in the follow-up course IL2212 Embedded Software.

3.8.3.2 IL2212 Embedded Software

Course offered at: KTH Royal Institute of Technology
Course interval: It is offered every spring semester.
Credits: 7.5 ECTS credits
Number of students: 50
Link: https://www.kth.se/social/course/IL2212/

Organization:
Ingo Sander – KTH Royal Institute of Technology
Kathrin Rosvall – KTH Royal Institute of Technology
Hosein Attarzadeh – KTH Royal Institute of Technology
George Ungureanu – KTH Royal Institute of Technology
Nima Khalilzad – KTH Royal Institute of Technology
Mohamed Tagelsir Mohamed Elhussein – KTH Royal Institute of Technology

Description:
The course IL2212 Embedded Software is a follow up course of IL2206 Embedded Systems and given at master level at KTH Royal Institute of Technology. The course addresses the design process of embedded software with a focus on real-time on multiprocessor architectures. The course has the following main topics:

- Classical real-time theory
- Models of computation
- Design space exploration for mixed-criticality systems
- Correct-by-construction software design

CONTREX related content:
The course IL2212 has a very strong relation to CONTREX and results of CONTREX are continuously integrated into the course. Currently the course contains lectures about the following CONTREX-related ongoing activities and results:

- Models of computation
- Analysis methods for synchronous data flow
- Design space exploration for mixed-criticality
- ForSyDe modelling
- Correct-by-construction software design based on ForSyDe