Public

FP7-ICT-2013- 10 (611146) **CONTREX**

Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties

Project Duration 2013-10-01 – 2016-09-30 Type IP

	WP no.	Deliverable no.	Lead participant
	WP6	**D6.3.4**	**ECSI**

CONTREX Dissemination Report (Final)

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History of Changes

ED.	REV.	DATE	PAGES	REASON FOR CHANGES
SR	0.1	2016-09-30	26	Initial version
KG	0.2	2016-09-30	33	Added OFFIS contribution
NK	0.3	2016-09-30	35	KTH updates
FH	0.4	2016-09-30	42	UC update
DQ	0.5	2016-09-30	44	EDALab update
JF	0.6	2016-09-30	44	Intecs update
KG, AA	0.7	2016-09-30	48	OFFIS and iXtronics update
MP, GP	0.8	2016-09-30	51	POLIMI and POLITO contributions added
KG	0.9	2016-09-30	51	CONTREX website statistics added
KG	1.0	2016-09-30	51	Final release

Contents

1 Introduction

This document summarizes all dissemination activities that were undertaken by the CONTREX project consortium as a whole and by each individual partner of the consortium in the last period of the project execution (it covers the period from the last dissemination report – period 1).

From the very beginning the CONTREX consortium initiated and carried out dissemination activities that were focused on increasing the visibility of project results, impact the most important standardization activities and industry adoption and in general gaining a world-wide interest about its progress and results.

This second phase was also used to work closely with running R&D projects with similar objectives and to establish common actions with them. Very concrete activities were done together with OpenES, and within the Mixed-Critacality Cluster with PROXIMA and DREAMS projects.

Having the above high-level objectives in mind a common presentations and posters were done at the most prominent conferences in the domain: DATE, FDL, DASIP, ESLsyn to name the most important.

One of the most important activities of CONTREX, in which several partners of the consortium were pro-actively involved was a series of very successful Forum Workshop at the DAC Conference (2014, 2015 and 2016) on System to Silicon Performance Modelling and Analysis. The success of this initiative was proven by the growing participation as well as by the number of top electronic companies' representatives participating to these events.

These initial activities created a very good basis for collaboration with other projects and for establishing relations with the community (research partners and potential industrial customers) of the CONTREX results.

2 Dissemination Impact Measures

In order to control the efficiency of all dissemination actions, the consortium has implemented the mechanism enabling to collect progressively the following information on each specific dissemination activity undertaken by the whole consortium or by group of partners or each partner separately. This will contain:

- Event name, authors, dates and place;
- Presentation and paper (pdf, bib);
- Target audience (listed in the Table 1 below)
- Measures of impact are the collected information associated to each scientific publication in order to maintain the traceability of the concerned paper. The measures of impact are listed in Table 2 (below).

This information will enable the consortium to understand impact of each activity, to take corrective actions or improve the dissemination.

2.1 Target Audience

For each dissemination action, the consortium will define the addressed target audience (initially planned and effectively participating in the training) according to the following classification:

Type	Domain	Main Targets
System Companies (Europe, WW)	Aeronautics / Aerospace	EADS / Airbus / Astrium / Thales / ThalesAlenia / Selex / GMV
	Automotive	OEMs
	Communication / Networking	Ericsson, NSN, Axis
Application developers	Aeronautics	Thales, ThalesAleniaSpace, Astrium
Subsystem Providers (Tier 1, Subsystems)	Aerospace	Thales Communication
	Automotive	Bosch, Continental, Valeo, Magneti Marelli, Melexis, …
Microelectronics	All domains	ST, Infineon, Intel, Freescale, Renesas
IP/VIP Providers	All domains	ARM, Imagination, Synopsys IP, Cadence IP
EDA / Tools	System / HW / SW	Magillem, Calypto, Agilent, NEC, Intel CoFluent, Big 3, Mirabilis, Wind River, Green Hills
Research	System / HW / SW	Relevant research / university (all Europe)

2.2 Measures of Efficiency

In order to estimate how useful the dissemination actions were, the CONTREX consortium will provide some measures with each training activity:

Dissemination Degree	Appropriate Means	Measures of Success	Qualification
General awareness	Domain-specific conferences	# Participants # Contacts established + qualification Follow up after the event / outcome	• Industry / Academia • Research, management, engineering • Info exchange / Cooperation
	Workshops, seminars	# Participants Participant profile	• Industry / Academia • Industry type, mngmt, engineering, research
	Articles	Publication type Estimated reach Citations	• Conf paper, journal, press article • Conf participation, edition
Education on concepts / solutions / tools	Training sessions	# Participants Participant profile Follow-up	• Industry: management/engineering • Academia
	Training material (e.g. web courses, videos)	# Downloads Geographical regions Domains .com, .edu	
	Hands-on Demos	# Participants Follow up	• Industry / Academia • Industry type, mngmt, engineering, research
Standardisation	• Cooperation in std bodies • Workshops	# Proposals submitted # Proposals adopted Workshop success	• Overall impact of proposal on final standard
Tool Adoption	Delivery / Install Training	# Installations / licenses / users # Trainings # Inquiries / maintenance / applications	• Usage: evaluation / production test / production, large deployment • Interactive / exchange

3 Consortium-Level Dissemination Activities

3.1 CONTREX Website

The CONTREX project website is available at http://contrex.offis.de

Figure 1: Screenshot of the CONTREX website

The Website provides information about the project, project related news, dissemination material, contact information and the required legal information.

The menu website of the website is as follows:

- Main
  - Project
    - Objectives
    - Work Packages
    - Consortium
  - News
  - Dissemination
    - Scientific Publications
    - Events
    - Deliverables
    - Training
    - European Mixed-Criticality Cluster

- Contact
- Imprint
- Impressum

Access statistics have been collected starting from April 2014.

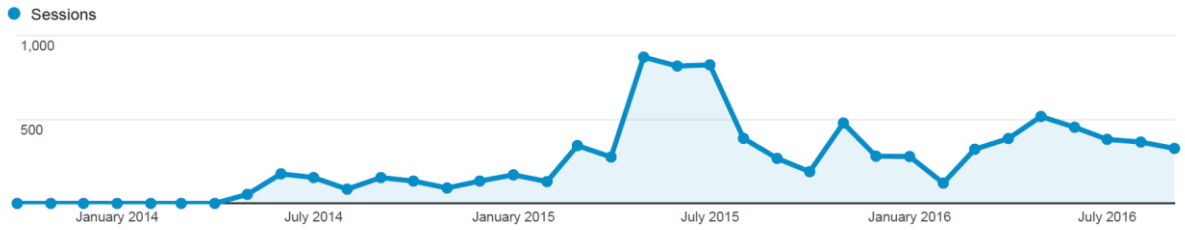


Figure 2: Number of Sessions over time

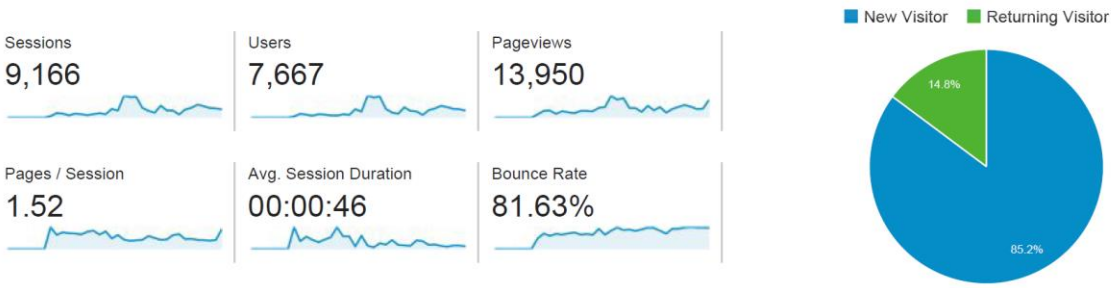


Figure 3: Advanced session statistics

	Country	Sessions	% Sessions
1.	Russia	1,697	18.51%
2.	United States	1,694	18.48%
3.	(not set)	964	10.52%
4.	Germany	885	9.66%
5.	Italy	478	5.21%
6.	United Kingdom	388	4.23%
7.	Spain	294	3.21%
8.	France	294	3.21%
9.	China	217	2.37%
10.	Japan	154	1.68%

Figure 4: Session breakdown per country

3.2 ESLsyn Conference 2015

Date & Location: June 10-11, 2015
San Francisco, CA, USA (co-located with DAC)
Organizer: ECSI

The still increasing need for enhanced productivity in designing highly complex electronic systems drives the evolution of design methods beyond the traditional approaches. To cover functional and especially non-functional requirements should be checked on a design model and covered during the design process.
Virtual prototyping, design space exploration and system synthesis with the goal of optimized and functionally correct product implementations are needed for designing both HW and SW parts. The system design teams expect newer and more efficient methods and tools supporting better management of the design complexity and reduction of the design cycle time all together, breaking the trend to compromise on the evaluation of various design implementation options. Designing at higher levels of abstraction is a viable way to better cope with the system design complexity, to verify earlier in the design process and to increase code reuse.
ESLsyn is a forum to discuss automated system design methods that enable efficient modeling of systems to provide the capability to synthesize HW platforms and embedded software with particular aspects related to synthesis. The main aim of the conference is to bring research institutions and industrial partners in the domain of ESL synthesis closer together by informing practitioners of the latest theoretical results, and challenging theoreticians with complex industrial problems. ESLsyn wants to provide a discussion platform for experience exchange between providers of synthesis technology and industry users, but also will be a forum to discuss scientific concepts and paradigms for the future evolution of synthesis methods. It therefore welcomes both academic and industrial participants.
The organizers are grateful to Forrest Brewer, Achim Rettberg, Yuko Hara-Azumi and Benjamin Carrion-Schafer for presenting their keynote and invited talks at ESLsyn 2015.
The organizing committee was also very grateful to the very large group of people that made this all happen: The 27 members of the technical program committee and their sub-reviewers. Finally, ESLsyn enjoyed the valuable support from the IEEE Council on Electronic Design Automation (CEDA).

Impact Assessment	
Target Audience	Industry and academia • Total participation: 24 • Industry: 10 • University/Research: 14
Participants	C-Lab, Calypto, Cornell University, Escuela Técnica Superior de Ingeniería Informática, Hella, National University of Computer and Emerging Sciences - Lahore, NEC, OFFIS, Politecnico di Torino, Tokyo Institute of Technology, U Lund, U Oldenburg, UC Santa Barbara, Université Nice Sophia Antipolis, Hong Kong Polytechnic University
Comments	• Presentation of CONTREX technical poster • Discussion around the poster, presenting the standardisation context

3.3 DAC Workshop 2015: System to Silicon Performance Modeling and Analysis

Date & Location:
June 7, 2015 – San Francisco, USA
Organizer: ECSI

Rationale for this year edition:
The integration of heterogeneous electronic systems composed of SW and HW requires not only a proper handling of system functionality, but also an appropriate expression and analysis of various extra-functional properties: timing, energy consumption, thermal behavior, reliability, cost and others as well as performance aspects related to caching, non-determinism, probabilistic effects.
The workshop addresses cross-domain aspects related to the design and verification framework covering methodology, interoperable tools, flows, interfaces and standards that enable formalization, specification, annotation and refinement of functional and extra-functional properties of a system. Special emphasis will be given to formalization and expression of ***power, temperature, reliability, degradation and aging***.
Several research and industry efforts address (parts of) the problem. However, there is a need for community-wide cooperation to establish a holistic vision on extra-functional property treatment, and to agree on research and development directions and further on validation of applicable solutions and standardization.
This event will support collaboration between main actors from system and microelectronics industry, EDA and research.
The workshop is inviting submissions of short abstracts industrial and scientific work in progress and practical solution and experiences.


Figure: The System-to-Silicon Performance workshop audience.

Impact Assessment	
Target	System companies, Microelectronics companies, Research centres, Universities, Standardisation
Audience	Aachen University of Technology, Airbus , Analog Devices, Inc., Broadcom Corporation, Cadence, Carnegie Mellon University, Chapman Consulting, Credit Suisse, CSR, CST AG, D. E. Shaw Research, DOCEA Power, Ecole Centrale de Lyon, EDXACT SA, ETRI, Faraday Technology Corp., FAU Erlangen-Nürnberg, Fraunhofer IIS, Friedrich-Alexander-Universität Erlangen-Nürnberg, Fudan University, Huawei Technologies Co., Ltd., IBM Corporation, Imagination Technologies Ltd., imec, Imperial College London, Infineon Technologies AG, Intel Corporation, iRoc Technologies, L-3 Communications, LEAT/CNRS, Leibniz University of Hannover, LG Electronics, Library Technologies, Inc., MediaTek, Inc., Mentor Graphics Corporation, Microchip Technology, Inc. , Micron Technology, Inc., National Security Research Institute, National Taiwan University of Science and Technolo, National Tsing Hua University, NC State University, Northeastern University, NVIDIA Corporation, Olympus, Oracle Corporation, Osaka University, Oticon A/S, Panasonic Corporation, Politecnico di Milano - DEIB, Qualcomm, RWTH Aachen University, Samsung Electronics Co., Ltd., Sasken Communication Technologies Ltd., Semiconductor Manufacturing International Corp., Seoul National University, Silvaco, Sk hynix, Sonics Inc., Spin Transfer Technologies, Stanford University, STMicroelectronics, Synopsys, Inc., Technische Universität München, The Aerospace Corporation, Toshiba Corporation, Trajectory Design Automation Corp., TSMC, TU Dortmund, UC Irvine, University Bremen, University of British Columbia, University of California at San Diego, University of California, Irvine, University of California, Santa Barbara, University of Illinois, University of Kaiserslautern, University of Texas at Austin, University of Virginia, Utah State University, Virginia Tech, Western Digital Corporation, Xilinx, Inc.
Participation profile	• Participants total: 123 registered, 60+ present constantly in the room • 59% Industry (!) • 39% Academia • 2% others (e.g. consulting)
Impact	• Presentation of CONTREX approach to the very wide audience, mostly from industry • Collaboration with related projects: PAPP, CRAFTERS, OPENES

3.4 FDL 2015

Date & Location:
September 13-15, 2015 – Barcelona, Spain
Organization: ECSI

Forum for Design Languages (FDL) is a well established international forum devoted to dissemination of research results, practical experiences and new ideas in the application of specification, design and verification languages to the design, modeling and verification of integrated circuits, complex hardware/software embedded systems, and mixed-technology systems. Several technical areas have been addressed:

- *UML and MDE for Embedded System Specification & Design (UMES)* – model driven methods, mostly based on the Unified Modeling Language, increasingly support semi-formal methods for system level design of complex embedded systems including highly programmable platforms and heterogeneous Systems-on-Chip.

- *Language Based System Design (LBSD)* – addresses language-based modeling and design techniques for simulation, debugging, transformation, and analysis of hardware/software embedded systems.

- *Assertion Based Design, Verification & Debug (ABD)* – welcomes research contributions, tool demonstrations, reports on standardization activities and effective applications in all aspects of innovative property expression and processing, with an emphasis on frontier design levels, verification, automatic synthesis and mechanized design aids.

- *Embedded Analog and Mixed-Signal System Design (EAMS)* – addresses design, modeling and verification of analog/mixed-signals systems.

Among industrial and academic participants, discussions on CONTREX project occurred during poster sessions and conference special sessions. CONTREX project had an accepted publication at FDL2015 conference, also a project poster was presented to give background information to the attendees on the project approach and results.

CONTREX presented (with the main implication of OFFIS and ECSI) technical posters displayed during the coffee/lunch breaks and during the poster session for discussion with all participants.

Impact Assessment	
Target Audience	Academia and industry in system design, microelectronics, embedded systems 50-60 participants HW platform + HdS community: Research partners + Infineon, Bosch, Continental, Cadence, Mentor Graphics, Synopsys
Impact	Established valuable contacts with industry partners: Continental, NXP, ST, Infineon
Comments	• Several valuable contacts with researchers working on system design methodology and design flows • Specific aspects like modelling, verification in the design methodology were addressed

3.5 DASIP 2015

Date & Location:
October 8-10, 2014 – Madrid, Spain
September 23-25, 2015 – Cracow, Poland
Organization: ECSI

The conference globally addresses the context of hardware design of complex applications for image and control processing, with the goal of presenting the latest results in the domain of design and architectures along several axes: design methods and tools, development platforms, architectures and technologies, use-cases and applications as well as smart sensing systems.

The Special Sessions have the purpose of introducing the DASIP community to relevant and new hot topics that are for sure of great interest for the audience of the conference, such as special arithmetic for signal and image processing, visual scene analysis for multi-core, many-core and hybrid architectures, or just-in-time compilation of architectures for image processing.
The Demo Night presented collaborative projects featuring timely topics on hardware platforms, prototypes, design frameworks, tools and more. We hope the format of demo night, held together with some refreshments, helps to maximize the interaction with the presenters. Also, the program has been defined to cover large number of domains. We also hope that all other sessions, with oral presentations and posters will lead to a large number of exchanges between attendees, helping not only on enhancing knowledge and research skills, but also on improving your links with other groups or individuals.

CONTREX took benefit of the event to present system design methodology relevant to the development of efficient architectures of complex signal and image processing that require analysis of various performance metrics to meet system requirement. Poster has been presented during several poster sessions all over the conference days.

Impact Assessment	
Target Audience	Academia and industry in system design, microelectronics, embedded systems 60-80 participants: EPFL, INRIA, Technische Universität Darmstadt, Åbo Akademi Universitu, Polytech'Nantes, Technische Universität München, Instituto de Microelectronica de Sevilla, Kalsruhe Institute of Technology, DGIST, Universita di Bologna, Tampere University of Technology, University of Twente, Polytechnique Montréal, Fraunhofer IOSB, Technical University of Denmark, INSA Rennes, AGH University of Science and Technology, Indian Institute of Technology, Bombay, E.T.S.I. INFORMÁTICA, IRISA, Leibniz Universität Hannover, Universaité Bretagne Sud, Université Paris Sud, University of the Basque Country, LIRMM, University of Arkansas, Universita degli Studi di Cagliari, ENSTA-Paristech, AGH University of Science and Technology, Tima Laboratory, Universidad CEU San Pablo, Instituto de Microelectronica de Sevilla, UPV, University of Sassari, Universidade do Porto, Centro de electronica Industrial.
Comments	• Several valuable contacts with researchers working on system design methodology and design flows • Specific aspects like performance analysis in the context of design methodology were discussed

3.6 DVCon Europe Conference & Exhibition 2015

Date & Location: November 11-12, 2015
Munich, Germany
Organizer: ECSI

DVCon Europe is a technical conference in Europe targeting the application of standardized languages, tools, and methodologies for the design and verification of electronic systems and integrated circuits. Hosted by Accellera Systems Initiative, the format of DVCon Europe is

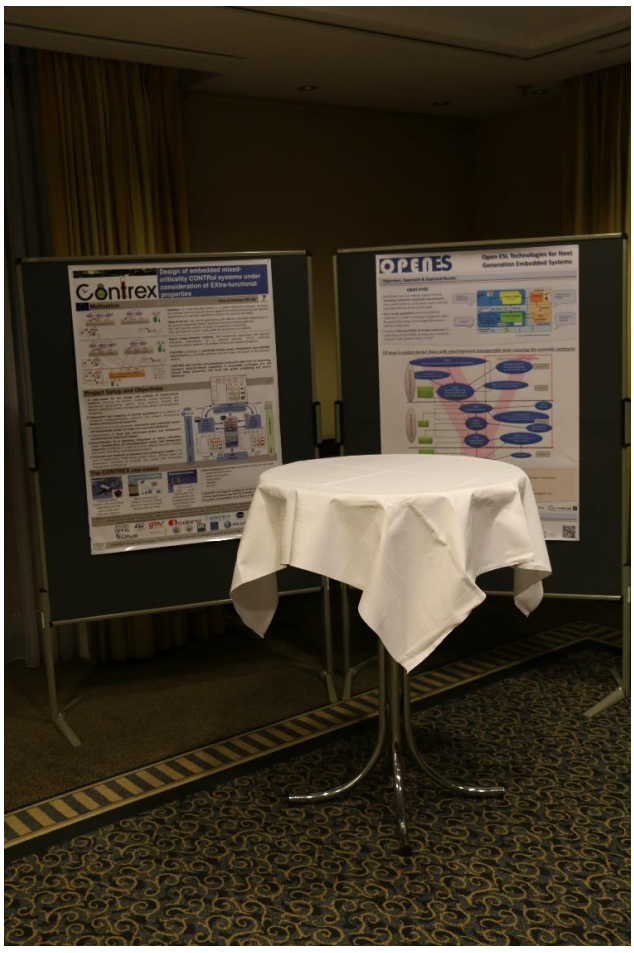
similar to the successful DVCon United States conference held for over 20 years in the Silicon Valley.
In order to boost the interest, usage and development of electronic design automation (EDA) and intellectual property (IP) standards in Europe, this highly technical conference is organized to invite industry experts to learn and share best practices on:

- The application of system-level design and verification languages such as SystemC, SystemVerilog or e
- The use of SystemVerilog Assertions (SVA) or the Property Specification Language (PSL)
- Verification methodologies based on the Universal Verification Methodology (UVM)
- IP reuse, automation and integration standards based on IP-XACT
- Low power design and verification using the Unified Power Format (UPF)

General topic areas on Electronic System Level (ESL), Verification & Validation, Analog/Mixed-Signal, IP reuse, Design Automation, and Low Power design and verification, will be highlighted in tutorials, papers, and poster sessions.
With a highly technical focus on System and IC design, verification, and integration, DVCon Europe is a very practical and industry-focused conference on EDA standards and standardization.
Conference attendees are primarily designers of electronic systems, ASICs and FPGAs, as well as those involved in the research, development and application of EDA tools and IP integration.

DVCon Europe 2015 welcomed more than 350 participants, managers and engineers from system and microelectronics industry. Also more than 25 exhibitors were present at the exhibition floor with leading EDA, IP and service providers.

CONTREX had a booth at the DVCon Exhibition together with three other projects in the domain: OpenES, CRAFTERS and PAPP.



Impact Assessment	
Target	System companies, Microelectronics companies, Research centres, Universities, Standardisation
Audience	ABILIS SYSTEMS, ACCELLERA, AEDVICES CONSULTING, AGNISYS, AIRBUS OPERATIONS, AIRBUS OPERATIONS SAS, ALTERA, AMIQ, AMIQ CONSULTING, AMIQ EDA, APPLIEDMICRO, ARM, BOOST VALLEY, BREKER SYSTEMS, CADENCE DESIGN SYSTEMS, CAEN SPA, CATENA RADIO DESIGN, CIRRUS LOGIC, CONTI TEMIC, CONTINENTAL AUTOMOTIVE, CONTINENTAL TEVES, COSIDE, COVERIFY, CREATIVE CHIPS, DIALOG SEMICONDUCTOR, DINI GROUP, DIZAIN-SYNC, DMOS GMBH, DOCEA POWER, DOULOS, ECSI, ERICSSON, ERICSSON AB, EVATRONIX, EXCELLICON, FRAUNHOFER AISEC, FRAUNHOFER IIS/EAS, FREESCALE, FUNDAÇÃO CPQD, HONEYWELL, HTV GMBH, IBM, INFINEON, INOVA SEMICONDUCTORS, INTEL, INTEL IND PVT LTD, ISYST GMBH, KALRAY, MAGILLEM, MAXIM INTEGRATED, MENTOR GRAPHICS, MICRONAS, MICROSEMI, NEST GROUP, NESTECH, NOKIA, NUMERIK JENA GMBH, NXP Semiconductors, OFFIS, ONESPIN / EVISION, ONESPIN SOLUTIONS, REAL INTENT / Europelaunch, ROBERT BOSCH GMBH, SEMIFORE, SIAE MICROELETTRONICA, SIEMENS AG , SIEMENS SRL, SOLVERTEC, SPANSION, STMICROELECTRONICS, SYNOPSYS, SYOSIL, TEXAS INSTRUMENTS, TVS, UNIVERSITY OF BREMEN, UNIVERSITY PADERBORN, UNIVERSITY SOUTHAMPTON, VERILAB, VITESSE SEMICONDUCTOR, WAFER SPACE, XILINX, ZIPALOG INC
Participation profile	• 2014 Participants total:250+, 2015: 350+ • >90% from industry • 83 companies represented • 21 exhibitors in 2014, expected 25+ in 2015
Impact	• Presentation of OpeES approach to the very wide audience, mostly from industry • Collaboration with related projects: PAPP, CRAFTERS, CONTREX

3.7 DATE Workshop 2016

Date & Location:
March 14-18, 2016
Dresden, Germany
Organizer: ECSI

CONTREX organized in cooperation with the related project OpenES the open workshop that enabled to present the advances on technical development on both sides. Also there were presentations of case studies, as well as tool implementations from Magillem and EDAlab.

The last part of the event was devoted to reflect and discuss on possible common continuation of the work that was initiated by CONTREX and OpenES. The conclusion was that definitely serval activities brought very promising resluts, but the community needs to continue the effort to put in place a coherent, complete and deployable solution based on approved standards.

System-Level Power and Temperature Specification, Modelling and Analysis

Organizers: Kim Grüttner (OFFIS, DE), Laurent Maillet-Contoz (STMicroelectronics, FR), Adam Morawiec (ECSI, FR)

With the predicted device, core and multicore scaling, a recent study revealed that regardless of chip organization and topology, multicore scaling is power limited. It has been predicted that at 22 nm, 21% of a fixed-size chip must be powered off, and at eight nm, even more than 50%. A system engineer should be able to plan the power intent and break is down to the different hardware resources. With regard to the software, a system engineer should be aware of any possible cross-application interferences with respect to timing, power and thermal properties, as soon as possible in the design flow. Power and temperature management shall be considered in conjunction with the application needs and platform capabilities. For this reason, power and temperature properties need to be modelled and analyzed at the system level, because they can strongly affect the overall quality of service (performance, battery lifetime) or even cause the system to fail meeting its real-time and safety requirements.

In this talk, we present our perspectives on the integration and usage of power and temperature models in SystemC and IP-XACT. This covers the specification of platform properties (extra-functional model) as well as the dynamic capturing, processing, and extraction of power/temperature information during the simulation. In particular, the following topics will be addressed:

- Modeling of extra-functional properties (especially power and temperature) in executable system-level models (ESL models)
- Estimation techniques to build/generate/annotate ESL models with extra-functional properties and extra-functional property models
- Expression of Power Management techniques on ESL
- Specification and monitoring of extra-functional properties
- Integration with relevant standards to support future interoperability of models: SystemC, IP-XACT
- Integration into industrial tools

Planned Program:

9:00 – 9:15	**Opening and Workshop Overview**
9:15 – 10:00	**OpenES Modeling Toolkit** *Laurent Maillet-Contoz (STMicroelectronics, France)*
10:00 – 10:30	**Case Study: IP-XACT Extensions for Safety-Critical Embedded Systems** *Ralph Weissnegger (CISC, Austria)*
10:30 – 11:00	Coffee Break & Exhibition
11:00 – 11:30	**Power State Machines: State-based System-level Power Estimation and Modelling** *Daniel Lorenz (OFFIS, Germany)*
11:30 – 12:00	**From RTL IP to Functional System-Level Models with Extra-Functional Properties** *Franco Fummi (EDALab, Italy)*
12:00 – 12:30	**IP-XACT Extensions for Extra-functional Properties** *Emmanuel Vaumorin (Magillem, France)*
12:30 – 13:30	Lunch & Exhibition
13:30 – 14:00	**Timed Value Streams: Tracing, Monitoring and Analysis of Extra-functional Properties in SystemC** *Kim Grüttner (OFFIS, Germany)*
14:00 – 14:30	**Timed Value Stream-based Power and Temperature Model** *Ralph Görgen (OFFIS, Germany)*
14:30 – 15:00	Coffee Break & Exhibition
15:00 – 15:45	**Discussion: Enhance Interoperability of Models and Tools by Upgrading and Extending Existing Open Standards (SystemC TLM, SystemC-AMS, IP-XACT)**
15:45 – 16:00	**Closing and Concluding Remarks**

This workshop is supported by the European projects OpenES (http://www.openes-project.org) and CONTREX (https://contrex.offis.de).

Impact Assessment	
Target Audience	• DATE audience from industry and academia
Comments	• Presentation of CONTREX technical content: keynote, case studies, tool implementation • Discussion/alignment with OpenES • Event though the event was open to external participation it was a working event between CONTREX and OpenES to better understand the technical solutions proposed by the two projects; a very good technical discussion continued through the entire day

3.8 DAC Workshop 2016: System to Silicon Performance Modeling and Analysis

Date & Location:
June 5-9, 2016
Austin, TX, USA
Organizer: ECSI

Rationale
The integration of heterogeneous electronic systems composed of SW and HW requires not only a proper handling of system functionality, but also an appropriate expression and analysis of various extra-functional properties: timing, energy consumption, thermal behavior, reliability, cost and others as well as performance aspects related to caching, non-determinism, probabilistic effects.
The workshop addresses cross-domain aspects related to the design and verification framework covering methodology, interoperable tools, flows, interfaces and standards that enable formalization, specification, annotation and refinement of functional and extra-functional properties of a system. Special emphasis will be given to formalization and expression of ***power, temperature, reliability, degradation and aging***.
Several research and industry efforts address (parts of) the problem. However, there is a need for community-wide cooperation to establish a holistic vision on extra-functional property treatment, and to agree on research and development directions and further on validation of applicable solutions and standardization.
This event will support collaboration between main actors from system and microelectronics industry, EDA and research.
The workshop is inviting submissions of short abstracts on industrial and scientific work in progress and practical solution and experiences.

Main topics
- Extra-functional property modeling (power, temperature, reliability, aging, …)
- Power and temperature analysis at SoC level: future needs and requirements
- Evolution and extensions of standards like UPF, IP-XACT to express extra-functional properties
- Power and temperature simulation and analysis at system-level
- System level reliability and aging models
- Reliability from transistor to RTL level: e.g. NBTI models including basic physical properties

Workshop Organizers:
- Laurent Maillet-Contoz, STMicroelectronics, France
- Kim Grüttner, OFFIS, Germany
- Gjalt de Jong, ArchWorks, Belgium
- Adam Morawiec, ECSI, France

Organized by R&D Collaborative projects:

DESIGN AUTOMATION CONFERENCE 52

ecsi

DAC 2016 Workshop on
System-to-Silicon Performance Modeling and Analysis
Power, Temperature and Reliability
Agenda

9:00 Welcome & Agenda
Adam Morawiec (ECSI, France)

9:15 Keynote 1: System Performance Modeling & Analysis in the Electronics Century
Eugenio Villar (University of Cantabria, Spain)

10:00 Session 1: System-Level Power and Temperature Specification, Modelling and Analysis
1.1 System-level Tracing, Monitoring and Analysis of Extra-Functional Properties
Achim Rettberg, (U Oldenburg & Hella AG, Germany)
1.2 Speed-Up in Design and Evaluation of Safety-Critical Systems based on UML-Profiles and IP-XACT (Case Study / Application Presentation)
Ralph Weissnegger (CISC Semiconductor, Austria)
1.3 Incremental Traceability Framework for Functional and Extra-Functional Properties in Embedded System Design
Emmanuel Vaumorin (Magillem Design Services, France)

11:00 Coffee Break

11:15 Keynote 2: Extra-Functional Properties Modelling Environment and Ecosystem
Laurent Maillet-Contoz (STMicroelectronics, France)

12:00 Keynote 3: Generic Multicore Enablement for Effective Programming
Andreas Herkersdorf (Chair for Integrated Systems, Technische Universität München, Germany)

12:45 Lunch

13:30 Keynote 4: Balancing the Effects of Process Variations, Aging, and Application Workload in Multi-Core Systems
Diana Marculescu (Carnegie Mellon University, USA)

14:15 Session 2: Ageing and Variation Effects Prediction
Organizers: *Christoph Sohrmann & Roland Jancke (Fraunhofer Institute for Integrated Circuits IIS, Germany)*
2. 1 Yield Analysis and Optimization of Full Custom Circuits considering Aging Effects
Michael Pronath (MunEDA, Germany)
2.2 Modeling Short and Long-term Effects of Aging from the Defect to Application Level
Victor M. van Santen, Hussam Amrouch and Jörg Henkel (Karlsruhe Institute of Technology, Germany)
2.3 NBTI Simulation for Aging of key Characteristics in Analog Circuits
Roland Jancke (Fraunhofer IIS/EAS, Germany)
2.4 Charge Trapping Phenomena in MOSFETS: From Noise to Bias Temperature Instability
Gilson I. Wirth (Universidade Federal do Rio Grande do Sul, Brazil)

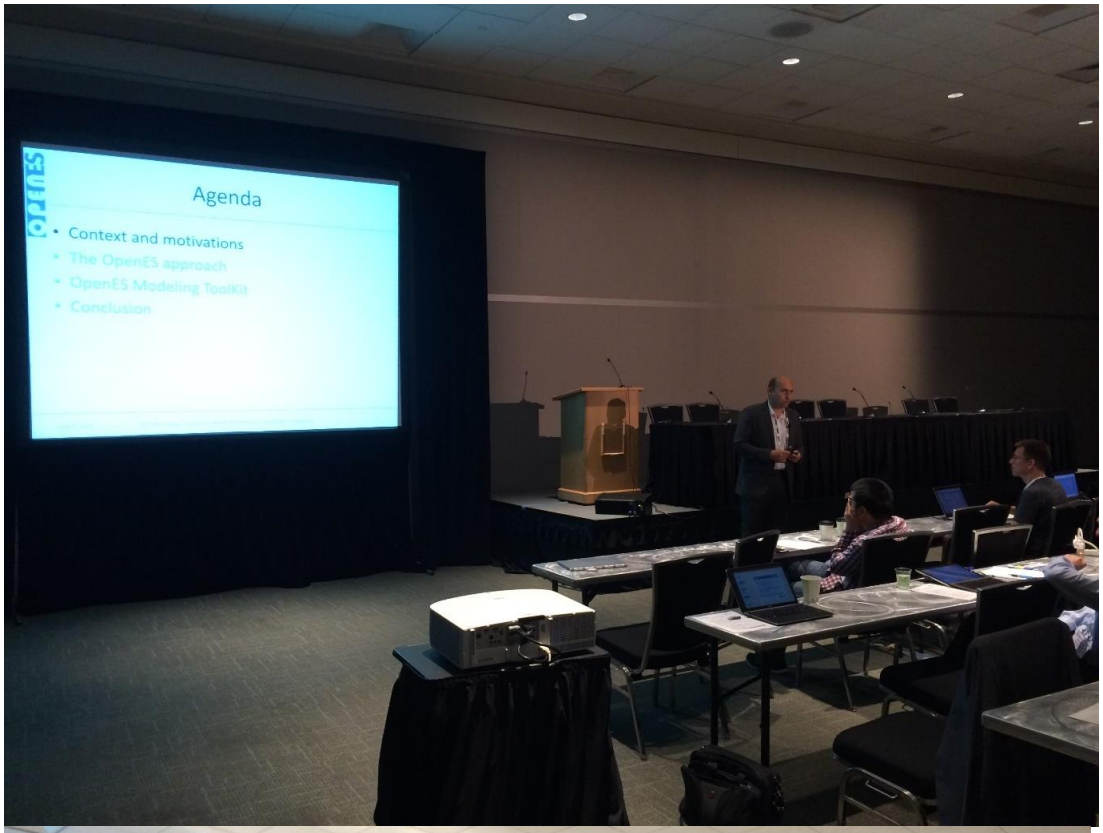
15:35 Coffee Break

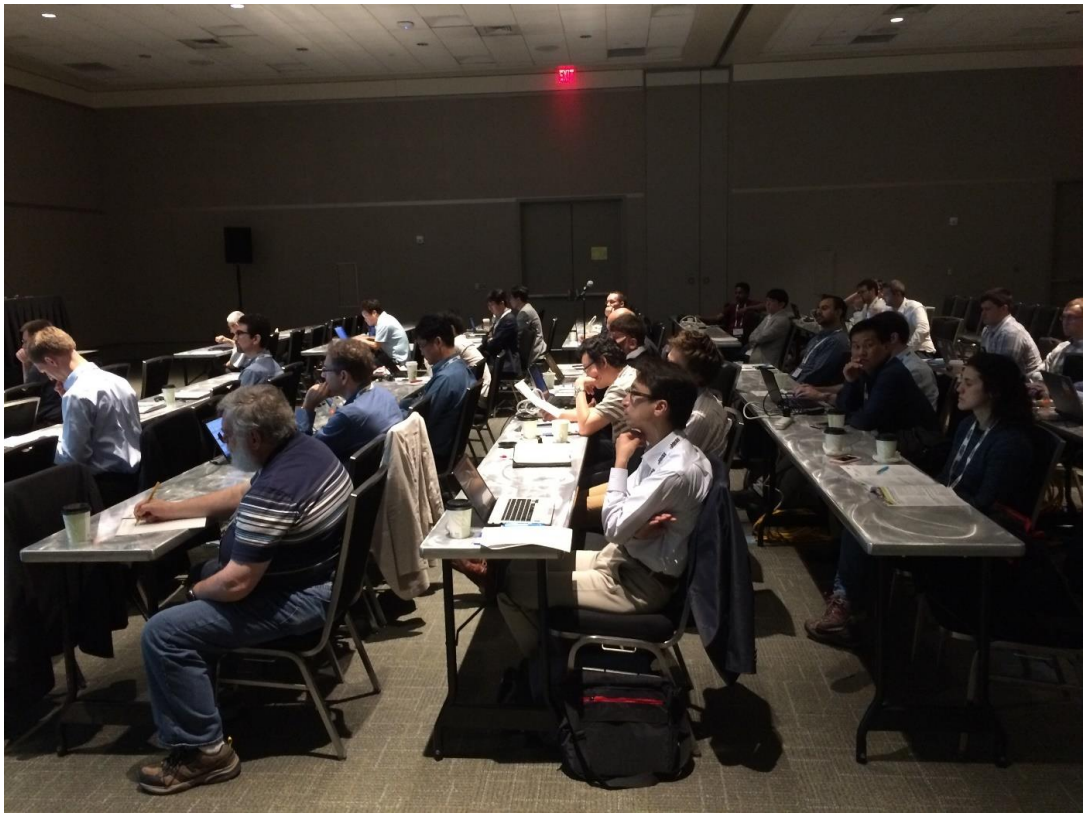
15:50 Session 3: Tool Support for Handling Ageing and Variation Prediction
3.1 Aging effects in Automotive Smart Power ICs
Roberto Stella (STMicroelectronics, Italy)
3.2 Modeling of Variability and Aging Effects Across Abstraction Layers
Adrian Evans (iROC Technologies, France)

16:30 End

Organized by R&D Collaborative projects:

Contrex OPENES


OpenES
Agenda
Context and motivations
The OpenES approach
OpenES Modeling ToolKit
Conclusion



Impact Assessment	
Target Audience	• DAC participants: world-wide industry and academia • System, Fab, Fabless, EDA, IP, research
Participation	• 45 registered people • +70 entering the room • Companies & organizations represented: Ajou University, ARM Ltd., Aurrion Inc., Carnegie Mellon University, CEA LIST, Cirrus Logic, Inc., Ericsson, Fraunhofer IIS/EAS, Graz University of Technology, Hella, iRoc Technologies, Karlsruhe Institute of Technology, Leibniz University of Hannover, LG Electronics, Marvell Semiconductor, Inc., MunEDA GmbH, Oracle Corporation, Qualcomm Technologies, Inc., Samsung Austin R&D Center, Samsung Electronics Co., Ltd., Seagate Technology, LLC, Socionext, Inc., Sony Corp., STMicroelectronics, SuZhou PowerCore Technology, Synopsys, Inc., Technische Universität München, UFRGS, University of Cantabria, US Department of Defense (DoD)
Comments	• Very good exposure to world-wide audience • Very strong industrial participation: Qualcomm, Samsung, LG, Sony, Ericsson, ARM, Marvell, Seagate, Cirrus… • One of the most prestigious places to organize the CONTREX Forum workshop at DAC • Third event in a series of workshops initiated, set-up and conducted by CONTREX • One of the best participation among all DAC workshops

3.9 FDL 2016

Date & Location:
September 14-16, 2016 – Bremen, Germany
Organization: ECSI

The Special Session has been proposed by the CONTREX project and accepted by the Programm Committee for FDL 2016 Conference:

System Performance Modeling & Analysis Based on Extra-Functional Properties
Chair : Adam Morawiec - ECSI

Abstract :
The integration of heterogeneous electronic systems composed of SW and HW requires not only a proper handling of system functionality, but also an appropriate expression and analysis of various extra-functional properties: timing, energy consumption, thermal behavior, reliability, cost and others as well as performance aspects related to caching, non-determinism, probabilistic effects.

The session addresses cross-domain aspects related to the design and verification framework covering methodology, interoperable tools, flows, interfaces and standards that enable formalization, specification, annotation and refinement of functional and extra-functional properties of a system. Special emphasis will be given to formalization and expression of power, temperature, reliability, degradation and aging. Several research and industry efforts address (parts of) the problem. However, there is a need for community-wide cooperation to establish a holistic vision on extra-functional property treatment, and to agree on research and development directions and further on validation of applicable solutions and standardization.

Contributions from CONTREX will be presented in this session.

Impact Assessment	
Target Audience	• Most prominent academia and industry participation in the area of languages for specification and design • Standardization
Participation	• ~ 80 participants • +70 entering the room
Comments	• Very good exposure to experts in language design, application, extensions • Very good academic and industrial participation •

3.10 CONTREX Book

The consortium is jointly working on a book containing the main technical results and their demonstration and practical explanation on the project's industrial use-cases. The book will be completed after the end of the project. The release is scheduled for the end of 2017. The book is organized as follows:

Proposed Title: Virtual Integration Testing for Mixed-Criticality Systems under Consideration of Power and Temperature Constraints

Abstract
Modern Multi-Core System on Chips enable the implementation of new performance hungry applications that previously could not be realized on single core processors. Furthermore, they enable integration of many embedded applications on a single chip that have previously implemented on several devices. In addition, mixed-criticality systems, which integrate a mixture of safety and non-safety relevant applications on the same computer, aim to profit from these multi-core benefits. The main new challenges that arise for a mixed-criticality system implementation on multi-core architectures are unpredictable sources of interference between safety-relevant and non-safety-relevant applications. They originate from e.g. timing anomalies due to shared resource usage, power and thermal induced coupling due to shared power supply nets and high integration density.
To prevent the failure of such a highly integrated mixed-criticality system, the system engineer should be aware of any possible cross-application interferences with respect to timing, power and thermal properties as soon as possible in the design flow. For this reason, the extra-functional properties need to be modelled and analyzed at the system level, because they can strongly affect the overall quality of service (performance, battery lifetime) or even cause the system to fail meeting its real-time and safety requirements.
This book addresses the challenges of power and thermal control of a mixed-criticality multi-rotor system in which a Xilinx Zynq MPSoC integrates safety-critical flight control and non-safety-critical high-demanding video processing. It covers new concepts of UML/MARTE based specification for mixed-criticality systems, the specification of platform properties (extra-functional model) as well as the dynamic capturing, processing, and extraction of power/temperature information during the simulation in a virtual platform. Furthermore, the presented concepts and tools will be applied to the design flow of the mixed-criticality multi-rotor system. In particular, the run-time optimization and management techniques to control the power consumption and waste heat discharge will be presented.

Proposed Structure

Chapter 1: Introduction
Main contributor: OFFIS
Storyline of the book (see storyline of CONTREX HiPEAC 2016 Tutorial https://www.hipeac.net/events/activities/7330/contrex/)

Chapter 2: UML/Marte for the specification, design and analysis of mixed-criticality systems
Main contributor: UC
Content: UML/MARTE extensions (mixed-criticality, power, temperature)

Chapter 3: Composition with guarantees for high-integrity component assembly in mixed-criticality systems

Main contributor: Intecs
Content: CHESS Tool (contracts for power)

Chapter 4: Platform power characterization, structural representation and platform generation
Main contributor: EDAlab
Content:

- PSM generation
- PSM IP-XACT representation
- VP configuration and generation

Chapter 5: Simulation based virtual integration testing for extra-functional properties in mixed-criticality systems on a single chip
Main contributor: OFFIS
Content:

- Zynq based VP
- Power model
- Temperature model

Chapter 6: Fast power and thermal simulation with SystemC-AMS [PoliTo]
Main contributor: PoliTo
Content:

- SystemC-AMS based thermal model
- battery model

Chapter 7: Run-time resources management
Main contributor: PoliMi
Content: BBQ-RTM

Chapter 8: Joint Analytical and Simulation-based Design Space Exploration
Main contributor: KTH, UC
Content: Mixed Analytical Simulative DSE

Chapter 9: Multi-Rotor Flight Control and Payload Processing on a Single Chip
Main contributor: GMV, UC, OFFIS
Main content: Multirotor demonstrator

Chapter 10: Automotive black-box with low energy event detection capabilities
Main contributor: Vodafone, PoliMi
Content: Telematics box

Chapter 11: Introduction of a virtual platform based validation and verification process for the development of critical telecom equipment
Main contributor: Intecs, OFFIS
Content: Telecom use-case

Chapter 12: Conclusion and outlook

4 Partner-Level Dissemination Activities

4.1 OFFIS

4.1.1 Publications

2016

- Kim Grüttner. In: "Model-Implementation Fidelity in Cyber Physical System Design" (to appear). Chapter: "**Empowering Mixed-Criticality System Engineers in the Dark Silicon Era: Towards Power and Temperature Analysis of Heterogeneous MPSoCs at System-Level**". Springer, 2016.

- Ralph Görgen, Kim Grüttner, Fernando Herrera, Pablo Penil, Julio Medina, Eugenio Villar, Gianluca Palermo, William Fornaciari, Carlo Brandolese, Davide Gadioli, Sara Bocchio, Luca Ceva, Paolo Azzoni, Massimo Poncino, Sara Vinco, Enrico Macii, Salvatore Cusenza, John Favaro, Raul Valencia, Ingo Sander, Kathrin Rosvall, and Davide Quaglia. "**CONTREX: Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties**". In: Euromicro Conference on Digital System Design (DSD). Aug. 2016.

- Sören Schreiner, Ralph Görgen, Kim Grüttner, and Wolfgang Nebel. "**A Quasi-Cycle Accurate Timing Model for Binary Translation Based Instruction Set Simulators**". In: 2016 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS). July 2016.

- Ralf Stemmer, Maher Fakih, Kim Grüttner, and Wolfgang Nebel. "**Towards State-Based RT Analysis of FSM-SADFGs on MPSoCs with Shared Memory Communication**". In: Integrating Dataflow, Embedded computing and Architecture (IDEA'2016). Apr. 2016.

- Sebastian Warsitz and Maher Fakih. "**Simulink-Modell-Übersetzung in synchrone Datenflussgraphen**". In: Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV'2016)

2015

- Philipp A. Hartmann, Kim Grüttner, and Wolfgang Nebel. "**Advanced SystemC Tracing and Analysis Framework for Extra-Functional Properties**". In: The 11th International Symposium on Applied Reconfigurable Computing (ARC'15). Apr. 2015.

- Henning Schlender, Sören Schreiner, Malte Metzdorf, Kim Grüttner, and Wolfgang Nebel. "**Teaching Mixed-Criticality: Multi-Rotor Flight Control and Payload Processing on a Single Chip**". In: Proceedings of the 2015 Workshop on Embedded and Cyber-Physical Systems Education (WESE). Oct. 2015.

- Sören Schreiner, Kim Grüttner, Sven Rosinger and Wolfgang Nebel. „**Ein Verfahren zur Bestimmung eines Powermodells von Xilinx MicroBlaze**

MPSoCs zur Verwendung in Virtuellen Plattformen“ In 18. Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV 2015). March 2015.

2014

- Domenik Helms, Kim Grüttner, Reef Eilers, Malte Metzdorf, Kai Hylla, Frank Poppen and Wolfgang Nebel**. “Considering Variation and Aging in a Full Chip Design Methodology at System Level”.** The 2014 Electronic System Level Synthesis Conference (ESLsyn'14), May 31- Jun 01 2014, San Francisco, CA, USA.

- Daniel Lorenz, Kim Grüttner and Wolfgang Nebel. **„Data- and State-Dependent Power Characterisation and Simulation of Black-Box RTL IP Components at System-Level“.** 17th Euromicro Conference on Digital Systems Design (DSD 2014).

- Gregor Nitsche, Kim Grüttner and Wolfgang Nebel. “**Towards Satisfaction Checking of Power Contracts in Uppaal**”. Forum on Specification and Design Languages 2014, October 2014, Munich, Germany.

- Kim Grüttner, Philipp A. Hartmann, Tiemo Fandrey, Kai Hylla, Daniel Lorenz, Stefan Stattelmann, Björn Sander, Oliver Bringmann, Wolfgang Nebel and Wolfgang Rosenstiel. “**An ESL Timing & Power Estimation and Simulation Framework for Heterogeneous SoCs**”. Proceedings of International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS XIV), Samos, Greece, July 14-17, 2014

- Sören Schreiner, Kim Grüttner, and Sven Rosinger. “**Autonomous flight control meets custom payload processing: A mixed-critical avionics architecture approach for civilian UAVs**”. In: Proceedings of the 5th IEEE Workshop on Self-Organizing Real-Time Systems. June 2014.

- Salvador Trujillo, Roman Obermaisser, Kim Grüttner, Francisco J. Cazorla, and Jon Perez. “**European Project Cluster on Mixed-Criticality Systems**”. In: Performance, Power and Predictability of Many-Core Embedded Systems (3PMCES) Workshop. Mar. 2014.

2013

- Philipp Reinkemeier, Philipp Ittershagen, Ingo Stierand, Philipp A. Hartmann, Stefan Henkler, and Kim Grüttner. “**Seamless Segregation for Multi-Core Systems**”. Technical Report OFFIS e.V., Aug. 2013. URL: http://ses.informatik.uni-oldenburg.de/download/bib/paper/OFFIS-TR2013_SegregationMultiCore_20130805.pdf .

4.1.2 Presentations at Conferences / Workshops

2016

- Kim Grüttner "**Design of embedded mixed-criticality systems under consideration of power and temperature**" EMC2 Project Conference, September 2016, Paris, France.
- Ralph Görgen "**Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties**" PATMOS & VARI 2016, European Project Session, September 2016, Bremen, Germany.
- Kim Grüttner "CONTREX project pitch" Collaboration Workshop Advanced Computing and Cyber-Physical Systems 2016, 14 June 2016, Brussels, Belgium.
- Achim Rettberg, Kim Grüttner, Daniel Lorenz, Ralph Görgen. "**System-level Tracing, Monitoring and Analysis of Extra-Functional Properties**" System-2-Silicon Workshop (S2S'16) at DAC 2016, June 2016, Austin, TX, USA.
- Kim Grüttner, Ralph Görgen. "**Analysis of Power - Measurement, Simulation, and Composability**" IMPAC: Getting more for less: Innovative MPSoC Architecture Paradigms for Analysability and Composability of Timing and Power, DATE Friday Workshop, March 2016, Dresden, Germany.
- Daniel Lorenz. "**Power State Machines: State-based System-level Power Estimation and Modelling**" OpenES & CONTREX Projects Workshop: System-Level Power and Temperature Specification, Modelling and Analysis, DATE, March 2016, Dresden, Germany.
- Kim Grüttner. "**Timed Value Streams: Tracing, Monitoring and Analysis of Extra-functional Properties in SystemC**" OpenES & CONTREX Projects Workshop: System-Level Power and Temperature Specification, Modelling and Analysis, DATE, March 2016, Dresden, Germany.
- Ralph Görgen. "**Timed Value Stream-based Power and Temperature Model**" OpenES & CONTREX Projects Workshop: System-Level Power and Temperature Specification, Modelling and Analysis, DATE, March 2016, Dresden, Germany.
- Kim Grüttner "**The notion of time in virtual platforms and extraction of extra-functional properties**" DATE Tutorial: Internet-of-Things: Virtual Platforms in the Internet-of-Things Era – State of the art and perspectives, March 2016, Dresden, Germany.
- Sören Schreiner. "**A Mixed-Criticality MPSoC Case-Study: The Multi-Rotor Avionics and Payload Computer System**" CONTREX Tutorial: Virtual Integration Testing for Mixed-Criticality Systems under Consideration of Power and Temperature Constraints, HiPEAC 2016 Conference, January 2016, Praha, Czech Republic.
- Kim Grüttner. "**Virtual Integration Testing for Power and Temperature using Virtual Platforms**" CONTREX Tutorial: Virtual Integration Testing for Mixed-Criticality Systems under Consideration of Power and Temperature Constraints, HiPEAC 2016 Conference, January 2016, Praha, Czech Republic.

- Kim Grüttner, Ralph Görgen, Sören Schreiner, Marco Feltes, Martin Bornhold. "**Energy, power and thermal management and its impact on safety**", MCS Workshop at HiPEAC 2016 Conference, January 2016, Praha, Czech Republic.

2015

- Kim Grüttner. "**Towards model-based power and temperature analysis of heterogeneous MPSoCs at system-level**" Kolloquium des Graduiertenkollegs "Heterogene Bildsysteme" at Friedrich-Alexander-Universität Erlangen-Nürnberg, April, 2015

- Kim Grüttner. "**Empowering mixed-critical system engineers in the dark silicon era: Towards power, temperature and aging analysis of heterogeneous MPSoCs at system-level**". Keynote at 1st Workshop on Model-Implementation Fidelity (MiFi) at DATE'15, March 2015, Grenoble, France.

- Kim Grüttner. "**Towards Platforms for Mixed-Criticality Systems"**. MCC Speakers Corner at ARTEMIS/ITEA Co-Summit 2015, March 2015, Berlin, Germany.

- Kim Grüttner. "**Towards power, temperature and aging analysis and estimation for SoCs at system-level**". Workshop MCS: Integration of mixed-criticality subsystems on multi-core and manycore processors at HiPEAC Conference, January 2015, Amsterdam, Netherlands.

- Omar Kacimi, Thomas Peikenkamp ,Ingo Stierand, Kim Grüttner, Philip Ittershagen, Philipp Reinkemeier, Heinz Hille. "**Interoperability for Mixed/Safety-Critical Systems Development Environments**", Workshop MCS: Integration of mixed-criticality subsystems on multi-core and manycore processors at HiPEAC Conference, January 2015, Amsterdam, Netherlands.

2014

- Kim Grüttner. "**Modelling, Simulation and Analysis of Mixed-Criticality Systems Under Consideration of Extra-functional Properties**" DAC Workshop on System-to-Silicon Performance Modeling and Analysis, San Francisco, CA, USA, June 5th, 2014.

- Seven Rosinger "**Analysis of extra-functional properties power, temperature, and degradation in MCS**", MCC Workshop, July 2014, Brussels, Belgium

- Philipp A. Hartmann. "**Modelling, simulation and analysis of extra-functional properties of multi-core platforms in multi-application scenarios**". RAPIDO'14: 6th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools, January 2014, Vienna, Austria.

- Philipp A. Hartmann. "**Are the results of the EU research projects really sharable and exploitable by the industrial and academic communities?**" Panel: "EU research on multi-many core" at PARAM-DITAM Workshop, HiPEAC 2014 Conference, 20 January, 2014

- Kim Grüttner. "**Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties**", 2nd International workshop on

the Integration of mixed-criticality subsystems on multi-core and manycore processors, HiPEAC Conference 2014, 21-22 January 2014, Vienna, Austria.

2013

- Kim Grüttner. "**Towards power, temperature and aging analysis and estimation for SoCs at system-level**". EU Workshop: Cyber-Physical Systems: Uplifting Europe's innovation capacity, October, 2013, Brussels

4.1.3 Exhibitions and Demonstrations

2016

- DATE 2016: **Mixed Criticality Project Cluster Exhibition Booth**, March 2016, Dresden, Germany.
- Ralph Görgen, Kim Grüttner, Sören Schreiner "**Virtual Platforms and Model-based Design for Early Analyses of Extra-functional Properties in Mixed Criticality Systems**", DATE 2016 University Booth, March 2016, Dresden, Germany.

2015

- ARTEMIS/ITEA Co-Summit 2015: **Mixed Criticality Project Cluster Exhibition Booth**, March 2015, Berlin.
- DATE 2015: **Mixed Criticality Project Cluster Exhibition Booth**, March 2013, Grenoble, France.

2014

- DATE 2014: **Mixed Criticality Project Cluster Exhibition Booth**, March 2014, Dresden, Germany.

4.1.4 Other dissemination activities

2016

- Special Session "**MCSDIA: Mixed-Criticality System Design, Implementation and Analysis**". At EUROMICRO DSD/SEAA 2014. August 2016, Limassol, Cyprus. Special Session Organizers and Chairs: Kim Grüttner and Eugenio Villar.
- CONTREX article in the **Brochure of the Collaboration Workshop Advanced Computing and Cyber-Physical Systems 2016**.
- HiPEAC Workshop "**4th International workshop on the "Integration of mixed-criticality subsystems on multi-core and manycore processors (MCS)**", January 2016, Prague, Czech Republic. Workshop Co-Organizers: Francisco Cazorla, Jon Perez, Kim Grüttner, Roman Obermaisser.
- HiPEAC Tutorial "**Virtual Integration Testing for Mixed-Criticality Systems under Consideration of Power and Temperature Constraints**". January 2016,

Prague, Czech Republic. Tutorial Co-Organizers: Eugenio Villar, Kim Grüttner and William Fornaciari.

- DATE Tutorial "**Internet-of-Things: Virtual Platforms in the Internet-of-Things Era – State of the art and perspectives**". March 2016, Dresden, Germany. Co-Organizers: Kim Grüttner and Davide Quaglia.

- DATE Co-Located Workshop "OpenES & CONTREX Projects Workshop: System-Level Power and Temperature Specification, Modelling and Analysis". March 2016, Dresden, Germany. Co-Organizers: Kim Grüttner, Laurent Maillet-Contoz and Adam Morawiec.

- DATE Friday Workshop "**IMPAC: Getting more for less: Innovative MPSoC Architecture Paradigms for Analysability and Composability of Timing and Power**". March 2016, Dresden, Germany. Co-Organizers: Ralph Görgen, Francisco J. Cazorla and Roman Obermaisser.

- Production of video material

    - CONTREX Project Video: https://www.youtube.com/watch?v=udu-KPKbyKk

    - CONTREX Project Video (with subtitle): https://www.youtube.com/watch?v=UJs6ZUwCHJs

    - CAMeL-View - OVP Co-Simulation of a Quadrocopter: https://www.youtube.com/watch?v=Rjyj1YmtSBg

    - OVP based virtual platform running video processing algorithm (object detection): https://www.youtube.com/watch?v=sdEdAwV1jbs

2015

- Special Session "**MCSDIA: Mixed-Criticality System Design, Implementation and Analysis**". At EUROMICRO DSD/SEAA 2014. August 2015, Funchal, Madeira, Portugal. Special Session Organizers and Chairs: Kim Grüttner and Eugenio Villar.

- FDL 2015 Special Session "**High Integrity Multi-Core Modelling for Future Systems (Hi-MCM)**", September 2015, Barcelona, Spain. Special Session Organizers: Kim Grüttner, Roman Obermaisser and Francisco J. Cazorla.

- HiPEAC Workshop "**3rd International workshop on the "Integration of mixed-criticality subsystems on multi-core and manycore processors (MCS)**", January 2015, Amsterdam, The Netherlands. Workshop Co-Organizers: Francisco Cazorla, Jon Perez, Kim Grüttner, Roman Obermaisser, Sascha Uhrig.

2014

- Face-to-Face meeting "**Roadmap for SystemC Standardisation**" at DVCon Europe, October 2014, Munich, Germany.

- Face-to-Face meeting "**Roadmap for Accellera CCI-WG**" at DVCon Europe, October 2014, Munich, Germany.

- Special Session "**MCSDIA: Mixed-Criticality System Design, Implementation and Analysis**". At EUROMICRO DSD/SEAA 2014. August 2014, Verona, Italy. Special Session Organizers and Chairs: Kim Grüttner and Eugenio Villar.

4.2 STMICROELECTRONICS, ST-I

4.2.1 Publications

- Ralph Görgen, Kim Grüttner, Fernando Herrera, Pablo Penil, Julio Medina, Eugenio Villar, Gianluca Palermo, William Fornaciari, Carlo Brandolese, Davide Gadioli, Sara Bocchio, Luca Ceva, Paolo Azzoni, Massimo Poncino, Sara Vinco, Enrico Macii, Salvatore Cusenza, John Favaro, Raul Valencia, Ingo Sander, Kathrin Rosvall, and Davide Quaglia. "**CONTREX: Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties**". In: Euromicro Conference on Digital System Design (DSD). Aug. 2016.

4.3 GMV AEROSPACE AND DEFENCE SA UNIPERSONAL

4.3.1 Publications

- Ralph Görgen, Kim Grüttner, Fernando Herrera, Pablo Penil, Julio Medina, Eugenio Villar, Gianluca Palermo, William Fornaciari, Carlo Brandolese, Davide Gadioli, Sara Bocchio, Luca Ceva, Paolo Azzoni, Massimo Poncino, Sara Vinco, Enrico Macii, Salvatore Cusenza, John Favaro, Raul Valencia, Ingo Sander, Kathrin Rosvall, and Davide Quaglia. "**CONTREX: Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties**". In: Euromicro Conference on Digital System Design (DSD). Aug. 2016.

4.3.2 Other dissemination activities

Two internal dissemination activities have been held during this project period to present the methodology and technology chain used for the CONTREX project to other GMV project teams.

4.4 VODAFONE AUTOMOTIVE

4.4.1 Publications

- Ralph Görgen, Kim Grüttner, Fernando Herrera, Pablo Penil, Julio Medina, Eugenio Villar, Gianluca Palermo, William Fornaciari, Carlo Brandolese, Davide Gadioli, Sara Bocchio, Luca Ceva, Paolo Azzoni, Massimo Poncino, Sara Vinco, Enrico Macii, Salvatore Cusenza, John Favaro, Raul Valencia, Ingo Sander, Kathrin Rosvall, and Davide Quaglia. "**CONTREX: Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional**

properties". In: Euromicro Conference on Digital System Design (DSD). Aug. 2016.

4.5 EUROTECH

4.5.1 Publications

- Ralph Görgen, et. all, "CONTREX: Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties", Euromicro DSD/SEA 2016, Cyprus.
- "IT-centric IoT device management using Java and Eclipse Kura", Embedded Computing Design, February 18th, 2016

4.5.2 Presentations at Conferences / Workshops

- "Developing smart IoT applications using Eclipse Kura", EclipseCON 2015, Toulouse, June, 2015.
- "Plugging Configurability into Your IoT Application Gateway", JavaOne, San Francisco, October, 2015.

4.5.3 Exhibitions and Demonstrations

- DevNation CodeStarter – a evening of IoT hacking with Eurotech, June 26 2016, San Francisco.
- Participation as a technology provider in the Open IoT Challenge. In this context, several third parties projects adopted Kura IoT Framework.
- http://iot.eclipse.org/open-iot-challenge/
- Innotrans, Berlin, September, 2015.
- Embedded World, Nuremberg, February, 2016.
- IoT Evololution Expo, Fort Lauderdale, February, 2016.

4.5.4 Other dissemination activities

- Kura Open Sourcing:
    - Kura 1.2.0 released on June 04, 2015.
    - Kura 1.2.1 released on August 11, 2015.
    - Kura 1.2.2 released on September 04, 2015.
    - Kura 1.3.0 released on October 23, 2015.

  - Kura 1.4.0 released on February 09, 2016.
  - Kura 2.0.0 released on July 27, 2016.

- Kura Community Projects:
  - "Using Eclipse Kura, MQTT and CoAP to build a smart greenhouse", http://iot.eclipse.org/java/tutorial/
  - "Smart Helmet – Using Eclipse Kura",

    http://byrebg.blogspot.in/2015/03/smart-helmet-using-eclipse-kura.html
  - "Creating a maker friendly DIY IoT home automation solution",

    http://open-iot-challenge.bittailor.ch/2015/03/22/project-wrap-up/
  - "Cloud vehicle monitoring system CARRACHO",

    http://diyapps.blogspot.it/2015/03/eclipse-open-iot-challenge-final-post.html
  - Several project are available at the following link:

    https://tobiddev.wordpress.com/
  - "Configure IoT Gateway Applications with Kura",

    http://www.bitreactive.com/kura-config/
  - Agrinode, Send data from MQTT client to IBM Bluemix

    http://agrinode.tumblr.com/
  - IOT VAIDYA, Heart rate monitor

    http://iotvaidya.blogspot.it/2016/02/eclipse-open-iot-challenge-20-update-7.html
  - E-Health personal gateway

    https://tobiddev.wordpress.com/2016/01/25/ehealth-personal-gateway/

4.6 INTECS

4.6.1 Publications

- Ralph Görgen, Kim Grüttner, Fernando Herrera, Pablo Penil, Julio Medina, Eugenio Villar, Gianluca Palermo, William Fornaciari, Carlo Brandolese, Davide Gadioli, Sara Bocchio, Luca Ceva, Paolo Azzoni, Massimo Poncino, Sara Vinco, Enrico Macii, Salvatore Cusenza, John Favaro, Raul Valencia, Ingo Sander, Kathrin Rosvall, and Davide Quaglia. "**CONTREX: Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties**". In: Euromicro Conference on Digital System Design (DSD). Aug. 2016.

- John Favaro, Salvatore Cusenza, *et al.*, "Introduction of a virtual platform based validation and verification process for the development of critical telecom equipment," in: CONTREX Book, to be published in 2017.

4.6.2 Presentations at Conferences / Workshops

Intecs participated in two editions of Embedded World in Nuremberg, Germany (February 2014 and 2015), in both the industrial section with a company booth in which we provided information flyers on the CONTREX project; and in the research conference section, where we met and discussed with other stakeholders in the embedded mixed-criticality systems area, as well as giving support to the CONTREX lead team on the project presentation.

Intecs participated in ERTS2 in Toulouse in February 2014, in which it distributed information on CONTREX in the embedded real-time systems domains of interest – all of the CONTREX applications domains (telecom, avionics, automotive) traditionally have significant representation from industry in that conference.

Intecs participated in the European Co-Summit in Berlin in 10-14 March 2015, in which we gave support to the lead team presenting CONTREX at the booth and giving presentations.

4.6.3 Other dissemination activities

As the principal provider of Use Case 3, Telecommunications, Intecs gave support to all of its use case technological providers (primarily OFFIS, EDALab, KTH, and Docea / Intel) for their own dissemination activities in conferences and workshops.

4.7 iXtronics GmbH

4.7.1 Publications

Publications are planned for the phase after the project.

4.7.2 Presentations at Conferences / Workshops

A workshop within the master degree program in computer science of the Carl von Ossietzky University Oldenburg with the project group. This workshop is the basis for the project group Avionic Architecture. In the project group Avionic Architecture 12 students developed an avionics for a multi-rotor system, which is based on a Xilinx ZYNQ Multiprocessor System-on-Chip (MPSoC). The postulated result of the course was to get a stable flying system, which uses the processing power of the MPSoC not only for the flight algorithms but also for another performance needing on-board task. The main focus of the workshop was on Model-driven development.

4.7.3 Exhibitions and Demonstrations

Demonstrations of intermediate implementations of the upcoming CAMeL-View-CONTREX-toolbox were performed for customers within internal events.

4.7.4 Internal Events

Several face-to-face meetings with different customers from the automotive and mechanical engineering industries. IX gave an outlook of the upcoming CAMeL-View-CONTREX-toolbox and discussed the new features with the customers.

4.8 EDALab

4.8.1 Publications

- A. Danese, G. Pravadelli, I. Zandonà, Automatic generation of power state machines through dynamic mining of temporal assertions, Proceedings of IEEE/ACM Design Automation & Test in Europe Conference & Exhibition (DATE), 14-18 Mar. 2016, Dresden, Germany, pp. 606-611, ISBN 978-3-9815370-7-9.

- F. Demrozi, G. Pravadelli, F. Stefanni, Automatic generation of self-adaptive transactors from PSL assertions, Proceedings of ECSI Forum on specification & Design Languages, 14-16 Sept. 2016, Bremen, Germany, pp.1-6.Presentations at Conferences / Workshops

- A. Danese, G. Pravadelli, I. Zandonà, Automatic generation of power state machines through dynamic mining of temporal assertions, Proceedings of IEEE/ACM Design Automation & Test in Europe Conference & Exhibition (DATE), 14-18 Mar. 2016, Dresden, Germany, pp. 606-611, ISBN 978-3-9815370-7-9.

- F. Demrozi, G. Pravadelli, F. Stefanni, Automatic generation of self-adaptive transactors from PSL assertions, Proceedings of ECSI Forum on specification & Design Languages, 14-16 Sept. 2016, Bremen, Germany, pp.1-6.

4.8.2 Exhibitions and Demonstrations

EDALab organized a booth at DVCon Europe 2015 to present HIFSuite-based virtual platform integration; for this event, EDALab prepared new dissemination material (Figure 5) and during this event, EDALab collected more than 30 contacts about interested companies.

Figure 5 Front page of dissemination leaflet for DVCon Europe 2015.

4.8.3 Other dissemination activities

EDALab co-organized some tutorials as follows:

- D. Quaglia, K. Gruettner, Virtual Platforms in the Internet-of-Things Era – State of the Art and New Perspectives, Tutorial at IEEE/ACM Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden (Germany), 14 March 2016.
- D. Quaglia, K. Gruettner, Virtual Integration Testing for Mixed-Criticality Systems under Consideration of Power and Temperature Constraints – A highly integrated Avionics and Payload Computing Use-Case, Tutorial at HIPEAC, Prague (Czech Republic), 18 January 2016.

EDALab supported the following dissemination events at IEEE/ACM Design Automation & Test in Europe Conference & Exhibition (DATE) 2016:

- Michele Lora, A Homogeneous Platform-Based Design Approach for the Design of Heterogeneous Systems, DATE2016 PhD Forum.
- Alessandro Danese, Graziano Pravadelli, Daniel Lorenz, PSMGen: Automatic generation of power state machines, DATE2016 University Booth.

Finally, EDALab put effort to disseminate HIFSuite tool (extended in CONTREX project). Two main actions were done:

- New HIFSuite website (Figure 6) with ad-hoc domain name to improve visibility; the web site allows the download of a free evaluation version of the tool (about 30 in the last year) and the collection of access statistics (about 100 accesses per month).
- New HIFSuite newsletter sent periodically to 150 contacts collected during exhibitions and on the website (Figure 7).

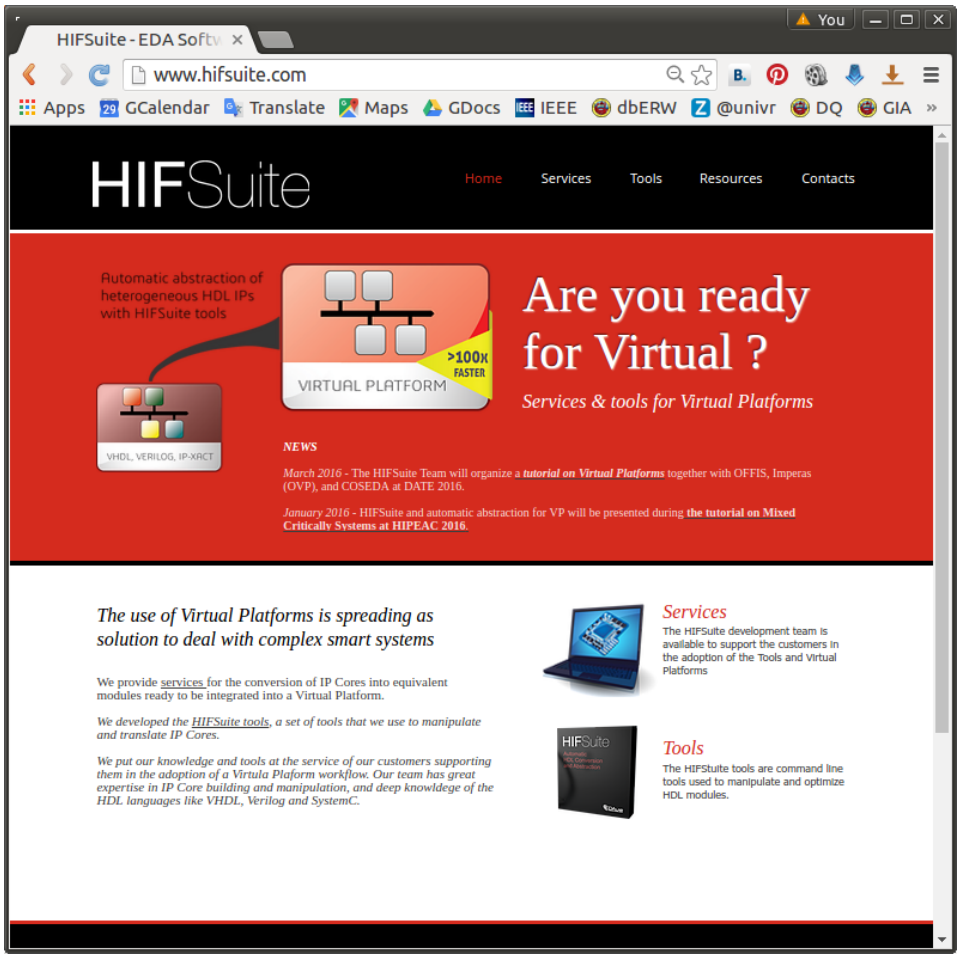


Figure 6 Main page of new HIFSuite web site.

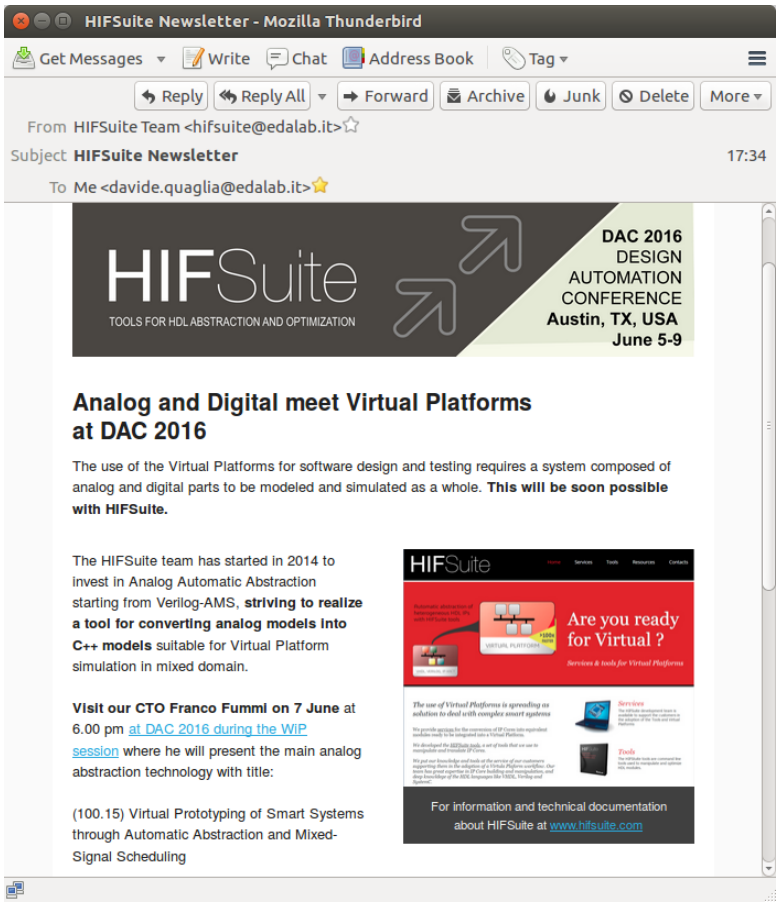


Figure 7 Example of the new HIFSuite newsletter.

4.9 INTEL

4.9.1 Presentations at Conferences / Workshops

No specific dissemination activities besides the presentation at the DAC 2015 workshop.

4.10 POLITECNICO DI MILANO

4.10.1 Publications

- Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano. “DeSpErate: Speeding-up Design Space Exploration by using Predictive Simulation Scheduling”. In Proceedings of DATE 2014 - International Conference on Design, Automation and Test in Europe. Dresden, Germany. March 2014.

- Edoardo Paone, Davide Gadioli, Gianluca Palermo, Vittorio Zaccaria e Cristina Silvano. “Evaluating Orthogonality between Application Auto-Tuning and Run-Time Resource
- Management for Adaptive OpenCL Applications”. In Proceedings of ASAP -

International Conference on Application-specific Systems, Architectures and Processors. Zurich, Switzerland. June 2014.

- Mariagiovanna Sami, Gianluca Palermo. "Virtual Semi-Concurrent Self-Checking for Heterogeneous MPSoC Architectures: A DSE Approach" In Proceedings of ASAP - International Conference on Application-specific Systems, Architectures and Processors. Zurich, Switzerland. June 2014.
- Carlo Brandolese, Luigi Rucco, William Fornaciari. Optimal wakeups clustering for highly-efficient operation of WSNs periodic applications. IEEE international conference on information communication and embedded systems (ICICES). Chennai, Tamilnadu, India, February 2014.
- Carlo Brandolese, Luigi Rucco, William Fornaciari. An optimal model to partition the evolution of periodic tasks in wireless sensor networks. IEEE international symposium on a world of wireless mobile and multimedia networks. Sydney, Australia, June 2014.
- Edoardo Paone, Francesco Robino, Gianluca Palermo, Vittorio Zaccaria, Ingo Sander and Cristina Silvano. "Customization of OpenCL Applications for Efficient Task Mapping under Heterogeneous Platform Constraints" Accepted in DATE 2015 – Design Automation and Test in Europe 2015.
- Fernando Herrera, Ingo Sander, Kathrin Rosvall, Edoardo Paone, Gianluca Palermo "An Efficient Joint Analytical and Simulation-based Design Space Exploration Flow for Predictable Multi-Core Systems" RAPIDO15 - 7th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools. Amsterdam, The Netherlands, January 2015.
- Amir Hossein, Ashouri; Giovanni, Mariani; Gianluca, Palermo and Cristina, Silvano; "A Bayesian Network Approach for Compiler Auto-tuning for Embedded Processors", ESTIMedia'2014 - IEEE Symposium on Embedded Systems for Real-Time Multimedia. New Delhi, India, October 2014.
- Patrick Bellasi, Giuseppe Massari, and William Fornaciari. 2015. Effective Runtime Resource Management Using Linux Control Groups with the BarbequeRTRM Framework. ACM Trans. Embed. Comput. Syst. 14, 2, Article 39 (March 2015), 17 pages.
- Simone Libutti, Giuseppe Massari, William Fornaciari "Addressing Task Co-scheduling on Multi-core Heterogeneous Systems: An Energy-Aware Perspective " HIPEAC Workshop on Energy Efficiency with Heterogeneous Computing (EEHCO), Jan. 19 2015, Amsterdam
- Giuseppe Massari, Simone Libutti, William Fornaciari, Federico Reghenzani and Gianmario Pozzi "Resource-Aware Application Execution Exploiting the BarbequeRTRM", Res4Ant 2016, Dresden (GER).

4.10.2 Presentations at Conferences / Workshops

- The paper "DeSpErate: Speeding-up Design Space Exploration by using Predictive Simulation Scheduling" has been presented by Gianluca Palermo at DATE 2014 Dresden, Germany. March 2014. The event is very large, however the audience of the session was around 40 people.

- Gianluca Palermo presented a poster at HIPEAC 2014 (Jan 2014, Vienna, Austria) on "DRuiD: Designing Reconfigurable Architectures with Decision-making Support" describing the usage of Machine Learning techniques in HW/SW application mapping for FPGA based designs. Globally the event included more than 400 people. Among them with around 10-15 researchers and PhD students a detailed technical discussion have been done on the content of the poster.

- On the same events Gianluca Palermo as co-organizer of the RAPIDO workshop, moderated an invited talk session on functional and extra-functional modelling of multicore platform where a presentation of CONTREX given by Philipp Hartmann from OFFIS has been included. The audience of the RAPIDO workshop during the invited session was around 40 people from both industry and academia.

- Carlo Brandolese presented the paper "Optimal wakeups clustering for highly-efficient operation of WSNs periodic applications" at ICICES2014. The number of attendees of the event was around 200 peoples, 30 people were in the specific session where the paper has been presented.

- Gianluca Palermo presented the paper "Evaluating Orthogonality between Application Auto-Tuning and Run-Time Resource Management for Adaptive OpenCL Applications" in ASAP14 within the IBM site in Zurich. The number of attendees was around 80 people for the session. In the same event Gianluca Palermo presented also a poster titled "Virtual Semi-Concurrent Self-Checking for Heterogeneous MPSoC Architectures: A DSE Approach" that attracted 10-15 researchers to discuss deeply on the topic.

- The paper "Customization of OpenCL Applications for Efficient Task Mapping under Heterogeneous Platform Constraints" has been presented by Gianluca Palermo at DATE 2015 in Grenoble France March 2015. This work have been developed as a collaboration between KTH and PoliMi, and raised lot of interest among the audience. The event is very large, however the audience of the session was around 60 people.

- Gianluca Palermo presented the paper "A Bayesian Network Approach for Compiler Auto-tuning for Embedded Processors" in ESTIMEDIA within the Embedded System Week in New Delhi. The number of attendees of the session was around 40 peoples coming from both industries and academia.

- Gianluca Palermo as co-organizer of the RAPIDO workshop co-located with HIPEAC 2015 (Jan 2015, Amsterdam), moderated an invited talk session on modelling extra-functional properties on multicore architectures to increase the attention on this CONTREX key aspect. The audience of the RAPIDO workshop during the invited session was around 30 people from both industry and academia

- Gianluca Palermo as co-organizer of the RAPIDO workshop co-located with HIPEAC 2016 (Jan 2016, Prague), moderated two invited talk sessions on "System Level Power Analysis: Challenges, Use-Cases and a new Standard" and "Virtual Platform Extensions for Software Development of Smart Embedded System" to increase the attention on this CONTREX key aspect. The audience of the RAPIDO workshop during the invited session was around 40 people from both industry and academia

- Giuseppe Massari presented the paper "Resource-Aware Application Execution Exploiting the BarbequeRTRM" at RES4ANT workshop co-located with DATE

conference. The number of attendees of the event was around 60 peoples both from academic and industry.

- IWES 2016 - Italian Workshop on Embedded Systems - Pisa, Italy 19-20 September 2016 - William Fornaciari (PoliMI): "From cps to high - end computing: common problems and synergies" The number of attendees was more then 50 peoples mainly composed by academic people.

4.10.3 Other dissemination activities

Prof. William Fornaciari had a talk at Chiesi Farmaceutici SpA with title "From embedded systems to high performance computing - problems and solutions while waiting for the IOT" 9 Giugno 2016 - Pama, Italy.

Some internal events have been used at Polimi to internally disseminate the work done in CONTREX.

In particular, CONTREX related tools developed at POLIMI have been outlined during some master degree level courses at POLIMI: Embedded System Design, Advanced Operating Systems and Advanced Computer Architectures.

Moreover some internal seminars to the POLIMI research group not involved in the project, including also MSc, Graduate and PhD students, have been organized:

- Davide Gadioli. "ARGO: A C++ framework for monitoring application level extra-functional properties and supporting application auto-tuning". April 2014.
- Edoardo Paone: "Improving DSE with Constraint Programming techniques for efficient DoE definition (Report of the period at KTH)". January 2014.
- Gianluca Palermo: "Automatic Design Space Exploration using MOST". September 2014.
- Amir Ashouri. "Compiler Auto-tuning: a DSE approach". July 2014.
- Edoardo Paone. "Using DSE for run-time adaptation". June 2014.
- Gianluca Palermo. "Joint Analytical-Simulation based DSE for Mixed critical systems". January 2015.
- Gianluca Palermo "Customization of OpenCL Applications for Efficient Task Mapping under Heterogeneous Platform Constraints". April 2015
- Gianluca Palermo "Exploring Irregular Design Spaces using the Adaptive Replica Search" September 2015.
- Amir Ashouri. "A DSE approach to Compiler Auto-tuning using MOST". July 2015.
- Emanuele Vitali, "iNARK - INteraction Analysis fRameworK for Mixed Critical Systems" June 2016.
- Emanuele Vitali "Including iNark in the JAS-DSE framework for Mixed Critical Systems" September 2016.

4.11 POLITECNICO DI TORINO

4.11.1 Publications

1. Sara Vinco, Michele Lora, Enrico Macii and Massimo Poncino, "IP-XACT for smart systems design: extensions for the integration of functional and extra-functional models", *ECSI Forum on specification & Design Languages*, Bremen, Germany 2016, pp.1-8.

2. S. Vinco, Sara, Y. Chen, E. Macii, M. Poncino, "A Unified Model of Power Sources for the Simulation of Electrical Energy Systems", *ACM Great Lake Symposium on VLSI (GLSVLSI)*, 18-20.05.2016, Boston, USA, 2016, pp. 281-286.

3. S. Vinco, Sara, Y. Chen, E. Macii, M. Poncino, "Fast Thermal Simulation using SystemC-AMS", *ACM Great Lake Symposium on VLSI (GLSVLSI)*, 18-20.05.2016, Boston, USA, 2016, pp. 427-432.

4. Y. Chen, E. Macii, M. Poncino, "Frequency Domain Characterization of Batteries for the Design of Energy Storage Subsystems", *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2016)*, 26-28/9/2016, Tallinn, Estonia 2016.

4.11.2 Presentations at Conferences / Workshops

The above paper have been presented at the respective conferences. Paper 1) was presented by a co-author of another institution, 2) and 3) were presented by Sara Vinco, paper 4) was presented by another colleague not listed as a co-author but that participated at the conference.

4.11.3 Exhibitions and Demonstrations

No presentation has been done at exhibitions concerning the contributions relative to CONTREX.

4.11.4 Other dissemination activities

- Massimo Poncino, Enrico Macii (POLITO), Michelangelo Grosso (STP).

  RTSI 2015 (International IEEE Forum on Research and Technologies for Society and Industry, Torino, Italy. Tutorial "Power Efficiency in the Design of Smart IoT Devices",

  In the presentation, explicit link to CONTREX activities (use of Inemo platform, power and battery modeling) was made
- Massimo Poncino, Enrico Macii (POLITO), Michelangelo Grosso (STP).

  DATE 2016 Tutorial "Power Efficiency in the Design of Smart IoT Devices", Dresden, Germany. In the presentation, explicit link to CONTREX activities (use of Inemo platform) was made
- Massimo Poncino.

  Seminar "Towards Computer-Aided Design of Electrical Energy Systems: Challenges and Solutions", University of California, Irvine, USA, April 22th, 2016

In the presentation, CONTREX activities was made (power as an extra-functional property, and extension of the methodology to other extra-functional properties like temperature and reliability)

4.12 UNIVERSIDAD DE CANTABRIA

4.12.1 Publications

- Medina J.L., González Harbour M., Gutiérrez JJ.., Palencia J.C., Cuevas C., López P., and Drake J.M.. "Experiencing the multi-path schedulability analysis capabilities in MAST 1.5. In Proc. of Forum on Design and Specification Languages 2014", pp 175-176. Munich, Germany, October 14th-16th, 2014.

- Fernando Herrera (UC), Kathrin Rosvall, Ingo Sander (KTH), Edoardo Paone and Gianluca Palermo (PoliMi). "An Efficient Joint Analytical and Simulation-based Design Space Exploration Flow for Predictable Multi-Core Systems". In RAPIDO'15 7th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools 21 Jan 2015, Amsterdam, The Netherlands.

- F. Herrera, P. Peñil, and E. Villar. "A model-based, single-source approach to design-space exploration and synthesis of mixed-criticality systems". 18th International Workshop on Software and Compilers for Embedded Systems, SCoPES 2015, ACM. Schloss Rheinfels, St. Goar, Germany. 2015-06.

- F. Herrera, P. Peñil, and E. Villar. "Enhancing Analyzability and Time Predictability in UML/MARTE Component-based Application Models". Forum on specification & Design Languages (FDL 2015). Barcelona, Spain. Sept., 2015-09.

- E. Ebeid, J. Medina, D. Quaglia and F. Fummi. "Extensions to the UML Profile for MARTE for Distributed Embedded Systems". Forum on specification & Design Languages (FDL 2015). Barcelona, Spain. Sept., 2015-09.

- F. Herrera, P. Peñil, E. Villar. "UML/MARTE Modelling for Design Space Exploration of Mixed-Criticality Systems on top of Time-Predictable HW/SW Platforms". Jornadas de Computación Empotrada (JCE15). Córdoba, Spain. 2015-09.

- R. Gorgen, K. Grutner, F. Herrera, G. Palermo, W. Fornaciari, C. Brandolese, D. Gadioli, S. Boccio, L. Ceva, P. Azzoni, M. Poncino, S. Vinco, E. Macii, S. Cusenza, J. Favaro, R. Valencia, I. Sander, K. Rosvall, and D. Quaglia "CONTREX: Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties". Euromicro DSD 2016. Limassol, Cyprus. 2016-08

- F. Herrera, J. Medina, E. Villar. "Modelling Hardware/Software Embedded Systems with UML/MARTE: A Single-Source Design approach". In Springer "Handbook of Hardware/Software Codesign". Ed.s Soonhoi Ha and Jürgen Teich. Aceptada

In addition to the reported publications, there are on-going activity on publications derived from UC research in CONTREX. They are reported together with the their current status.

- Book chapter: F.Herrera, J. Medina and E.Villar. "Modelling Hardware/Software Embedded Systems with UML/MARTE: A Single-Source Design Approach". In

Handbook of Hardware/Software Codesign". Priinted version to appear in Feb. 2017 (Electronic version will be available earlier).

- Research paper: F. Herrera, J. Medina and E.Villar. "A Framework for UML/MARTE Modelling and Design of Mixed-Criticality Systems: Model Validation and Generation of Performance Analysis Models". Submitted to Journal of Systems Architecture. In 2nd revision process.

- Research paper: F. Herrera, E. VIllar, K. Rosvall, H.A. Niaki, I. Sander, E. Vitali, G. Palermo. "A System-Level Modelling, Analysis and Design Framework for Mixed-Criticality Systems". To be submitted to Transactions on Embedded Computing Systems (TECS). Submission scheduled for end of November.

4.12.2 Presentations at Conferences / Workshops

UC attended and made presentations of all the conference and workshop papers reported in section 4.12.1. In addition to that, the following presentations at conferences where given:

- F. Herrera. "UML/MARTE modelling for mixed-criticality systems". Tutorial "CONTREX: Virtual Integration Testing for Mixed-Criticality Systems under Consideration of Power and Temperature Constraints" in HIPEAC 2016. Jan., 2016.

- F. Herrera and E. Villar. "Fidelity of native-based performance models for Design Space Exploration". MiFi Workshop in DATE 2016 in http://www.date-conference.com/conference/workshop-w03. March, 2016.

4.12.3 Exhibitions and Demonstrations

- F. Herrera. Poster presentation of the first version of the JAS-DSE methodology in HiPEAC 2015: https://www.youtube.com/watch?v=lHKzfH5hOmU

- "Poster presentation in HiPEAC 2016". F. Herrera and E. Villar. "UML/MARTE Modelling of Mixed-Criticality Systems: A quadcopter Use Case".

- University Booth in DATE 2016: F. Herrera and E. Villar. "CONTREP: A single-source framework for UML-based Modelling and Design of Mixed-Criticality Systems". 2016-03

Figure 8. F.Herrera during the presentation of the CONTREP framework in DATE'16 UBooth.

4.12.4 Other dissemination activities

- In the CONTREX Technical meeting hold in Oldenburg in December 2014, the CONTREX UML/MARTE modelling methodology and the preliminary version of the JAS-DSE methodology were presented.
- Proff. E. Villar co-chaired the Special Session on Mixed-Criticality System Design, Implementation and Analysis (MCSDIA) in EUROMICRO DSD/SEAA 2014, hold in Verona, Italy, August 27-29, 2014.
- Talk in the Shonnan Meeting: E.Villar. "Modeling, Analysis, and Verification of Cyber-Physical Systems in the Electronics Century". March, 23th, 2016.

Figure 9. Proff E.Villar disseminated CONTREX results in the Shonan experts group meeting.

In addition to the dissemination activities reported above, UC has developed three new websites in CONTREX.

A site for the single-source modelling and design methodology, at http://umlmarte.teisa.unican.es, has been developed. Figure 10 shows the home page. This site disseminates the single-source modelling and design methodology centered on the UML/MARTE methodology. Documentation on the UML/MARTE modelling methodology is accessable from this site. In the same way that the UML/MARTE model at the centre of the ESL design activities supported, this site serves as a central point to different front-end and back-end tools supporting the single-source design approach. For instance, the eSSYN site (http://essyn.com) for SW synthesis can be accessed from this site. Two new sites, linked by this central site, have been also generated in CONTREX.

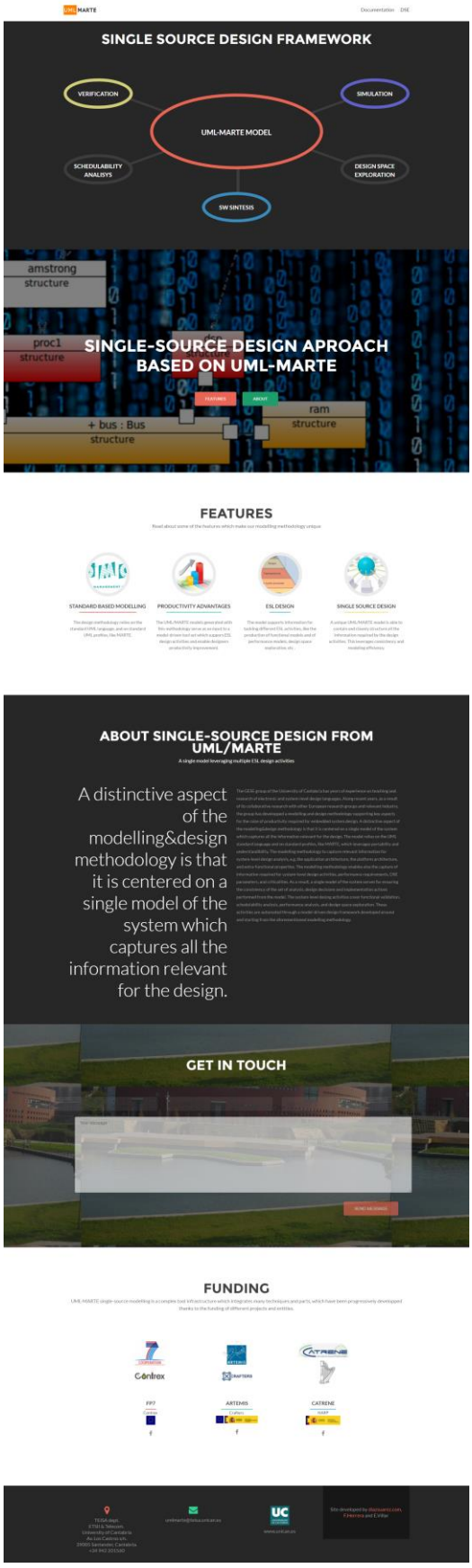


Figure 10. Main page of the single-source modelling and design methodology developed in CONTREX.

A specific site for the CONTREX Eclipse Plug-in (CONTREP) has been generated and published at http://contrep.teisa.unican.es. The home page of the CONTREP website is shown in Figure 11.

Figure 11. Main page of the CONTREX Eclipse plug-in developed in CONTREX.

Finally, a website for the VIPPE tools has been developed and published at http://vippe.teisa.unican.es. Figure 12 shows the home page.

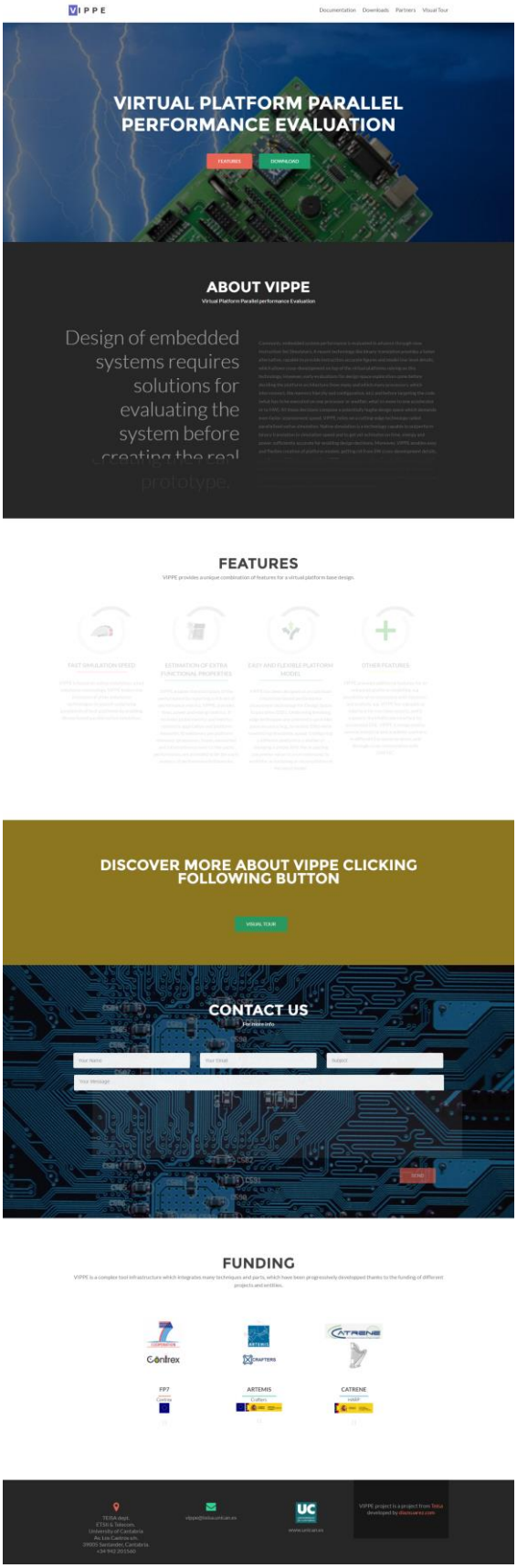


Figure 12. Main page of the VIPPE tool developed in CONTREX.

As can be seen in the figures, the home sites make a brief introduction to the methodology/framework/tool and presents their main benefits.

The home pages also make a brief introduction, with the motivations, and to the novel technologies, for the understanding of how the benefits are achieved.

The home sites also present the funding organizations endorsing the work. In the cases where several funding organizations have endorsed the work, a synthetic description stating what each organization/project has funded is deployed when the cursor is moved over the project logo.

At the end of the home site allow the contact for questions, and for requiring the trial or use of the tool,

The top of the home sites provide links for documentation, download and other aspects of interest related to the methodology or tool.

4.13 KUNGLIGA TEKNISKA HOEGSKOLAN

4.13.1 Publications

- N. Khalilzad, K. Rosvall, and I. Sander. A modular design space exploration framework for multiprocessor real-time systems. In Forum on Specification and Design Languages (FDL 2016), Bremen, Germany, Sept. 2016.
- S. Attarzadeh-Niaki and I. Sander. An extensible modeling methodology for embedded and cyber-physical system design. SIMULATION: Transactions of The Society for Modeling and Simulation International, 92(8):771-794, 2016.
- G. H. Blindell, C. Menne, and I. Sander. Languages, Design Methods, and Tools for Electronic System Design, chapter Synthesizing Code for GPGPUs from Abstract Formal Models, pages 115-134. Springer, 2016.
- S. Attarzadeh-Niaki and I. Sander. Integrating functional mock-up units into a formal heterogeneous system modeling framework. In International Symposium on Computer Architecture and Digital Systems (CADS), Oct. 2015.

4.13.2 Presentations at Conferences / Workshops

- Nima Khalilzad, Towards Designing Efficient End-to-end Resource Reservations for Distributed Embedded, Proceedings of the Forum on specification & Design Languages (FDL'16) Work-in-Progress session, Bremen, Germany.
- Ingo Sander, Joint Analytical and Simulation-Based Design Space Exploration for Mixed-Criticality Systems. Invited Talk at Embedded Conference Scandinavia (3-4 Nov 2015), Stockholm, Sweden.
- Kathrin Rosvall, Flexible and Trade-Off-Aware Constraint-Based Design Space Exploration for Streaming Applications on Heterogeneous Platforms. Presentation at CPSWeek: Workshop on Joint Analytical and Simulation-Based Design Space Exploration for Mixed-Criticality Systems (IDEA 2016), Vienna, Austria.

4.13.3 Exhibitions and Demonstrations

4.13.4 Other dissemination activities

The following lectures are strongly related to CONTREX WP2. In particular they take up the problems of shared resources, the use of models of computation, the ForSyDe modelling libraries and the analytical design space exploration technique used in CONTREX.

- Lectures as part of IL2212 Embedded Software (master course, KTH, around 50 students given once a year):
    - System Design with ForSyDe (90 minutes)
    - Correct-by-Construction Design of Embedded Real-Time Multiprocessor Applications (90 minutes)
    - A constraint-based design space exploration framework for real-time applications on MPSoCs (45 minutes)

4.14 ST-POLITO

4.14.1 Publications

Monography (written in Italian) with the following title:
"Analisi del consumo energetico di un sensore inerziale integrato in tecnologia MEMS" (P. Chiaravalle), July 2015
done by a student of Politecnico of Turin for his BS.

4.14.2 Presentations at Conferences / Workshops

- RTSI Forum 2015 - Power Efficiency in the Design of IoT Devices" (E. Macii, M. Poncino, M. Grosso),
- DATE 2016 - Power Efficiency in the Design of Smart IoTDevices" (E. Macii, M. Poncino, M. Grosso)

5 Relations to Other Projects

Within the MCC cluster (DREAMS, PROXIMA and CONTREX), several activities were planned and jointly organized:

- Joint MCC paper
  - Salvador Trujillo, Roman Obermaisser, Kim Grüttner, Francisco J. Cazorla, and Jon Perez. "European Project Cluster on Mixed-Criticality Systems". In: Performance, Power and Predictability of Many-Core Embedded Systems (3PMCES) Workshop. Mar. 2014.
- Mixed-Criticality Forum website (http://www.mixedcriticalityforum.org/home/)
- Joint cluster reviews with embedded MCC workshops
- Common Special Session at the FDL 2015 Conference
- Joint booth with posters at the ARTEMIS Co-Summit
- Strong MCC partner contribution in DSD special session MCSDIA (2014, 2015 and 2016)
- Joint booths with poster at DATE 2014, 2015 and 2016
- Series of joint HiPEAC MCS workshops (2014, 2015 and 2016) with embedded community building event
- DATE 2016 joint Friday Workshop IMPAC

A strengthened relation has been developed with the OpenES project:

- CONTREX objectives, approach and expected results has been presented to the whole OpenES consortium (by the common partner Docea Power)
- The workshop on System to Silicon Performance Modeling and Analysis at DAC 2015 and 2016 has been developed in tight cooperation with OpenES
- Joint OpenES and CONTREX workshop at DATE 2016
- Common session at the FDL 2016 Conference