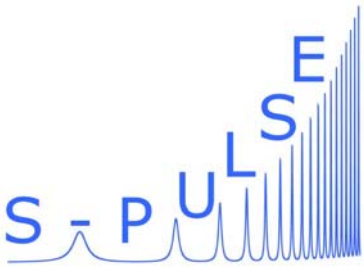

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S-PULSE deliverable D1.4.1: Critical Review and Research Agenda

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This document reviews the issues and challenges for superconductive electronics (SE) identified in WP1 and advises on an agenda based on priorities in accordance with the roadmap (deliverable D1.3.2). The technological development guidelines will structure human and financial resources mobilisation to insure technical activity as identified in the strategic plan. This task is devoted to study user-oriented system design and the impact of SE on the whole system, either originating at the circuit level or at the system level, depending on applications. The industrial guidance insures a proper match between end-users requirements and system architecture.
Reports about the international status of SE outside Europe have been delivered (D1.1.1 & D1.1.2) showing the aggressive support of US and Japanese societies to SE. Today the U.S.A. and Japan operate a foundry service for the fabrication of complex integrated superconductive electronics. The development of this technology will support the competitiveness of European industry with potential applications in
- high-speed ICT components with low energy consumption,
- non-destructive material evaluation for quality assurance,
- IR and THz imaging technology for security, pharmaceutical and chemical industry,
- quality assurance by means of standardization / measurements,
- communication and cryptography.

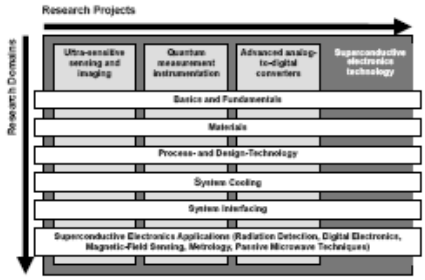

Fig. 1-1. European superconductive electronics research matrix.

The matrix in figure 1-1 shows how the defined projects are to be integrated and that the entire innovation chain from basic research to system implementation is covered. The described organization scheme avoids doubling of R&D effort and increases effectiveness by combining European research and fabrication capabilities.
The identified four research projects are described in more detail subsequently.

Although the present technology can be used for simple circuits of less than a few thousand junctions, it is clear that the issue with the highest priority is the development of the foundry, a “transverse” project linked to the other 3 application-oriented projects. In order to keep track with the development in the U.S.A and Japan, a long term stability of the European technological basis for superconductive electronics is essential but is not offered by short-term project funding in national and European projects. Many European institutes utilize for experiments in basic physics in-house design and fabrication of superconductive circuits. This low-complexity electronics is very often a research branch in numerous laboratories and not yet industrially applied. However, the recent installation of FLUXONICS Foundry for the first time provides for a high-level and open-access technological basis for the production of integrated superconductive electronics. Since the quality and circuit yield is a function of foundry throughput, it is essential to focus the European demands in this emerging technology field. The long-term stability and the goals of the shrink-path strategy can be achieved by a

European Superconductive Electronics Centre (ESEC) which, as proposed in deliverable D1.2.2, should consist of three divisions: design, fabrication and testing. The design division includes the adapted tools necessary for simulation, layout and design of the special SE devices. Design rules are available for the routinely used standard processes. A cell library supports the development of layout and design by the user. The fabrication division is doing the real fabrication of the devices; the development of a reliable SNS junction technology using Niobium is desirable. The testing division assures the fabrication by checking and testing the devices at low temperatures and high frequencies if need be. For a detailed description of the technical aspects, please refer to deliverable D1.2.2.
The cooperation within the FLUXONICS and the streamlining of the European research directions within the S-PULSE project leads to the fulfilment of all preconditions in terms of expertise, structure, ways of communication, and cooperation given. It is concluded that the proposed ESEC appears to be feasible as judged from the abovementioned expert-based preconditions.

Superconductive electronics technology comprises not only the fabrication process, but also the corresponding device and circuit design.
The SE technology must be focused to reach VLSI integration level as fast as possible. Only this level of integration allows getting access to real-world applications being of significance for the society and the industry as well. Furthermore, only this level of circuit complexity allows to fully exploit the unique features of SE. Therefore, the research goals in this field have to follow strictly the shrink path: to downsize the junctions, to increase the critical current density through improved lithography and to increase the number of metallisation layers. For this, it is necessary to improve the lithographic process, to include CMP and finally, to reach a new level in process control.

Goals for the next two years SE technology:

- 5:1 projection lithography,
- 2.5 µm Josephson junction size,
- j_C=2 kA/cm^2,
- robust technology for large SNS circuits,
- Noise-optimized extremely thin films and structures down to nm size.

Goals for the next five years SE technology:

- planarization by CMP,
- 1.0 µm Josephson junctions size,
- j_C=10 kA/cm^2,
- 6-10 wiring / screening layers,
- nanostructures on wafer-scale demonstrated,
- process control and simulation demonstrated
- VLSI circuits demonstrated.

The design infrastructure is seen as the enabler for intentionally introducing functionality into technological structures. In order to get best functionality and compatibility to the international mainstream of circuit design, the software tools for SE to be developed in future should be linked as best as possible to the software used in semiconductor design. Also, the knowledge about these tools has to be disseminated. One example is the NioPulse software tool suite which is especially developed for SE. It is created for fast, closed-cycle design and offers simulation [6-4]. Design for Yield (DFY) still has to be established. Another important topic is the development of a cell library for mixed-signal circuits. The capabilities to simulate the whole SE system have to be developed. Furthermore, adapted circuit architectures are required.

Goals for the next two years SE design infrastructure:
- compatibility of design formats in European groups,
- cell libraries optimized and characterized,
- Design for Yield (DFY) established,
- Analogue-mixed-signal circuit simulation.

Goals for the next five years SE design infrastructure:
- unified European design tool suite,
- cell libraries and design kits experimentally proven,
- DFY approach consolidated by fabrication statistics,
- verification by simulation on system level,
- Cell-library-based analogue-mixed-signal circuits demonstrated.

Application – driven project planning

Based upon the assessment of the status of the research on SE in Europe and upon the projections of the future research work described deliverables D1.1.2 & D1.3.2, three main research projects can be identified:
- Ultra-sensitive sensing and imaging,
- Quantum measurement instrumentation,
- Advanced analog-to-digital converters.

These projects are defined according to the expected strengthening of the European competitiveness in SE so that real-world applications in this technology with societal and industrial impact become viable. They cover essential research domains as:
- Basics and Fundamentals,
- Materials,
- Process and Design Technology,
- System Cooling,
- System Interfacing.

Project: Ultra-sensitive sensing and imaging

Superconductive radiation and photon detectors cover a very wide spectral range from millimetre to nanometre wavelengths or in the energy scale between meV and keV. Superconducting detectors are also emerging as detector-of-choice in mass identification with high throughput of macromolecules such as proteins and virus. In the next years all the different types of detectors should be improved and optimized to reach the ultimate quantum limit in the respective spectral range for applications in instruments for fundamental research in astronomy, material science, security, chemistry and biology. There is room for improvement regarding sensitivity, speed and response of all detector types. Especially fundamental research on quantum physics most certainly will advance the performance of superconducting sensors. In the first place such quantum limited detectors will be useful for scientific and/or medical applications. Nevertheless, also future industrial applications (passive security screening, identification of substances, geological exploration – detection of raw materials, minerals, ground water – and environmental protection, imaging of archaeological objects. …) will benefit from these advancements.

Observing current trends, it becomes obvious that the main technology drivers are imaging and high throughput applications, which require large arrays of sensors to fill the focal plane of an appropriate photon or ion beam. Therefore a large effort has to be put on maturing single detectors to devices which combine a large number of superconducting detectors and their readout whilst enhancing the manufacturing technology to make such focal plane array manageable and economically feasible. Due to the sophisticated sensors, this involves not only a pure chip design but the implementation of such devices into an adapted cryo-environment, meaning a cryogen-free cooler and a low noise readout / data acquisition chain.

Some applications with large impact to societal needs like imaging of X-ray, optical and THz signals in the fields of security, telecommunications at high bit rate, materials and health will require a mature thin film nanotechnology to fabricate large-area detectors and large number of single pixel detectors or even small and large arrays. This technology should be able to fabricate up-to a million detectors on a chip with nm-size dimensions of the active devices embedded in a complex microwave wiring environment with several metallic layers.
In addition, large detector arrays will require an integrated ultra-low power readout circuitry with sufficiently high bit rate capability and very low back-action to the detectors. Obviously, such a new readout technology can be realized with an ultra-low power RSFQ technology. The power dissipation of the actual existing RSFQ technology should be reduced by a factor of 1000. Therefore an appropriate RSFQ technology should be developed. In the next years feasibility studies will demonstrate the functionality of this approach and will lead to a new complex design of arrays and readout electronics.

Goals for the next two years:

- For mm- and sub-mm-applications, Transition-Edge Sensors (TES) single pixel detectors will be optimized and integrated in small arrays.
- For the same spectral range, especially for the THz for coherent receivers Nanowire Hot-Electron Bolometers (HEB) will be improved.
- For IR and Visible spectral range Superconducting Nanowire Single Photon Detectors (SNSPD) will be optimized at the single pixel and array stage to achieve large area coverage and imaging.
- For heavy ions and macromolecules, Superconducting StripLine Detectors (SSLD) will be implemented for subnanosecond response time at few mm pixel size and ≥ 5K operating temperature for 100% efficient detection of massive proteins.

For mm- and sub-mm-applications, Transition-Edge Sensors (TES) single pixel detectors will be optimized and integrated in small arrays.

- First ultra-low power RSFQ circuits, Frequency-Domain (FDM) and Code-Division Multiplexer (CDM) will be developed and demonstrated for detector readout.
- The nanotechnology for detector and RSFQ fabrication will be optimized with a focus on nm-sized dimensions for multi-pixel arrays and integration with ultra-low power RSFQ devices.

Goals for the next five years:

- Imaging applications of X-ray, optical and THz signals with large arrays up-to 1000x1000 pixel demonstrated in laboratory.
- Small TES arrays will be implemented in real systems, e.g. for THz scanners.
- First arrays with Single-Photon and Single-Molecule Detectors will be demonstrated in real applications for biology, chemistry and quantum communication.
- First practical readout circuits with ulta-low power RSFQ, FDM and CDM will be demonstrated.

Project: Quantum measurement instrumentation

Superconductive devices are playing an important role for fundamental metrology and high-precision measurements by means of quantum standards, which enable the reference of units to fundamental constants. These quantum standards provide uniform measuring capabilities independently from space and time at an accuracy level that can not be reached using room temperature instrumentation. While quantum standards are presently well-established for DC applications and only at national metrology institutes, future activities strongly aim for simple and user-friendly instruments for AC applications, which are to be routinely used not only at special laboratories but at the workshop floor of industrial and private companies. As metrology based on quantum standards is of outstanding relevance for the society, specific metrology-aimed developments are presently funded by the EC within the European

Metrology Research Programme (EMRP). This programme is focused on the metrological aspects of new developments, which are mainly performed at national metrology institutes. The proposed activities here do not overlap with the EMRP, but are to push forward such developments which enable the implementation and distribution of quantum-based measuring capabilities onto a broad and user-friendly measurement instrumentation platform in Europe as mentioned above. The envisaged goals for the next two and five years are listed below. A promising approach for future developments is here the integration of adapted superconducting digital electronics into novel quantum measurement instrumentation.
Improved fabrication technologies will play a key role in reaching these ambitious goals. The technological developments have to be focused on two main directions: First, improved superconductor, normal metal and dielectric materials as well as Josephson junctions with a wide range of dimensions on their basis will be needed for the realization of robust and adapted circuits for quantum voltage and quantum current measurement instruments. An envisaged goal for the next two years is here the development of more robust junctions for electrical current standards in the sub-nanoamps range. Secondly, the fabrication of large series arrays will require the VLSI integration level especially for voltage standards at the 10-V level. In addition, the improved fabrication technology will strongly push forward the development of detectors for electrical quantities and with sensitivity approaching the limits imposed by quantum mechanics as for example SQUIDs or electrometers.
An important goal in the field of quantum measurement instrumentation is the development of a quantum multimeter being a user-friendly multimeter for measuring voltages, resistances, and currents directly referenced to quantum standards. A first prototype version of this top-level instrument will probably be demonstrated within 5 years. This multi-purpose instrument will be used at national metrology institutes and in the long term for on-site calibrations and precision measurements in university and industry laboratories, respectively.

Goals for the next two years:

- concept of a modified 1-V quantum synthesizer,
- concept of a quantum multimeter.

Goals for the next five years:

- modified 1-V quantum synthesizer,
- first version of a quantum multimeter demonstrated.

Project: Advanced analogue-to-digital converters

One of the important stakes of future generations of ground- or space-based telecommunication networks relies on the possibility to introduce flexibility in the payloads through configuration by software. This is called software-defined radio (SDR). The main objective is to propose systems to operators and users for which parameters like frequency bands, modulation formats, and number of channels per carrier can be modified after the system is built and during its entire life. This objective is particularly important for satellites that are now built with a 15-year life expectancy, but also for related ground systems that need to adapt to the rapidly changing telecommunication field for a minimal cost. The general trend is to address a higher number of final users with a broader individual bandwidth, of the order of tens of Mbits/s. Associated services range from phone, mobile TV, professional mobile internet and interactive TV, point-to-point connection for large files [6-3].
Nevertheless, the SDR technique requires ultrafast analogue-to-digital converters (ADC). The currently available semiconductor ADCs only offer a bandwidth of a few GHz with no more than 8 effective bits. The state-of-the-art and future expectations of semiconductors lead to an improvement of performance of only 1.5 bit every 7 years, with a constant sampling rate. Consequently the expected performances of semiconductors in this particular field are very far from what is needed, even in a time frame of 10 to 15 years.

The direct digitization of radiofrequency signals at microwave sampling rates is the most promising way of introducing the flexibility in future telecommunication systems. The all-digital technique is the main trend in this field, allowing to filter or reconfigure modulated formats of received signals in specific frequency bands, to reprogram signal processing algorithms, or even to modify the radiation pattern of software-controlled agile antennas, all this on-the-fly.
To achieve these tasks, Superconducting Digital Electronics has two key advantages on other technologies:
- the already demonstrated possibility to sample signals at frequencies in the 100 GHz range with the RSFQ technique, with negligible power consumption;
- the possibility of obtaining extremely high dynamic range due to the fundamental quantum accuracy of the digital bit in multiples of the magnetic flux quantum h/2e, based on quantum mechanics. The quantum accuracy is not available in the semiconductor circuits digitization principle. This greatly limits their linearity. Thus, complex architecture and circuits to overcome the issue are required.
To achieve the goals required by SDR, it is necessary to develop extremely sensitive ADCs having the high desired dynamic range. Since the circuits need to be cooled at cryogenic temperatures, it is advisable to perform as many tasks as possible on the ADC chip, like on-chip direct signal processing, for the same cryogenic price since the power consumption of complex RSFQ chips is in the 500 mW range at maximum. This requires circuits with about 10000 logic gates, which fit on a 1 cm^2 chip, that need to be fabricated with a low-Tc technology, as a necessary step to gain knowledge on designs and architectures since the technology is mature, before envisioning higher-Tc superconductors.

Goals for the next two years:

- prove ADC design with current 1 kA/cm^2 low-Tc technology.

Goals for the next five years:

- prove ADC design with entire signal processing with current 1 kA/cm^2 low-Tc technology;
- prove ADC design with current 10 kA/cm^2 low-Tc technology.

Inter-relation between the proposed projects

The efforts on the project SE technology are favourably in close connection with each of the application fields in order to directly support the successful accomplishment of the three main research projects.
Three application-oriented projects are supported by dedicated development of SE technology which comprises the particular fabrication processes and the specific design capabilities for devices and circuits. A European SE Network of partners control the interaction of the projects.