7th RTD Framework Program

REALITY

Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies

Contract No 216537

Deliverable D7.7

Final project report

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The REALITY Consortium consists of:

Interuniversity Microelectronics Centre (IMEC vzw)	Prime Contractor	Belgium
STMicroelectronics S.R.L. (STM)	Contractor	Italy
Universita Di Bologna (UNIBO)	Contractor	Italy
Katholieke Universiteit Leuven (KUL)	Contractor	Belgium
ARM Limited (ARM)	Contractor	United Kingdom
University Of Glasgow (UoG)	Contractor	United Kingdom

1. Disclaimer

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2. Acknowledgements

3. Document revision history

Date	Version	Editor/Contributor	*Comments*
17/09/2010	V0.1	Miguel Miranda	First draft
30/09/2010	V0.3	Andrew Brown, Paul Zuber, Ben Geeraerts, Andrea Acquaviva, Yves Laplanche, Giuseppe Desoli	Technical inputs from most partners for the different WPs.
1/10/2010	V0.5	Andrew Brown, Paul Zuber, Ben Geeraerts, Andrea Acquaviva, Yves Laplanche, Giuseppe Desoli, Miguel Miranda	Update from technical inputs from all partners. Most tables of resources in Section 12 are completed. Project management sections to be done
2/10/2010	V0.6	Miguel Miranda, Andrea Acquaviva	Update from UNIBO and IMEC on table of resources
3/10/2010	V0.7	Miguel Miranda	Project Management added
5/10/2010	V0.8	Yves Laplanche	ARM's explanation of resources added
4/10/2010	V1.0		First Final Version
7/10/2010	V1.1	Yves Laplanche, Andrea Acquaviva	Updates on table of resources for ARM and UNIBO
15/12/2010	V1.2	Eleonora Medeot, Bruno Jansen	Updates including audit certificates from ARM and UNIBO

4. Preface

The scope and objectives of the REALITY project are :

- Development of design techniques, methodologies and methods for real-time guaranteed, energy-efficient, robust and adaptive SoCs, including both digital and analogue macro-blocks“

The Technical Challenges are :

- To deal with increased static variability and static fault rates of devices and interconnects.
- To overcome increased time-dependent dynamic variability and dynamic fault rates.
- To build reliable systems out of unreliable technology while maintaining design productivity.
- To deploy design techniques that allow technology scalable energy efficient SoC systems while guaranteeing real-time performance constraints.

Focus Areas of this project are :

- “Analysis techniques” for exploring the design space, and analysis of the system in terms of performance, power and reliability of manufactured instances across a wide spectrum of operating conditions.

- “Solution techniques” which are design time and/or runtime techniques to mitigate impact of reliability issues of integrated circuits, at component, circuit, architecture and system (application software) design.

The REALITY project has started its activities in January 2008 and is planned to be completed after 30 months. It is led by Dr. Miguel Miranda of IMEC. The Project Coordinator is Dr. Miguel Miranda from IMEC. Five contractors (STM, ARM, KUL, UoG, UNIBO) participate in the project. The total budget is 2.899 k€.

5. Abstract

This report is deliverable D7.7: “Final report”. The reporting period covers from M25 until M32. Hence it covers roughly the last semester of project execution after the second review meeting.

6. List of Abbreviations

REALITY	Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies
CAD	computer aided design
DSP	digital signal processing
HW	Hardware
IC	integrated circuit
SoC	system on chip
SW	Software

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PROJECT PERIODIC REPORT

Grant Agreement number: 216537

Project acronym: REALITY

Project title: “Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies”

Funding Scheme: Collaborative project (STREP)

Date of latest version of Annex I against which the assessment will be made:

Periodic report: 1st ☐ 2nd ☐ 3rd ☒ 4th ☐

Period covered: from 01/01/2010 to 31/08/2010

Name, title and organisation of the scientific representative of the project's coordinator:

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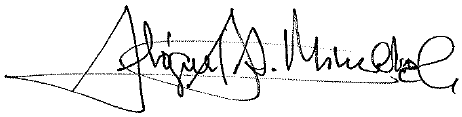
10. Declaration by the scientific representative of the project coordinator

I, as scientific representative of the coordinator of this project and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;
- The project has fully achieved its objectives and technical goals for the period;
- The public website is up to date, if applicable.
- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project and if applicable with the certificate on financial statement.
- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 15 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

Name of scientific representative of the Coordinator: Miguel Miranda Corbalan

Date: 17/09/2010



Signature of scientific representative of the Coordinator

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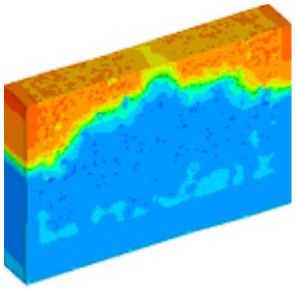
11. Publishable summary: "Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies"

Project Facts:

- FP7 Project : European Community funded
- Coordination : IMEC
- Website : www.fp7-reality.eu
- Duration : 30 Months
- Effort : 382 person-months
- Industry : ARM (UK), ST Microelectronics (Italy)
- Start date : 1st January 2008
- University : Glasgow (UK), Bologna (Italy), Leuven (Belgium)
- Research Centre : IMEC (Belgium)

Scope:

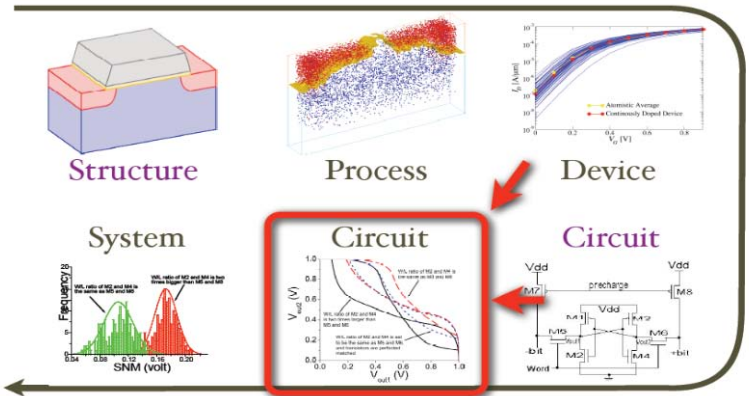
- Scaling beyond the 32 nm technology
- Tackle the increased variability and changing performance of devices from device unto system level.



Random discrete dopants in a 35 nm MOSFET from the present 90 nm technology node.

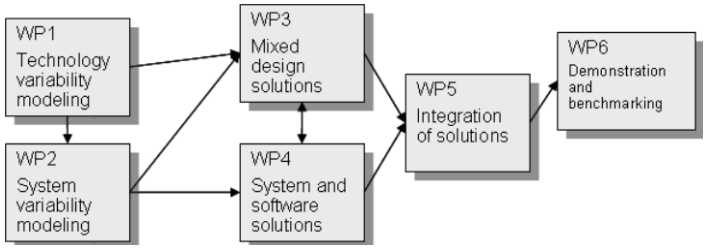
Challenges:

- Increased static variability and static fault rates of devices and interconnects.
- Increased time-dependent dynamic variability and dynamic fault rates.
- Build reliable systems out of unreliable technology while maintaining design productivity.
- Deploy design techniques that allow technology scalable energy efficient SoC systems while guaranteeing real-time performance constraints.



Proposed solution:

- System analysis of performance, power, yield and reliability of manufactured instances across a wide spectrum of operating conditions.
- Generally applicable solution techniques to mitigate the impact of reliability issues of integrated circuits, at component, circuit, and architecture and system design.



WP1: Device variability and Reliability Models (WP leader: UoG)

Having completed the simulation of variability in the 32nm devices including random discrete dopants, line edge roughness and metal gate granularity, this was used as a starting point for investigating reliability issues due to the trapping of electrons and/or holes in defect states in the gate stack during circuit operation. To each fresh device were added additional fixed charges, randomly within the channel, based on the trap sheet density, and a full 3D simulation was performed. Distributions of threshold voltages and V_T shifts were obtained.

Using the strategy for statistical compact model extraction developed in the project for use with PSP compact models, a statistical library of compact models was created based on the 32nm technology. This can be used for Monte Carlo statistical circuit simulation. An approach based on Principal Component Analysis of the data extracted from the statistical device simulations, which allows correlations between extracted parameters to be maintained, has been developed for on-the-fly calculation of statistical model parameters.

Using the statistical compact models developed for the 45nm technology, including different levels of NBTI/PBTI degradation, a detailed investigation of the effect of statistical variability and reliability on the performance of an SRAM cell was performed.

ARM has used the output of the cell level characterisation from WP5 and WP6 to analyse the difference between the statistical models from the foundry and from UoG available in the project through the variability injectors generated by IMEC.

Deliverable D1.2, due at T0+27, was successfully delivered on time.

WP2: System and circuit characterization and sensitivity analysis (WP leader: IMEC)

The goal of this WP is to develop advanced methodologies and techniques for statistical analysis. The intention is to read the output of transistor level variability, as provided by WP 1, and to propagate this information all the way from the device level to the product level. The WP also targets developing and fully characterizing a limited standard cell library (50-100 cells) for synthesis and analysis based on restricted design rules for use in WP2, WP3, WP4, and WP5.

Commercial EDA solutions (e.g., fast circuit simulators, SSTA tools, power analysis tools, etc) were reused in the flow wherever possible in combination with Monte Carlo-based simulation techniques in order to guarantee the compatibility with existing electronic design simulation/verification tools and easy adoption by engineers trained to these tools. This was not always possible. Even commercial tools show bugs or are simply inappropriate for particular purposes. This can occur in any area, in particular in the areas of electrical simulation, characterization, statistical characterization, and statistical static timing analysis. Depending on case, new methods were developed and implemented, or commercial vendors were asked to revise their products.

New methods were identified in the areas of standard cell characterization (ST's hybrid flow, imec's VAM, UoG's characterizer), memory characterization (ARM's extreme value theory based memory margining application, imec's MemoryVAM), statistical timing analysis (ST's hybrid flow on the digital level, imec's VAM), as well as system level analysis (VAM).

Also considered in this WP is the strategic aspect of the standardization of the interfaces between different abstraction levels to enable the propagation of variability specific information throughout the design flow. To "lubricate" the flow developed here and applied and integrated in all other work packages, we put in place a standard electronic Information Format (IF) that keeps statistical information and exists parallel to the classical top-down and bottom-up design flows.

All deliverables (D2.3 and D2.4) have been submitted on time.

WP3: Mixed mode countermeasures (WP leader: KUL)

In work package 3, an advanced reliability simulation technique including process variability in the simulation flow was developed. In order to get a computationally efficient solution, a Response Surface Model (RSM) based simulation technique is proposed. In this approach the vast number of computationally intensive simulations needed to perform a Monte-Carlo analysis, is replaced by the evaluation of an analytical model of the circuit. The focus of this work is not to obtain a highly accurate prediction of yield, but to analyze the spatial and temporal reliability of a circuit in a reasonably short time frame. When compared to direct Monte-Carlo yield simulation, examples indicate this method to have a simulation speedup ranging from 1 to 3 orders of magnitude, without sacrifying accuracy. Additionally, weak spot analysis allows to improve the design or to reduce design margins and to gain extra performance.

Also, with the availability of the 32nm compact models, an extra iteration on the KUL SRAM memory has been done. The reliability simulation framework has been applied to one cell of the KUL memory (full memory analysis is performed by the MemoryVAM). A huge amount of minimal sized cells, of which the functionality of every single one is critical demands big design margins. The most vulnerable parts of a memory were identified to be the cells, the sense amplifiers and the timing. Cell stability can be increased by reducing the cell load capacitance. For this reason, divided bit lines are introduced. Additional advantages include possible speed and energy gains. The impact of NBTI, on the performance of one cell has been simulated as a function of cell voltage. Other improvements include sharing sense amplifiers and usage of a configurable timing circuit to reduce variability effects. Some estimations of the effect of BEOL-variability have been done. At this moment, these variations seem to have a limited effect due to the averaging out for the big wires and the small impact of small wires. A fully functional 1KB SRAM memory with a word length of 32bit was build. The obtained speed was 1GHz. Total write energy was 0.69pJ, read energy was a bit higher: 1.07pJ.

WP4: System level countermeasures (WP leader: UNIBO)

The activity of UNIBO in year 3 has been devoted to the porting and optimization of system level policies to the target platform and validation benchmark. We evaluated the capability of the techniques to compensate the variability impact on application performance. The impact of variability on multicore multimedia platform makes hard to get the a certain QoS from the running software because of the speed variations across the cores, which causes a sub-optimal exploitation of the platform parallelism. Moreover, QoS and power consumption vary from platform to platform.

Thanks to a smart allocation of the workload, it is possible to compensate this impact, obtaining an improvement of the QoS and energy consumption for a given platform as well as an increase of the predictability across many variability affected platforms. System level compensation allows to better guarantee the QoS with respect to a non compensated one. Indeed, a smart workload allocation strategy applied to a variability affected platform, helps reducing the deadline misses and reduces the energy consumption.

During the reporting period, we optimized the workload allocation policies so that they can be applied on-line on a frame-by-frame basis. The optimization was targeted to the reduction of the execution time of the policies, to provide the wanted QoS level with minimum energy, independently form the variability impact on the platform. The techniques have been ported to a relevant industrial case study of a multicore multimedia platform, with a single voltage domain, multiple frequency domain. Since variability causes the cores to be characterized by different speeds, the designer can tune each core to its maximum supported frequency to improve performance. However, now he/she has to handle a heterogeneous platform. This may cause inefficiencies when allocating multitask applications, because the speed heterogeneity lead to a unbalanced allocation. This effect can be compensated by a smart allocation, thanks to which the designer can exploit the advantage of having clocked the system in a heterogeneous way without paying the price of the unbalancing and thus overall leading to a better QoS with respect to a non-compensated platform.

WP5: Design flow, integration, proof of concept (WP leader: ARM)

No summary available. These work package activities have been completed during the earlier reporting period.

WP6: Validation and assessment of results (WP leader: ST)
This WP reported on the analysis, validation and industrial impact for all of the REALITY outcomes.
The validation and benchmarking revolved around a two pronged strategy based on the leverage of an industrially proven embedded microprocessor design provided by ARM, the ARM926, and an advanced

multiprocessor based multimedia accelerator platform from STM, the xSTream platform. Much of the project conclusions are gathered in the reports produced by WP6.
For the first time, full scale 3D simulation of statistical variability associated with metal gate granularity and the corresponding metal work function variations has been carried out to clarify the magnitude of statistical variability in 32 nm CMOS transistors with high-k/metal gate stack. In addition, technology has been developed to simulate the statistical aspects of reliability associated with NBTI/PBTI.
Also for a first time, a full statistical characterization of an ARM core has been achieved. A correlation between the timing, leakage and dynamic power has been demonstrated on local (within die) and non-local (above die) variations. The traditional corner analysis could be benchmarked with innovative statistical analysis techniques. Using the ARM core as driver, REALITY has confirmed that the SRAM components are responsible for more than the half of the variations on critical path timing. Much focus has been placed by both state-of-the-art and EDA vendors on the logic while the variability challenges remain in the memories themselves. For that purpose REALITY has been also first in deploying a holistic statistical characterization flow including SRAM analysis variations at and their evolution over time.
REALITY has also for first time evaluated the impact of process variation in SW level metrics showing process variability is not only a concern for HW but for SW as well. It has concluded that variability affecting multi-core multimedia platforms makes it hard to guarantee a certain QoS from the running application's functionality. The speed variations across the cores cause sub-optimal and platform-dependent parallelism. REALITY has developed an approach to compensate this by using a smart allocation of the workload at run-time, hence also at the SW level, and obtaining an improvement of QoS by 20% and energy consumption by 15% while obtaining better platform predictability.
For that purpose, different circuit design techniques for system adaptation have been investigated, among them Adaptive Body Biasing (ABB). REALITY has shown that even though the possible compensation range in speed up due to ABB is significantly reduced compared to the previous node, it remains still available at 32nm. The technique has been validated on the ALU design of the ARM core using specially characterized commercially available libraries.
The xSTream platform was used as a test case for a system level driver and benchmarking environment to develop and validate multitask sw allocation and scheduling policies in the presence of different kinds of variability 'control and measuring knobs'.
To enable the project to obtain trends and projection on real industrial application retrofitted with such sw control stacks, the system platform needed to be an executable model capable of supporting real-time simulation of applications. The system level validation and benchmarking activities carried out in WP6 have resulted in hundreds of simulation trials were a number of parameters were changed by selecting statistical relevant distributions produced by the IP block variability analysis flows. Results were analyzed in terms of multiple objective metrics keeping power consumption, yield, area and cost into account. The final impact analysis carried out in WP6 did not attempt to exhaustively provide a coverage of all of the advantages and drawbacks; but rather identified and highlighted the concrete impact, for example in terms of adoption of the variability characterization flow, variability aware design techniques, sw and hw countermeasures, when applied to pragmatic product like development conditions measured by a choice of objective industrially relevant metrics applied to pragmatic product like development conditions.

Objectives for the period 2, Project M24 until M32

The reporting Period 3 covers the project time-schedule M24 until M32, i.e. starting from 1st January 2010 until 31st August 2010. This report is a progress report for such period. Also serves a final report.

Description of the performance / research indicators (all targets for Y3 have been met!)

WP	After year 1	After year 2	At end of project
WP2 Circuit to System Variability	Preliminary version of a RDR std. cell library [32nm]. Flow definition and framework set up for variability characterization. Correlated variability energy timing flow definition and set up.	Variability characterization of a [32nm] RDR std cell library. Exploitation of the variability aware modelling flow on the driver application vehicle, including a solution for IP blocks and memories.	Methodology fine tuned. Feedback from benchmarking acknowledged.
WP3 Mixed design	Description of the variability and reliability analysis methods at circuit level	Demonstration of the developed method on SRAM and analog circuits	Validation of the developed method
WP4 Algorithm	Software techniques for flexible data and workload allocation for migration (the base flexible RTSM support)	Control algorithms for system level reliability and variability management (exploiting of the base RTSM support)	Porting, optimization and tuning for the target evaluation platform of: (a) the flexible RTSM, (b) the control algorithms
WP5 Integration	Definition of characterization blocks, macrocells, and system level architecture	Validation and application of methods to macrocells and integration into system	Final system integration, validation feeding into WP6 benchmarking
WP6 Benchmarking	Identification of relevant industrial applications and associated requirements and evaluation metrics	Definition of the validation plan Benchmarking of block level IPs	Benchmarking of system level platform Evaluation of results and impact according to validation plan criteria

12. Work progress and achievements during the period

12.1. WP1: Device variability and Reliability Models (WP leader: UoG)

Having completed the simulation of variability in the 32nm devices including random discrete dopants, line edge roughness and metal gate granularity, this can be used as a starting point for investigating reliability issues due to the trapping of electrons and/or holes in defect states in the gate stack during circuit operation. Reliability problems in sub-45 nm technology devices will have a distinct statistical manifestation and the change in the characteristics of any nano-CMOS device during circuit operation will vary depending on the actual position of single or multiple defect charges in the channel region of the transistor. We have carried out a detailed 3D simulation of the statistical distribution of the corresponding changes in device characteristics due to microscopic manifestations of particular device defect configurations.

Here we have used the same 3 densities of trapped charge, suggested by IMEC, as with the 45nm device (10^{11}cm^{-2}, 5×10^{11}cm^{-2} and 10^{12}cm^{-2}). The starting point is the 200 devices already simulated with all relevant sources of variability. In the statistical simulation of the transistor degradation, to each device was added additional fixed charges, randomly within the channel, based on the sheet density. The 200 devices were then simulated with each of the different trap densities. This additional channel charge will act to increase the absolute threshold voltage, however the shift in V_T will depend on both the actual number and the location of the original dopant charges, and on the number and location of the additional trapped charges. Figure 1 shows the distribution of V_T and the shift in V_T (ΔV_T) as normal probability plots, for the different levels of degradation in the pMOSFET.

It was seen that the shift in V_T increases with increasing trap density due to the extra negative charge at the interface. For the 45nm devices it was observed that an increasing trap density lead to an increase in σV_T due to the interaction of the additional charge with the current paths formed in the non-degraded device. The lack of a strong dependence of σV_T on the trap density in this 32nm case may be due to increased screening of the additional interface charge due to use of a metal gate compared to the poly-silicon gate used in the 45nm technology.

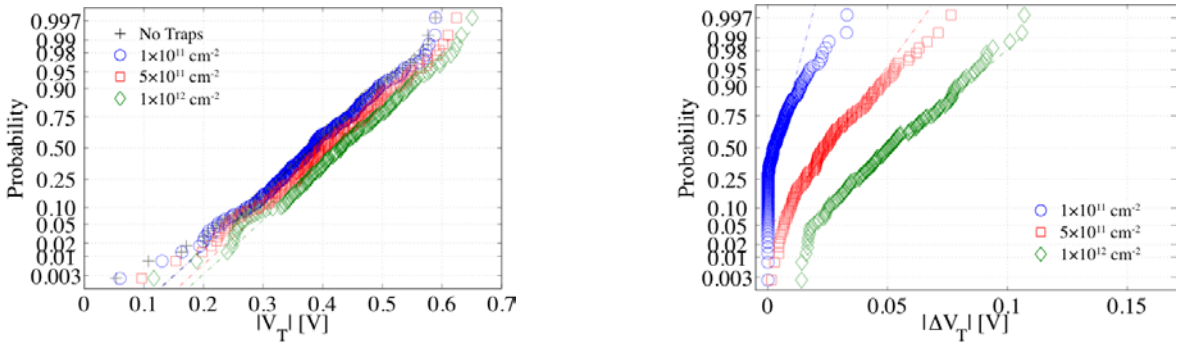


Figure 1: Normal probability plot showing the distribution of threshold voltages for different levels of degradation of the p-channel device and the associated shift in V_T from the trap-free device. V_D=-1.0V

A two-stage direct statistical compact model extraction procedure is applied without any pre-assumption of parameter distribution, correlation or sensitivity. As a result this approach will provide the most accurate representation of the current voltage characteristics obtained from physical 3D simulation or from measurement. In the first stage of the extraction process, a local level parameter extraction strategy is applied to obtain a complete set of PSP parameters for a uniformly doped device with no sources of variability. Figure 2 shows the result of the full parameter extraction for the uniform nMOSFET. Good agreement with the original simulation data from which the models are extracted has been achieved.

In the second stage, using the compact model extracted in stage one as a base, a number of the model parameters are re-extracted to account for the variation between the uniform model and the characteristics of a device affected by statistical variability. Based on the physical analysis of the impact of intrinsic statistical variability on device operation, 7 possible fitting parameters have been identified for re-extraction with PSP. Figure 3 shows the distribution of RMS errors calculated for the extraction of compact models from the

simulation of 200 devices with statistical variability, and demonstrates how the number of parameters that are re-extracted affects the accuracy of the statistical compact model cards when compared to the original simulation data from which they are extracted.

Using the ensemble of models generated by direct statistical parameter extraction, a statistical compact model library for the 32nm device has been constructed and devices in circuits can be randomly selected from the library during statistical circuit simulation. Although this is the most rigorous method of performing statistical circuit simulation, the available statistical sample size is pre-determined by size of the compact model library. Common practice in Monte Carlo circuit simulation is to generate statistical parameter values on the fly. An approach based on Principal Component Analysis (PCA) of the data extracted from the statistical device simulations, which allows correlations between extracted parameters to be maintained, has been developed.

Using the statistical compact models developed for the 45nm technology, including different levels of NBTI/PBTI degradation, a detailed investigation of the effect of statistical variability and reliability on the performance of an SRAM cell was performed. This showed that when NBTI in the pMOSFETs is considered, increasing trap density leads to a decrease in the static noise margin (Fig. 4). When PBTI in the nMOSFETs is also considered the mean of the SNM does not change but the standard deviation of SNM increases. ARM has used the output of the cell level characterisation from WP5 and WP6 to analyse the difference between the statistical models from the foundry and from UoG available in the project through the variability injectors generated by IMEC.

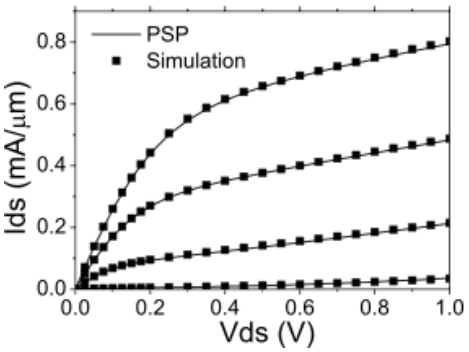


Figure 2: Fit of the extracted compact model compared to the original simulation data for the nominal nMOSFET device with no sources of variability.

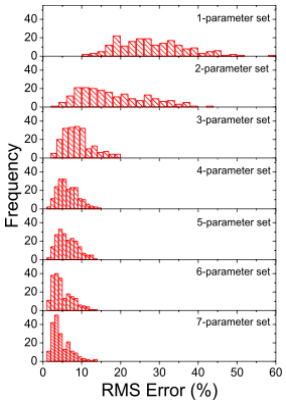


Figure 3: Distribution of RMS errors. with the number of model parameters reextracted.

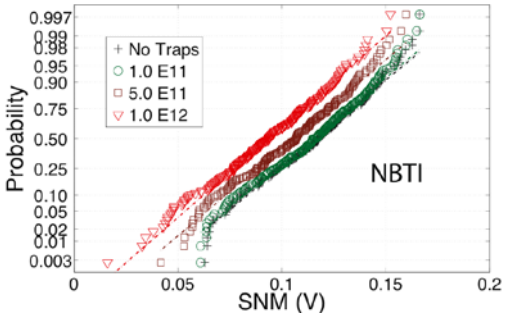


Figure 4: Normal probability plot of static noise margin for different degradation stages of NBTI

Use of resources

Partner	*Planned effort (MM)*	*Actual effort (MM)*
UOG	*6*	*16.3(*)*
IMEC	*0*	*0*
UNIBO	*0*	*0*
ST	*0*	*0*
KUL	*0*	*0*
ARM	*0.8*	*0.8*
TOTAL	*6.8*	*17.1*

(*) Unforeseen extra time spent on the simulations of n/pbti with the metal gate, particularly looking at unexpected results, meant that extra manpower was required to deal with extraction of compact models, using and refining the new PSP extraction strategy. Additionally, extra work was done to demonstrate the value of our statistical compact models in a full investigation of the effects of statistical reliability issues in SRAM cells. Luckily we were able to resource this within budget due to the favourable exchange rate between the pound and the euro.

12.2. WP2: System and circuit characterization and sensitivity analysis (WP leader: IMEC)

12.2.1. (Task 2.1.1) – Statistical Characterization of Standard Cell Libraries

Local random mismatch will potentially increase design working frequency. Mismatch requires extra margins for skew and pulse width, thus impacting achievable performance. Using larger cell size to reduce mismatch conflicts with tight area and power constraints in advanced nanometer technologies. In the reporting period ST I has developed a local random mismatch-aware Static Timing Analysis (STA) technique that can provide a bridge between traditional Deterministic STA (DSTA) and Statistical Static Timing Analysis (SSTA), in the frame of the Hybrid Statistical Timing Analysis (HSTA) flow concept proposed in Task 2.3. The impact of mismatch was characterized at cell level and used to predict the mismatch impact on paths for digital clock networks within 10% error margin that in absolute terms is within few picoseconds. This mismatch characterization activity was mainly focused on including the mismatch impact in clock-tree network design. The approach can be implemented in current timing analysis tools using inputs from traditional DSTA, to derive advanced (and less pessimistic) margins. It builds on a mainstream DSTA technique and thus is easily implementable in current design flows, and its novelty stems from the compromise on error margins to enable fast implementation time and minimal overheads. The error margins are within acceptable limits.
Silicon-proven industrial models were used to characterize the impact of mismatch. Standard cells were taken from ST 45nm CMOS production library (same technology used for previous activity on statistical characterization), and it was used a realistic interconnect model with the resistance to capacitance ratio extracted from ST industrial 45nm process for routing interconnects to include slew degradation and have a comparable reference of path depth to design size. Realistic clock paths were constructed using automated scripts enforcing clock-tree design rules. The goal of mismatch-aware STA was to predict the statistical $\mu \pm 3\sigma$ (average shift, standard deviation) limits around corner cases.
It was achieved a good level of accuracy through mismatch-aware STA to calculate the impact of mismatch on different parameters in a clock-tree path. Verification using Monte Carlo simulations on different configurations validated this approach, which can be easily implemented in current design flows with small overheads. Therefore, it was established a direct and effective link between the advanced R&D activities carried out in WP2 during the first phase of the project, and a fast industrial exploitation.

In 2010 ARM has invested time on the SSTA characterization of the standard cells libraries. The task started in 2009 lead to an evaluation of the accuracy of the flow. At that time the conclusion of the study had us stop investigations on this flow. Following the latest improvements from our tool provider ARM wanted to analyse a little bit more the potential of a commercially available flow. We are currently trying to put in place a flow to validate the information extracted from higher level designs in order to verify the complete approach.

ARM has also spent some efforts to go on debugging the classical characterization flow in order to adapt it to the needs of the VAM characterization. The team was challenged on the repeatability of the flow. A clean definition of the spice options has to be defined in order for all the characterization to go through with the same simulation condition which is necessary for an accurate comparison of the results. The high number of characterization necessary for one Temperature / Voltage condition also challenged to team on a good robustness of the process in order not to loos time due to high failure rates during the simulations.
In addition the minor improvements in the memory statistical characterization tool have been carried out in parallel with an effort spent to transfer the knowledge generated in the project to other groups in the company leading to an effort increase in this work package.
A memory critical path slice of the memory designed in WP3 was made by K.U.Leuven. As this memory is a complex hierarchically structured circuit, a lot of effort was spend in making sure equivalent load capacitances were added on all levels while still trying to remove as much circuitry as possible in order to decrease simulation time. Testbenches for memory energy, memory delay and hold time were made. These tests were run with MVAM.

12.2.2. (Task 2.3) - Hybrid (corner/statistical) Statistical Analysis flow for Digital Blocks

Statistical analysis solutions for random within-die (WID) variations (such as the local random mismatch) available today are quite complex for an effective industrial exploitation. Most approaches for WID variations are focused on systematic mismatch, which can be ameliorated by means of manufacturing-driven improvements (regular design, restricted design rules, resolution enhancement techniques). In REALITY ST I demonstrated that Statistical Static Timing Analysis (SSTA) is a good estimator of random WID variations, but in general, it lacks ease of deployment in an industrial environment, and requires a lot of efforts to characterize the statistical libraries. Moreover, it also true that chip designers in an industrial environment, who have to satisfy tough turn-around-time requirements, and have to meet strict time-to-market windows dictated by an increasingly fierce competition, do not want to change the traditional sign-off methodology for timing verification based on DSTA.

Therefore, it is necessary to develop a rapidly deployable solution based on existing and reliable commercial CAD tools and an industrial digital design flow, which also uses industrial models to reduce the impact of random intra-die variations at the cell level. Moreover, it is necessary to define the basic set of process parameters to effectively characterize the standard cell libraries. The objective of this activity (Task 2.3) was to develop a hybrid statistical analysis flow based on commercial DSTA tools and a new technique to consider the impact of random WID variations (i.e., device mismatch characterized in Task 2.1.2). By means of this approach it was possible to analyze the local random variations without using the traditional design margins (based on derating factors) are either pessimistic or risky, as it was demonstrated in WP2. The hybrid flow allows reducing the design margins and removing some pessimism, without changing the digital sign-off flow and methodology. To enable this hybrid flow, new techniques to characterize statistical libraries including the contribution of local device mismatch have been defined in order to avoid running a full Monte Carlo analysis, which is extremely time-consuming.
The Hybrid Statistical Timing Analysis (HSTA) flow developed during the reporting period is outlined in Figure 4.

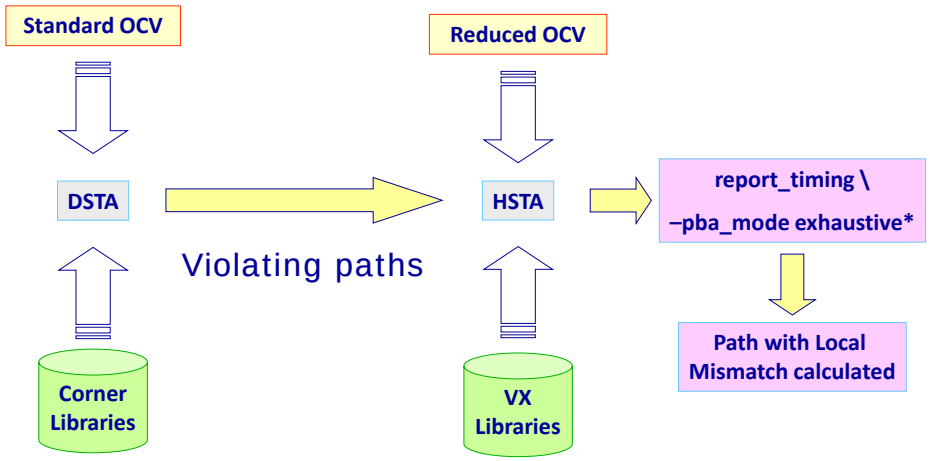


Figure 4. Hybrid statistical timing analysis flow

This approach was used to evaluate the impact of random mismatch variations on digital designs in ST CMOS045LP (45nm low-power) technology. The trial design considered is a digital core (Figure 5), whose characteristics are the following:

- 200K nets;
- Main clock period (CLK): 2.2ns;
- Highly tuned for high-speed and low-power;
- Representative of CPU's in majority of future ST designs;
- Main clock insertion delay: about 1.3 ns.

2297 setup and 4926 hold path were analyzed. In terms of runtime, overall 1K single path per minute was processed on fast machine. Some relevant flow performance data are reported in Table 1.

Figure 5. Digital core layout

Table 1. Flow performance data

	Step	Host	Runtime
DSTA	Import data	Dual Core Xeon 3GHz, 16GB	1m 14s
	Update timing		5m 13s
HSTA	Setup (2297 paths)	Quad Core Xeon 3.33GHz, 32GB	2m 11s
	Hold (4926 paths)		4m 19s

The HSTA flow developed and exercised during the reporting period will be used at ST to consider the impact of process variations during timing verification. The preliminary results are quite encouraging, both in terms of reduced pessimism and reduced turn-around-time.

12.2.3. (Task 2.4) – System Level Statistical Analysis

A SoC comprises high-level components such as processors, memories, accelerators, etc. The large majority of SoCs contains well defined register boundaries between any of these high-level components. We have concluded that the statistical critical timing of the SoC is the maximum of the timing of any of its components, and the statistical energy (for dynamic) and power (for leakage) is the sum of their individual energy/power, we can formalize the statistics of the SoC in base of two stochastic properties:

- The Cumulative Density Functions (CDF) of the maximum value of two stochastic variables is the product of their CDF;
- The Probabilistic Density Functions (PDF) of the sum of two stochastic variables is the convolution of their PDF.

The idea was implemented and benchmarked on a wireless processor with good accuracy and excellent runtime results. Having a complete framework for variability impact propagation of correlated timing and power metrics enables the co-exploration of the design and manufacturing space. These can include technology options, like evaluations the impact of high-k metal gates or high/low Vth devices; manufacturing options, like restricted design rules; circuit options, like threshold voltage assignment in MTCMOS libraries or different circuit architectures; architecture options, like memory organization partitioning versus aggregation.

12.2.4. (Task 2.5) – Variation Information Format Framework

A key part to “lube” the complexity and density of information of any variability aware design flow is a “Variability Aware Modelling information format” (VAM IF). Thus imec developed a format that considers connections between five levels of abstraction of modelling or simulation. It defines how variability information must be carried from the one level to the other, and was used throughout the WP’s of REALITY.
The format accepts data from WP1 in form of injectors. These are additional circuit elements that model the variability of transistors. This can be done for several transistor types, but also differently degraded transistors. The information format is also capable of storing and retrieving variability data on higher levels, such as the ones worked out in WP2, WP3, WP4, and integrated in WP5, like variable standard cells, memory macros, processor parts, processors or systems thereof. Its application layer allows to graphically publish the variability information in several formats. This is used heavily in almost all workpackages, especially WP6.

Use of resources

Partner	*Planned effort (MM)*	*Actual effort (MM)*
UOG	*0*	*0*
IMEC	*2.4*	*2.4*
UNIBO	*0*	*0*
ST	*5*	*5*
KUL	*0*	*0(*)*
ARM	*0*	*4(**)*
TOTAL	*7.4*	*11.4*

(*) KUL had a contribution in WP2 in 2010 but that one has been made free of cost to the project
(**) *An additional effort has been spent on characterization with VAM to adapt our flow to the needs of WP6. What is more in 2009 we have demonstrated that the SSTA characterization of the cell for local variations was failing. We have done some more investigation on this topic after the release of new tools versions. The team has spent some more time in the SRAM characterization transfer to the production groups.*

12.3. WP3: Mixed mode countermeasures (WP leader: KUL)

In this work package, an advanced reliability simulation technique including process variability in the simulation flow was developed. Also, with the availability of the 32nm compact models, an extra iteration on the KUL SRAM memory has been done. The reliability simulation framework has been applied to one cell of the KUL memory (full memory analysis is performed by the MemoryVAM).

Efficient variability-aware reliability simulation

In order to get a computationally efficient solution, a Response Surface Model (RSM) based simulation technique is proposed. In this approach the vast number of computationally intensive simulations needed to perform a Monte-Carlo analysis, is replaced by the evaluation of an analytical model of the circuit. The focus of this work is not to obtain a highly accurate prediction of yield, but to analyze the spatial and temporal reliability of a circuit in a reasonably short time frame. To reduce the simulation complexity the set of design of experiments, used to build the RSM, is divided into two parts. First, a screening analysis with linear complexity provides a linear model and eliminates unimportant design parameters. Then, in a second step, a regression analysis is conducted to model significant non-linearities. Finally, as an output, the analysis tool provides:

- An aged version of the circuit netlist.
- A model for the behavior of any circuit performance parameter as a function of process-variability parameters and circuit age.
- The production yield as a function of circuit age.
- The estimated model error and yield error.
- A list with circuit reliability weak spots.

When compared to direct Monte-Carlo yield simulation, examples indicate this method to have a simulation speedup ranging from 1 to 3 orders of magnitude, without sacrificing accuracy. The simulation results enable a designer to verify whether his/her circuit will behave according to its specifications over the entire product lifetime. Also, weak spot analysis allows to improve the design or to reduce design margins and to gain extra performance.

Table 1: The reliability analysis technique was validated on a set of 7 analog and digital test circuits. Experiments show fast simulation results (under 10 minutes for all test circuits) with good accuracy (<2% error).

	#factors/ #NRS	$\overline{\varepsilon_{\text{ols}}}$ [%]	$\sigma_{\varepsilon,\text{ols}}$ [%]	$\hat{\sigma}_{\varepsilon,\text{ols}}$ [%]	$\frac{\sigma_{\text{p}}}{\sigma_{\varepsilon,\text{ols}}}$	Analysis Time [min:sec]
1	5/19	0.04	0.57	0.65	45.9	1:28
2	14/43	-0.31	1.44	1.19	16.2	2:32
3	15/53	-0.09	0.28	0.46	74.0	3:37
4	27/95	-0.20	0.41	0.40	47.4	4:46
5	35/121	0.14	1.30	1.01	12.6	9:09
6	20/61	0.01	0.26	0.26	94.8	2:06
7	141/343	-0.12	0.98	1.10	22.3	9:46

[1]: One-stage Amplifier [Gain]
[2]: LC-VCO [V_{osc}]
[3]: Differential Pair Amplifier [Gain]
[4]: Symmetrical OTA [Offset]
[5]: Ring Oscillator [Frequency]
[6]: AND Gate [Fall Time]
[7]: IDAC [Normalized Output Voltage ($\frac{V_{out}}{RI}$)]

Design of variability resilient memory blocks

By occupying a major part of the area of current SoCs, memory design is specifically important in the context of variability and reliability. A huge amount of minimal sized cells, of which the functionality of every single one is critical demands big design margins. The most vulnerable parts of a memory were identified to be the cells, the sense amplifiers and the timing.

Cell stability can be increased by reducing the cell load capacitance. For this reason, divided bit lines are introduced. Additional advantages include possible speed and energy gains. A new metric, the transient static noise margin can be used to get a more realistic prediction of the stability. The effect NBTI when increasing the cell voltage has been simulated. It seems to be not negligible, but also not dominant.

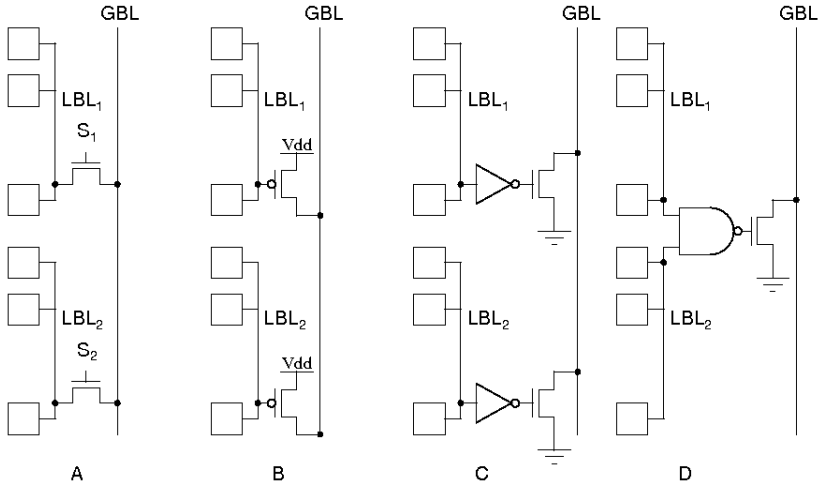


Figure 6 Different local bit line architectures

Sharing sense amplifiers result in less variability both due to the reduction in number of SA's as due to the possibility to increase their size with less energy or are penalties.

A configurable timing circuit can be used to counter variability in the timing, but also to adapt the memory control on a die basis to the specific cell and sense amplifier speed thus reducing speed and energy loss due to pessimistic margin design. Low power configurable delay lines were designed for this purpose.

Some estimations of the effect of BEOL-variability have been done. At this moment, these variations do not seem to have a big effect due to the averaging out for the big wires and the small impact of small wires.

A fully functional 1KB SRAM memory with a word length of 32bit was build. Used features include fully divided word lines, divided bit lines, low swing on the global bit lines for read and write, local sense amplifiers, a dynamic x decoder, high threshold voltage cells, shared global sense amplifiers etc. The obtained speed was 1GHz. Total write energy was 0.69pJ, read energy was a bit higher: 1.07pJ.

Use of resources

Partner	*Planned effort (MM)*	*Actual effort (MM)*
UOG	*0*	*0*
IMEC	*0*	*0*
UNIBO	*0*	*0*
ST	*0*	*0*
KUL	*11*	*10.8*
ARM	*0*	*0*
TOTAL	*11*	*10.8*

12.4. WP4: System level countermeasures (WP leader: UNIBO)

During the reporting period M25-M32 the activity of WP4 was completed in M27. The final deliverable D4.3 was submitted to the EC. In this deliverable UNIBO reported the optimization of the policies on the target platform. The selected benchmark where the optimization has been performed is a multithreaded MPEG2 video decoder, ported to the target platform as part of the activity in WP6 in collaboration with ST.

ST and Unibo have been tuning the SW control algoritms for system level variability management adjusting both the model implementation in the simulation platform and the definition of the SW task scheduling policies to better adapt to the outcomes of the benchmarking campaign performed in WP6. The work has revolved around refinements of the implementation and choice of parameters associated to the BP_LP and other policies, integration of the performance monitoring blocks parameters validation results (leakage meter, speed meter, temperature sensor), and thermal modelling.

The application is composed of three parts: a control part which scans the current frame, a slice decoding, and an inverse discrete cosine transform (IDCT). There is also a fourth step, performed after the decoding of each frame, associated with the commit of results. We modified the program so that the scan of the current frame is performed by the GPE, the slice decoding and the IDCT can be parallelized and executed on a generic number of xPEs, and the commit of results is performed by the GPE.

The slice decoding and the IDCT have been divided in independent tasks whose number can be equal or greater than the number of xPEs. Regarding the latter case, a dispatcher has been implemented on the host core to schedule the different tasks on the xPEs. To increase performances we further modified the code to execute the commit of the previous frame during the execution of the current frame on the xPEs. The task execution model is shown in Figure XX1, where it is also shown how the task allocation policy, developed in WP4, is applied to the MPEG2 benchmark and optimized.

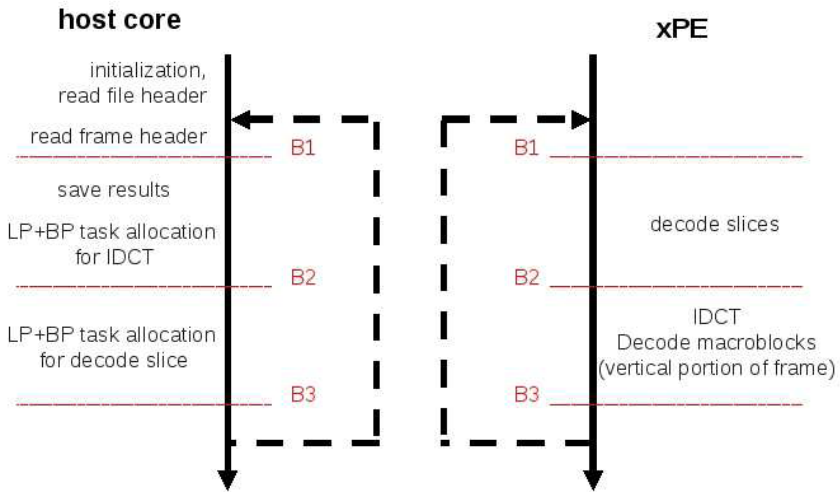


Figure 7 Task allocation policy applied to the MPEG2 benchmark

More specifically, there are two functions parallelized that are IDCT and decode slice. These two functions generate a number of tasks, which is a parameter. For each of the two functions the task allocation policy (LP+BP) is applied (phases B2 and B3).

The optimization performed on the policy was targeted to make possible the on-line workload allocation on a frame-by-frame basis. In particular, during the processing of a single frame, the policy is applied two times. The first time for the allocation of the tasks performing the parallel slice_decoding function, and the second time for the allocation of the tasks performing the IDCT function.

In order to make this possible, we implemented a fast version of the LP algorithm. This allows to reduce the computation time of the LP part of the policy, making it possible to be executed during frame decoding. Another optimization was performed on the BP part of the policy. Here we implemented a new customized version which has the objective of improving the deadline miss rate with respect to the original one. The customized version exploits the information about time constraint, explicitly provided by the application or by the user, to allocate the tasks on the processors. The original implementation of the bin packing algorithm does not take this information into account, while it tries to minimize the exceeding cycles when fitting a task into a core.

We performed our tests on the variability-aware platform simulator developed with ST microelectronics and characterized using the variability models generated by VAM (see D4.3). The results reported in D4.3 have demonstrated firstly that the proposed policy have a negligible run-time overhead and thus it can be applied online. Secondly, they allow to compensate the effect of variability on the quality of service (i.e. number of missed frames) and that they improve reference state-of-the art policies, providing better quality and more predictability across degraded platforms. Finally, the proposed policy achieves this results while minimizing the energy consumption.

Table 2 Fraction of deadline misses caused by the various policies for different number of tasks for the slice decoding and IDCT functions.

	RANDOM	RANK FREQ	RANK POWER	LP+BP
4-task	1.00	0.40	0.88	0.40
8-task	0.00	0.00	0.00	0.00
12-task	0.12	0.00	0.00	0.00

Table 3 Energy consumption for different number of tasks for the slice decoding and IDCT functions.

	RANDOM	RANK FREQ	RANK POWER	LP+BP
4-task	0.69	0.50	0.62	0.50
8-task	0.78	0.75	0.76	0.59
12-task	0.77	0.75	0.75	0.55

A summary of these results are reported in Table XX1 and XX2. In the rows there are different level of parallelism for each kernel of the MPEG2 application, while on the columns we compared the proposed policy (LP+BP) with competitors (RANK FREQ and RANK POWER) and a random allocation. Figure XX1 reports performance results in terms of deadline misses, while Figure XX2 in terms of energy consumption. It can be seen that LP+BP result in frame misses only with 4 tasks. This result is because of the too low parallelism, indeed all the other policies have the same or worse results. On the other side, the proposed policy consistently reduces the energy consumption.

Use of resources

Partner	***Planned effort (MM)***	***Actual effort (MM)***
UOG	*0*	*0*
IMEC	*0*	*0*
UNIBO	*0.25*	*7(*)*
ST	*2*	*2*
KUL	*0*	*0*
ARM	*0*	*0*
TOTAL	*2.25*	*9*

(*) The actual number of actual MMs effort is for UNIBO higher than initially planned because we used much more junior resources than expected that resulted in more PMs. As a consequence, there is not impact on the budget.

12.5. WP5: Design flow, integration, proof of concept (WP leader: ARM)

No summary available. These work package activities have been completed during the earlier reporting period.

Use of resources

Partner	*Planned effort (MM)*	*Actual effort (MM)*
UOG	*Not Applicable (NA)*	*NA*
IMEC	*NA*	*NA*
UNIBO	*NA*	*NA*
ST	*NA*	*NA*
KUL	*NA*	*NA*
ARM	*NA*	*NA*
TOTAL	*NA*	*NA*

12.6. WP6: Validation and assessment of results (WP leader: ST)

Task 6.4:

Although this task completed in the past reporting period, certain results had to be amended and/or augmented from what reported in D6.3. Further simulation and analysis were performed as some of the preconditions on the availability of input data become available as part of the activities in WP2, WP4 and WP6. These additional results were reported and included in D6.4.

In particular in 2010 Imec (free of effort) together with ARM has invested significant effort amending and extending some of the results reported earlier in D6.3 in a clearer and more explicit way. This has involved performing a whole new set of statistical characterization jobs for library characterization (ARM), memory characterization (imec) and processor core characterization (imec). The reason is the block level evaluation report as specified by the validation plan (D6.3) was approved on condition that deficiencies will be corrected in this report. In concrete we have:

- Provided imec's statistical memory characterization tool and supported its use to clarify the sources for ARM's and KUL's memory performance mismatches.
- Performed characterization runs of our tools in validation conditions (e.g., temperature, voltage and process) not reported in D6.3 applicable to the synthesis and analysis of the block-level test vehicle.
- Provided additional characterization runs for an assessment of the variability degradation at the level of the system's building block (ARM926) for the case 0.9C 125C (thus, worst case conditions). We have used strongly aged variability injector models (trap concentration of $1x10^{12}cm^{-2)}$ which influences local random variability while process-dependent global variability remains constant. The results point to non notable effects in timing, leakage and/or dynamic energy variability under ageing. We conclude that ageing impact on timing and/or power deviations on the statistical response of the core using high-K metal gate devices is at 32nm negligible.

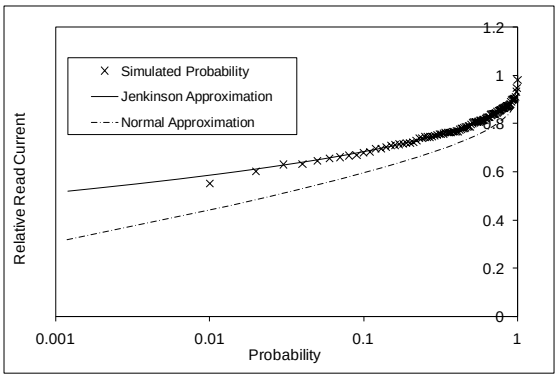
In addition Imec has in 2010 provided (free of effort) an analysis of project results impact for selected industrial scenarios. In concrete it has quantified the impact of memory variability within a system, concluding that SRAM components are responsible for more than the half of the variations on critical path timing. Hence, Statistical Timing Analysis (SSTA) flows that assume predictable timing response from these components lead to over-optimistic conclusions. Much focus has been placed by both state-of-the-art and EDA vendors on the logic while the variability challenges remain in the memories themselves. For that purpose REALITY has been first in deploying a holistic statistical characterization flow including SRAM analysis.
Of course must be noted that a skilled memory designer is aware of variability and sets additional margins to the device library corners to ensure safe operation and good yield. However, the amount of this extra margins can be quantified using the REALITY approach, whereas the state of the art is based on design adaptations after first silicon feedback. Imec has quantified that the amount of (as always, measured at 3sigma=99.9%) optimism when neglecting the mismatch of the memories is about 7% of the clock period. The TT point is at 93% which means we have to provide 13.5% additional safety margin to capture memory and logic variability (6.5% if we only take logic into account). Hence the different between considering or not variability impact on memories is about 50% for local random variations. In the context of total variation (including the global component), this range becomes 20%.
In WP6 KUL analyzed the impact and reported on research conducted in WP3.1 that resulted in the development of advanced degradation effect models for hot carrier and NBTI transistor reliability phenomena. Also, an efficient simulation method to emulate the impact of time-varying stress on the operation of an analog circuit was proposed. Simulation results on an example circuit indicated how DC-only reliability simulator can result in large errors on lifetime assessment of analog circuits. In WP3.2 an efficient method to include the impact of process variability in the circuit reliability analysis flow was proposed.
Experiments indicated how process variability interacts with time-dependent reliability effects resulting in time-dependent circuit yield. Usage of commercial reliability simulation tools, not including process variability, can therefore result in a large error on the lifetime estimation
During this last period of the project ARM has put a lot of effort generating the necessary Standard Cells data we needed for an interesting characterization of the ARM926. Variations in the voltage conditions, temperature as well as in the type of models have been done in order to fully cover the variability analysis. The following table shows the list of the characterizations performed.

Voltage / Temperature	Origin of Models	Type of variations	Justifications
0.9V 125°C	UoG - Fresh	Local and Global*	Référence
0.9V 125°C	Foundry	Local	Analyse Difference from Models

0.9V 25°C	UoG - Fresh	Local and Global*	Temperature Effects
1.1V 125°C	UoG - Fresh	Local and Global*	Voltage Effects
0.9V 125°C	UoG - Aged	Local	Aging Effects
0.9V -40°C	UoG - Fresh	Local and Global*	Temperature Effects
1.1V 125°C	UoG - Fresh	Local and Global*	Temperature and Voltage Effect

**Note that since UoG is focused on local variations the information on global variations are extracted from the foundry models*.

The VAM flow being Monte Carlo based one hundred libraries had to be characterized for each condition. We therefore have spent some time to automate the initialisation of the characterization flow in order to fit to the VAM data base structure. This allowed reducing the potential errors we could generate by manipulating hundreds of liberty file from different characterization conditions.
To cope with the timing constraint we have used the CPU resources coming from two different internal clusters in the company.
The memory statistical margining flow has been developed on a 45nm SRAM cell showing a large variability. A comparison between the new flow and previous methods based on normal distributions has been carried out and showed a great improvement on the accuracy of the method (see figure).
After the initial tests in the 45nm node the method was applied on 32nm node in SOI technology memories by "production" designers with support from the REALITY team.



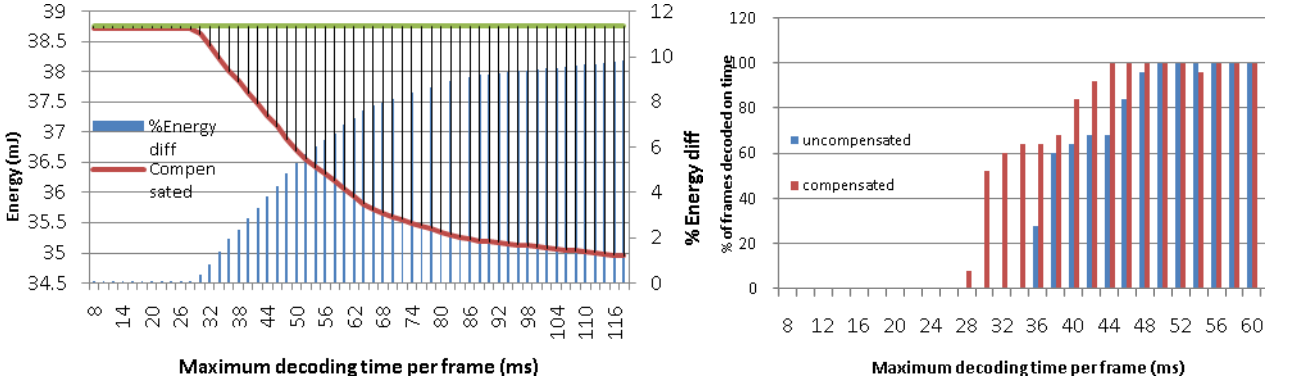
Task 6.5.2:

Evaluation and benchmarking of the system level integration of the building blocks from WP3, and WP4 as defined by the validation plan. This included evaluation of the SW heuristics and integrated HW/SW mechanisms that interact and interface to low level measuring block as defined in WP4

The bulk of the reporting period work for ST with the support of UNIBO was documented in D6.4 for the the analysis performed on two ideal corner reference system evaluation platforms for maximum frequency and power variability injected, starting from the variability ranges provided by the VAM flows.

An extensive set of benchmarking and analysis was performed on the system level xSTream platform for a relatively large number of 'virtual' chips instantiated from global and local variability clouds produced by the REALITY project to assess the performance and energy benefit of SW countermeasures developed to cope with variability.

During the reporting period, the activity of UNIBO in WP6 focused on three main activities, all carried out in collaboration with ST: i) Implementation and consolidation of the target simulation platform; ii) Porting of the MPEG2 benchmark to the target platform; iii) Validation of the policy on the target platform and benchmark. Concerning the first point, UNIBO and ST implemented a variability-aware version of the target simulation platform of the ST xstream processing engine. The variability models have been included as a simulator plug-in. Also, power and performance emulated monitors have been implemented. A thermal model has been integrated to evaluate the impact of temperature on the variability. Concerning the second point, the porting of the MPEG2 benchmark was completed and the policy developed in WP4 was applied to the main parallel kernels. Concerning the third point, extensive experimentation was performed to validate the capability of the proposed policy to compensate the effect of both global and local variability in the multicore platform.



Significant results were highlighted in D6.4 from the analysis of the large amount of data collected during the benchmarking campaign, for example the two charts above show the potential for both energy reduction and yield improvements enabled by deployment of the SW control techniques.
All partners of WP6 have also worked on analyzing the impact of the technology and flows developed by REALITY when applied to selected industrially relevant use cases. This work has been documented in D6.5 with a comparison for between REALITY-approach and previous approach regarding memory variability, variability under aging, impact of memory variability in a system, impact of performing time-varying aware reliability analysis on design, impact of system level variability and QoS under system level compensated conditions, impact of using Forward Body Biasing, impact of memory margining, and finally the impact on a typical multimedia SoC of system level compensation techniques.

Use of resources

Partner	*Planned effort (MM)*	*Actual effort (MM)*
UOG	*0*	*0*
IMEC	*0*	*0(*)*
UNIBO	*2*	*24.53(*****)*
ST	*6*	*9.5(**)*
KUL	*0*	*0.3(***)*
ARM	*5.2*	*8.5(****)*
TOTAL	*13.2*	*42.83*

(*) IMEC had a significant contribution in WP6 in 2010 but that one is free of cost to the project
(*) ST used additional 3.5MM required to accommodate lengthy platform level simulation runs (thousands of aggregated server CPU hours) that needed to be repeated for new variability results and adjusted SW policy parameters post D6.4
(***) KUL made a contribution to Deliverable D6.5: Analysis of project results impact for selected industrial scenarios. Initially there was no manpower allocated for this effort in the DoW.
(****) ARM has allocated 1.2MM from WP5 to WP6. After the initial results analysis additional corners characterizations appeared to be an interesting work to perform in order to have a relevant comparison. ARM finally characterized in the WP6.
(*****) The actual number of actual MMs effort is for UNIBO higher than initially planned because we used much more junior resources than expected that resulted in more PMs. As a consequence, there is not impact on the budget.

12.7. WP7: Project management (WP leader: IMEC)

A description of the work in this work package can be found in section 14 on project management.

Use of resources

Partner	*Planned effort (MM)*	*Actual effort (MM)*
UOG	*0.18*	*0.18*
IMEC	*2.4*	*3.35(*)*
UNIBO	*0.75*	*0.75*
ST	*0.3*	*0.3*
KUL	*0.5*	*0.5*
ARM	*0.4*	*0.4*
TOTAL	*4.53*	*5.48*

(*) Overhead in management for project coordination due to the extension in the duration of the project

12.8. WP8: Exploitation and Dissemination (WP leader: IMEC/ARM)

A description of the work in this work package can be found in deliverable 8.5 which is the second revision of the dissemination and use plan. This deliverable contains the work of all partners.

Use of resources

Use of resources*Partner*	*Planned effort (MM)*	*Actual effort (MM)*
UOG	*0*	*0(*)*
IMEC	*0.6*	*0.6*
UNIBO	*0*	*0*
ST	*0.7*	*0.7*
KUL	*1.4*	*1.4*
ARM	*0.8*	*1.8(**)*
TOTAL	*3.5*	*4.5*

(*) UoG has free of cost contributions to WP8
(**)ARM has hosted the REALITY workshop on June. It has generated 1MM additional for the complete

13. Deliverables and milestones tables

Planned Deliverables between T0+25M and T0+32M (All delivered)

Del. no.[1]	Deliverable name	WP no.	Lead beneficiary	Nature [2]	Dissemination level [3]	Delivery date from Annex I (proj month) [4]	Delivered Yes/No	Actual / Forecast delivery date
D2.3	Report on Variation-Aware Statistical Characterization Techniques	WP2	IMEC	R	PU	T0+27M	Yes	T0+27M
D2.4	Report on Variation-Aware electronic information format	WP2	IMEC	R	CO	T0+27M	Yes	T0+27M
D3.2.bis	Report on mixed-signal circuit reliability models & design of variability resilient memory IP blocks (part 2)	WP3	KUL	R	CO	T0+30M	Yes	T0+30M
D4.3	Report: Porting, optimization and tuning for the target evaluation platform of: (a) the flexible RTSM, (b) the control algorithms	WP4	Unibo	R	PP	T0+27M	Yes	T0+27M
D 6.4	System level evaluation report as specified by the validation plan	WP6	ST	R	PP	T0+30M	Yes	T0+31M

[1] Deliverable numbers in order of delivery dates: D1 – Dn
[2] Please indicate the nature of the deliverable using one of the following codes:
R = Report, **P** = Prototype, **D** = Demonstrator, **O** = Other
[3] Please indicate the dissemination level using one of the following codes:
PU = Public
PP = Restricted to other programme participants (including the Commission Services)
RE = Restricted to a group specified by the consortium (including the Commission Services)
CO = Confidential, only for members of the consortium (including the Commission Services)
[4] Month in which the deliverables will be available. Month 1 marking the start date of the project, and all delivery dates being relative to this start date.

D 6.5	Final application report containing an analysis of the impact of project results on meaningful industrial product scenarios	WP6	ST	R	CO	T0+31M	Yes	T0+31M
D7.6	Project activity report	WP7	IMEC	R	PU	T0+25M	Yes	T0+25M
D7.7	Final report	WP7	IMEC	R	PU	T0+32M	Yes	T0+32M
D7.8	Awareness and wider societal implications report	WP7	IMEC	R	PU	T0+32M	Yes	T0+32M
D8.4	Project workshop	WP8	IMEC	R	PU	T0+31M	Yes	T0+31M
D8.5	Dissemination and use plan (second issue)	WP8	ARM	R	PU	T0+32M	Yes	T0+32M
D8.6	Press release at the end of the project	WP8	IMEC	R	PU	T0+32M	Yes	T0+32M

Table 4 List of planned Deliverables for Year 3

Planned Milestones between T0+M13 and T0+24M

TABLE 2. MILESTONES							
Milestone no.	Milestone name	Work package no	Lead beneficiary	Delivery date from Annex I	Achieved Yes/No	Actual / Forecast achievement date	Comments
M6	Statistical device compact model for IMB/ST device architecture at 32nm	WP1	UOG	Month 27	Yes	M25	Project board meeting
M7	Final Dissemination and Use plan	WP8	IMEC	Month 32	Yes	M32	Project board meeting

Table 5 List of planned Milestones for Year 3

14. Project management

14.1. Consortium management tasks and achievements;

The Project Coordination and related Management tasks are a vital part of the successful execution of the REALITY project. The applied management approach is fully embedded into the daily operations of the REALITY project. This section describes the achievements and organization in the REALITY project during the first reporting period. This way of working will be continued throughout the entire project timeline. The project coordination and management aims at providing the necessary infrastructure to support the complicated task of decision making and communication between the REALITY partners. The organizational structure of the REALITY project management is presented in the figure below:

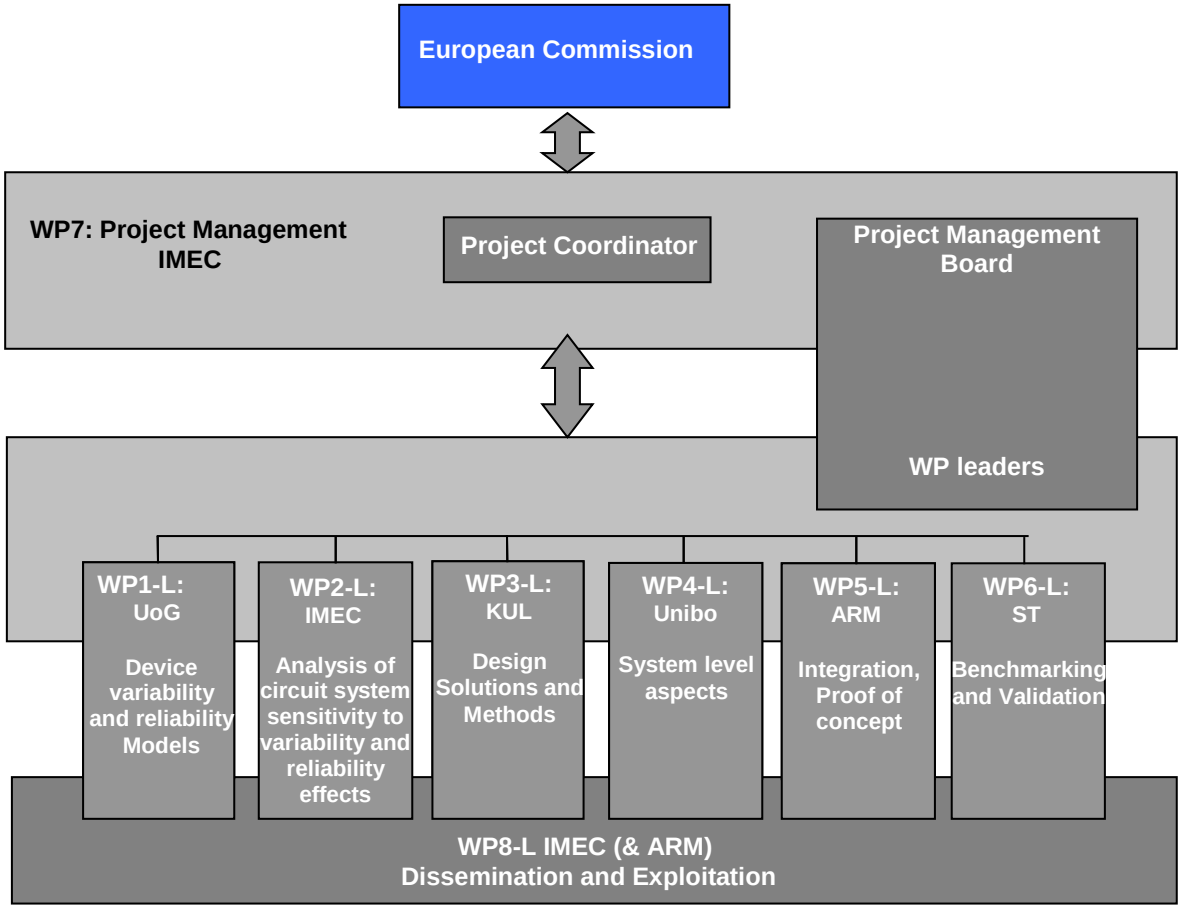


Figure 8 REALITY project team and coordination

IMEC acts as the project coordination of the **REALITY** project. IMEC oversees the day-to-day management and acts as the liaison between the project and the EC.

A Snapshot of the main management tasks :

- Keeping the global overview of the project.
- Communication list compilation and keeping it up-to-date.
- The technical management of the project, oversight and steering the scientific and technological development in the project.
- Keeping the actiontracker and follow-up the timely closure of actions.
- Keeping and follow-up of the Decisions list.
- Organizing the Risk Management.
- Monitoring deliverables and milestones, organizing the proper review of deliverables.

- Measuring the actual progress against technical objectives.
- Recommendations about major changes in the planned work.
- Chair the Project Management Board.
- Organization of the Project Management Board meetings and Project Technical meetings, including definition of the Agenda and key topics.
- Driving the dissemination and use (see deliverable report D8.3) activities
- Collection and submission of cost statements, overview of budget situation
- Promotional flyers and posters
- Organizing Contract negotiation for consortium agreement
- Update of the Description of Work, version v2.0

The Project Management Board is comprised of one member from each partner (WP leaders) and is chaired by the project coordinator. The input from the respective organization of each member regarding coordination, planning, monitoring and reporting will be disseminated in the board. Finally, the board is responsible for all the strategic decisions regarding the direction of the project. These responsibilities include:

- Strategic planning
- Managing assets complementary to innovation: budget, addition of new partner
- Contract negotiation for consortium agreement
- Set up of Non Disclosure Agreement (NDA)
- Contracts and licensing agreements resulting from the valorization initiatives
- Protection of intellectual property
- Technology transfer

For practical reasons, the project management board meetings and project team meetings – except the technical workshops – have been combined in the first reporting period.

The Work package leaders are responsible for the coordination and execution of the tasks and the deliverables within their respective work package. They have reported all technical results regarding the project (deliverables, publications, etc.) to the project coordinator.

14.2. Problems which have occurred and how they were solved or envisaged solutions

14.2.1. REALITY Top Risks to date:

There is a continuous evolution in problems occurring. Some major risks which were identified at the project kickoff have materialized and proper actions were made to ensure the impact was mitigated. Some other risks which were identified did not come true or the priority (severity or probability) was much lower than expected, and finally a few new risks popped up during the course of the first reporting period.

The objectives of this reporting period are relevant and thanks to the infrastructure and bonds setup among partners built in the previous two periods the execution of these have been relatively straight forward. The increased interest for exploitation of the results by the industrial partners proves that the objectives of this project have been relevant. The objectives for the reporting period have been achieved. The variability characterization platform put in place during period 2 for 32nm process and multi-core system applications have enabled the partners to explore further its capabilities thus offering the opportunity to prove the tremendous impact on the semiconductor industry of our variability aware design methodology and this with the minimum of effort and resources.

No further top risks have been identified and/or deveooped during the last reporting period.

14.2.2. Changes:

Consolidated Changes in the Description of work:

The description of work was updated with version 6, on April 28th 2010 reflecting the changes in the consortium and updates and clarification in the original D.O.W.; Table 2 below shows the overview of the justifications of the updates.

Please note: No manpower was changed; the total budget of the project remains the same. The project objectives remain the same.

Partner	WP	Changes	Explanation if needed
KUL	WP3	New deliverable D3.2.bis. This an update of deliverable D3.2. Due date M30	late delivering of technology data that has forced one of our partners (KUL) them to enter the third reporting period to re-submit deliverable D3.2 (rejected after the review meeting) in the form of a new deliverable D.3.2.bis
	WP3	T3.2 moves ending date from M24 to M30	Accommodates to new delivering date
ST	WP6	D6.4 moves date from M27 to M30	D6.4 – System Evaluation Report (has ending date dependency with D3.2.2) new due date moves from M27 to M30
	WP6	D6.5 moves date from M30 to M31	D6.5 – Final Evaluation Report (has starting date dependency with D6.4) new due date moves from M30 to M31
	WP6	T6.5.1 & T6.5.2 moves ending date from M30 to M31	Accommodates to new delivering date
IMEC	WP7	D7.7 moves date from M30 to M32	D7.7 - Final activity report (has starting date dependency with D6.5) new due date moves from M30 to M32
	WP7	D7.8 moves date from M30 to M32	D7.8 – Awareness societal implications (has has starting date dependency with D6.5) new date moves from M30 to M32
	WP7	WP7 moves date from M30 to M32	Accommodates to new delivering date
	WP8	D8.4 moves date from M29 to M31	D8.4 - Project Workshop (has starting date dependency with D6.4) new date moves from M29 to M31
	WP8	D8.5 moves date from M30 to M32	D8.5 – 2nd issue dissemination and use plan (has has starting date dependency with D6.5) new date moves from M30 to M32
	WP8	D8.6 moves date from M30 to M32	D8.6 - Press release at end of workshop (has has ending date dependency with D7.8) new date moves from M30 to M32
	WP8	T8.2 moves date from M30 to M32	Accommodates to new delivering date
	WP7	Extend project duration from 30M to 32M	The ending date is extended by two months to accommodate the ending date of

Table 6: Update of the DoW

Changes in the project plan

As identified in section 15.2.2, some risks materialized in period 2. Therefore corrective actions were planned, resulting in a change of the original work plan. All changes in the original work plan have been identified in table 6. In addition the ending date of the project had to be postponed by two months, hence from 30 to 32 months to accommodate for delays caused by the later delivering of the technology data (see period report Y2 D7.6).

14.3. List of project meetings, dates and venues in year 1 :

The table 7 shows an overview of the meetings held in the third reporting period (project month M25 until M32. One room project meetings with having all consortium partners to join (work package leaders and scientific key members), are typically held each 6 months or more frequently when necessary. For efficiency reasons it was decided by the consortium partners to combine as much as possible the milestone meeting with the project management board meeting and the technical review. When necessary, separate and dedicated technical meetings were organized with specific topics. Conference calls were planned monthly during the first year of the project.

Meeting name	Meeting Purpose	Meeting Type	WP's	Date	Venue
2st review meeting with EC PO and reviewers	Official review meeting with EC Evaluate if project follows proposed DoW Decide if payments proceed	REVIEW meeting with PO and reviewers	WP1 until WP8	March 26, 2010	IMEC offices, Leuven Belgium
Monthly conference call	Handle administrative issues Keep track of deliverables and delivery dates Follow up of the action tracker Clarify technical contributions from partners	Administrative and TECHNICAL	WP1 until WP8	Monthly	Conference call
Partner Meeting 5 (Pm5)	Measure and ensure a constant level of information sharing about the progress in all the Work Packages. Get a common understanding of the technical status and priorities Align the work packages, milestones, timelines and (administrative) reporting Assessment of all the risks, including definition of alternative actions Escalation path if necessary, Update of the DoW Clarify the expectations of all partners Review and approval of the deliverable report Team building Prepare upcoming review meeting	MILESTONE M3 PROJECT MANAGEMENT BOARD + TECHNICAL	WP1 until WP8	March 25 2010	IMEC offices, Leuven Belgium

Table 7: Overview of project meetings

14.4. Project planning and status :

The table 8 shows an overview of the committed deliverables in the first reporting period which were submitted to the EC. All of the scientific and dissemination deliverables were provided on time as planned. Some deliverables were postponed. This was also communicated towards the EC.

Del. no.[5]	Deliverable name	WP no.	Lead	Nature [6]	Dissemination	Delivery date

[5] Deliverable numbers in order of delivery dates: D1 – Dn
[6] Please indicate the nature of the deliverable using one of the following codes:
R = Report, **P** = Prototype, **D** = Demonstrator, **O** = Other

			beneficiary		level [7]	
D2.3	Report on Variation-Aware Statistical Characterization Techniques	WP2	IMEC	R	PU	T0+27M
D2.4	Report on Variation-Aware electronic information format	WP2	IMEC	R	CO	T0+27M
D3.2.bis	Report on mixed-signal circuit reliability models & design of variability resilient memory IP blocks (part 2)	WP3	KUL	R	CO	T0+30M
D4.3	Report: Porting, optimization and tuning for the target evaluation platform of: (a) the flexible RTSM, (b) the control algorithms	WP4	Unibo	R	PP	T0+27M
D 6.4	System level evaluation report as specified by the validation plan	WP6	ST	R	PP	T0+31M
D 6.5	Final application report containing an analysis of the impact of project results on meaningful industrial product scenarios	WP6	ST	R	CO	T0+31M
D7.6	Project activity report	WP7	IMEC	R	PU	T0+25M
D7.7	Final report	WP7	IMEC	R	PU	T0+32M
D7.8	Awareness and wider societal implications report	WP7	IMEC	R	PU	T0+32M
D8.4	Project workshop	WP8	IMEC	R	PU	T0+31M
D8.5	Dissemination and use plan (second issue)	WP8	ARM	R	PU	T0+32M
D8.6	Press release at the end of the project	WP8	IMEC	R	PU	T0+32M

Table 8 List of deliverables submitted to the EC

14.5. Impact of deviations materialized from the planned milestones and deliverables

[7] Please indicate the dissemination level using one of the following codes:
PU = Public
PP = Restricted to other programme participants (including the Commission Services)
RE = Restricted to a group specified by the consortium (including the Commission Services)
CO = Confidential, only for members of the consortium (including the Commission Services)

No major deviation exists in the planning of deliverables, nor the execution of the REALITY that may affect the final outcome of the project compared to the original schedule. Whenever necessary, practical constraints have been taken into account in the precise definition of meetings and in providing deliverables. However, the duration of the project had to be extended by two months, the ending date of the project had to be postponed from 30 to 32 months to accommodate for delays caused by the later delivering of the technology data (see period report Y2 D7.6).

14.6. Development of the Project website :

The www.fp7-reality.eu website is online since april 2008 and contains a Public area. It is the official homepage of the project and that serves as a public repository for all project related information. Consortium restricted information and project related documents (action trackers, deliverables, meeting slides…) are stored on a dedicated wiki page (http://www-micrel.deis.unibo.it/~reality/wiki/index.php/Main_Page).

The public web site gives interested users access to a number of public pages providing a description of the project objectives, news, announcement of upcoming events, links to exhibitions where the REALITY project will be represented, contact information and reports or specifications.

Further details on the website and its statistical monitoring information can be found in **deliverable report D8.5**

14.7. Use of foreground and dissemination activities during this period :

Within the REALITY consortium all partners contribute to a large extend equally to the dissemination of the project results. Extensive details on the dissemination approach and achievements can be found in deliverable report D8.5 submitted to the EC in October 2010.

IPR, Access rights and licensing have been made explicit and described in an elaborate way in the Consortium Agreement which was signed by all consortium partners.

14.8. Coordination activities comment – key message :

The key message regarding the REALITY coordination activities can be summarized as follows :

- **Deliverables have been achieved on time as planned.**
- **Numerous Scientific Publications have been achieved.**
- **Information has been shared within the consortium, but individual partners have also become active in a bilateral context.**
- **True collaboration exists within the consortium, as well as outside the** REALITY **context.**
- **The** REALITY **research topic has and will remain to have industrial relevance.**
- **Furthermore, the** REALITY **research topic is at the core of the industrial partners activity.**

15. Explanation of the use of the resources

15.1. ST Microelectronics

Table : Personnel, subcontracting and other major cost items for Beneficiary "ST" for period 3			
STM	**Item description**	**Amount**	**Explanations**
	Personnel costs RTD MNG	€155,681 €1,834	1 Manager, 6 R&D eng, 2,728.85 hours total 0.12MM Management 18.33MM engineers List of individual involved with Management:

			• Giuseppe Desoli R&D Director & Fellow People involved with RTD • Giuseppe Desoli R&D director, Fellow • Davide Pandini, Senior engineer • Francesco Papariello, SW engineer • Andrea Carlo Ornstein, SW engineer • Tommaso Majo, design engineer • Cristiano Forzan, design engineer • Guido Angelo Repetto, design engineer
	Audit certificate	€6,160 D	
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		€163,675	

15.2. IMEC

Table : Personnel, subcontracting and other major cost items for Beneficiary "IMEC" for period 3			
IMEC	**Item description**	**Amount**	**Explanations**
	Personnel costs	€46,979.83	RTD Personel costs of 2.10MM (E1 type) engineers and 0.9MM (E3 type) senior engineers). Management cost of 3.3MM. . In detail the following persons in RTD: • Zuber Paul (researcher) • Miranda Corbalan Miguel (Principal Scientist) In detail the following persons in Management: • Miranda Corbalan Miguel Principal Scientist (engineer)
	Consumables	€0	
	Travels	€6,685.04	Travel cost of: • Invited Talk Miguel Miranda at DATE conf in Dresden Germany on REALITY • Organization of second and third (final) REALITY review meeting at Imec • Invited Talk Miguel Miranda at Technical Univ. Madrid, Spain on REALITY • Presentation conference paper of Paul Zuber at DAC conf. in Annaheim, USA • Participation on REALITY workshop in Cambridge UK
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		€53,664.87	

Adjustment to period 2

Table : Personnel, and other major cost items for Beneficiary "IMEC" for period 2 –Adjustment			
IMEC	**Item description**	**Amount**	**Explanations**

	Adjustment on overhead costs for RTD	€-33,400.0	The overhead costs computed in period 2 where based on rates of 2008. This adjustment reflects the computation of the 2009 overhead costs using the 2009 overhead rates available in 2010
	Adjustment on overhead costs for Management	€-5,877.25	The overhead costs computed in period 1 where based on rates of 2008. This adjustment reflects the computation of the 2009 overhead costs using the 2009 overhead rates available in 2010
TOTAL INDIRECT COSTS AS CLAIMED ON FORM C		€-39,277.25	

15.3. University of Glasgow

Table : Personnel, subcontracting and other major cost items for Beneficiary "UoG" for period 3			
UoG	**Item description**	**Amount**	**Explanations**
	Personnel costs	€63,465.05	16.3MM in RTD: • Andrew Brown (Research Associate) • Antonio Martinez (Research Associate) 0.17MM in Management: • Asen Asenov (Professor) • Scott Roy (Reader)
	Other	€15,046.30	Travel to project meetings, and to conferences for dissemination of results. Computer workstation for devlopment of simulation software. Computer consumables.
	Major Cost Item	€28,674.18	Additional nodes to upgrade our compute cluster in order to run the simulations required by the project
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		€107,185.53	

15.4. Katholieke Universiteit Leuven

TABLE 3.1 PERSONNEL, SUBCONTRACTING AND OTHER MAJOR DIRECT COST ITEMS FOR BENEFICIARY KUL (KATHOLIEKE UNIVERSITEIT LEUVEN) FOR THE 3ND YEAR			
Work Package	**Item description**	**Amount**	**Explanations**
3,6,7,8	Personnel	€ 68,587.00	12,65 person months of scientific

			researchers + 0.35 person months of a professor. In detail the following persons in RTD: • Ben Geeraerts (senior researcher) • Stefan Cosemans (senior researcher) • Yi Ke (researcher) • Athanasios Stefanou (researcher) • Wim Dehaene (professor) • Georges Gielen (professor)*
3,6,7,8	Other	€ 149.00	Workshop travel costs + small pcb components
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		€ 68,736.00	

15.5. University of Bologna

Table : Personnel, subcontracting and other major cost items for Beneficiary "UNIBO" for period 3			
UNIBO	**Item description**	**Amount**	**Explanations**
WP4/5/6/7	Personnel costs	85.128,80	Three grants for research are activated with three young graduated collaborators in order to carry out the activities foreseen for UNIBO in the REALITY project, corresponding to about 17 person/month. Dr Andrea Acquaviva, Dr Davide Brunelli and Dr Pullini Antonio are involved in this project through a research collaboration contract to cooperate on all project related activities and in particular on WP6, with a total of about to 8,5 p/m. Dr Carlo Caione, Dr Bojan Milosevic, Dr Kakoee Mohammad Reza and Dr Andrea Bartolini are involved in the project with occasional collaboration contracts for a total of about 4 P/M. Prof. Luca Benini and Prof. Michela Milano are involved in the activities foreseen within WP 5, 6 and 7 for a total of about 2,5 person/months. Due to the unavailability of a senior researcher, the number of PM has been higher and at low cost than foreseen because the activities have been performed by junior researchers.
WP4	Subcontract	28.153,14	According to the Annex I of the Grant Agreement a subcontract is activated with the University of Cagliari. The amount of 23.809,00 corresponds to the second tranche of payment for the above mentioned activity. The amount of 4.344,14 corresponds to the cost for the Certificate of Financial Statement.
WP5/6/7	Major cost item 'Travel & Subsistence'	11.612,14	Reimbursements of travel and subsistence costs for the participation to the following events: • Project and review meetings; • Meetings with partners

			• Participation to DATE conference 2010, Eurosys 2010, GLSVLSI 2010, SIES 2010, ISCC 2010, Computing Frontier Conference and workshops in Grenoble and Cambridge.
WP4/8/6	Major cost item 'Other Costs'	4.578,01	These costs are incurred: • For the organisation of a seminar in Bologna and for the remuneration of the speaker invited • Dissemination material
WP6	Consumables	1.501,73	The consumables purchased are: lab consumables and the Mentor graphics software for high-level synthesis which had the purpose of generating benchmarks of synthesizable arithmetic and control circuits for the purpose of testing the ABB synthesis approach developed by UNIBO on a set of internal benchmarks.
WP4/6	Equipment	131,29	The cost incurred refers to the depreciation of the PC QUAD660.
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		131.105,10	

Adjustment to period 1

Table : Personnel, subcontracting and other major cost items for Beneficiary "UNIBO" for period 1 - Adjustment			
UNIBO	**Item description**	**Amount**	**Explanations**
WP3, WP4	Travel and Sub.	752,34	Adjustment refers to travel cost incurred during period 1 but paid after the submission of the financial reports for period 1 and 2.
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		752,34	

Adjustment to period 2

Table : Personnel, subcontracting and other major cost items for Beneficiary "UNIBO" for period 2 - Adjustment			
UNIBO	**Item description**	**Amount**	**Explanations**
WP3	Personnel costs	-929,57	Adjustment due to the correction of some costs related to the contract of Igor Loi and to the costs of Prof Luca Benini.
WP4	Subcontract	350,00	This amount is related to the catering costs which were originally considered as Other Costs.
WP3, WP4	Travel and Sub.	271,96	The adjustment refers to travel cost incurred during period 2 but paid after the submission of the financial report for period 2 and to the correction of the airport taxes amount of some travels in period 2.
WP4/6	Equipment	-17,92	This adjustment is due to the correction of calculation the depreciation costs calculation.
WP4	Consumables	9,00	This amount corresponds to the correction of the

			consumables costs in P2.
WP8	Other direct Costs	-374,71	The adjustment refers to the correction of purchase costs of dissemination material in period 2 and to the swopping of the catering costs to the category Subcontract.
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		-691,24	

15.6. ARM

Table : Personnel, subcontracting and other major cost items for Beneficiary "ARM" for period 3			
ARM	**Item description**	**Amount**	**Explanations**
WP2, 6, 7 and 8	Personnel Cost	€68,899	1 manager, 1 engineer working part time on the project: 10.6pm spent during the period. The following employees were involved in the R&D activities: • Yves Laplanche (R&D manager) • Selma Laabidi (R&D engineer)
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		€68,899	

Adjustment to period 2

Table : Personnel, subcontracting and other major cost items for Beneficiary "ARM" for period 2 - Adjustment			
ARM	**Item description**	**Amount**	**Explanations**
WP1, 2, 6, 6, 7 and 8	Personnel costs	€2,811	The personnel costs were impacted by the normalisation of the working hours, and the adjustment made to the indirect cost rate. The actual 2009 indirect cost rate is now used for this period, and it is superior to the indirect cost rate previously used in the calculation. Overall, these changes caused a slight increase of the personnel costs for period 2.
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		€2,811	

Adjustment to period 1

Table : Personnel, subcontracting and other major cost items for Beneficiary "ARM" for period 1 - Adjustment			
ARM	**Item description**	**Amount**	**Explanations**
WP1, 2, 6, 6,	Personnel costs	€-56,716	The personnel costs claimed for period 1 dropped because normalised hours are now used instead of actual working hours.
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		€-56,716	

16. Financial statements – Form C and Summary financial report

The form C has been uploaded to the NEF online webtool by all partners.

17. Certificates

See pages: 46-65

Independent Report of Factual Findings on costs claimed under a Grant Agreement financed under the Seventh Research Framework Programme (FP7)

Prof. Luca Benini (Scientific Responsible)
Università di Bologna
Viale Risorgimento,2
18/11/2010

In accordance with our contract dated 01/10/2010 with Università di Bologna "the Beneficiary" and the terms of reference attached thereto (appended to this Report), we provide our Independent Report of Factual Findings ("the Report"), as specified below.

Objective

We **Studio Legale e Commerciale Associato Cippitani, Di Gioacchino Iozzolino & Chiappalupi**, established in **Via Margutta 1a, 00187 Roma, Italy,** represented for signature of this audit certificate by **Dr. Roberto Di Gioacchino**, acting as "Revisore contabile" (according to the *Registro dei Revisori, Ministero della Giustizia della Repubblica Italiana*, n. 104277), have performed agreed upon procedures regarding the cost declared in the Financial Statement of University of Bologna, hereinafter referred to as the Beneficiary, to which this Report is attached, and which is to be presented to the Commission of the European Communities under grant agreement "Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies"- REALITY-G. A. Number 216537 (the 'Grant Agreement'). for the following periods:

P1-1/January/2008 to 31/December/2008.
P2-1/January/2009 to 31/December/2009.
P3-1/January/2010 to 31/August/2010.

This engagement involved performing certain specified procedures, the results of which the European Commission uses to draw conclusions as to the eligibility of the costs claimed.

Scope of Work

Our engagement was carried out in accordance with:
- the terms of reference appended to this Report and:
- International Standard on Related Services ('ISRS') 4400 *Engagements to perform Agreed-upon Procedures regarding Financial Information* as promulgated by the International Federation of Accountants ('IFAC);
- the *Code of Ethics for Professional Accountants* issued by the IFAC. Although ISRS 4400 provides that independence is not a requirement for agreed-upon procedures engagements, the European Commission requires that the Auditor also complies with the independence requirements of the *Code of Ethics for Professional Accountants;*

As requested, we have only performed the procedures set out in the terms of reference for this engagement and we have reported our factual findings on those procedures in the table appended to this Report.
The scope of these agreed upon procedures has been determined solely by the European Commission and the procedures were performed solely to assist the European Commission in evaluating whether the costs claimed by the Beneficiary in the accompanying Financial Statement has been claimed in accordance with the Grant Agreement. The Auditor is not responsible for the suitability and appropriateness of these procedures.
Because the procedures performed by us did not constitute either an audit or a review made in accordance with International Standards on Auditing or International Standards on Review Engagements, we do not express any assurance on the Financial Statement.
Had we performed additional procedures or had we performed an audit or review of the Financial Statement of the Beneficiary in accordance with International Standards on Auditing, other matters might have come to our attention that would have been reported to you.

Comm. Roma n. 7290 - Reg. rev. cont. n. 104277 - Albo dott.
Dott. Roberto Di Gioacchino

Sources of Information

The Report sets out information provided to us by the management of the Beneficiary in response to specific questions or as obtained and extracted from the Beneficiary's information and accounting systems.
The subject of our engagement is:

- the *interim* Financial Statements in which the beneficiary declared that the total amount of eligible cost is equal to euro 175.837 in connection with the Grant Agreement for the period covering *from 1/01/2008 to 31/12/2008.*

- the *adjustment interim* Financial Statements in which the beneficiary declared that the total amount of eligible cost is equal to euro 7.439 in connection with the Grant Agreement for the period covering *from 1/01/2008 to 31/12/2008.*

- the *interim* Financial Statement in which the beneficiary declared that the total amount of eligible cost is equal to euro 163.711 in connection with the Grant Agreement for the period covering *from 1/01/2009 to 31/12/2009.*

- the *adjustment final* Financial Statement in which the beneficiary declared that the total amount of eligible cost is equal to minus euro 113 (+1203-1316= -113) in connection with the Grant Agreement for the period covering *from 1/01/2009 to 31/12/2009 (the amount of + 1203 represents an adjustment to period 1/01/2008-31/12/2008; the amount of -1316 represents an adjustment to period 1/01/2009-31/12/2009) .*

- the *final* Financial Statement in which the beneficiary declared that the total amount of eligible cost is equal to euro 192.876 in connection with the Grant Agreement for the period covering *from 1/01/2010 to 31/08/2010.*

Factual Findings

The above mentioned Financial Statement per Activity was examined and all procedures specified in the appended table for our engagement were carried out. On the basis of the results of these procedures, we found:
All documentation and accounting information to enable us to carry out these procedures has been provided to us by the Beneficiary. Except as indicated below, no exceptions were noted.

Exceptions

The following exceptions were noticed:

For the period 1/01/2010-31/08/2010 the Beneficiary provides the Auditor only with the annual personnel costs relating to the year 2009; the Auditor recomputed the hourly rate by dividing the personnel costs relating to the year 2009 by the average number of productive hours, which was then compared to the hourly rate charged by the Beneficiary.

For the employee with the role of "Full Professor" the auditor obtained an annual full time record to show the actual productive time. For this employee, the Auditor has ascertained that the number of hours registered for year 2009 is equal to 1409 hours. Such number of hours is lower than the average number of 1512 used to calculate the hourly rate. For the same employee, the Auditor has ascertained that the number of hours registered for the period 1/01/2010-31/08/2010 is equal to 948 hours. Such number of hours is lower than the average number of hours used to calculate the hourly rate proportioned to the period (1512/12 X 8 = 1008).
For the employee with the role of "Associated Professor" the auditor obtained an annual full time record to show the actual productive time. For this employee, the Auditor has ascertained that the number of hours registered for year 2008 is equal to 976 hours. Such number of hours is lower than the average number of

hours registered for year 2009 is equal to 553 hours. Such number of hours is lower than the average number of 1512 used to calculate the hourly rate. For this employee, the Auditor has ascertained that the number of hours registered for the period 1/01/2010-31/08/2010 is equal to 676 hours. Such number of hours is lower than the average number of hours used to calculate the hourly rate proportioned to the period (1512/12 X 8 = 1008).

The Auditor has ascertained that the number of hours registered for the Researcher assistant Francesco Paterna for the period 1/04/2008-31/03/2009 is equal to 1503 hours. Such number of hours is lower than the average number of 1512 used to calculate the hourly rate.

The Auditor has ascertained that the number of hours registered for the Researcher assistant Pullini Antonio for the period 1/02/2009- 31/01/2010 is equal to 1506 hours. Such number of hours is lower than the average number of 1512 used to calculate the hourly rate.

For the employees with the role of "Full Professor" and "Associated Professors", with regard to the hours dedicated to the other activities not directly connected to the project, the Auditor obtained the full time record only on annual basis to show the total actual productive time.

In the case of the subcontract indicated with the number 1, the beneficiary declared that there are no tendering documents because the University of Cagliari is the only service supplier on the market, because of the particular technical / scientific object of the service.

Use of this Report

This Report is solely for the purpose set forth in the above objective.

This Report is prepared solely for the confidential use of the Beneficiary and the European Commission and solely for the purpose of submission to the European Commission in connection with the requirements as set out in Article II.4.4 of the Grant Agreement. This Report may not be relied upon by the Beneficiary or by the European Commission for any other purpose, nor may it be distributed to any other parties. The European Commission may only disclose this Report to others who have regulatory rights of access to it, in particular the European Anti Fraud Office and the European Court of Auditors.

This Report relates only to the Financial Statement specified above and does not extend to any other financial statements of the Beneficiary.

No conflict of interest exists between the Auditor and the Beneficiary in establishing this Report. The fee paid to the Auditor for providing the Report was € 4.344,14 vat included equal to **€ 0,00.**

We look forward to discussing our Report with you and would be pleased to provide any further information or assistance which may be required.

Roma, 18 November 2010

Studio Legale e Commerciale Associato
R. Cippitani, R. Di Gioacchino I.Iozzolino & Chiappalupi
Roberto Di Gioacchino,
(Legal Representative and Revisore contabile)

Comm. Roma n. 7290 - Reg. rev. cont. n. 104271 - Albo dott. Dott. Roberto Di Gioacchino

The Auditor designs and carries out his work in accordance with the objective and scope of this engagement and the procedures to be performed as specified below. When performing these procedures the Auditor may apply techniques such as inquiry and analysis, (re)computation, comparison, other clerical accuracy checks, observation, inspection of records and documents, inspection of assets and obtaining confirmations or any others deemed necessary in carrying out these procedures. Please consider that the procedure carried out by the Auditor concerning any Cost Category reported in the table below, has been carried out according to analythical method: no sample method has been used. The European Commission reserves the right to issue guidance together with example definitions and findings to guide the Auditor in the nature and presentation of the facts to be ascertained. The European Commission reserves the right to vary the procedures by written notification to the Beneficiary. The procedures to be performed are listed as follows:

Personnel costs

Procedures:

1. Recalculate hourly personnel and overhead rates for personnel (full coverage if less than 20 employees, otherwise a sample of minimum 20, or 20% of employees, whichever is the greater),indicate the number of productive hours used and hourly rates.
Where sampling is used, selection should be random with a view to producing a representative sample.
Productive hours' represent the (average) number of hours made available by the employee in a year after the deduction of holiday, sick leave and other entitlements. This calculation should be provided by the Beneficiary.
[if average costs are used, a separate independent report is required on the methodology]

Full coverage procedures performed:

Intra muros consultant

For all employees and intra muros consultants -the total number is equal to 12- the Auditor has obtained the personnel costs (salary and employer's costs) from the payroll system together with the productive hours from the time records of each employee.
For all the intra muros consultants - the number of these consultants is equal to 6 - the Auditor recomputed the hourly rate by dividing the actual personnel costs by the actual productive hours, which was then compared to the hourly rate charged by the Beneficiary.
No exceptions were noted.

Professors and researchers assistants

For the employees with the role of "full professor", "associated professor "and "researcher" , "PhD student", "research assistant" the average number of productive hours was 1512. The number of employees with the role of "Full professor" is equal to 1. The number of employees with the role of "Associated professor" is equal to 1. The number of employees with the role of "researcher assistant" ("assegnista di ricerca") is equal to 4.

For these employees -the number of these employees is equal to 6 - the Auditor recomputed the hourly rate by dividing the actual personnel costs by the average number of productive hours, which was then compared to the hourly rate charged by the Beneficiary.

The following exceptions were noticed:

For the period 1/01/2010-31/08/2010 the Beneficiary provides the Auditor only with the annual personnel costs relating to the year 2009; the Auditor recomputed the hourly rate by dividing the personnel costs relating to the year 2009 by the average number of productive hours, which was then compared to the hourly rate charged by the Beneficiary.

For the employee with the role of "Full Professor" the auditor obtained an annual full time record to show the actual productive time. For this employee, the Auditor has ascertained that the number of hours registered for year 2009 is equal to 1409 hours. Such number of hours is lower than the average number of 1512 used to calculate the hourly rate. For the same employee, the Auditor has ascertained that the number of hours registered for the period 1/01/2010-31/08/2010 is equal to 948 hours. Such number of hours is lower than the average number of hours used to calculate the hourly rate proportioned to the period (1512/12 X 8 = 1008).
For the employee with the role of "Associated Professor" the auditor obtained an annual full time record to show the actual productive time. For this employee, the Auditor has ascertained that the number of hours registered for year 2008 is equal to 976 hours. Such number of hours is lower than the average number of 1512 used to calculate the hourly rate. For this employee, the Auditor has ascertained that the number of hours registered for year 2009 is equal to 553 hours. Such number of hours is lower than the average number of 1512 used to calculate the hourly rate. For this employee, the Auditor has ascertained that the number of hours registered for the period 1/01/2010-31/08/2010 is equal to 676 hours. Such number of hours is lower than the average number of hours used to calculate the hourly rate proportioned to the period (1512/12 X 8 = 1008).
The Auditor has ascertained that the number of hours registered for the Researcher assistant Francesco Paterna for the period 1/04/2008-31/03/2009 is equal to 1503 hours. Such number of hours is lower than the average number of 1512 used to calculate the hourly rate.
The Auditor has ascertained that the number of hours registered for the Researcher assistant Pullini Antonio for the period 1/02/2009- 31/01/2010 is equal to 1506 hours. Such number of hours is lower than the average number of 1512 used to calculate the hourly rate.

Procedures:
2. For the same selection examine and describe time recording of employees (paper/ computer, daily/weekly/monthly, signed, authorised).

Full coverage procedures performed:
Employees and intra muros consultant record their time on the project on a daily basis using a computer based system. The time-records were authorized by the Scientific Responsible of the Project or other superior.
An exception was noticed : for the employees with the role of "Full Professor" and "Associated Professors", with regard to the hours dedicated to the other activities not directly connected to the project, the Auditor obtained the full time record only on annual basis to show the total actual productive time.

Procedures:
3. Employment status and employment conditions of personnel. The Auditor should obtain the employment contracts of the employees selected and compare with the standard employment contract used by the Beneficiary. Differences which are not foreseen by the Grant Agreement should be noted as exceptions.

Full coverage procedures performed:

All the Employees have been checked by the Auditor. For the employees , the Auditor inspected their employment contracts and found that they were:

-Directly hired by the Beneficiary in accordance with its national legislation,
-Under the sole technical supervision and responsibility of the latter,
-Remunerated in accordance with the normal practices of the Beneficiary.

Procedures:
4. Use of average personnel costs

Full coverage procedures performed:
Not Applicable

Subcontracting

Procedures:
5. Obtain a written description from the Beneficiary regarding 3rd party resources used and compare with Annex 1 to the Grant Agreement

Full coverage procedures performed:
The Auditor compared the description of the 3rd party resources provided by the Beneficiary to the specifications in Annex 1 to the Grant Agreement, and found them to be the same specification in **Annex** 1 to the Grant Agreement, and found them to be the same.

The beneficiary stipulated the follows subcontracts:

1) **Università degli Studi di Cagliari**

This University implemented a task migration support for the xstream multiprocessor simulator made available by ST-IT and used a target platform for the reality project to benchmark and validate system level countermeasures. This Subcontract is mentioned in Annex 1. The total cost claimed for this service is Euro 47.619 (VAT is not included).

2) **CAMST SOC. COOP. A R.L**

This Company provides the catering service. The cost claimed for this minor service is Euro 350 (vat is not included) .This subcontract is not mentioned in Annex I.

Procedures:
6. Inspect documents and obtain confirmations that subcontracts are awarded according to a procedure including an analysis of best value for money (best price-quality ratio), transparency and equal treatment. Full coverage if less than 20 items, otherwise a sample of minimum 20, or 20% of the items, whichever is the greater.

Full coverage procedures performed:
In relation to the above mentioned subcontracts, the Auditor has not obtained tendering documents.

In the case of the above mentioned subcontract indicated with the number 1, the beneficiary declared that there are not tendering documents because the University of Cagliari is the only service supplier on the market, because of the particular technical / scientific object of the service.

Other Direct Costs

Procedures:
7. Allocation of equipment subject to depreciation is correctly identified and allocated to the project. Full coverage if less than 20 items, otherwise a sample of minimum 20, or 20% of the items, whichever is the greater.

Full coverage procedures performed:

The Auditor traced the equipment charged to the project to the accounting records and the underlying invoices. The Beneficiary has documented the link with the project on the invoice and purchase documentation, and, where relevant, the project accounting. The asset value was agreed to the invoice and no VAT or other identifiable indirect taxes were charged. The depreciation method used to charge the equipment to the project was compared to the Beneficiary's normal accounting policy and found to be the same.

Procedures:
8. Travel costs correctly identified and allocated to the project (and in line with Beneficiary's normal policy for non-EC work regarding first-class travel, etc.) Full coverage if less than 20 items, otherwise a sample of minimum 20, or 20% of the items, whichever is the greater. The Beneficiary should provide written evidence of its normal policy for travel costs (e.g. use of first class tickets) to enable the Auditor to compare the travel charged with this policy.

Full coverage procedures performed:
The Auditor inspected all Travels documents and found that the Beneficiary has allocated travel costs to the project by marking of invoices and purchase orders with the project reference, resulting in traceable allocation in the project accounts. The costs charged were compared to the invoices and found to be the same. No VAT or other identifiable indirect taxes were charged. The Beneficiary did not use first class travel.

Procedures:
9. Consumables correctly identified and allocated to the project. Full coverage if less than 20 items, otherwise a sample of minimum 20, or 20% of the items, whichever is the greater.

Full coverage procedures performed:
The Auditor inspected all the Consumable invoices and found that the Beneficiary has allocated consumable costs to the project by marking of invoices and purchase orders with the project reference, resulting in traceable allocation in the project accounts. The costs charged were compared to the invoices and found to be the same. No VAT or other identifiable indirect taxes were charged.

Indirect Costs

Procedures:
10. Obtain and review a detailed breakdown of Indirect costs (reconciled to the accounting records) and confirm that the following costs are not present:
a) identifiable indirect taxes including value added tax,
b) duties,
c) interest owed,
d) provisions for possible future losses or charges,
e) exchange losses, cost related to return on capital,
f) costs declared or incurred, or reimbursed in respect of another Community project,
g) debt and debt service charges, excessive or reckless expenditure5.

Full coverage procedures performed:
Not Applicable because the Beneficiary uses Transitional Flat rate methods of calculation of indirect costs.

Procedures:
11. Assess use of a simplified method of calculation of overheads at the level of the legal entity. The Beneficiary may use a simplified method of calculation (either due to the lack of analytical accounting or legal requirement to use a form of cash-based accounting).
This does not permit the use of a generalised estimate, or the use of a 'standard' rate that is not derived from the accounting records of the period in question. Thus the rate (but not the methodology) should be updated for each accounting period.

Full coverage procedures performed:
Not Applicable because the Beneficiary uses Transitional Flat rate methods of calculation of indirect costs.

Procedures:
12. Inspect and compare exchange rates into Euros.

Full coverage procedures performed:

The Beneficiary uses accounts in Euro and converts costs incurred in other currencies according to their usual accounting practice, according to art. II.6 n. 4 of the grant agreement.

Procedures:
13. Identification of receipts. The Beneficiary is obliged to declare in its claim any receipts related to the project (income from events, rebates from suppliers, etc.)

Full coverage procedures performed:
The Auditor examined the relevant project accounts and obtained representations from the Beneficiary that no receipts must be claimed.

Procedures:
14. Identification of interest yielded on pre-financing. The Beneficiary, when it is the coordinator of the project, is obliged to declare interest yielded on pre-financing

Full coverage procedures performed:
The beneficiary is not the project coordinator

Roma, 18 November 2010

Studio Legale e Commerciale Associato
R. Cippitani, R. Di Gioacchino I.Iozzolino & A. Chiappalupi
Roberto Di Gioacchino
(Legal Representative and Revisore contabile)

Albo dott. Comm. Roma n. 7290 - Reg. rev. cont. n. 104277 - Dott. Roberto Di Gioacchino

Ministero della Giustizia

Consiglio Nazionale dei Dottori Commercialisti e degli Esperti Contabili

Registro Revisori Legali S.r.l.

Roma, 3 giugno 2010

SI ATTESTA CHE

Cognome Nome: DI GIOACCHINO ROBERTO

Nato a: TERNI il 20 aprile 1965

Codice Fiscale: DGCRRT65D20L117R

Residente in: STRADA DI CIVITELLA, 121 - TERNI (TR)

con D.M. del 25 novembre 1999 pubblicato nella Gazzetta Ufficiale della Repubblica Italiana, supplemento n. 100 del 17 dicembre 1999, è stato iscritto nel Registro dei Revisori Contabili secondo quanto disposto dal D.Lgs. 27 gennaio 1992 n. 88 con decorrenza giuridica dal 17 dicembre 1999.

Lo stesso ha assunto il numero progressivo 104277, risulta ancora iscritto e, per effetto del D.Lgs. 27 gennaio 2010 n. 39 art. 43, comma quarto, a decorrere dal 7 aprile 2010, è revisore legale.

Si rilascia, a richiesta dell'interessato, in carta da bollo, per gli usi consentiti dalla legge.

Il Consigliere Segretario
(Prof. Giorgio Sganga)

00185 Roma - Piazza della Repubblica, 68 - Tel. 06.45236501

ALMA MATER STUDIORUM UNIVERSITA' DI BOLOGNA

DIPARTIMENTO DI ELETTRONICA INFORMATICA E SISTEMISTICA
Direzione e amministrazione: Viale Risorgimento 2 - 40136 Bologna (I)
Tel. 051 2093001 - Fax 051 2093073 - C.F. 80007010376 - P.IVA 01131710376

1.B Related to the Certificate on the Financial Statements (Form D)
Letter of Representation

Bologna, 01.10.2010

Studio Legale e Commerciale Associato
Cippitani, Di Gioacchino & Iozzolino
Via Margutta 1-a,
00187 - **Roma**

Dear Madam, Dear Sir,
Taking into consideration our responsibility, as mentioned in Article 1.1 of Annex VII - Form D of the FP7 Grant Agreement N° 216537 (Project "Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies"- REALITY) with the European Commission and in connection with your engagement to perform agreed-upon procedures regarding the Financial Statement (Form D) covering the period from 1/01/2008 to 31/08/2010 (the "Financial Statement"), we hereby confirm the following representations made to you during your engagement:

- We are responsible for the preparation of the Financial Statement covering the period starting 1/01/2008 and ending 31/08/2010 in accordance with the Grant Agreement and for their accuracy and completeness.
- We have made available to you all records, documents, statements and information that we believe are relevant for the purpose of the agreed-upon-procedures you have performed.
- We have complied with the conditions of the consortium agreement.
- Personnel costs:
  - (Option 1) Personnel costs reported in the Financial Statement are not based on budgeted or estimated amounts. They are calculated using rates based on actual costs, and reflect the time actually worked on the REALITY project during the period covered by the Financial Statement.
- Subcontracts and contracts to suppliers of goods and services are awarded in accordance with a procedure including an analysis of best value for money (best price-quality ratio), transparency and equal treatment.
- Indirect costs reported in the Financial Statement do not include any of the following costs:
  - Identifiable indirect taxes including value added tax (for instance local business and property taxes);
  - Duties (for instance customs duties);
  - Interest owed;
  - Provisions for possible future losses or charges (for instance provisions for doubtful debt (but not normal accruals);
  - Exchange losses, cost related to return on capital (for instance exchange losses from billing in a foreign currency);
  - Costs declared or incurred, or reimbursed in respect of another Community project;
  - Debt and debt service charges,
  - Excessive or reckless expenditure (for instance loan charges);
  - Implicit interest (leasing costs or other credit arrangements);
  - Costs attributable to activities other than the research activities covered by the REALITY project, such as manufacturing, education, marketing of products or services, etc.
- Purchases in connection with the REALITY project are made according to the principles of best value for money (best price-quality ratio), transparency and equal treatment. No excessive or reckless expenditure is included in the Financial Statement.

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• The receipts declared in the Financial Statement represent a complete record of the sources of income connected with the European Commission funded project (for example, income from events, rebates from suppliers…), and have been recorded in accordance with our normal accounting practices.
• All interest yielded on pre-financing of the REALITY project during the period covered by the Financial Statement has been reported in the Financial Statement.
• No event has occurred after 31/08/2010, which would have a impact upon the Financial Statement.
• Nothing has come to our attention during the period under review, including management actions and/or other matters of importance that might be considered to represent financial irregularities, fraud or an illegal act which would have an impact on the Financial Statement

prof. Giovanni Emanuele Corazza

DIPARTIMENTO DI ELETTRONICA INFORMATICA E SISTEMISTICA * UNIVERSITA' DI BOLOGNA

STUDIO LEGALE E COMMERCIALE
R. CIPPITANI, R. DI GIOACCHINO,
I. IOZZOLINO & A. CHIAPPALUPI
UN AMMINISTRATORE

UNIVERSITA` DEGLI STUDI DI BOLOGNA
DIPARTIMENTO DI ELETTRONICA
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COD. FISC. 80007010376 – Part. IVA 01131710376

Terms of Reference for an Independent Report of Factual Findings on costs claimed under a Grant Agreement financed under the Seventh Research Framework Programme (FP7)

The following are the terms of reference ('ToR') on which Alma Mater Studiorum- Università di Bologna 'the Beneficiary' agrees to engage Studio Legale e Commerciale R. Cippitani, R. Di Gioacchino I. Iozzolino & Chiappalupi 'the Auditor' to provide an independent report of factual findings on a Financial Statements prepared by the Beneficiary and to report in connection with a European Community financed grant agreement concerning the Seventh Research Framework Programme (FP7), concerning "Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies"- REALITY-G. A. Number 216537 (the 'Grant Agreement'). Where in these ToR the 'European Commission' is mentioned this refers to its quality as signatory of the Grant Agreement with the Beneficiary. The European Community is not a party to this engagement.

1.1 Responsibilities of the Parties to the Engagement

'The Beneficiary' refers to the legal entity that is receiving the grant and that has signed the Grant Agreement with the European Commission.

The Beneficiary is responsible for preparing a Financial Statement for the Action financed by the Grant Agreement in compliance with such agreements and providing it to the Auditor, and forensuring that these Financial Statements can be properly reconciled to the Beneficiary's accounting and bookkeeping system and to the underlying accounts and records. Notwithstanding the procedures to be carried out, the Beneficiary remains at all times responsible and reliable for the accuracy of the Financial Statement.

The Beneficiary is responsible for the factual statements which will enable the Auditor to carry out the procedures specified, and will provide the Auditor with a written representation letter supporting these statements, clearly dated and stating the period covered by the statements.

The Beneficiary accepts that the ability of the Auditor to perform the procedures required by this engagement effectively depends upon the Beneficiary providing full and free access to the Beneficiary's staff and its accounting and other relevant records.

'The Auditor' refers to the Auditor who is responsible for performing the agreed-upon procedures as specified in these ToR, and for submitting an independent report of factual findings to the Beneficiary.

The Auditor must be independent from the Beneficiary.

The Auditor is qualified to carry out statutory audits of accounting documents in accordance with the Directive 2006/43/EC of the European Parliament and of the Council of 17 May 2006 on statutory audits of annual accounts and consolidated accounts, amending Council Directives 78/660/EEC and 83/349/EEC and repealing Council Directive 84/253/EEC or similar national regulations.

The procedures to be performed are specified by the European Commission and the Auditor is not responsible for the suitability and appropriateness of these procedures.

1.2 Subject of the Engagement

The subject of this engagement is *the final* financial Statement in connection with the Grant Agreement for the following periods:

P1: 01/01/2008-31/12/2008
P2: 01/01/2009 -31/12/2009
P3: 01/01/2010-31/08/2010

1.3 Reason for the Engagement

The Beneficiary is required to submit to the European Commission a certificate on a Financial Statement in the form of an independent report of factual findings produced by an external auditor in support of the payment requested by the Beneficiary under Article II.4 of the Grant Agreement. The Authorising Officer of the Commission requires this Report as he makes the payment of costs requested by the Beneficiary conditional on the factual findings of this Report.

1.4 Engagement Type and Objective

This constitutes an engagement to perform specific agreed-upon procedures regarding an independent report of factual findings on costs claimed under the Grant Agreement.

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The awarding of this engagement (DEIS 864-05/10/2010) has been accomplished according to the provisions of the Bologna University Financial regulations governing the purchase of goods and services (Art. 5, comma 1, letter q.)
As this engagement is not an assurance engagement the Auditor does not provide an audit opinion and expresses no assurance. The European Commission derives its assurance by drawing its own conclusions from the factual findings reported by the Auditor on the Financial Statement and the payment request of the Beneficiary relating thereto.
The Auditor shall include in its Report that no conflict of interest exists between it and the Beneficiary in establishing this Report, as well as the fee paid to the Auditor for providing the Report.

1.5 Scope of Work
1.5.1 The Auditor shall undertake this engagement in accordance with these ToR and:- in accordance with the International Standard on Related Services ('ISRS') 4400 *Engagements toperform Agreed-upon Procedures regarding Financial Information* as promulgated by the IFAC;
- in compliance with the *Code of Ethics for Professional Accountants* issued by the IFAC. Although ISRS 4400 provides that independence is not a requirement for agreed-upon procedures engagements, the European Commission requires that the Auditor also complies with the independence requirements of the *Code of Ethics for Professional Accountants*.
1.5.2 Planning, procedures, documentation and evidence The Auditor should plan the work so that the procedures can be effectively performed. For this purpose he performs the procedures specified in 1.9 of these Terms of Reference ('Scope of Work –Compulsory Report Format and Procedures to be Performed') and uses the evidence obtained from these procedures as the basis for the Report of factual findings.

1.6 Reporting
The Report of factual findings, an example of which is attached to this ToR, should describe the purpose and the agreed-upon procedures of the engagement in sufficient detail in order to enable the Beneficiary and the European Commission to understand the nature and extent of the procedures performed by the Auditor. Use of the reporting format attached as Annex VII of the Grant Agreement is compulsory. The Report should be written in the language indicated in Article 4 of the Grant Agreement. In accordance with Article II.22 of the Grant Agreement, the European Commission and the Court of Auditors have the right to audit any work carried out under the project for which costs are claimed from the Community, including the work related to this engagement.

1.7 Timing
The report should be delivered by 31 October 2010

1.8 Other Terms
1.8.1 Auditor's fees and out of pocket expenses
The amount of fees for the activities described in this ToR shall be calculated as follows
A fix amount of Euro 1500 plus a percentage of 0,50 % of the costs claimed in the financial costs statement of the Beneficiary.
The Beneficiary shall reimburse any out of pocket expenses related aforementioned activity.
The above mentioned fees and reimbursement shall be charged of the percentage of 4% for compulsory social charge.
Such amounts are VAT exempted within the limit of percentage of European Commission contribution as provided by the article number 72 paragraph 3 number 3 of DPR 633/1972 of Italian Law .

1.8.2 Time limits, applicable law and competent court
The timing as under paragraph 1.7 will be observed on condition that all necessary documents end information are provided.
However such documents and information shall be provided at least 20 days prior the date indicated in the paragraph 1.7.
1.8.3 The beneficiary shall provide the auditor with the documents and information listed under the annex A hereinafter enclosed and any further documents and information needed by the auditor.
1.8.4 The present agreement shall be governed by the Italian Law and the competent court shall be Terni.

1.9 Scope of Work – Compulsory Report Format and Procedures to be Performed

Independent Report of Factual Findings on costs claimed under a Grant Agreement financed under the Seventh Research Framework Programme (FP7)

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TELEFONO (051) 2093001 – FAX (051) 2093073
COD. FISC. 80007010376 – Part. IVA 01131710376

To be printed on letterhead paper of the Auditor

<Name of contact person(s)>, < Position>
< Beneficiary's name>
<Address>
<dd Month yyyy>

In accordance with our contract dated <dd Month yyyy> with <name of the Beneficiary> "the Beneficiary"
and the terms of reference attached thereto (appended to this Report), we provide our Independent Report
of Factual Findings ("the Report"), as specified below.

Objective

We *[legal name of the audit firm]*, established in *[full address/city/state/province/country]* represented for signature of this Report by [*[name and function of an authorised representative]* have performed agreedupon procedures regarding the cost declared in the Financial Statement(s) of [*name of beneficiary*] hereinafter referred to as the Beneficiary, to which this Report is attached, and which is to be presented to the Commission of the European Communities under grant agreement *[EC grant agreement reference:title, acronym, number]* for the following period(s) *[insert period(s) covered by the Financial Statement(s) per Activity]*. This engagement involved performing certain specified procedures, the results of which the European Commission uses to draw conclusions as to the eligibility of the costs claimed.

Scope of Work

Our engagement was carried out in accordance with :
- the terms of reference appended to this Report and:
- International Standard on Related Services ('ISRS') 4400 *Engagements to perform Agreed-upon Procedures regarding Financial Information* as promulgated by the International Federation of Accountants ('IFAC);
- the *Code of Ethics for Professional Accountants* issued by the IFAC. Although ISRS 4400 provides that independence is not a requirement for agreed-upon procedures engagements, the European Commission requires that the Auditor also complies with the independence requirements of the *Code of Ethics for Professional Accountants;*

As requested, we have only performed the procedures set out in the terms of reference for this engagement and we have reported our factual findings on those procedures in the table appended to this Report.

The scope of these agreed upon procedures has been determined solely by the European Commission and the procedures were performed solely to assist the European Commission in evaluating whether the costs claimed by the Beneficiary in the accompanying Financial Statement has been claimed in accordance with the Grant Agreement. The Auditor is not responsible for the suitability and appropriateness of these procedures.

Because the procedures performed by us did not constitute either an audit or a review made in accordance with International Standards on Auditing or International Standards on Review Engagements, we do not express any assurance on the Financial Statements.

Had we performed additional procedures or had we performed an audit or review of the Financial Statements of the Beneficiary in accordance with International Standards on Auditing, other matters might have come to our attention that would have been reported to you.

Sources of Information

The Report sets out information provided to us by the management of the Beneficiary in response to specific questions or as obtained and extracted from the Beneficiary's information and accounting systems.

Factual Findings

The above mentioned Financial Statement(s) per Activity was (were) examined and all procedures specified in the appended table for our engagement were carried out. On the basis of the results of these procedures, we found:

All documentation and accounting information to enable us to carry out these procedures has been provided to us by the Beneficiary. Except as indicated below, no exceptions were noted.

Exceptions

In some cases, the Auditor was not able to successfully complete the procedures specified.
These exceptions are as follows:

UNIVERSITA` DEGLI STUDI DI BOLOGNA
DIPARTIMENTO DI ELETTRONICA
INFORMATICA E SISTEMISTICA

DIREZIONE E AMMINISTRAZIONE
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TELEFONO (051) 2093001 – FAX (051) 2093073
COD. FISC. 80007010376 – Part. IVA 01131710376

exceptions such as inability to reconcile key information, unavailability of data which prevented the Auditor from carrying out the procedures, etc. should be listed here. The Commission will use this information to decide the amounts which will be reimbursed.

Use of this Report

This Report is solely for the purpose set forth in the above objective.

This Report is prepared solely for the confidential use of the Beneficiary and the EuropeanCommission and solely for the purpose of submission to the European Commission in connection with the requirements as set out in Article II.4.4 of the Grant Agreement. This Report may not be relied upon by the Beneficiary or by the European Commission for any other purpose, nor may it be distributed to any other parties. The European Commission may only disclose this Report to others who have regulatory rights of access to it, in particular the European Anti Fraud Office and the European Court of Auditors.

This Report relates only to the Financial Statement(s) specified above and does not extend to any other financial statements of the Beneficiary.

No conflict of interest exists between the Auditor and the Beneficiary in establishing this Report. The fee paid to the Auditor for providing the Report was € _____.

We look forward to discussing our Report with you and would be pleased to provide any further information or assistance which may be required.

[legal name of the audit firm]
[[name and function of an authorised representative]
<dd Month yyyy>,<Signature of the Auditor>

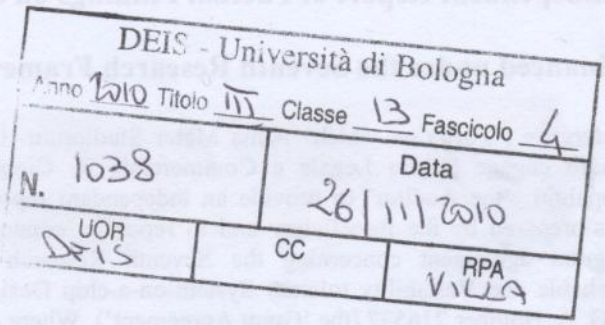
Date, 1/10/2010

On behalf of the Beneficiary

DIPARTIMENTO DI ELETTRONICA INFORMATICA E SISTEMISTICA
UNIVERSITA' DI BOLOGNA

On behalf of Studio Legale e Commerciale R. Cippitani, R. Di Gioacchino & I. Iozzolino

STUDIO LEGALE E COMMERCIALE
R. CIPPITANI, R. DI GIOACCHINO,
I. IOZZOLINO & A. CHIAPPALUPI
UN AMMINISTRATORE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Mr B Jansen
Office of the CTO Operations Manager
ARM Limited
110 Fulbourn Road
CAMBRIDGE
CB1 9NJ

10 December 2010

Dear Mr Jansen

In accordance with our contract dated 26 November 2010 with ARM Limited "the Beneficiary" and the terms of reference attached thereto (appended to this report), we provide our Independent Report of Factual Findings ("the Report"), as specified below.

Objective

We, Staffords Cambridge LLP, established in CPC1, Capital Park, Fulbourn, CAMBRIDGE, CB21 5XE, UK, represented for signature of this Report by Matthew Pettifer (a Partner in the Firm) have performed agreed-upon procedures regarding the cost declared in the Financial Statements of ARM Limited, hereinafter referred to as the Beneficiary, to which this Report is attached, and which is to be presented to the Commission of the European Communities under grant agreement N° 216537 (REALITY) for the following periods; January 2008 through December 2008, January 2009 through December 2009 and January 2010 through June 2010.

This engagement involved performing certain specified procedures, the results of which the European Commission uses to draw conclusions as to the eligibility of the costs claimed.

Scope of Work

Our engagement was undertaken in accordance with:

- the terms of reference appended to this Report and:
- International Standard on Related Services ('ISRS') 4400 *Engagements to perform Agreed-upon Procedures regarding Financial Information* as promulgated by the International Federation of Accountants ('IFAC);
- the *Code of Ethics for Professional Accountants* issued by the IFAC. Although ISRS 4400 provides that independence is not a requirement for agreed-upon procedures engagements, the European Commission requires that the Auditor also complies with the independence requirements of the *Code of Ethics for Professional Accountants*

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J R Stafford LLB FCA CTA M Inst D
S D Ellis MA (Oxon) ACA
M C A Pettifer MA (Cantab) ACA CTA

10 December 2010

As requested, we have only performed the procedures set out in the terms of reference for this engagement and we have reported our factual findings on those procedures in the table appended to this Report.

The scope of these agreed upon procedures has been determined solely by the European Commission and the procedures were performed solely to assist the European Commission in evaluating whether the costs claimed by the Beneficiary in the accompanying Financial Statement has been claimed in accordance with the Grant Agreement. The Auditor is not responsible for the suitability and appropriateness of these procedures.

Because the procedures performed by us did not constitute either an audit or review made in accordance with International Standards on Auditing or International Standards on Review Engagements, we do not express any assurance on any Financial Statements.

Had we performed additional procedures or had we performed an audit or review of the Financial Statements of the Beneficiary in accordance with International Standards on Auditing, other matters might have come to our attention that would have been reported to you.

Sources of Information

The Report sets out information provided to us by the management of the Beneficiary in response to specific questions or as obtained and extracted from the Beneficiary's information and accounting systems.

Factual Findings

The above mentioned Financial Statements per Activity were examined and all procedures specified in the appended table for our engagement were carried out. On the basis of the results of these procedures we found:

All documentation and accounting information to enable us to carry out these procedures has been provided to us by the Beneficiary. Except as indicated below no exceptions were found.

/....cont'd

10 December 2010

Exceptions

In some cases the Auditor was not able to successfully complete the procedures specified. These exceptions are as follows:

1. The Financial Statements and the procedures thereon refer to "productive hours", being total contracted hours, less holiday, public holiday, training and sickness. In the Financial Statements and the calculations backing them up the hours used as the divisor in the calculations was found to be the contracted hours less holidays and public holidays only. The result of this is that the divisor is greater than it could otherwise be and so the allocated costs are less than they could potentially be. We did not undertake to pursue this any further for the purposes of the calculation of the average productive hours in procedure 1 as the difference is in the ECs favour.

2. Although time records are kept on a weekly basis they are only signed off at project completion by the project manager as a true record of the time allocated to the project and not on a weekly or monthly basis.

3. All costs are intended to be actual, but in the case of the indirect costs the basis for the allocation is normally the agreed actual costs from the previous audited Financial Statements for the 31 December year end. This has meant that in the final reporting the indirect costs for January to June 2010 use the rates from the year to 31 December 2009 but these have been found to be lower than the actual costs for the first 6 months of 2010 from a report produced for us by the Beneficiaries finance department.

Use of this Report

This Report is solely for the purpose set forth in the above objective

This report is prepared solely for the confidential use of the Beneficiary and the European Commission and solely for the purpose of submission to the European Commission in connection with the requirements set out in Article II.4.4 of the Grant Agreement. This Report may not be relied upon by the Beneficiary or by the European Commission for any other purpose, nor may it be distributed to any other parties. The European Commission may only disclose this Report to others who have regulatory rights of access to it, in particular the European Anti Fraud Office and the European Court of Auditors.

This report relates only to the Financial Statements specified above and does not extend to any other Financial Statements of the Beneficiary.

/....cont'd

10 December 2010

No conflict of interest exists between the Auditor and the Beneficiary in establishing this Report. The fee paid to the Auditor for providing the Report was €2,433 excluding VAT.

We look forward to discussing our Report with you and would be pleased to provide any further information or assistance which may be required.

Yours sincerely

Staffords Cambridge LLP

STAFFORDS CAMBRIDGE LLP
Mr MCA Pettifer