E3NETWORK

Energy Efficient E-band transceiver for backhaul of the future networks

DELIVERABLE **D.2.2**

Report on the measurements of the E-Band RF /Analogue Front-end Blocks 1

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1	26/06/2014	R. Berenguer (CEIT)	Draft version
2	20/07/2014	D. del Rio (CEIT) R. Berenguer (CEIT) I. Guruceaga (CEIT) J. L. Gonzalez (CEA-Leti) W. Debski (SiR) C. Martinez (INCIDE)	All sections
3	23/07/2014	D. del Rio (CEIT) J.F. Sevillano (CEIT)	Index of acronyms and Section 6 added

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INDEX OF ACRONYMS

- ADC: Analog to digital converter
- BGA: Ball grid array
- BW: Bandwidth
- CE: Common emitter
- DAC: Digital to analog converter
- DNL: Differential nonlinearity
- EM: Electromagnetic
- ENOB: Effective number of bits
- ESD: Electrostatic discharge
- FMC: FPGA Mezzanine Card
- FPGA: Field programmable gate array
- FS: Frequency synthesizer
- HGM: High gain mode
- I/O: Input / Output
- I/Q: In-phase / Quadrature
- IF: Intermediate frequency
- IFA: Intermediate frequency amplifier
- ILO: Injection-locked oscillator
- INL: Integral nonlinearity
- IRR: Image rejection ratio
- LGM: Low gain mode
- LNA: Low-noise amplifier
- LO: Local oscillator
- LVDS: Low-voltage differential signaling
- MDAC: Multiplying digital to analog converter
- mmW: Millimeter wave
- MN: Matching network
- MOM: Metal-Oxide-Metal
- NF: Noise figure
- OCP1dB: Output 1dB compression point
- PA: Power amplifier
- PAE: Power-added efficiency
- PCB: Printed circuit board
- PDK: Process design kit
- PFD: Phase frequency detector
- PLL: Phase-locked loop
- PLS: Post layout simulation
- PN: Phase noise
- PTAT: Proportional to absolute temperature
- QAM: Quadrature amplitude modulation
- Rx: Receiver
- SFDR: Spurious-free dynamic range
- SINAD: Signal-to-noise and distortion ratio
- SPI: Serial peripheral interface
- Tx: Transmitter
- VCO: Voltage-controlled oscillator

EXECUTIVE SUMMARY

This document presents simulation results of the re-designed building blocks of the analogue transmitter and receiver front-ends. These results show that most of the specifications of these building blocks in the updated D1.2.2 document are fulfilled. Furthermore, a much lower DC power consumption than in other commercial solutions is observed.

In the transmitter part, the IF I/Q modulator, PA and mmW up-converter mixer have been redesigned. Within the receiver, the LNA, IF amplifier and mmW down-converter mixer have been redesigned. Simulation results of all these blocks are provided within this document. Moreover, simulation results of the re-designed frequency synthesis blocks are presented.

For the converters, a testing platform for the designed digital-to-analogue converter has been built. This document shows the signal integrity analysis performed for this board. Additionally, the designed ADC is described and some simulation results of the ADC presented.

Finally, system simulations have been performed with the specifications updated in D1.2.2. This document shows that the performance of the system keeps fulfilling the required specifications.

Within WP2, an early prototype of the IF circuitry, based on discrete components, has been designed and implemented. This early prototype includes both the IF I/Q modulator and demodulator. This IF prototype will be employed by WP3 to test their digital base-band processor and the parameter and estimation controller. This document presents measurement results of these early IF prototype.

1. INTRODUCTION

1.1 Description of Tx analogue Front-end

The architecture of the analogue transmitter, with the block diagram shown in Figure 1.1-1 was described in deliverable D2.1. Some of the blocks have been re-designed to fulfil the specifications for the correct system performance. The design and performance of such blocks will be presented over the document.

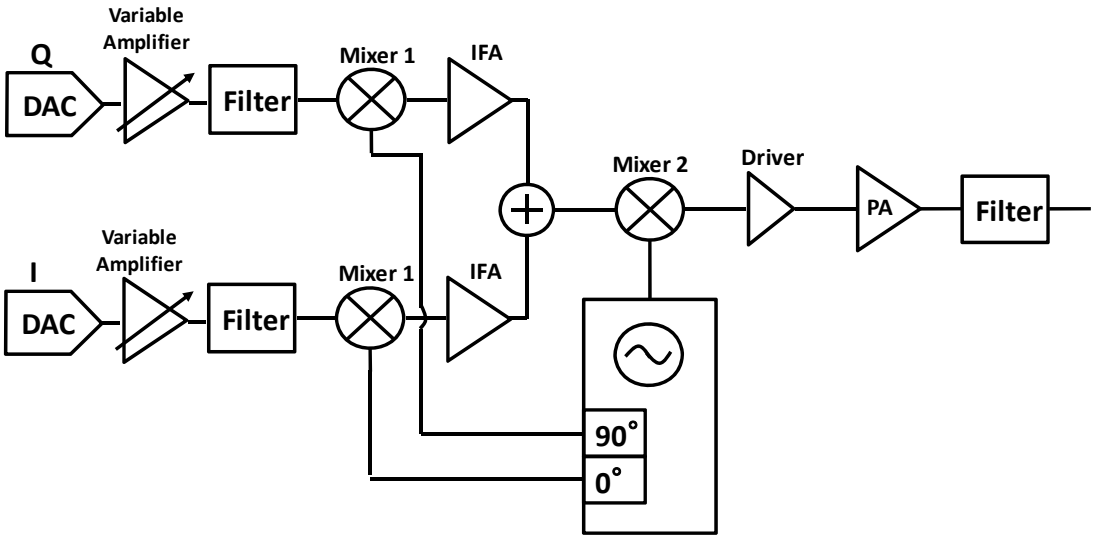


Figure 1.1-1 Block diagram of the transmitter analogue front-end

1.2 Description of Rx analogue Front-end

The architecture of the RF-analogue reception chain was presented in deliverable D1.2. Figure 1.2-1 shows the block diagram of the receiver which is a two-stage down-conversion architecture. The parameters of the receiver blocks were defined in the previous project phase and reported in D2.1.

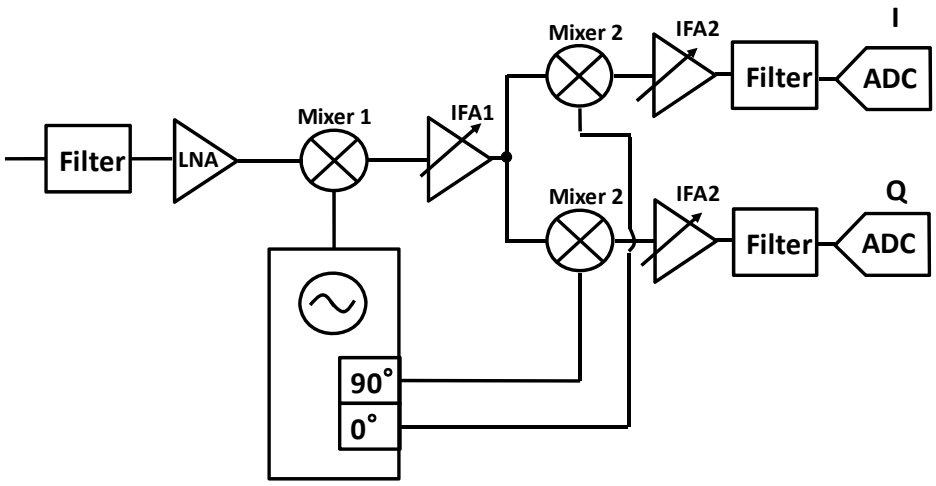


Figure 1.2-1 Block diagram of the receiver analogue front-end

1.3 Description of signal generation block for Tx and Rx

The signal generator block for Tx and Rx is composed of three subsystems: a PLL based on a 30 GHz VCO and a 25 MHz input reference, an IF LO signal generator and a mmW LO signal generator. Its block diagram is shown in Figure 1.3-1.

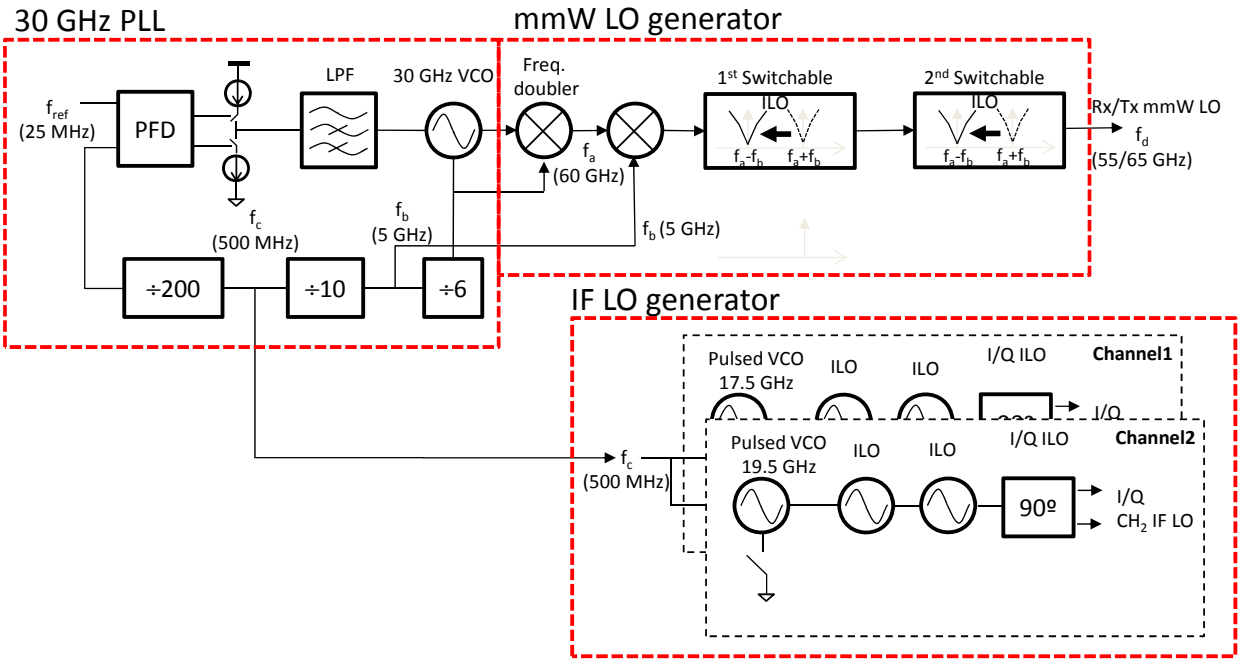


Figure 1.3-1 Block diagram of the E3Network signal generator block

The mmW LO generator is composed of a frequency doubler to obtain a 60 GHz frequency signal and a mixer that using an intermediate frequency output of the PLL at 5 GHz generates a two tone signal containing the two possible mmW LO frequencies: 55 GHz and 65 GHz. A chain of two switchable ILOs is used to select the desired frequency to be provided to the Tx or the Rx in order to address the lower or upper part of the E-band.

The IF LO generator uses an intermediate frequency of 500 MHz provided by the PLL to generate a multi-harmonic signal containing the desired IF LO frequency. This signal is filtered by a chain of two ILOs and I/Q signals are generated using a wideband poly-phase filter.

2. TX RESULTS

2.1 Updated Power Amplifier results

2.1.1. Circuit description

The circuit consists of two identical unit cells, combined at the output using an integrated balun to provide a single-ended output, as shown in Figure 2.1-1. Additionally, a balun is also added at the input, so that on-wafer measurement of the standalone power amplifier (PA) can be performed using a single-ended probe.

Figure 2.1-2 shows the schematic of each of the unit cells, with all the power cells and matching networks. They consist of 5 CE stages in addition to one pre-driver in cascode configuration placed at the input, which provides enough gain to the device and drives it to compression before the previous blocks (such as the up-conversion mixer) compress.

Each power cell is made of very high speed npn bipolar transistors, with bigger emitter areas towards the amplifier output to achieve better power handling capability and smaller sizes at the input to increase the efficiency and to achieve a higher input impedance, thus making the impedance matching easier. The total emitter area of the output stage (6^{th} stage) is 24 μm², which is reduced in 25% at the 5^{th} and 4^{th} stages. Another reduction of 12.5% is performed for stages 2^{nd} and 3^{rd}, whereas the transistors of the 1^{st} cascode stage have emitter areas of 5.2 μm², with a further reduction of 58.5%. These areas are divided into various parallel cells.

Parallel R-C networks are placed at the input of the last 4 CE stages in order to introduce losses at low frequencies and ensure inter-stage stability, which is necessary due to the feedback effect produced by the parasitic capacitances of big transistors. As for the 1^{st} CE stage, stability is ensured by placing a 1KΩ resistor between both differential cells at the output of the driver.

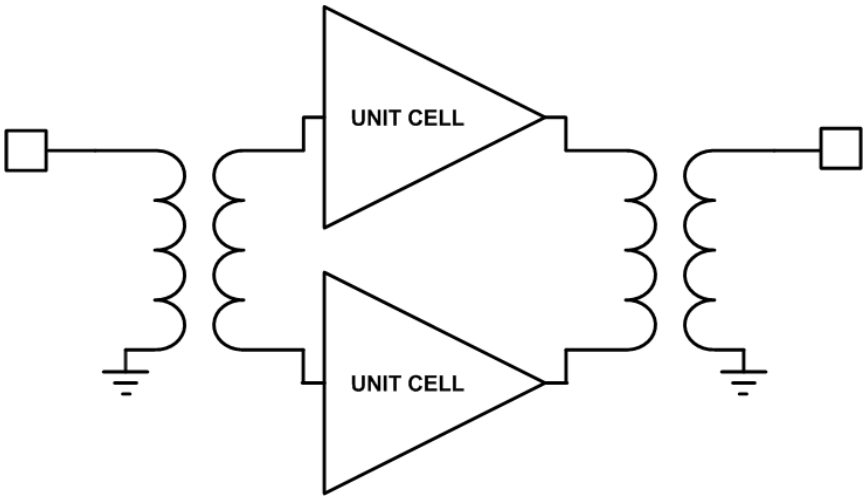


Figure 2.1-1 Block diagram of the PA architecture

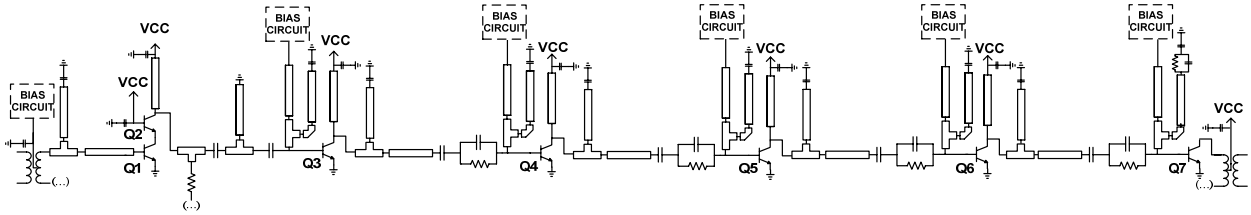


Figure 2.1-2 Simplified schematic of each PA unit cell

With regard to the impedance matching, the output balun is designed so that it presents the optimum impedance for maximum output power to the output stage, when a 50 Ω termination is placed at the output in parallel to the capacitance of the pad. Input matching is achieved using a distributed matching network at the input of the driver, so as to present a 50 Ω input impedance to a probe connected to the input pad. Inter-stage matching networks are also implemented using distributed elements and are designed to provide gain flatness over the E-Band and enough output compression power, as well as to present low impedances to the bases of the transistors, which is necessary for reliable operation above BV_{CE0}.

All the transmission lines are implemented as side-shielded microstrip lines, using the top ultra-thick metal for the main conductor and stacking the first 2 metals to provide the GND plane. Regarding the capacitors, interdigitated MOM capacitors are constructed using the top thick metals and a GND shield with the first 2 metals, so as to achieve higher Q factors at mm-wave frequencies than with the MOM capacitors provided with the PDK.

A VCC value of 1.8 V is selected, which provides a balance between safe operation above BV_{CE0} and enough voltage swing at the output for the required 1dB compression point. The different stages are independently biased using simple PTAT current mirrors, as the one shown in Figure 2.1-3, with a mirror ratio of 15:1 to minimize current consumption and increase the efficiency. Additionally, the resistor Ra is chosen small enough (~30Ω) to allow for safe operation at VCC > BV_{CE0}, whereas the bias circuit is isolated from the circuit at mm-wave frequencies by using a long transmission line for the connection. VCC and the voltage reference Vref for each stage are set externally in order to compensate for temperature and process variations and to adjust the total gain of the amplifier if necessary.

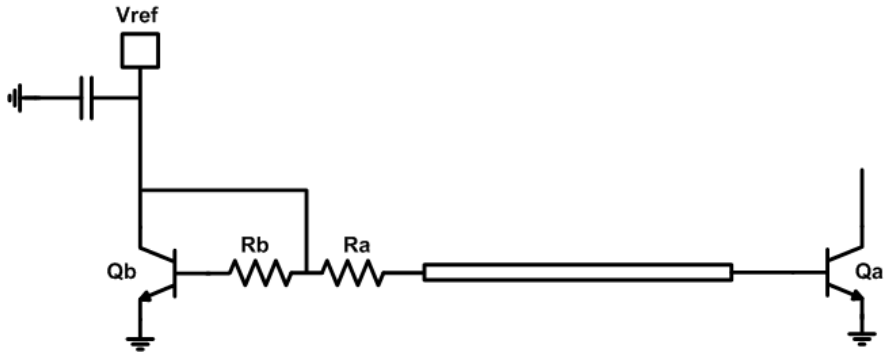


Figure 2.1-3 Schematic of a PTAT current mirror

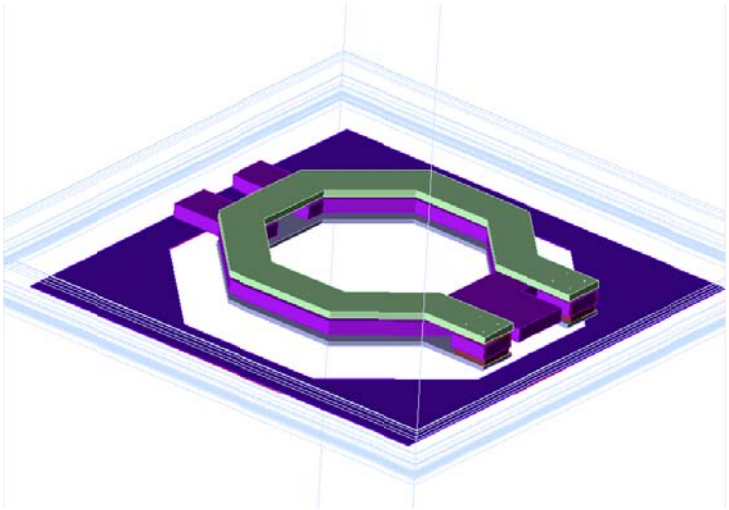


Figure 2.1-4 3D view of the implemented transformer balun

As explained before, an integrated octagonal transformer balun is used to convert the differential output to single ended. Figure 2.1-4 shows its 3D view as introduced in the EM simulator. The primary is implemented using a single turn in M8, whereas the secondary is made using single M7 and AP turns connected in parallel. Thus, the primary is surrounded at both its upper and lower sides by the secondary and the coupling is maximized, whereas the lower turn provides shielding to the primary, which is the turn with a higher current. A balun with the same structure is used at the input for testing purposes.

The final layout of the PA block occupies an area of 1692 x 924 μm² and is shown in Figure 2.1-5. All the path widths and vias are designed to fulfil the electromigration and maximum current limits at 125 ºC.

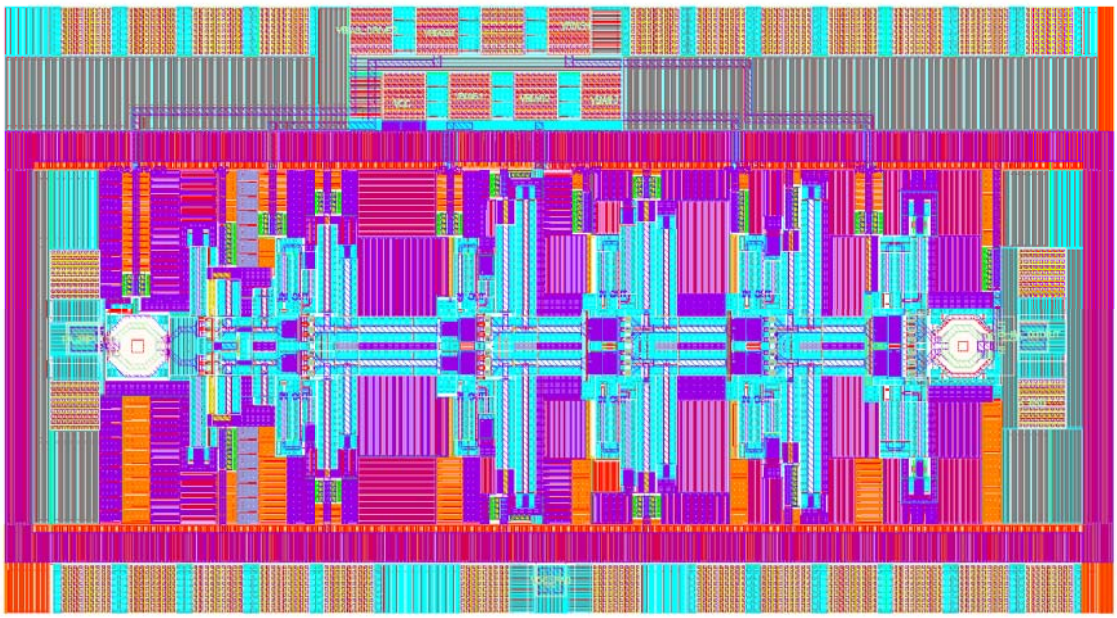


Figure 2.1-5 Layout of the PA, including PADs

2.1.2. Results

All the results presented in this section are based on post-layout simulations, in which the passive structures such as transmission lines, capacitors, baluns and interconnections have been EM simulated using *Agilent Momentum* and the transistors layouts are extracted with the RCc PLS tool included with the PDK.

The insertion loss of the output balun has been simulated standalone, and is shown in Figure 2.1-6. As it can be observed, it has a minimum loss of 0.7 dB at the centre of the E-Band and is less than 1.5 dB across the band of interest.

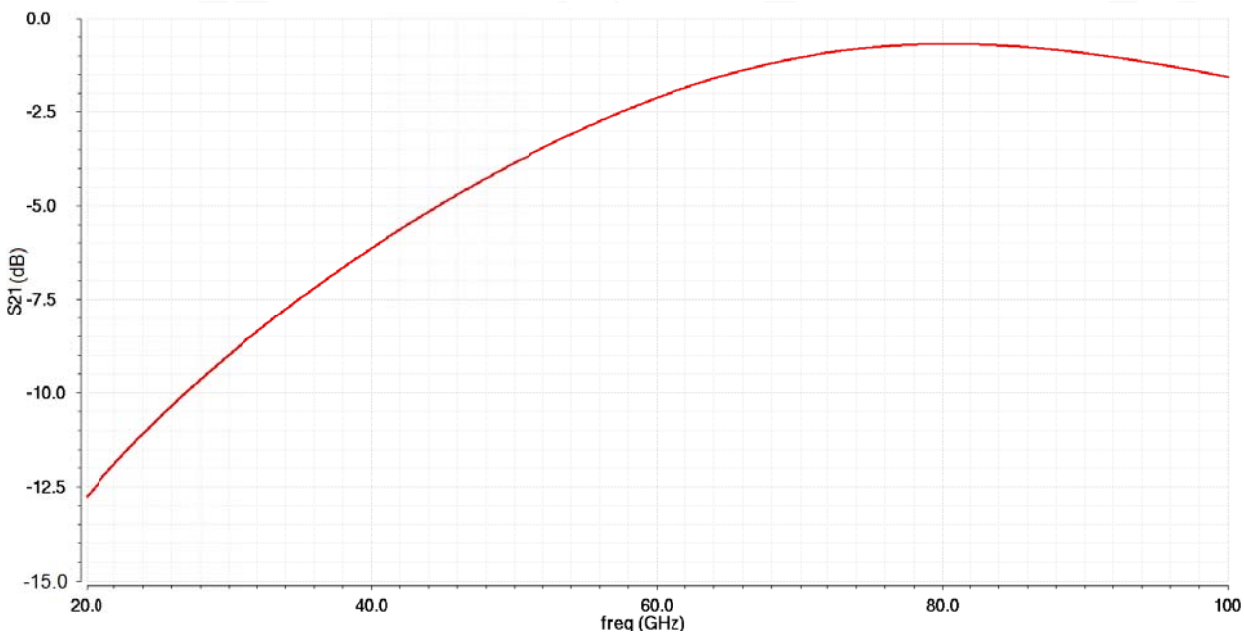


Figure 2.1-6 Simulated insertion loss of the output balun

Regarding the complete PA, Figure 2.1-7 shows the simulated S-parameters with the exception of S12, which is <-80dB and, thus, does not fit into the plot. As it can be observed, the S21 parameter has a 3-dB bandwidth of 70 - 91.8 GHz, with a maximum value of 29.8 dB at 89 GHz and a gain flatness better than 1dB across 2 GHz channels. The input matching is better than -10 dB from 65 GHz to 92 GHz and the output matching is better than -10dB from 74 GHz to 94 GHz, with a value better than -8.14 dB at the lower part of the E-Band (71-74 GHz).

In addition, the gain of the PA can be adjusted by changing the bias voltage of the pre-driver. As it is shown in Figure 2.1-8, a variation bigger than 8 dB in the S21 can be achieved, while the input matching is not significantly degraded.

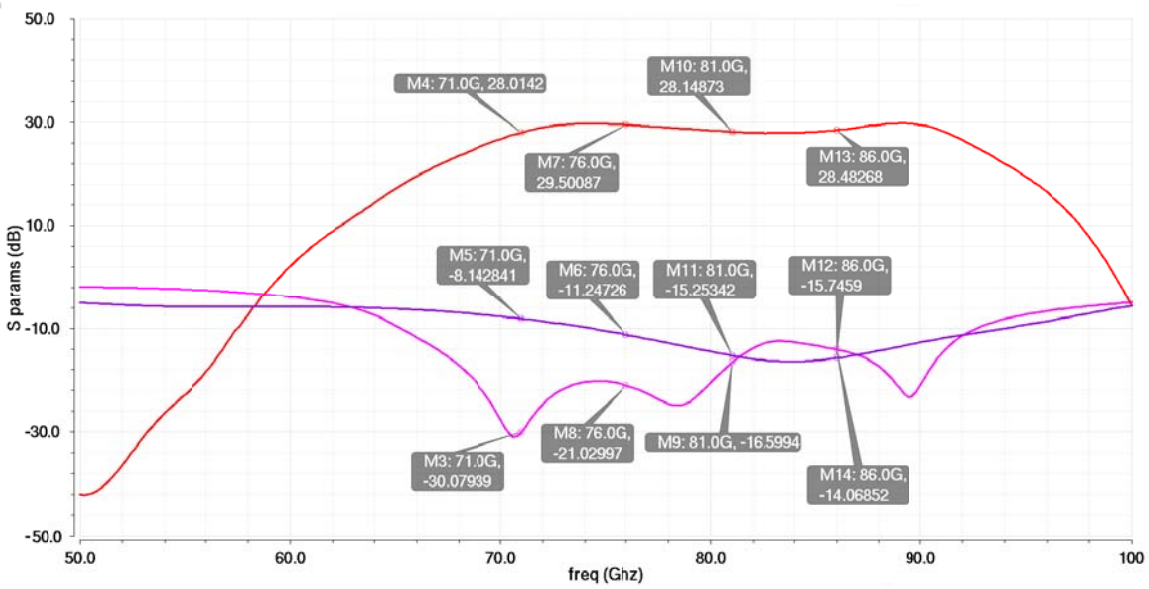


Figure 2.1-7 Simulated S-parameters of the PA

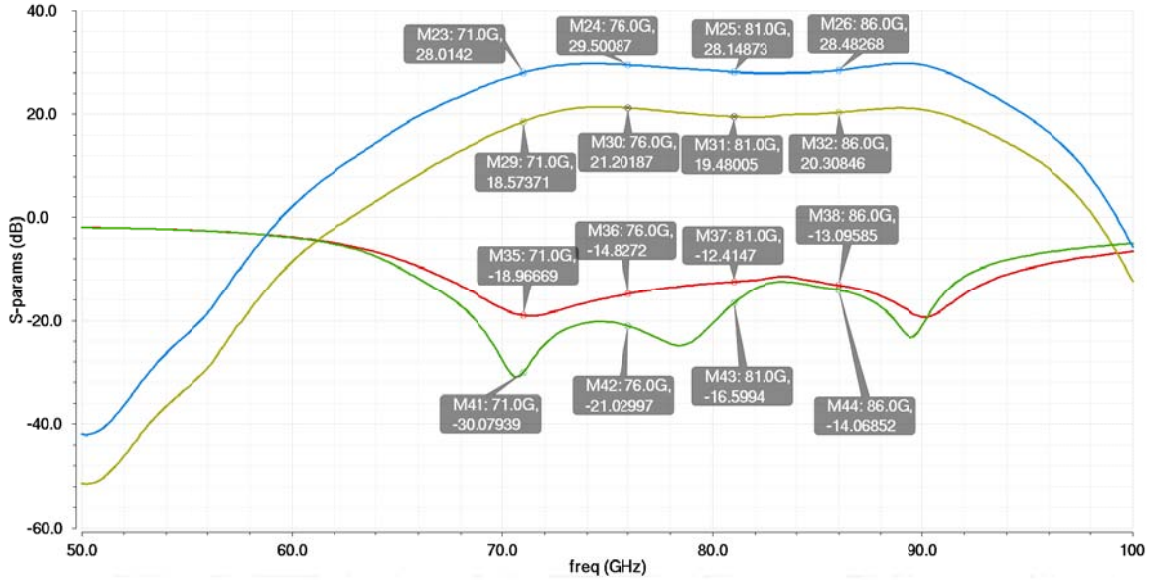


Figure 2.1-8 Variation of S21 and S11 when the bias voltage of the pre-driver is changed

As for the gain compression, Figure 2.1-9 shows the simulated power gain as a function of the input power at 71 GHz. As it can be observed, the gain increases before reaching compression, which pushes the 1dB compression point towards the saturation point (there is only a round 1dB difference between both values). This effect increases the output 1-dB compression point, which is shown in Figure 2.1-10 for the whole band of interest. A maximum value of 21 dBm is obtained at the lowest part of the E-Band, whereas it is bigger than 20.4 dBm at the highest frequencies. 1dB can be added to these values to obtain the saturation point.

Regarding the efficiency, the PAE is simulated at compression and plotted in Figure 2.1-11. It has a peak value of 21.53 % at 71GHz and a minimum value of 19.22 % at 86 GHz, for the simulated DC power consumption of 575 mW.

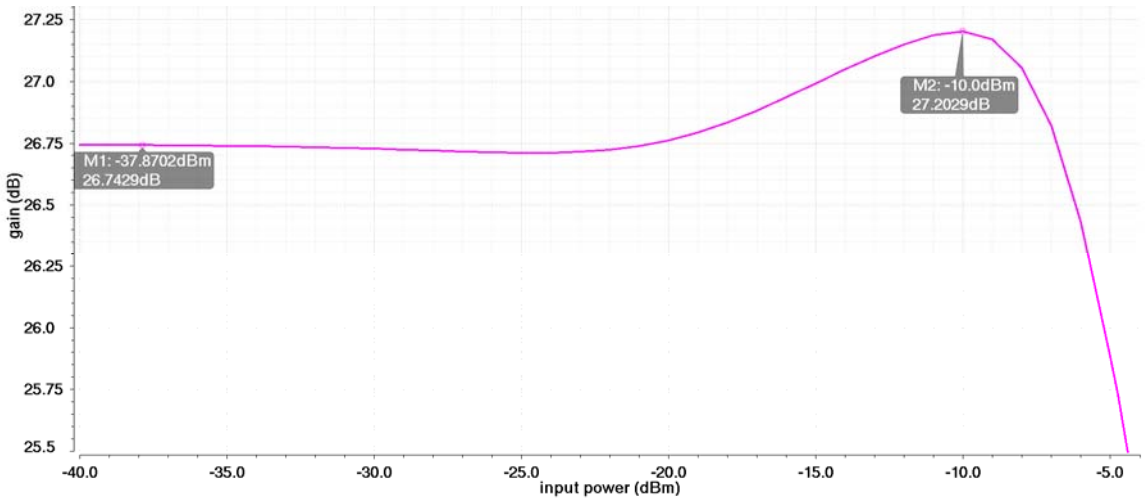


Figure 2.1-9 Simulated PA power gain as a function of Pin at 71 GHz

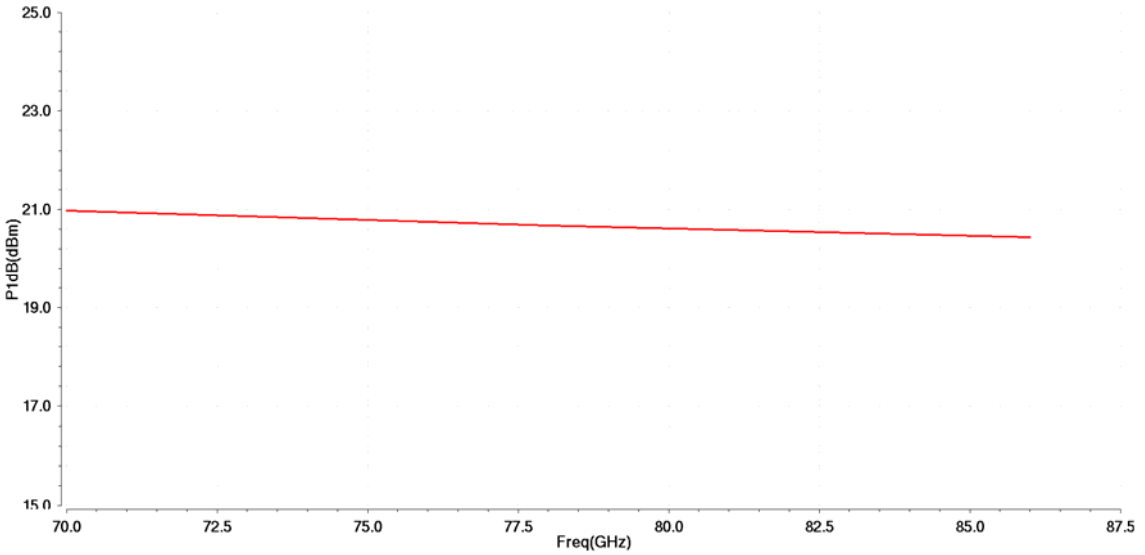


Figure 2.1-10 Simulated OCP1dB of the PA as a function of frequency

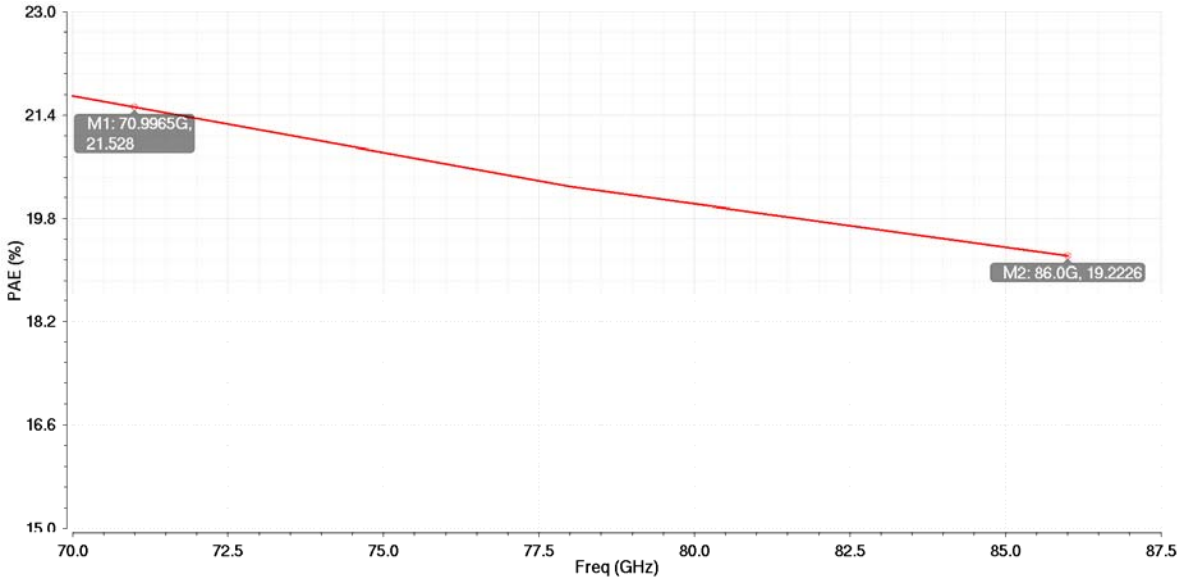


Figure 2.1-11 Simulated PAE of the PA at compression as a function of frequency

The stability of the PA is also simulated, obtaining the μ factor shown in Figure 2.1-12. A μ factor bigger than 1 is obtained for all frequencies, which ensures the unconditional stability of the amplifier.

In addition, the noise figure is plotted in Figure 2.1-13, and has a maximum value of 8.24 dB at 71 GHz and a minimum value of 7.25 dB at 76 GHz.

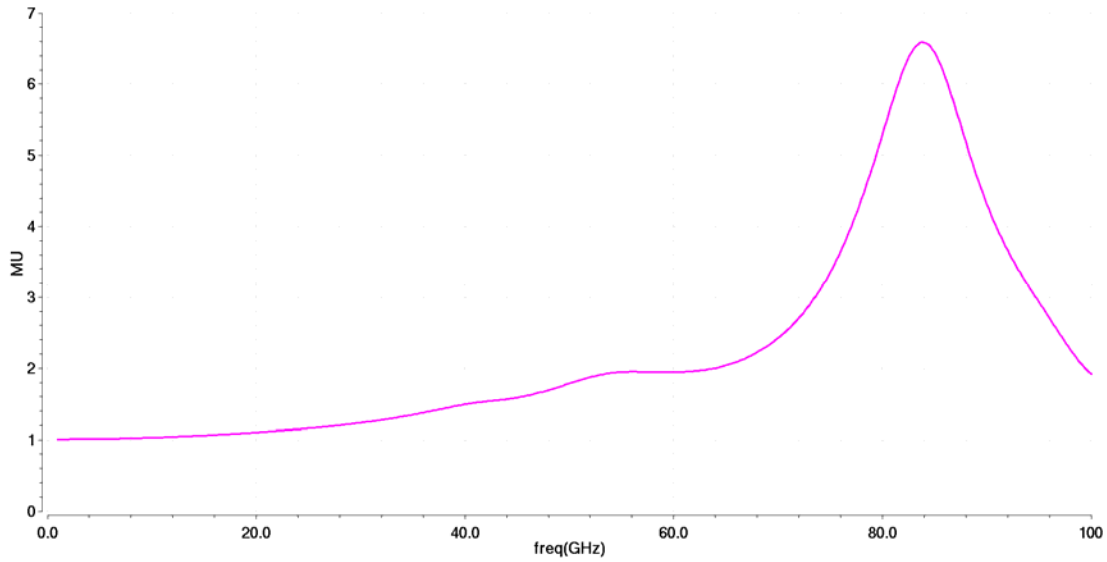


Figure 2.1-12 Simulated μ stability factor of the PA as a function of frequency

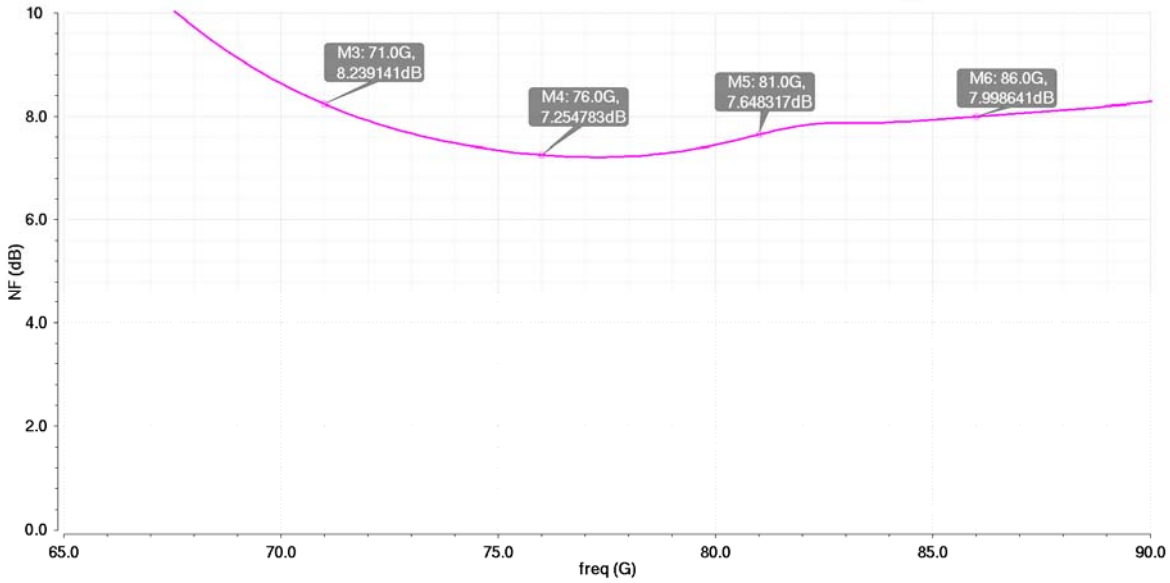


Figure 2.1-13 Simulated NF of the PA

The main results of the simulations are given and compared with those in deliverable D1.2.2 in Table 2.1-1.

Parameter	Min. Value[1]	Max. Value[2]	Spec. in D1.2.2	Comments
S21	28.01 dB	29.5 dB	28 dB	Spec. fulfilled
3-dB BW	70 Ghz	91.8 GHz	70-76 / 81-86 GHz	Spec. fulfilled
S11	-30 dB	-12 dB	< -10 dB	Spec. fulfilled
P1dB	20.4 dBm	21 dBm	18 dBm	Spec. fulfilled
DC power	-	575 mW	-	
PAE at P1dB	19.22 %	21.53 %	-	
NF	7.25 dB	8.24 dB	8.5 dB	Spec. fulfilled
VCC	-	1.8 V	-	
Area	-	1.56 mm²	-	

Table 2.1-1 Summary of simulation results for the power amplifier

1 , 2 Min. and Max. Values refer to values inside the E-Band (71-76, 81-86 GHz).

2.2 Updated mmW Mixer results

2.2.1. Circuit description

The mm-wave up-converter mixer circuit, shown in Figure 2.2-1, consists of a double-balanced mixer core and a buffer connected at the LO input of the core to drive it with more power than the typically provided by the mm-wave LO (around 0 dBm or less). Centre-tapped transformers are used to electrically isolate the LO and RF ports from the rest of the circuit as well as to provide DC biasing.

Additionally, two more transformer baluns are added to provide single-ended inputs at the IF and LO ports, so that on-wafer measurement can be performed. These ports are also matched to 50 Ω, taking the PAD capacitances into account. A resistor is used for impedance matching at the LO port, whereas a resistor in parallel with a MOM capacitor provided with the PDK are used for matching the IF input. As for the RF output, it is left differential because it will not be measured standalone but connected to the PA. A 50 Ω load is expected at this point, which is transformed to the optimum impedance for conversion gain and compression of the mixer by a custom-made MOM capacitor placed in parallel with the transformer.

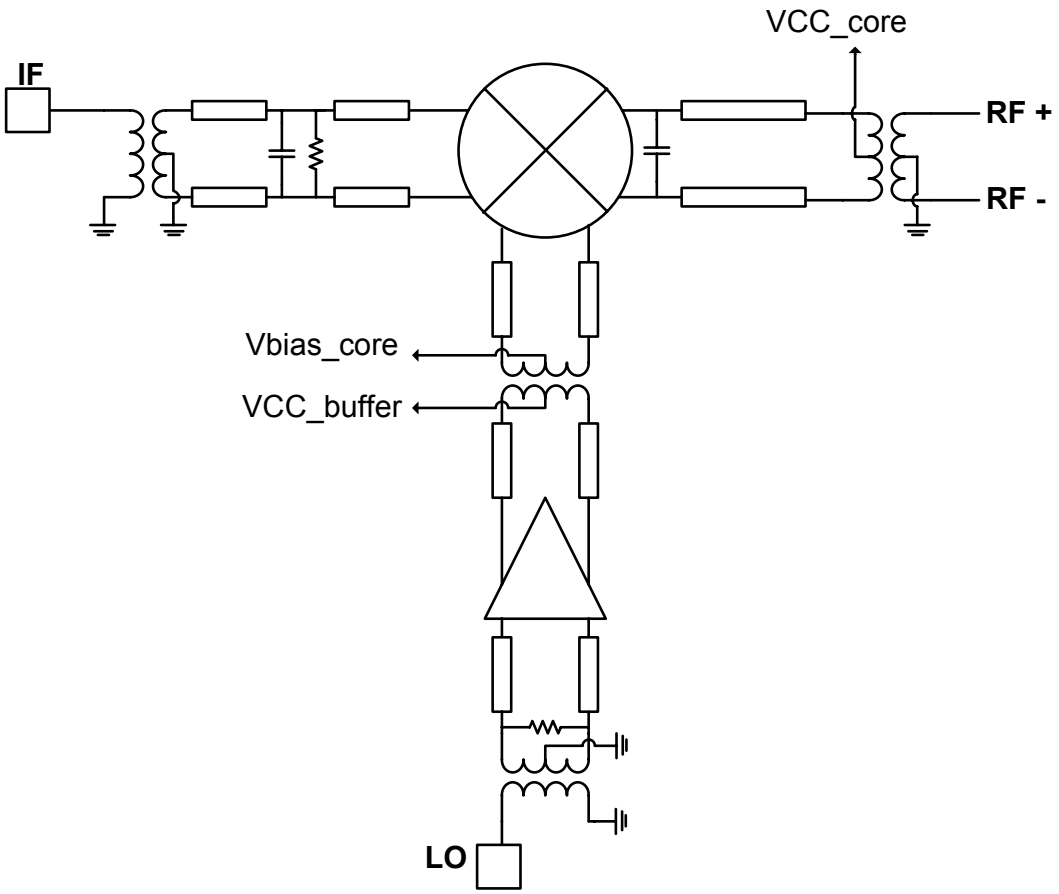


Figure 2.2-1 Block diagram of the mmW mixer

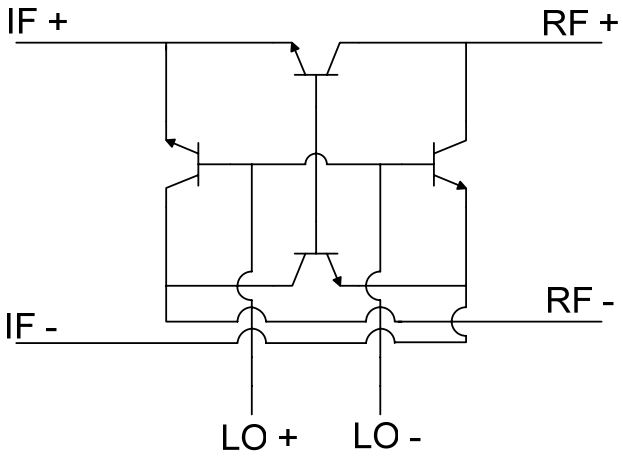


Figure 2.2-2 Schematic of the mmW mixer core

The mixer core is implemented using a double-balanced passive ring architecture, using bipolar transistors for the switching as shown in Figure 2.2-2. A DC voltage of 650 mV is applied to the transistor bases, which helps minimizing conversion losses but still makes the DC current consumption negligible, and a VCC value of 1.4 V is selected. Both DC voltages are applied through the centre taps of the transformers, as explained before.

The schematic of the LO buffer can be seen in Figure 2.2-3. It consists of a differential common-base amplifier, where a bias voltage of 800 mV is applied to the bases through two big resistors. Both the VCC voltage of 1.3V for the collectors and the DC ground path for the emitters are provided using the centre taps of the transformers.

The simulated total DC consumption is 2.4 mW, mostly consumed by the LO buffer. All the DC voltages can be controlled externally, so that temperature and process variations, as well as inaccuracies of the models can to some extent be compensated. This way it is also possible to tune the conversion gain of the mixer and adapt to variations of the power provided by the LO.

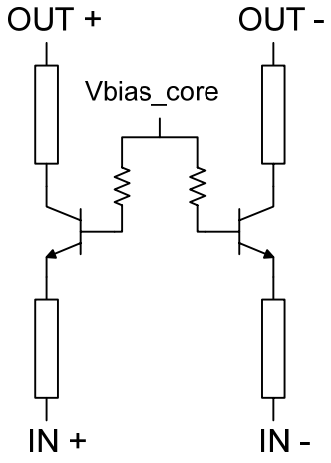


Figure 2.2-3 Schematic of the mmW LO buffer

Figure 2.2-4 shows the layout of the described block, with a total area of 0.307 mm².

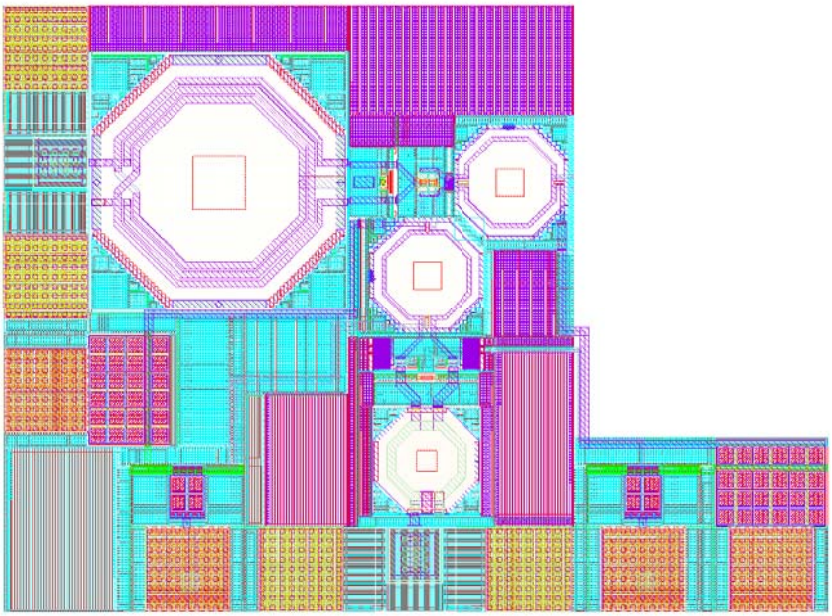


Figure 2.2-4 Layout of the mmW mixer, including PADs

2.2.2. Results

The same procedure explained in Section 2.1.2 has been followed for the post-layout simulations of the mm-Wave up-converter mixer, and all the simulations assume a power of 0 dBm at the LO port and 50 Ω load at the RF output.

Figure 2.2-5 shows the conversion gain as a function of the IF for LO frequencies of 55 and 65 GHz, which result in output frequencies of 71.5-75.5 GHz and 81.5 – 85.5 GHz. As it can be observed, the gain ranges from -5.32 to -4.76 dB at the lower part of the E-Band and from -4.49 to -5.04 dB at the higher part, resulting in a gain flatness better than 0.6 dB at each sub-band.

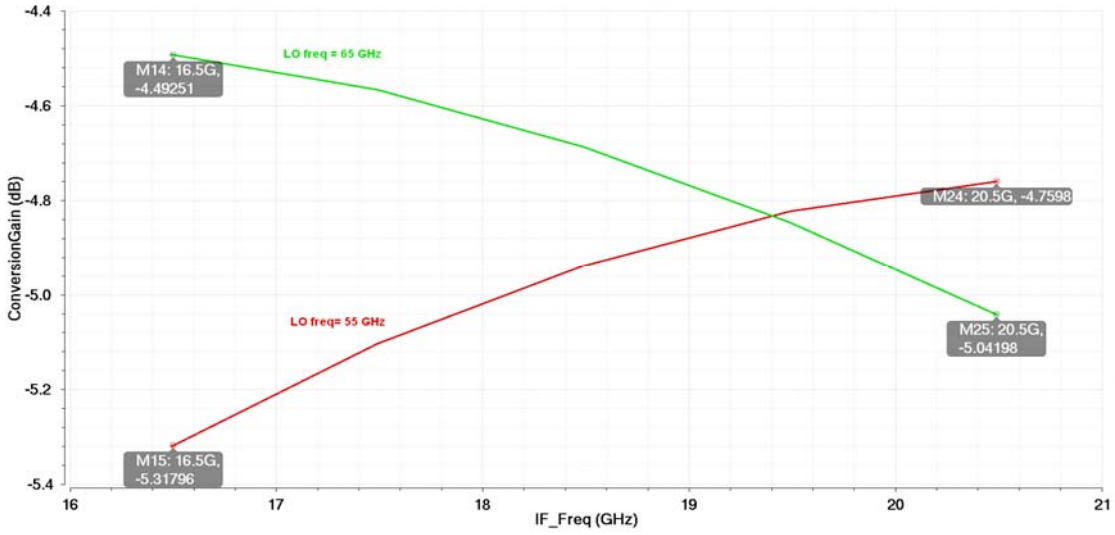


Figure 2.2-5 Simulated conversion gain of the mmW mixer for LO frequencies of 55 and 65 GHz

Similarly, the output 1 dB compression point is plotted in Figure 2.2-6 as a function of the IF for LO frequencies of 55 and 65 GHz. As it is shown, it is better than -5 dBm for the 81-86 GHz band and better than 2 dBm for the 71-76 GHz band, which allows for the required back-off.

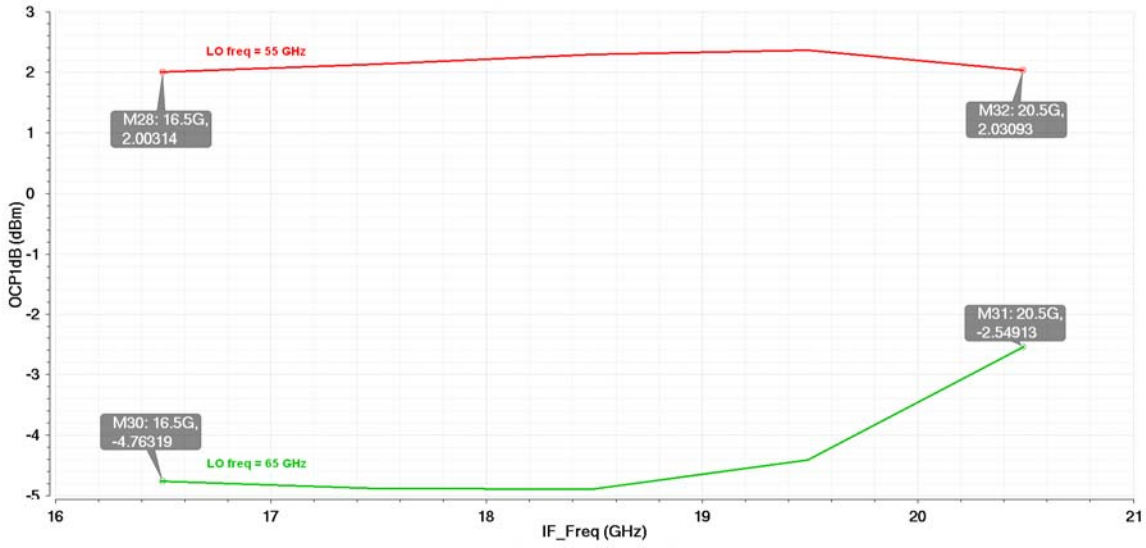


Figure 2.2-6 Simulated output P1dB of the mmW mixer for LO frequencies of 55 and 65 GHz

Figure 2.2-7 and Figure 2.2-8 show the reflection coefficients at the IF and LO ports respectively, when a 50 Ω single-ended port is connected to them. The input matching at these ports is better than -10 dB from 15 to 22.75 GHz at the IF port and from 49.29 to 67.72 GHz at the LO port. The bandwidth of the input matching covers, therefore, the input IF band and the considered LO frequencies of 55 and 65 GHz.

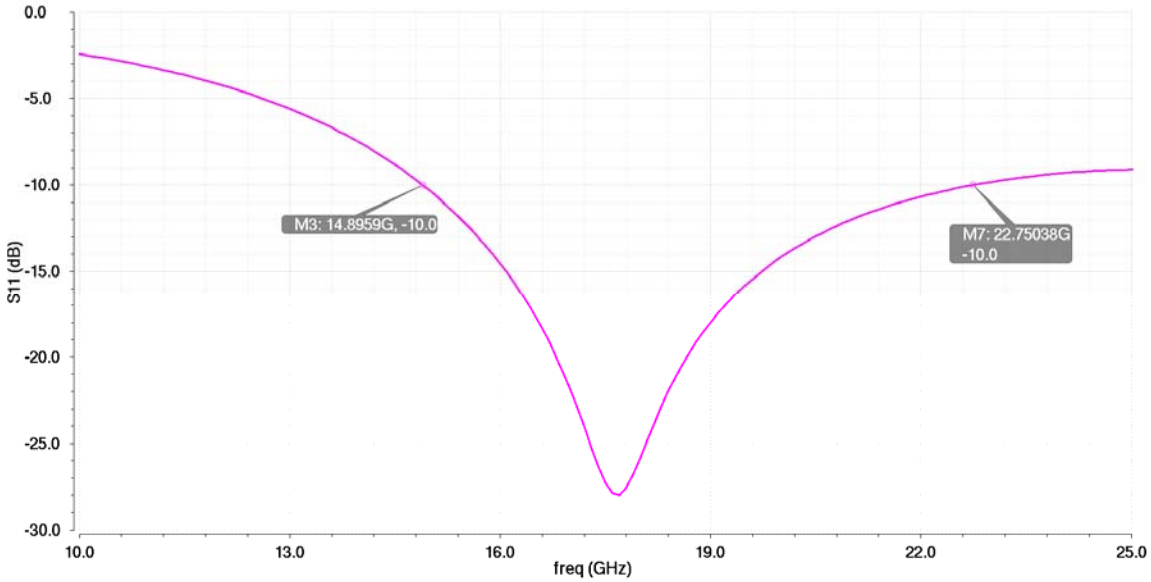


Figure 2.2-7 Simulated input matching at the IF port of the mmW mixer

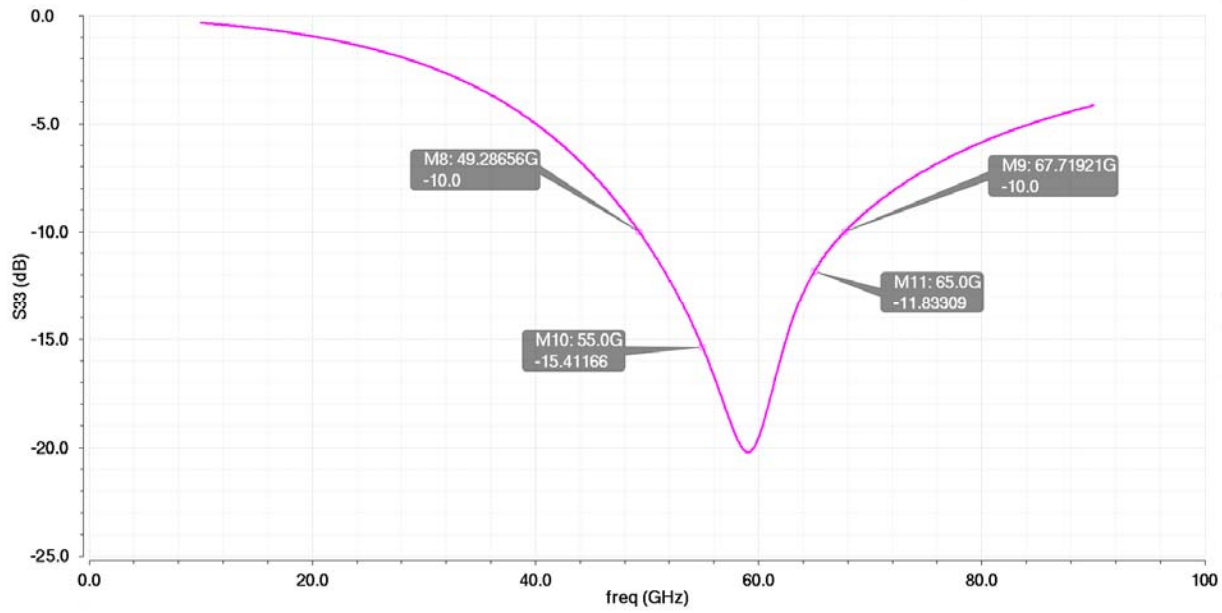


Figure 2.2-8 Simulated input matching at the LO port of the mmW mixer

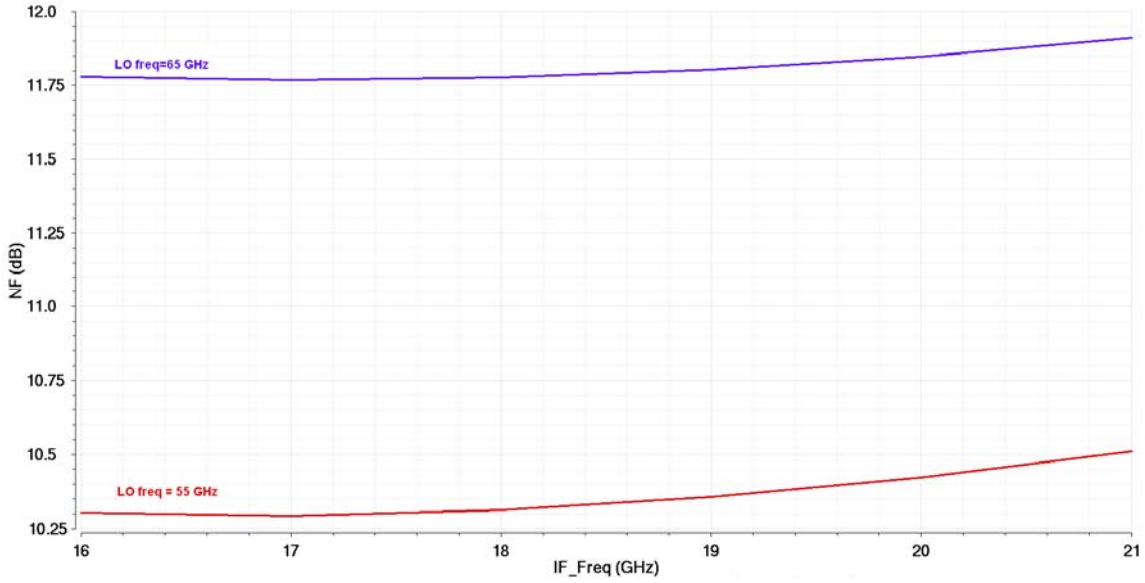


Figure 2.2-9 Simulated noise figure of the mmW mixer for LO frequencies of 55 and 65 GHz

In addition, the NF of the mixer is lower than 10.55 dB at the 71-76 GHz band and lower than 11.9 dB at the 81.86 GHz band, as it can be derived from the plot in Figure 2.2-9.

Table 2.2-1 summarizes the main simulation results and compared them to the specifications of the block.

Parameter	Min. Value	Max. Value	Spec. in D1.2.2	Comments
Conversion Gain	-5.32 dB	-4.49 dB	-8 dB	A variable attenuator is planned to be included in the next redesign
Output bandwidth	70 GHz	87 GHz	70-77 / 80-87 GHz	Spec. fulfilled
IF bandwidth	15 GHz	21 GHz	15-21 GHz	Spec. fulfilled
LO frequency	55 GHz	65 GHz	55 / 65 GHz	Spec. fulfilled
Input matching at IF port	-28 dB	-10 dB	-	
Input matching at LO port	-20 dB	-10 dB	-	
Output P1dB	-4.8 dBm	2.4 dBm	-5 dBm	Spec. fulfilled
Noise Figure	10.3 dB	11.9 dB	12 dB	Spec. fulfilled
DC power	-	2.4 mW	-	
Area	-	0.307 mm²	-	

Table 2.2-1 Summary of simulation results for the mmW up-conversion mixer

2.3 mmW Tx module (mmW mixer & PA) results

2.3.1. Circuit description

Once the mmW mixer and the PA were designed, they have been integrated in a single circuit, as an approach to the final integrated transmitter. A 50 Ω differential impedance was chosen for the interface between both blocks due to simplicity reasons.

In order to make the connection, the input balun is removed from the PA input to make it differential and a matching network (MN) is added, as shown in Figure 2.3-1. As in the standalone PA the bias for the 1st stage (cascode pre-driver) was applied through the centre tap of the balun, two big resistors are added now to both positive and negative inputs connected to the bias point.

The layout of the circuit can be observed in Figure 2.3-2, occupying an area of 1.627 mm².

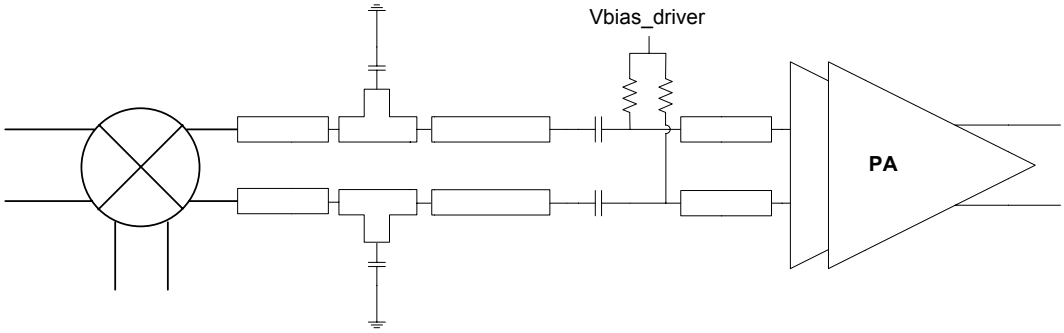


Figure 2.3-1 Schematic of the MN between the mmW mixer and the PA

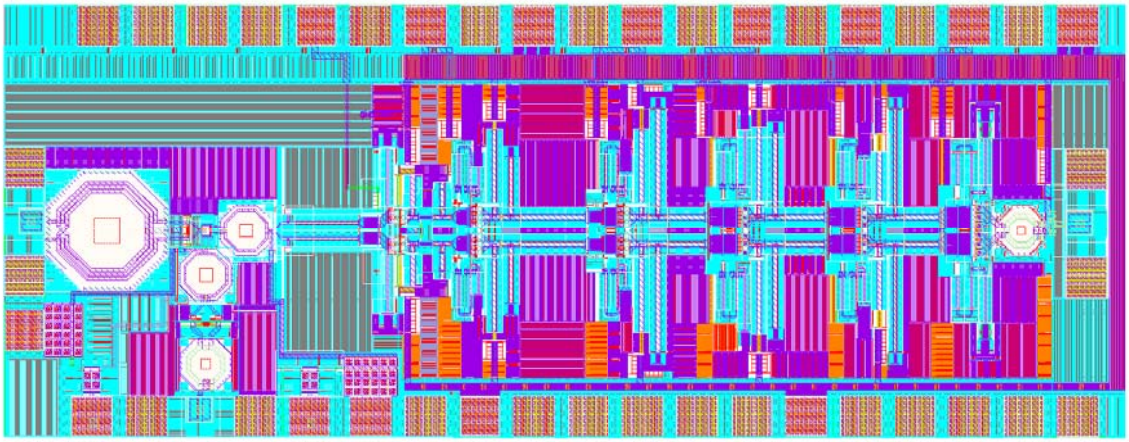


Figure 2.3-2 Layout of the mmW mixer and the PA, including PADs

2.3.2. Results

Figure 2.3-3 shows the input matching at the PA differential input, when a 50 Ω differential port is connected. It is observed that with the designed MN the input matching is better than -10 dB from 62.83 to 96.52 GHz.

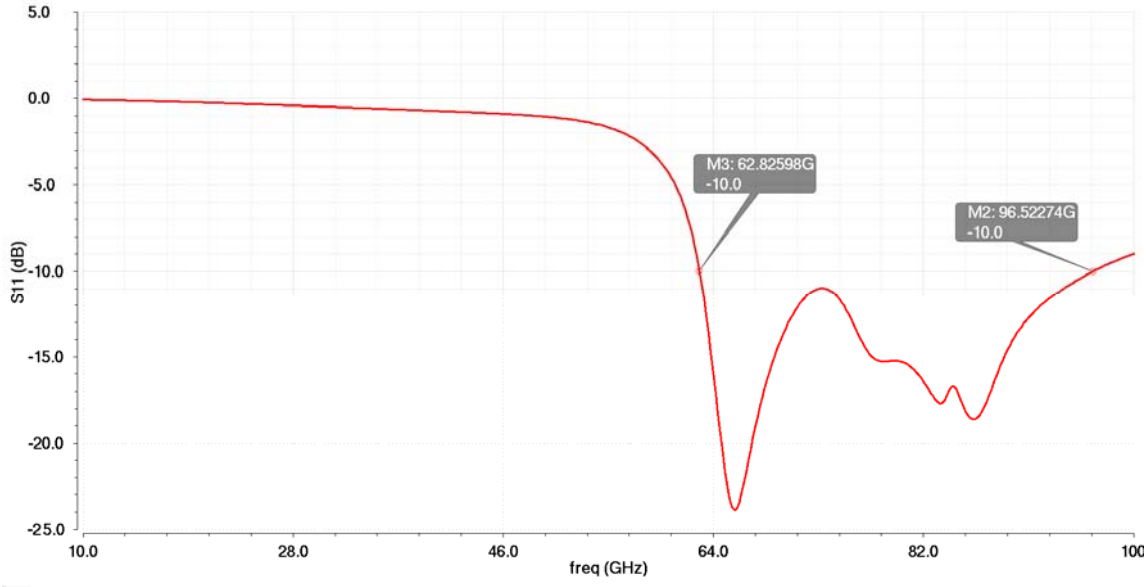


Figure 2.3-3 Input matching at the PA differential input

In order to check the behaviour of this circuit, the gain compression curves have been simulated at 2 frequencies: 72 GHz and 82 GHz, and are plotted in Figure 2.3-4 and Figure 2.3-5. It can be seen that the conversion gain is around 22-23 dB, which agrees well with the PA gain and the mixer conversion loss. As far as the output power compression is concerned, values of around 19 dBm are achieved. It can be seen that there is a small degradation when compared to the PA P1dB, but the specification is still fulfilled.

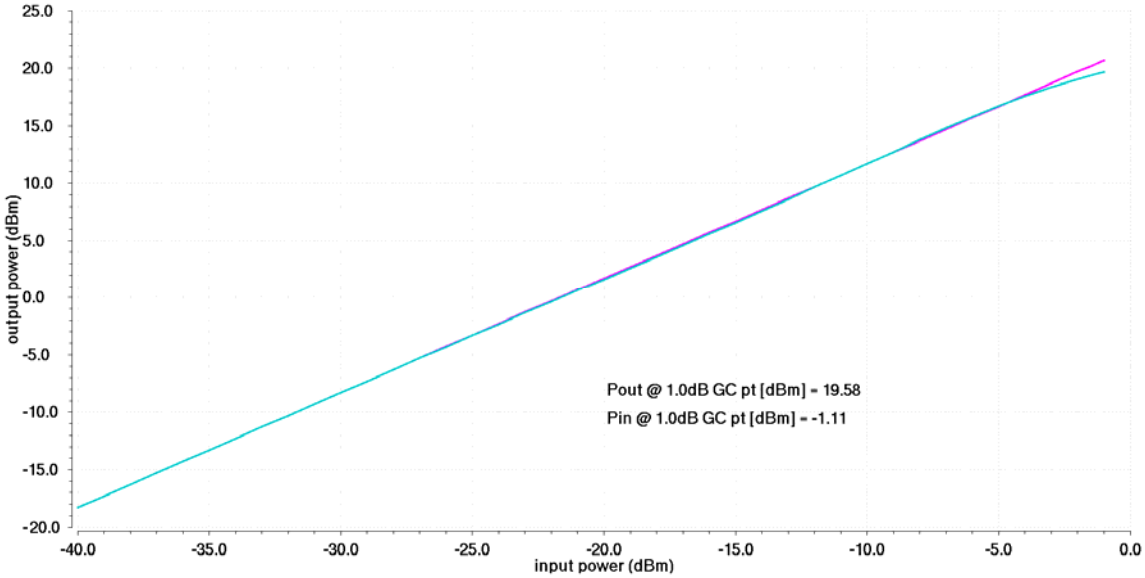


Figure 2.3-4 Gain compression curve of the mmW mixer + PA at 72 GHz

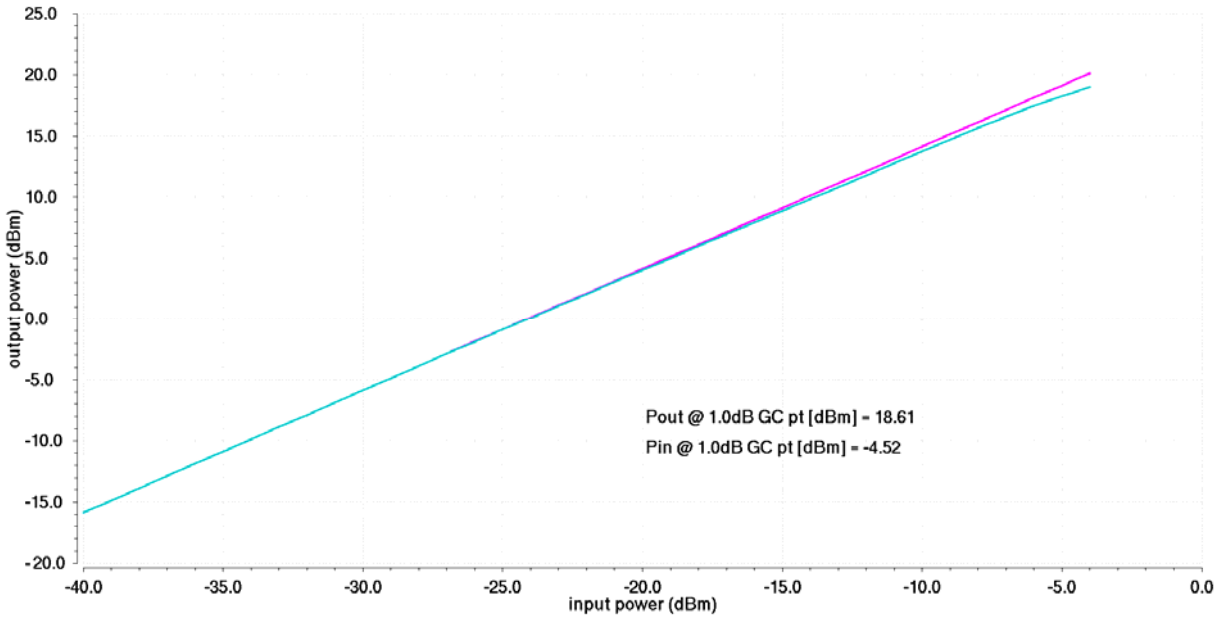


Figure 2.3-5 Gain compression curve of the mmW mixer + PA at 82 GHz

The main simulation results are summarized in Table 2.3-1 and compared to the specifications of the block.

Parameter	Min. Value	Max. Value	Spec. in D1.2.2	Comments
Conversion Gain	21.69 dB	23.13 dB	20 dB	Variable attenuator is planned to be included in the next redesign
Output P1dB	18.61 dBm	19.58 dBm	18 dBm	Spec. fulfilled
DC power	-	558 mW	-	
Area	-	1.627 mm²	-	

Table 2.3-1 Summary of simulation results for the mmW Tx module

2.4 Updated IF Mixer results

2.4.1. Circuit description

Figure 2.4-1 shows the schematic of the baseband to IF up-converter mixer. It consists of a Gilbert Cell followed by an output stage with cascode configuration, which are coupled using a centre-taped integrated transformer.

As it is shown, the differential input includes a resistive matching network, which can be varied between two different configurations depending on the external balun connected at the input. There is also a LO buffer to drive the mixer with enough power, which is connected to the LO input using a balun for on-wafer testing purposes. This port is matched to 50 Ω using a RC matching network. A similar procedure is used for the IF port, which is also single-ended for measurement purposes.

Additionally, a linearization loop is placed to increase the output power of the block, as it can be observed in the lower part of the schematic. When enabled, it modifies the bias voltage of the output gain stage depending on the mixer output power, thus increasing its linearity.

The selected VDD is 1.2 V for the mixer core and output stage and 1.5 V for the LO buffer. As for the linearization loop, its VDD can be varied to compensate for temperature and process variations as well as to adjust the gain of the loop.

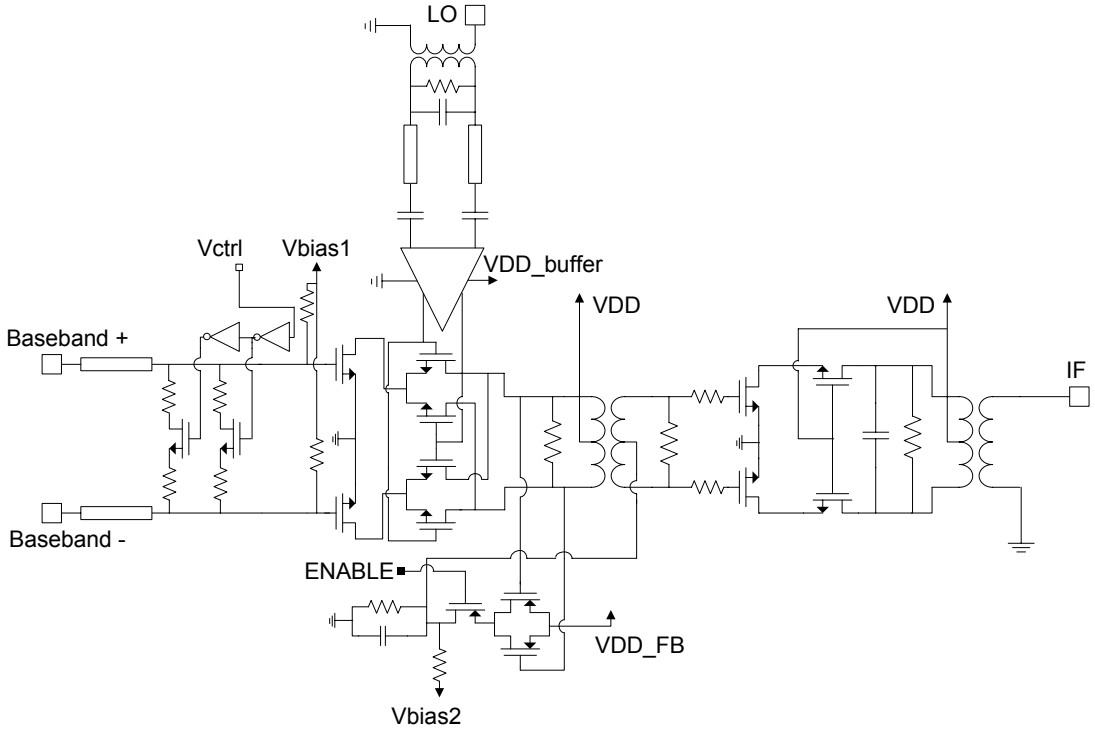


Figure 2.4-1 Schematic of the IF up-converter mixer

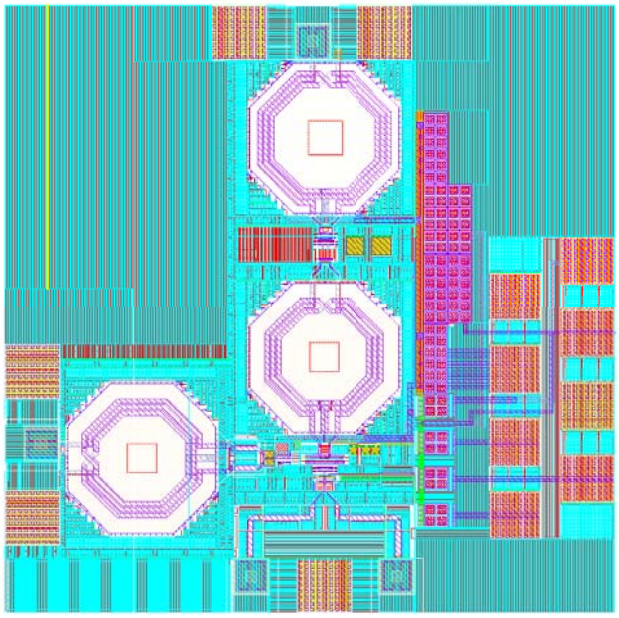


Figure 2.4-2 Layout of the IF up-converter mixer, including PADs

The layout of this block can be observed in Figure 2.4-2, which occupies an area of 0.7 mm².

2.4.2. Results

Figure 2.4-3 to Figure 2.4-5 show the matching at the different ports of the IF up-converter mixer. As it can be observed, the S11 parameter at the baseband input port is better than -10 dB up to 1.54 GHz, being -13 dB at 1 GHz. This wide bandwidth behaviour is achieved due to the resistive matching network. As for the LO port, the reflection coefficient is better than -10 dB from 15.88 to 22.15 GHz, which means that it is well matched for the LO frequencies of 17.5 and 19.5 GHz. The output matching of the mixer, shown in the S33 plot, is better than -10 dB from 16.46 to 21.08 GHz, which covers the range of output bandwidth of the different channels.

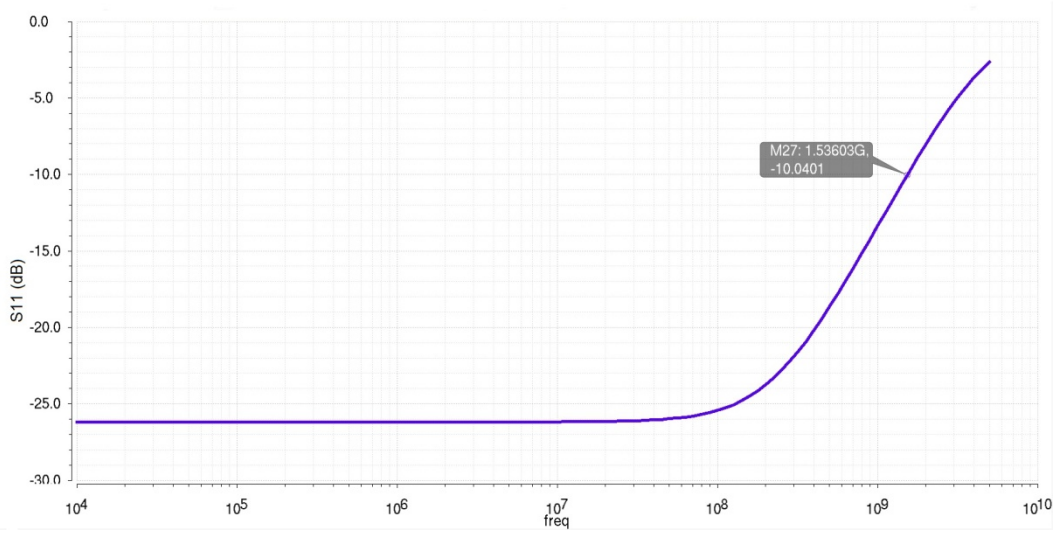


Figure 2.4-3 Input matching at the input port of the IF mixer

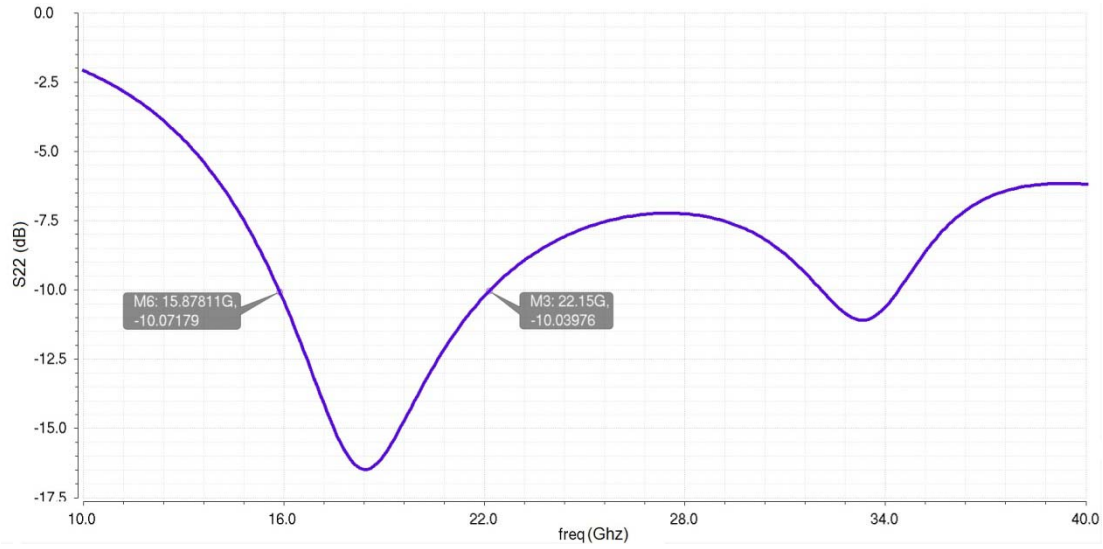


Figure 2.4-4 Input matching at the LO port of the IF mixer

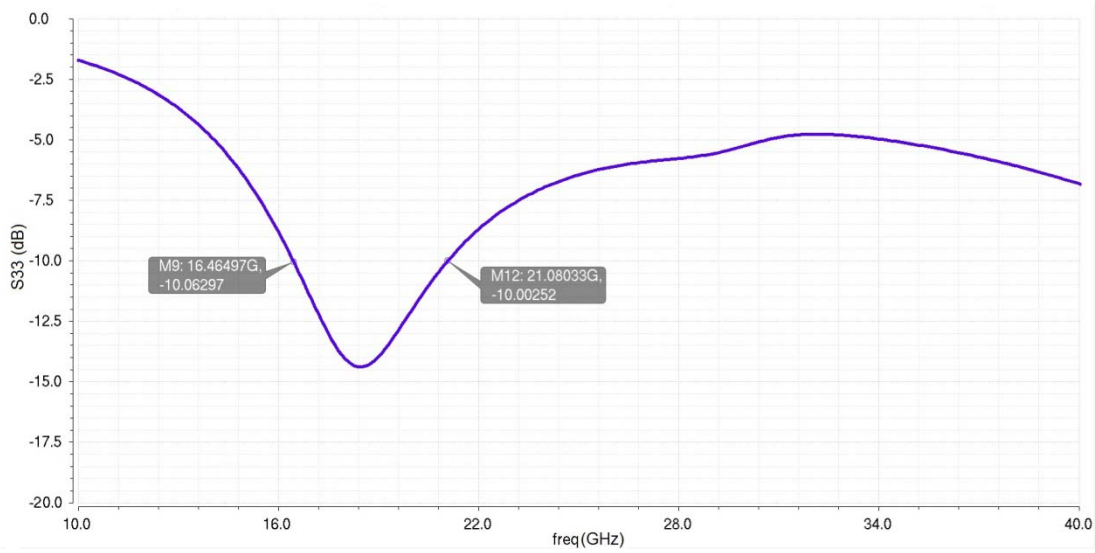


Figure 2.4-5 Output matching of the IF mixer

The behaviour of the linearization loop at the LO frequencies of 17.5 and 19.5 GHz can be derived from Figure 2.4-6 and Figure 2.4-7 respectively. It is observed that when the input power is higher than about -15 dBm, the loop increases the gain, thus making the compression point bigger.

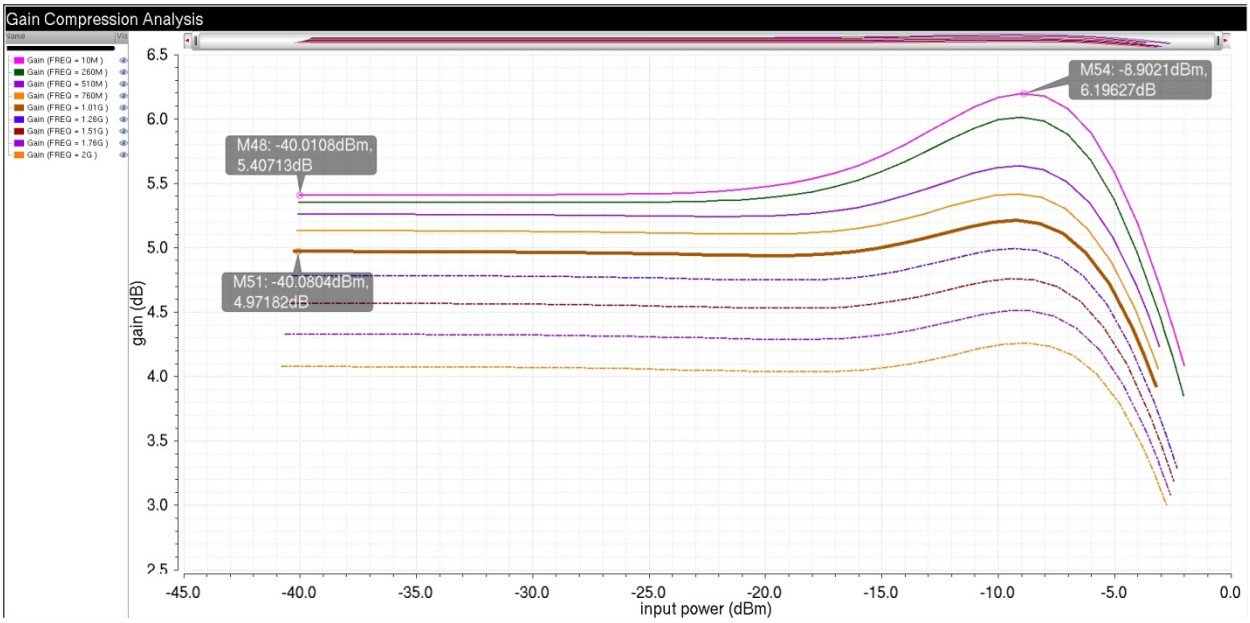


Figure 2.4-6 Power gain as a function of the input power for LO freq of 17.5 GHz

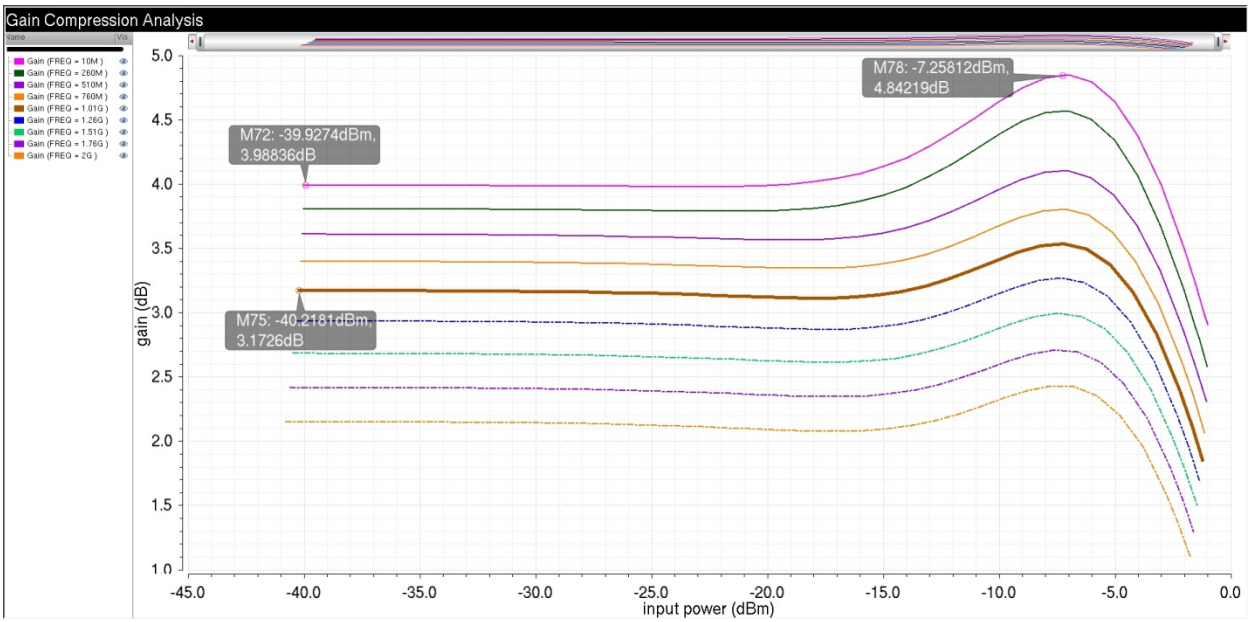


Figure 2.4-7 Power gain as a function of the input power for LO freq of 19.5 GHz

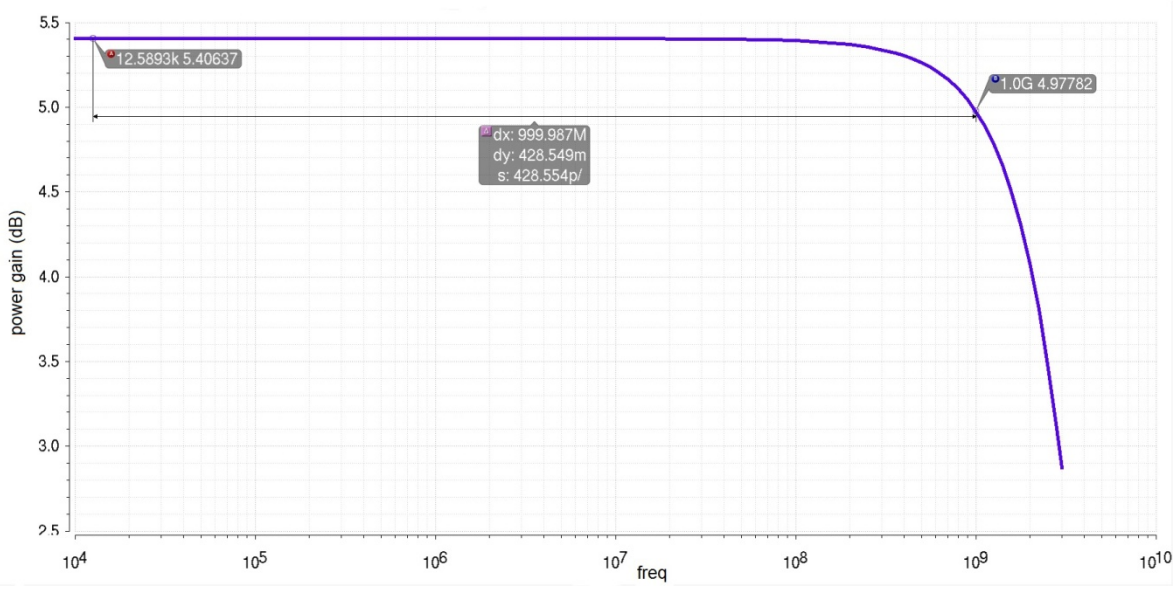


Figure 2.4-8 Power gain as a function of input frequency for LO freq of 17.5 GHz

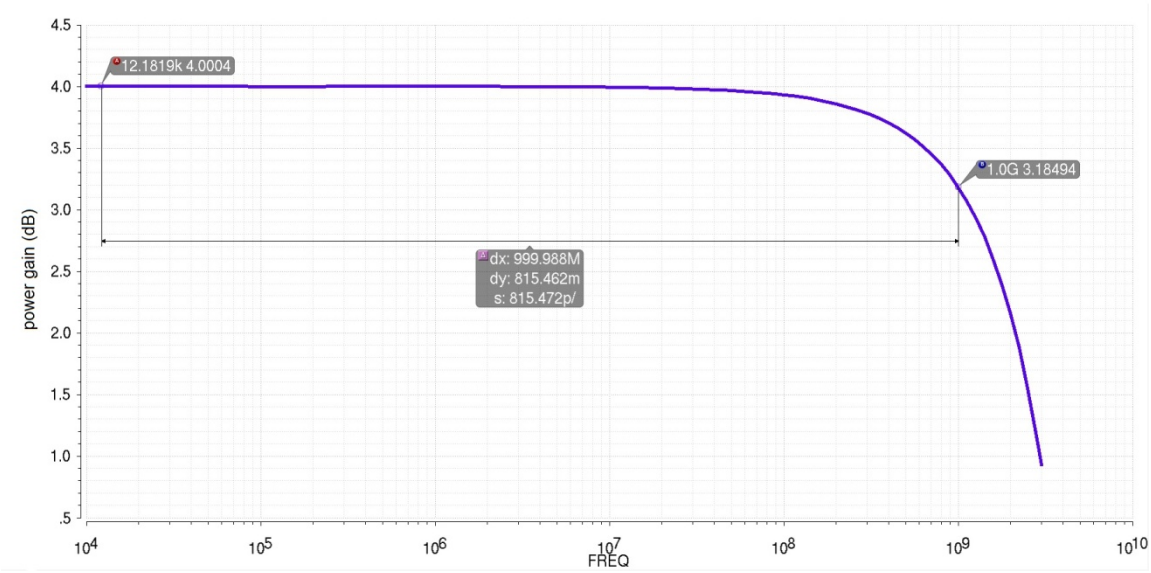


Figure 2.4-9 Power gain as a function of input frequency for LO freq of 19.5 GHz

Figure 2.4-8 and Figure 2.4-9 show the power gain as a function of the input baseband frequency for LO frequencies of 17.5 and 19.5 GHz respectively. A maximum value of 5.4 dB is achieved at the 17.5 GHz band, with a decay of less than 0.43 dB at 1 GHz. The gain decreases 3 dB at about 3 GHz, resulting in an output 3-dB bandwidth of around 6 GHz. With regard to the 19.5 GHz channel, the maximum power gain is 4 dB, with a decay of 0.8 dB at 1 GHz. In this case the gain decreases 3 dB at 2 GHz, giving an output 3-dB bandwidth of 4 GHz.

Regarding the 1 dB compression point, Figure 2.4-10 and Figure 2.4-11 show the output-referred P1dB for both channels as a function of the input frequency. A maximum value of 1.85 dBm is observed at the 17.5GHz channel, with a minimum value of 0.67 dBm at 1 GHz input. Similarly, the maximum value is around 1.85 dBm for the 19.5 GHz channel with a minimum value of 0.41 dBm at 1 GHz input.

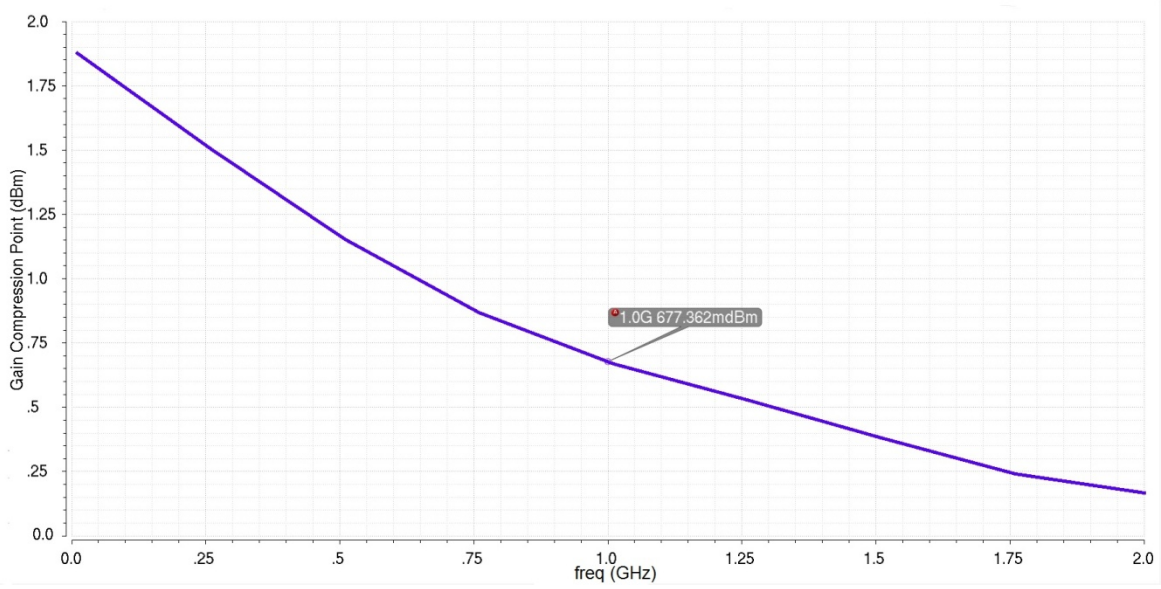


Figure 2.4-10 Output 1dB compression point as a function of frequency for LO freq of 17.5 GHz

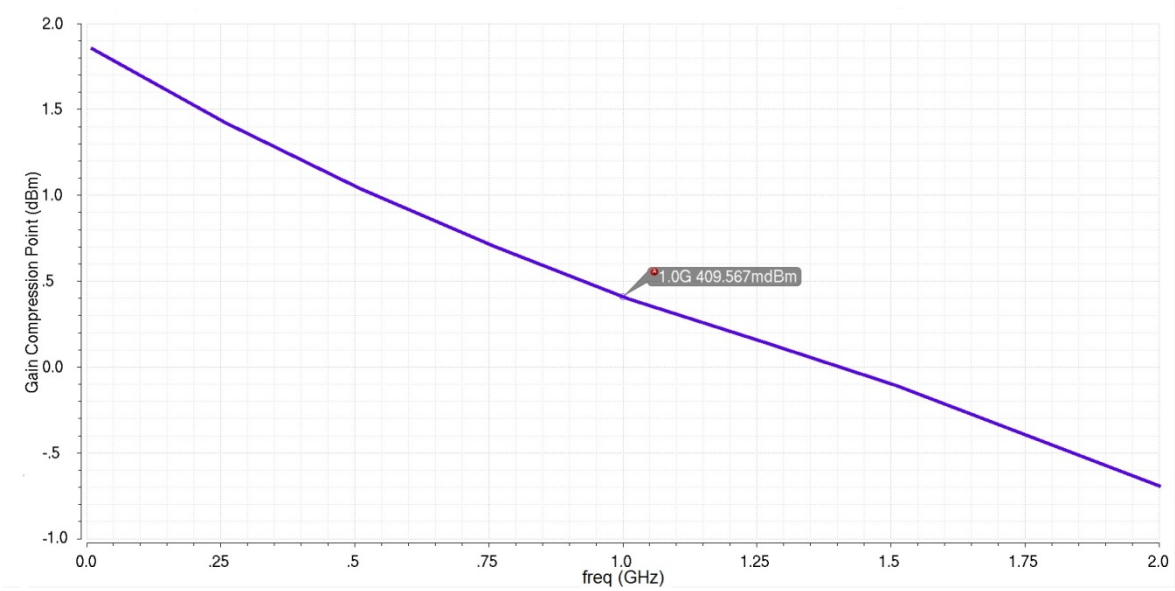


Figure 2.4-11 1dB compression point as a function of frequency for LO freq of 19.5 GHz

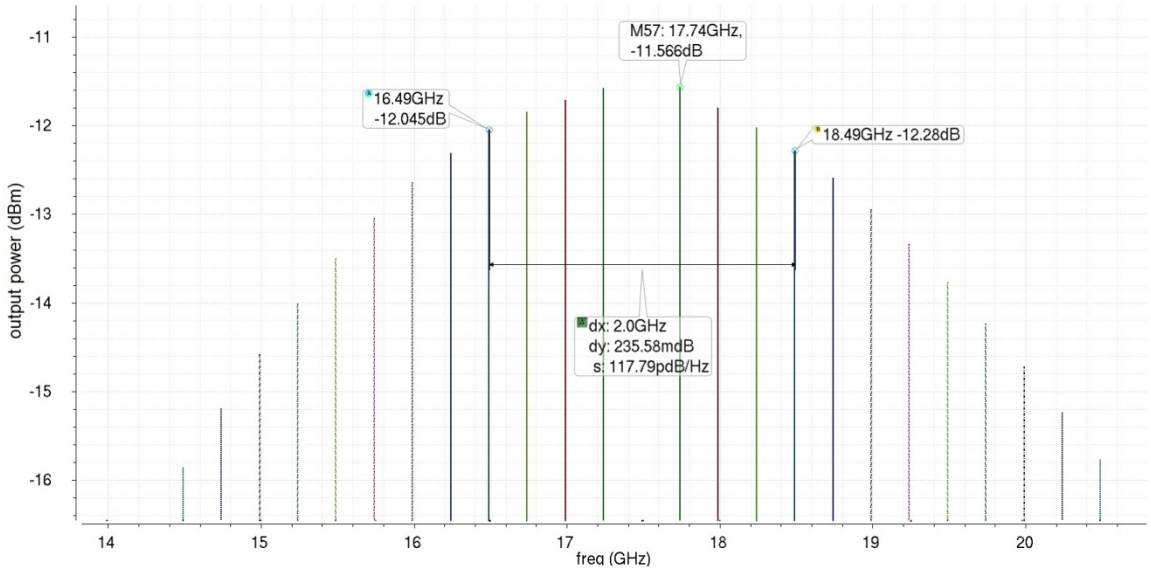


Figure 2.4-12 Output power spectrum for the 17.5 GHz channel

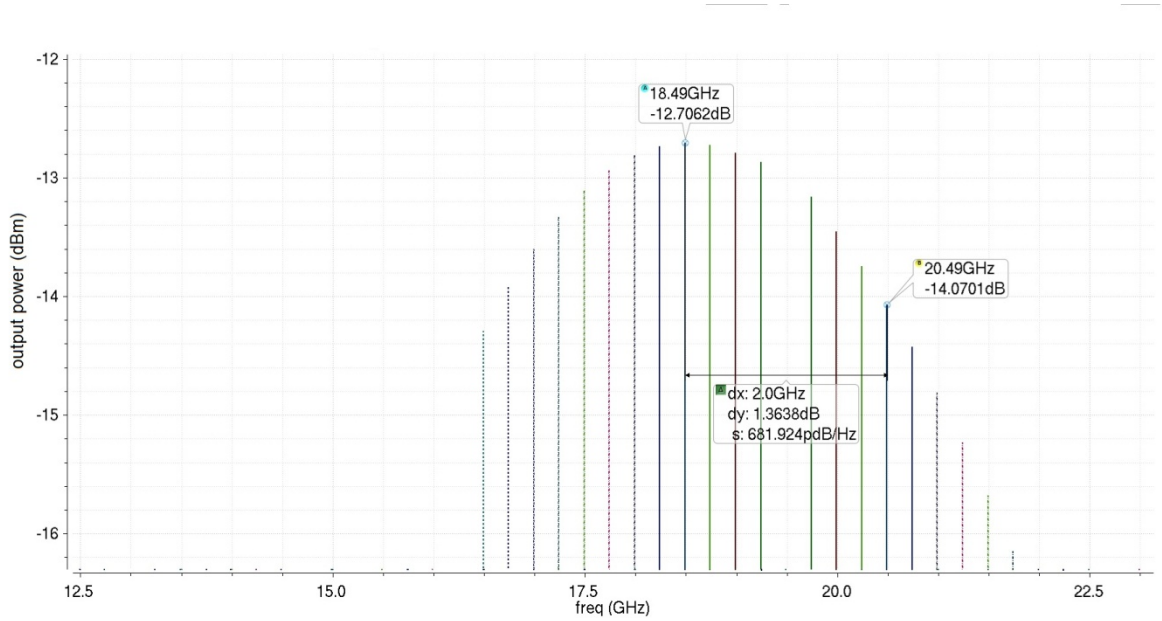


Figure 2.4-13 Output power spectrum for the 19.5 GHz channel

The output power spectrum is shown in Figure 2.4-12 and Figure 2.4-13, for an input power of -17 dBm. A flatness of 0.7 dB can be observed at the 17.5 GHz channel and of 1.37 dB at the 19.5 GHz channel. The LO signal is 27 dBc below the output signal of the mixer for both bands, as shown in Figure 2.4-14 and Figure 2.4-15.

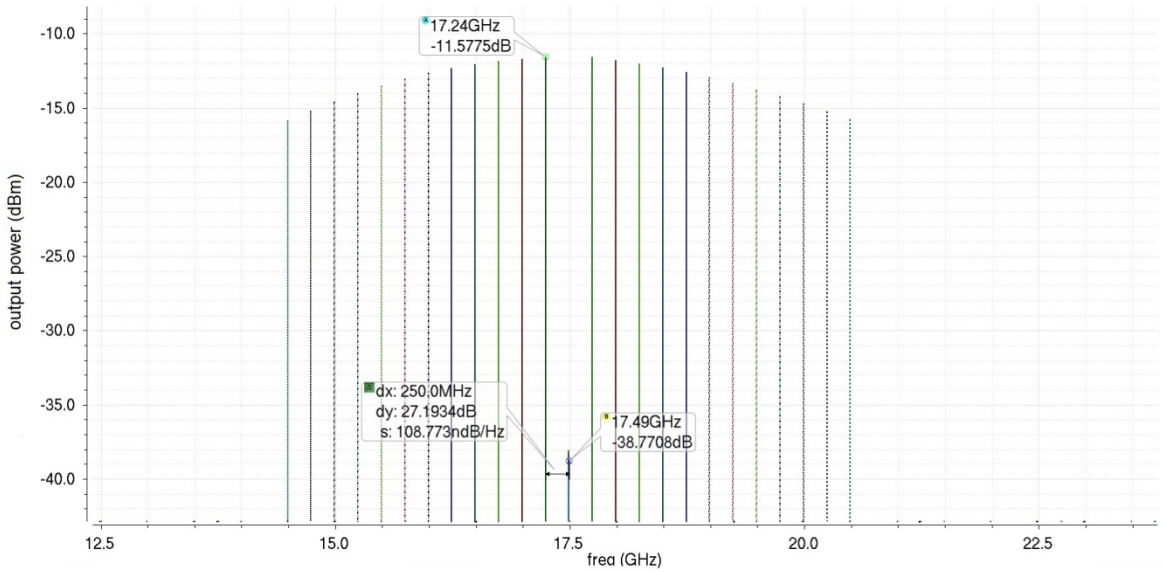


Figure 2.4-14 Output spectrum showing the LO signal for the 17.5 GHz channel

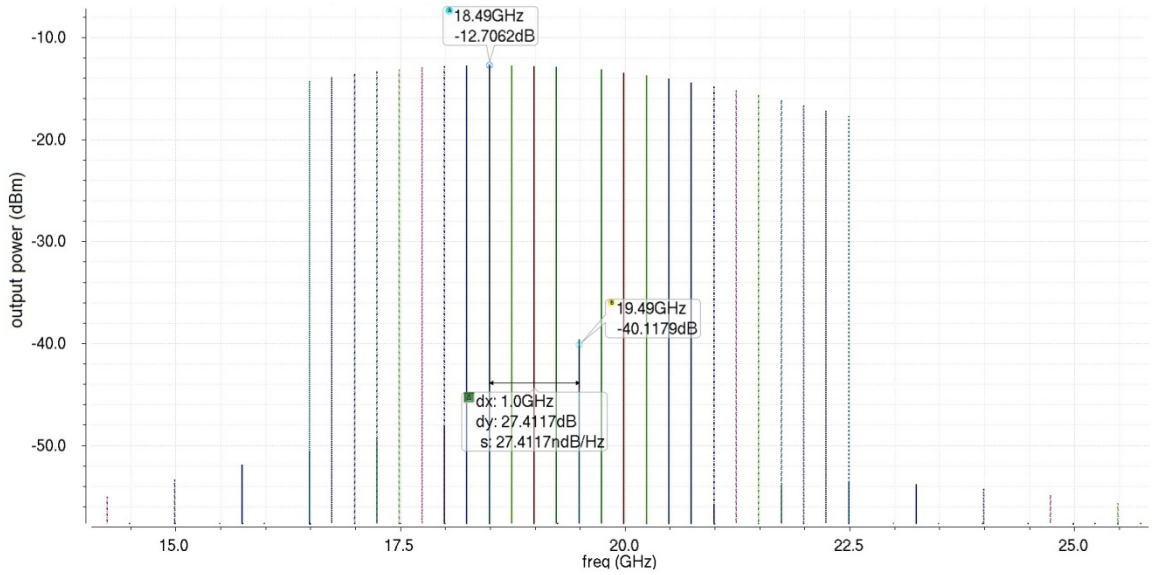


Figure 2.4-15 Output spectrum showing the LO signal for the 19.5 GHz channel

The noise figure of this block is shown in Figure 2.4-16 and Figure 2.4-17 for both channels. It has a minimum value of 6.89 dB at the 17.5 GHz channel and of 7.35 dB at the 19.5 GHz channel. A big increase is observed close to DC due to effects such as flicker noise. The impact of flicker noise is expected to be small due to the employed modulation scheme where signal power close to DC is minimized.

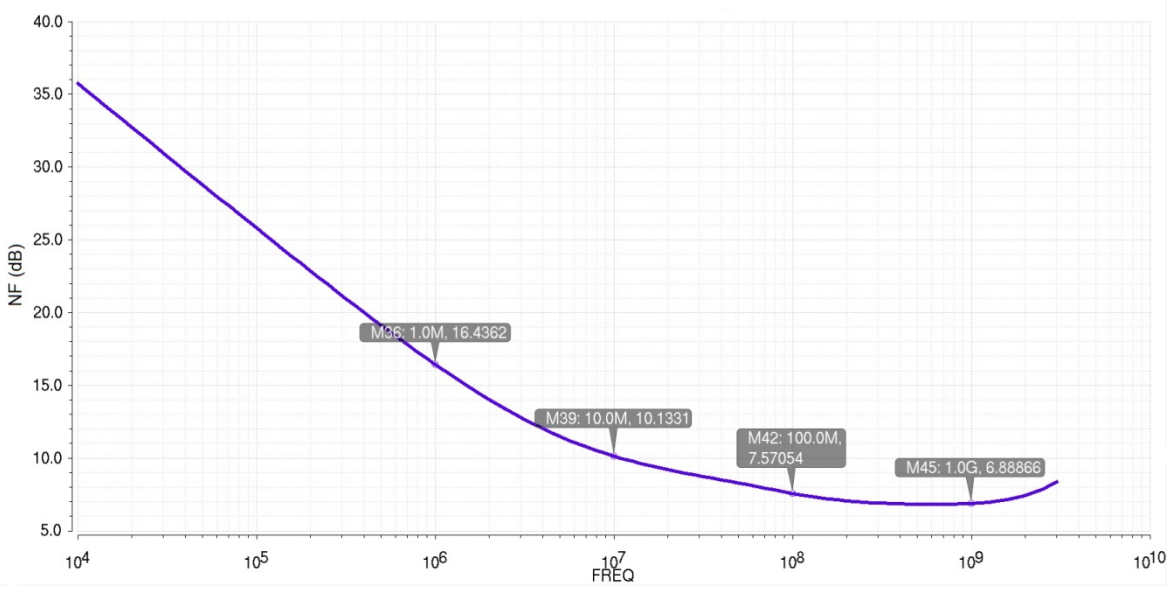


Figure 2.4-16 Noise figure at the 17.5 GHz channel as a function of the input frequency

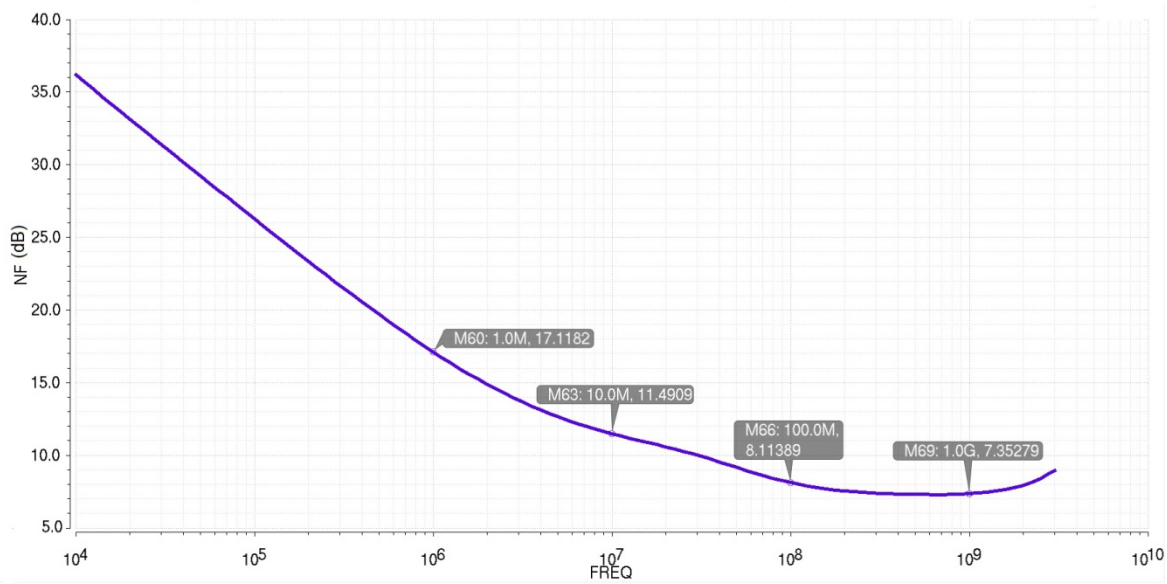


Figure 2.4-17 Noise figure at the 19.5 GHz channel as a function of the input frequency

The main given simulation results are summarized in Table 2.4-1 and compared to the specifications of the IF up-conversion mixer.

Parameter	Min. Value	Max. Value	Spec. in D1.2.2	Comments
Conversion Gain	3.18 dB	5.4 dB	3 dB	Spec. fulfilled
Output 3dB bandwidth	6 GHz	-	6 GHz	Spec. fulfilled
LO frequency	17.5 GHz	19.5 GHz	17.5 / 19.5 GHz	Spec. fulfilled
Input matching at BB port	-26 dB	-13 dB	-10 dB	Spec. fulfilled
Input matching at LO port	-16.5 dB	<-10 dB	-10 dB	Spec. fulfilled
Output matching at IF port	-14.5 dB	-10 dB	- 10 dB	Spec. fulfilled
Output P1dB	0.41 dBm	1.85 dBm	0 dBm	Spec. fulfilled
LO leakage at IF port	-40.1 dB	-38.8 dB	-36 dB	Spec. fulfilled
Noise Figure	6.89 dB	-	10 dB	Spec. fulfilled; NF increase close to DC is taken into account in the baseband signal generation.
DC power	-	50 mW	-	
Area	-	0.7 mm²	-	

Table 2.4-1 Summary of simulation results for the IF up-conversion mixer

2.5 Tx IQ Modulator results

2.5.1. Circuit description

The block diagram of the IQ modulator circuit is shown in Figure 2.5-1. It consists of two IF mixers like the one described in Section 2.4, whose output currents are added using a balun. A single LO signal is used, which is fed into a poly-phase filter to provide 90º phase difference at the in-phase and quadrature mixers. Integrated baluns are used at both LO and IF ports for on-wafer testing purposes.

Special care is placed on the layout symmetry, so that no phase difference is introduced into the LO signal of the I and Q channels. The layout of this block can be observed in Figure 2.5-2, with an area of 1.073 mm², including all the PADs.

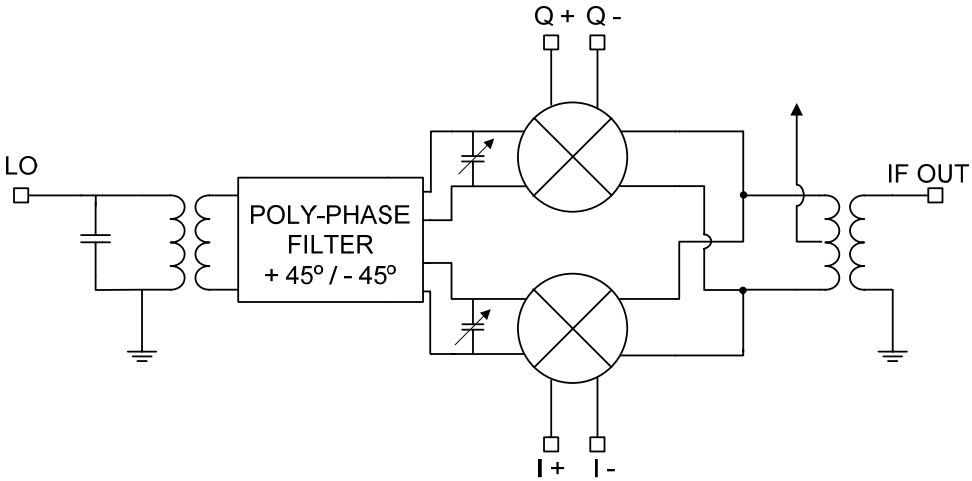


Figure 2.5-1 Block diagram of the IQ modulator

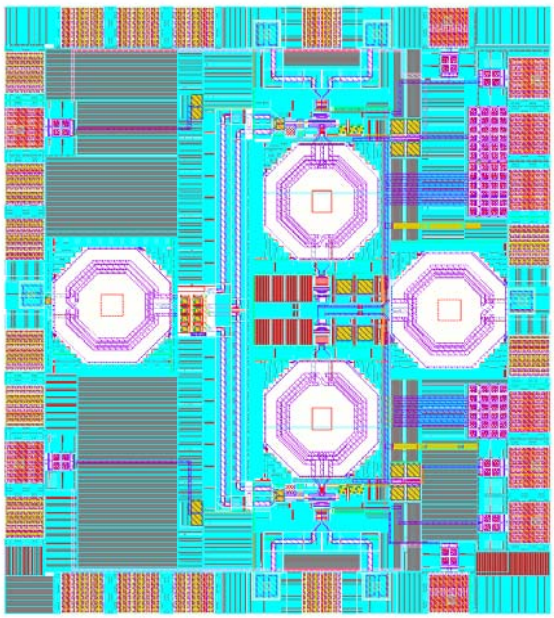


Figure 2.5-2 Layout of the IQ modulator, including PADs

2.5.2. Results

Figure 2.5-3 to Figure 2.5-5 show the matching at the different ports of the IQ modulator. As it is observed, the input matching at the I and Q ports is better than -10 dB up to 1.44 GHz, which is very similar to that reported in Section 2.4.2. The S33 parameter at the LO input is -13.6 dB at 17.5 GHz and -12.3 dB at 19.5 GHz. As for the output of the modulator, it is well matched to 50 Ω in the band of interest as well, with S44 equal to -9.24 dB at 16.5 GHz and -15.26 dB at 20.5 GHz.

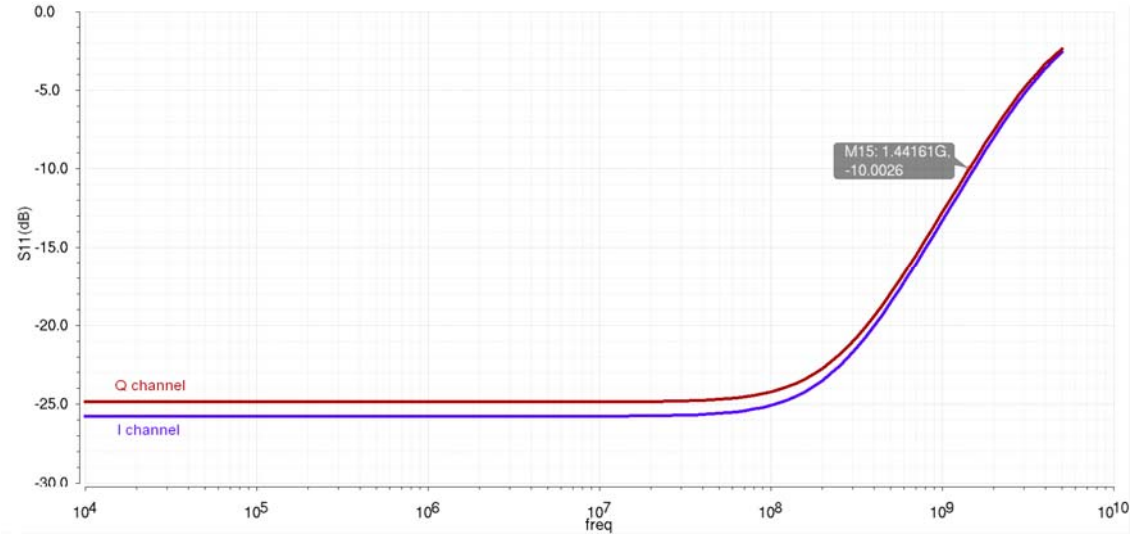


Figure 2.5-3 Input matching at the I and Q ports of the IQ modulator

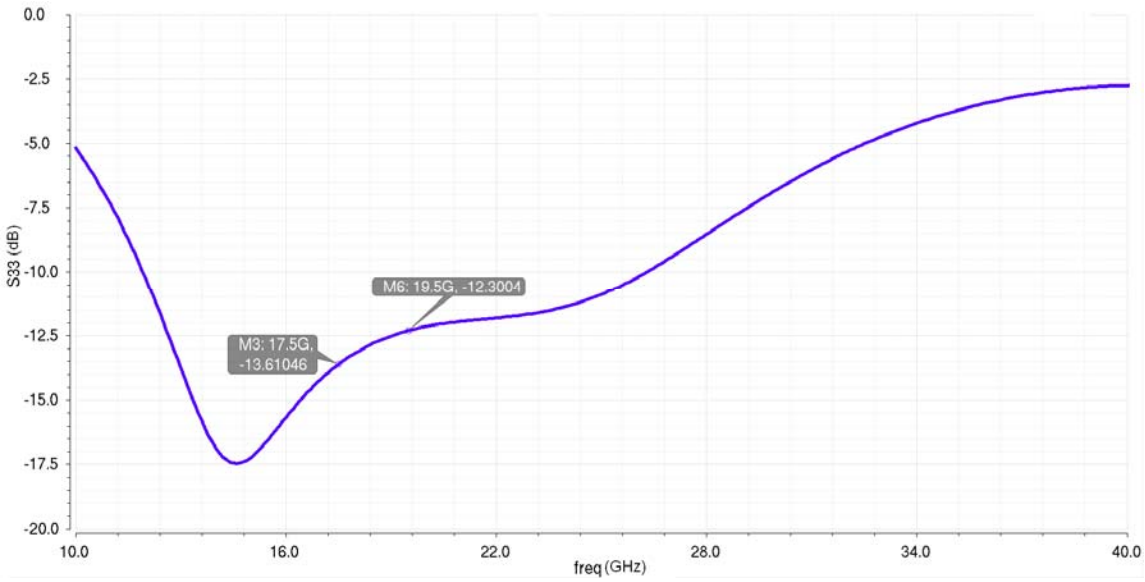


Figure 2.5-4 Input matching at the LO port of the IQ modulator

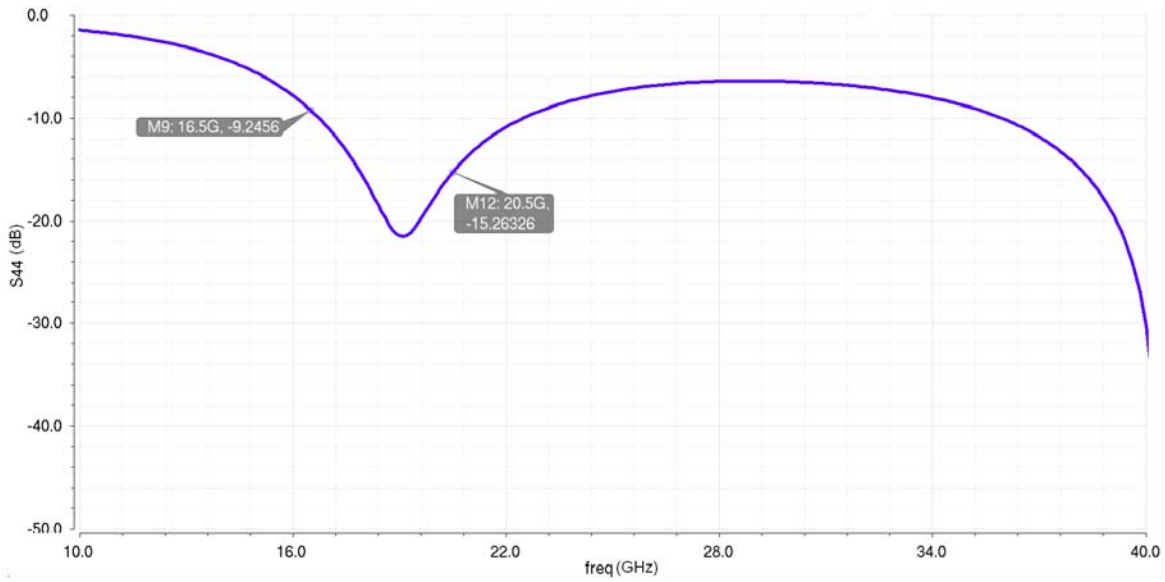


Figure 2.5-5 Output matching of the IQ modulator

Figure 2.5-6 and Figure 2.5-7 show the output power spectrum when the same signal is introduced in the I and Q inputs for the 17.5 and 19.5 GHz bands, whereas the behaviour when the signal is introduced with 90º phase difference can be seen in Figure 2.5-8 and Figure 2.5-9. It is observed that the gain flatness is very similar to that reported for the case of a single IF mixer. The rejection of the LO signal can be extracted as well, which is more than 23 dBc below the power of the output signal.

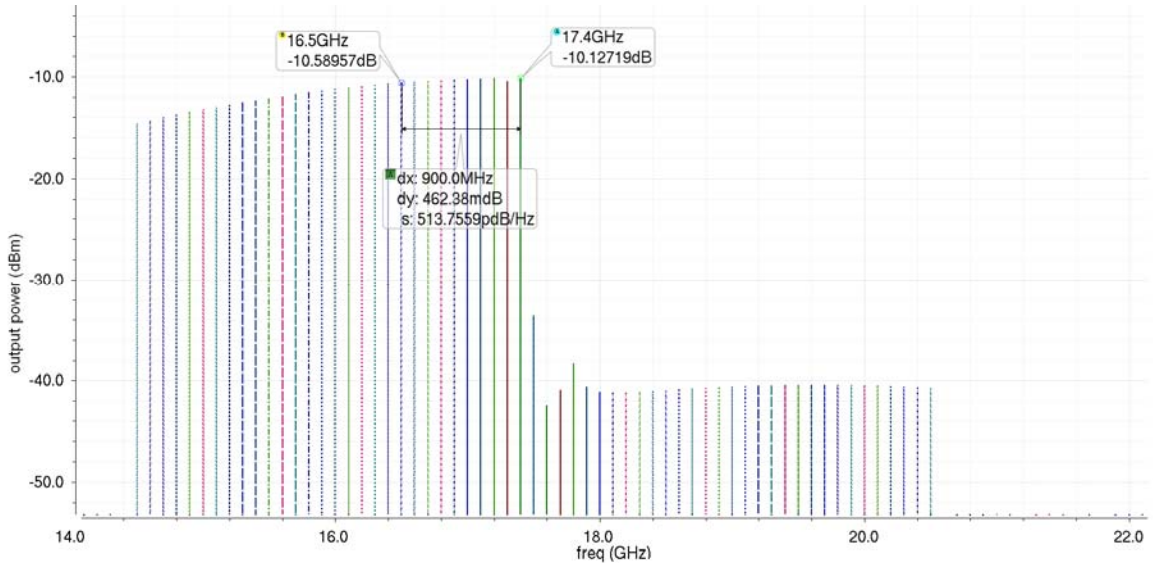


Figure 2.5-6 Output spectrum when the same signal is introduced in I and Q, at 17.5 GHz

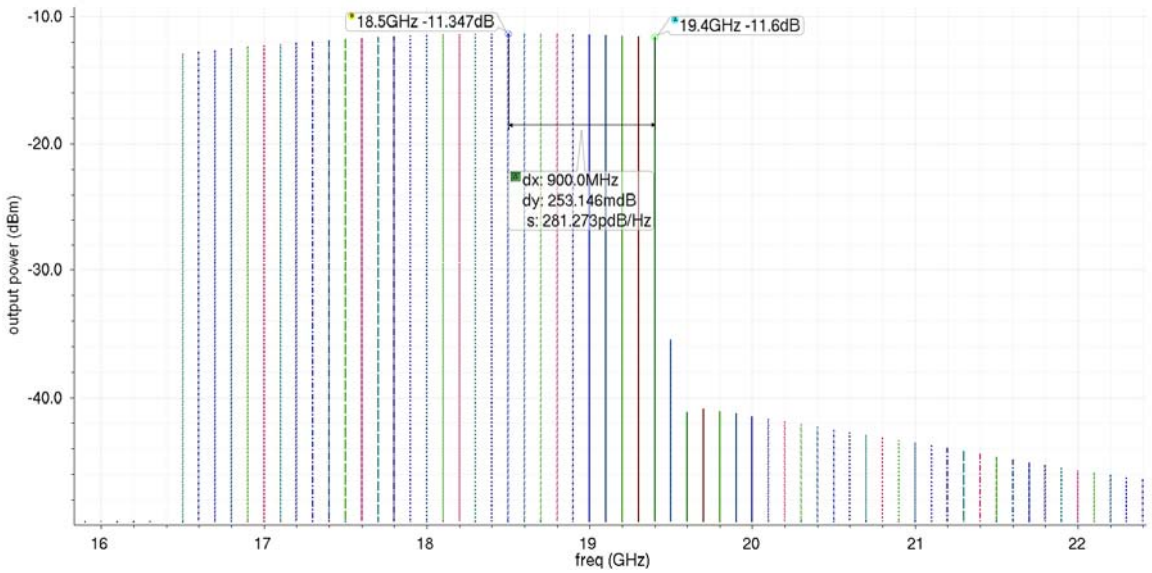


Figure 2.5-7 Output spectrum when the same signal is introduced in I and Q, at 19.5 GHz

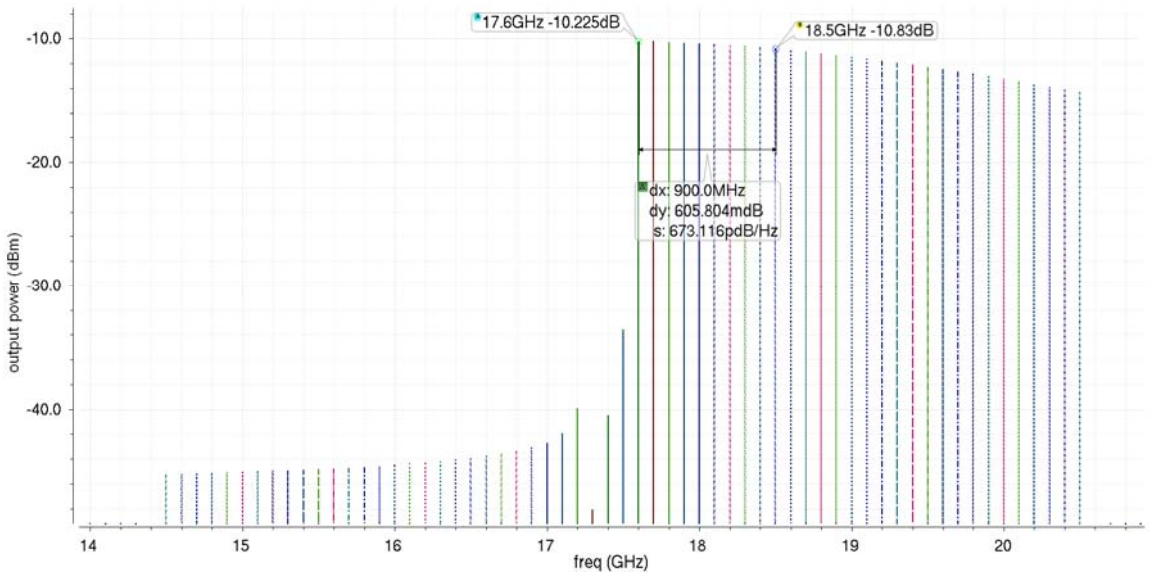


Figure 2.5-8 Output spectrum when a signal with 90º phase shift is introduced in I and Q, at 17.5GHz

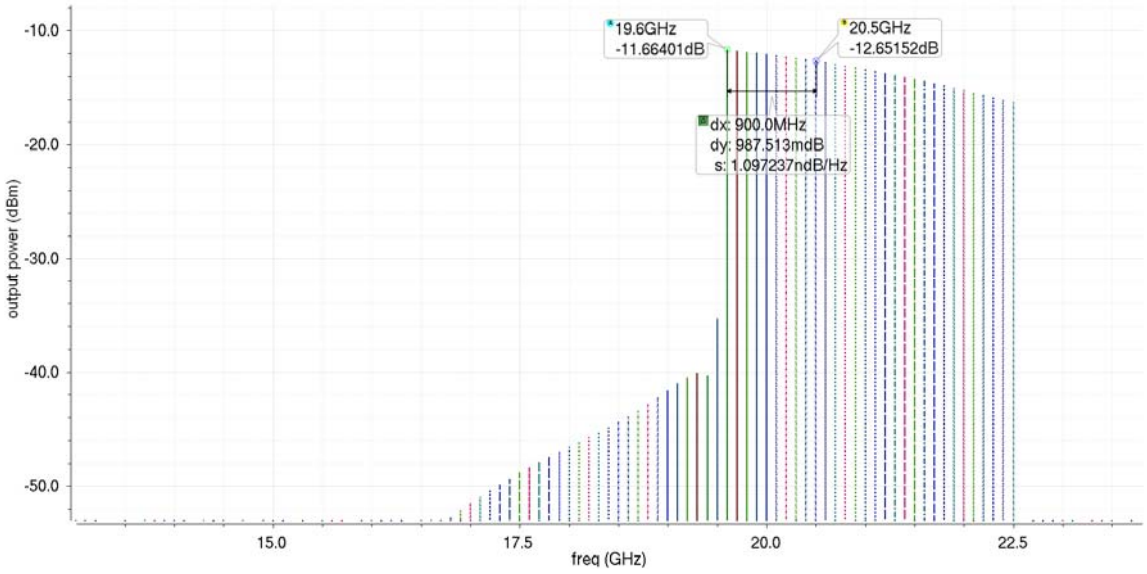


Figure 2.5-9 Output spectrum when a signal with 90º phase shift is introduced in I and Q, at 19.5GHz

Similarly, the rejection of the signal at the image frequency can be extracted from Figure 2.5-10 to Figure 2.5-13. It is observed that the image is more than 28 dBc below the power of the output signal.

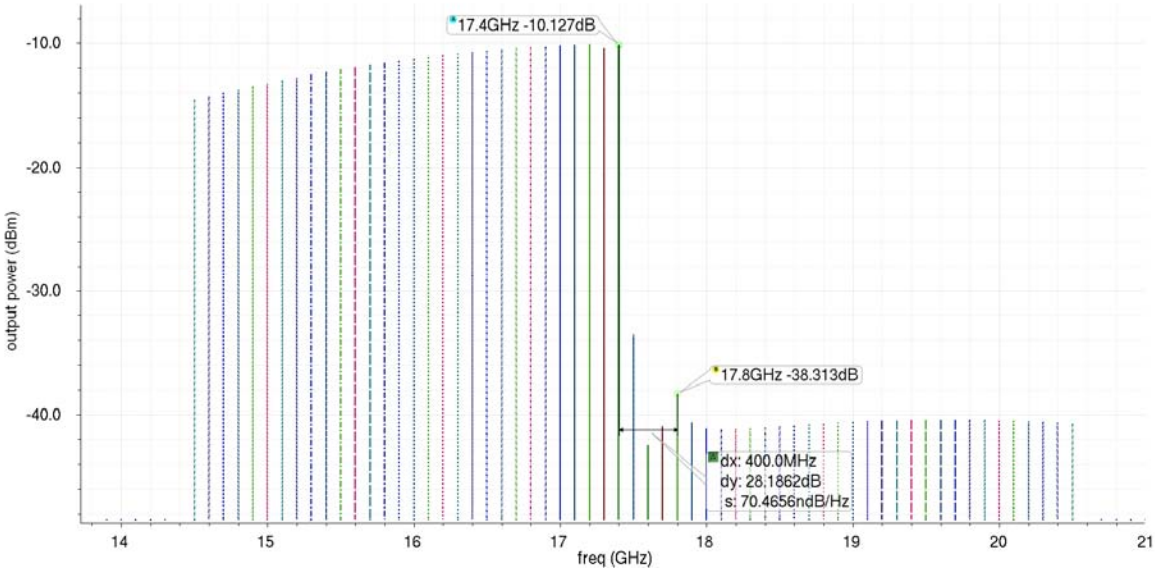


Figure 2.5-10 Output spectrum showing the image signal power when same signal is introduced in I and Q, at 17.5 GHz

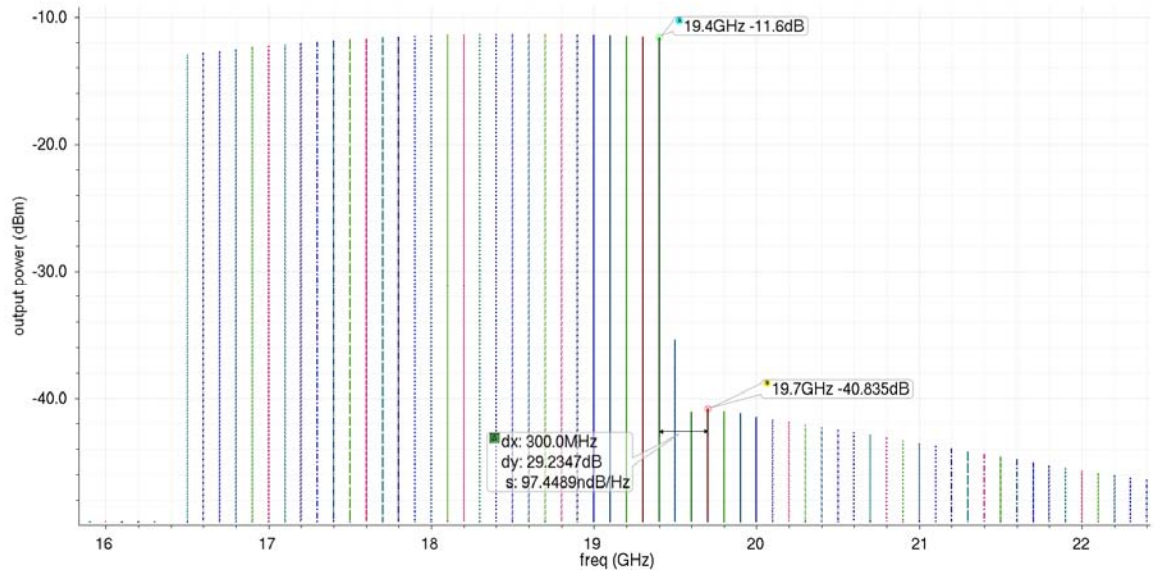


Figure 2.5-11 Output spectrum showing the image signal power when same signal is introduced in I and Q, at 19.5 GHz

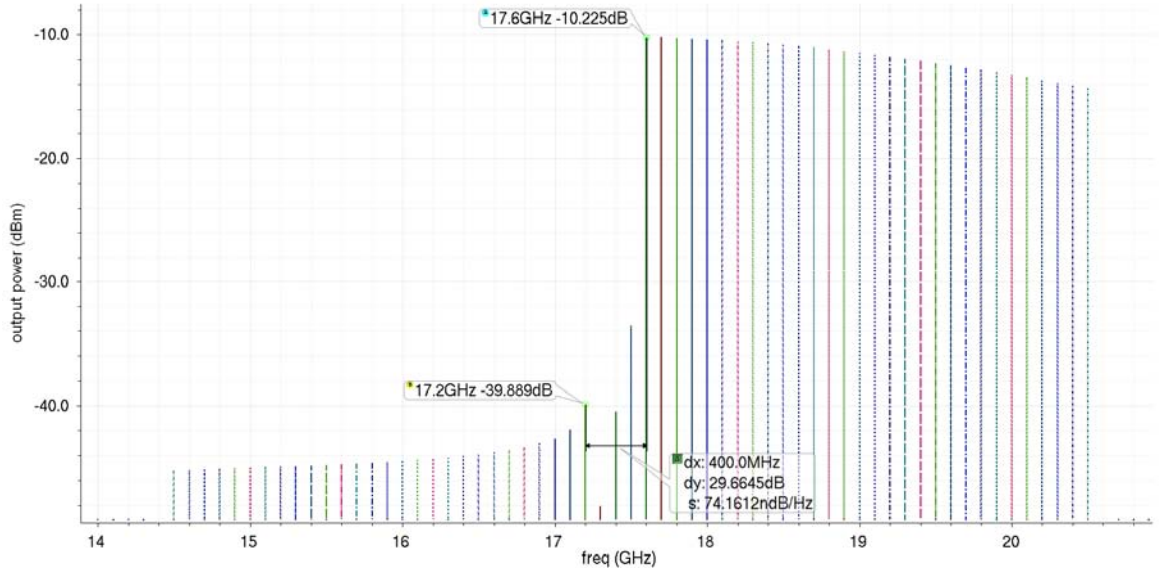


Figure 2.5-12 Output spectrum showing the image signal power when a signal with 90º phase difference is introduced in I and Q, at 17.5 GHz

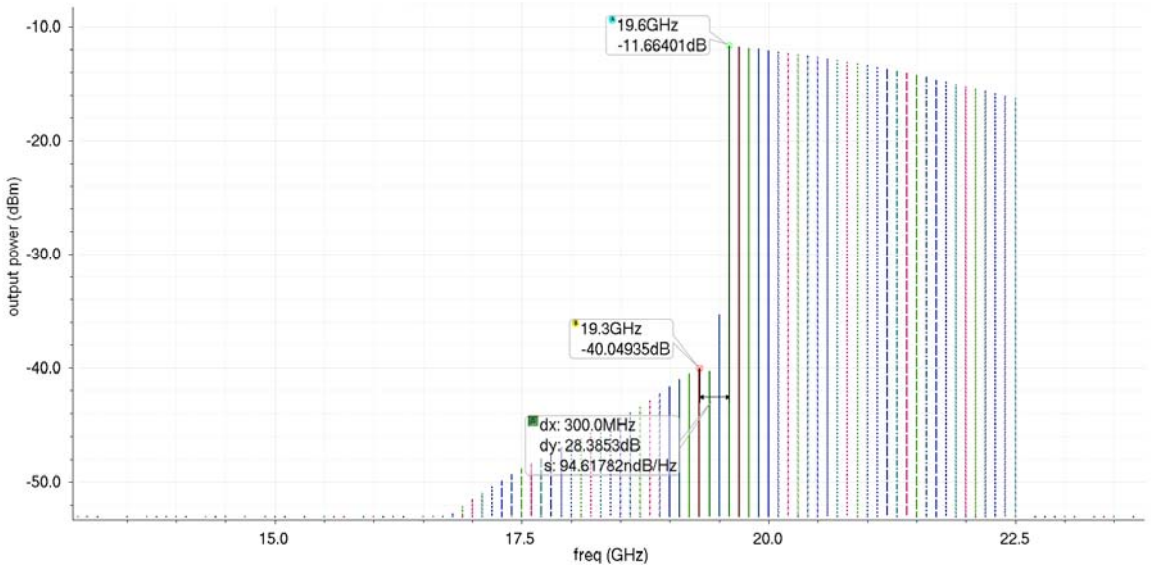


Figure 2.5-13 Output spectrum showing the image signal power when a signal with 90º phase difference is introduced in I and Q, at 19.5 GHz

In order to check the gain and compression performance of the IQ modulator compared to that of a single mixer, the power gain as a function of the input power and the input frequency is plotted in Figure 2.5-14 and Figure 2.5-15 for the 17.5 GHz channel, while the output 1 dB compression point is plotted in Figure 2.5-16 as a function of the baseband input frequency. It can be observed that the power gain is between 9.43 dB and 9.84 dB and that the loop behaves similarly to the case of the single mixer. The output P1dB is more than 5.6 dBm across the whole band. These values are higher than those of the single IF up-converter mixer, which agrees with the fact that the currents are added at the output.

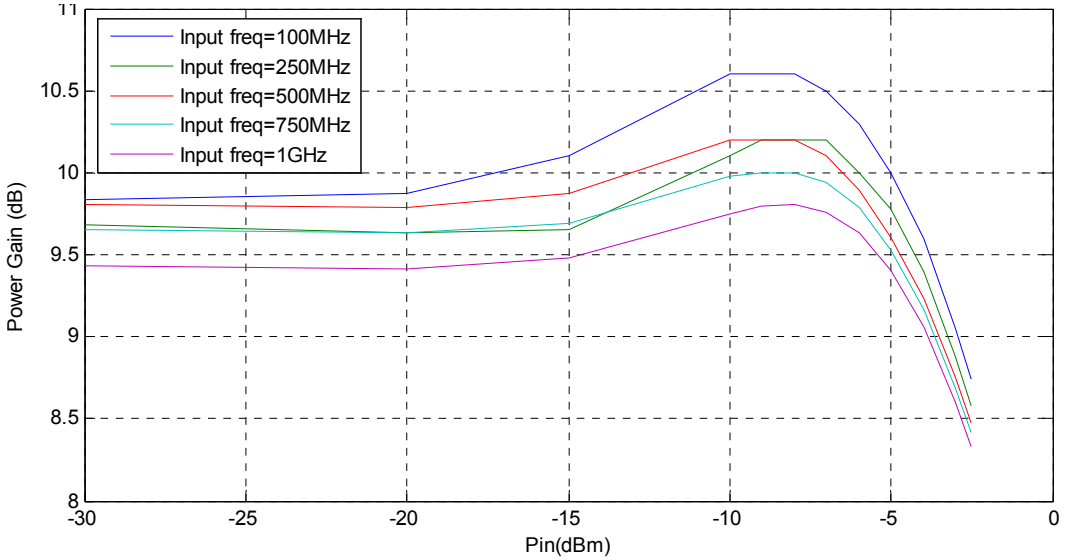


Figure 2.5-14 Power gain as a function of the input power for LO frequency of 17.5 GHz

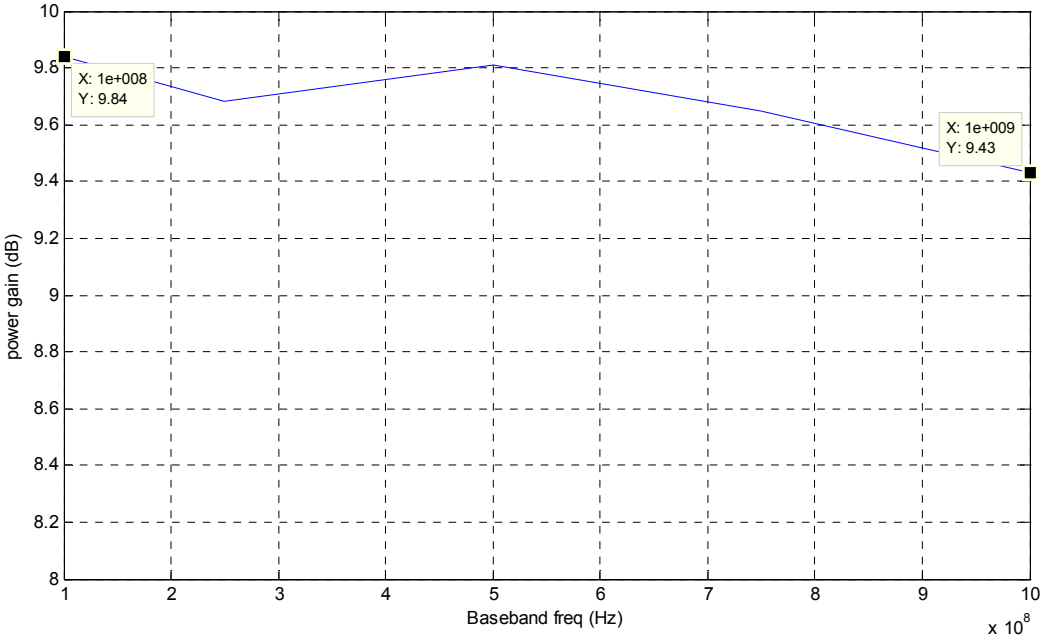


Figure 2.5-15 Power gain as a function of the baseband input frequency for LO frequency of 17.5GHz

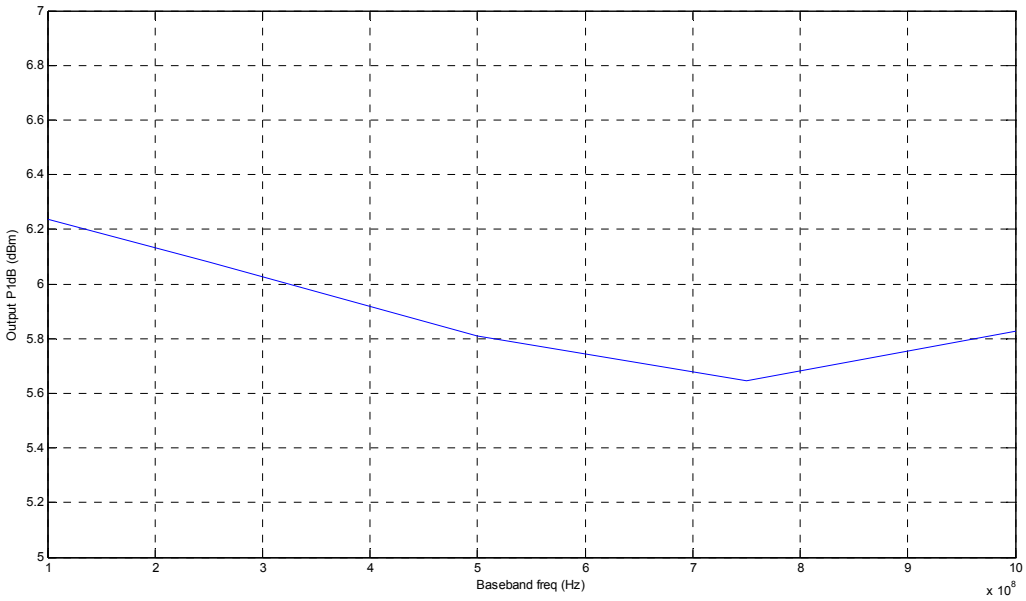


Figure 2.5-16 Output P1dB as a function of the baseband input frequency for LO frequency of 17.5GHz

The main simulation results are summarized in Table 2.5-1.

Parameter	Min. Value	Max. Value	Comments
Conversion Gain	9.43 dB	9.84 dB	Parameter updated in the table of system values
LO frequency	17.5 GHz	19.5 GHz	Spec. fulfilled
Input matching at BB port	-26 dB	-13 dB	Spec. fulfilled
Input matching at LO port	-13.61 dB	-12.3 dB	Spec. fulfilled
Output matching at IF port	-15.26 dB	-9.25 dB	Spec. fulfilled
Output P1dB	5.6 dBm	6.24 dBm	Spec. fulfilled
LO leakage at IF port	-23.84 dBc	-23.38 dBc	Spec. fulfilled
Image leakage at the IF port	-29.66 dBc	-28.19 dBc	Spec. fulfilled
DC power	-	96 mW	
Area	-	1.073 mm²	

Table 2.5-1 Summary of simulation results for the IQ modulator

3. RX SIMULATION RESULTS

3.1 Updated LNA results

3.1.1. Circuit description

The re-simulation of the LNA designed in the first production run with newest PDK delivered by ST showed performance degradation and redesign was required. In order to fulfil the system specifications a three-stage LNA is required as depicted in Figure 3.1-1. The high frequency of operation allows using transmission lines for input and output matching as well as for the loads of the transistors. The configuration of input and output matching structures is designed to guarantee broadband operation and robust ESD protection simultaneously.

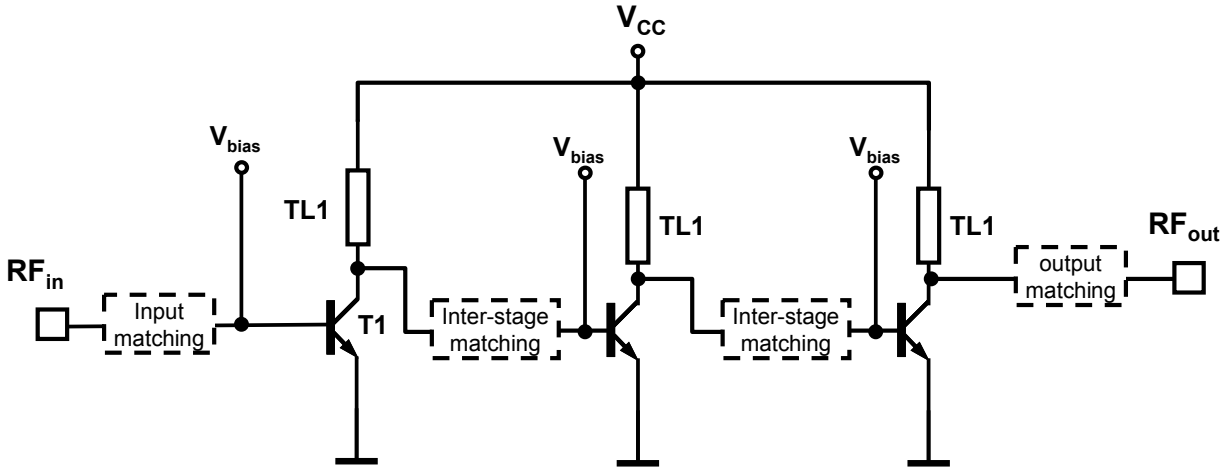


Figure 3.1-1 Schematic of the three-stage LNA

3.1.2. Results

The circuit is built and simulated in Cadence. The passives library provided by CEA has been used, which includes transmission lines and pads, as well as the ST PDK providing all other components.

Figure 3.1-2 and Figure 3.1-3 show the input and output matching of the LNA in the frequency band of interest. The input matching is a compromise between best fit for power and noise match. Broadband matching techniques were employed to achieve good match over whole E-band.

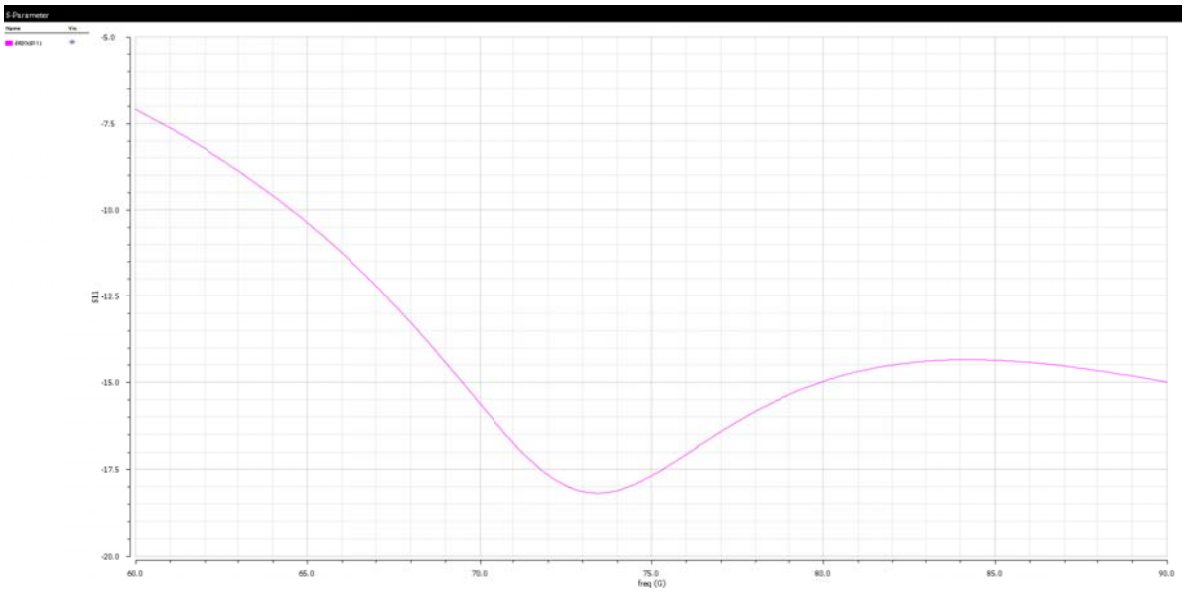


Figure 3.1-2 Simulated S11 of the LNA

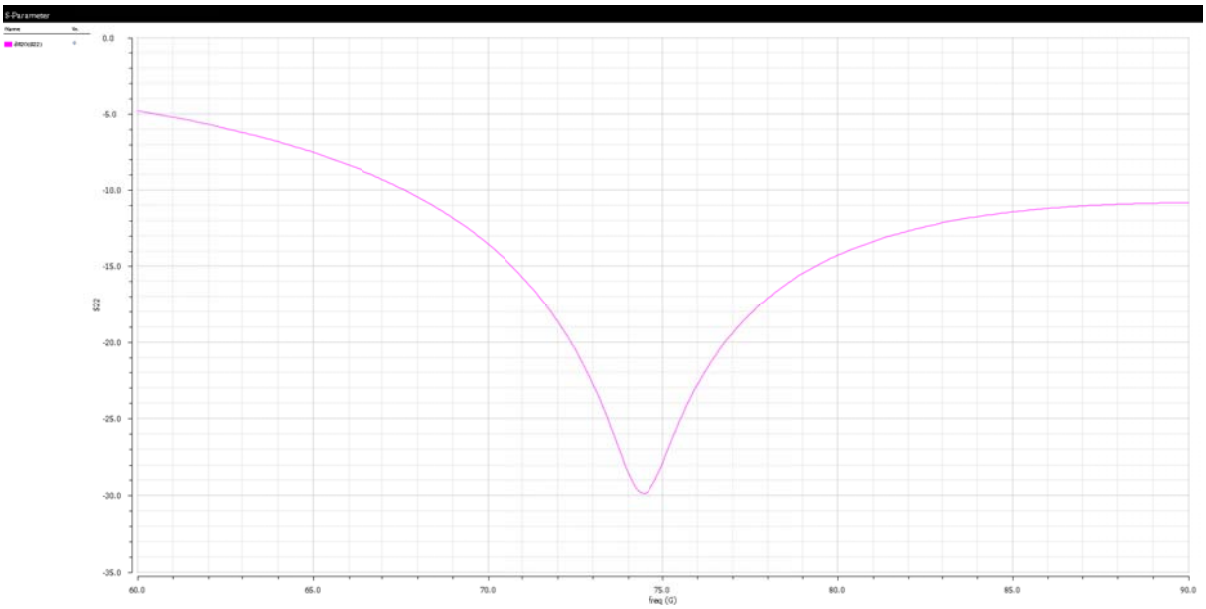


Figure 3.1-3 Simulated S22 of the LNA

The simulated gain of the LNA is shown in Figure 3.1-4. It achieves 17dB of gain at 77GHz. The gain drops to 16.1dB and 15.5dB at 71GHz and 86GHz respectively. The LNA features reverse isolation better than 40dB in the whole band of interest as depicted in Figure 3.1-5.

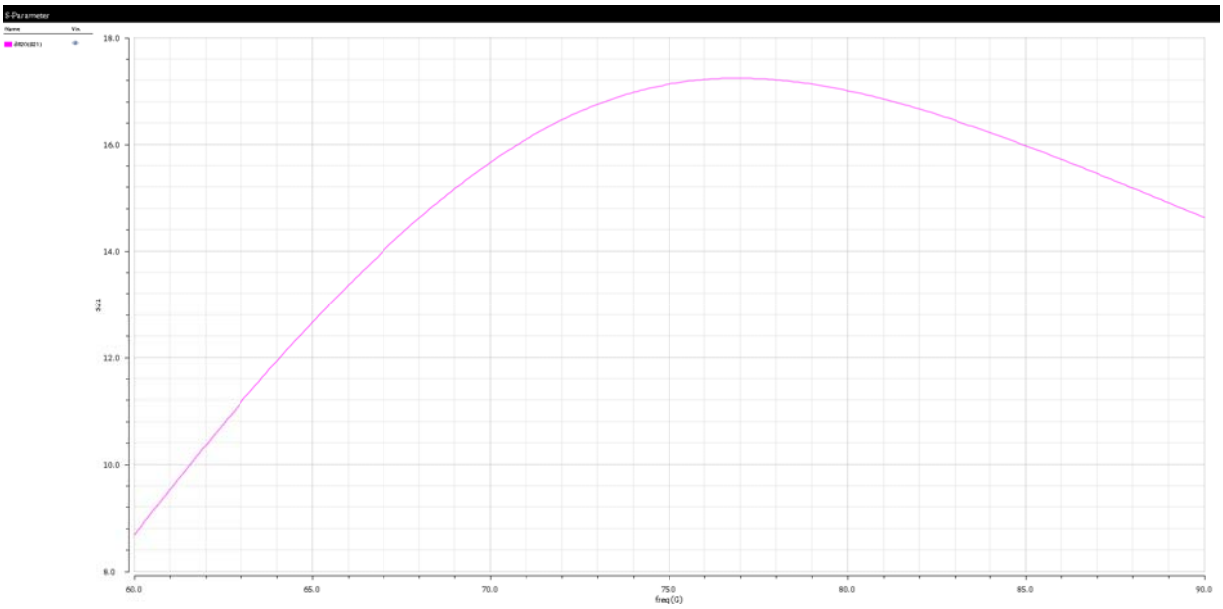


Figure 3.1-4 Simulated gain of the LNA

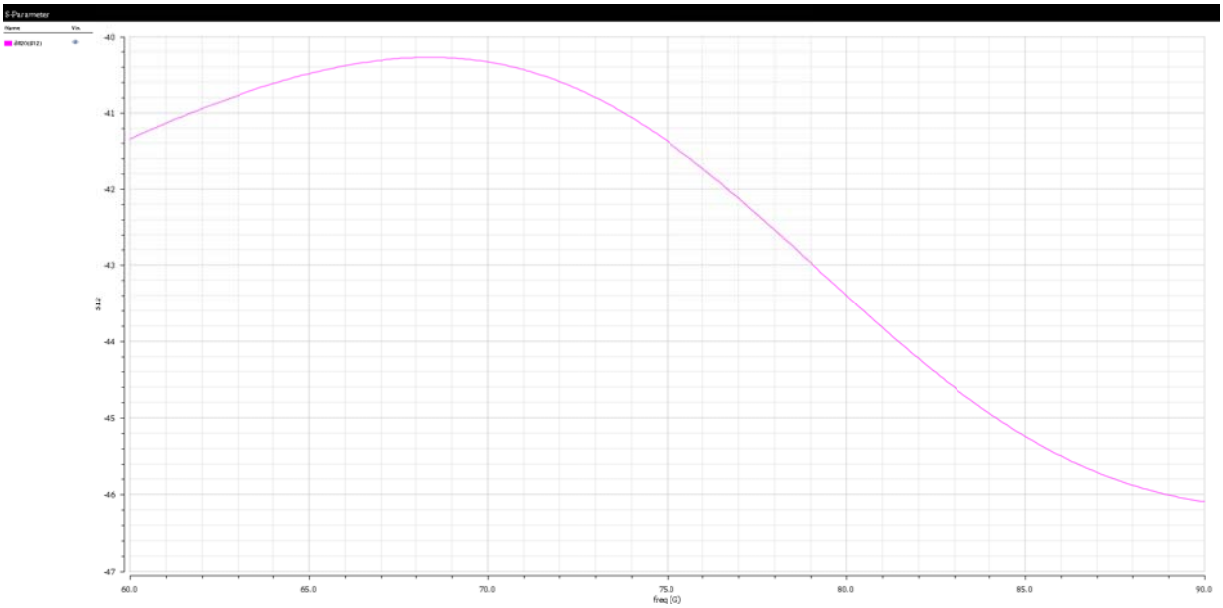


Figure 3.1-5 Reverse isolation of the LNA

The simulated noise figure of the LNA is below 5.1dB in the band of interest as shown in Figure 3.1-6. The linearity of the LNA simulated at 74GHz and 84GHz is depicted in Figure 3.1-7 and Figure 3.1-8, respectively. The LNA reaches compression point for input signal level of -12.7dBm at 74GHz and -11.32dBm at 84GHz.

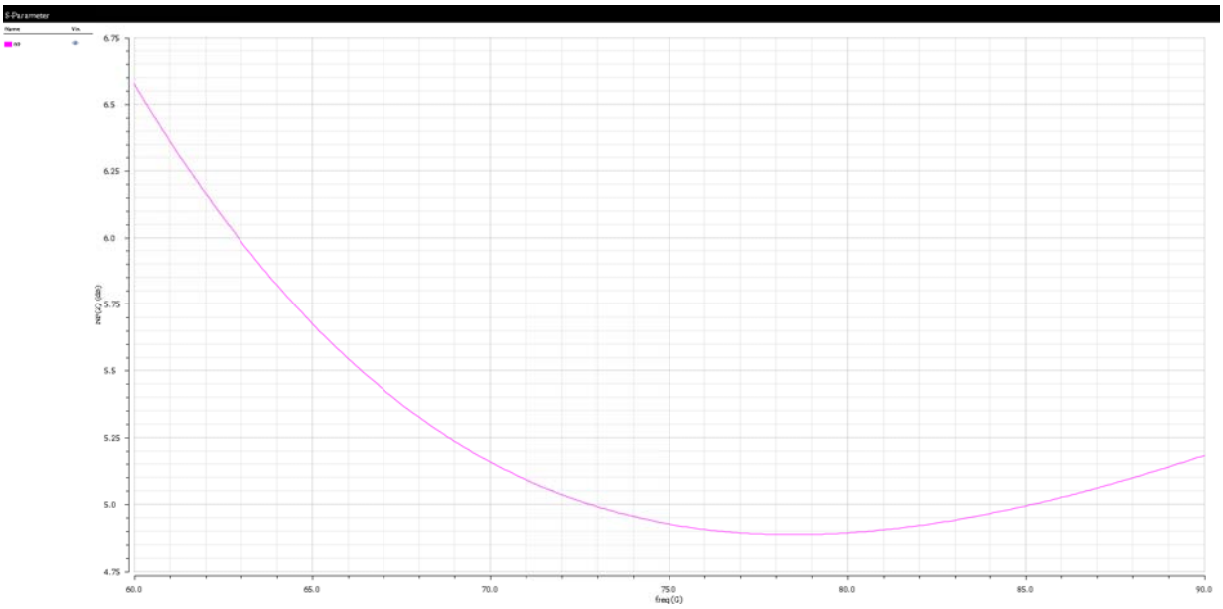


Figure 3.1-6 Simulated noise figure of the LNA

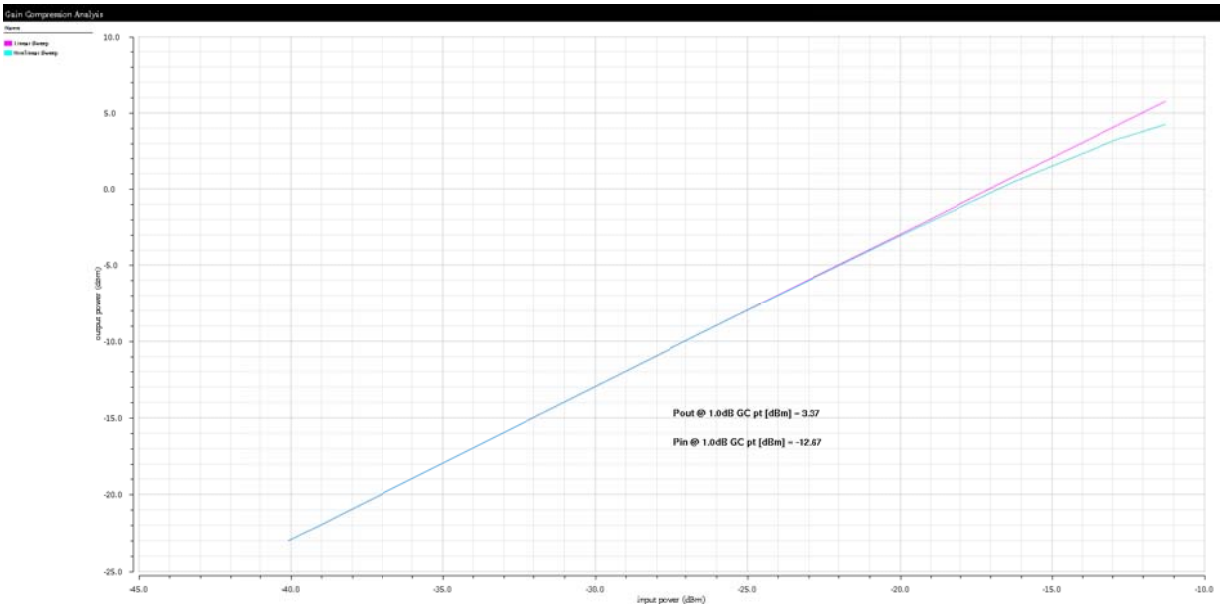


Figure 3.1-7 Simulated linearity of the LNA at 74GHz

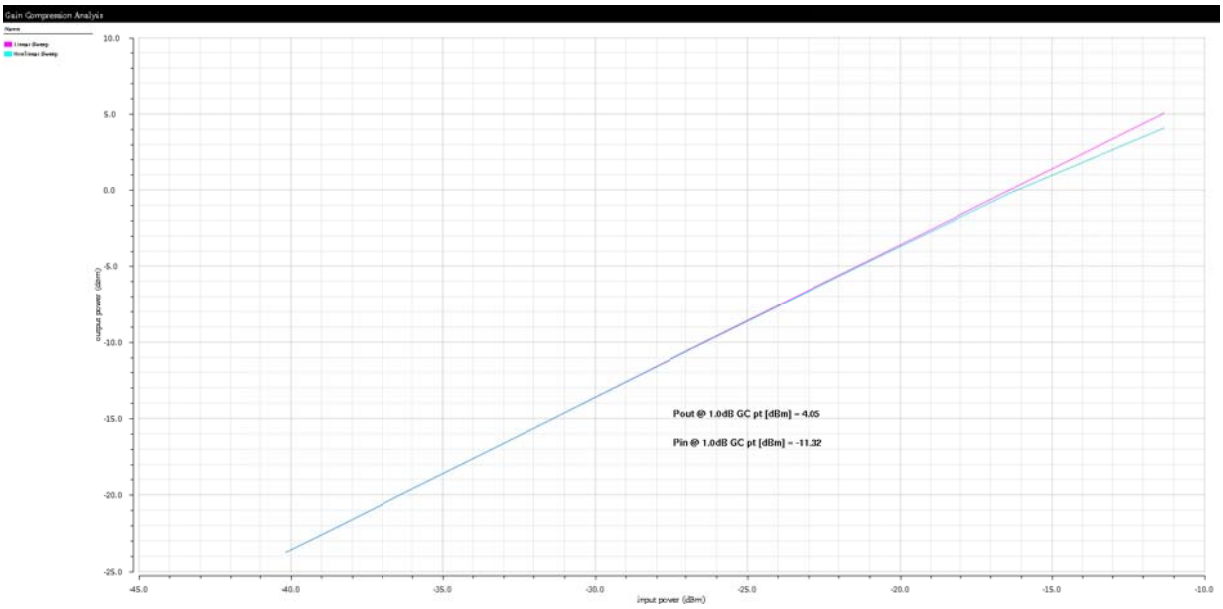


Figure 3.1-8 Simulated linearity of the LNA at 84GHz

The layout of the LNA occupies an area of 420x550 μm^2 and is shown in Figure 3.1-9.

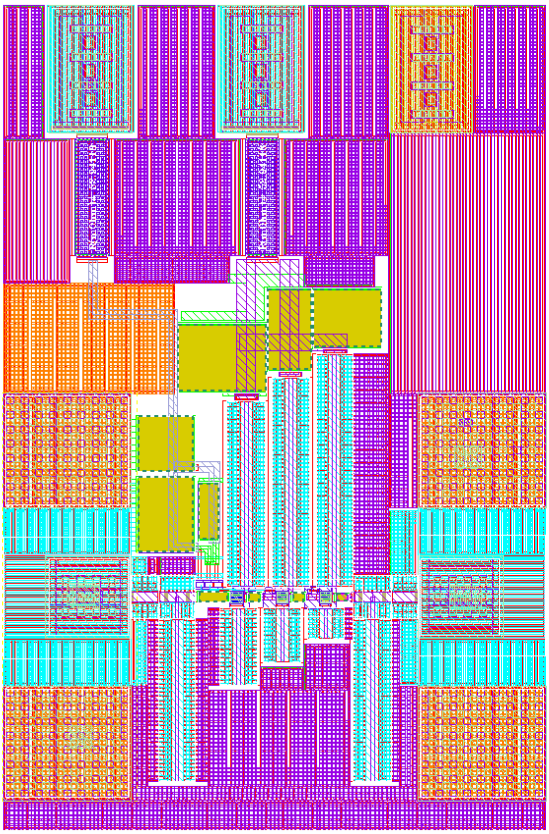


Figure 3.1-9 Layout of the LNA

3.1.3. Comparison of simulation results with specifications in D1.2.2

Table 3.1-1 shows the comparison between LNA parameters coming from the specification phase and the simulated values.

Parameter	Simulation Result	Spec. met?	Comments
RF Output Frequency	70GHz - 77GHz and 80GHz - 87GHz	YES	
RF Output bandwidth	7	YES	
Input Impedance	50 Ω	YES	
Input match at Fc	- 14dB	YES	
Reverse isolation at Fc	40dB	YES	
Power gain	17dB	NO	Gain is 1dB lower than specified, this can be compensated in following stages of RX
Output 1dB compression point	-4dBm	YES	
Noise Figure	5.1dB	YES	
Gain ripple	0.5dB	YES	

Table 3.1-1 Summary of simulation results for the LNA

3.2 Updated IFA results

3.2.1. Circuit description

The intermediate frequency amplifier (IFA1) is a single stage fully differential type. It utilizes current-splitting technique to achieve gain control, maintain its input and output return loss in different mode and also maintain the current of LNA in both high gain and low gain mode. The schematic of the IFA is shown in Figure 3.2-1.

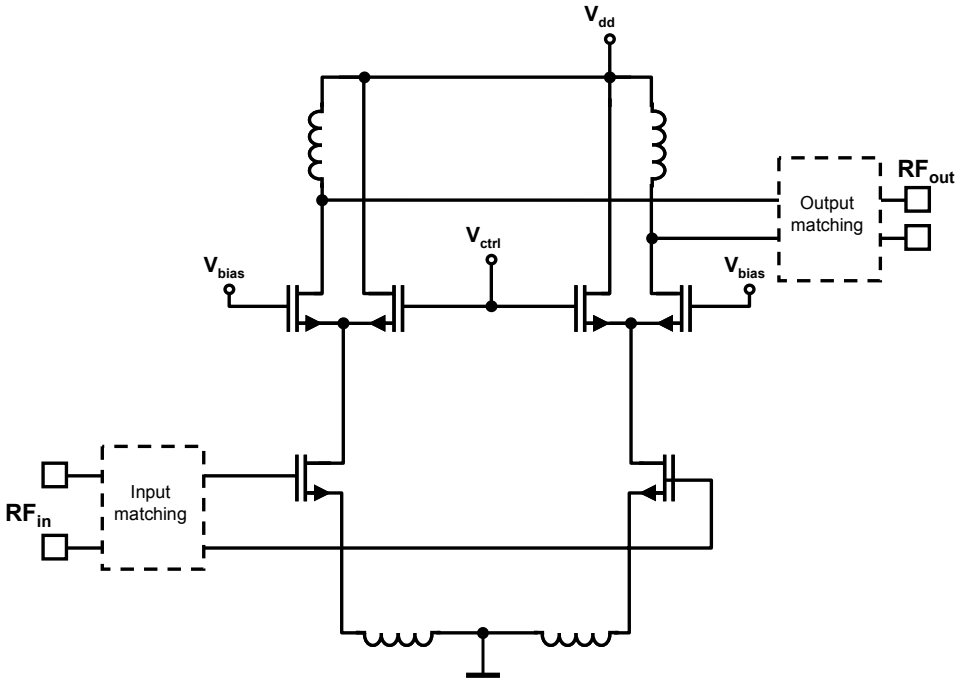


Figure 3.2-1 IFA schematic

3.2.2. Results

Figure 3.2-2, Figure 3.2-3, Figure 3.2-4 and Figure 3.2-5 show the input and output matching of the IFA in the frequency band of interest for high gain mode (HGM) and low gain mode (LGM), respectively. The input matching as well as the output matching is not severely affected by the gain switching.

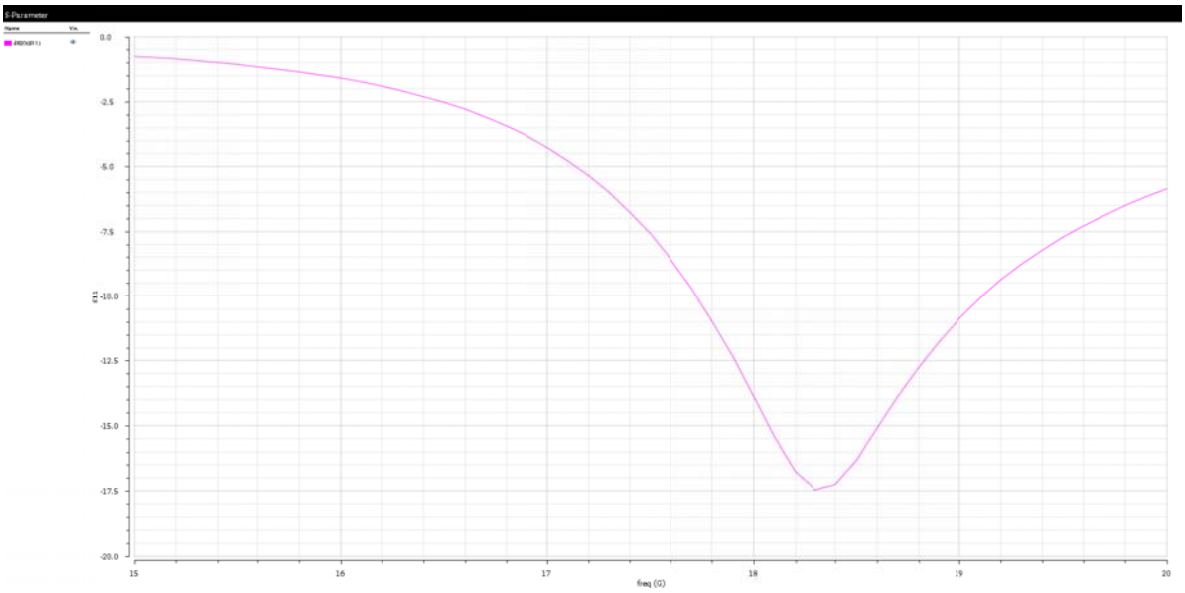


Figure 3.2-2 Simulated S11 for HGM

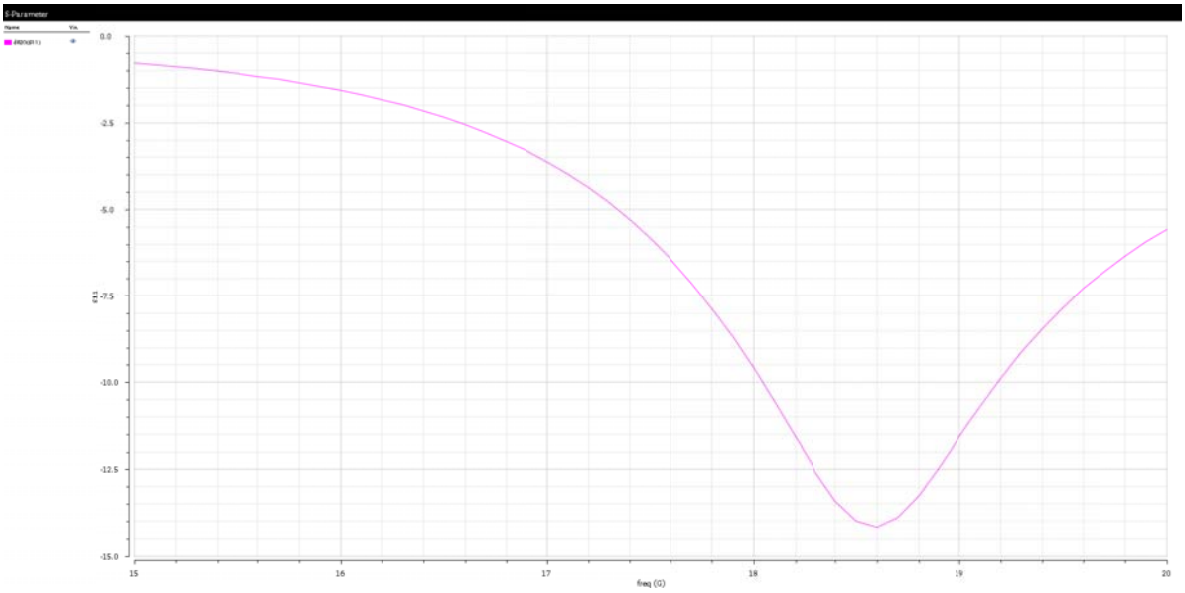


Figure 3.2-3 Simulated S11 for LGM

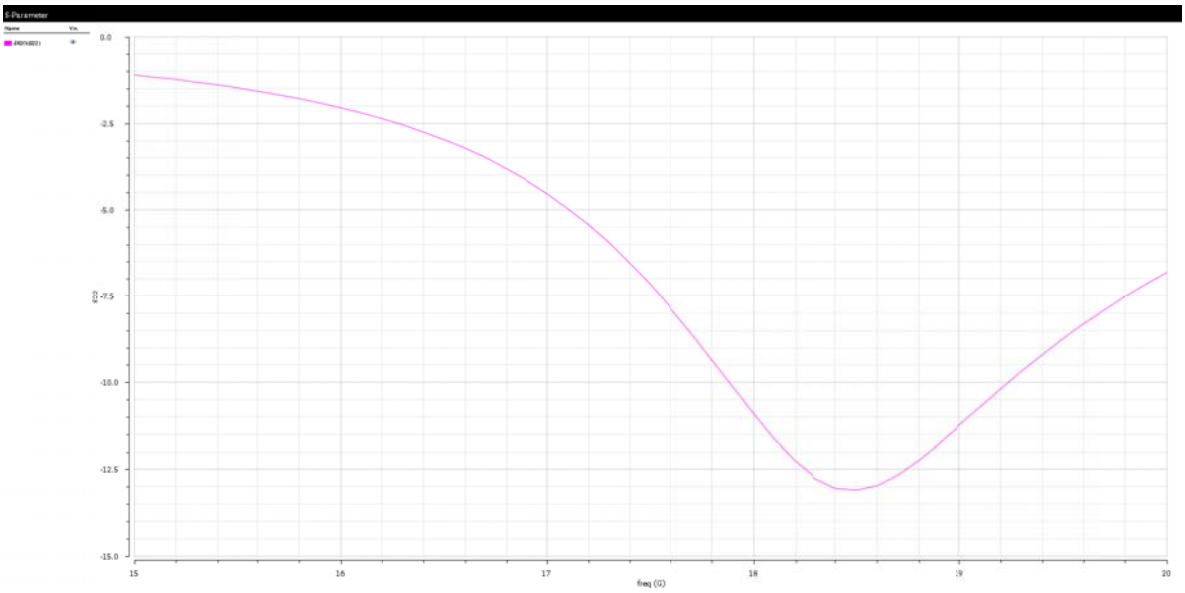


Figure 3.2-4 Simulated S22 for HGM

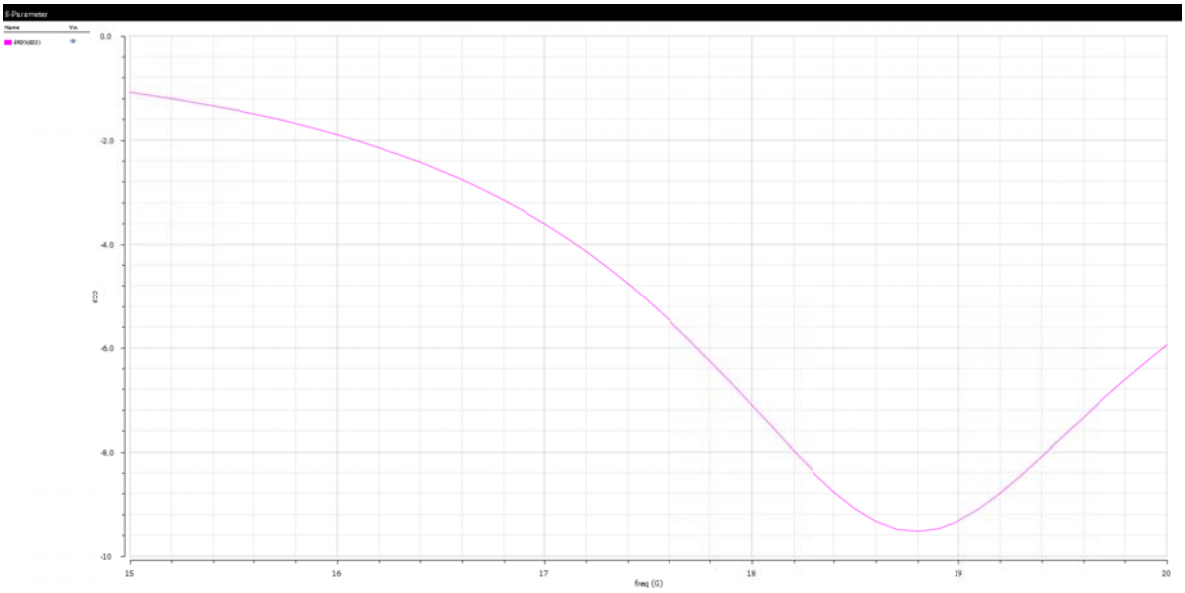


Figure 3.2-5 Simulated S22 for LGM

The simulated gain of the IFA is shown in Figure 3.2-6 and Figure 3.2-7. The IFA achieves 12.5dB and -2.5dB of gain at 18.8GHz for high and low gain setting respectively. 3dB bandwidth of the amplifier exhibits 2.2GHz. The IFA features reverse isolation better than 26dB in the whole band of interest as depicted in Figure 3.2-8 and Figure 3.2-9. The simulated noise figure of the IFA is below 3dB over the 3dB bandwidth for HGM (Figure 3.2-10). In LGM the amplifier achieves a noise figure of 7dB as depicted in Figure 3.2-11.

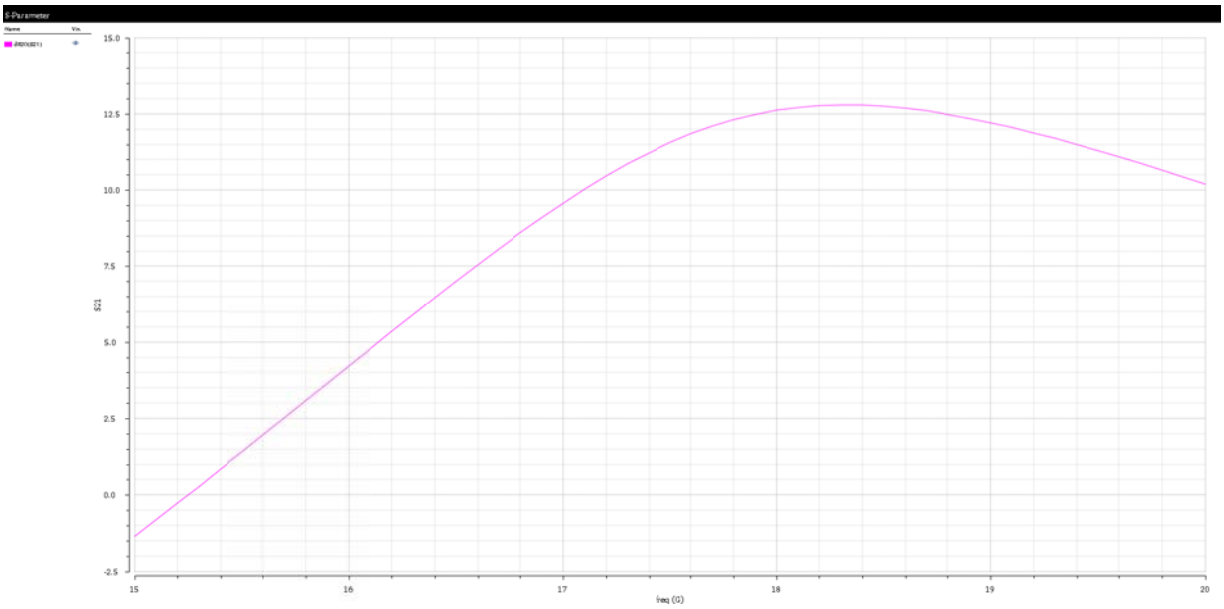


Figure 3.2-6 Simulated gain of the IFA for HGM

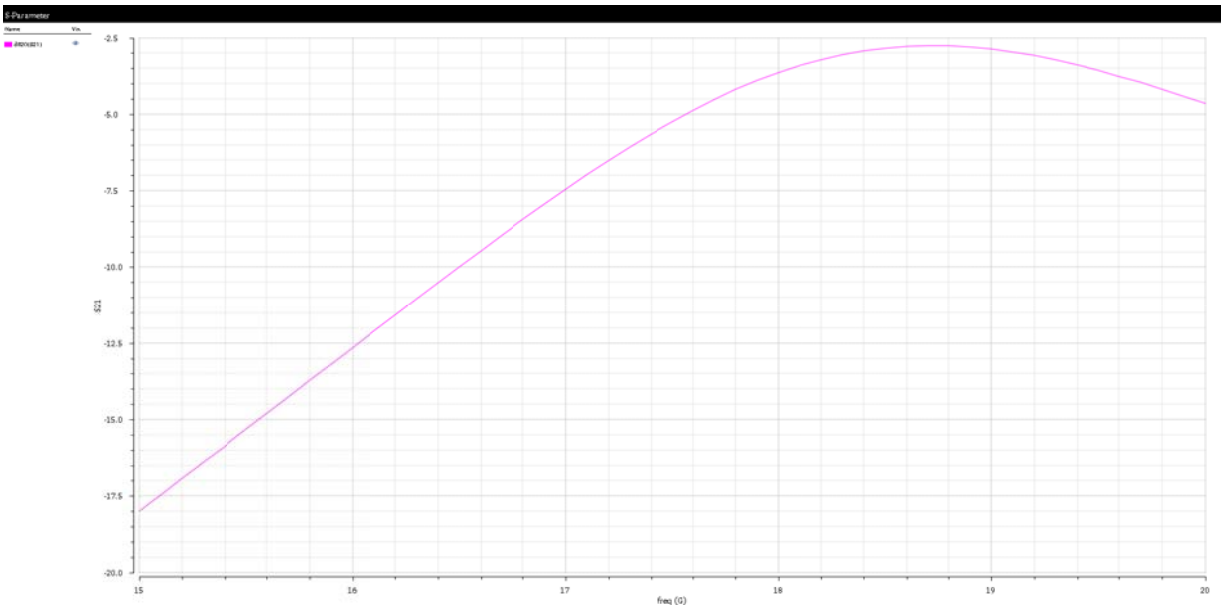


Figure 3.2-7 Simulated gain of the IFA for LGM

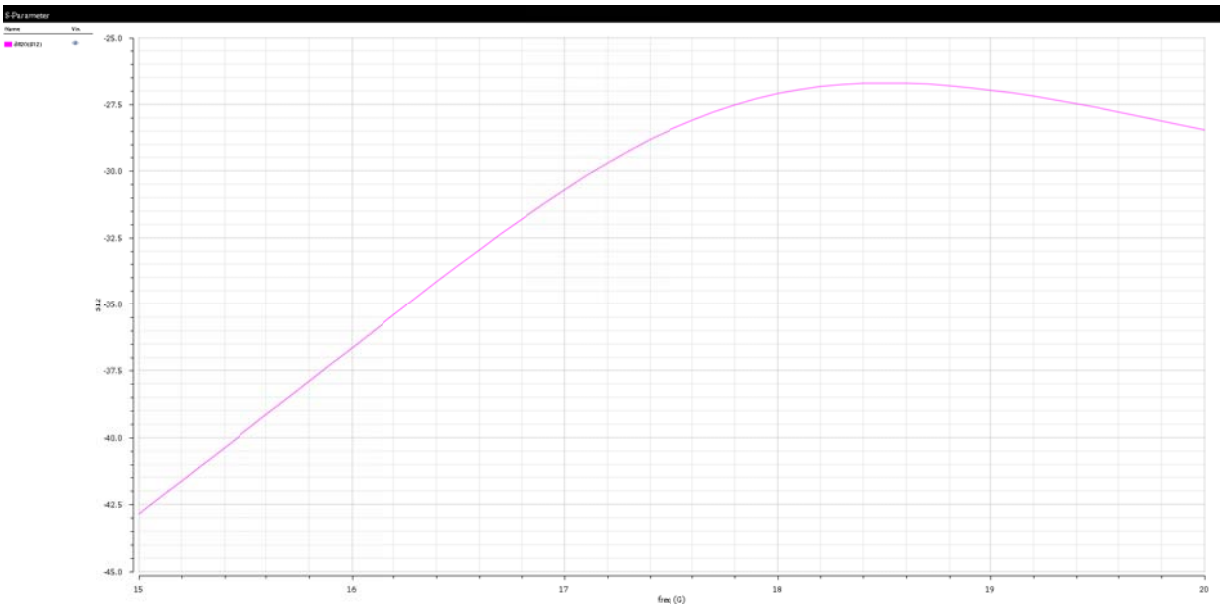


Figure 3.2-8 Reverse isolation of the IFA for HGM

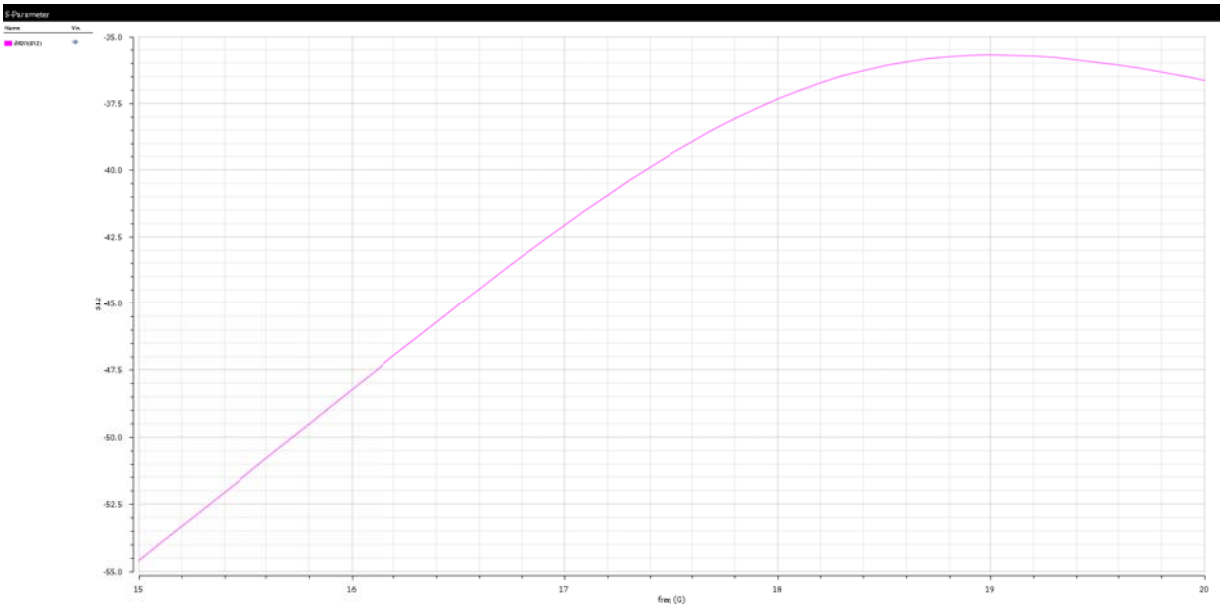


Figure 3.2-9 Reverse isolation of the IFA for LGM

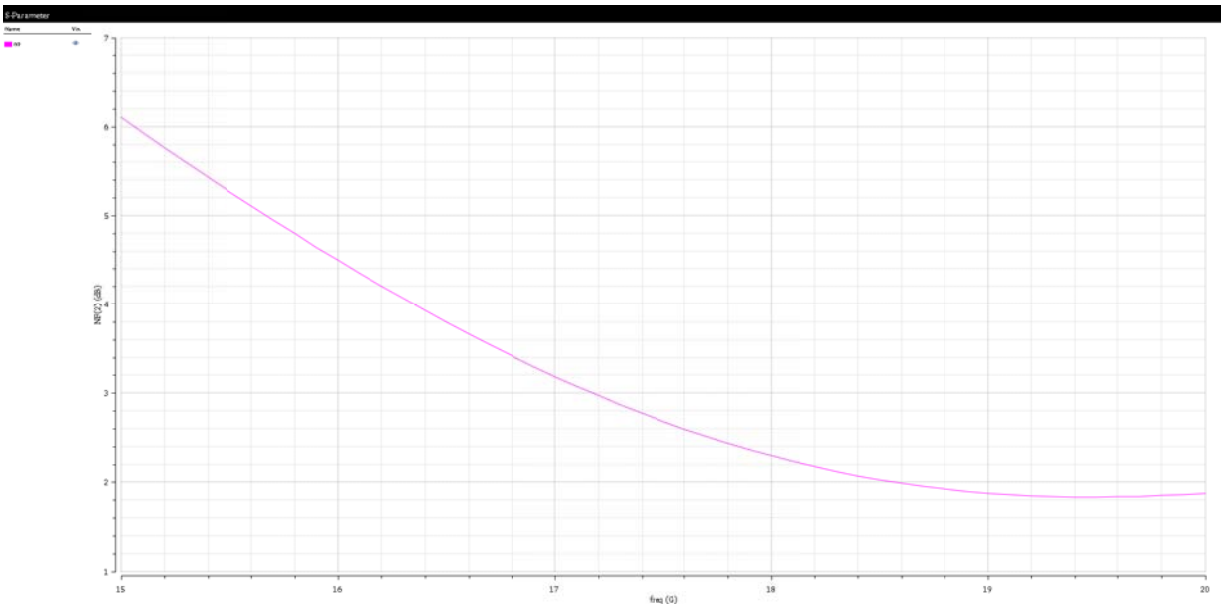


Figure 3.2-10 Simulated noise figure of the IFA for HGM

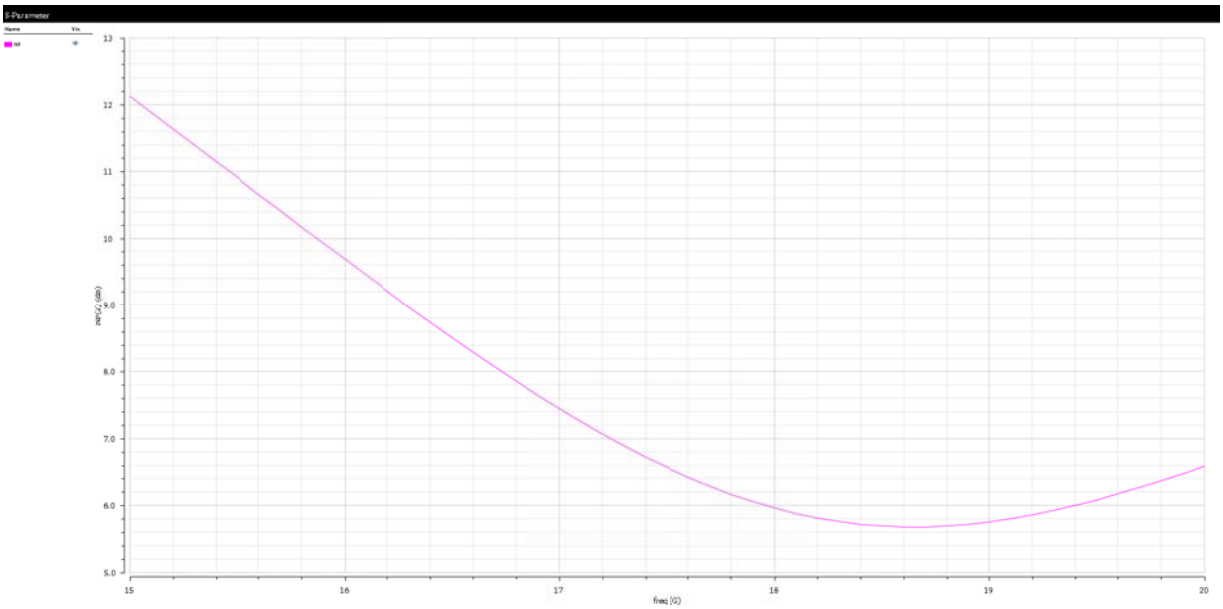


Figure 3.2-11 Simulated noise figure of the IFA for LGM

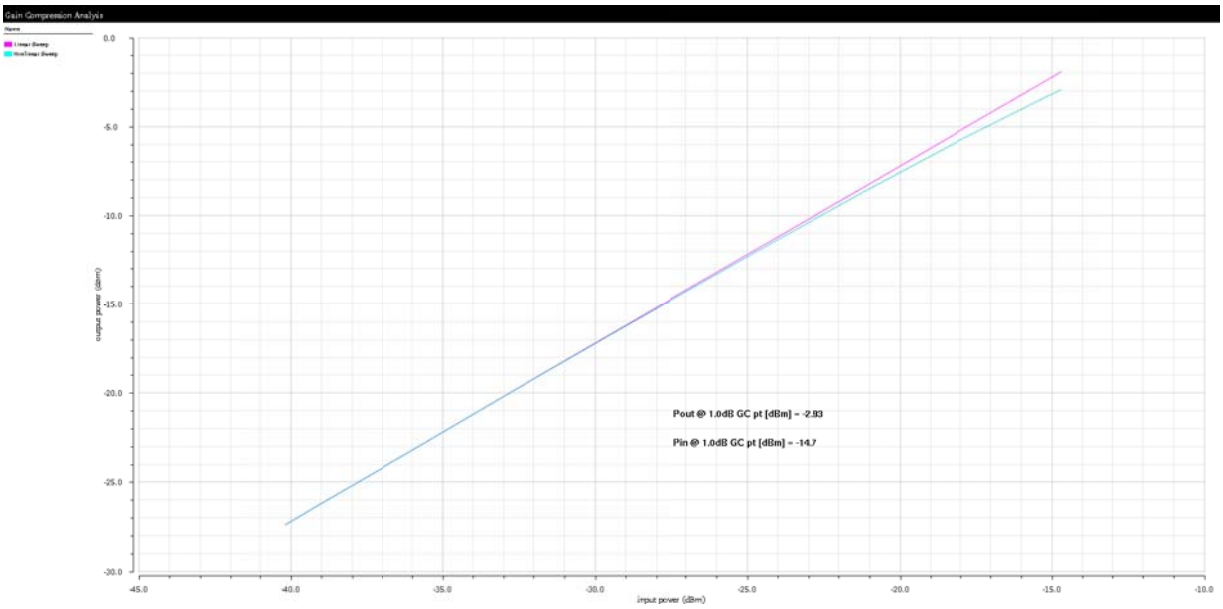


Figure 3.2-12 Simulated linearity for HGM

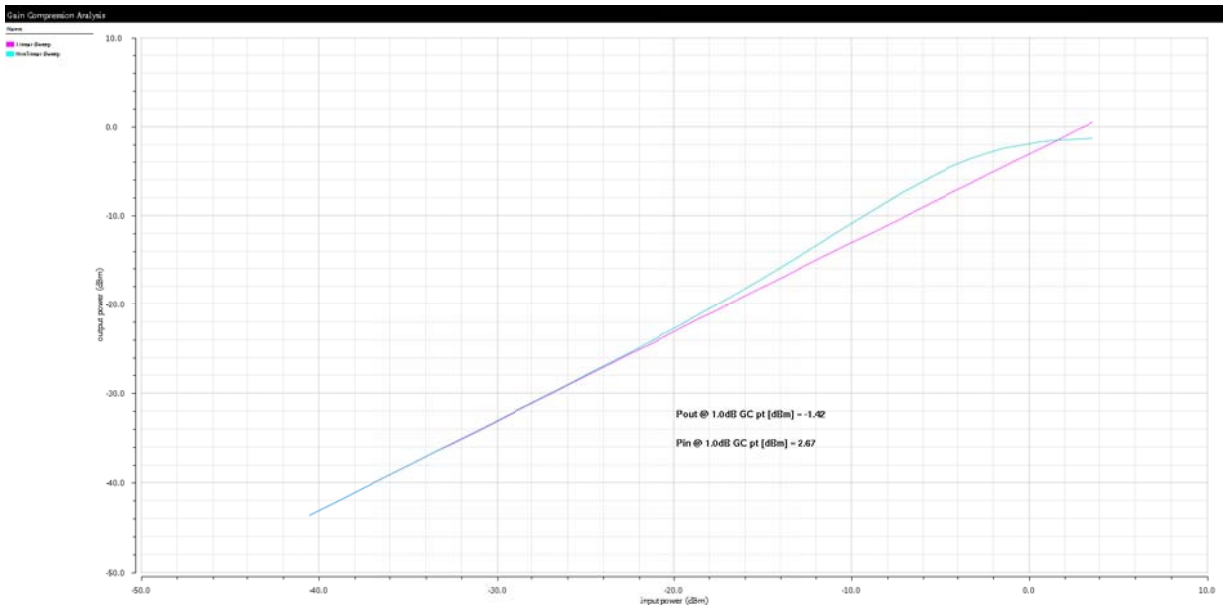


Figure 3.2-13 Simulated linearity for LGM

The linearity of the IFA simulated at 18.9GHz in HGM and LGM is presented in Figure 3.2-12 and Figure 3.2-13. The IFA reaches 1dB output compression point at output signal level of -2.9dBm for HGM and -1.4dBm for LGM.

The layout of the IFA is shown in Figure 3.2-14. The circuit occupies an area of 625x900 μm².

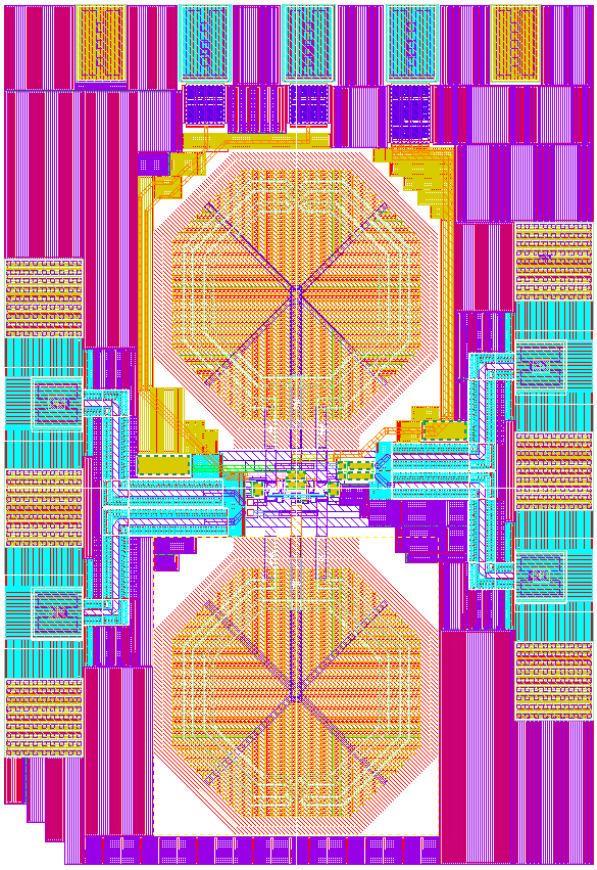


Figure 3.2-14 Layout of the IFA

3.2.3. Comparison of simulation results with specifications in D1.2.2

Table 3.2-1 shows the comparison between IFA parameters coming from the specification phase and the simulated values.

Parameter	Simulation Result	Spec. met?	Comments
IF Input Frequency	16GHz - 21GHz	NO	Band switching required – will be implemented in the next redesign
RF Output bandwidth	7	YES	
Input Impedance	100 Ω	YES	
Output Impedance	100 Ω	YES	
Input match at Fc	- 15dB	YES	
Reverse isolation at Fc	26dB	YES	
Power gain (HGM)	12.5dB	YES	
Power gain (LGM)	-2.5dB	NO	2.5dB lower than specified. Redesign is needed
Gain step	10dB	NO	Gain step 15dB, can be optimized if required
Noise Figure (HGM)	3dB	YES	
Noise Figure (LGM)	7dB	YES	
Output 1dB compression point (HGM)	-2.9dBm	YES	
Output 1dB compression point (LGM)	-1.4dBm	YES	

Table 3.2-1 Summary of simulation results for the IFA

3.3 mmW Receiver results

3.3.1. Circuit description

A block diagram of the mmW RX is shown in Figure 3.3-1. It consists of LNA, mixer and IFA. The circuit converts the signals from 70-77GHz and 80-87GHz bands to 16-21GHz IF band. The LO signal will be delivered from external source of 55GHz and 65GHz depending in the input band of operation. The LNA and IFA described in previous sections are slightly modified (only matching structures) to get the best performance in combination with mixer. The mixer implemented here is a standard double-balanced Gilbert cell structure.

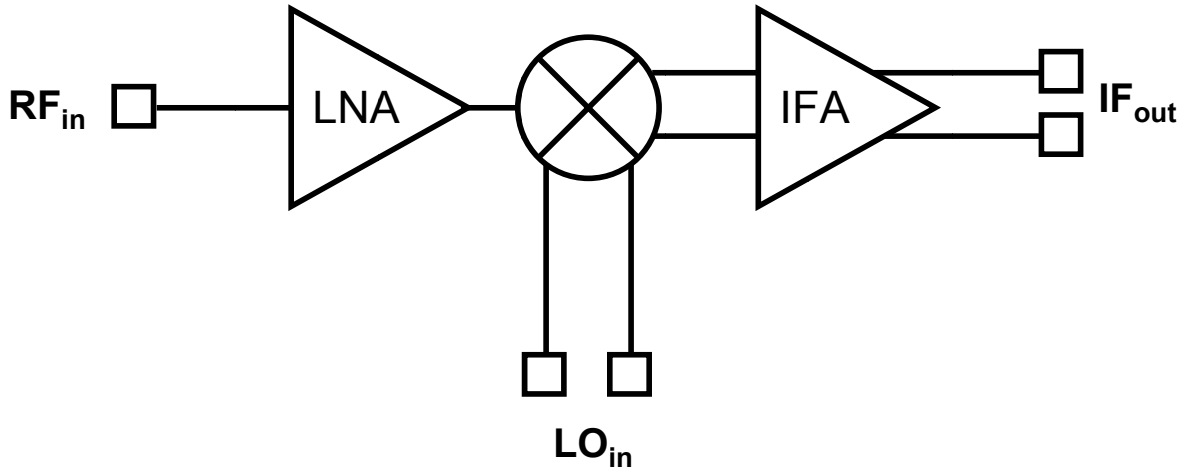


Figure 3.3-1 Block diagram of mmW RX

3.3.2. Results

Figure 3.3-2, Figure 3.3-3 and Figure 3.3-4 show the matching at all three high frequency ports of the mmW RX in the relevant frequency bands.

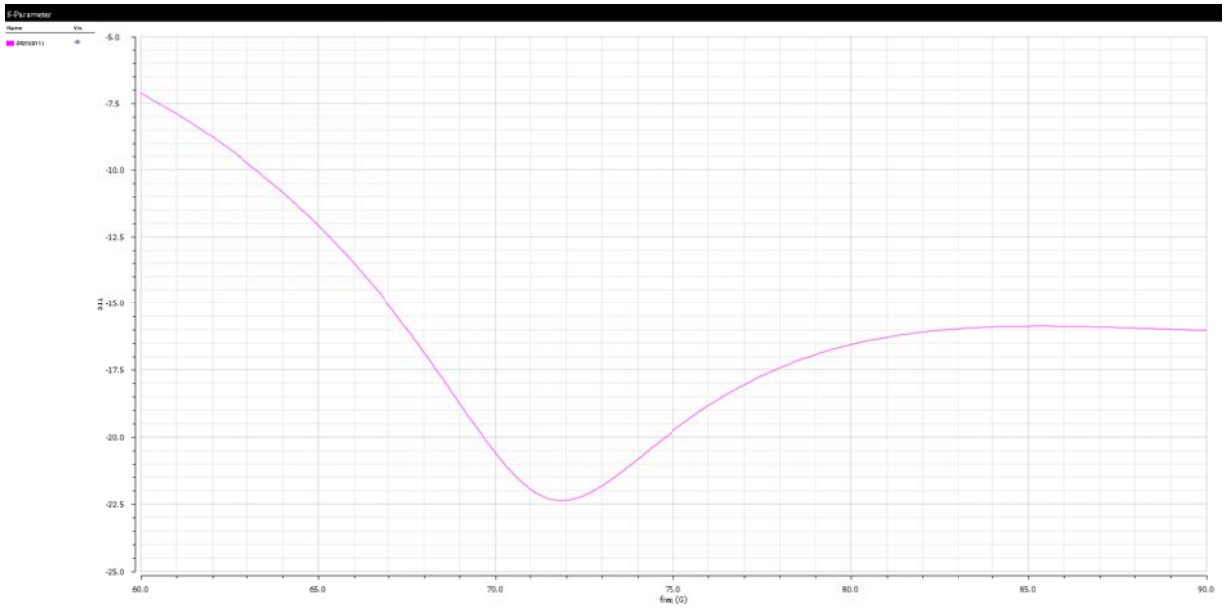


Figure 3.3-2 Simulated S11 at RF input port

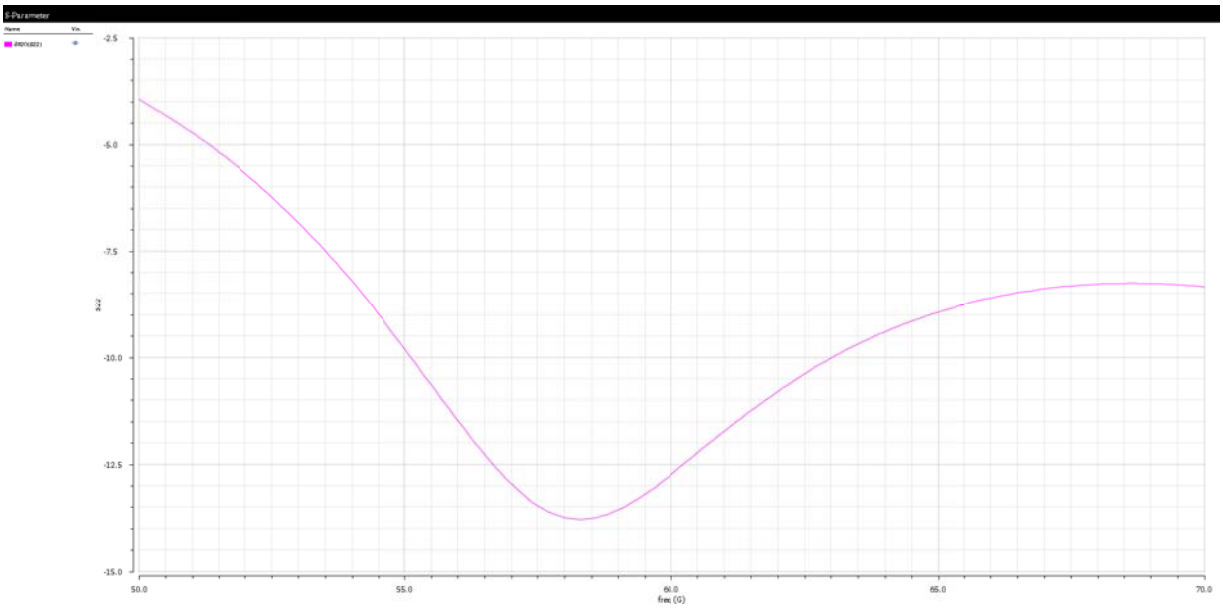


Figure 3.3-3 Simulated S11 at LO input port

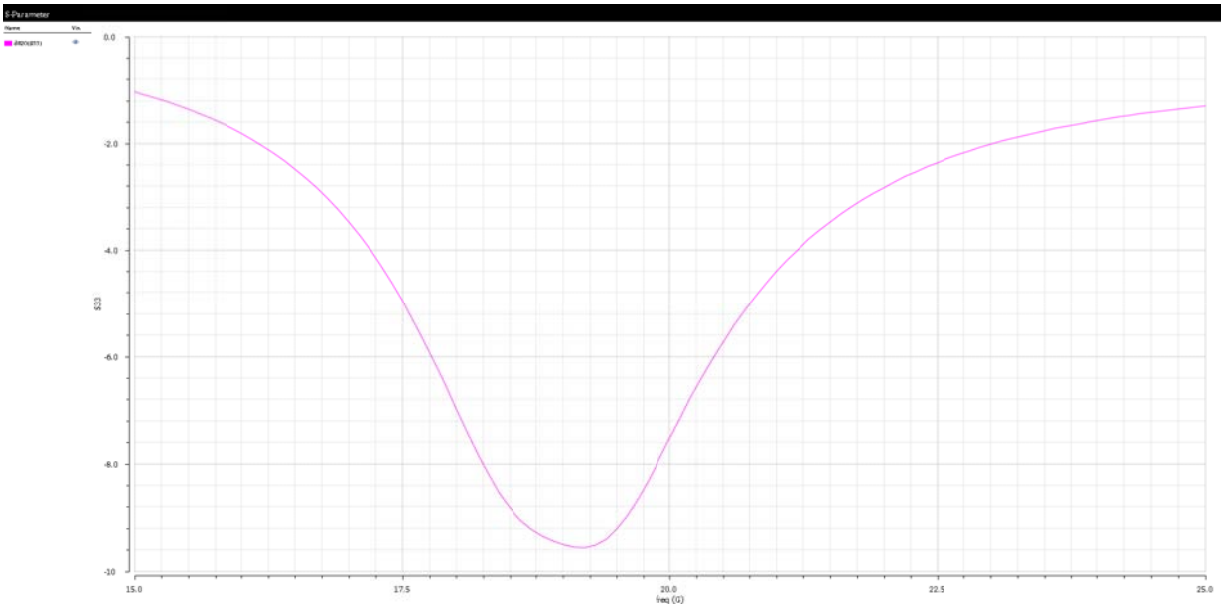


Figure 3.3-4 Simulated S22 at IF output port

The simulated conversion gain of the mmW RX is shown in Figure 3.3-5 and Figure 3.3-6. The simulation was performed for fixed LO frequency and swept RF input frequency. The mmW RX achieves 37.5dB and 25.5dB of gain for high and low gain modes in the lower part of E-band respectively. Conversion gain values of 35.2dB and 23dB for high and low gain setting are obtained for the upper part of E-band.

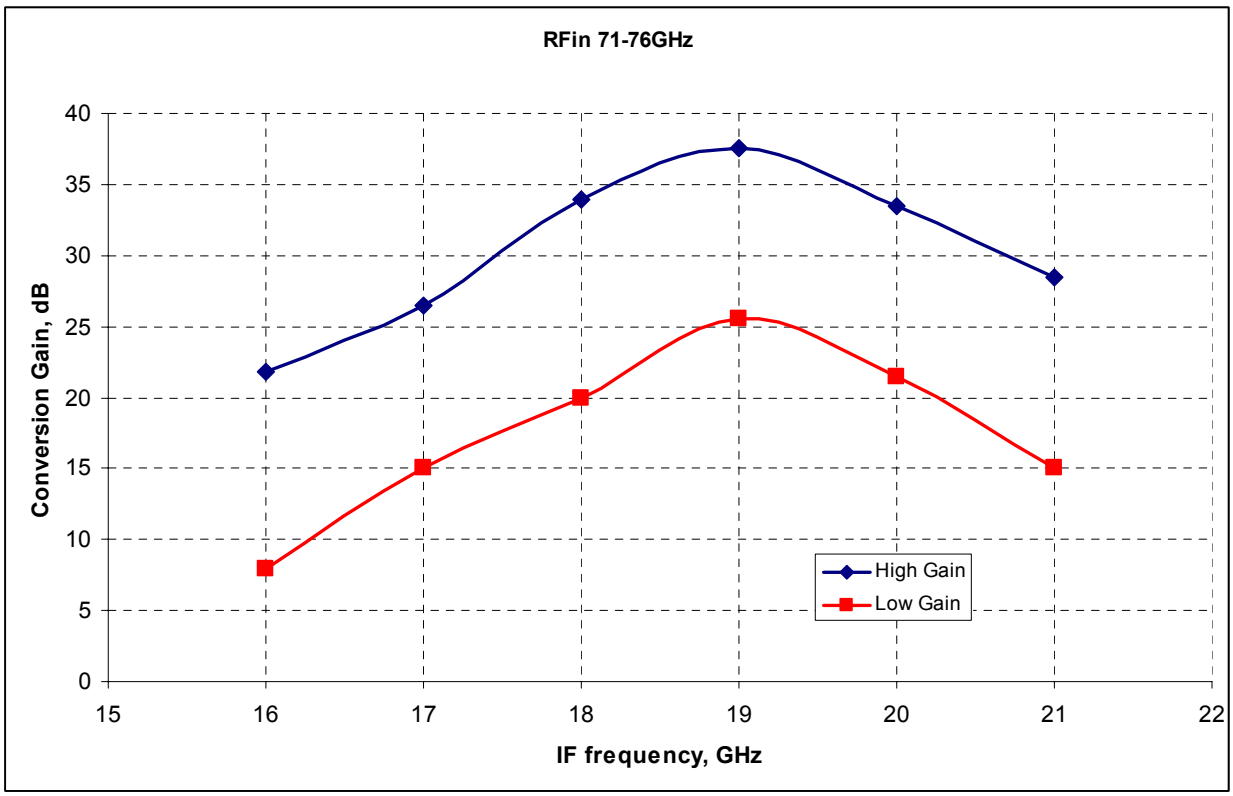


Figure 3.3-5 Conversion gain of the mmW RX in HG and LG modes for the lower part of E-band

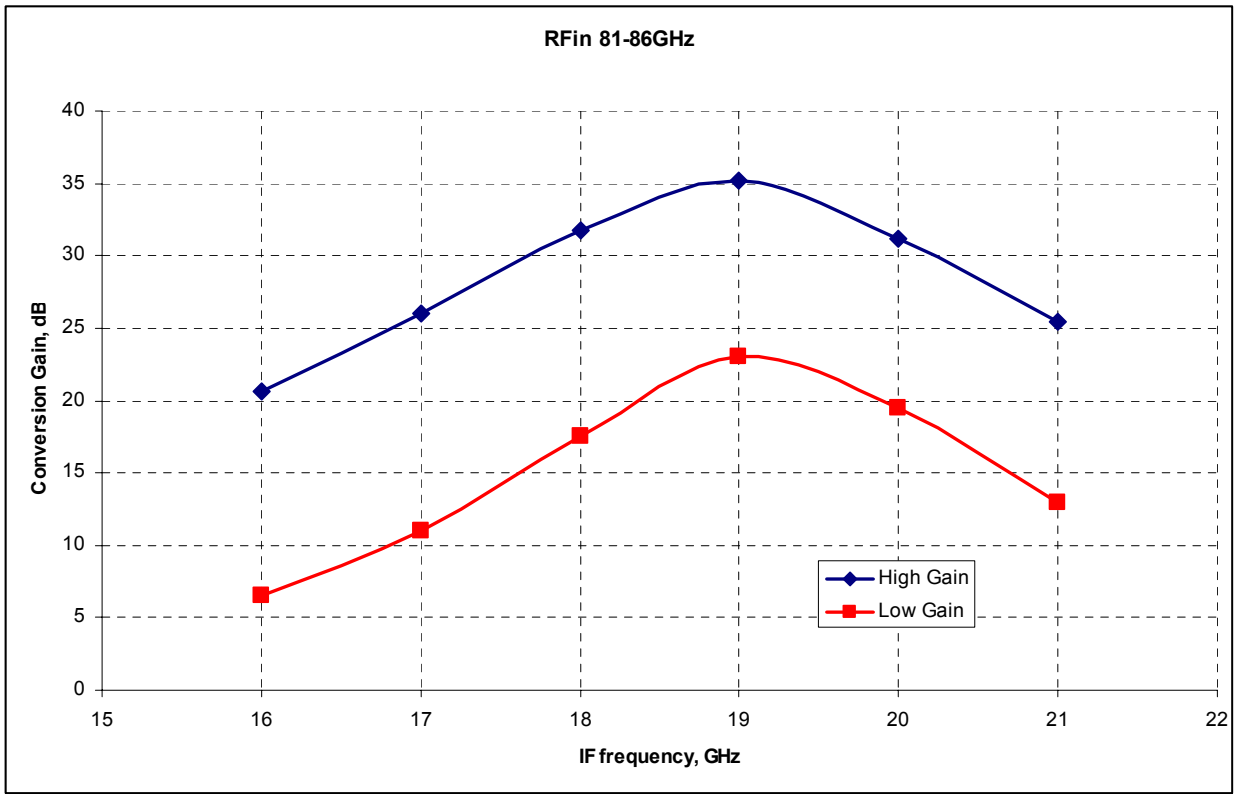


Figure 3.3-6 Conversion gain of the mmW RX in HG and LG modes for upper part of E-band

The linearity of the mmW RX simulated at 74GHz in HGM and LGM is presented in Figure 3.3-7 and Figure 3.3-8. 1dB output compression point at input signal level of -39.2dBm for HGM and -29.7dBm for LGM is achieved.

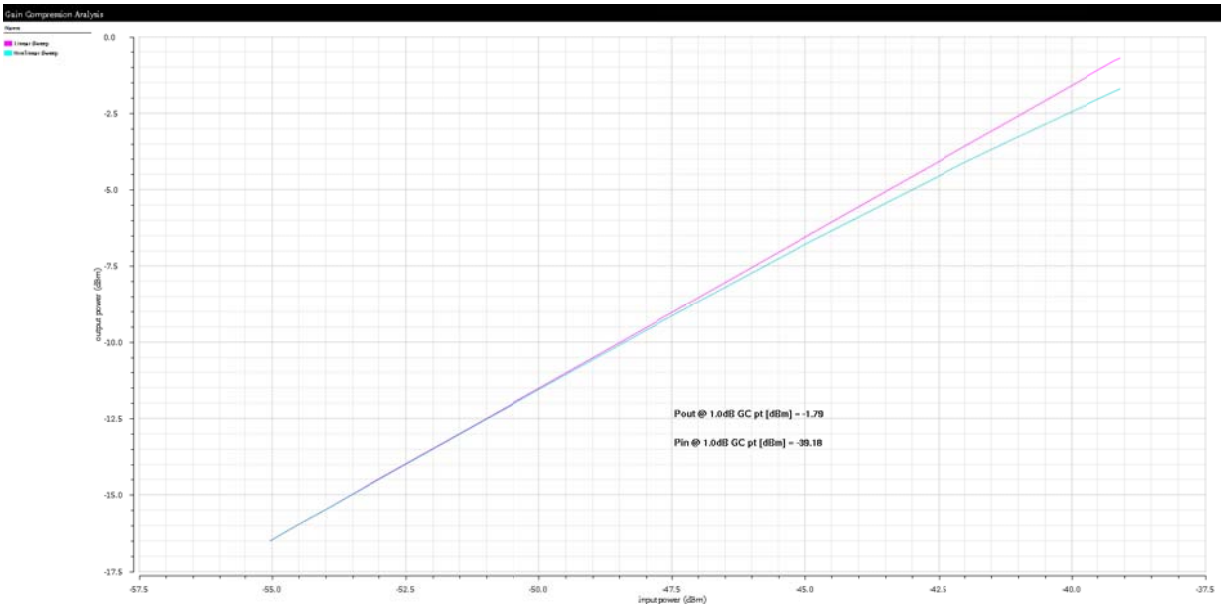


Figure 3.3-7 Linearity of the mmW RX at 74GHz in HG mode

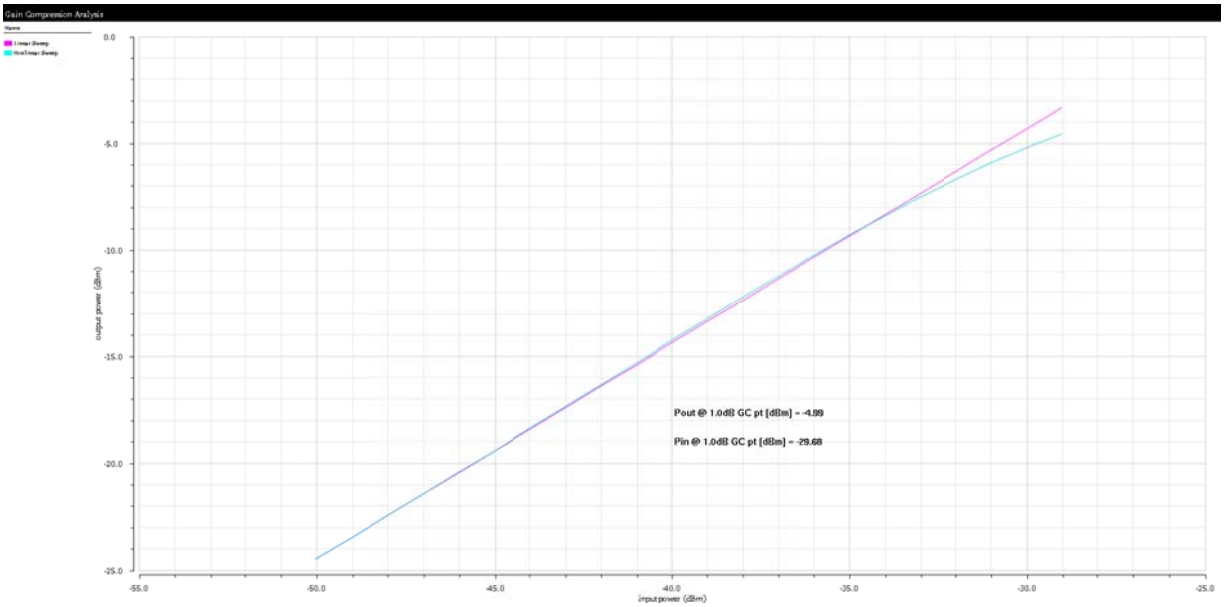


Figure 3.3-8 Linearity of the mmW RX at 74GHz in LG mode

The linearity of the mmW RX simulated at 84GHz in HGM and LGM is depicted in Figure 3.3-9 and Figure 3.3-10. 1dB output compression point at input signal level of -36.6dBm for HGM and -26.9dBm for LGM is achieved.

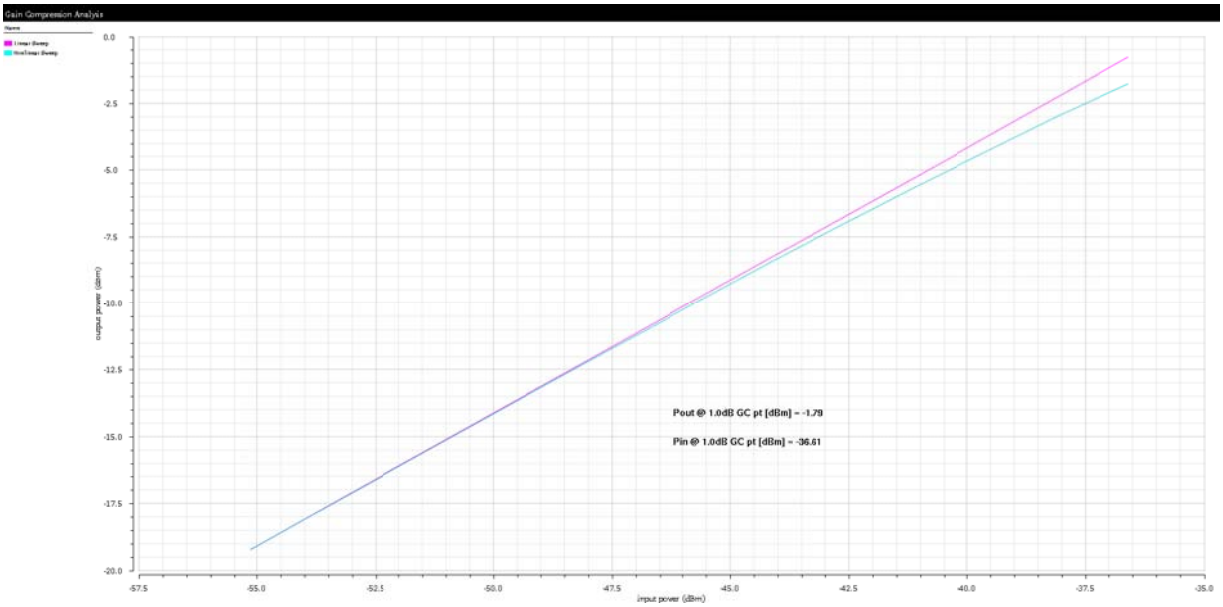


Figure 3.3-9 Linearity of the mmW RX at 84GHz in HG mode

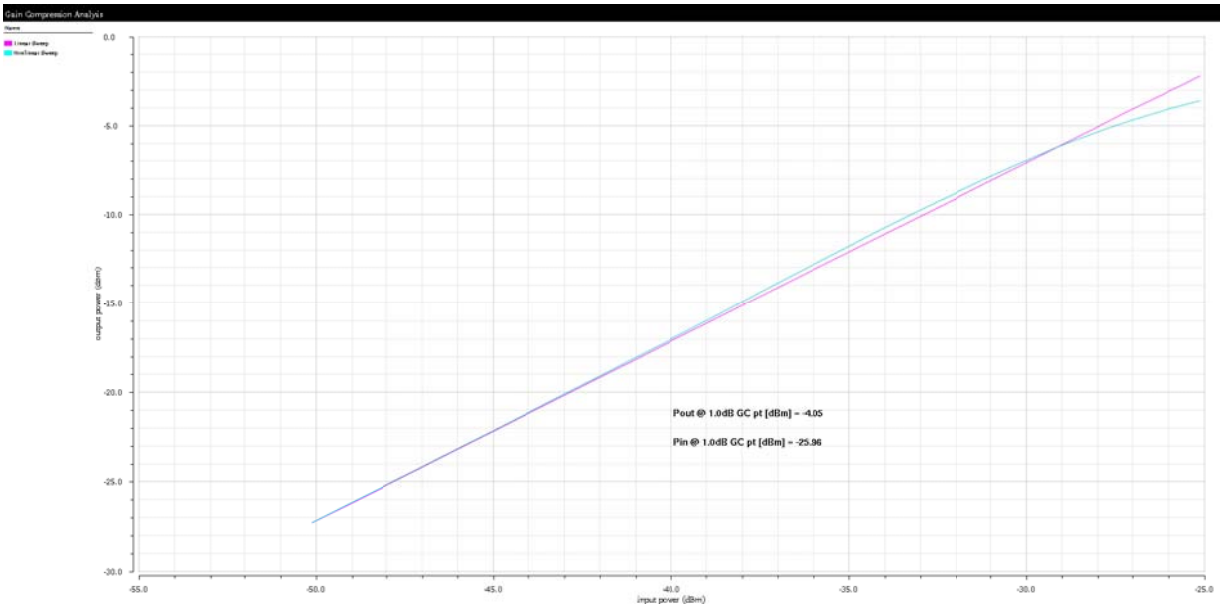


Figure 3.3-10 Linearity of the mmW RX at 84GHz in LG mode

The layout of the receiver occupies an area of 1x1mm^2 and is shown in Figure 3.3-11.

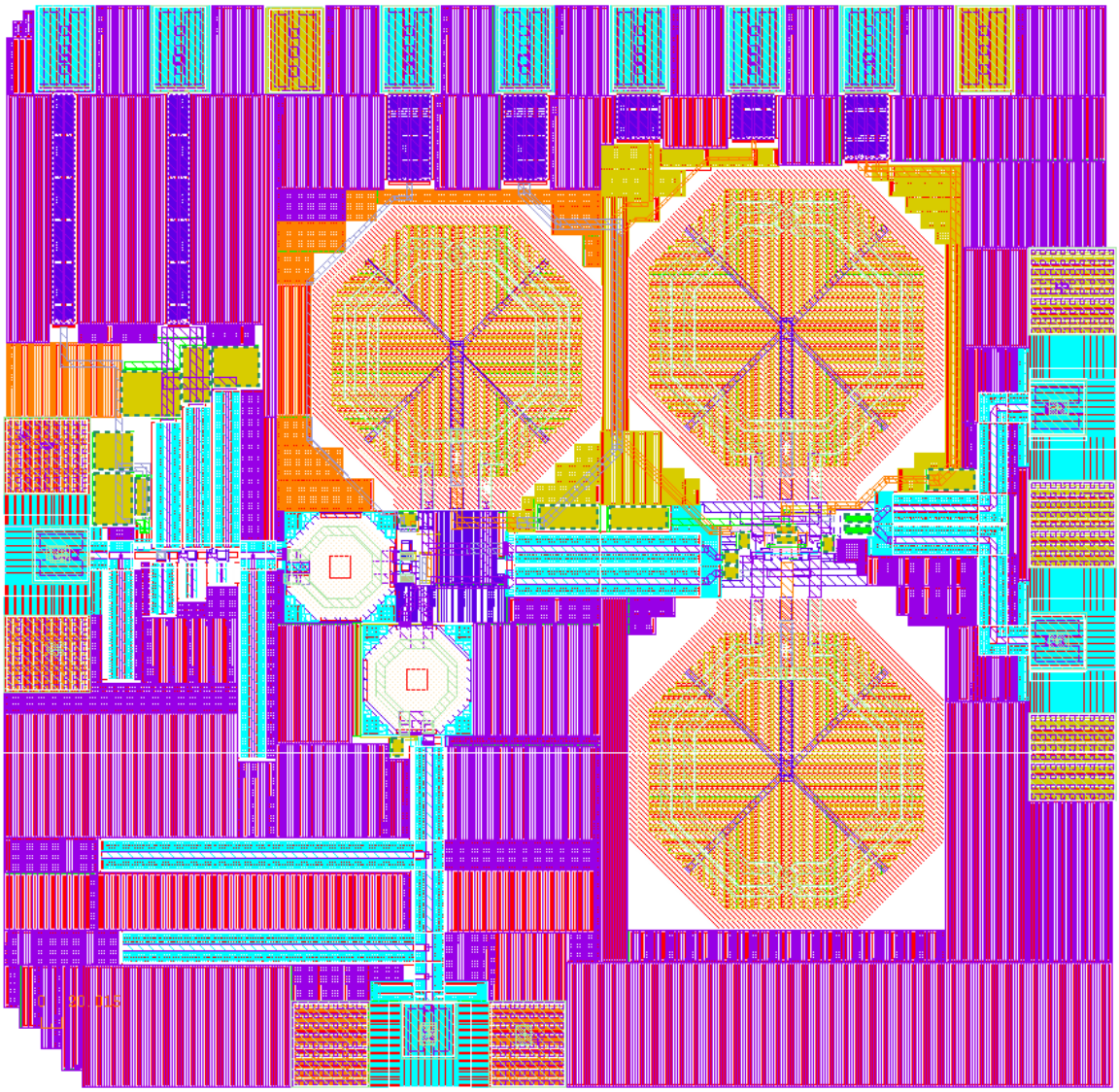


Figure 3.3-11 Layout of mmW RX

4. SIGNAL GENERATION RESULTS

4.1 PLL loop optimization

The PLL is based on an integer-N architecture with 2nd order loop-filter, shown in next figure.

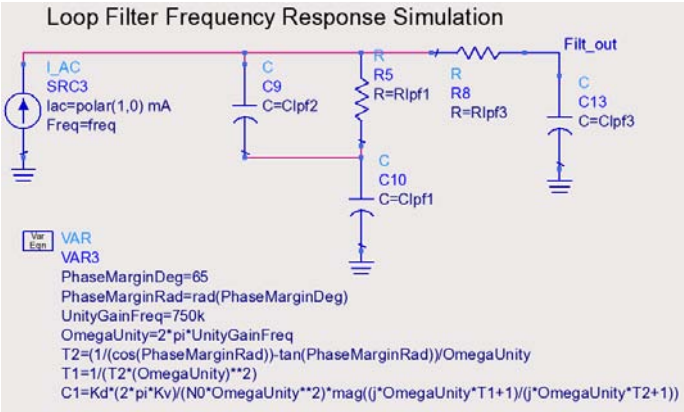


Figure 4.1-1 PLL loop filter and calculation of the 2nd order system components

The filter is simulated alone in an open loop and in closed loop using linearized models for the other components of the PLL. Next figure shows one example of filter characteristic for a specification of cut-off frequency of 750 kHz.

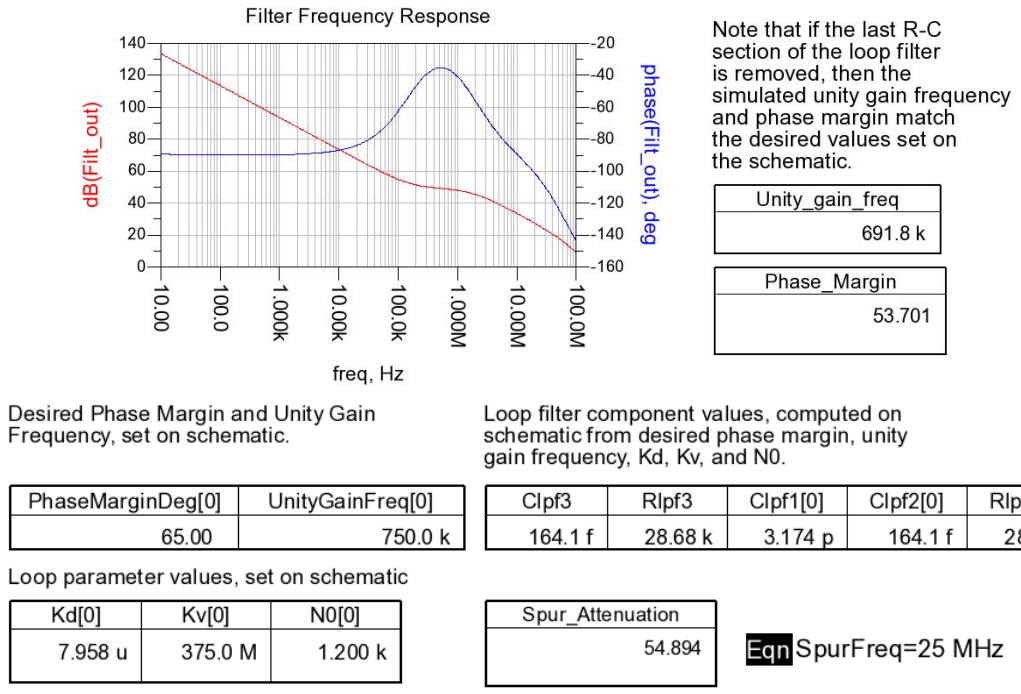


Figure 4.1-2 PLL loop filter example

The results shown in Table 4.1-1 correspond to several filter characteristics with cut-off frequency ranging from 100 kHz up to 1/10 of f_{REF}. Note that the last rows of the table contain capacitor values that are difficult to obtain with external components. These values can be increased by a factor of 10 if the charge pump current is also increased by a factor of 10.

Spec f_c	C_3	R_3	C_1	C_2	R_1	f_c	Ph.marg	Spur
kHz	pF	kΩ	pF	pF	kΩ	kHz	degrees	dBc
100	9.228	3.824	178.5	9.228	38.24	91.20	53.8	-98.41
250	1.476	9.559	28.56	1.476	95.59	229.1	53.7	-76.72
350	0.753	13.38	14.57	0.753	133.8	316.2	53.8	-69.57
500	0.369	19.12	7.141	0.369	191.2	457.1	53.7	-62.50
750	0.164	28.68	3.174	0.164	286.8	691.8	53.7	-54.90
1000	0.093	38.24	1.785	0.093	382.4	912.0	53.8	-49.70
2500	0.015	95.59	0.285	0.014	955.9	2291	53.7	-33.71

Table 4.1-1 Several loop filer characteristics for K_{vco} = 375 MHz/V, I_{CP} = 50 µA and N_0 = 1200

The cut-off frequency of the filter plays an important role in the overall phase-noise characteristic of the FS. The position of the cut-off frequency with respect to the phase noise level of the VCO and the reference determines the relative contribution of each of them to the total phase noise at the output of the PLL. Figure 4.1-3 shows the results of an optimization study where the goal is to minimize the total integrated phase noise. According to this figure, the optimum unit-gain frequency specification for the PLL loop filter is 350 kHz. Table 4.1-2 shows the phase noise data at various offset points for the 65 GHz mmW LO output and Figure 4.1-4 shows the phase noise profiles and the contributors for the same cases.

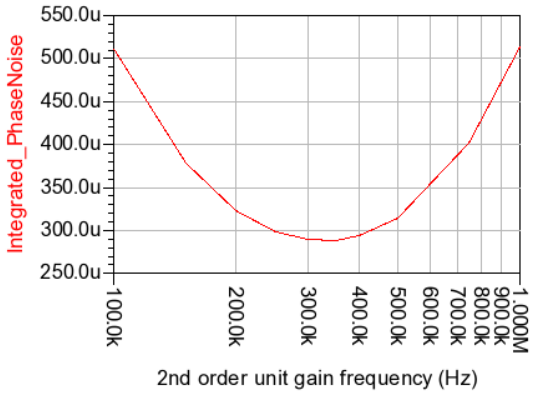


Figure 4.1-3 Integrated phase noise at the output of the 30 GHz VCO in closed loop for a sweep of specified unity gain frequency parameter

f_c	PN @10k	PN @100k	PN@1M	PN@10M	PN@1G
	dBc/Hz	dBc/Hz	dBc/Hz	dBc/Hz	dBc/Hz
100 kHz	-85.08	-79.31	-101.10	-121.31	-150.52
350 kHz	-88.77	-86.96	-98.02	-121.29	-150.52
1 MHz	-88.84	-90.06	-88.82	-119.60	-150.52
2.5 MHz	-88.84	-90.44	-87.89	-108.94	-150.52

Table 4.1-2 Phase noise values of the 65 GHz mmW LO output for K_{vco} = 375 MHz/V, I_{CP} = 50 µA and N_0 = 1200, Mixer NF=10 dB and various specified unity-gain loop filter frequencies

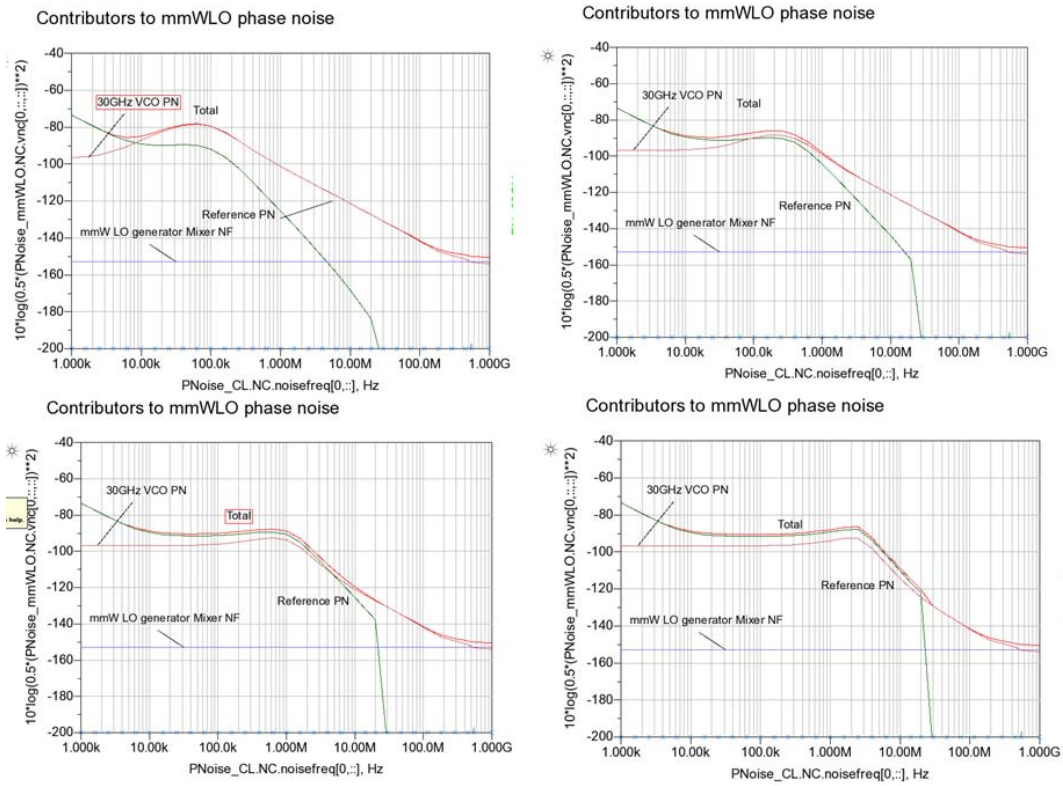
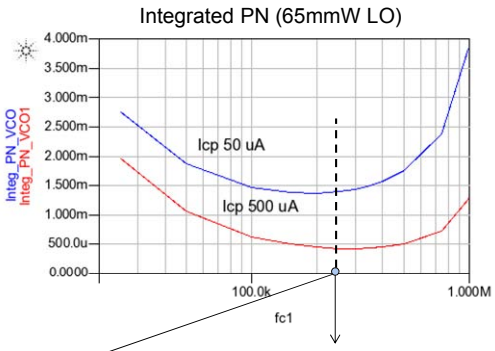


Figure 4.1-4 Phase noise contributors to the 65 GHz mmW LO output phase noise for increasing filter unity-gain frequency specifications (100 kHz, 350 kHz, 1 MHz and 2 MHz, from left to right and from top to bottom)

A final study has been performed regarding the loop filter and charge pump components sizing. There is a degree of freedom in the PLL loop design that consists on changing the charge-pump current. If it is multiplied by 10, the capacitor C1 and all the other become multiplied by 10 as well, which results in a reduction by a factor of 10 on the value of the loop filter resistors.



50 µA Charge Pump:
- Minimum Integrat. PN 1.4m
- C1 value: 28 pF, C2, C3 value: 1.5 pF
- R1 value: 95 kΩ

500 µA Charge Pump:
- Minimum Integrat. PN 420u
- C1 value: 285 pF, C2, C3 value: 15 pF
- R1 value: 9.5 kΩ

Figure 4.1-5 Impact of CP current and loop-filter resistors on integrated phase noise of the PLL

4.2 Updated IF LO generator results

The initial phase noise obtained with the previous IF LO generator resulted too high for allowing 64QAM modulation. A redesign of the IF LO generator has been made after identifying the source of the excess phase noise, which corresponded to the noise floor at medium offsets. This noise comes from the multiplication of the noise floor of the shaping circuit that generates the control signals needed to start and stop the pulsed oscillator. These circuits have been re-designed and the noise floor has been reduced from -120 dBc/Hz up to -126 dBc/Hz (DSB phase noise), as shown in Figure 4.2-1 for the 19.5 GHz IF LO frequency case.

Furthermore, the two ILOs have a low-pass characteristic regarding far offset phase noise floor, and contribute to reduce the noise floor for frequency offsets beyond that low-pass cut off frequency. In the case of the ILOs of the IF LO generator, the cut-off frequency offset is of 250 MHz. Since the signal bandwidth is very large, the contribution of the phase noise at far offsets has a significant impact on the Rx and Tx operation. The output level is 1 Vpp at the differential signal found at the output of the 2nd ILO (before the 50Ohms buffer of the prototype).

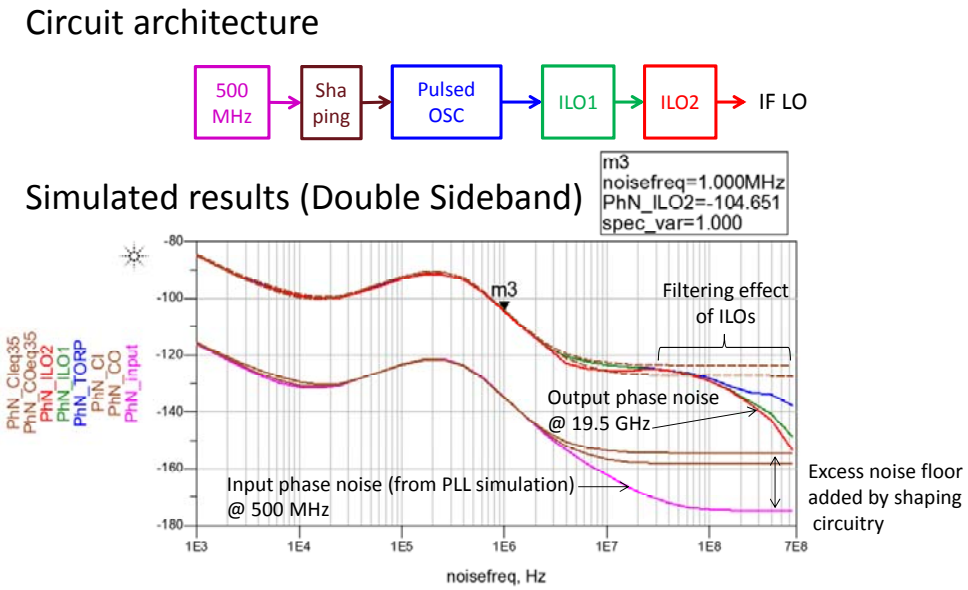


Figure 4.2-1 Simulation results of the phase noise characteristics of the IF LO generator of the FS for a specified loop filter unity gain frequency of 350 kHz and LO frequency of 19.5 GHz

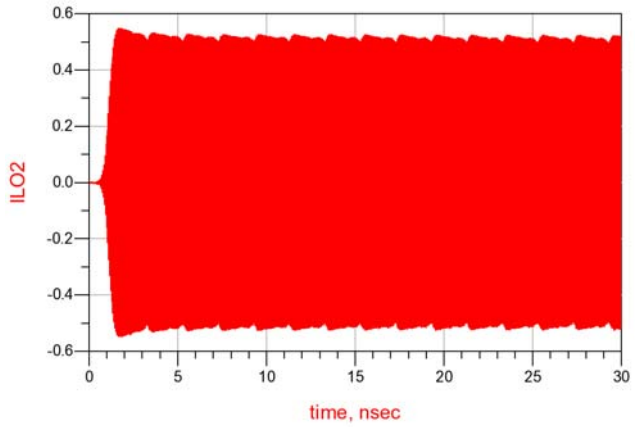


Figure 4.2-2 Output signal of the IF LO generator for LO frequency of 19.5 GHz

4.3 I/Q generator

The IF LO generator is completed with a poly-phase filter that generates phase and quadrature differential signals from the input mono-phase differential signal. This circuit will be integrated inside the Tx and Rx, close to the IF mixer. The circuit features a two-stage architecture, based on a basic stage of R-C networks as illustrated in Figure 4.3-1. The layout of the implementation of the two stages is shown next to it.

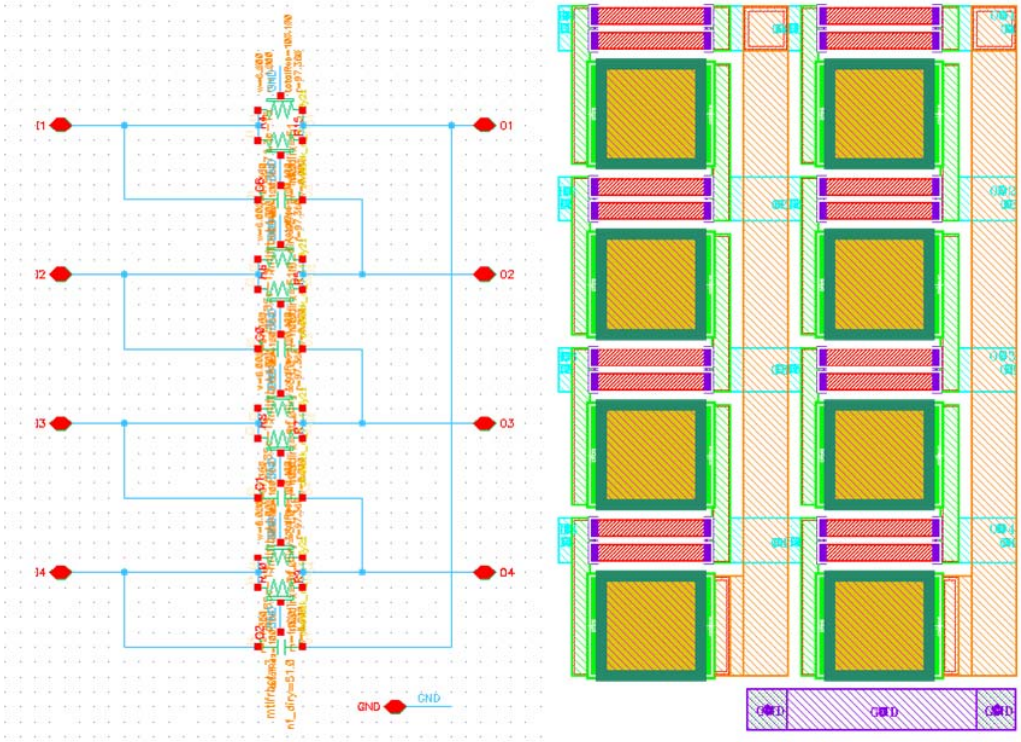


Figure 4.3-1 Circuit schematic of the basic stage of the poly-phase filter and the layout of the two stages

The simulations results for the two LO frequencies corresponding to 2 GHz bandwidth channels are shown below.

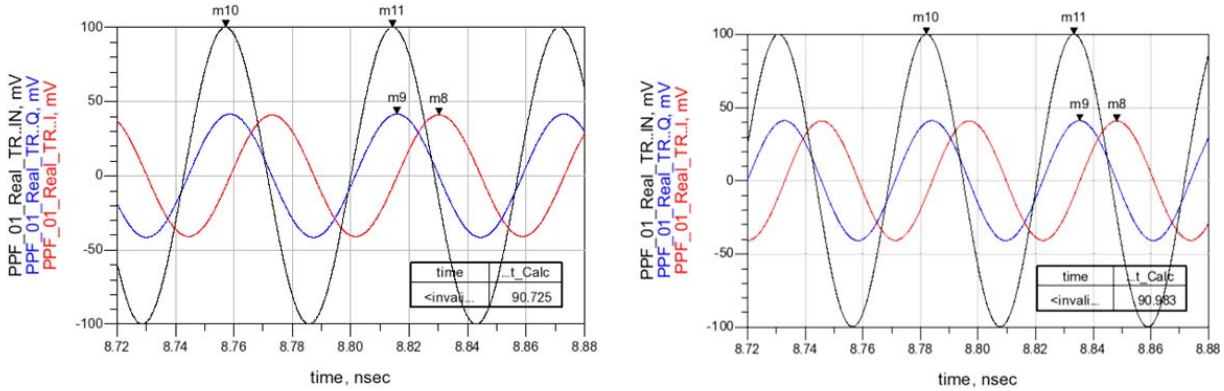


Figure 4.3-2 Simulated operation of the I/Q poly-phase generator for 17.5 GHz LO frequency (left) and 19.5 GHz LO frequency (right)

4.4 Updated mmW LO generator results

The mmW LO generator block, specifically the programmable selection section based on ILOs has been re-designed to improve the rejection of the non-wanted mmW LO spur and to improve the power consumption. It has been submitted to the 2nd run on BiCMOS55nm technology. Figure 4.4-1 shows the block diagram of the prototype including two ILOs in cascade, a 50 Ω differential input matching network and a 50 Ω differential output buffer. The first ILO is loaded by a buffer circuit, shown in Figure 4.4-2 (b). The second ILO is loaded by the same buffer followed by a 50 Ω stage, shown in Figure 4.4-2 (c).

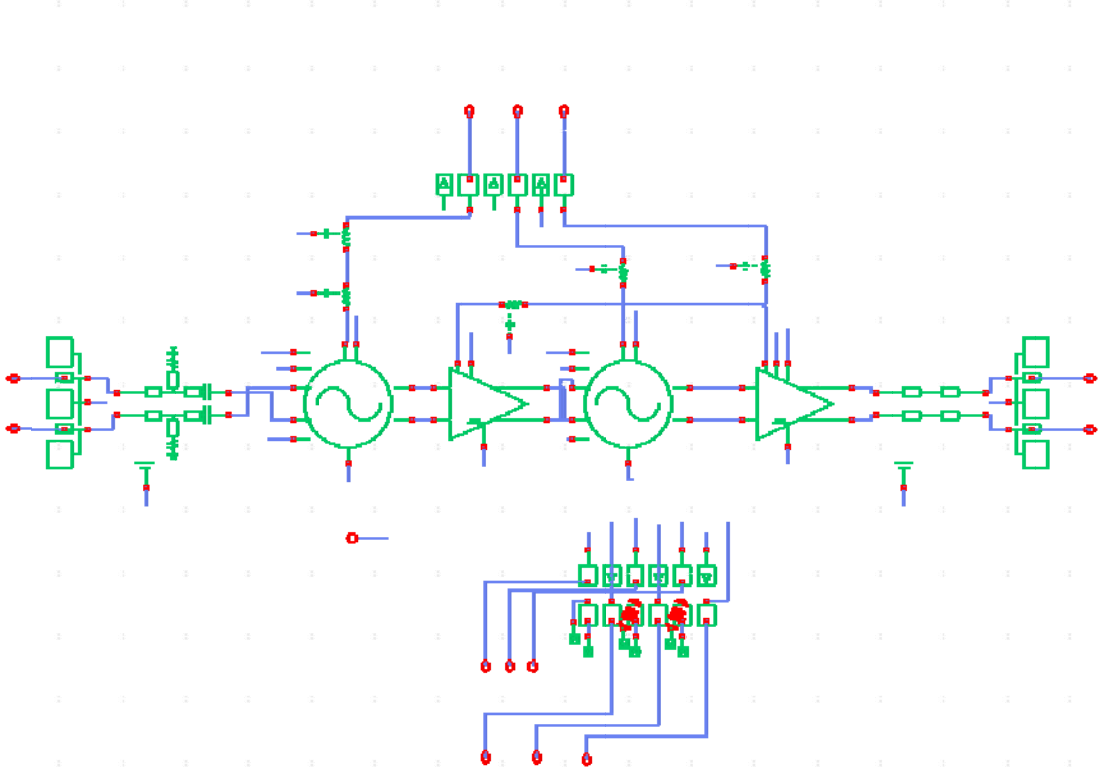


Figure 4.4-1 Block diagram of the mmW frequency selector section of the mmW LO generator

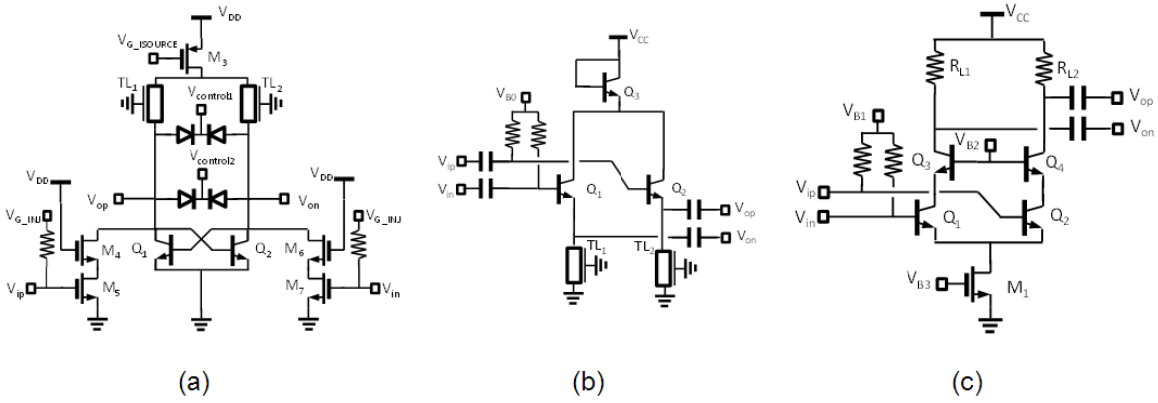


Figure 4.4-2 Schematics of the various circuits composing the mmW LO frequency selector

(a) ILO, (b) inter-ILO buffer stage, (c) 50 Ω output buffer stage

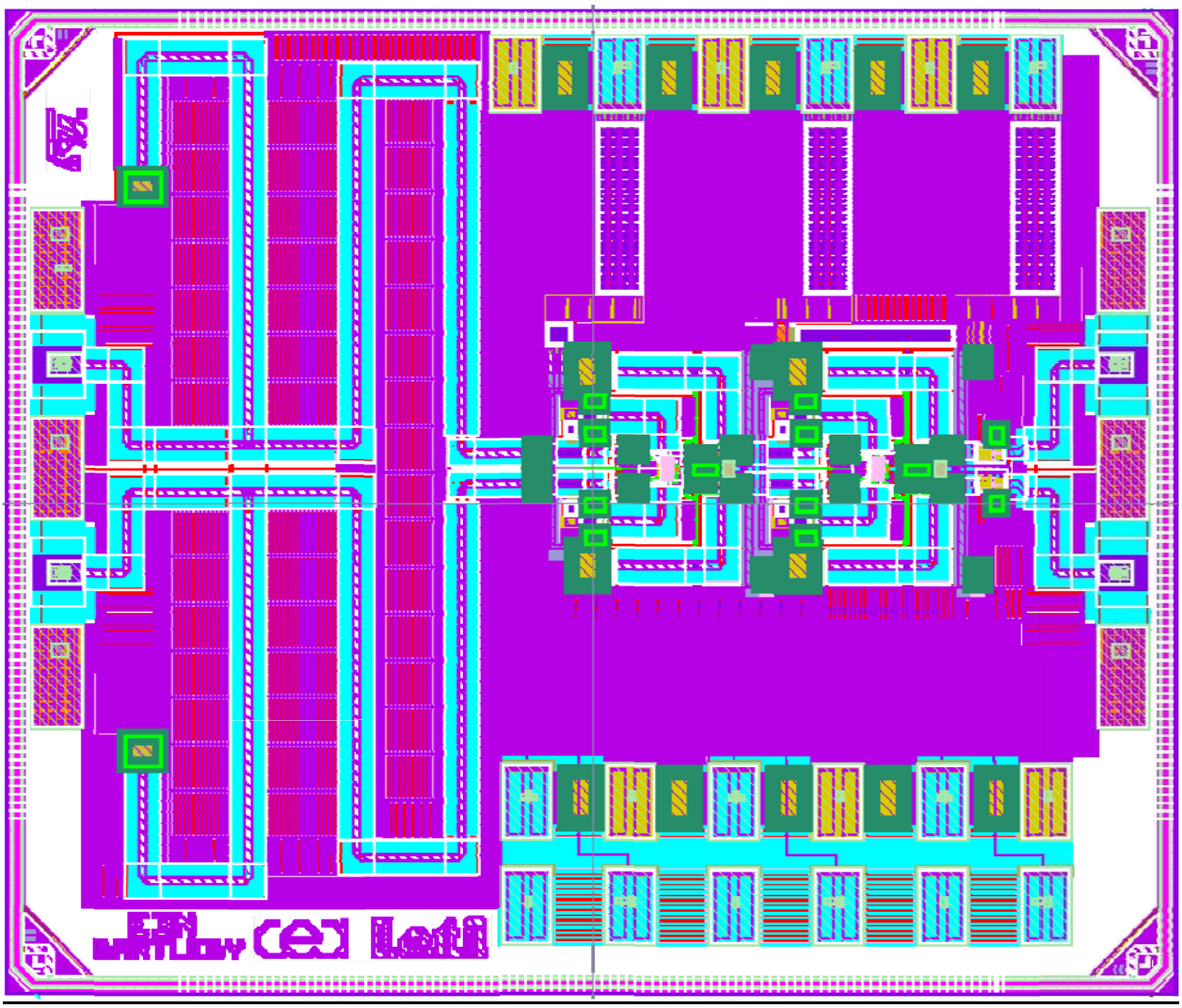


Figure 4.4-3 Layout view of the mmW LO frequency selector prototype

Figure 4.4-4 shows the output signal obtained with a -10 dBm input signal consisting in two tones at 55 GHz and 65 GHz for the two possible selection modes (red and blue). The rejection of the non-wanted mmW LO signal is greater than 30 dB en both cases. The output amplitude is 600mVpp for both cases.

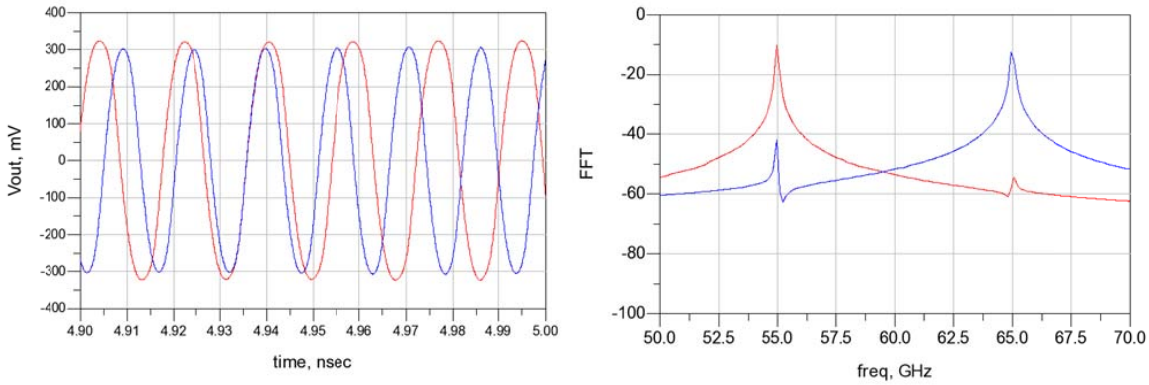


Figure 4.4-4 Time and frequency domain operation of the mmW LO frequency selector for a -10dBm input

In order to evaluate the impact of output buffers on the phase noise floor, another analysis has been performed. The data from the buffers to be used on the Rx and Tx have been used to add a last stage on the circuit schematic of the mmW LO frequency selection ILOs chain, as shown in Figure 4.4-5:

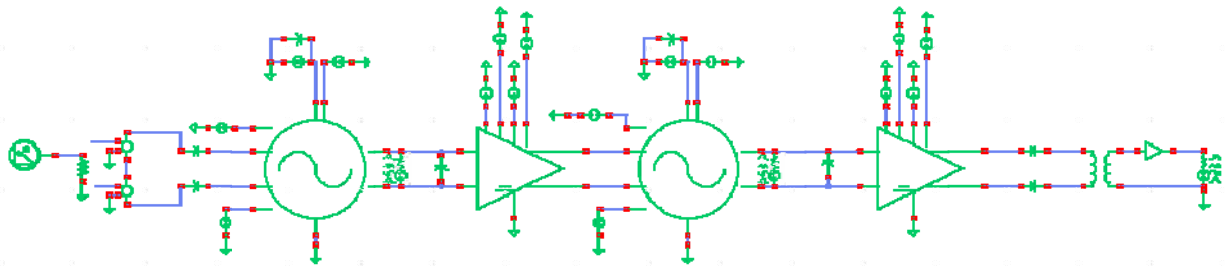


Figure 4.4-5 Test bench used for the simulation of the impact of the ILOs and the mmW LO buffer on the phase noise

The conclusion of this study is that the contribution of the buffers to the output phase noise depends on the input signal amplitude. For larger signal amplitude at the input of the ILOs chain, the impact on the phase noise floor is smaller. However, there is a trade-off with the rejection of the non-wanted mm LO signal at the output (note that the input signal contains the two LO frequencies, 55 GHz and 65 GHz but that the output signal must contain only one of the two tones). This trade-off is illustrated by Figure 4.4-6 and Figure 4.4-7.

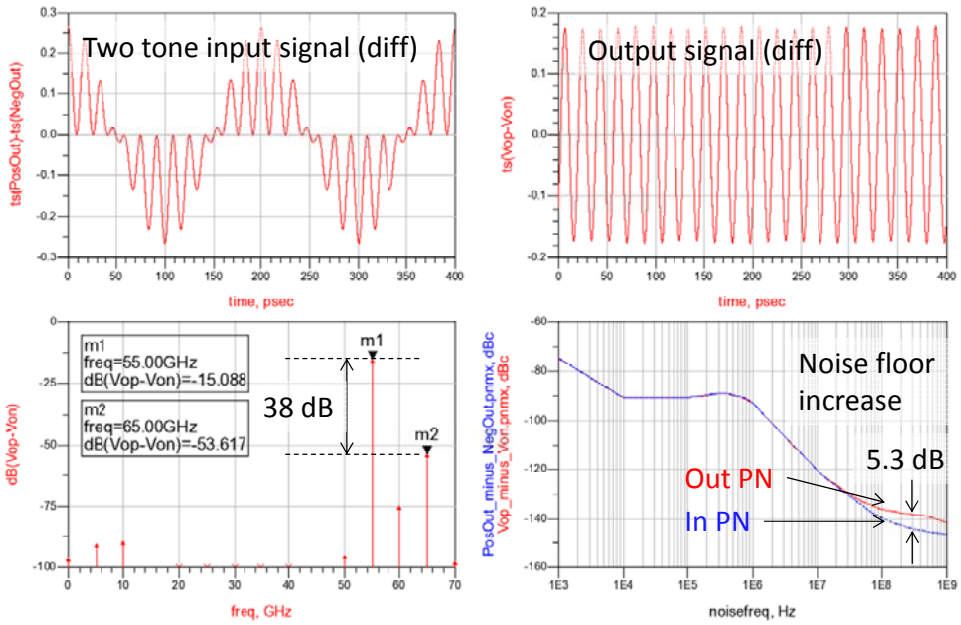


Figure 4.4-6 Results of phase noise and rejection of the adjacent LO freq. for the lower amplitude case

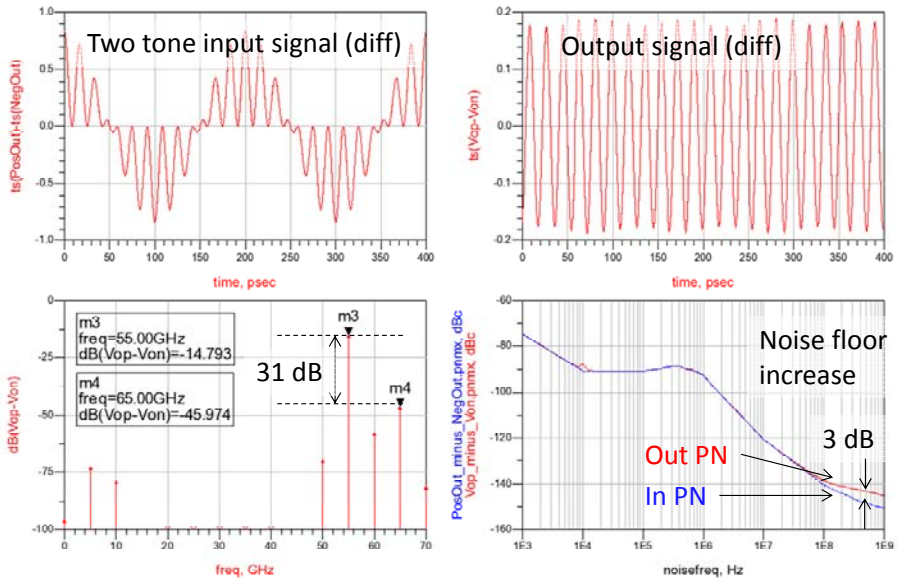


Figure 4.4-7 Results of phase noise and rejection of the adjacent LO freq. for the higher amplitude case

4.5 mmW LO two tones generator based on a mixer

The two-tone signal required as input for the mmW LO frequency selector is implemented using a Gilbert cell mixer as the one shown in Figure 4.5-1.

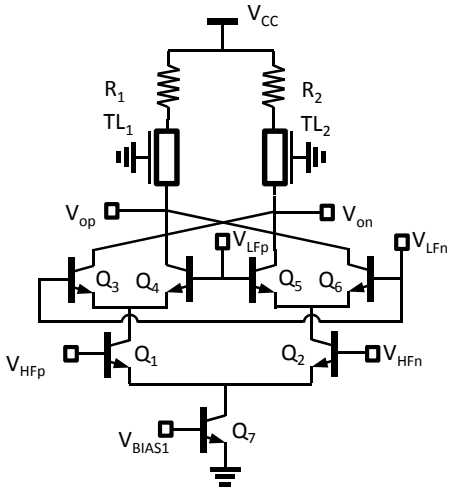


Figure 4.5-1 mmW LO two-tones generator based on a mixer

The circuit generates the two tones by mixing the 60 GHz frequency signal output by the doubler 30 GHz VCO of the PLL and the 5 GHz intermediate frequency generated also by the PLL after a division by 6 of the 30 GHz VCO frequency. Simulation results are shown in the next figures.

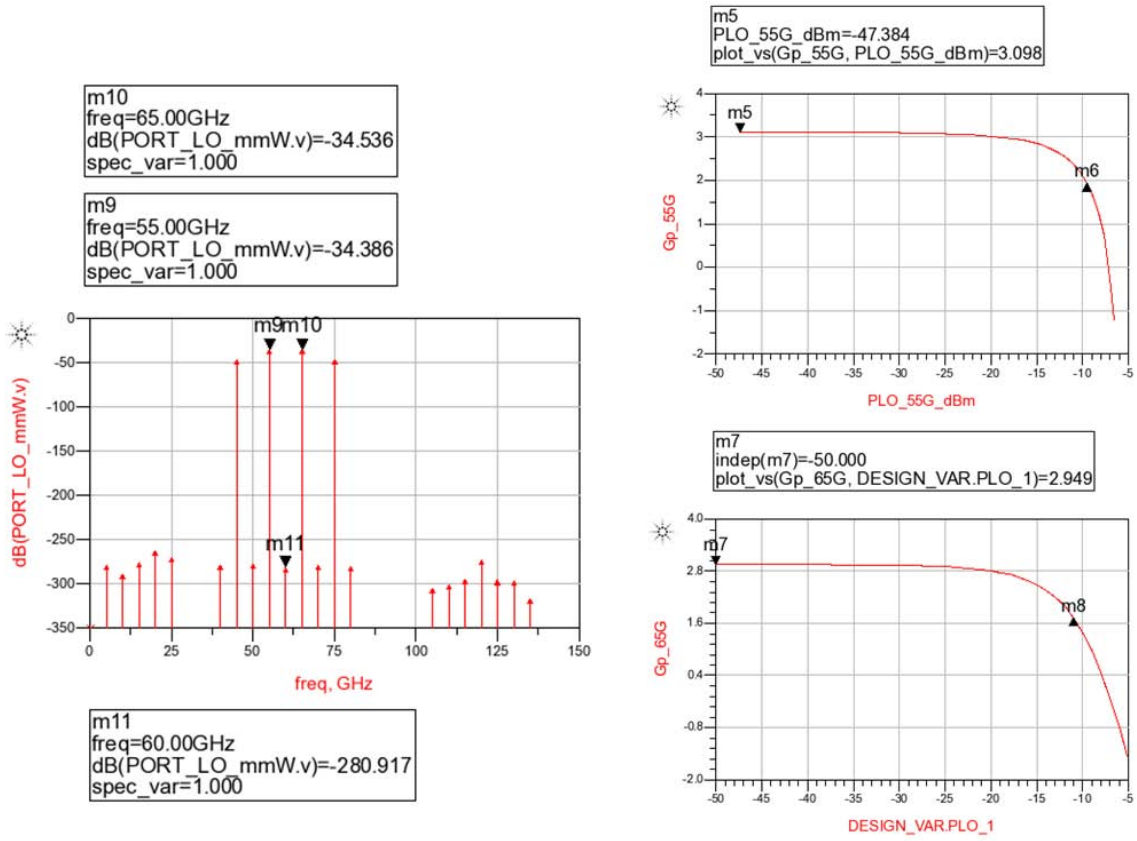


Figure 4.5-2 Frequency domain and conversion gain of the two-tones mmW LO generator

.

The noise floor of the mmW LO signals generated by the mmW LO two-tones for high offsets is limited by either the noise floor of the VCO inside the PLL or by the NF of the mmW LO generator mixer, depending on which is higher. The NF of the mixer has a different impact for different VCO power levels. Figure 4.5-3 and Figure 4.5-4 present the results of the behavioural simulations of the FS for different NF values and VCO power levels. A higher VCO amplitude results in a larger impact of the same NF value for the mixer.

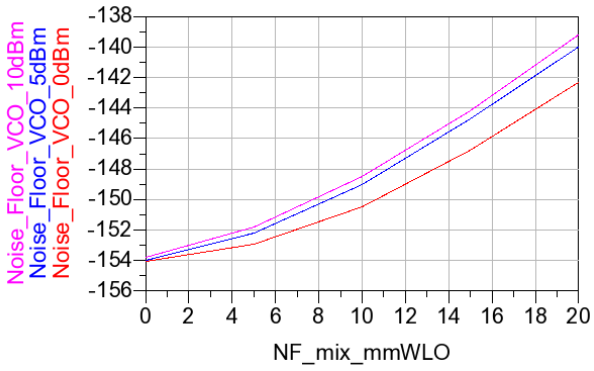


Figure 4.5-3 Impact of the NF of the mmW LO generator mixer and the VCO amplitude on the phase noise floor at large offsets of the 65 GHz mmW LO output

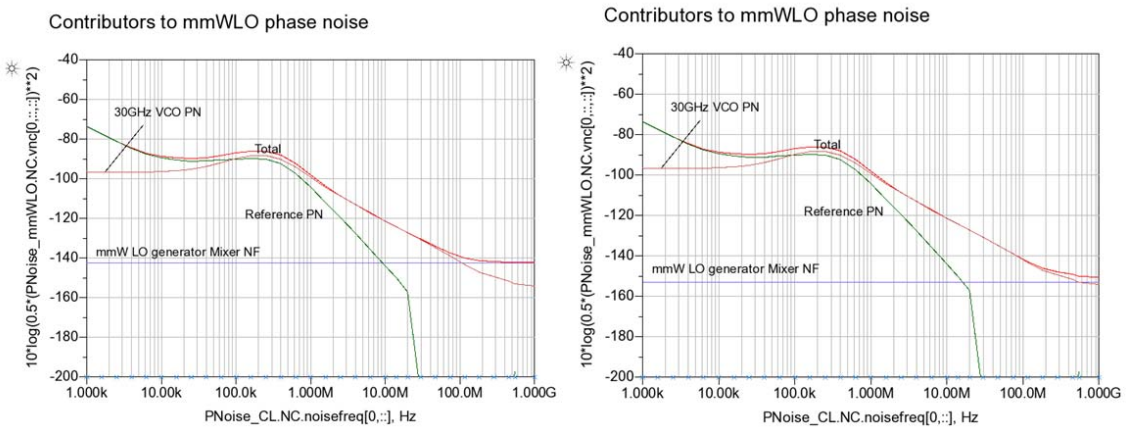


Figure 4.5-4 Impact of the NF of the mmW LO generator mixer and the VCO amplitude on the phase noise floor at large offsets of the 65 GHz mmW LO output; left NF = 20 dB, right NF = 10 dB

4.6 Overall Signal Generator Results

A behavioural model of the complete signal generator comprising the PLL and the IF and mmW LO generators has been implemented. The core of the model consists on the PLL loop plus some mixers, multipliers and dividers that generate the input signals to the IF and mmW LO generators. The phase noise at those intermediate signals is characterized and used as input for the post-layout, circuit level simulation of the ILO chains of the mmW and IF LO signal generators.

The goal of this model is to provide a simulation environment for the optimization and validation of the signal generator block in the context of the overall E-band Tx and Rx. The simulation results in terms of phase noise and signal levels are used as parameters for a Matlab model that allows to add phase noise to the system level simulation of the complete Rx and Tx, therefore allowing an investigation on the impact of the phase noise on the link operation as well as a validation of the compensation algorithms implemented in the digital baseband.

Figure 4.6-1 shows the block diagram of the PLL behavioural model including some additional blocks for the generation of the IF and mmW LO signal generators input signals.

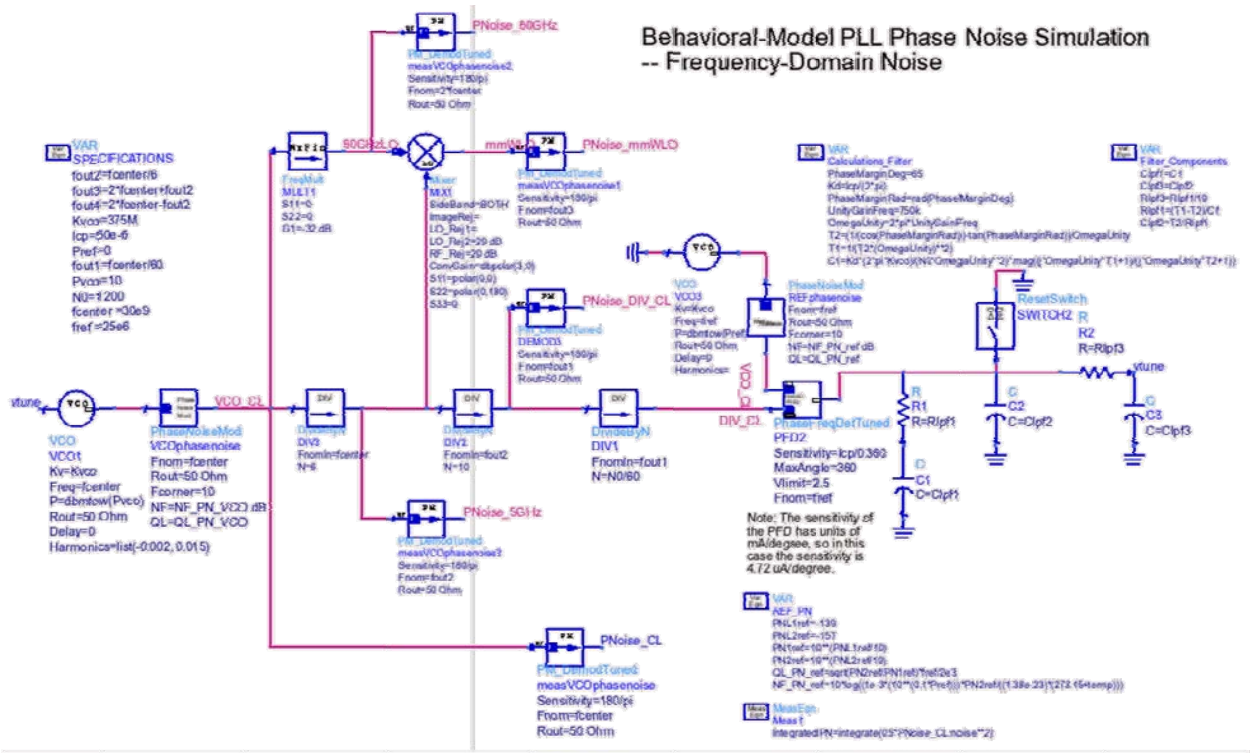


Figure 4.6-1 Block diagram of the behavioural model of the PLL and additional sub-blocks

Figure 4.6-2 shows an example of time domain loop locking transient and the spectrum of the 60GHz output signal including phase noise. The lock time is around 3ns. The variations after the locking are due to the phase noise introduced in the VCO and input reference oscillators.

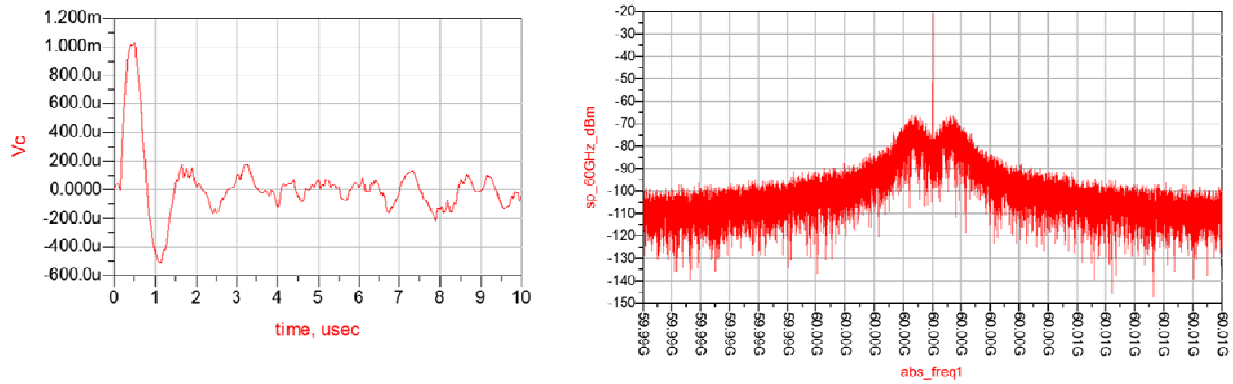


Figure 4.6-2 Locking transient simulation of the PLL and spectrum of the 60 GHz signal output, including phase noise

Figure 4.6-3 shows phase noise simulation results at various outputs of the behavioural model: the 65 GHz mmW LO output tone (before the mmW LO frequency selector), the 5GHz and 500 MHz output frequency signals and the open loop 30 GHz VCO phase noise model.

Figure 4.6-4 allows investigating the main contributors to the 65 GHz mmW LO frequency term phase noise. Note that the ILOs of the mmW frequency selector will not add phase noise to this signal.

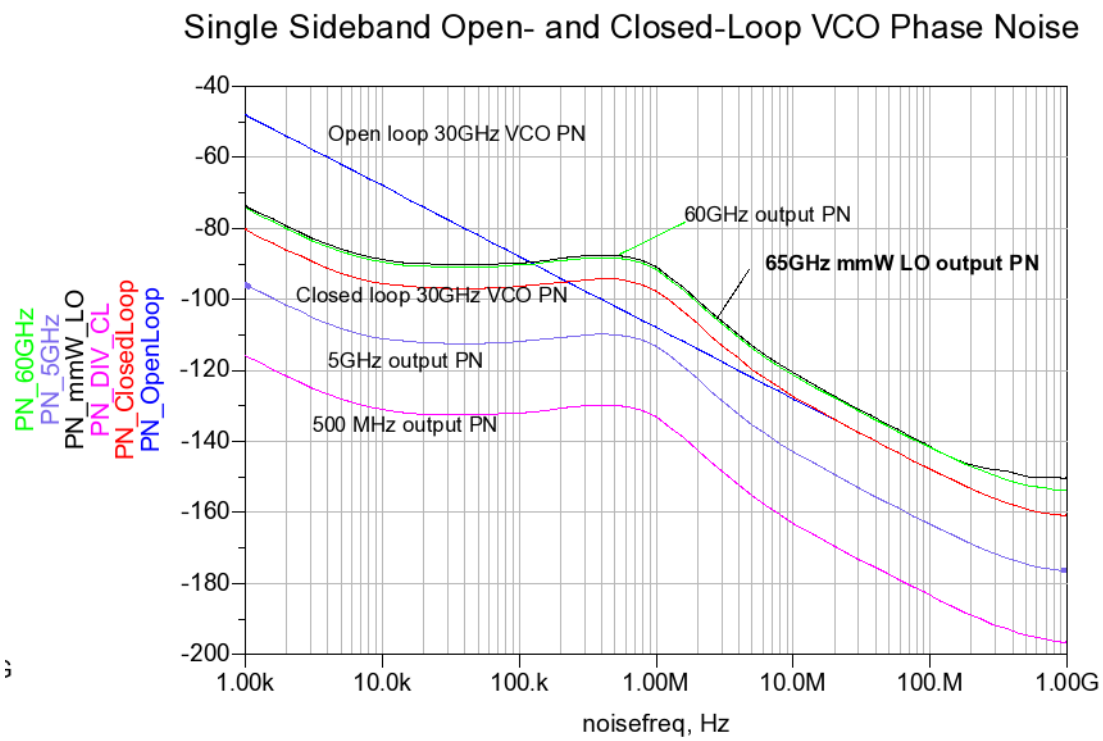


Figure 4.6-3 Single sideband phase noise at different outputs of the frequency generator for the 750 kHz loop filter case

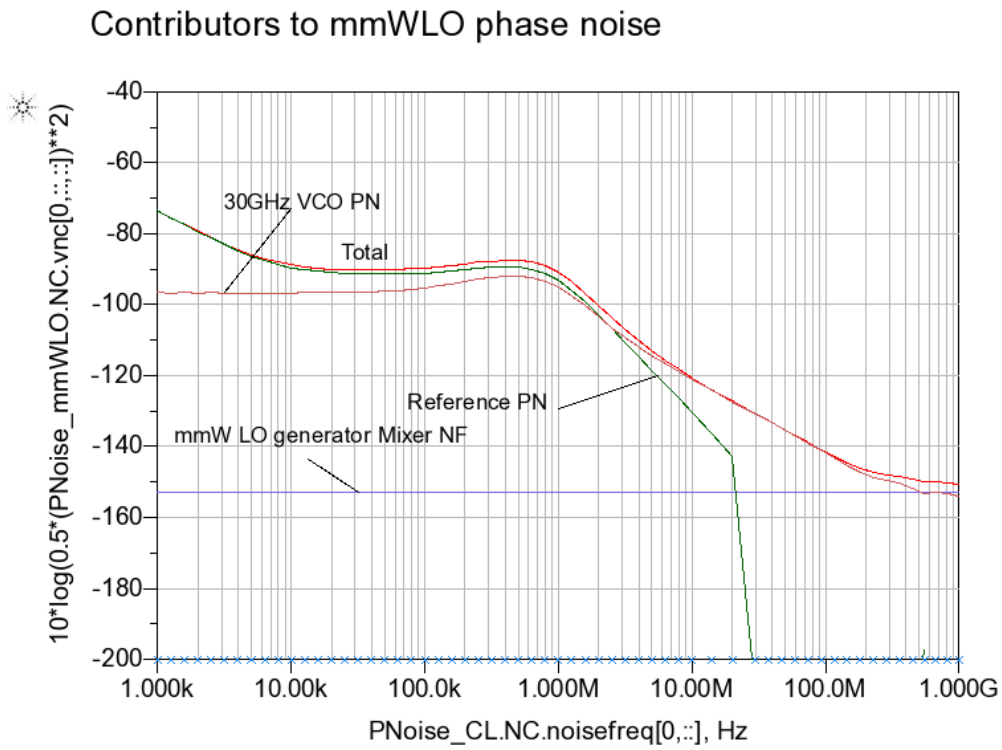


Figure 4.6-4 Analysis of the different contributors to phase noise at the 65 GHz mmW LO output of the frequency generator for the 750 kHz loop filter case

The phase noise profiles shown in the previous figures are modelled in Matlab in order to allow for system level studies of the impact of the phase noise on the overall Rx/Tx and even in a complete link including modulation, transmission, reception, demodulation and detection, with specific algorithms implemented in digital baseband to compensate for various RF and analog impairments such as frequency and phase drift, I/Q mismatching and phase noise. The implementation of such phase noise generation process is illustrated in Figure 4.6-5. The final results of the frequency generator block can be summarized with Figure 4.6-6.

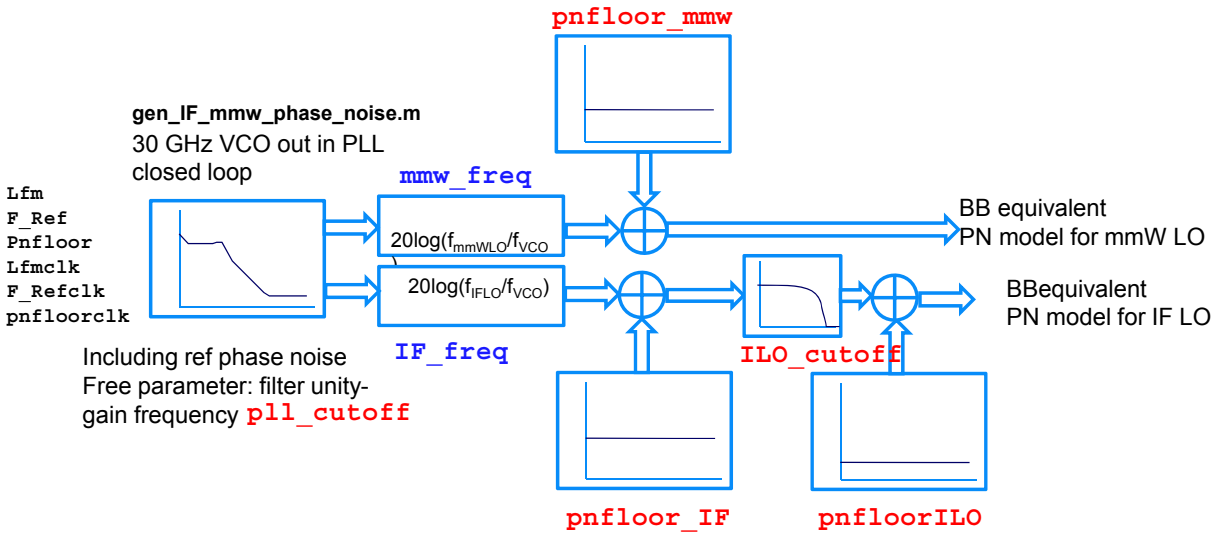


Figure 4.6-5 Illustration of the Matlab process for generating phase noise profiles for system level simulations from the signal generation phase noise results

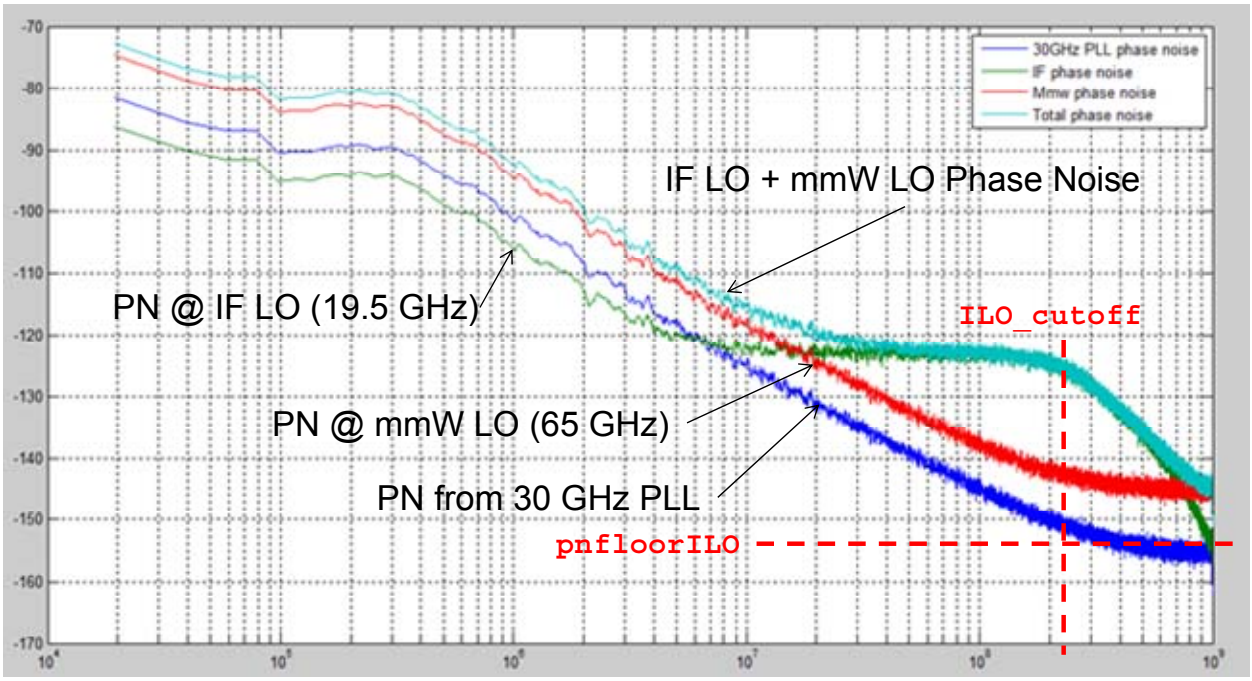


Figure 4.6-6 Matlab phase noise model including all phase noise sources for mmW and IF LO outputs of the signal generator

Table 4.6-1 and Table 4.6-2 show a comparison between the resulting performance of the various blocks of the signal generator and the updated specifications of D.1.2.2. Note that all phase noise values are obtained based on the phase noise of the 60 GHz output of the PLL, as obtained by system level simulations including the phase noise of the 30 GHz VCO and frequency doubler output presented in D.2.1. Note that the results concerning phase noise have been transformed in single-sideband noise from the double-sideband results shown in some of the figures above in order to compare them with the specifications, which were defined as single-sideband phase noise.

Parameter	Spec	Result	Units	Fulfilled
SSB Phase noise @ 1Mhz, IF LO for 64QAM (16-21 GHz)	-105	-108	dBc/Hz	Yes
1st SSB Phase noise floor, below ILO cut-off, IF LO for 64QAM (16-21 GHz)	-126	-129	dBc/Hz	Yes
ILO filter cut-off freq., IF LO for 64QAM (16-21 GHz)	250	250	MHz	Yes
2nd SSB Phase noise floor, IF LO for 64QAM (16-21 GHz)	-155	-159	dBc/Hz	Yes
Upper frequency channel (2 GHz BW)	17.5	17.5	GHz	Yes
Upper frequency channel (2 GHz BW)	19.5	19.5	GHz	Yes
Output level (before 50 Ohms buffer)	0.5	1.0	Vpp	Yes

Table 4.6-1 Summary of simulation results for the IF synthesizer

Parameter	Spec	Result	Units	Fulfilled
Frequency range	55-65	55-65	GHz	Yes
SSB Phase noise @ 10Mhz, mmW VCO for 64QAM (60 GHz)	-123	-117	dBc/Hz	No
SSB Phase noise floor, mmW LO for 64QAM (55/65 GHz)	-130	-147	dBc/Hz	Yes
Output Level	>-5	-3	dBm	Yes
Rejection to non-wanted LO freq.	-	>30	dBc	-

Table 4.6-2 Summary of simulation results for the mmW synthesizer

5. DAC & ADC RESULTS

5.1 DAC

The design effort has been focused on developing the testing platform for the designed DAC. The goal is to have a testing platform compatible with the FPGA board (the same used for the digital base band) that allows the DAC characterization. To achieve this goal, custom lead frame, test board and FPGA firmware have been developed.

5.1.1. Circuit description

Custom lead frame: Several options were analyzed for packaging the DAC samples. The idea is to minimize the parasitic series inductance added by the package in the DAC outputs. In order to accomplish this, the original idea was to use BGA package. After initial enquiries on this, it was realized that the cavity size of existing BGA boards for the high number of IOs was too high for the size of the device, leading to high series inductance due to long bondwires, apart from the potential manufacturing problems for long bondwires. The development of a customized BGA package was rejected because it was beyond the scope of this project. Therefore, a custom solution has been the chosen option. This custom solution is built using alumina as substrate. The assembly consists of two stacked boards, of which the top one has a window to place the DAC die inside. The concept can be seen in Figure 5.1-1.

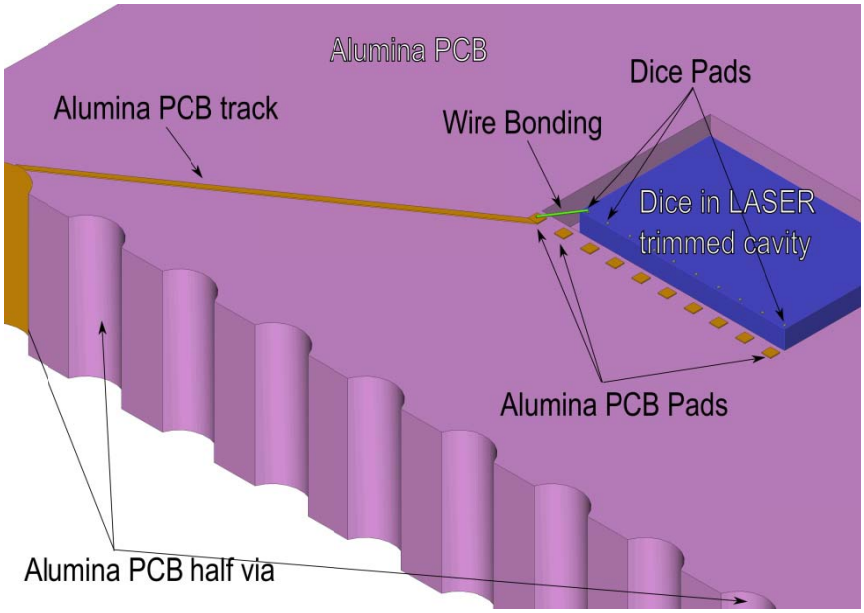


Figure 5.1-1 Two stacked alumina custom lead frame concept

The soldering to the test board will be done using half vias placed all around the perimeter of the alumina assembly, as shown in Figure 5.1-2.

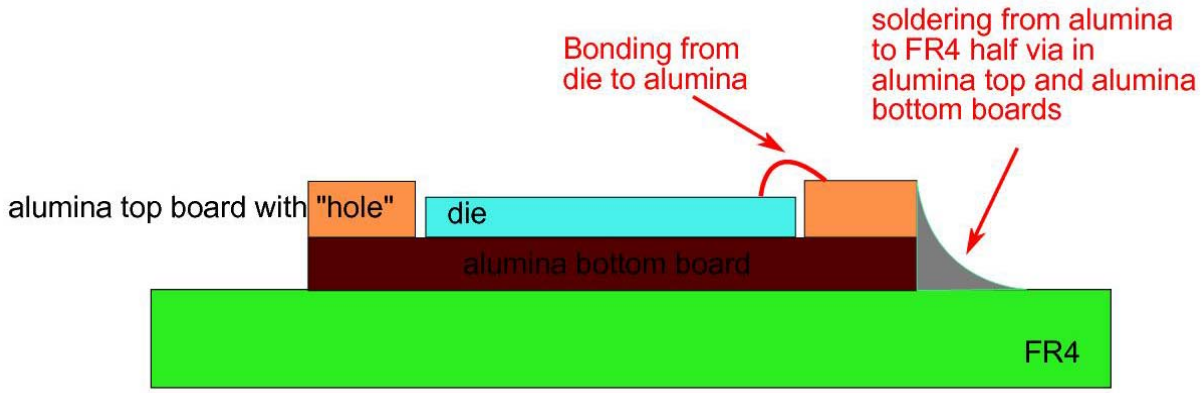


Figure 5.1-2 Detail of DAC lead frame soldering to test board

Figure 5.1-3 shows the complexity of the bonding work due to the big amount of signals to be connected.

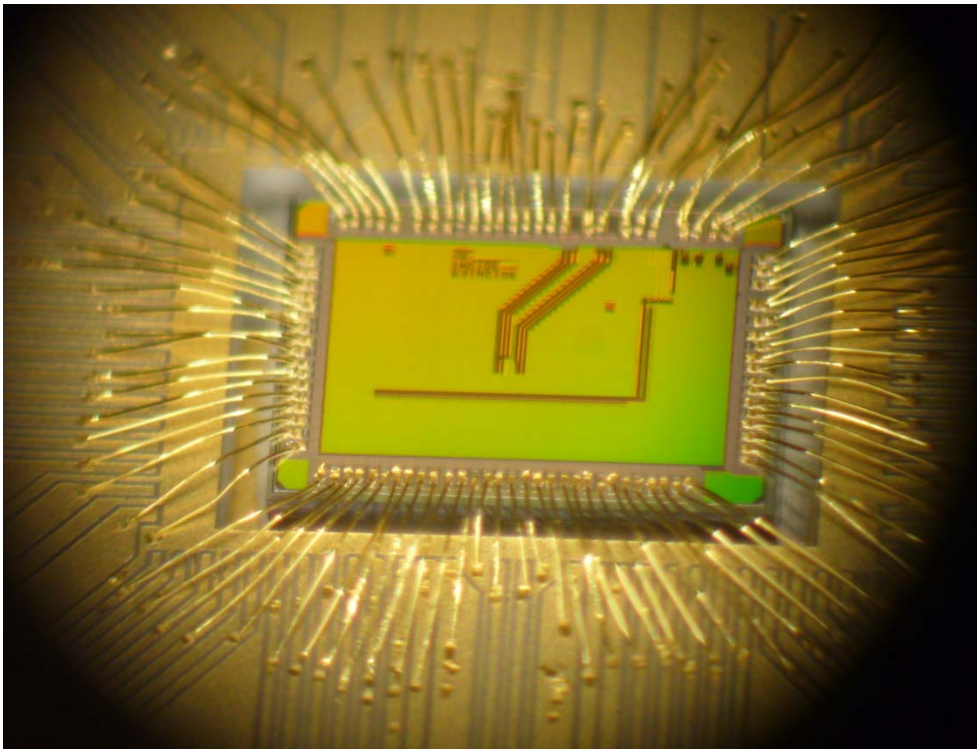


Figure 5.1-3 Detail of DAC bonding

Test board: The test board is designed using *Mentor Graphics Expedition PCB* and *Mentor Graphics Hyperlynx* to ensure signal integrity. It uses 8 layers, through all vias and blind vias. It is designed following ANSI/VITA 57.1 standard, and it incorporates all the needed circuitry to characterise the integrated DAC: Test points, current sensors, configuration jumpers… All components have been selected considering that they can be acquired in small quantities and that they have short delivery time, so that the schedule of the project is not compromised.

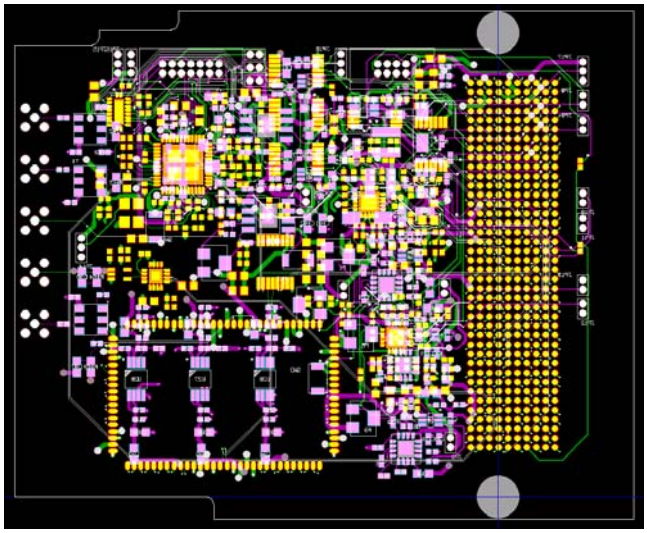


Figure 5.1-4 DAC test board layout

Additionally, the test board has been designed in standard FR-4 and special care was taken during the design to avoid noise propagation between different parts of the circuit. The circuitry was designed to be connected to the VC707 Evaluation Board using the HPC (high pin count) FMC connector.

Instrumentation selection: The required instrumentation was identified and it is ready to be used during the DAC validation. Remarkable items in this list are a 26.5 GHz spectrum analyzer (Agilent E4440A) and a 2.25 GHz oscilloscope (Agilent Infiniium 54846A).

FPGA code development: The needed FPGA code was developed to generate the test patterns for the DAC characterization. The developed FPGA code can provide sinusoidal and sawtooth signal at different frequencies. Furthermore it can adjust small delays between clock coming from the DAC and provided data signals.

5.1.2. Results

Signal integrity analysis: To minimise signal integrity issues, *Mentor Hyperlynx* was used to analyse not only the test board layout, but the custom lead frame as well. Furthermore a whole system FPGA board – DAC test board – custom DAC lead frame – DAC was simulated. Post-layout simulation results have been used to improve the test board layout, until the signal integrity simulations are acceptable.

Preliminary analysis allows determining test board layout restrictions needed to avoid signal integrity issues. This preliminary analysis results can be seen in the next figures.

Figure 5.1-5 shows signal at the DAC LVDS pads coming from the testing board FMC connector.

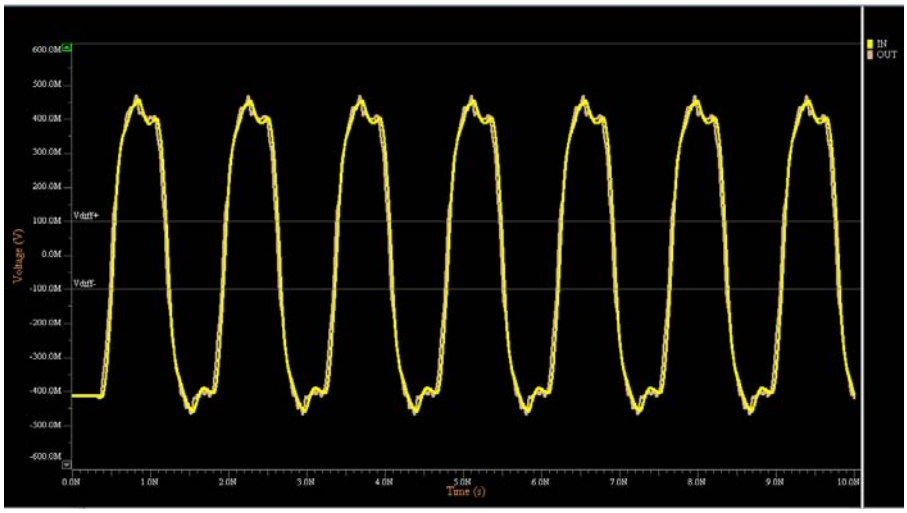


Figure 5.1-5 Signal integrity simulation including test board and custom lead frame. Signal reaching the integrated DAC LVDS pads from FMC connector

Figure 5.1-6 shows the 2.8 GHz clock signal reaching the DAC, coming from the frequency synthesizer.

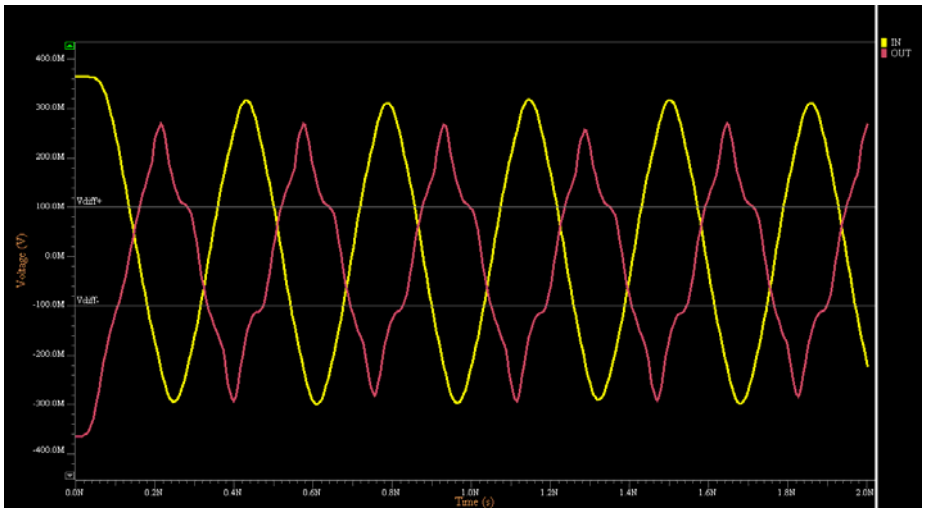


Figure 5.1-6 Signal integrity simulation including test board and custom lead frame. Frequency synthesizer 2.8 GHz clock reaching the DAC

Figure 5.1-7 shows cross talk analysis. Victim signals blue (output signal) and pink (input signal) are placed surrounded by two aggressor LVDS signals (green, orange, yellow and light blue). As it can be seen the victim signals are not affected by the aggressor ones.

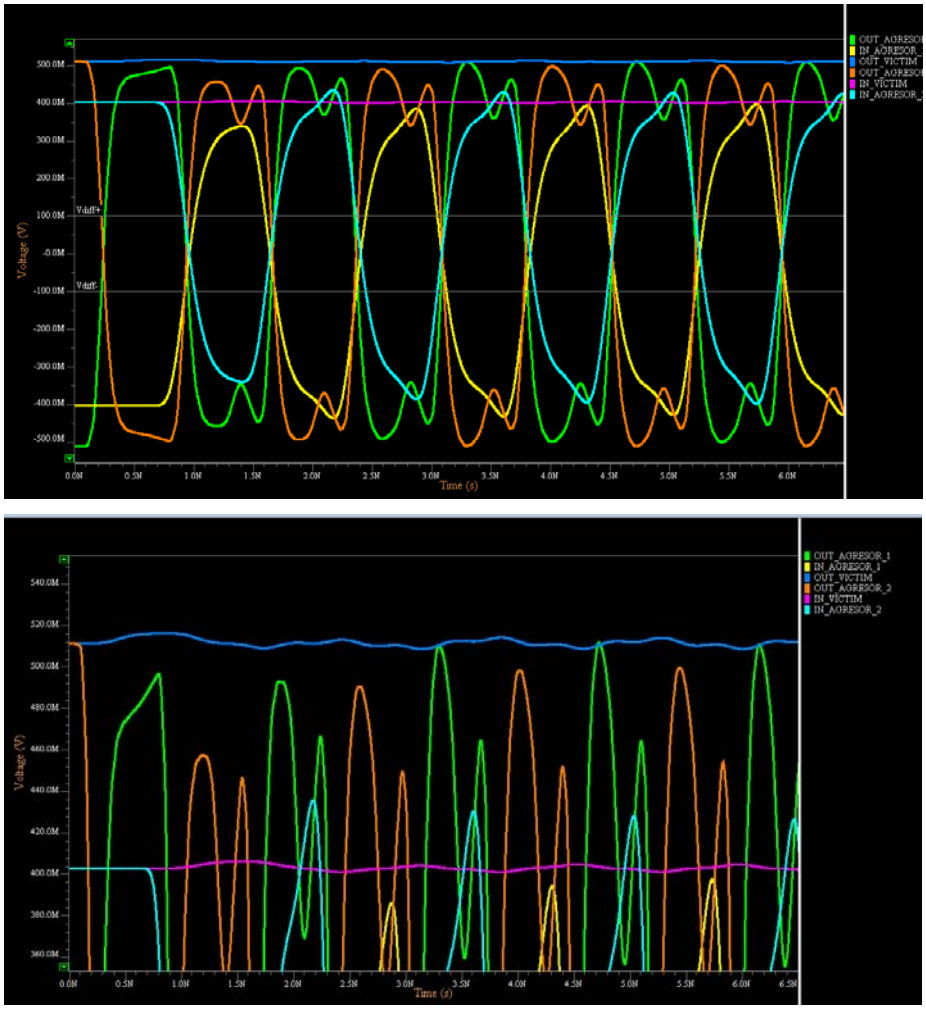


Figure 5.1-7 Signal integrity simulation including testing board and custom lead frame. Cross talk analysis.

One important topic in signal integrity is to minimise skew between data signals. Maximum allowed skew was simulated using *Hyperlynx* and introduced to the *Expedition PCB* restrictions to ensure correct timing between data signals. As can be seen in Figure 5.1-8, zigzag routing technique was used to compensate data signal skew.

Figure 5.1-8 Detail of zigzag routing technique to compensate data signal skew

Signal integrity analysis is an iterative process. Once the board is fully routed, new signal integrity analysis is performed using the final board layout to model the board behaviour. If needed, the layout is slightly modified to improve the behaviour.

5.2 ADC

5.2.1. Circuit description

The ADC is based on two sub-ADCs, each of those operating at half the total sampling rate, preceded by a single sample and hold circuit operating at the full sampling rate. The use of a single sample and hold increases the requirements for this circuit in terms of bandwidth, but compared to the solution with two interleaved ADCs having each of those a half sampling rate sample and hold, it eliminates the inherent problems to synchronize both ADCs.

Each of the two sub-ADCS has pipeline architecture, made up of seven 1.5-bit MDAC stages followed by a 2-bit Flash ADC. A Digital Core cell is also foreseen, which synchronizes the outputs of the different MDAC stages and offers a digital error correction for some physical effects appearing inside the ADC.

The main sample-and-hold is based on a flip-around architecture in order to enable low power consumption, while still reaching good performance in terms of noise, gain, dynamic range and distortion behaviour. Bootstrapped switches are used in order to reduce the clock-feedthrough, to make it signal independent and to improve linearity.

The overall block diagram is depicted in Figure 5.2-1; apart from the blocks mentioned above, voltage and current reference blocks are available, as well as a clock distribution block. The clock distribution block has turned out to be a very critical block, which carefully optimized can improve the overall signal-to-noise ratio. The overall circuit is completed by input clock buffers, and output LVDS buffers for clock and data transmission.

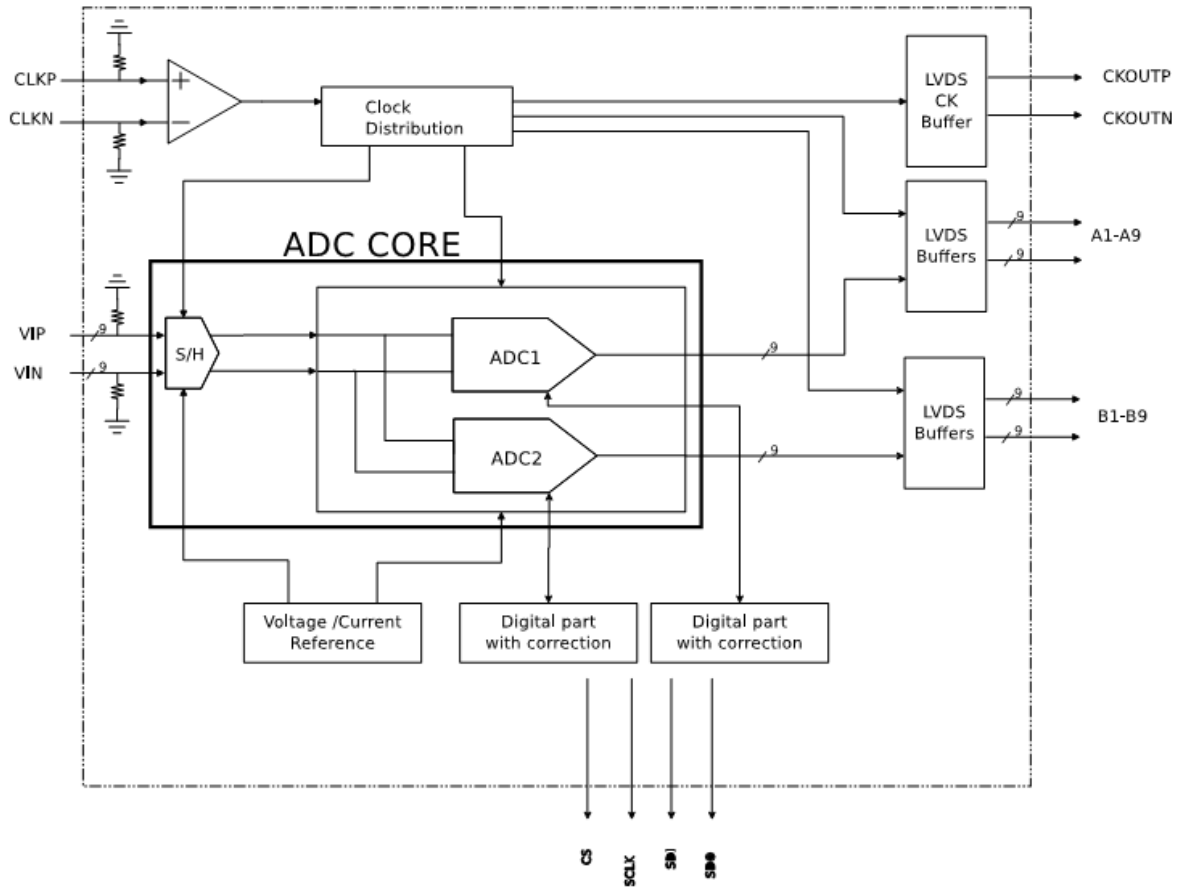


Figure 5.2-1 ADC block diagram

The digital correction is thought as a static foreground calibration technique, which corrects errors due to capacitor mismatch, gain error and op-amp non-linearity. The calibration procedure is based on injecting some accurate DC signals at the test input of the ADC, and measuring the outputs at intermediate points in the ADC. The calibration is therefore “static”, so that the synthesized digital part does not need to operate at high clock rates, and therefore the power consumption does not need to be high. The prototype circuit is thought in a way that the coefficients will be calculated off-line, and written into the Digital Core using the available SPI interface. The SPI interface can also be used to program different calibration values inside the ADC.

5.2.2. Results

The simulation results obtained with the design including all real blocks are presented in this section.

Figure 5.2-2 shows the dynamic behaviour of the ADC for an input signal of 1GHz and a sampling frequency of 2.8Gsps.

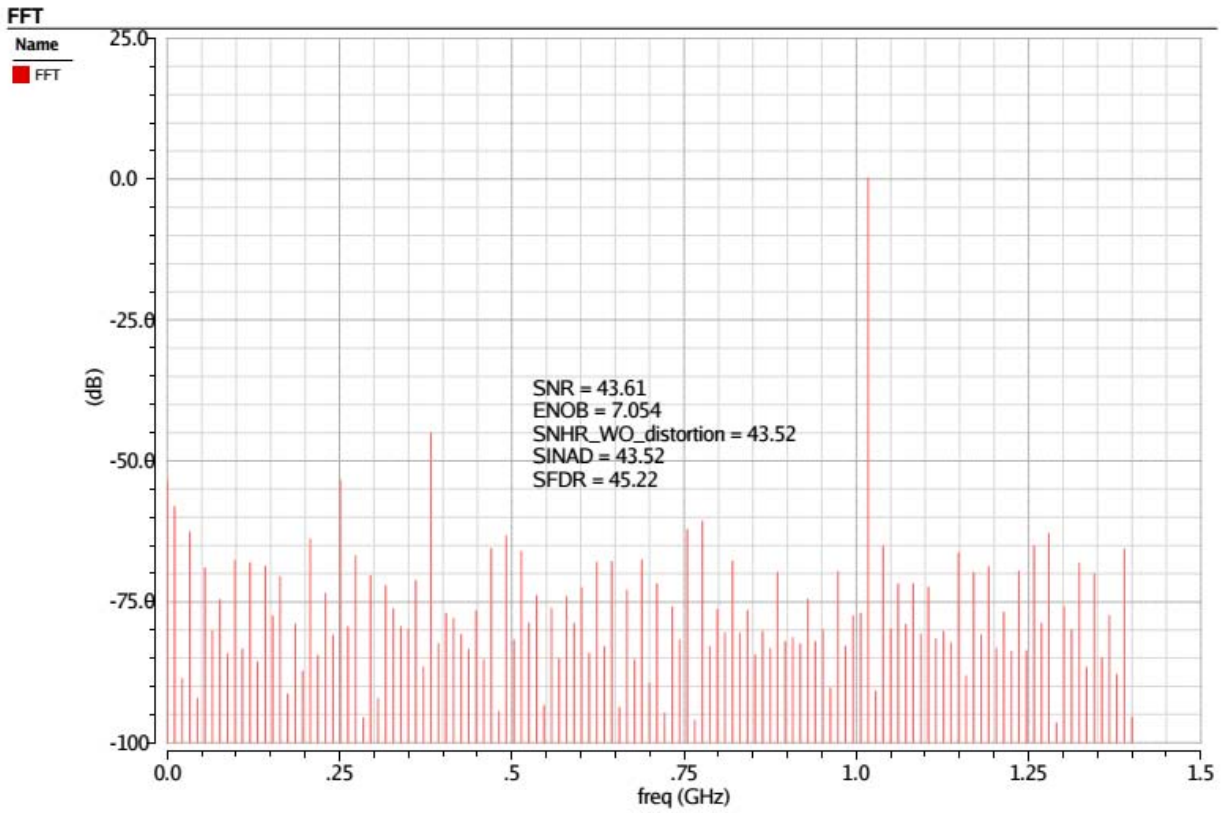


Figure 5.2-2 ADC dynamic performance

Figure 5.2-3 shows the input-output transfer curve of the ADC.

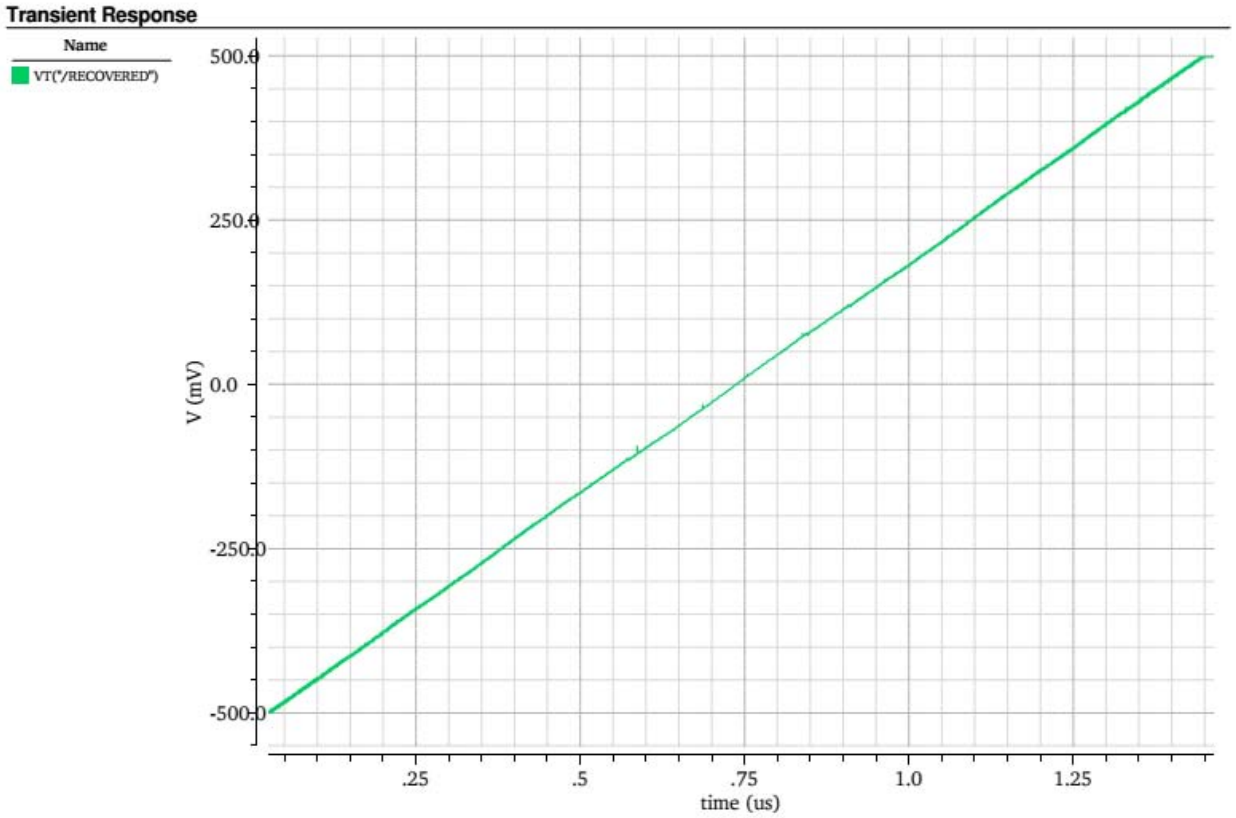


Figure 5.2-3 ADC input-output transfer curve

The complete results obtained so far are summarized in Table 5.2-1. These results are reported without using the digital error correction techniques. It is expected that applying such correction techniques will bring the ADC results inside the specifications.

Parameter	Simulation result			Units	Conditions	Spec. met?
	Min	Typ	Max			
Power consumption				W		YES
Max input voltage		500		mV		YES
Input bandwidth	1			GHz	Simulations run only up to 1GHz; input bandwidth is higher	
Sampling frequency		2.8		Gsps	Simulations have been run at 2.8Gsps	YES
Latency		32		Clock cycles		YES
Resolution		9		bit		YES
ENOB		7.0		bit	At 1GHz and 2.8Gsps	NO
INL		2.1		LSB		YES
DNL		0.9		LSB		NO
SFDR		45		dBc	At 1GHz and 2.8Gsps	NO
SINAD		43		dB	At 1GHz and 2.8Gsps	NO

Table 5.2-1 Summary of simulation results for the ADC

6. SYSTEM LEVEL SIMULATION

In order to assess the impact of the above simulation results in the overall system performance, system level simulation has been performed. Figure 6.1-1 shows the BER performance in the same scenario as in Section 3.1.1.6 of D3.2, but with the RF frontend parameters updated with the results presented above. No significant degradation is observed with respect to the result presented in D3.2.

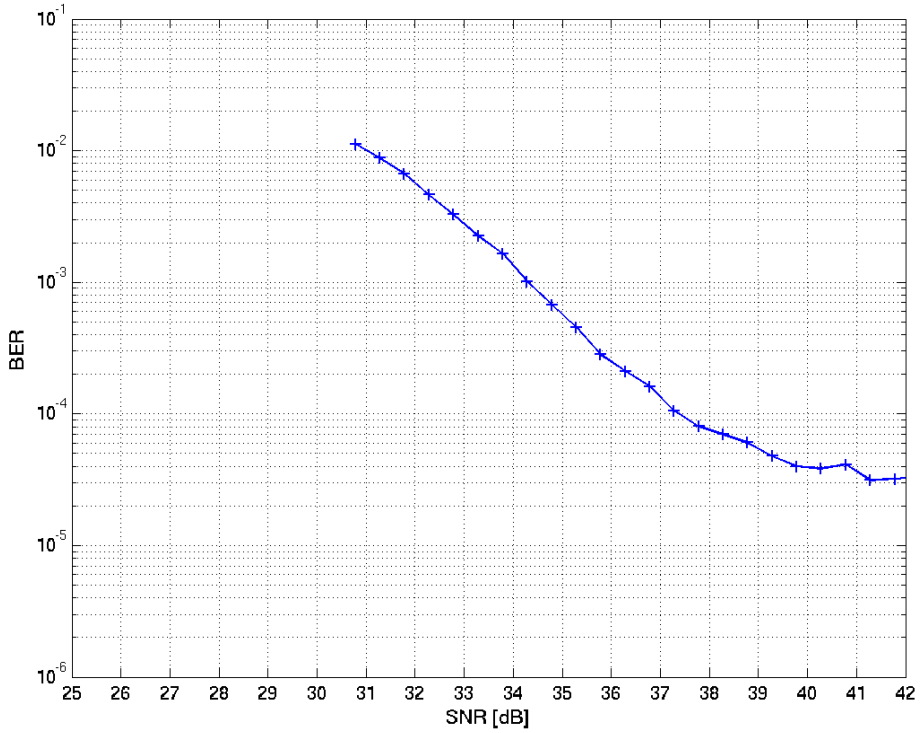


Figure 6.1-1 Impact on BER performance of overall RF impairments on configuration 2dbbx1aif (two digital subbands) with a DC-notch at the transmitter with a bandwidth of 3MHz. The x-axis is the SNR at receiver antenna port.

7. EARLY PROTOTYPE OF IF TRANSCEIVER

The idea behind the IF transceiver early prototype is to provide to WP3 a hardware platform where they can test with real hardware all the implemented modulation and demodulation algorithms. It can also be a good platform to start testing the different healing techniques. The early prototype of the IF transceiver includes all the sub-assemblies that are necessary to carry the analogue base-band signal conditioning and I&Q analogue modulation to an IF channel with a maximum bandwidth from 16 to 21GHz. The IF I&Q down-conversion and demodulation modules are also included in the prototype. The basic characteristics of this early prototype are:

UP-CONVERTER

- INPUT Baseband maximum through flow on I&Q branches: 10Gbit/sg
- INPUT average level on I&Q branches: -8dBm
- OUTPUT frequencies for IF output: 16 to 21GHz
- OUTPUT maximum bandwidth: 2GHz
- OUTPUT average level: -9dBm
- OUTPUT typical harmonics & spurious rejection: >38dB
- OUTPUT Image Rejection Ratio (IRR): typical >35dB
- TOTAL typical GAIN: -1dB

DOWN-CONVERTER

- INPUT frequency: 2GHz BW channel on 16 to 21GHz Band
- INPUT level: typ. -17dBm
- OUTPUT level in I&Q branches: -12dBm typ.
- OUTPUT Image Rejection Ratio (IRR): typical >38dB (min. 35dB)
- TOTAL typical GAIN: 5dB

Next section describes the architecture of the early prototype of the IF transceiver in order to implement the described basic characteristics.

7.1 Architecture description

Figure 7.1-1 and Figure 7.1-2 show the block diagram and the implementation of the IF early prototype, which was planned to include the necessary healing devices in order to detect and heal the I & Q imbalances.

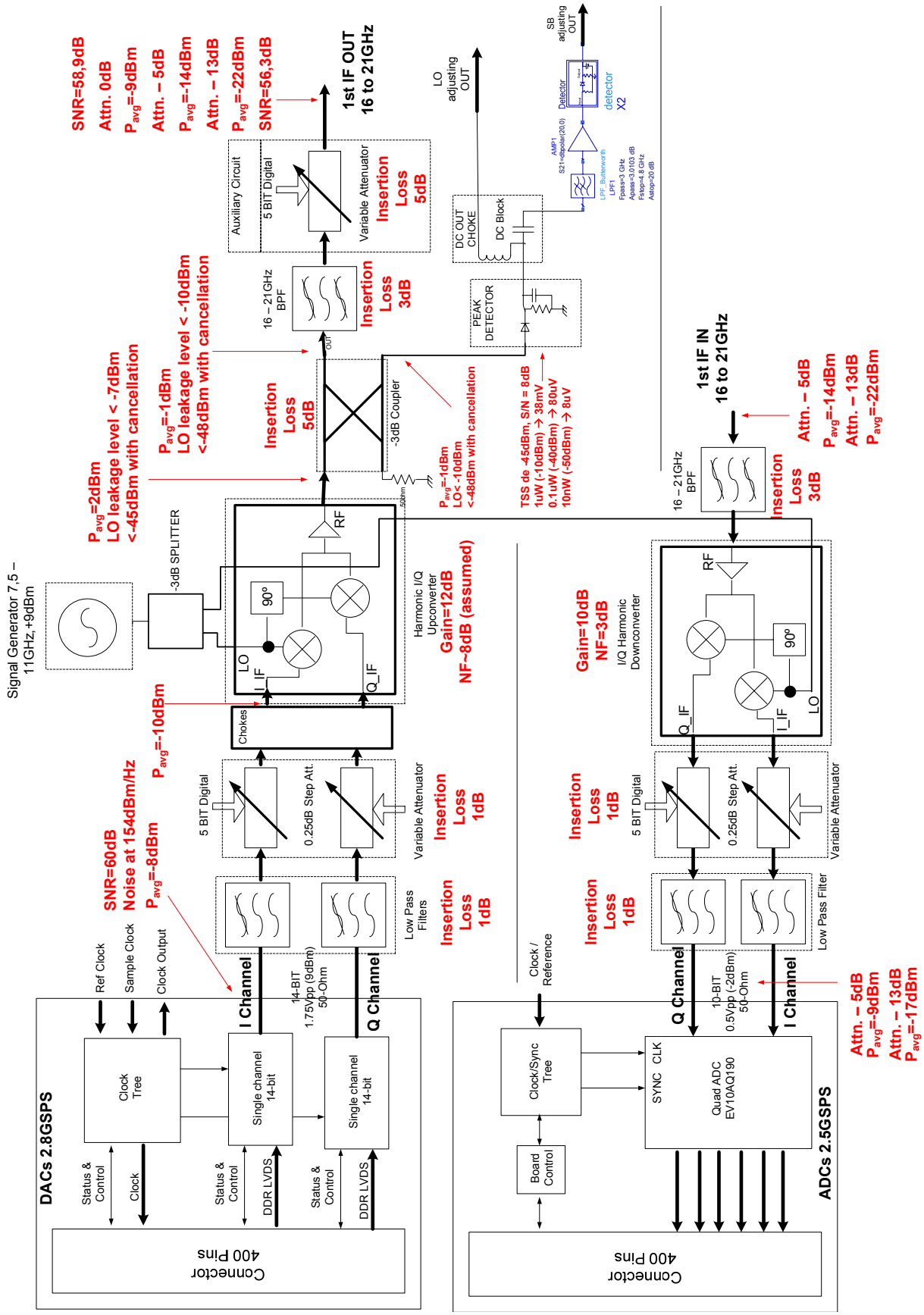


Figure 7.1-1 Block diagram of the IF transceiver prototype

As shown in Figure 7.1-2 , the prototype is constructed over a FR-4 base board (PCB), which is in charge of distributing the power supply to the different modules.

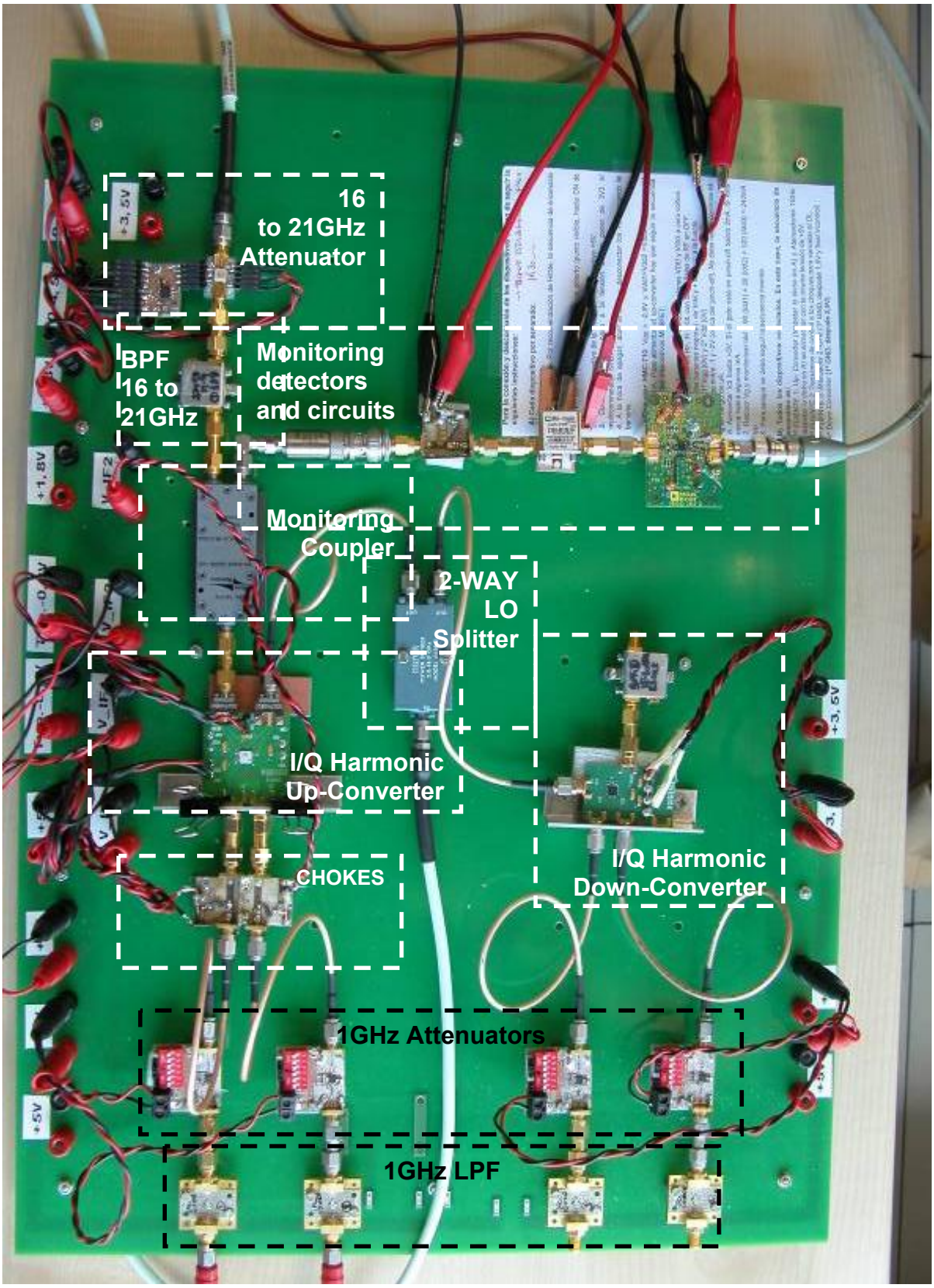


Figure 7.1-2 Photograph of the implemented IF transceiver prototype

Section 7.2 presents the measurement results that characterize this early IF prototype, in a step-by-step manner, beginning with the Up-Converter and ending with the Down-Converter devices.

7.2 Results

7.2.1. Base Band Low Pass Filters

As shown in Figure 7.1-1 , the first component in the Tx and Rx analogue signal chain is the low pass filter (LPF) after the DACs and before the ADCs. As described in deliverable D2.1 the filters LFCN-1000 and LFCN-1000D from Minicircuits were the ones selected. The filters are based on a LTCC (Low Temperature Co-fired Ceramic) technology. Figure 7.2-1 shows the measured S-parameters of the LPFs from 10MHz to 12GHz. 4 samples of each filter model have been measured. Measured results agree with the filter datasheet and as shown in Figure 7.2-2, no significant differences were observed concerning amplitude and phase between the different filters, which is important in order to estimate the gain and phase imbalance of the signal path in the IQ modulator and demodulator. The maximum measured gain and phase imbalance in the signal bandwidth were lower than 0.08/-0.03dB and ±2.7º respectively at 1GHz.

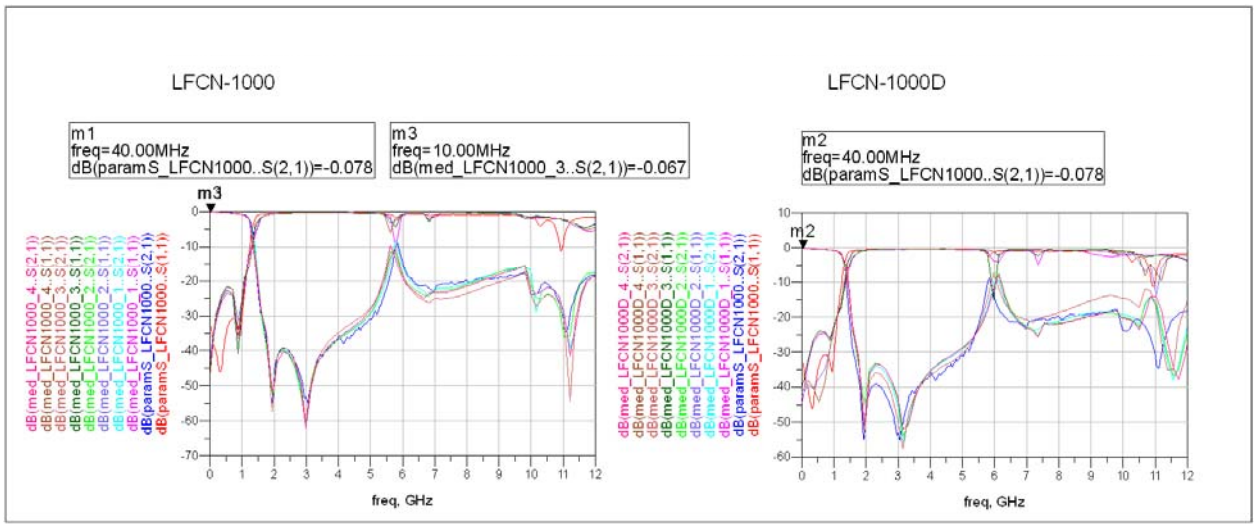


Figure 7.2-1 Measured S-parameters of the baseband LPF LFCN-1000

7.2.2. Base Band Attenuators

As shown in Figure 7.1-1 , the next component in the Tx and Rx analogue signal chain is the baseband attenuator. By selecting the attenuation value in each path (I&Q), non frequency selective amplitude imbalances can be corrected in steps of 0.25dB. It will also be possible to adjust the signal level in the Tx chain. Figure 7.2-3 shows the measured S-parameters of the selected attenuator. As shown, the 3-dB bandwidth of the attenuator is well above 1GHz.

Figure 7.2-4 shows the measured amplitude and phase difference between two measured samples. As shown, the amplitude difference is smaller than 0.04dB and the phase difference is below ±0.14º. The low frequency behaviour shows a pole around 150MHz. This is due to the DC block capacitor of 100pF, placed at the input and at the output of the attenuator. As shown in Figure 7.2-5, when changed to 100nF the low frequency pole goes well below 1MHz without degrading the high frequency attenuator characteristics (f<4GHz).

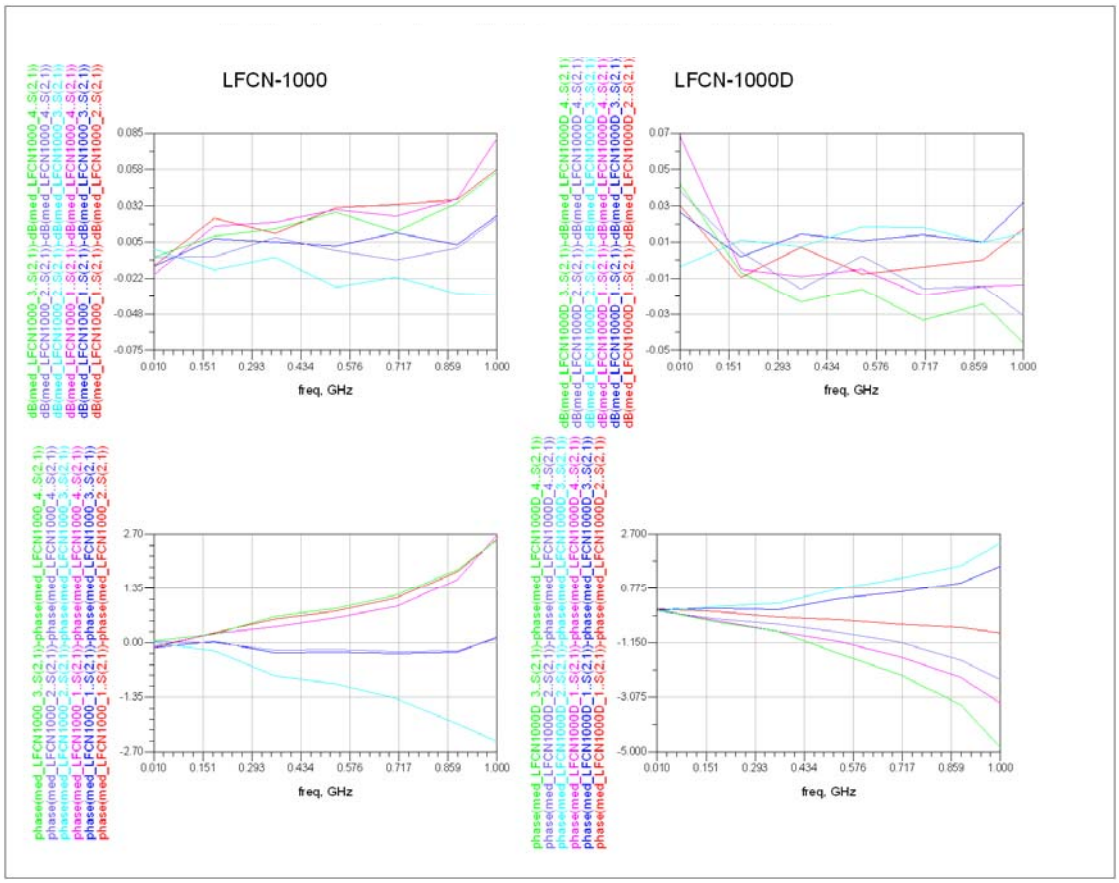


Figure 7.2-2 Amplitude and phase imbalance between the measured filters

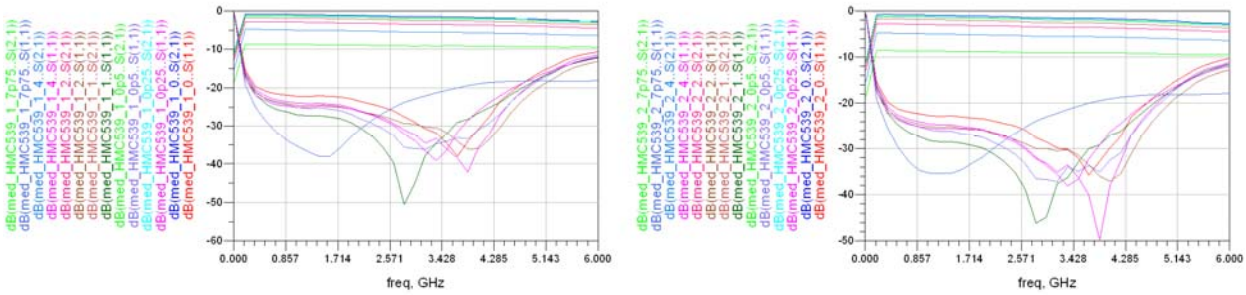


Figure 7.2-3 Measured S-parameters of the attenuator

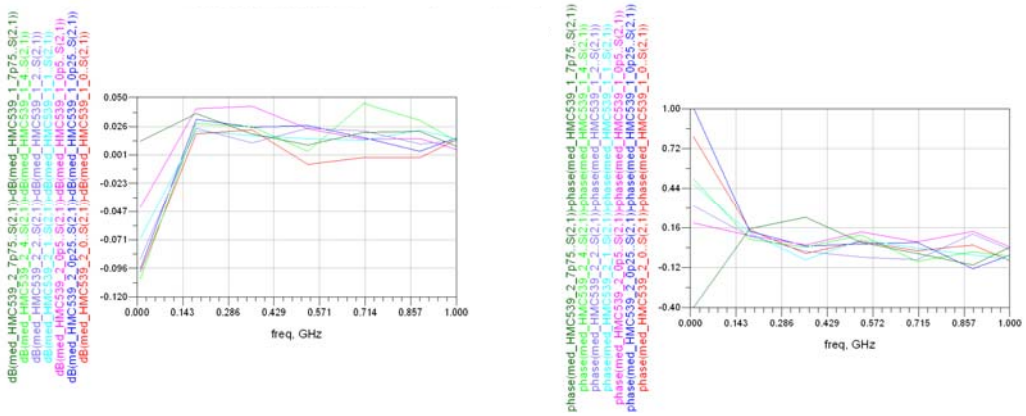
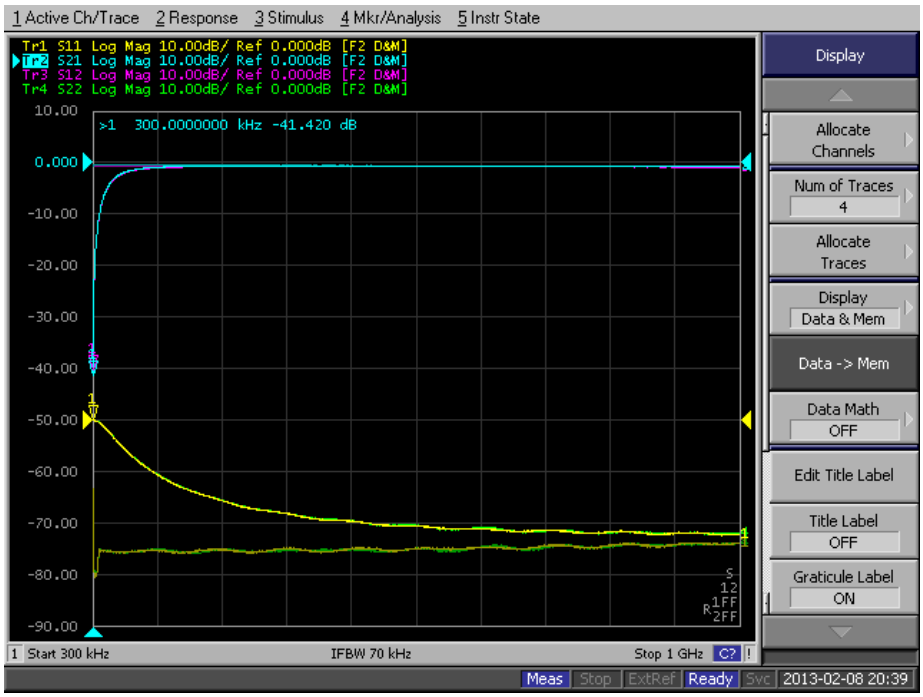
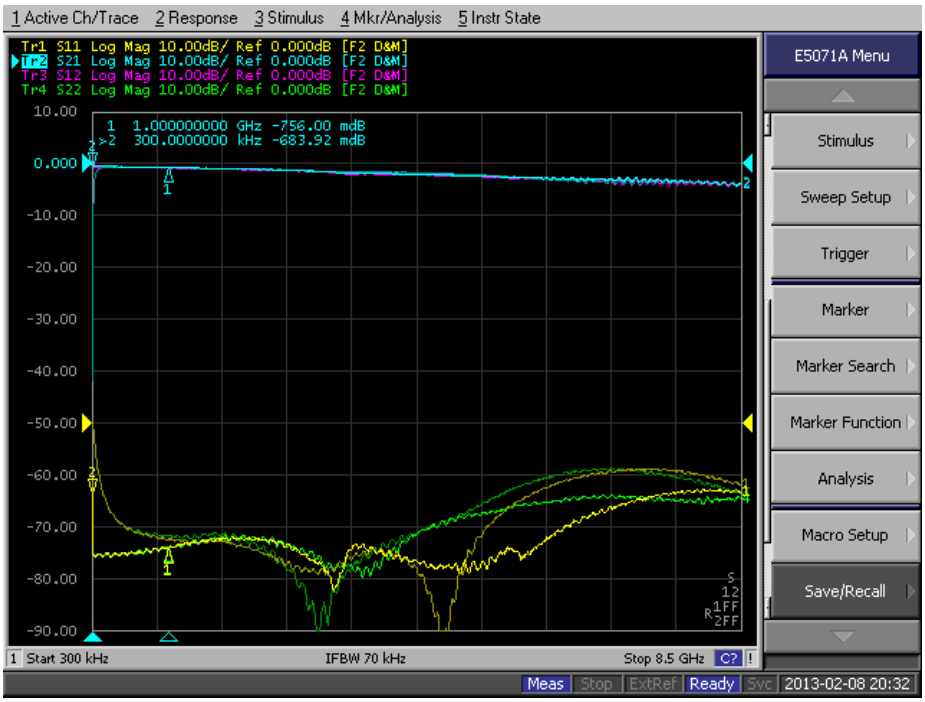


Figure 7.2-4 Measured amplitude and phase difference between two attenuators



(a)



(b)

Figure 7.2-5 Low frequency response of the attenuator with a by-pass capacitor of (a) 100pF and (b) 100nF

7.2.3. I/Q UPCONVERTER 16 - 21GHz BAND

The next component in the Tx analogue signal chain is the I&Q modulator. The following sections present the different implemented test set-ups and the measurement results in order to characterize the modulator circuit.

1st. Test Set-Up:

Figure 7.2-6 shows the block diagram of the test set-up to characterize the main parameters of the I&Q modulator circuit. The biasing voltages and current consumption are: Vgg = -0.8V and VDD1 = VDD2 = VDD3 = 5V. Total I_{dd} approx. 250mA. To power the up-converter it is important to follow the standard typical sequence of MESFET devices.

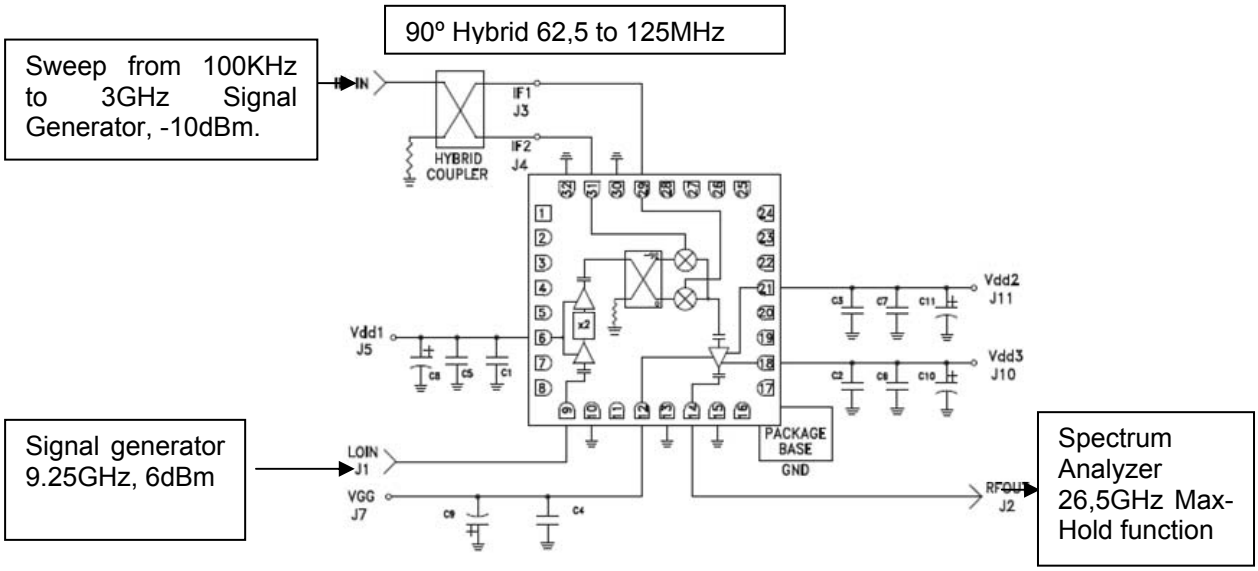
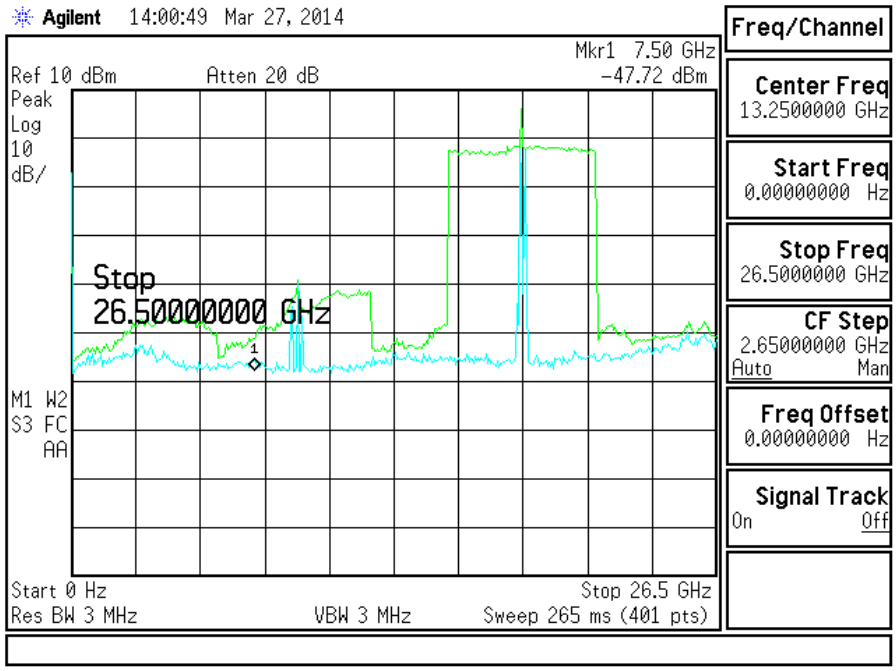
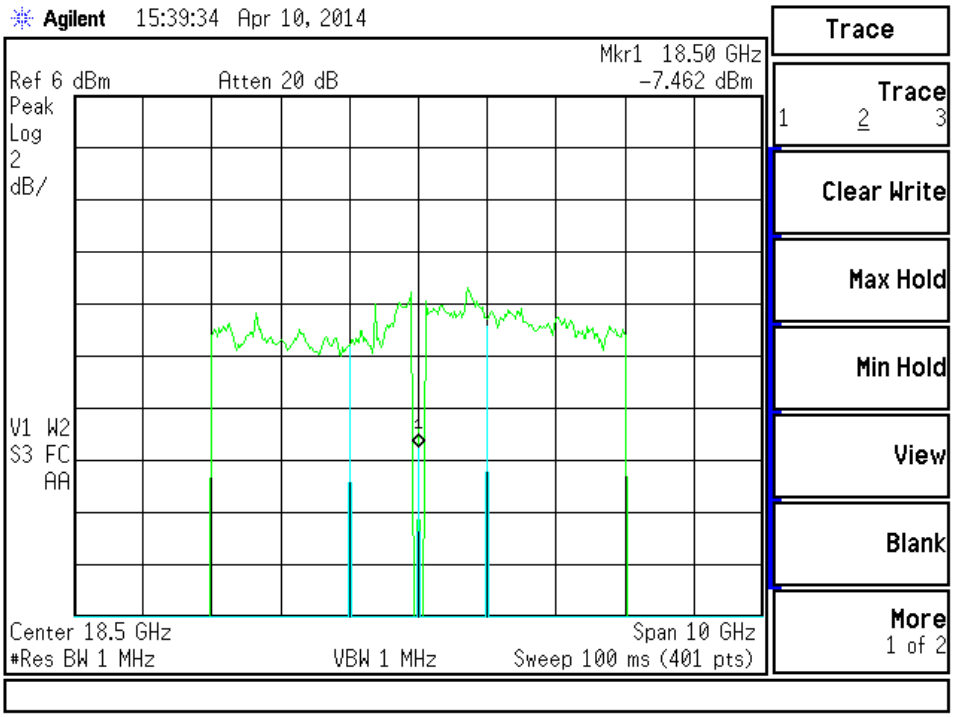


Figure 7.2-6 Test Set-up configuration to measure I&Q modulator main characteristics

Figure 7.2-7 shows the output frequency response of the I&Q modulator. As shown the output 2dB bandwidth centred at 18.5GHz is bigger than 6GHz, which is enough for the considered application. The measured gain is approx. 10.5dB and the 2xLO-RF isolation around 15dB. These measurements were performed without the input hybrid for broadband operation.



(a)



(b)

Figure 7.2-7 Measured (a) output frequency response for the I&Q modulator (b) Detail of the pass-band

The 90º hybrid is used to measure the image rejection response of the I&Q modulator. The hybrid generates 90º phase shift from 62.5 to 125MHz. Figure 7.2-8 shows the image rejection response modulated by the periodic behaviour of the hybrid. As shown the image rejection value is 20dBc, which is in line with the datasheet of the modulator.

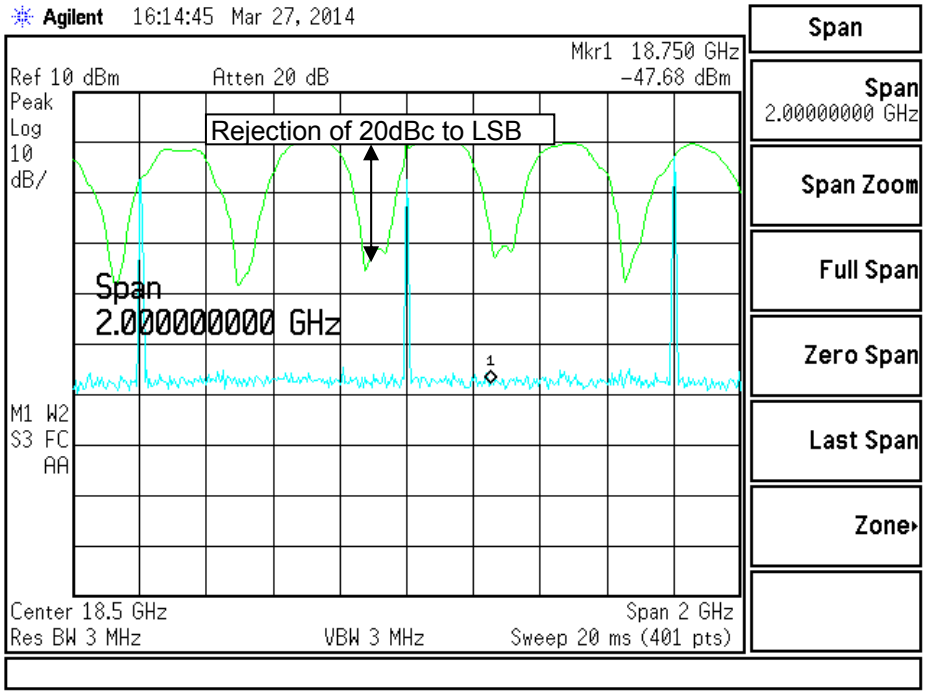


Figure 7.2-8 Image rejection response

2nd. Test Set-Up:

In order to improve the LO-RF isolation, two control voltages have been added (V_{IF1} and V_{IF2}). These voltages will be set by the parameter estimator and controller (PEC) in order to minimize the impact of the 2xLO-RF isolation in the transceiver performance. Figure 7.2-9 shows the test set-up. Figure 7.2-10 shows the measured spectrum after control voltages are applied showing a 2xLO-RF isolation higher than 50dB for carrier frequencies from 16.5GHz to 20.5GHz.

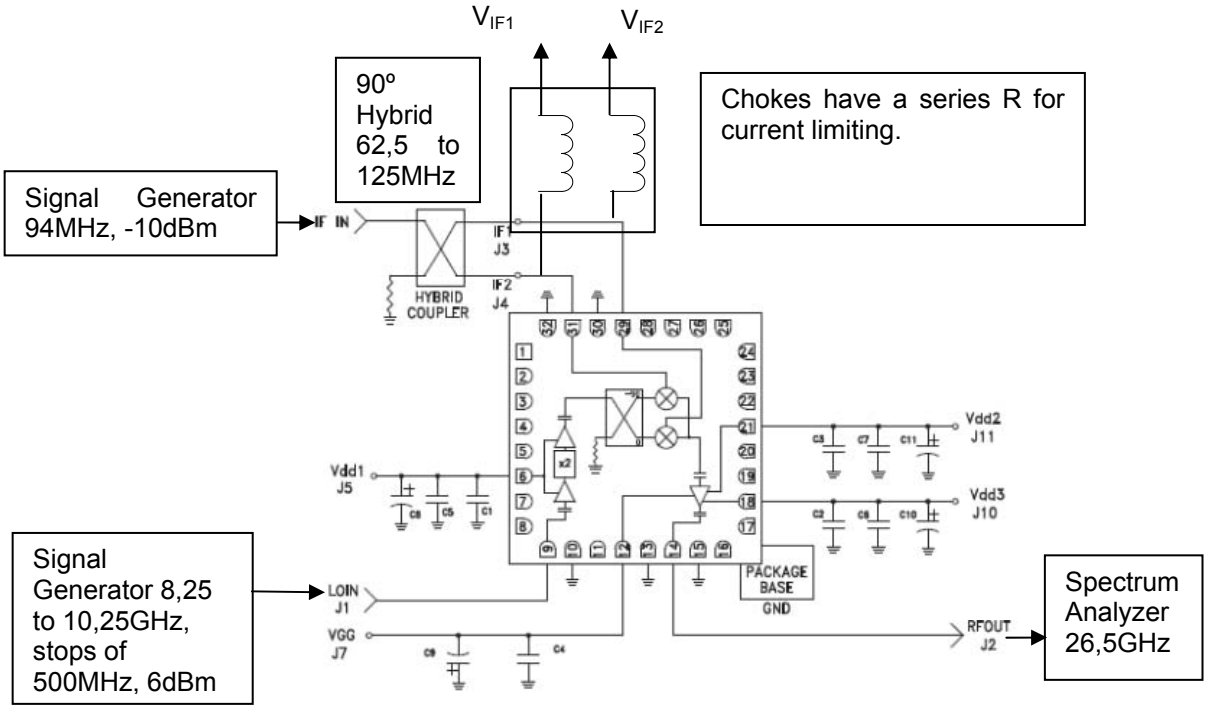
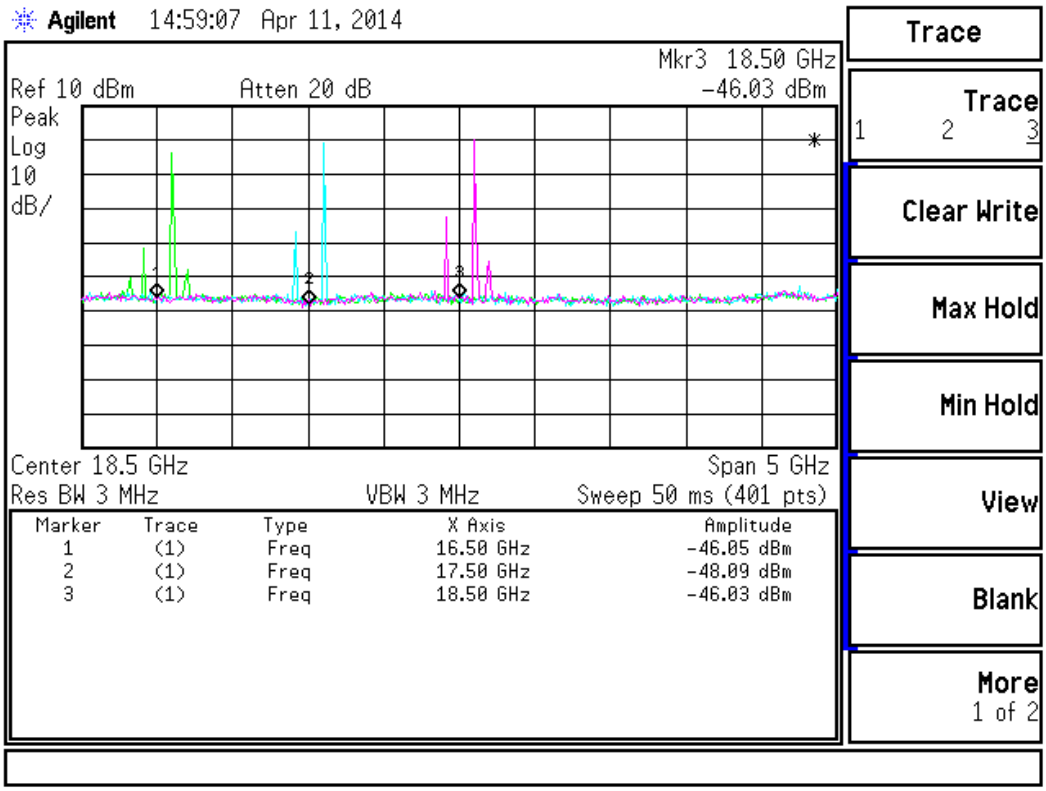
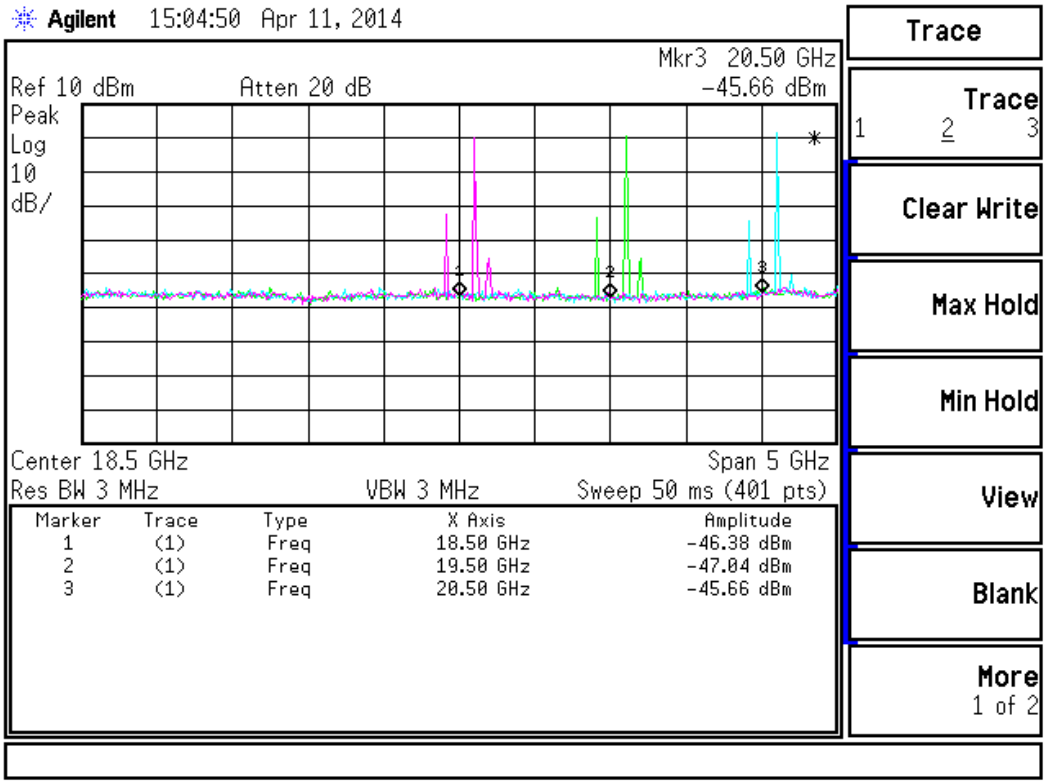


Figure 7.2-9 Test set-up to measure LO-RF isolation improvement when two control DC voltages are applied (V_{IF1} and V_{IF2})



(a)



(b)

Figure 7.2-10 Measurement of the improvement of the LO-RF isolation for (a) 16.5GHz, 17.5GHz, 18.5GHz, (b) 19.5GHz and 20.5GHz carrier frequencies

Table 7.2-1 shows the 2xLO-RF isolation values for different applied control voltages (V_{IF1} and V_{IF2}) at different carrier frequencies. As shown, the 2xLO-RF isolation values after applying healing techniques are higher than 50dB.

LO (RF_out / 2)	16,5GHz	17,5GHz	18,5GHz	19,5GHz	20,5GHz
LO-RF isolation without polarization	19,5dB	17,5dB	13dB	16dB	15,5dB
V_{FI1}	-0,95V	0,98V	2,34V	2,27V	2,05V
V_{FI2}	-1,76V	-2,637V	-3,947V	.2,297V	-1,977V
LO-RF isolation With polarization	>50dB	>50dB	>50dB	>50dB	>50dB

Table 7.2-1 LO-RF isolation value for different applied control voltages at different carrier frequencies

3rd. Test Set-Up:

In order to improve the image rejection value, some signal phase pre-distortion is added through the synchronized signal generators. Figure 7.2-11 shows the test set-up.

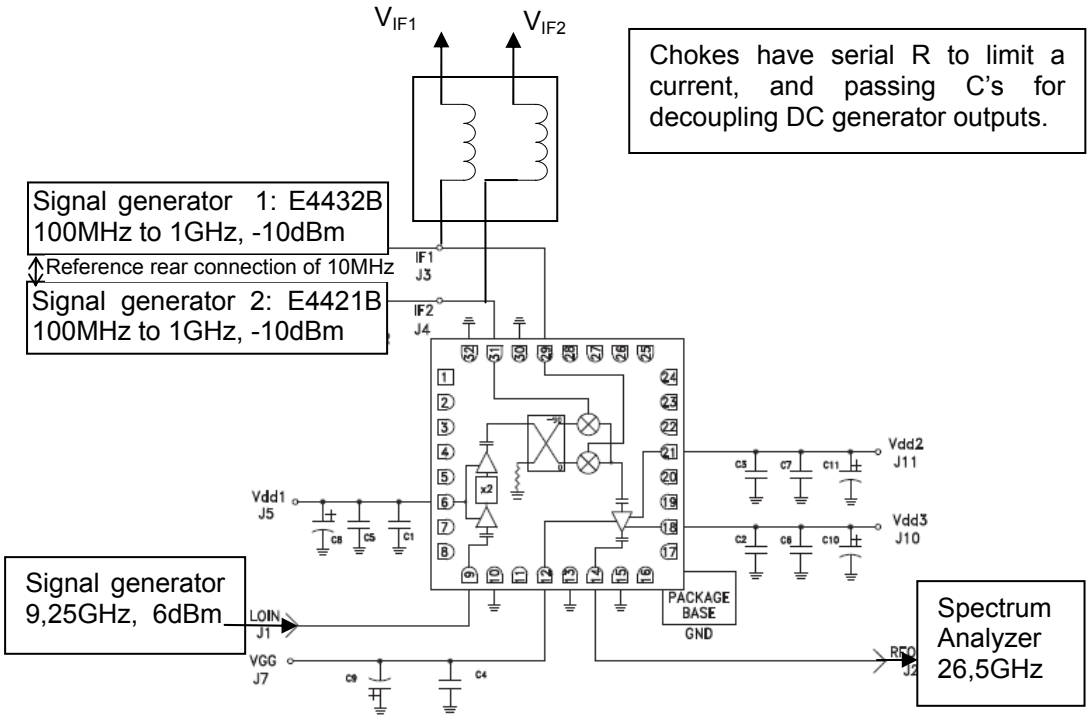
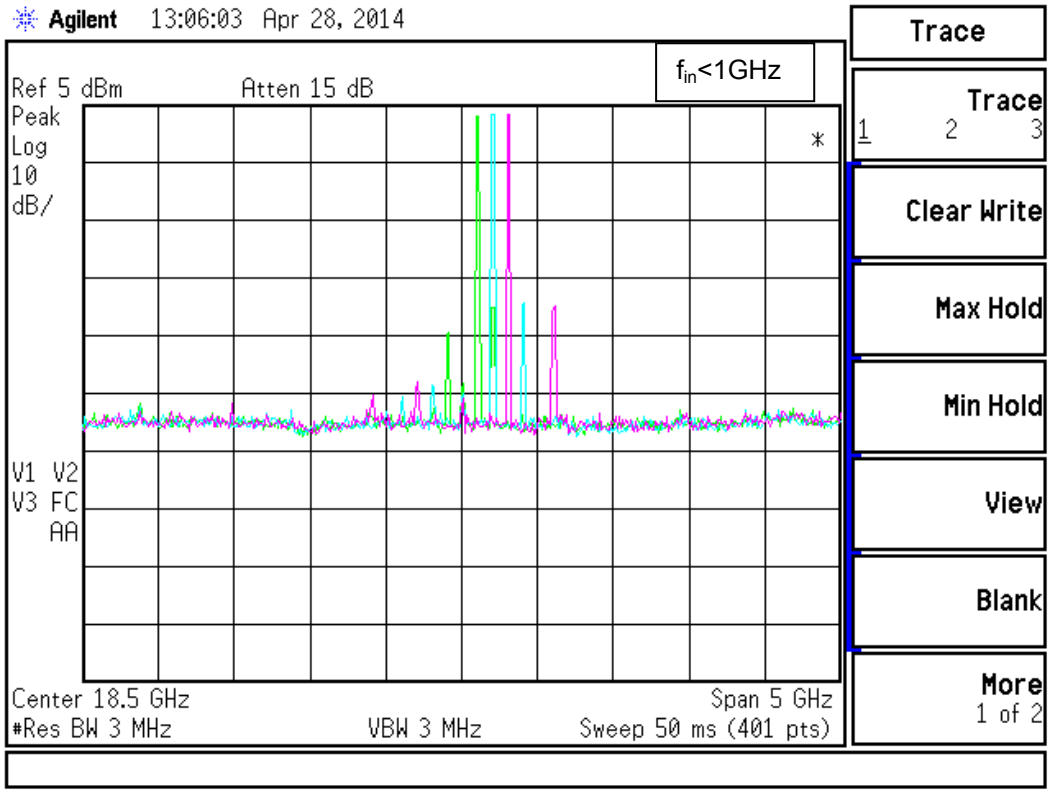


Figure 7.2-11 Test set-up to apply phase pre-distortion to the I&Q modulator and improve image rejection value

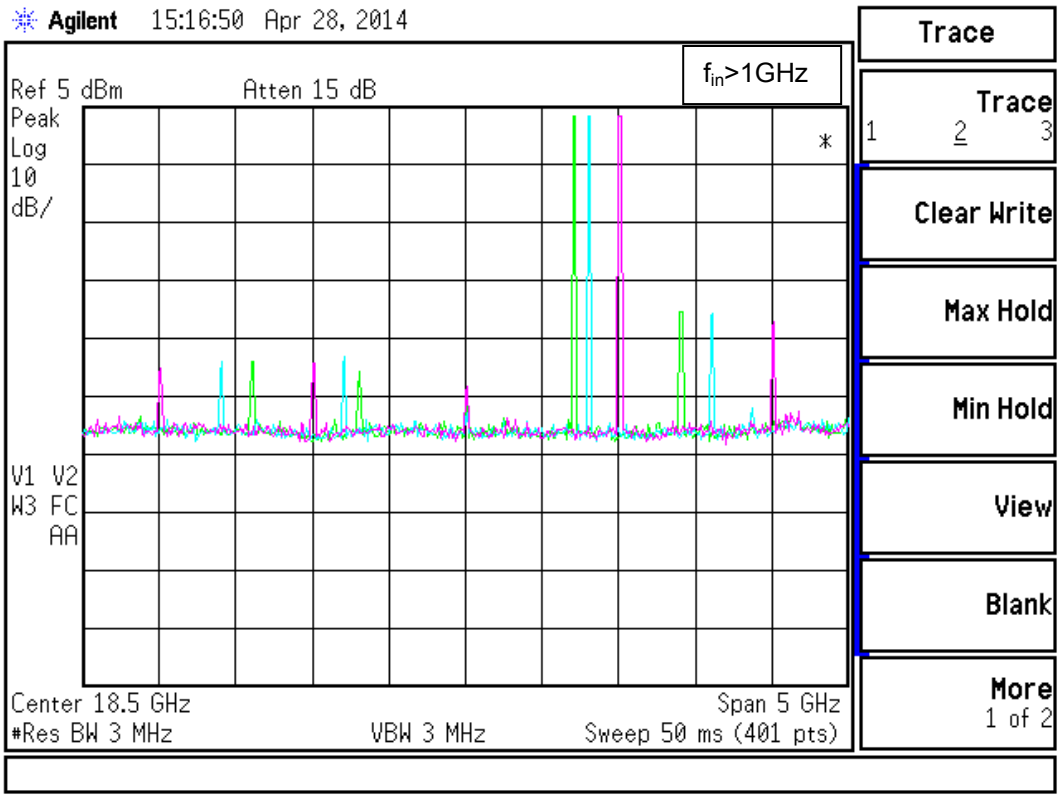
Input ,MHz→	100	200	300	400	500	600	700	800	900	1000
IF1_I (relative phase at generator for LSB rejection> 45dB)	Manual Reset of the phase reference for this frequency is done. Other frequencies relate to this.	3º	-105º	121º	61º	62º	-137º	160º	156º	94º
IF1_Q	The input Q is not adjusted									
V_{FI1} (V)	2,29	2,19	2.09	2.1	2.1	2.19	2.29	2.29	2.39	2.39
V_{FI2} (V)	-3,4	-3,4	-3.5	-3.6	-3.6	-3.8	-3.8	-3.8	-3.8	-3.8
	The LO is rejected in general> 50dB, one only point measured with > 45dB									

Table 7.2-2 Applied voltages at different IF frequencies for image rejection improvement

Figure 7.2-12 shows the image rejection and 2xLO leakage at different frequencies of the channel centred at 18.5GHz. As shown image rejection values below 35dBc and 2xLO-RF isolation values below 45dB are possible in all cases.



(a)



(b)

Figure 7.2-12 Measured image rejection, LO leakage at different frequencies of the channel centred at 18.5GHz (a) f_{in}<1GHz (b) f_{in}>1GHz

As shown in the previous, figure 7.2-12, by using two control voltages and phase pre-distortion it is possible to improve 2xLO-RF isolation and image rejection values of the I&Q modulator. Currently some work is being developed in order to design and select the detectors to measure image rejection and LO leakage and, therefore, provide the inputs to the parameter estimator and controller (PEC).

7.2.4. 16 to 21GHz Band Pass Filter

In order to check the need of a band-pass filter from 16GHz to 21GHz, an inter-digital filter on a low loss microwave substrate has been implemented after the I&Q modulator. The measurements of 3 equal implemented filters are presented in Figure 7.2-13.

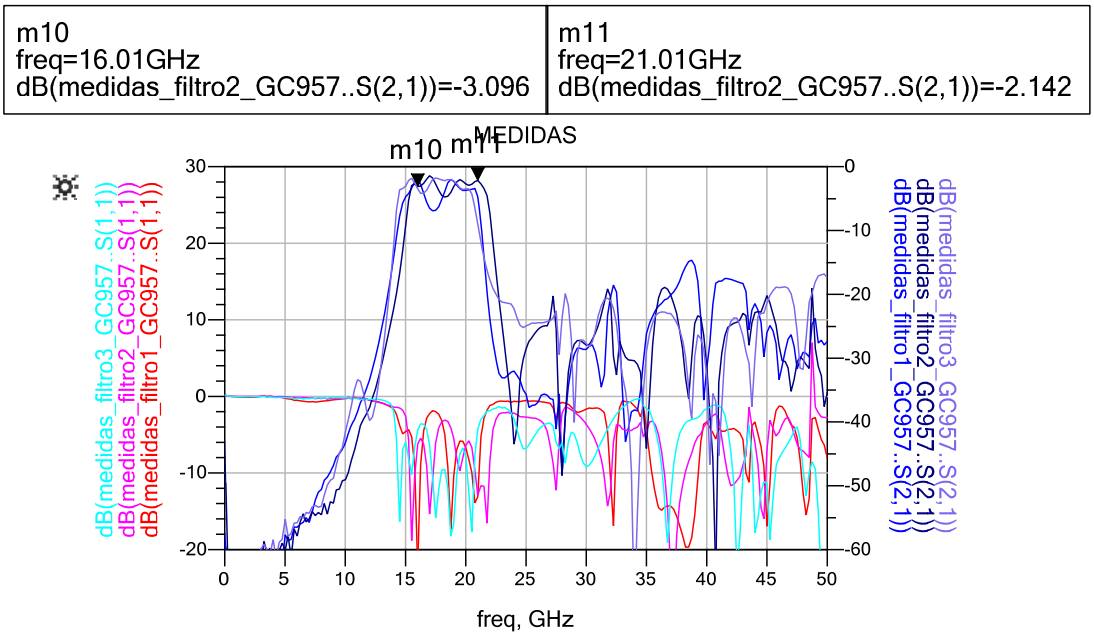


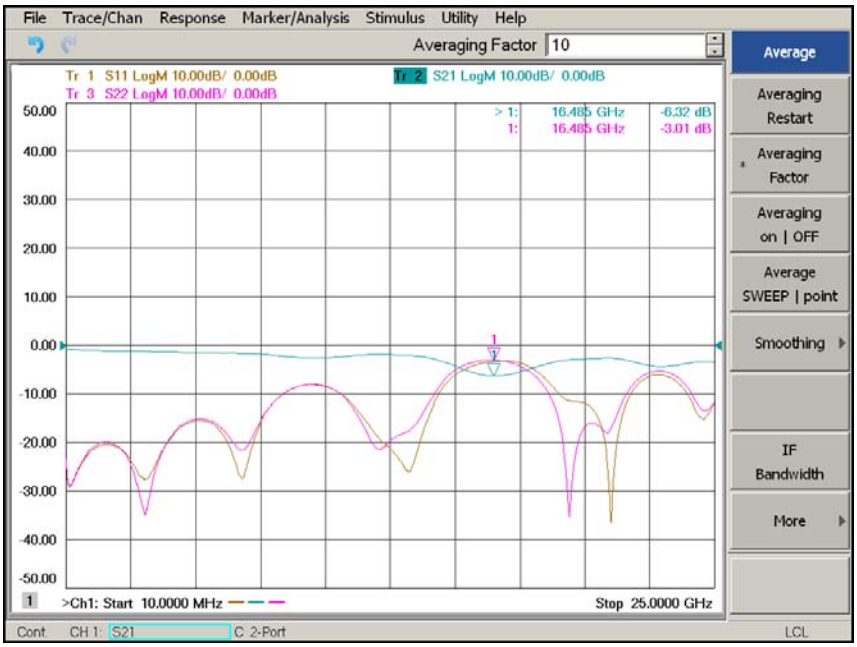
Figure 7.2-13 Measurement results of the IF filter

As shown, the filter presents a good rejection around 20dB up to a frequency of 50GHz, but the input matching in the centre of the band is poor. The reason for this is the poor quality of the GC957 housing SMA connector and the difficulty of the transition to the microstrip. In fact, the mismatch improves when contact plates are placed to GND near the transition. Work is in progress to provide an ad-hoc box with a good transition to the microstrip.

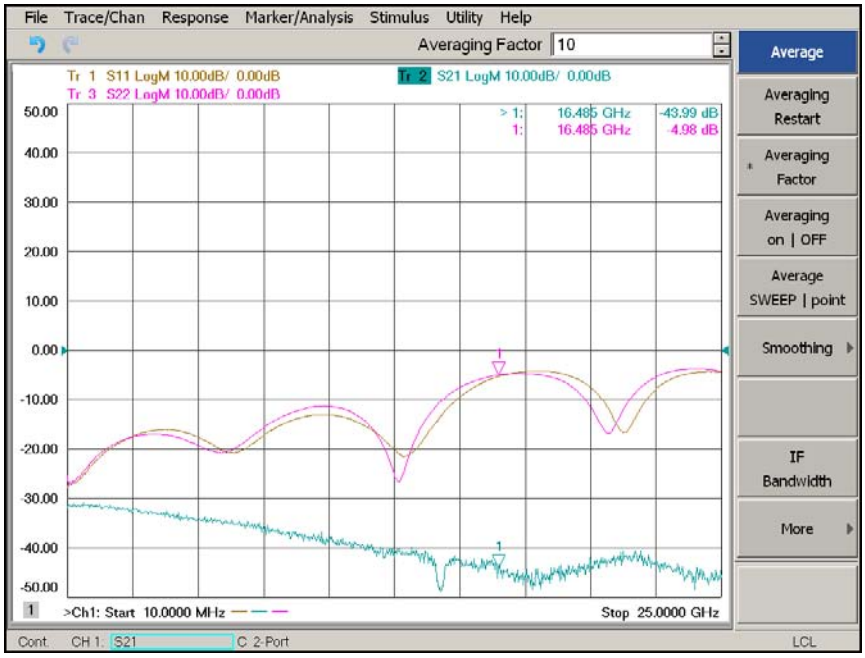
7.2.5. 16 to 21GHz Attenuator

The attenuator after the band-pass filter will be used either to fix the signal level for the mmW part while keeping a high SNR or to simulate channel attenuation when IF Tx part and IF Rx part are connected in loopback configuration in order to test digital baseband transmission and reception algorithms.

A broadband variable attenuator from DC to 30GHz, mounted on an evaluation board is used. An auxiliary circuit is employed to generate two complementary DC voltages, in order to enhance the linearity and return losses of the attenuator. Figure 7.2-14 shows the measured results for the 16-21GHz attenuator.



(a)



(b)

Figure 7.2-14 Measured results for the 16-21GHz attenuator (a) 3dB attenuation (b) 43dB attenuation

Figure 7.2-14 shows a poor matching in the band from 16 to 21GHz; the attenuation range is quite linear and extends from -3dB to -43dB with DC control signals adequately configured. The reason for this poor matching at the frequency of interest it the SMA connector. Work is in progress to improve that matching with higher quality super-SMA or 3.5mm connector launchers. Preliminary results are shown in Figure 7.2-15.

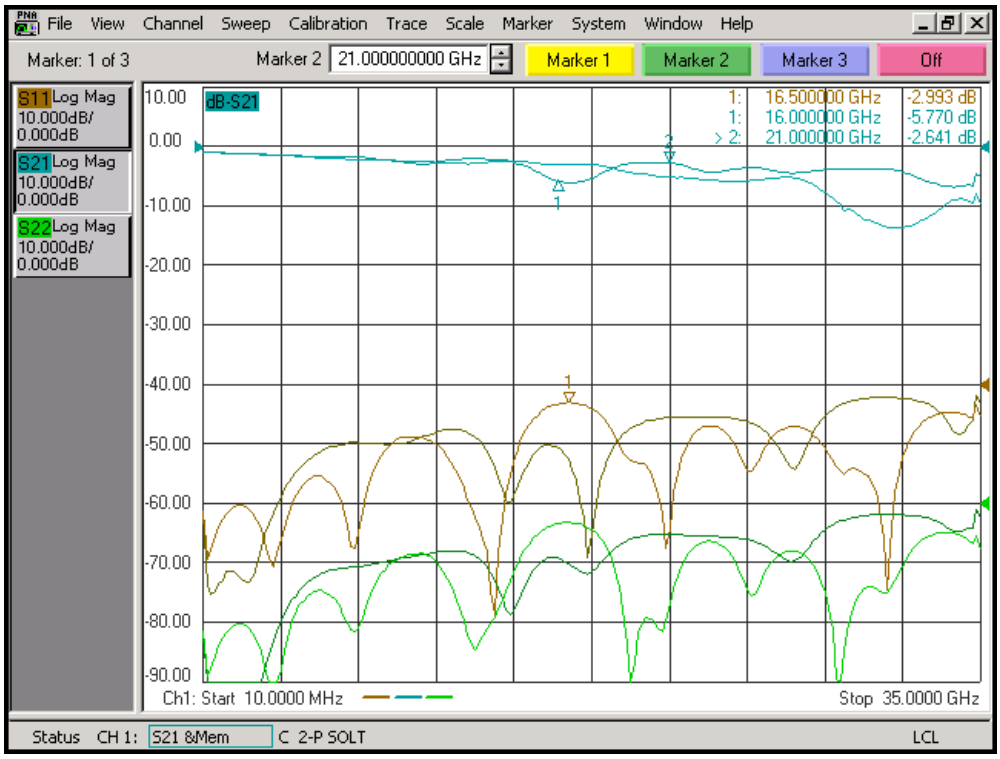


Figure 7.2-15 Preliminary results for the 16 to 21GHz attenuator with higher quality SMA connector

7.2.6. Down-Converter characterization

4th Test Set-Up:

The down-converter I&Q demodulator measurements are presented in this section. Figure 7.2-16 shows the test set-up.

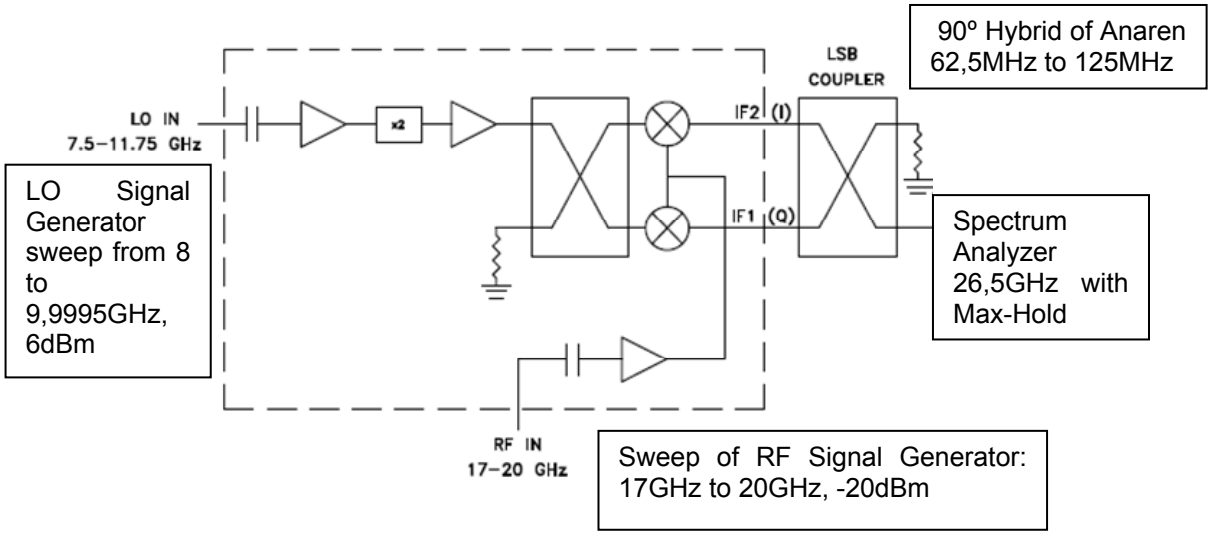


Figure 7.2-16 Test set-up for the basic characterization of the I&Q demodulator

Figure 7.2-17 shows the frequency response measurement of the I&Q demodulator for an LO frequency of 9.25GHz and baseband signal swept from DC to 3GHz. The measured gain is around 10.5dB, which is in line with the datasheet.

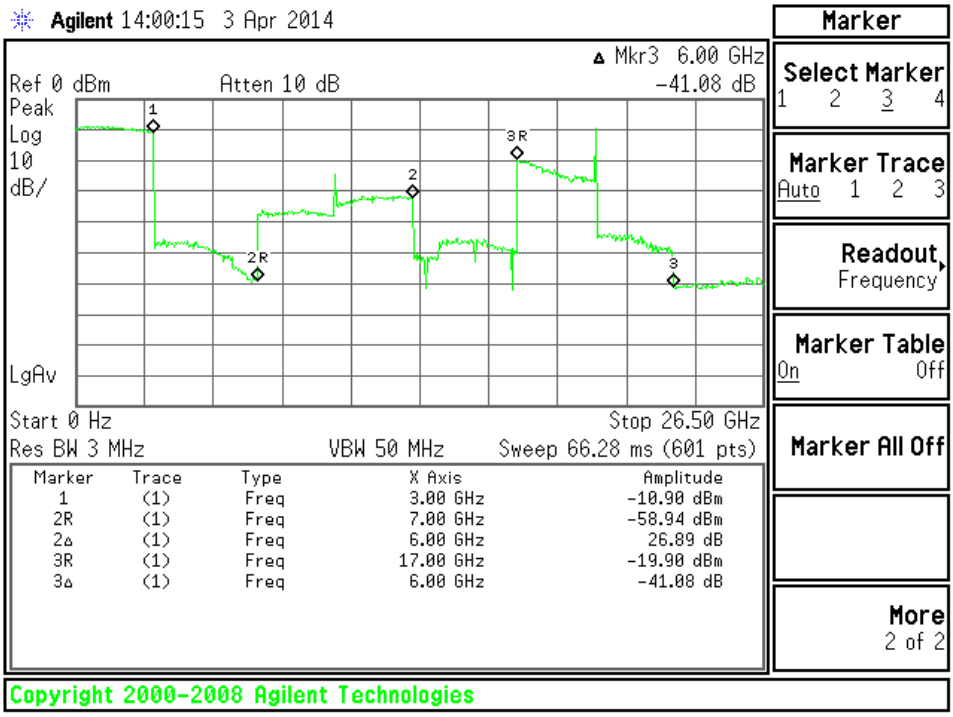


Figure 7.2-17 Frequency response measurement of the I&Q demodulator

Figure 7.2-18 shows the image rejection measurement. As shown a value of 20dB is obtained without any calibration. That is a little bit higher that what was specified in the datasheet. This might be due to the used input hybrid. The rejection of LO is 30dB, and for 2xOL is 16dB.

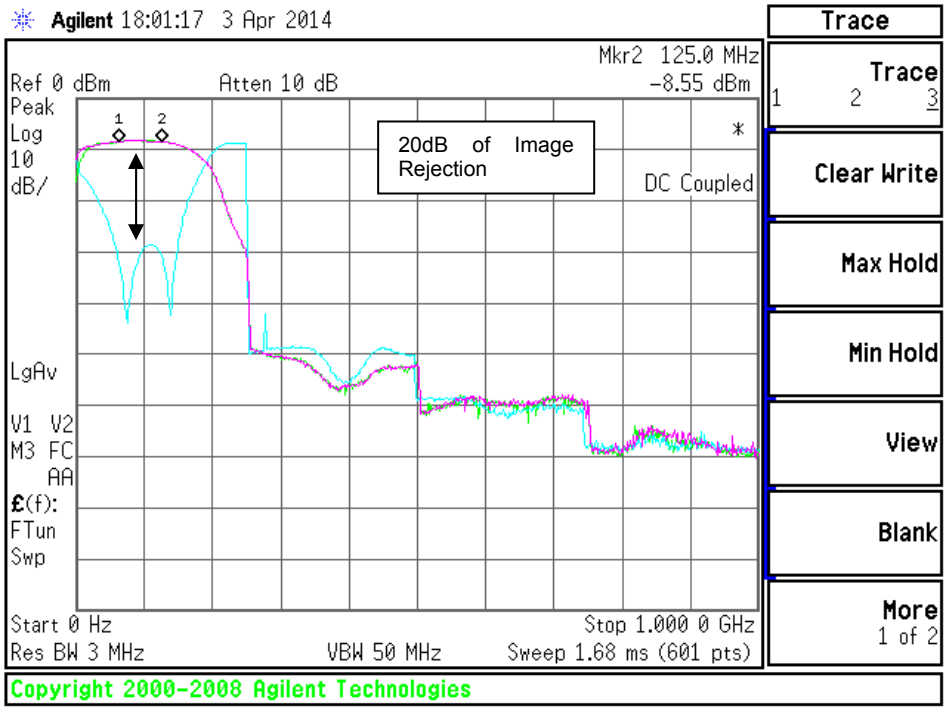


Figure 7.2-18 I&Q demodulator image rejection measurement

The low frequency pole response is limited by the DC block (Inmet mod. 8301) component placed to protect the Spectrum Analyzer.

6.2.11.2, 5th. Test Set-Up:

Finally, the down-converter is measured with an Oscilloscope to characterize the amplitude and phase imbalances. Figure 7.2-19 shows the test set-up.

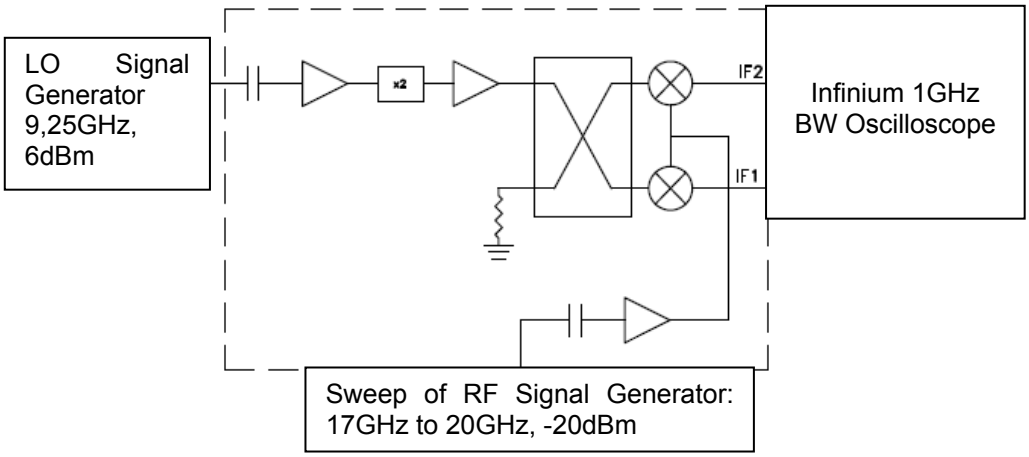


Figure 7.2-19 Test set-up for measurement of the amplitude and phase imbalances

The amplitude imbalance has been measured in dB, comparing the amplitude of the I&Q baseband signals when the RF frequency is swept from 17 to 20GHz, and the LO is swept accordingly to give a baseband IF signal of 1GHz. In all the cases, the measured amplitude imbalance is well below 1 dB.

The phase imbalance is measured comparing the relative phase between I&Q baseband signals from 1MHz to 1GHz, sweeping RF signal from 17 to 20GHz and sweeping the LO accordingly to give a baseband IF signal. The results are summarized in Table 7.2-3.

IF freq (MHZ)→ RF freq (GHz) ↓	1	100	300	500	700	900	1000	Peak phase imbalance (º)
17	91º	82º	78º	68,5º	62º	48º	47º	-44º
17,5	86º	81º	73º	64º	52º	47º	45º	-41º
18	82º	79,5º	74º	66º	55º	50º	42º	-40º
18,5	84,7º	80º	72º	59º	52º	51º	43º	-41,7º
19	84,8º	80º	68º	62º	50,5º	42º	39,5º	-45,3º
19,5	80º	76º	68º	61º	50º	43º	39º	-41º
20	78,8º	74º	64,5º	58º	51º	44º	40,5º	-38,3º
Peak phase imbalance (º)	-12,2º	-8º	-13,5º	-10,5º	-11º	-8º	-8º	

Table 7.2-3 Measured phases at the output of the I&Q demodulator

The results are in line with the datasheet specification.

8. CONCLUSIONS

The re-design of the building blocks of the analogue transmitter and receiver front-ends has been presented in this document. Results show that most of the specifications in the updated D1.2.2 document are fulfilled. Furthermore, a much lower DC power consumption than in other commercial solutions is observed.

In the transmitter part, the IF I/Q modulator, PA and mmW up-converter mixer have been redesigned, and the following blocks have been sent to fabrication:

- IF I/Q modulator, standalone.
- E-Band PA, standalone.
- mmW transmitter, consisting of the up-converter mixer and power amplifier.

As for the receiver, the LNA, IF amplifier and mmW down-converter mixer have been redesigned as well. The circuits that have been sent for fabrication are:

- LNA
- IFA
- mmW receiver, consisting of the LNA, the mmW down-converter mixer and the IFA.

Regarding the frequency synthesis blocks, they have been designed as well. The mmW LO signal generator has been submitted for manufacture, and the rest of the blocks will be sent once they are re-adjusted according to the measurement results of the circuits of the first tapeout.

System simulations have been performed with the updated simulation results, and the performance of the system fulfils the required specifications.

Additionally, a platform with a discrete version of the IF circuitry has been designed and implemented, including both the IF I/Q modulator and demodulator. Hence, the digital design group can start testing the different designed algorithms for the signal generation and reception, as well as different algorithms to compensate the imperfections introduced by the analogue front-end.