HIGH PERFORMANCE AND EMBEDDED ARCHITECTURE AND COMPILATION

Project Acronym: *HiPEAC*
Project full title: High Performance and Embedded Architecture and Compilation
Grant agreement no: *ICT-217068*

DELIVERABLE 3.1

SPREADING EXCELLENCE REPORT

1. Summary on Spreading Excellence

An important aspect of a network of excellence is to create visibility for its members and for the research carried out in the network, while at the same time integrating the network members.

Improving the visibility of our community

The role of the *Conference* and *Journal* are to improve the scientific visibility in the area of high-performance and embedded processors. They will help in the *promotion of talented young researchers* by inviting them in the visible role of program committee member or reviewer for the journal.

On top of this, publications at other major conferences will be stimulated through an original *Award* program.

The *Newsletter* aims at publicising the activities of our community beyond the strict scientific community: within industry, among public officials, and towards Asia, whose researchers only infrequently participate in scientific forums at this moment. At the same time, it is a means for promoting HiPEAC groups and achievements beyond the standard scientific articles.

The *HiPEAC Technical Reports* allow the rapid presentation and dissemination of academic work, time stamping hot research ideas, and help show the breadth and scope of the HiPEAC community.

The *Roadmap* helps the HiPEAC community to regularly revisit the key scientific challenges, and it helps disseminating the HiPEAC vision beyond the HiPEAC community.

Integrating our community

The *Summer School* aims at raising the standards of our PhD students and members by confronting them with renowned teachers in our domains, whatever their geographic origin. It is also a networking event resulting in long-lasting individual links among students, between students and faculty or engineers, and among faculty and engineers.

The *Web Seminars* offers a continuous training cycle for the community, and they also offer an opportunity for researchers, junior and senior alike, to publicise their activity within the HiPEAC community and beyond, possibly triggering new collaborations. The *industrial workshops* are networking events between academia and companies where the academics learn more about the industrial challenges, and the industrial researchers are confronted with the lastest academic research results.

Beyond the cooperation with large companies, we also aim at *stimulating the development of Start-ups* by HiPEAC researchers. Currently, 7 HiPEAC researchers have set up innovative SMEs, and we intend to further support these companies as well as stimulate new initiatives.

Finally, the *Web Site* serves as a meeting place for all HiPEAC activities.

The Spreading Excellence Program consists of 11 specific tasks:

2. Task 3.1: Conference

The conference is one of the main public events organised by the HiPEAC network. It is quite succesful, attracting a wide audience and offering high quality workshops and tutorials.

The topics called for in the conference and the workshops are the topics of the HiPEAC research agenda as described in the research program. The conference and workshops are completely open to both HiPEAC members and non-members from all over the world.

The conference is supervised by a steering committee, which decides on the chairs and the location of the conference and reports to the HiPEAC steering committee. The logistics of the conference are handled by the chairs, supported by the HiPEAC technical and administrative staff.

2.1. HiPEAC 2008 Conference, Goteborg

The HiPEAC 2008 Conference, which was organised by Chalmers in Goteborg, was funded by HiPEAC1. However, we will provide a short overview of this conference here as well.

The Conference

The conference was organised by Chalmers, and was held at the Chalmers Conference Center, in Goteborg, Sweden.

The Conference was a two-day event, from January 28 to January 29, 2008.

Paper Acceptance Rate

77 papers from Europe, USA and Asia were submitted to the conference. 25 were presented at the conference (32% acceptance rate).

Conference Committee

The following people were involved in organising the conference:

GENERAL CO-CHAIRS		
Per Stenström	Chalmers University of Technology	Sweden
Michel Dubois	University of Southern California	USA
PROGRAM CO-CHAIRS		
Manolis Katevenis	University of Crete/FORTH	Greece
Rajiv Gupta	University of California	Riverside
PROGRAM COMMITTEE		
Angelos Bilas	FORTH & Univ. of Crete	Greece
Mats Brorsson	KTH	Sweden
Koen De Bosschere	University of Ghent	Belgium
Jack Davidson	University of Virginia	USA
Marc Duranton	NXP Semiconductors	Netherlands
Babak Falsafi	Carnegie Mellon University	USA
Paolo Faraboschi	HP Labs	Spain
Kristian Flautner	ARM	UK

Chris Gniady	University of Arizona	USA
Wen-mei Hwu	University of Illinois	USA
Paolo Ienne	EPFL	Switzerland
Norm Jouppi	HP Labs	USA
Mahmut Kandemir	Penn. State Univ.	USA
Stefanos Kaxiras	University of Patras	Greece
Christos Kozyrakis	Stanford University	USA
Scott Mahlke	Univ. of Michigan	USA
Peter Marwedel	Univ. Dortmund	Germany
Avi Mendelson	Intel	Israel
Andreas Moshovos	University of Toronto	Canada
Mike O'Boyle	Edinburgh University	UK
Kunle Olukotun	Stanford University	USA
Yunheung Paek	Seoul National Universiry	Korea
Santosh Pande	Georgia Inst. of Technology	USA
Yale Patt	University of Texas at Austin	USA
Alex Ramirez	Univ. Pol. de Cataluna & BSC	Spain
Lawrence Rauchwerger	Texas A&M University	USA
John Regehr	University of Utah	USA
Andre Seznec	INRIA	France
Guri Sohi	University of Wisconsin	USA
Olivier Temam	INRIA	France
Josep Torrellas	University of Illinois	USA
Mateo Valero	Univ. Pol. de Cataluna & BSC	Spain
David Whalley	Florida State University	USA
Sudhakar Yalamanchili	Georgia Institute of Technology	USA
WORKSHOPS/TUTORIALS CHAIR		
Mats Brorsson	KTH	Sweden
LOCAL ARRANGEMENTS CHAIR		
Ewa Wäingelin	Chalmers University of Technology	Sweden
FINANCE CHAIR		
Per Waborg	Chalmers University of Technology	Sweden
Wouter De Raeve	Ghent University	Belgium
PUBLICITY CHAIR		
Mike O'Boyle	University of Edinburgh	U.K.
PUBLICATIONS CHAIR		
Theo Ungerer	University of Augsburg	Germany
SUBMISSIONS CHAIR		
Michiel Ronsse	Ghent University	Belgium
WEB CHAIR		
Sylvie Detournay	Ghent University	Belgium
STEERING COMMITTEE		
Mateo Valero	UPC	Spain

Anant Agarwal	MIT	USA
Koen De Bosschere	Ghent University	Belgium
Mike O'Boyle	University of Edinburgh	UK
Brad Calder	University of California	USA
Rajiv Gupta	University of California	Riverside
Wen-mei W. Hwu	UIUC	USA
Josep Llosa	UPC	Spain
Margaret Martonosi	Princeton University	USA
Per Stenström	Chalmers University	Sweden
Olivier Temam	INRIA Futurs	France

Conference Program

Day 1: Monday January 28

9:00 - 10:00	KEYNOTE. Supercomputing for the Future, Supercomputing from the Past *Mateo Valero, Barcelona Supercomputing Center*
10:30 - 12:00	SESSION I. Multithreaded and Multicore Processors *CHAIR: Georgi Gaydadjiev, T. U. Delft, Netherlands*
	MIPS MT: A Multithreaded RISC Architecture for Embedded and Real-Time Processing *Kevin D. Kissell* *MIPS Technolgies Inc.*
	rMPI: Message Passing on Multicore Processors with On-Chip Interconnect *James Psota and Anant Agarwal* *MIT*
	Modeling Multigrain Parallelism on Heterogeneous Multi-core Processors: A Case Study of the Cell BE *Filip Blagojevic, Xizhou Feng, Kirk W. Cameron and Dimitrios S. Nikolopoulos* *Virginia Tech*
13:30 - 15:00	SESSION IIa. Reconfigurable - ASIP *CHAIR: Chris Gniady, University of Arizona, USA*
	BRAM-LUT tradeoff on a Polymorphic DES Design *Ricardo Chaves, Blagomir Donchev, Georgi Kuzmanov, Leonel Sousa and Stamatis Vassiliadis* *Instituto Superior Tecnoci/INESC-ID and TUDelft*
	Architecture Enhancements For The ADRES Coarse-Grained Reconfigurable Array *Frank Bouwens, Mladen Berekovic, Bjorn De Sutter and Georgi Gaydadjiev* *IMEC and TUDelft*
	Implementation of an UWB Impulse-Radio Acquisition and Despreading Algorithm on a Low Power ASIP *Jochem Govers, Jos Huisken, Mladen Berekovic, Olivier Rousseaux, Frank Bouwens, Michael de Nil and Jef van Meerbergen* *Eindhoven University of Technology, IMEC, Philips Research Eindhoven and Silicon Hive*
13:30 - 15:00	SESSION IIb. Compiler Optimizations *CHAIR: Koen De Bosschere, University of Ghent, Belgium*
	Fast Bounds Checking Using Debug Register *Tzi-cker Chiueh* *Stony Brook University*
	Studying Compiler Optimizations on Superscalar Processors through Interval Analysis

	Stijn Eyerman, Lieven Eeckhout and James E. Smith *Ghent University and University of Wisconsin-Madison*
	An Experimental Environment Validating the Suitability of CLI as an Effective Deployment Format for Embedded Systems *Marco Cornero, Roberto Costa, Ricardo Fernandez Pascual, Andrea Ornstein and Erven Rohou* *STMicroelectronics*
15:30 - 17:00	SESSION III. Industrial Processors & Application Parallelization *CHAIR: Mike O'Boyle, Edinburgh University, UK*
	Compilation Strategies for Reducing Code Size on a VLIW Processor with Variable Length Instructions *Todd Hahn, Dineel Sule, Eric Stotzer and Mike Asal* *Texas Instruments*
	Experiences with Parallelizing a Bio-Informatics Program on the Cell BE *Hans Vandierendonck, Sean Rul, Michiel Questier and Koen De Bosschere* *Ghent University*
	Drug Design Issues on the Cell BE *Harald Servat , Cecilia Gonzalez-Alvarez , Xavier Aguilar, Daniel Cabrera-Benitez and Daniel Jimenez-Gonzalez* *Barcelona Supercomputing Center and Universitat Politecnica de Catalunya*

Day 2: Tuesday January 29

8:30 - 10:00	SESSION IV. Power-Aware Techniques *CHAIR: Mats Brorsson, KTH, Sweden*
	COFFEE: COmpiler Framework For Energy-aware Exploration *Praveen Raghavan, Andy Lambrechts, Javed Absar, Murali Jayapala, Francky Catthoor and Diederik Verkest* *KULeuven, IMEC, STMicroelectronics and VUB*
	Integrated CPU and Cache Power Management in Multiple Clock Domain Processors *Nevine AbouGhazaleh, Bruce Childers, Daniel Mosse and Rami Melhem* *University of Pittsburgh*
	Variation-Aware Software Techniques for Cache Leakage Reduction using Value-Dependence of SRAM Leakage due to Within-Die Process Variation *Maziar Goudarzi, Tohru Ishihara and Hamid Noori* *Kyushu University*
10:30 - 12:00	SESSION V. High-Performance Processors *CHAIR: Kevin Kissell, MIPS Technolgies Inc., France*
	The Significance of Affectors and Affectees Correlations for Branch Prediction *Yiannakis Sazeides, Andreas Moustakas, Kypros Constantinides and Marios Kleanthous* *University of Cyprus and University of Michigan*
	Turbo-ROB: A Low-Cost, Simple Checkpoint/Restore Accelerator *Patrick Akl and Andreas Moshovos* *University of Toronto*
	LPA: A First Approach to the Loop Processor Architecture *Alejandro Garcia, Oliverio J. Santana, Enrique Fernandez, Pedro Medina and Mateo Valero* *Barcelona Supercomputing Center, University Politecnica de Catalunya and Universidad de Las Palmas de Gran Canaria*
13:30 -	SESSION VI. Profiles: Collection and Analysis

15:00	*CHAIR: Dimitrios Nikolopoulos, FORTH, Crete, Greece*
	Complementing Missing and Inaccurate Profiling using a Minimum Cost Circulation Algorithm *Roy Levin, Gad Haber and Ilan Newman* *Haifa University and IBM Haifa Labs*
	Using Dynamic Binary Instrumentation to Generate Multi-Platform SimPoints: Methodology and Accuracy *Vincent M. Weaver and Sally A. McKee* *Cornell University*
	Phase Complexity Surfaces: Characterizing Time-Varying Program Behavior *Frederik Vandeputte and Lieven Eeckhout* *Ghent University*
15:30 - 17:30	SESSION VII. Optimizing Memory Performance *CHAIR: Andreas Moshovos, University of Toronto, Canada*
	MLP-Aware Dynamic Cache Partitioning *Miquel Moreto, Francisco J. Cazorla, Alex Ramirez and Mateo Valero* *Barcelona Supercomputing Center and Universitat Politecnica de Catalunya*
	Compiler Techniques for Reducing Data Cache Miss Rate on a Multithreaded Architecture *Subhradyuti Sarkar and Dean M. Tullsen* *UCSD*
	Code Arrangement of Embedded Java Virtual Machine for NAND Flash Memory *Chun-Chieh Lin and Chuen-Liang Chen* *National Taiwan University*
	Aggressive Function Inlining: Preventing Loop Blockings in the Instruction Cache *Yosi Ben Asher, Omer Boehm, Daniel Citron, Gadi Haber, Moshe Klausner, Roy Levin and Yousef Shajrawi* *Haifa University and IBM Research Lab, Haifa*

Conference Attendance

The conference was attended by 256 participants.

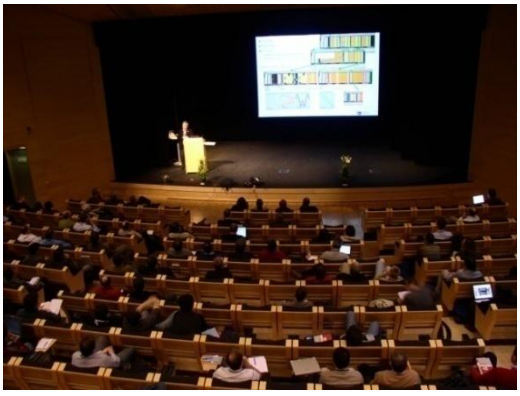
53 attendants came from industry. The attending companies were:

ABB Network Management	IAR Systems	Saab Microwave Systems
ARM	IBM	STMicroelectronics
CAPS Enterprise	Infineon Technologies	Technion
Central Research Laboratory, Hitachi, Ltd.	Intel Corporation	Texas Instruments
Codeplay Software Ltd.	MIPS Technologies Inc.	Thales Research & Technology
Ericsson	Nema Labs	Volvo Technology
HP	NXP Semiconductors	

The attendants came from 26 different countries:

Sweden	47
Spain	41
France	24
UK	23
USA	19
Belgium	16
The Netherlands	15
Germany	15
Norway	11
Italy	10
Israel	5
Greece	4
Cyprus	4
Russia	3
Portugal	3
Turkey	2
Switzerland	2
Japan	2
Iran	2
Finland	2
Taiwan	1
Serbia	1
Scotland	1
Poland	1
Denmark	1
Canada	1

The majority of the attendants came from Sweden, where the conference was held.



133 conference-goers were member of or affiliated with HiPEAC. This means that almost half of the attendants did not have a formal connection to HiPEAC.

Student Grants

We were able to give a grant to 42 PhD students. The grant waives the registration fee. All students who applied for a grant were given one.

Workshops and Tutorials

On January 27, 4 workshops were organised, as well as 1 tutorial:

- MULTIPROG workshop (Programmability Issues for Multi-Core Computers)
- SMART'08 workshop (Statistical and Machine learning approaches to ARchitectures and compilaTion)
- 2nd HiPEAC Workshop on Reconfigurable Computing
- INA-OCMC workshop (Interconnection Network Architectures: On-Chip, Multi-Chip)
- The Sunflower Toolsuite Tutorial

The workshops and tutorials were attended in total by 201 people.

2.2. HiPEAC 2009 Conference, Paphos

The 4th International Conference on High Performance and Embedded Architectures and Compilers was organised by the University of Cyprus, in Paphos, Cyprus

The Conference

The Conference took place from January 25-28, 2009, at the Amathus Hotel in Paphos, Cyprus. For the first time the conference was extended to a three-day programme, again preceded by a full day of workshops and tutorials.

Paper Acceptance Rate

This year we received 97 paper submissions, of which 14 submissions were co-authored by a program committee member. Papers were submitted from 20 different nations (approximately 46% from Europe, 15% from Asia, 32% from North America, 4% from Africa and the Middle East, and 3% from South America).

27 papers were accepted, i.e., an acceptance rate of 28%.

Conference Committee

The following people were involved in the organisation of the conference:

GENERAL CO-CHAIRS		
Andre Seznec	IRISA/INRIA	France
Joel Emer	INTEL/MIT	USA
PROGRAM CO-CHAIRS		
Michael O'Boyle	University of Edinburgh	UK
Margaret Martonosi	Princeton University	USA
PROGRAM COMMITTEE		
David Albonesi	Cornell University	USA
Eduard Ayguade	UPC	Spain
Francois Bodin	CAPS Enterprise	France
John Cavazos	University of Delaware	USA

Albert Cohen	INRIA	France
Marco Cornero	ST	Italy
Lieven Eeckhout	Ghent University	Belgium
Guang Gao	University of Delaware	USA
Thomas Gross	ETH Zurich	Switzerland
Michael Hind	IBM	USA
Mary J. Irwin	Pennsylvania State University	USA
Russell Joseph	Northwestern University	USA
Ben Juurlink	TU Delft	Netherlands
Stefanos Kaxiras	University of Patras	Greece
Rainer Leupers	University of Aachen	Germany
Gabriel Loh	Georgia Tech University	USA
José Martínez	Cornell University	USA
Bilha Mendelson	IBM Research	Israel
Andreas Moshovos	University of Toronto	Canada
David Padua	UIUC	USA
Markus Pueschel	CMU	USA
Li-Shiuan Peh	Princeton University	USA
Lawrence Rauchwerger	Texas A&M Univ.	USA
Ronny Ronen	Intel Corp.	Israel
Yiannakis Sazeides	University of Cyprus	Cyprus
Vassos Soteriou	Cyprus Univ. of Technol.	Cyprus
Per Stenström	Chalmers University	Sweden
Olivier Temam	INRIA	France
M. J. Thazhuthaveetil	Indian Inst. of Science	India
Richard Vuduc	Georgia Tech University	USA
WORKSHOPS/TUTORIALS CHAIR		
Stefanos Kaxiras	Univesirty of Patras	Greece
LOCAL ARRANGEMENTS CHAIR		
Yiannakis Sazeides	University of Cyprus	Cyprus
FINANCE CHAIR		
Wouter De Raeve	Ghent University	Belgium
PUBLICITY CHAIR		
Hans Vandierendonck	Ghent University	Belgium
PUBLICATIONS CHAIR		
Theo Ungerer	University of Augsburg	Germany
SUBMISSIONS CHAIR		
Michiel Ronsse	Ghent University	Belgium
WEB AND REGISTRATION CHAIR		
Klaas Millet	Ghent University	Belgium
STEERING COMMITTEE		
Anant Agarwal	MIT	USA
Koen De Bosschere	Ghent University	Belgium

Michel Dubois	Univ. of Southern California	USA
Rajiv Gupta	Univ. of California	Riverside
Wen-mei W. Hwu	UIUC	USA
Manolis Katevenis	Univ. of Crete/Forth	Greece
Per Stenström	Chalmers University	Sweden
Theo Ungerer	University of Augsburg	Germany
Mateo Valero	UPC	Spain

Conference Program

Day 1: January 26, 2009

9:00-10:00	KEYNOTE I: Challenges on the Road to Exascale Computing, *Kathryn O'Brien, IBM Research*
10:30-12:30	SESSION I.Dynamic Translation and Optimisation *CHAIR: David Padua, UIUC*
	Steal-on-abort: Improving Transactional Memory Performance through Dynamic Transaction Reordering *Mohammad Ansarin, Mikel Luján, Christos Kotselidis, Kim Jarvis, Chris Kirkham, Ian Watson (University of Manchester)*
	Predictive Runtime Code Scheduling for Heterogeneous Architectures *Víctor Jiménez (BSC), Lluís Vilanova (UPC), Isaac Gelado (UPC), Marisa Gil (UPC), Grigori Fursin (INRIA), Nacho Navarro (UPC)*
	Collective Optimization *Grigori Fursin, Olivier Temam* *(INRIA)*
	High Speed CPU Simulation using LTU Dynamic Binary Translation *Daniel Jones, Nigel Topham* *(University of Edinburgh)*
14:00-15:30	SESSION II. Low level Scheduling *CHAIR: John Cavazos, U Deleware*
	Integrated Modulo Scheduling for Clustered VLIW Architectures *Mattias V. Eriksson and Christoph W. Kessler* *(Linköping university)*
	Software Pipelining in Nested Loops With Prolog-Epilog Merging *Mohammed Fellahi and Albert Cohen* *(INRIA)*
	A Flexible Code Compression Scheme using Partitioned Look-Up Tables *Martin Thuresson, Magnus Själander, Per Stenström* *(Chalmers University of Technology)*
16:00-18:00	SESSION III. Parallelism and Resource Control *CHAIR: Yiannakis Sazeides, U Cyprus*
	MLP-Aware Runahead Threads in a Simultaneous Multithreading Processor *Kenzo Van Craeynest, Stijn Eyerman, Lieven Eeckhout* *(Ghent University)*
	IPC Control for Multiple Real-Time Threads on an In-order SMT Processor *Jörg Mische, Sascha Uhrig, Florian Kluge, Theo Ungerer*

	(University of Augsburg)
	A Hardware Task Scheduler for Embedded Video Processing *Ghiath Al-Kadi, Andrei Sergeevich Terechko* *(NXP Semiconductors)*
	Finding Stress Patterns in Microprocessor Workloads *Frederik Vandeputte and Lieven Eeckhout* *(Ghent University)*

Day 2: January 27, 2009

8:30-10:00	SESSION IV. Communication *CHAIR: Andre Seznec, IRISIA/INRIA*
	Deriving Efficient Data Movement from Decoupled Access/Execute Specifications *Lee W. Howes (Imperial College London), Anton Lokhmotov (Imperial College London), Alastair F. Donaldson (Codeplay Software), Paul H.J. Kelly (Imperial College London)*
	MPSoC Design using Application-Specific Architecturally Visible Communication *Theo Kluter, Philip Brisk, Edoardo Charbon, Paolo Ienne* *(EPFL)*
	Communication Based Proactive Link Power Management *Sai Prashanth Muralidhara and Mahmut Kandemir* *(Pennsylvania State University)*
10:30-12:30	SESSION V. Mapping for CMPs *CHAIR: Per Stenstrom, Chalmers*
	Mapping and synchronizing streaming applications on Cell processors *Maik Nijhuis (University of Amsterdam), Herbert Bos (University of Amsterdam), Henri E. Bal (INRIA), and Cédric Augonnet (INRIA)*
	Adapting Application Mapping to Systematic Within-die Process Variations on Chip Multiprocessors *Yang Ding, Mahmut Kandemir, Mary Jane Irwin, Padma Raghavan (Pennsylvania State University)*
	Accommodating Diversity in CMPs with Heterogeneous Frequencies *Major Bhadauria (Cornell University), Vince Weaver (Cornell University), Sally A. McKee (Chalmers University of Technology)*
	A Framework for Task Scheduling and Memory Partitioning for Multi-Processor System-on-Chip *Hassan Salamy and Jagannathan Ramanujam* *(Louisiana State University)*

Day 3: January 28, 2009

9:00-10:00	KEYNOTE II Compilers in the manycore era *Francois Bodin, CAPS enterprises*
10:30-12:30	SESSION VI. Power *CHAIR: Mary Jane Irwin, PSU*
	Hybrid Super/Subthreshold design of a Low Power Scalable-Throughput FFT Architecture *Michael B. Henry, Leyla Nazhandali* *(Virginia Polytechnic Institute and State University)*
	Predictive Thermal Management for Chip Multiprocessors using Co-designed Virtual Machines *Omer Khan and Sandip Kundu* *(University of Massachusetts)*

	HeDGE: Hybrid Dataflow Graph Execution in the Issue logic *Suriya Subramanian and Kathryn S. McKinley* *(University of Texas at Austin)*
	Compiler Controlled Speculation for Power Aware ILP Extraction in Dataflow Architectures *Muhammad Umar Farooq, Lizy John, Margarida F. Jacome* *(University of Texas at Austin)*
14:00-15:30	SESSION VII. Cache Issues *CHAIR: Ben Juurlink, Delft*
	Revisiting Cache Block Superloading *Matthew A. Watkins (Cornell University), Sally A. McKee (Chalmers University of Technology), and Lambert Schaelicke (Intel Corporation)*
	ACM: An Efficient Approach for Managing Shared Caches in Chip Multiprocessors *Mohammad Hammoud, Sangyeun Cho, and Rami Melhem* *(University of Pittsburgh)*
	In Network Caching For Chip Multi Processors *Aditya Yanamandra, Mary Jane Irwin, Vijaykrishnan Narayanan, Mahumut Kandemir, Sri Hari Krishna Narayanan* *(Pennsylvania State University)*
16:00-17:00	SESSION VIII. Parallel embedded applications *CHAIR: Joel Emer, INTEL/MIT*
	Parallel LDPC Decoding on the Cell/B.E. Processor *Gabriel Falcão (University of Coimbra), Leonel Sousa (Technical University of Lisbon), Vitor Silva (University of Coimbra), José Marinho (University of Coimbra)*
	Parallel H.264 Decoding on an Embedded Multicore Processor *Arnaldo Azevedo (Delft University of Technology), Cor Meenderinck (Delft University of Technology), Ben Juurlink (Delft University of Technology), Andrei Terechko (NXP), Jan Hoogerbrugge (NXP), Mauricio Alvarez (UPC), Alex Ramirez (UPC,BSC)*

Conference attendance

The conference was attended by 198 participants, of which 17 from industry.

The attendants came from 23 different countries:

USA	23
Cyprus	22
Spain	21
France	19
Greece	14
UK	14
Germany	13
The Netherlands	13
Belgium	12
Italy	10
United Kingdom	10
Sweden	5
Norway	3
Portugal	3
Austria	2

Brazil	2
Finland	2
Israel	2
Poland	2
Russia	2
Switzerland	2
Romania	1
Scotland	1

While logically the number of attendants from the organising country (Cyprus) is high, we notice the high attendance from the USA. We also welcomed participants from Russia and Brazil.

Student Grants

This year we were able to give a grant to 36 students. This means that all students who applied for a grant received the registration fee grant.

Workshops and Tutorials

On January 25, the day preceding the conference, the HiPEAC clusters and task forces organised 7 workshops and 1 tutorial:

- GROW: GCC Research Opportunities Workshop
- 3rd Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip
- 2nd Workshop on Programmability Issues for Multi-Core Computers (MULTIPROG-2009)
- 1st Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO09)
- 3rd HiPEAC Workshop on Reconfigurable Computing WRC 2009
- 1st Workshop on Design for Reliability (DFR)
- 3rd Workshop on Statistical and Machine learning approaches to Architectures and compilation (SMART'09)
- Tutorial on Architecture Design for Soft Errors, Shubu Mukherjee, Intel Corporation

175 people attended the workshops:

GCC Research Opportunities Workshop	38
Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip	23
Workshop on programmability Issues for Multi-core Computers	38
Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools	24
Workshop on Reconfigurable Computing	22
Workshop on Design for Reliability	25
Workshop on statistical and Machine learning approaches to Architectures and compilation	39
Tutorial on Architecture Design for Soft Errors	24

Relatively spoken, more people have taken the opportunity to attend one of the workshops or tutorials compared to last year.

2.3. Conference Ranking

There is no easy way of ranking conferences as there is for journals, which are usually associated with impact factors based on the average number of citations. A systematic investigation of citation counts for the papers published in the HiPEAC conference is underway.

3. Task 3.2: Summer School

The successful international ACACES Summer School continues to be one of the most attractive events organised by HiPEAC.

The International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems is open to a wide audience, while we keep a balance between country, senior-junior, gender and industry-academia.

The Summer School programme consists of a combination of courses on the different topics covered by the HiPEAC research agenda. This is guaranteed by letting the different HiPEAC clusters suggest the best possible teachers for their own topic. This list of teachers is supplemented by topics considered to be of general interest to the whole network (e.g., dealing with cross-cutting concerns like power, reliability, …). The teaching staff consists of academics and industrial researchers, Europeans and non-Europeans alike. Former Summer School teachers normaly keep their links with the cluster that proposed them (as associate member).

Besides the courses, we organise a poster session where the PhD-students can present their own research to the other participants of the school. This is an excellent networking event for the young PhD students, which can lead to extra research ideas and contacts. During the summer school, the HiPEAC collaboration grant program is also presented to allow the students to further develop the newly made contacts.

During this poster session, we take the opportunity to present our network, and related FP6 and FP7-projects. Every project representative is available to give more information about their project.

3.1. 4th International Summer School – 2008

The Summer School

The fourth summer school was organised at the premises of Telecom Italia Learning Services (Tils), in L'Aquila, Italy. The Summer School started on July 13 and ended on July 19.

The 2008 Summer School was supported by HiPEAC1.

Location

One of the strengths of the Summer School is the location. Situated in the beautiful L'Aquila, the infrastructure provided by Telecom Italia is ideal for the vision we have for the Summer School.

Next to the spacious and modern classrooms, the location provides the participants ideal opportunities to meet and network.

Separate meeting rooms are available, as well as opportunities to relax and have well appreciated social events.

Another strong point of this location is that it is at a remote location. All attendants, teachers and organisation stay in the same venue during the entire week, tremendously increasing the opportunities for interaction.

Having senior researchers and the Summer School teachers available during the whole week is a major advantage of the summer school.

Summer School Program

The Summer School program consists of 12 courses, covering the research domains our network is focused on. As mentioned earlier, the clusters suggest the teachers for the Summer School.

Apart from the courses, the Summer School also offers a keynote speech, as wel as an invited talk from industry. We adjust the program's focus based on the feedback we receive from the participants.

The 2008 Summer School courses where:

	Lecturer	Course title
Slot 1	Mary Lou Soffa	Dynamic, Path and Model-Based Code Optimizations
	Chaitali Chakrabarti	Low Power System Design
	Josep Torrellas	Multiprocessor Architectures for Speculative Multithreading
Slot 2	Nikil Dutt	Bus-based On-Chip Communication Architectures
	Paolo Ienne	Automatic Customization of Embedded Processors
	Dean Tullsen	Multicore and multithreaded processor architectures
Slot 3	Luca Benini	Communication-dominated architectures: toward Networks on Chip
	Babak Falsafi	Bridging the Processor Memory Performance Gap
	Leendert Van Doorn	Virtualization Technologies
Slot 4	Olav Lysne	Multiprocessor Interconnection Networks; Routing, Fault Tolerance and Scalabilty
	Christos Kozyrakis	Transactional Memory: Concepts, Implementations, and Opportunities
	Wayne Luk	Reconfigurable Technology and Custom Computing

The keynote was given by **Yale Patt** (University of Texas at Austin). It was titled **"The Multi-core Era: What does it mean? (and even more importantly, what does it NOT mean?)"**.

The invited talk was given by **Peter Magnusson** (founder of Virtutech), titled **"What your mother should have taught you about entrepreneurship".** The topic and speaker were chosen as part of the initiative to promote start-ups in the HiPEAC network.

Poster session

On Wednesday afternoon, the yearly poster session was held. This poster session gives PhD students the opportunity to present and discuss their work with fellow students or with the senior researchers and teachers present at the Summer School.

The increasing number of posters displayed shows the appreciation of the PhD students for this event. 80 posters were presented during the afternoon and stayed on display until the end of the Summer School.

Besides the PhD-students, we also invited related FP6/FP7-projects to present their project to the community during the poster session.

We were happy to welcome posters presented by the following projects:

- MOSART
- MERASA
- EMUCO
- ACOTES
- MILEPOST
- VELOX

Attendance

For the 2008 edition, we received 376 applicantions.

In order to ensure the opportunity to succesfully network and interact we limit the number of participants to 200.

When selecting the participants, our focus is to maximise the goals of the network, and to balance the audience.

Selection criteria are:

- Gender: we stimulate female attendance to increase the gender-balance;
- Affiliation: all industry applicants are accepted in order to increase industry participation;
- Country: we try to get a maximum number of different nationalities in order to make it a truly international event;
- Experience: our goal is to have an optimal mix of senior researchers and young phd-students and postdocs.

The attendance-breakdown was as follows.

Industry attendance

We had 28 participants coming from 17 different companies:

Alcatel-Lucent Bell
Altera Corp.
AMD
Analog Devices Inc.
ARM
Caps Entreprise
CodeSourcery Inc.
Gemalto
IBM Haifa Labs
Indra Sistemas
Intel
NXP
Simula Labs
STMicroelectronics Ltd.
Thales Research & Technology
T-Mobile, Crnogorski Telekom A.D.
Virtutech

During the Summer School, there was a private industry meeting on the industrial challenges, chaired by the HiPEAC roadmap coordinator. Their input was reflected in the roadmap document that is currently being prepared.

Additionally, Intel organised a special and well-attended tutorial on their tools for the applicants.

Gender balance

18 out of 200 attendants are female. All female applicants were admitted and female students are certain to receive a grant.

Members/non-members

96 of the people who attended the summer school are members or affiliated:

- 24 members
- 61 affiliated PhD students
- 9 affiliated colleagues
- 2 staff members

Except for the teachers, half of the attendants had no direct affiliation with HiPEAC.

Summer School Grants

106 students applied for a student grant. The student grant waves the registration fee. 60 students were given a grant.

Feedback

Every year we ask all Summer School participants to give their feedback on the Summer School through an extensive survey. 142 People, or 71% filled in the survey. All scales go from 0 to 5; with 5 indicating the highest score.

Organisation

The administration (admission, registration, payment)	4,6
The website (organisation, content)	4,5
The course schedule (1 week, 4 slots, 12 courses)	4,4
The location (Telecom Italia Campus)	4,5
Shuttle busses (Rome-L'Aquila)	4,3
The course material (booklets)	4,2
Price/quality (990 euro, all-in, full week)	4,2
Period (last week of July)	4,2

The organisation was rated very highly. We continue to try to improve this aspect of the event.

The program

The course offering	4,2
The keynote talk on Sunday evening	4,5
The invited talk on Monday evening	4,1
The poster session	4,2

All aspects of the program were rated very highly. We continue to try to offer an attractive program and interesting speakers.

Overall appreciation

Would you recommend ACACES to a colleague?	4,8
Will you come back next year?	4,3

We were happy to see that people who filled out the survey were very eager to recommend the Summer School to their colleagues. The high score for the second question shows that there is great interest to attend the Summer School more than once.

Course evaluation

	Course	Teacher	Overall	Recommandation	Average
Mary Lou Soffa	4,2	4,4	4,3	4,2	4,3
Babak Falsafi	4,3	4,3	4,2	4,3	4,3
Wayne Luk	3,7	3,9	3,6	3,6	3,7
Chaitali Chakrabarti	4,2	4,2	4,1	4,1	4,1
Josep Torrellas	4,3	4,2	4,3	4,3	4,3
Nikil Dutt	4,4	4,5	4,4	4,4	4,4
Paolo Ienne	4,3	4,4	4,3	4,2	4,3
Dean Tullsen	4,1	4,2	4,1	4,1	4,1
Luca Benini	4,0	4,0	4,0	4,0	4,0
Leendert Van Doorn	4,3	4,4	4,3	4,3	4,3
Olav Lysne	4,1	4,1	4,2	4,2	4,2
Christos Kozyrakis	4,6	4,6	4,5	4,5	4,5

All courses were evaluated high to very high. The result of the evaluation forms was sent to the respective teachers, including the comments.

3.2. 5th International Summer School – 2009

The Summer School

The 2009 ACACES Summer School will be organised at the site of Telecom Italia, in L'Aquila, Italy. It will start on July 12, 2009 and end on July 18, 2009.

Location

The Summer School takes place at the same location as last year.

Summer School Program

One of the feedback points we received from the participants last year was the lesser presence of embedded-oriented courses.

When constructing this year's programme, we took this feedback into consideration:

	Lecturer	**Course title**
Slot 1	David Albonesi	Power- and Reliability-Aware Microarchitecture
	Wailid Najjar	Opportunities and Challenges of Reconfigurable Computing
	Peter Puschner	WCET Analysis: Problems, Methods, and Time-Predictable Architectures
Slot 2	Jaejin Lee	Compilers and Runtimes Support for Explicitly Managed Memory Hierarchies
	Radu Marculescu	Networks-on-Chip: Why What, and How?
	Paul McKenney	Performance, Scalability, and Real-Time Response From the Linux Kernel
Slot 3	David Wood	Transactional Memory
	Grant Martin	Practical System-Level Design Methodologies for Processor-Centric SoC and Embedded Systems
	Kim Hazelwood	Process Virtualization and Symbiotic Program Optimization
Slot 4	Bruce Jacob	Embedded Systems, Memory Systems, and Embedded Memory Systems
	J. (Ram) Ramanujam	Optimizations for multicore and GPGPU architectures
	Lieven Eeckhout	Performance Evaluation and Benchmarking

The keynote will be given by **Steven Furber, University of Manchester.**

This year we will again organise a poster session.

4. Task 3.3: HiPEAC Journal

The HiPEAC Journal was first published in 2006. Its fourth volume is currently being prepared.

The HiPEAC journal differentiates itself from other publications in that it has a three-month reviewing cycle. Every accepted paper is also immediately published on the HiPEAC website.

The third volume of the journal received 22 submission, of which 14 were accepted for publication.

Accepted papers

Volume 3 accepted the following papers:

Dynamic Cache Partitioning Based on the MLP of Cache Misses	Miquel Moreto, Francisco J Cazorla, Alex Ramirez, Mateo Valero *(UPC/BSC)*
Cache Sensitive Code Arrangement for Virtual Machine	Chun-Chieh Lin, Chuen-Liang Chen *(National Taiwan University)*
Data Layout for Cache Performance on a Multithreaded Architecture	Subhradyuti Sarkar, Dean M. Tullsen *(University Of California)*
Improving Branch Prediction by considering Affectors and Affectees Correlations	Yiannakis Sazeides, Andreas Moustakas, Kypros Constantinidis, Marios Kleanthous *(University of Cyprus)*
Exploring the Architecture of a Stream Register-Based Snoop Filter	Matthias Blumrich, Valentina Salapura and Alan Gara *(IBM Thomas J. Watson Research Center)*
GROB: Implementing a Large Instrucion Window though Compression	F. Latorre, G. Magklis, J. Gonzalez, P. Chaparro, A. Gonzalez *(Intel Barcelona)*
Power-Aware Dynamic Cache Partitionning for CMPs	Isao Kotera, Kenta Abe, Ryusuke Egawa, Hiroyuki Takizawa, and Hiroaki Kobayashi *(Tohoku University, Japan)*
A Multithreaded Multicore System for Embedded Media Processing	Jan Hoogerbrugge and Andrei Terechko *(NXP Semiconductors)*
Parallelization Schemes for Memory Optimization on the Cell Processor : A Case Study on the Harris Corner Detector	T. Saidani, L. Lacassagne, J. Falcou, C. Tadonki, Samir Bouaziz *(Universite de Paris Sud)*
Constructing Application-specific Memory Hierarchies on FPGAs	H. Devos, J. Van Campenhout, I. Verbauwhede, D. Stroobandt *(Ghent University)*
autopin – Automated Optimization of Thread-to-Core Pinning on Multicore Systems	Tobias Klug, Michael Ott, Josef Weidendorfer, and Carsten Trinitis *(Technische Universitat Munchen)*
Robust Adaptation to Available Parallelism in Transactional Memory Applications	Mohammad Ansari, Mikel Luján, Christos Kotselidis, Kim Jarvis, Chris Kirkham, Ian Watson *(University of Manchester)*
Efficient Partial Roll-backing Mechanism for Transactional Memory Systems	M. M. Waliullah *(Chalmers)*
Software-Level Instruction-Cache Leakage Reduction using Value-Dependence of SRAM Leakage in Nanometer Technologies	Maziar Goudarzi, Tohru Ishihara, Hamid Noori *(Kyushu University, Fukuoka, Japan)*

5. Task 3.4: HiPEAC Roadmap

The first HiPEAC roadmap was published in 2007. The steering committee has taken the opportunity of HiPEAC2's launch to start the discussion and brainstorming on creating a new up-to-date roadmap.

The first steps to create the new roadmap, which is currently approaching its first draft, were taken at the cluster level. Every cluster was asked to present their vision on the future of the their research domain.

Because we consider industry input for the roadmap vital to the relevance of the document, a brainstorming session was organised at the Summer School. This event gathered the input of 28 company people, giving the view of 17 companies.

This large amount of data was then further processed by a roadmap committee, including industry.

The result of this convergence was presented at the pre-review in Paphos, and to the community at the general assembly meeting. The feedback was used to create a second draft which will be presented at the review meeting of the first year of HiPEAC.

6. Task 3.5: HiPEAC Newsletter

The newsletter workgroup is currently preparing the 18th issue. The issues are printed quarterly and mailed around the world.

The last newsletter issue had a circulation of 725 copies.

One new feature of the newsletter is the inclusion of guest columns, where respected members or member institutions get the opportunity to present their work and the relevance of HiPEAC for their institution.

The newsletter also serves as a dissemination tool to present the HiPEAC start-ups.

The volume of the newsletter has grown from an average of 12 pages to 16-20 pages.

We automatically include all new members.

6.1. Period 1 issues

During the reporting period, 4 issues of the HiPEAC newsletter were printed:

Issue 14: April 2008 (12 pages)

- Message from the HiPEAC coordinators
- In the Spotlight
  - Second Edition “Antiguos Alumnos UPV”
- Message from the project officer
- Hipeac Activity
  - HiPEAC Computing Systems Week
  - 5th HiPEAC Industrial Workshop
- Guest Column
  - Grant Martin, Chief Scientist, Tensilica, Inc.
  - ALaRI – University of Lugano
- HiPEAC Start-ups
- Promotion of HiPEAC start-ups
- PHD News
- Upcoming Events

Issue 15: July 2008 (16 pages)

- Message from the HiPEAC coordinators
- Message from the project officer
- Community News
- In the Spotlight
  - EC FP7 STREP Project VELOX
  - BSC and Microsoft Create Joint Research Centre in Barcelona for Parallel Computing
- Guest Column
  - SHAPES and its DIOPSIS Tile
  - Tsuyoshi Isshiki, Tokyo Institute of Technology
- HiPEAC Activity

    - HiPEAC Research Collaborations
- HiPEAC Start-ups
- PHD News
- HiPEAC Students
- Upcoming Events

Issue 16: October 2008 (20 pages)

- Message from the HiPEAC coordinator
  Community News:
    - Multicore days in Stockholm, Sweden
    - Awards and new books
- Message from the project officer
- HiPEAC Activity:
    - HiPEAC 2009 Conference
    - HiPEAC Fall Computing Systems Week
    - HiPEAC 6th Industrial Workshop
- In the Spotlight:
    - Good bye and Thanks Sylvie! Hello and Welcome Klaas!
    - EC STREP FP7 Apple-Core Project
    - EC STREP FP7 eMuCo Project
- Guest columns:
    - Norbert When, University of Kaiserlauten
    - Gerd Ascheid, RWTH Aachen University
- HiPEAC Start-ups

Issue 17: Januari 2009 (16 pages)

- Message from the HiPEAC coordinator
- Message from the project officer
- HiPEAC Activity:
    - HiPEAC Journal papers
    - ACACES 2009
    - First Workshop on Network on Chip Architectures (NoCArc2008)
    - HiPEAC Recorded Seminars
    - Promotion of HiPEAC Start-ups
- In the Spotlight:
    - ArchExplorer.org
    - EC FP6 STREP MILEPOST Project
    - EC FP7 STREP MULTICUBE Project
- Community News
    - Daniel Litaize (1945-2008)
    - New member: Javier Castillo
    - NVIDIA CUDA Challenge Award
    - Mateo Valero, among the 25 most influential scientists in Europe
    - New Book
    - Success for TM in GCC Project
- HiPEAC Start-ups
- HiPEAC Students and Trip Reports

- Phd News
- Upcoming events

7. Task 3.6: HiPEAC Technical Reports

HiPEAC technical reports are web-based time stamped internal reports. The goal of the technical reports is to publish the ideas of European researchers as soon as they mature, and make sure that ideas are credited to the original contributor.

The process of publishing an idea in the HiPEAC technical reports is lightweight. It suffices to submit an internal report to the HiPEAC website where the editor of the HiPEAC technical reports will quickly evaluate whether the idea is good enough to be put on the HiPEAC website. If so, the report is immediately published on the website, with the time stamp of the moment the document was submitted to the website.

7.1. Publication database

The first step related to the technical reports was to create a publication database.

This database is a list of all publications by a HiPEAC member or affiliate. While the database is mostly automatically generated, users have the possibility to contribute to the database, by insterting publications manually or by requesting changes to existing publications.

These publications are unfortunately not all related to direct HiPEAC work. It is therefore the task of the cluster coordinators to select those publications that present an accurate overview of cluster and task force activities. An easy-to-use interface was created to facilitate this process.

Our database currently holds 4870 publications:

2005	1128
2006	1212
2007	1296
2008	1182
2009	52

7.2. Tech Reports

The technical staff is working closely together with the tech reports coordinator to create a prototype of the mechanism.

The published idea can be made either public or private, depending on the rights given by the publisher. The author holds responsibility for the technical content and copyright. It is not the intention that a tech report is used for citation or reference. As soon as the idea is accepted as a paper it can be cited, and it will be transferred to the publication database.

The uploaded document is read-only. The service will guarantee that no adjustments can be made to the document once it is uploaded.

A discussion forum where people can discuss the contents of the tech report will be available.

The technical reports will not be published nor announced in the newsletter. Visibility for the idea should come from a successful publication. It is only available to HiPEAC members.

From a technical point of view, both commercial and open source solutions are available. As we are intending this service to be lightweight, we are looking into the open source alternatives (Open TSA, Digital Timestamping Service).

8. Task 3.7: Web Site

The HiPEAC web site is the most important instrument for HiPEAC's internal and external communication. It serves both as an extranet to disseminate information, as an intranet to disseminate research information among participants, and to provide the members and affiliates with the necessary information and tools. Several services have been added during the last year: the reimbursement service, the registration system for meetings, membership management, a publication database, the membership services, a reorganisation of the mailing lists, ...

During the coming reporting period, the website will get a major visual update, in order to better indicate the new project structure and to increase its potential use to external academics and companies.

8.1. Developments

During the first reporting period, the technical staff has made the following changes to the website.

New Drupal version

At the beginning of the new project, the underlying technology of the website, the CMS called Drupal, was upgraded from version 4.6 to version 5.3. All modules have been translated to be fully functional under the new version. This update allows members to more easily create content for the website by using simpler forms.

Membership

- The members' accounts have been improved to let each member easily manage his affiliate members and HiPEAC PhD students;
- A system of logs has been implemented to record all the actions performed on the users accounts. These logs are sent to the membership managers and also recorded in a table of logs visible to the SC members;
- A system to propose new members by the SC and HiPEAC coordinators has been created. This facilitates and structures the proposal of and decision on new member requests;
- The members' accounts have been improved. Now each member can have two affiliations;
- A system to send mails automatically when someone is accepted as member was added;
- For the cluster coordinators, an overview screen has been created with all the members, containing information about their cluster attendance, Summer School attendance and conference attendance. For each person they can also see more detailed information (for example whether the person requested an internship, a reimbursement request, a collaboration grant....);

- The public member list was improved. A world map has been added with an overview of all members. A sort and filter mechanism was added as well. The results of selections can be downloaded as a CSV file.

Steering Committee Meetings

- A flexible system has been added to manage the SC meetings, making it easy to compose the agenda, add relevant attachments and insert the minutes.
- Webex is now used for the meetings, and special help pages have been written (see http://www.hipeac.net/webex for more details).

Reimbursement module/Finance Overview

As described in the management report, the reimbursement module has been created to have a lightweight application to manage the project's fundings and reimbursements.

For the SC, a transparant financial overview was created.

Newsletter features

- Implementation of a new address book. Every SC member can modify or add new members to the address book.
- Possibility to download a CSV list of the complete address book.

Website groups

It is possible to create a private group on the HiPEAC website for collaborative work. Such a group provides:

- The possibility to make some kind of "wiki pages" which
  - can be modified by all the members of the group;
  - are by default private (i.e. only visible for the members of the group);
  - can be made public by modifying the audience (see below).
- A mailinglist @hipeac.net
- An SVN directory

Each of the research clusters and task forces of HiPEAC has a group. These groups are moderated by the coordinators of the each cluster/task force. It is also possible for coordinators to create sub-mailing list for their own group.

Google Analytics

At the start of HiPEAC2, Google Analytics was installed to have a more detailed overview of the visits and results of the website. The data provided can be found in the section below.

Web Seminars

A module was installed to count the downloaded seminars. For the next reporting period a more up to date and interactive web seminar system will be implemented.

Press Communications

A separate press section was created, to facilitate giving an overview of HiPEAC's appearance in press.

Progress Indicators

The progress indicators as described in the DoW are now visible on one page. This allows the SC members to easily track evolution of the progress indicators.

Publication database

The technical staff implemented a module that automatically mines publications from the DBLP and ACM database, adds them to the HiPEAC database with semi-automatic linking to the HiPEAC user. Members and users have the possibility to add, reject or adjust the data present in the database. If the user chooses to, he can upload a pdf with an abstract or full text to the publication. Every activity on the database is logged.

Company mailinglist

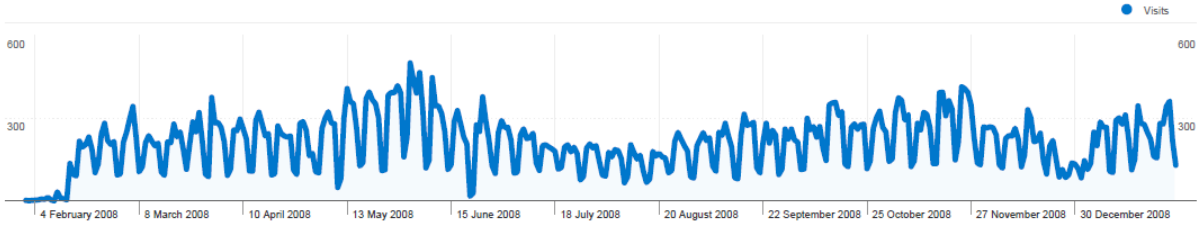
A separate mailinglist and web page containing all the company members' emails has been created.

8.2. Website numbers

Since February 2008, we use Google Analytics to keep track of the website visits and data.

The most important metrics will be discussed.

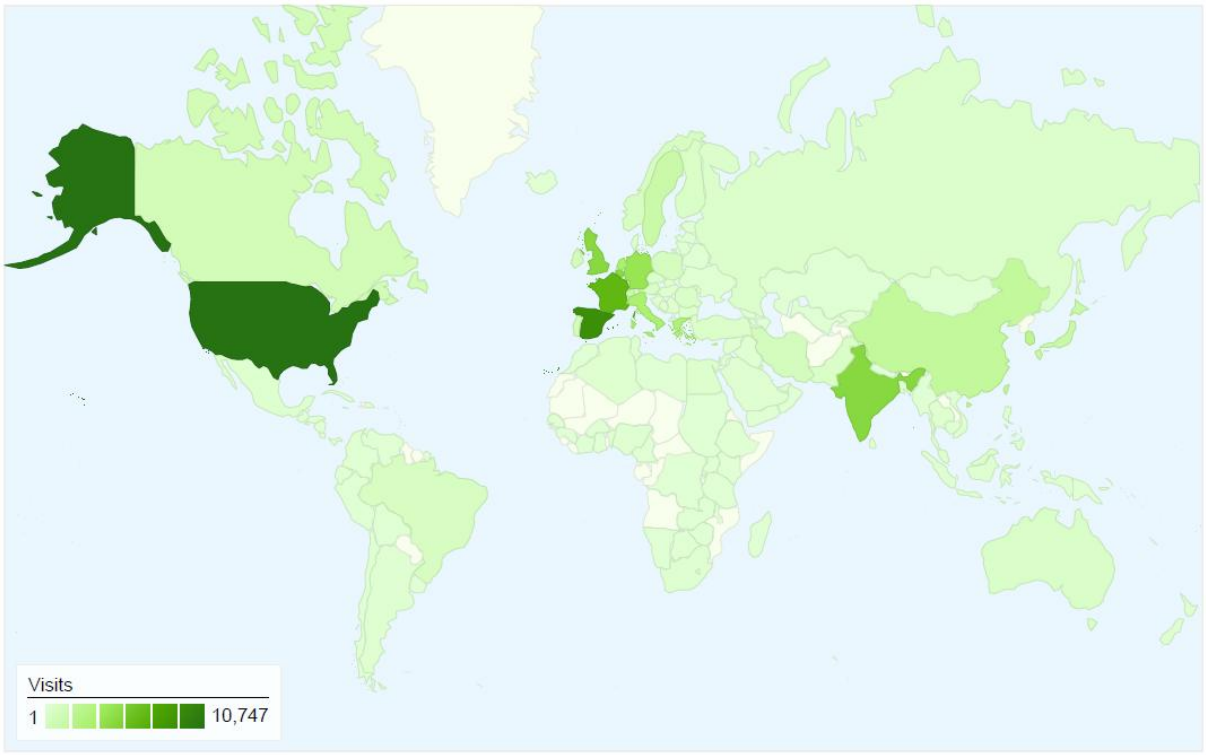
Visitors Report



In the period covered by the report, Google enabled us to report the following numbers

Visits	77 216
Unique visitors	40 563
Page Views	301 867
Avg Pages/visit	3.91
New visits	51,74%

The visitors come from 152 different countries:



United States	10.747	20%
Spain	8.886	17%
France	6.490	12%
India	4.818	9%
United Kingdom	4.753	9%
Belgium	4.684	9%
Germany	4.129	8%
Netherlands	3.165	6%
Italy	3.142	6%
Greece	2.886	5%

The main interest comes from the United States. The second most visitors come from Spain, also the country with the largest number of members in our network. A large number is also coming from India.

The numbers also show we have a high percentage of new visitors.

The average page count of a website visitor is 3.91, meaning the general visitor looks at almost 4 pages before leaving.

Visit length and depth

The average visitor spends more than 3 minutes on the site, visiting nearly 4 pages before leaving. However, more than half of the visitors spend less than 20 seconds on the website.

Registrations

In the first period of HiPEAC2, our website welcomed 461 new registrants.

8.3. Conclusions and future work

Although the website has been significantly improved throughout the years, the improvements were mainly aimed towards providing a better service for the members and affiliates. Several developments such as the publications database, the reimbursement system and the cluster meeting registrations are much appreciated by the members. A lot of improvements were made under the hood, which are indeed not visible to the outside world.

Due to our focus on providing our members with better services, the external view of our website needs updating.

The website should reflect more the new structure and vision of the network, and have a more focused approach towards industry.

These changes however need time and careful input from users and industry. In order to do this, the website's coordinator has gathered a task force to work on the website.

9. Task 3.8: Web Seminars

The goal of these joint seminars is to increase integration of different research groups by enabling frequent interaction, and facilitate presentations of their research work.

Recorded Web Seminars

During this period, 3 seminars (two from Industry) have been broadcasted from UPC to all HiPEAC members:

NVIDIA CUDA Software and GPU Parallel Computing Architecture	David Kirk (NVIDIA)	April 16, 2008	10
Industrial and Research Challenges in the Area of Multi-Core and Many Cores	Avi Mendelson (Intel)	December 19, 2008	20
Thermal Modeling, Analysis and Management of Multi-Processor Systems-on-Chip	David Atienza (Universidad Complutense de Madrid, EPFL)	January 7, 2009	7

(Note: numbers were only recorded since October 2008).

Streamed Web Seminars

Some Web seminars were not recorded due to authorisation issues or technical issues. They were only available through live streaming.

1. Ayose Falcón - Daniel Ortega (HP Labs, Barcelona): COTSon: Infrastructure for system-level simulation (30 January 2009)
2. David Brooks Harvard University Computer Design in the Nanometer Scale Era: Challenges and Solutions (15 July 2008)
3. Vasanth (Vas) Bala IBM T.J. Watson Research Center Management of Virtualized Environments: An IBM Research perspective (8 July 2008)

4. Frederica Darema National Science Foundation (NSF) Dynamic Data Driven Applications Systems (30 May 2008)
5. Sally McKee School of Electrical and Computer Engineering, Computer Systems Lab, Cornell University Efficient, Accurate Design Space Exploration (15 May 2008)
6. Valentina Salapura IBM Thomas J. Watson Research Center, Yorktown Heights, NY: Scaling Up Next Generation Supercomputers (8 May 2008)
7. Javier Setoain Rodrigo ArTeCS, Departamento de Arquitectura de Computadores y Automática de la Universidad Complutense de Madrid Análisis de imágenes hiperespectrales: extracción automática de endmembers (11 April 2008)
8. Emery Berger Deptartment of Computer Science, University of Massachusetts, Amherst: Resilient Runtime Systems (4 April 2008)
9. Ghuloum, Anwar Ct: C for Throughput Computing (10 March 2008)
10. David A. Bader Georgia Institute of Technology Petascale Computing for Large-Scale Graph Problems (5 March 2008)

10. Task 3.9: Industrial Workshops

This activity, that started during HiPEAC1, aims to increase relevance of the HiPEAC research to industry, and to strengthen the relationships between industrial and academic organisations.

The participating companies organise an Industrial Workshop twice a year, once in spring and once in fall. The Industrial Workshop is organised in conjunction with the cluster meetings.

10.1. Spring Industrial Workshop

The Workshop

The spring industrial workshop was organised by **HP Labs** in Barcelona, on June 4, 2008, during the Computing Systems Week.

The host of the event was the Exascale Lab of HP.

Workshop program

A keynote was given by **Hans Boehm** of HP Labs, titled ‘Getting C++ threads right”.

12 publications out of 16 were selected for the workshop. The HP Labs team contributed to the review process and the decision of the final program.

The program follows.

Session 1 – Compilation and Code Generation	*Compiling C to CLI for Heterogeneous Multicore System-on-Chips*	Erven Rohou, Andrea Ornstein and Marco Cornero *(ST Microelectronics)*
	Programming Multicore Systems Using Hierarchically Tiled Arrays	Diego Andrade *(U of A Coruna)*, James Brodman *(U of Illinois)*, Basilio B. Fraguela *(U of A Coruna)* and David Padua *(U of Illinois)*
	Polyhedral code generation for GPUs	Piotr Lesnicki, Cedric Bastoul, Albert Cohen, DaeGon Kim and Louis-Noel Pouchet *(INRIA)*
	Automating generation of data movement code for parallel	Lee Howes, Anton Lokhmotov, Paul Kelly *(Imperial College)*

	architectures with distributed memories	and Alastair Donaldson *(Codeplay)*
Session 2 – Tools	*COTSon: infrastructure for system-level simulation of clustered multicores*	Eduardo Argollo, Ayose Falcon, Paolo Faraboschi and Daniel Ortega *(HP Labs)*
	A Tool Environment for Data Locality Optimization on Chip-Multiprocessors	David Kramer, Oliver Mattes, Rainer Buchty and Wolfgang Karl *(U of Karslruhe)*
	Clock Synchronization in Cell BE Traces	Marina Biberstein, Yuval Harel and Andre Heilper *(IBM Haifa)*
	A Dynamic Analysis Tool for Finding Coarse-Grain Parallelism	Sean Rul, Hans Vandierendonck and Koen De Bosschere *(U Gent)*
Session 3 – Methodology	*CAPSULE: A Symbiotic Hardware/Software Approach for Facilitating the Parallelization of Programs with Complex Control Flow and Data Structures*	Olivier Certner, Zheng Li and Olivier Temam *(INRIA)*
	MAPS: An Integrated Framework for MPSoC Application Parallelization	Weihua Sheng, Jeronimo Castrillon, Jianjiang Ceng, Hanno Scharwaechter, Rainer Leupers, Gerd Ascheid, Heinrich Meyr (*RWTH Aachen)*, Tsuyoshi Isshiki and Hiroaki Kunieda *(Tokyo Tech)*
	On-chip memories, the OS perspective	Carlos Villavieja, Isaac Gelado, Alex Ramirez and Nacho Navarro *(UPC BSC)*
	Overhead of the spin-lock loop in UltraSPARC T2	Vladimir Cakarevic, Petar Radojkovic, Francisco Cazorla, Robert Gioiosa, Mario Nemirovsky, Mateo Valero, Manuel A. Pajuelo Gonzalez and Javier Verdu *(UPC-BSC)*

Workshop Attendance

The workshop at HP was attended by 121 people, of which 41 members, 36 affiliated PhD students and 28 affiliated colleagues. In addition, 25 HP engineers attended.

Of the 121 people not from HP Labs Barcelona, 16 people from industry were present, representing the following companies:

- NXP
- Thales
- Infineon
- ST Microelectronics
- Alcatel Lucent
- Ericsson
- ARM
- HP

Participants' Feedback

The participants of the workshop were asked for their feedback on the event.

40 attendants filled out the survey, about 1/3 of the participants.

	Low	Neutral	High
Industrial Workshop at HP Labs	0	21	19

Nobody gave a low rating for the workshop. The average rating is 2.38 out of 3.

In the comments, the industry presence was very much appreciated. Some participants indicated they expected more senior industry participation.

Host's Feedback

The host of the industrial workshop, also provided feedback on the event:

The outcome of the whole Industrial Workshop has been very positive for HP. Despite the intense organizational effort having this workshop at HP premises was the correct decision. We had the opportunity to establish many interesting connections with the HiPEAC community. In particular, this was an excellent way to expose our current research work and help us establish very strong relationship. Some of these are already starting to show important outcomes in facilitating the formation of consortia around project ideas that will target the upcoming FP7 calls. In general, we believe that these workshops are a good instrument to help bridge the gap between academic and industrial research.

10.2. Autumn Industrial Workshop

The workshop

The autumn industrial workshop was organised by Thales Research & Technology in their lab located near Paris, France. The event took place on November 26, 2008. The workshop was concluded with a social event sponsored by Thales.

Workshop program

Two keynotes were given by Thales engineers:

Keynote 1:Multicores make our lives harder

Eric Lenormand, Philippe Bonnot

In its wide range of mission critical embedded systems in the areas of aerospace, defense and security, and in particular in computation intensive domains close to the sensors, Thales has many requirements on computing architectures and design tools. While the advent of multi-cores offers a lot of opportunities in term of efficiency and performance, it exacerbates some problems that were already pending with single core architectures. Examples are real-time predictability, dependability, and industrial software design process. This talk will provide an overview of the different applications in the domain, the constraints we are facing as well as the tools and architectures we develop or use in the domain.

Keynote 2:Can we afford customization?

Fabrice Lemonnier, Sami Yehia

Beside parallelism, specialization and customization of processors are another path to more efficiency and performance. Looking at the spectrum that covers, on one extreme, the very

efficient but expensive ASICs to highly programmable accelerators, where general-purpose processors reside at the other extreme, a right balance is to be found. This talk will cover different points of this flexibility/efficiency spectrum through different solutions and research in this area.

The entire program of the workshop follows.

Session 1: Real time and fault tolerant architectures	Mitigating the Performance Degradation due to Faults in Non-Architectural Structures	Constantinos Kourouyiannis *(U of Cyprus)*, Yiannakis Sazeides *(U of Cyprus)* and Veerle Desmet *(U Gent)*
	Schedulability of Real-Time Fault-Tolerant Systems Using Multi-cores	Risat Mahmud Pathan, Jan Jonsson and Johan Karlsson *(Chalmers)*
Session 2: Multicores and memory architectures	A run-time configurable cache/scratchpad memory with virtualized user-level RDMA capability	George Nikiforos, George Kalokairinos, Vassilis Papaefstathiou, Stamatis Kavadias, Dionisis Pnevmatikatos and Manolis Katevenis *(FORTH)*
	Power-Efficient Scaling of CMP Directory Coherence	Stefanos Kaxiras, Georgios Keramidas, Ioannis Oikonomou and Athanasios Tollos *(U of Patras)*
	Dynamic System-Level Optimization in MulticoreArchitectures: The Example of Hardware Task Allocation	T. Theocharides *(U of Cyprus)*, M. K. Michael *(U of Cyprus)*, M. Polycarpou *(U of Cyprus)* and A. Dingankar *(Intel)*
Session 3: Customization and Application partitioning	Early Evaluation of Predictive Code Scheduling for Heterogeneous Architectures	Víctor J. Jiménez *(UPC)*, Lluís Vilanova *(UPC)*, Isaac Gelado *(UPC)*, Marisa Gil *(UPC)*, Grigori Fursin *(INRIA)* and Nacho Navarro *(UPC)*
	Sub-Algorithms: Suitable Entities for Execution on Co-processors	Sean Rul, Hans Vandierendonck and Koen De Bosschere *(U Gent)*
Session 4: Methodology and tools	Opening Up Automatic Structural Design-Space Exploration by Fixing Modular Simulation	Veerle Desmet *(U Gent)*, Sylvain Girbal *(INRIA)* and Olivier Temam *(INRIA)*
	Development of a Virtual Platform using the 'Chumby' Device as Case Study	Stefan Kraemer, Xiaowei Pan and Rainer Leupers *(RWTH Aachen)*
	Analyzing scalability limits of H.264 decoding due to TLP overhead	Mauricio Alvarez *(UPC)*, Arnaldo Azevedo *(TU Delft)*, Cor Meenderinck *(TU Delft)*, Ben Juurlink *(TU Delft)*, Andrei Terechko *(NXP)*, Jan Hoogerbrugge *(NXP)* and Alex Ramirez *(UPC)*

Workshop Attendance

104 people attended the industrial workshop. Also, 20 researchers from Thales Research & Technology attended the meetings.

Of the 104 people, 36 are HiPEAC members, 17 are affiliated phd students and 18 are affiliated colleagues.

Apart from Thales Paris researchers,19 industry affiliates attended the workshop, representing the following companies:

- IBM
- ARM
- Thales
- Transitive
- Microsoft
- Intel
- NXP
- ST Microelectronics
- Alcatel-Lucent

Host's feedback

After the event, the host provided his feedback on the impact of organising the event:

The Embedded Systems Lab at Thales Research and Technology (TRT) had the pleasure to host the HiPEAC cluster meeting and organize the 6th HiPEAC industrial workshop. This opportunity, given by the HiPEAC NoE, was received at the lab with great enthusiasm and commitment. It was also seen as major opportunities for TRT to expose the company, its role in the industry as a major actor in electronic systems dedicated to aerospace, defence and security and its different technologies that directly address the Architectures, compilers and embedded systems community interests and concerns.

-Some numbers

The event lasted for 5 days, where TRT hosted related FP6/FP7 project meetings during the first two days, organized the industrial workshop on the 26th of November and then hosted the HiPEAC cluster meetings on the 27th and 28th of November. A total of 158 people registered for the event and could benefit from the facilities to exchange, attend talks and meetings and hold private meetings in some rooms dedicated for that. Also it is worthwhile noting that, since the TRT building is relatively recent, it was the first time TRT hosted such a number of people. This gave a great visibility of the HiPEAC community to the different divisions and departments of TRT and also confirmed Thales as a major European industrial actor in embedded systems and architectures that address the security, defence and aerospace applications.

-Industrial workshop

Over 100 people attended the 6th industrial workshop as well as almost all engineers and researchers from the Embedded Systems Lab. TRT chosen a theme directly related to its industrial and research concerns: "Domain specific, real time and safety critical embedded systems in the multi-core era". During this workshop we accepted 10 papers related to the subject and organized two keynotes presented by different engineers and researchers from the Embedded System Lab at TRT. This larger space dedicated to the industrial needs, concerns, requirements and specific case studies from the industry gave a broader view and initiated a

lot of interactions and networking between industrial actors, researchers as well as PhD students attending the event. Two 40-minutes keynotes where dedicated to the interests of Thales in the domain, the first one addressed the problem of safety critical and hard real time applications in the multi-core era, and the other about application specific architectures and accelerators. Both keynotes where later subject too many discussions during the following cluster meetings.

-Feedback from the HiPEAC community

Since Thales is not a direct producer of general-purpose architectures, processors and consumer electronics products, many of the attendees were surprised to discover a large multinational company (70000+ employees) mainly based in Europe which have specific industrial requirements, advanced technologies in the field of security and mission critical embedded systems and needs that are of direct concerns to the HiPEAC community. The feedback we had was very positive in term of organization, topics discussed during the industrial workshop and impact on the upcoming research in the domain.

-Return for Thales

Hosting the cluster meeting and the industrial workshop was a unique opportunity for Thales to present itself as a major actor in the domain of embedded computing systems, especially for mission critical, defence and security systems. The event allowed the company to show the different technologies it has and that are of direct interest to the HiPEAC community and showed how the different concerns we have can directly shape and impact the European research community in the domain of embedded as well as high performance architecture.

Internally, the presence of more than 150 researchers in the premises of Thales drew the attention of the different labs and divisions on the role of the Embedded Systems Lab, the role Thales can have in impacting the research and technologies of embedded systems and the existence of very strong community in Europe, represented by HiPEAC, around the topics of computing systems, processors architectures and embedded systems.

-Cooperation impact

Many common interests emerged from the industrial workshop and the cluster meeting. The concerns Thales exposed in term of real time, security and safety critical issues in embedded systems opened the way to many potential cooperation and synergies between industrial and academics, and between the industrials themselves. Currently (Dec 08), the lab is discussing several potential FP7 proposals with several academic partners in the domain that emerged during the event.

-Social event:

Being aware of the unique opportunity presented to interact with the lead researchers and academics in the domain of architectures, compilers and embedded systems of the HiPEAC community, Thales organized a social event around a dinner to promote the interaction between Thales researchers and engineers and the HiPEAC research community.

11. Task 3.10: Promoting HiPEAC Start-Ups

This task aims to stimulate members to create new start-ups by organising one yearly event. Additionally, we embrace start-up companies by quasi-automatically inviting them as member companies, so they get access to all the resources of the network. By promoting these companies, we hope to contribute to their success.

This is the list of HiPEAC Start-Ups:

Acumem	http://www.acumem.com/pub/	Erik Hagersten
Caps Enterprise	http://www.caps-entreprise.com/	François Bodin
Nanochronous	http://www.nanochronous.com/home/	Manolis Katevenis
Nema Labs	http://www.nemalabs.com/	Per Stenström
QuviQ	http://www.quviq.com/	John Hughes
Splitted desktop	http://www.splitted-desktop.com/fr/	Olivier Temam
INOCS	http://www.inocs.com	Federico Angiolini
Kalray	http://www.kalray.eu	Benoît Dupont de Dinechin

In order to promote the start-ups, **Peter Magnusson**, founder of **Virtutech** was asked to give a keynote speech on start-ups at the ACACES Summer School. His speech was titled *"What your mother should have taught you on entrepreneurship".*

A presentation of the HiPEAC start-ups promotion activity was published in the HiPEAC Info 14, April 2008.

Deeper presentations of each start-up have appeared in the next HiPEAC Infos, two start-up's at a time. We have currently presented Acumem, CAPS-Enterprise, Nanochronous, Nema Labs and Quviq in HiPEAC Info 15, 16 and 17.

Since October, the coordinator of this task, Marco Cornero, left the consortium. The coordination of this task has, since the second period of HiPEAC, been taken over by the new partner, ST Grenoble, and its responsible scientist, Christian Bertin.

12. Task 3.11: HiPEAC Award

In our domain, the best possible means for achieving international visibility is to publish in, to be a program committee member of, or even to organise a major conference.

The HiPEAC award program aims to encourage the members to publish their work in one of the selected conferences (based on the quality of the conference, and the relative low number of European papers in these conferences).

12.1. Selected conferences

The SC agreed to stimulate publishing in one of the following conferences:

- Symposium on Principles of Programming Languages (POPL)
- Conference on Programming Language Design and Implementation (PLDI)
- Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)
- International Symposium on Computer Architecture (ISCA)
- International Symposium on High Performance Computer Architecture (HPCA)
- Symposium on Field-Programmable Custom Computing Machines (FCCM)
- Design Automation Conference (DAC)
- Symposium on Microarchitecture (MICRO)

The award consists of a certificate and a financial award of **€ 1000**.

12.2. 2008 results

In 2008, 15 papers were eligible for the paper award:

Conference	# Papers eligible
POPL	0
PLDI	1
ASPLOS	1
ISCA	2
HPCA	2
FCCM	2
DAC	5
MICRO	2

List of eligible publications

These publications by HiPEAC members are published at the selected conferences:

Paper Title	Authors	Conference
Iterative Optimization in the Polyhedral Model: Part II, Multidimensional Time	Louis-Noel Pouchet, Cedric Bastoul, John Cavazos and Albert Cohen	Programming Language Design and Implementation 2008
Dispersing proprietary applications as benchmarks through code mutation	Luk Van Ertvelde and Lieven Eeckhout	Architectural Support for Programming Languages and Operating Systems
A Two-Level Load/Store Queue based on Execution Locality	Miquel Pericàs, Adrian Cristal, Francisco J. Cazorla, Ruben González, Alex Veidenbaum, Daniel A. Jiménez and Mateo Valero	International Symposium on Computer Architecture 2008
Software-Controlled Priority Characterization of POWER5 Processor	Carlos Boneti, Francisco J. Cazorla, Roberto Gioiosa, Alper Buyuktosunoglu, Chen-Yong Cher and Mateo Valero	International Symposium on Computer Architecture 2008
Runahead Threads to Improve SMT Performance	Tanausu Ramirez, Alex Pajuelo, Oliverio J. Santana and Mateo Valero	High-Performance Computer Architecture 2008
An OS-Based Alternative to Full Hardware	Christian Fensch and Marcelo	High-Performance Computer

Coherence on Tiled CMPs	Cintra	Architecture 2008
Power and Branch Aware Word-Length Optimization	William Osborne, Jose Coutinho, Wayne Luk and Oskar Mencer	Field-Programmable Custom Computing Machines 2008
Credit Risk Modelling using Hardware Accelerated Monte-Carlo Simulation	David Barrie Thomas and Wayne Luk	Field-Programmable Custom Computing Machines 2008
Automated Hardware-Independent Scenario Identification	Juan Hamers and Lieven Eeckhout	Design Automation Conference 2008
MAPS: An Integrated Framework for MPSoC Application Parallelization	Jianjiang Ceng, Jeronimo Castrillon, Weihua Sheng, Hanno Scharwächter, Rainer Leupers, Gerd Ascheid, Heinrich Meyr, Tsuyoshi Isshiki and Hiroaki Kunieda	Design Automation Conference 2008
ADAM: Run-time Agent-based Distributed Application Mapping for On-chip Communication	Mohammad A. Al Faruque, Rudolf Krist and Jörg Henkel	Design Automation Conference 2008
Run-time Instruction Set Selection in a Transmutable Embedded Processor	Lars Bauer, Muhammad Shafique and Jörg Henkel	Design Automation Conference 2008
Multiprocessor Performance Estimation Using Hybrid Simulation	Lei Gao, Kingshuk Karuri, Stefan Kraemer, Rainer Leupers, Gerd Ascheid and Heinrich Meyr	Design Automation Conference 2008
Efficient unicast and multicast support for CMPs	Samuel Rodrigo, José Flich, José Duato, Mark Hummel	Symposium on Microarchitecture 2008
A Distributed Processor State Management/Architecture for Large-Window Processors	Isidro González, Marco Galluzzi, Alex Veidenbaum, Marco Antonio Ramírez, Adrián Cristal, Mateo Valero	Symposium on Microarchitecture 2008

Based on the rules set by the steering committee (a member can only receive a financial award once), the following 10 members were given a HiPEAC Financial Award:

- Francisco Cazorla
- José Duato
- Mateo Valero
- Albert Cohen
- Lieven Eeckhout
- Rainer Leupers
- Marcelo Cintra
- Wayne Luk
- Jörg Henkel
- Adrian Cristal