1. Publishable summary

1.1 Introduction

Organic electronics offer thin, light-weight, and flexible/bendy alternative to the silicon based microchips existing nowadays all around us. One of the main benefits for using organic materials in the production of electronic devices is the possibility to use large-area fabrication technologies such as printing. The potentiality of this technology is shown in the forecast made by IDTechEx which predicts that the market for printed and potentially printed electronics will rise to over $50 billion during this decade.

Despite the promising market forecasts, the use of organic thin film transistors and circuits in today's industrial products has been limited. The main obstacle for substantial market penetration of such organic electronic components has been the inability to achieve sufficient device performance using high-volume production methods. This has delayed the commercially viable implementation of organic transistors in complex electronic circuits and system development.

In response to this, the POLARIC (Printable, organic and large-area realisation of integrated circuits) project aimed to improve the performance of the organic electronic devices by developing the related fabrication methods. The 13 project partners were 3D-Micromac AG (Germany), AMO GmbH (Germany), Asulab Division of Swatch Group (Switzerland), BASF Schweiz AG (Switzerland), Cardiff University (CU), CSEM SA (Switzerland), Fraunhofer EMFT (Germany), IMEC (Belgium), Imperial College (UK), Joanneum Research (Austria), micro resist technology AG (Germany), Obducat Technologies AB (Sweden), and VTT Technical Research Centre of Finland as the coordinating organisation. POLARIC has received funding from the European Community's Seventh Framework Programme (FP7/2007-2013), under the area of Information and Communication Technologies (ICT). The project duration was from January 2010 until June 2014.

1.2 Objectives

The objective of the project was to realise high-performance organic electronic circuits on plastic substrate using large-area processing compatible fabrication methods. The transistor fabrication development was focused to enable a high resolution nanoimprinting lithography (NIL) step. Applying NIL enables small transistor channel lengths (below 1 μm) on plastic substrate and thereby an increase in operation frequency of the device. Another important concept to improve the performance has been the self-aligned fabrication principle, in which the critical patterns of the different layers are automatically aligned in respect to each other during the transistor fabrication. This decreases the parasitic capacitances and thereby increases the operating frequency, decreases the gate leakage currents, and is one of the key elements to enable the use of large-area fabrication concepts such as roll-to-roll (R2R) techniques. The target was to test the developed circuits first in basic electronic building blocks such as inverters and ring oscillators. Eventually, the technology development was to be exploited in the flexible active matrix liquid crystal display (AMLCD) and radio-frequency identification (RFID) demonstrators.

1.3 Overall strategy

There have been three main *fabrication platforms* used in the project. Towards the AMLCD demonstrators, *batch processing platform* has been used. Here, plastic substrate 10 cm by 10 cm in size has been used. The *batch processing platform* has utilised sheet-to-sheet type processing techniques such as photolithography in the patterning, in addition to the NIL based patterning. For

the RFID demonstrators, in which certain parts of an RFID tag are realised, *R2R processing platform* with web coating techniques is used. In the *R2R processing platform*, we have focused on the manufacturing techniques that offer the highest expectation for the throughput, the continuous-type roll-to-roll processing. Thus, it is not a stop-and-go type process, which would enable the use of lithography to define small features. The batch processing enables smaller footprint of the devices, whereas R2R processing opens up the possibilities for true large-area processing. In spite of this main division, the platform development has strong interlinks and it is often necessary to mix the batch processing and R2R processing platform. This is especially the case with the complementary OTFT technology development in the project, in which R2R compatible *gravure printing* is used as widely as possible to produce the device layers, but with a sheet-to-sheet batch process.

1.4 Work progress and achievements during the third reporting period

1.4.1 Combining NIL processing and self-aligned concept to TFT fabrication

The speed-limit of the thin-film electronics using a given set of materials is largely determined by channel length, source-drain to gate overlap, and contact resistance. TFT channels with lengths from 10 µm down to the sub-micrometre regime were patterned by UV based nanoimprint lithography. Thin polymer dielectrics with thickness down below 100 nm were employed in order to maintain low operation voltages of 10 V. The overlap lengths between source-drain and gate electrodes as low as 0.2 µm were achieved by self-aligned electrode definition using back-substrate exposure. Pentacene based organic thin film transistors with a low line edge roughness of channels, mobilities of the order of 0.1 cm^2/Vs, low contact resistance, and an on-off ratio of 10^4 were fabricated on 4”x4” flexible substrates. The stability and spatial distribution of channel length were assessed in detail with spreads of L ranging from 220 to 30 nm. A ring-oscillator with an average stage delay below 4 µs at an operation voltage of 7.5 V was demonstrated.

1.4.2 Modelling of self-aligned NIL based sub-micrometer pentacene-based organic thin-film transistors

The devices described above were used to select a model based on the “TFT Generic Charge Drift model” which works well for a broad range of channel lengths including the submicron TFTs. It was shown that these TFTs can be accurately modelled, thus giving access to complex circuit simulations and design. The results were published in *Organic Electronics* journal[1].

This dedicated static model was then updated to account for the subthreshold regime and was used to simulate a zero-V_{GS} inverter (one of the most basic unipolar logic gate). Based on the extracted noise margins, two methodologies were studied to assess the potential of the studied TFT technology in terms of p-logic digital circuits. The different analysis showed that these TFTs, in the current state of the technology, are still not ready for complex digital circuits as the throughput is expected to be quite low. The proposed methodology and related interpretation are technology-independent. Therefore, this analysis may serve as a basis to characterize unipolar-logic printed

[1] F. Zanella et al., “Design and modeling of self-aligned nano-imprinted sub-micrometer pentacene-based organic thin-film transistors”, Organic Electronics 14 (2013) 2756–2761.

electronics and can be further extended to complementary-logic circuits. These results were published in *IEEE Transactions on Electron Devices* journal[2].

1.4.3 Complementary OTFT technology

In order to decrease operating voltage and power consumption, and increase noise margins, n- and p-type OTFTs and organic complementary circuits were developed in the POLARIC project. The n- and p-type OTFT components consisted of short-channel UV-NIL or conventionally by photolithography patterned gates, thin organic photo-patterned or printed dielectric, self-aligned source and drain, and gravure printed semiconductors. Circuits were developed on plastic substrates using materials available within the POLARIC consortium. Complementary inverters and NAND gates were successfully fabricated and their DC and AC response were tested.

For complementary inverters based on short-channel UV-NIL gates, printed dielectric, self-aligned source and drain, and gravure printed semiconductors, optimal device behavior at low operational biases of V_{dd} = +9 V, giving a high inverter gain of G = 28, was achieved. The more robust process flow of short-channel conventionally patterned gates (L = 3 μm), photo-patterned dielectric, self-aligned source and drain, and gravure printed semiconductors was found to achieve the necessary yield and highly uniform behaviour for multiple working circuit elements. Inverter (NOT gates) had a 40 μs stage delay, and NAND logic gates could be operated at frequencies > 5 kHz at an operating bias of V_{dd} = +20V.

1.4.4 Nanogravure as method to pattern submicron scale gates for TFTs

Using special printing clichés developed in the project, doctorblade-less discontinuous dewetting as a method to fill ink cells was demonstrated for the nanogravure printing. Using this method, a range of liquid polymers and high boiling point solvents were printed onto the surface of a flexible substrate. This included micron and sub-micron lines, circles, dots, arrays of dots, and numbers. Finally, the nanogravure printed PMF etch resist process was used to pattern a sub-micron wide Au wire on the flexible PC substrates. This enables the use of the mehod e.g. in patterning of the gates for short channel transistors, when combined with the other process steps used in the project for TFT fabrication.

1.4.5 Demonstrators

AMLCD based flexible display demonstrator

The fabrication development and eventually the realisation of the AMLCD demonstrator were carried by 8 POLARIC project partners from 6 different countries. Thus, the establishment of working fabrication platform required a significant joint effort and solving a huge set of practical and technical challenges. As a result of this collaboration, 22 fully processed AMLCD backplanes ideally giving 88 individual flexible displays with different transistor channel geometries were produced. Of these, 10 backplanes were further processed into displays, contacted, and tested. Although the developed transistor technology is still in rather immature level, the results indicated that the technology generally is capable of fulfilling the specifications demanded by the AMLCD application.

[2] F. Zanella et al. “Submicrometer Organic Thin-Film Transistors: Technology Assessment Through Noise Margin Analysis of Inverters”, IEEE Transactions on Electron Devices, 61 (2014) 1508-1514.

R2R processed integrated circuits for RFID front end

The load modulator, antenna capacitor, and rectifying unit together constitute the front end of an RFID tag. The aim in this project was to utilise thin film transistors with very short (below 1 µm) channel lengths in this RFID front end circuitry. The target was to realise the fabrication process completely by using roll-to-roll (R2R) fabrication techniques. To achieve the short transistor channel lengths on R2R fabrication platform, hot-embossing based nanoimprint lithography (HE-NIL) was to be used in the process to pattern the critical features. The final important concept to be exploited was the self-aligned fabrication principle, in which the critical patterns of the different layers are automatically aligned in respect to each other during the transistor fabrication.

Along the R2R process development it was observed that the HE-NIL process was inapplicable for producing sub-micrometer scale TFT channels in large areas. In order to avoid a deadlock situation in the process development, and to simplify the fabrication process, the HE-NIL related process steps were replaced with flexographic printing and lift-off. This enabled the R2R fabrication of working transistors and Demo 4 circuits, with the cost of not achieving the targeted channel lengths.

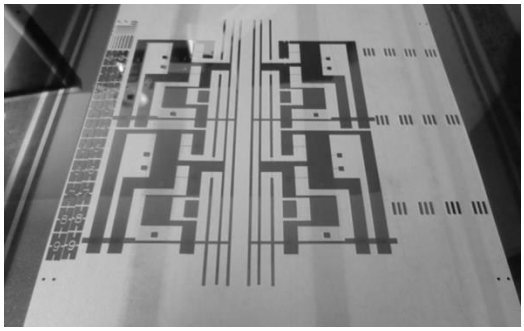

Figure 1. Roll-to-roll fabricated TFT circuits.

In the R2R demonstration run, a web (or roll) approximately 80 meters in length, containing more than thousand devices for the RFID front end was produced. One repetition section in the 300 mm wide roll is shown in Figure I. A TFT footprint was about 15 mm x 15 mm, and one RFID front end circuitry took an area of approximately 50 mm x 50 mm. The design margins were very conservatively selected, and the footprints can be decreased substantially. The minimum transistor channel length for the R2R fabricated TFTs in this work were 40 µm. Although being relatively short for a thin film transistor fabricated completely with continuous type roll-to-roll techniques, this transistor channel length is not in itself beyond the state-of-the-art. The on-currents in the TFTs remained relatively low, well below 1 µA. Also the on/off currents were measured to be modest, being in most cases below 10^3. However, the main success is in implementing the self-aligned fabrication concept to such TFT fabrication process on a R2R platform. This eliminates the problem of limited registration accuracy of the R2R equipment, and decreases the overlap capacitances. The achieved yield in this first demonstration was roughly 40% in average. With further fabrication development and process iterations, the yield could be improved substantially, while the parameter spread could be decreased.

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