Project Acronym : **AFSiD**

Atomic **F**unctionalities in **Si**licon **D**evices

Project no. 214989

Nano ICT project

Deliverable: D2.2: "Report on coupled SET and SET-FET function in particular two-atom(artificial) SET function, transport spectroscopy of two-atom SET"

Due date: Month 42
Delivery date: Month 42
Estimated manpower indicated in the grant agreement: 42 MM
Effective effort: 57MM

D2.2	Report on coupled SET and SET-FET function in particular two-atom(artificial) SET function, transport spectroscopy of two-atom SET	Dissemination Level: Public

Partners involved: CEA**, UTU,** MDM, HIT

Table of Contents

1. Abstract:

Excellent MOS-SETs have been realized in the project using optimized nitride spacers. Hundreds of devices have been characterized at low temperature. Charging energies up to 35ºmeV (eventually suitable for room temperature) have been identified for smallest functional devices from batch 2. Modelling was performed for detailed understanding of observed addition spectra. With multi-gate SETs compact and fully controllable coupled MOS-SETs have been realized and characterized in detail. A floating gate effect in due to discrete charging in poly-silicon gates is identified. Complex and hybrid device configurations have been designed and characterized, leading to an RF-SET configuration working at 750 MHz – with an application as a detector for charging effects in poly-silicon gates, an electron pump working at 100Mhz, a tunable SET-to-FET dvice using substrate polarization, a SET-FET configuration with clear hysteresis effects, a MOS-SET tunnel coupled to a single donor and finally a latch-switch realized with a tunnel coupled dot.

2. Realization and detailed understanding of excellent MOS-SETs using optimized nitride spacers.

In the previous report, data on a large number of artificial atom SETs were presented. An example of data from a well characterized device with gate length L=20nm, silicon wire width W=40nm, silicon wire thickness T_{Si}=8nm is displayed in fig. 2.1. On the left, the linear response at 4.2K is shown, exhibiting clear Coulomb oscillations with large separations in gate voltage between peaks, ranging from 75mV to 114mV with an average period of oscillation of approximately 90mV. The charge stability diagram measured at 4.2K is shown on the right. Clear Coulomb diamonds are visible.

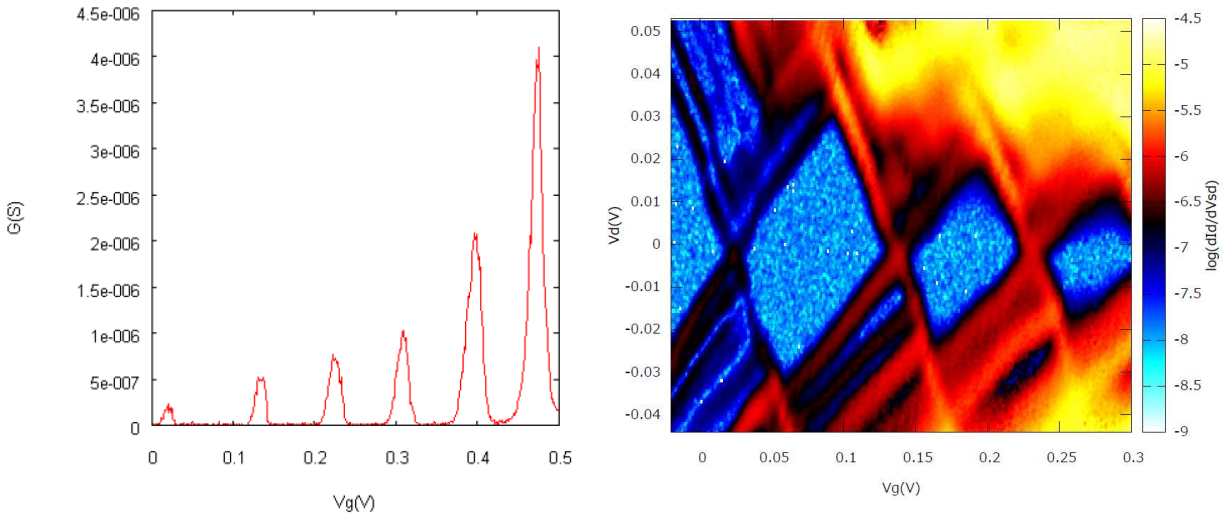


Figure 2.1: Id-Vg characteristics at 4.2K of single gate SET with L=20nm, W=40nm (left) and charge stability diagram (right, in Siemens).

In order to calculate the charging energy, capacitances were extracted from the first Coulomb diamond: C_s=1.6aF, C_d=1.7aF, C_g=1.4aF. This results in a charging energy of 35meV, which is among the highest reported in such devices [E. Leobandung, L Guo, Y. Wang, S.Y. Chou, Appl. Phys. Lett. 67, 938 (1995)] In addition to Coulomb diamonds, excited states are also clearly visible. The separation between the ground state and the first excited state is 11.8meV and 11.5meV between first excited state and second excited state.

Based on the experience with a large number of SETs as reported in the previous report, more detailed investigations of the relation between geometrical parameters such as channel width, gate length, silicon thickness and spacer width are reported:

Geometry dependence of Coulomb charging in SOI-SETs

The charging energy of an SET and therefore its suitability for high-temperature operation is determined by the effective size of the Coulomb Island. Considering the SET as a metallic dot one can derive the gate capacitance directly from the roughly equidistant spacing of the Coulomb Blockade Oscillations $\Delta V_g = e/C_g$. From a fit of the shape of a single thermally broadened conductance peak to $g(V_g) = g_{\max} \Big/ \cosh^2\left(\frac{\alpha e(V_g - V_{peak})}{2k_B T}\right)$, (cf. Figure 2.2) the gate sensitivity α can be determined, which relates the gate capacitance C_g to the total capacitance C_Σ according to $\alpha = C_g / C_\Sigma$.

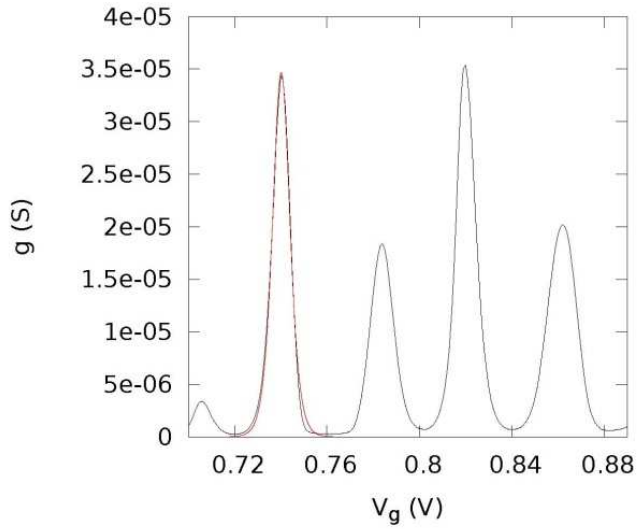


Figure 2.2: Coulomb Blockade Oscillations with single peak fit (red)

Single gate SETs consist of a silicon nanowire of width W with an overlapping polysilicon gate of length L. With a plate capacitor as a geometrical model the gate capacitance is calculated to $C_g=\varepsilon_0\varepsilon_r A/d$. Two different areas A and A* are considered as shown in Figure 2.3, where A* resembles the Fin-FET geometry with the silicon thickness T_{Si}.

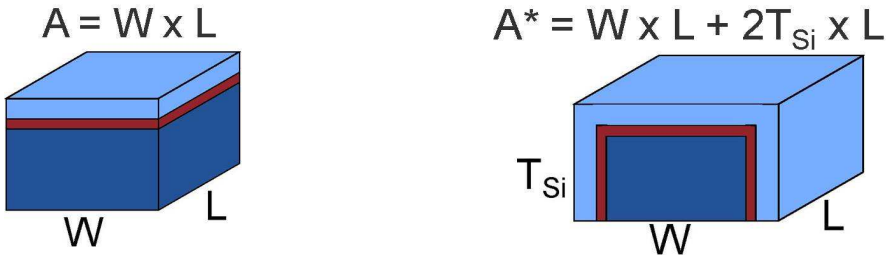


Figure 2.3: Gate and dot as a parallel plate capacitor (left), and modeled as a FIN-FET structure (right).

At UTU a large number of devices were investigated, taken from batch 1, batch 2 and from the pre-batch2 wafer. In total samples from 6 different wafers with various properties have been measured. All the SETs consist of an undoped nanowire with silicon thicknesses ranging from 8 nm to 20 nm. The range of both wire width and gate length was 20 nm to 100 nm. For each device several conductance peaks have been fitted and the average ΔV_g and α have been taken.

Gate capacitance vs. areas A and A* is presented in Fig. 2.4 left and center. The different colors represent different wafers with different properties such as silicon thickness and spacer size. The solid red line is the theoretical value for the gate capacitance. Obviously there is a high variability in these nanoscale devices; however there is a reasonable agreement between the experiments and the geometrical model. The large number of points below the solid red line in Figure 2.4 (center) indicates that the electronic size of the dot is often smaller than the physical size. On the right, the gate sensitivity α is shown as a function of gate capacitance, exhibiting a reasonable variability due to fluctuations of the total capacitance around $C_\Sigma=7.7\ 10^{-17}$ F, indicated by the dashed green line.

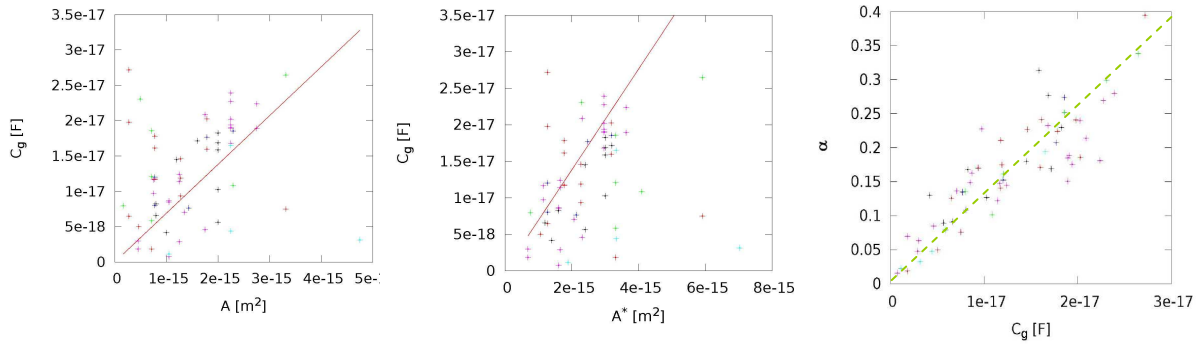


Figure 2.4: Gate capacitance C_g vs. area A (left), C_g vs. area A* (center) and α vs. gate capacitance C_g for a large number of SETs from different fabrication runs.

Simulation of artificial atom-states:

In order to account for the discrepancies between two nominally identical Single Electron Transistors (SETs) a three dimensional self-consistent simulator based on Current Spin Density Functional Theory (CSDFT) in the framework of the NanoTCAD ViDES package [Lisieri et al. , Journal of Computational Electronics, 6, 2007] was used at MDM.
It solves the many body Schrödinger equation using CSDFT in the local density approximation and in the effective mass approximation with parabolic bands, and yields the ground state of the system.
The SET is modeled as a silicon nanowire with length L and with a rectangular section of T_{Si} x W area without source and drain contact regions on the top of a silicon dioxide slab. The device has a tri-gate structure with L gate length and the gate is insulated from the nanowire with a T_{ox} thick silicon dioxide layer (see Fig.2.5).

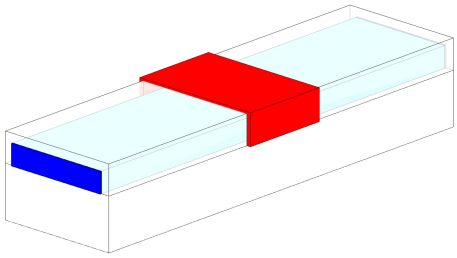


Fig. 2.5: Schematic device model

We explored the geometrical limits of an L=20 nm x W=20 nm nominal device within the lithographic process tolerance: L varies from 22 to 25 nm and W from 10 to 15 nm (T_{Si} is kept constant to 10 nm).
In Figs. 2.6 to 2.9 we show the simulated addition energies and the total spin of the system as a function of the number of electrons in the SET for the 4 different devices at a temperature of 4.2K when no magnetic field is applied. In the insets the spin of the electrons and the lowest subband level

for each valley in the plane normal to the transport direction are shown. The valleys along the transport direction are not shown for clarity and the shape of the section is also reported.

As can be seen, when the wire width W is changed from 10 to 15 nm (see Figs.2.6 and 2.7) the resulting addition energy patterns and spin filling sequences change: in particular note $E_{add}(1\rightarrow2)>E_{add}(2\rightarrow3)$ in Fig.2.6 whereas $E_{add}(1\rightarrow2)<E_{add}(2\rightarrow3)$ in Fig.2.7. Moreover, it is worth noting that in Fig. 2.6 the first four electrons are all spin-up filling the four valleys normal to the transport direction. Conversely, in Fig. 2.7 both spin-up and down electrons are occupying only the valleys along the T_{Si} direction.

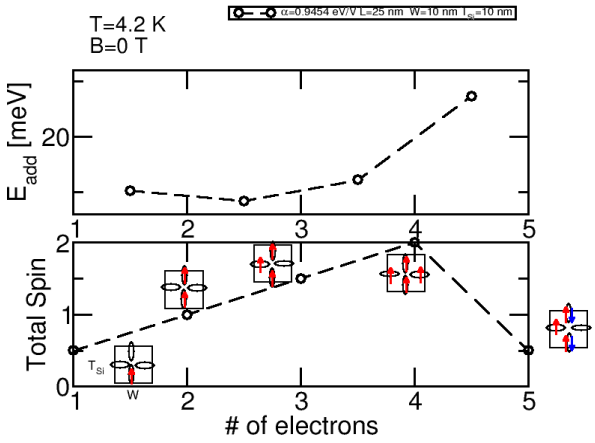


Figure 2.6: Addition energy and total spin for a device with L=22nm, W=10nm, α=0.9384

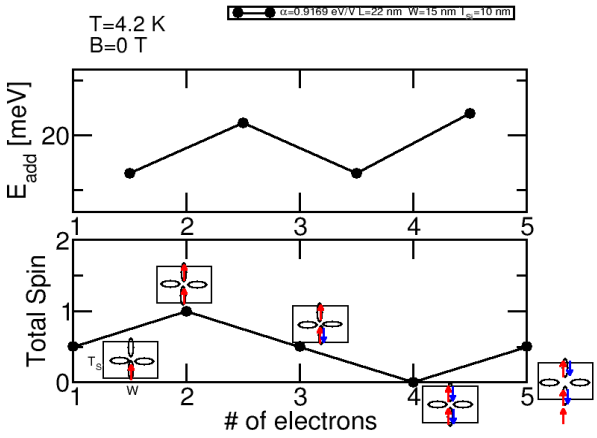


Figure 2.7: Addition energy and total spin for a device with L=22nm, W=15nm, α=0.9169

When L is increased (see Figs. 2.8 and 2.9 with respect to Figs. 2.6 and 2.7) the gate capacitance increases and as a result the charging energy is reduced. This leads to a qualitatively rigid downwards shift of the addition energy patterns in Fig. 2.8 and 2.9 whereas no change in the spin filling sequence is noted between Figs. 2.6 and 2.8 and between Figs. 2.7 and 2.9, respectively.

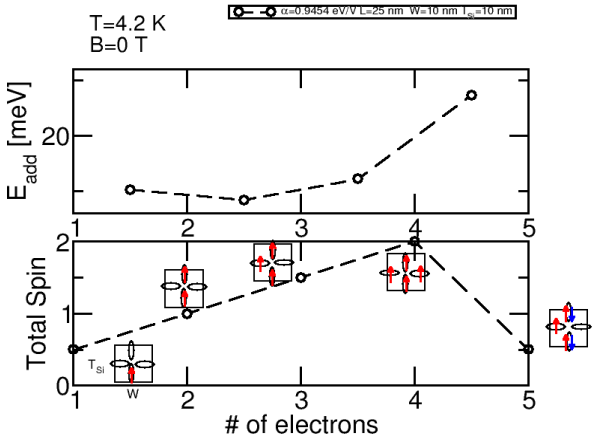


Figure 2.8: Addition energy and total spin for a device with L=25nm, W=10nm, α=0.9454

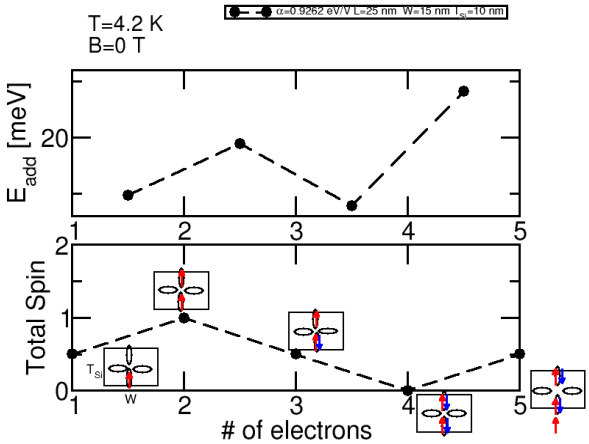


Figure 2.9: Addition energy and total spin for a device with L=25nm, W=15nm, α=0.9262.

In addition the electron charge density in the centre plane of the device, normal to the transport direction, has been simulated for two of the SETs considered here:
A) L=25 nm, W=10 nm (Fig. 2.8)
B) L=25 nm, W=15 nm (Fig. 2.9).

In Fig. 2.10 the simulated electron charge density in the plane (x=0 nm) normal to the transport direction is reported for N=1 to 4 electrons in SET A (left) and B (right). As can be seen, the cross-section of the wire strongly influences the shape of the charge density and the position of the centre of charge.

All these simulation results demonstrate the relevance of a fine control of the geometrical dimensions of the device to exploit the SETs as building blocks e.g. for a quantum computer.

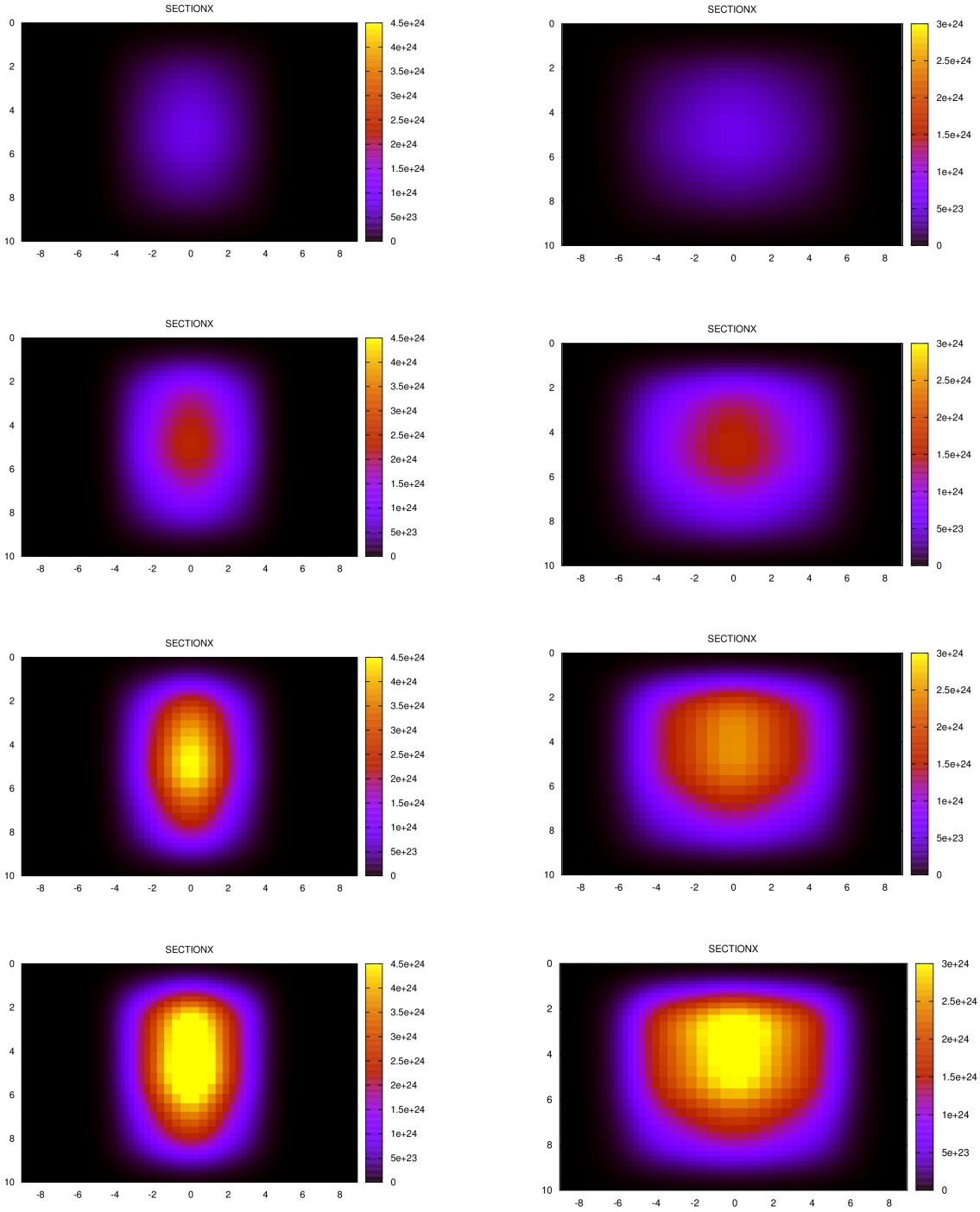


Figure 2.10: Cross section of charge density in centre plane normal to the transport direction for, from top to bottom, N= 1, 2, 3, 4 electrons in the artificial atom for device A (left) and B (right).

3. Validation of several complementary strategies for the realization of compact and fully controllable coupled MOS-SETs

Within AFSiD we have developed various strategies for building compact and controllable MOS-SETs. The first one - which has been largely described in the previous reports, is to use an undoped channel with a non-overlapping geometry. The so-called MOS-SET is an accumulation quantum dot located below the front gate in the silicon nanowire, separated from the source and drain by the undoped segment of the silicon nanowire. At M24 we have shown that this AFSiD device can be tuned from a MOS-SET with a charging energy in the 1 meV range to a MOS-SET with a charging energy as large as 13 meV. This has been realized by decreasing the size from 50*50 nm^2 typically to 20*20 nm^2.

During the last period we have concentrated first on coupled MOS-SETs, either in series or in parallel configurations, both in undoped or doped devices. Particular attention was paid to the control of the tunnel barriers (means, couplings) between the MOS-SETs.
Some results have been published in "Intrinsic and doped coupled quantum dots created by local modulation of implantation in a silicon nanowire" M. Pierre, B. Roche, R. Wacquez, X. Jehl, M. Sanquer, and M. Vinet JAP109, 084346 (2011).

The results obtained in this period confirm and extend the results already presented at M24.
A typical example is shown in figure 3.1 which corresponds to two arsenic doped silicon SETs in series with fully tuneable couplings - both inter-coupling and source-drain couplings. With this realization we have shown that doped and undoped silicon SETs, both very compact and eventually with fully tuneable couplings can be combined and integrated on a CMOS platform.

The substrate bias can also be used as another parameter for controlling the couplings. Moreover a combination of front and back gate voltage generate an electric field with a vertical gradient in the SOI that permits the control of the vertical position of the MOS-SETs. This is very specific to our dots made from thin SOI.

Another layout is to place the MOS-SETs in parallel. We consider in figure 3.2 the face-to-face sample already shown in WP1 but above the threshold (positive front gate voltage, moderately positive or zero substrate bias).

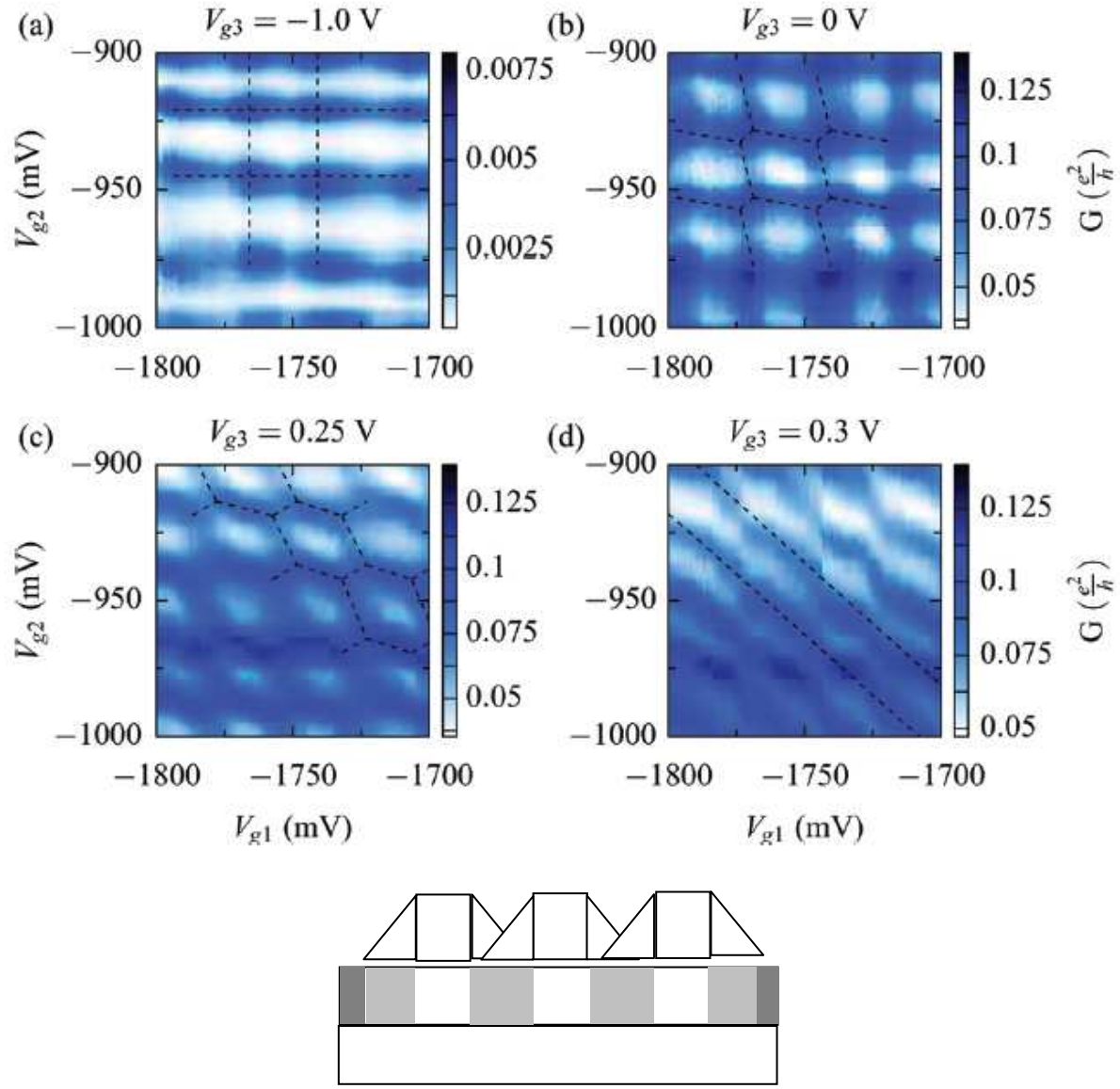


Figure 3.1: Colour plot of the drain-source conductance at 4.2K in a sample with three gates and with LDD implantation (light gray in schematic layout is LDD, dark grey is HDD and white is undoped). The panels correspond to different voltages Vg3 applied to the central gate. Vg1 and Vg2 are both strongly negative so that two dots are formed between gates 1 and 3 and gates 2 and 3. Dashed lines are guides for the eyes. (a) Capacitance coupling between the two dots is negligible. The points at which both dots are non-blockaded are on a square lattice. The lines joining these points are due to cotunneling. (b) Inter-dot capacitive coupling is increased. The points on the square lattice are extended along the diagonal. (c) A clear honeycomb pattern is observed, characteristic of a strongly capacitively coupled double dot system. (d) The diagonal pattern of lines indicates the formation of a single large dot (from JAP109, 084346 (2011)).

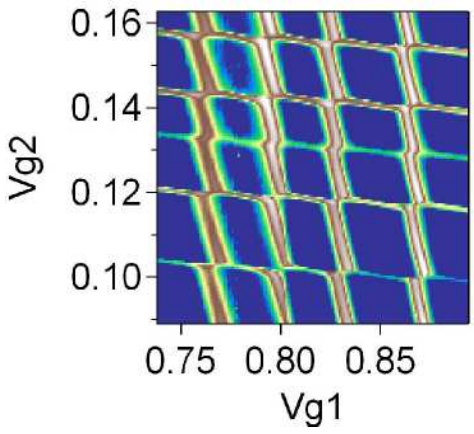


Figure 3.2. Colour plot diagram of the source –drain current recorded at T=0.1K in the sample presented on WP1 figure 1(?) in the accumulation regime (Vg1, Vg2 >0). A honeycomb diagram characteristics of the two MOS-SETs in parallel (located below gate 1 and gate 2) is obtained.

Detailed characterization of multi-artificial atom SET

A typical device for the characterization of multi-artificial atom SETs is depicted schematically in fig. 3.3. As one example Device 2 on scribe WRESP1 from Batch2, Wafer 1 with dimensions L=30nm, W=40nm, S_{gg}=60nm, silicon thickness = 8nm and double spacers (10nm and 15nm, see fig. 3.3) was investigated at 4.2K. Below each gate a quantum dot is formed.

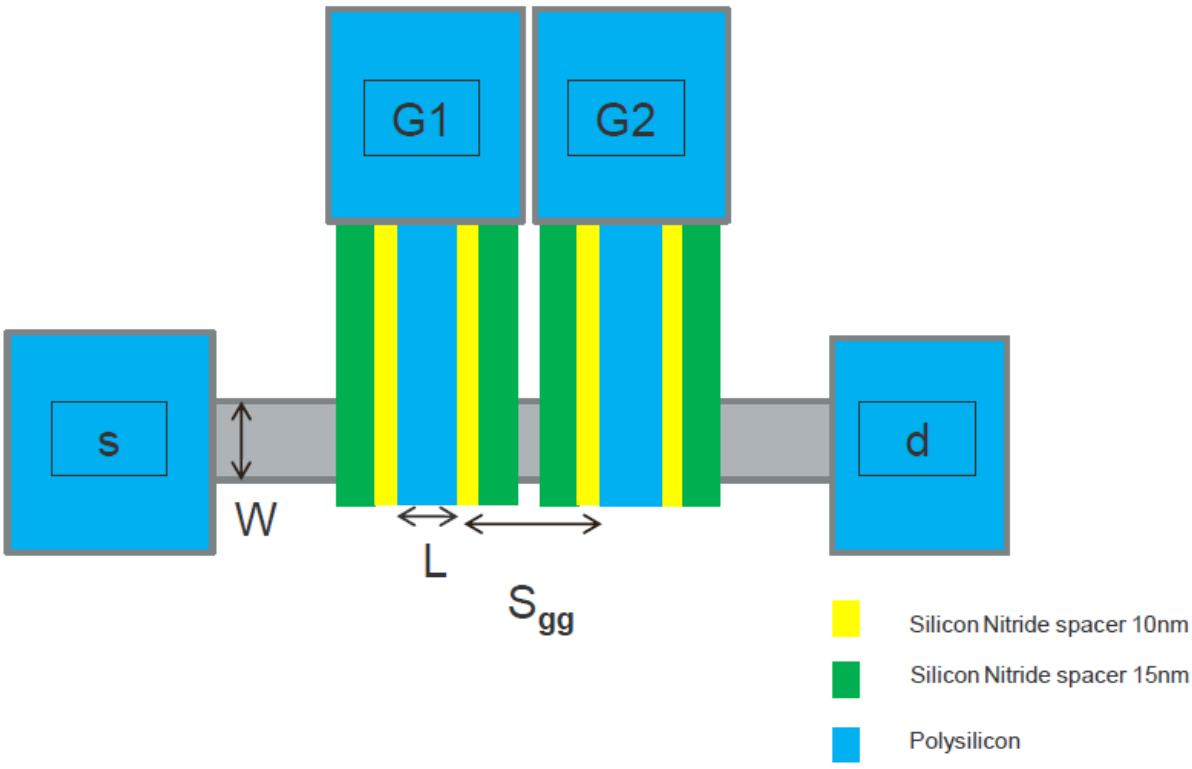


Figure 3.3. Schematic design of the double gate device investigated at 4.2K.

Each dot shows clear Coulomb blockade oscillations with periods ΔV_{g1}= 13.3mV and ΔV=14.3mV.

Charge stability measurements were performed while the interdot capacitance was tuned. As shown in fig. 3.4 the transition from weak interdot capacitance, where each gate tunes only the number of electrons in the dot formed below it, to intermediate interdot capacitance is clearly observed in the evolution of the charging diagram from a rectangular conductance pattern to a honeycomb pattern and finally to a diagonal pattern reflecting the formation of a single large dot. Fitting of the observed charging diagrams allows the capacitances in each region of operation to be determined.

A very different behaviour is observed in the device 2 on scribe WBPTP1 from Batch2, Wafer 3 with dimensions L=50nm, W=60nm, S_{gg}=50nm, silicon thickness = 12nm and spacers = 15nm. Due to the smaller spacers the region between gate1 and gate2 is not covered during S/D implant, leading to the formation of a metallic region in series with the usual dots.
The low temperature characteristics of the dots formed below the gates show a distinctive modulation suggestive of a series configuration resulting from the simultaneous tuning of both the metallic island between the gates as well as the dots.

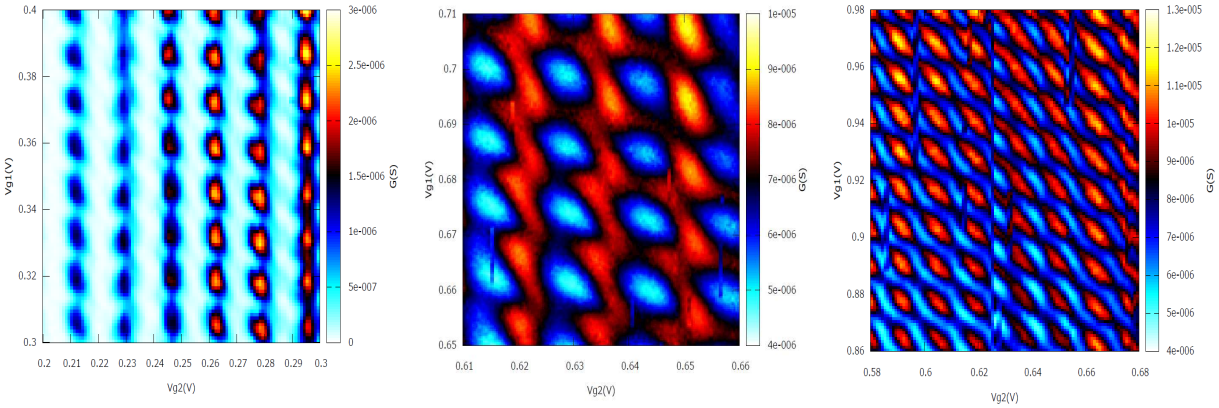


Figure 3.4: Charge stability measurement in different regions of V_{g1}-V_{g2} space showing transition from (left) weak interdot coupling, (center) intermediate interdot coupling, (right) strong interdot coupling.

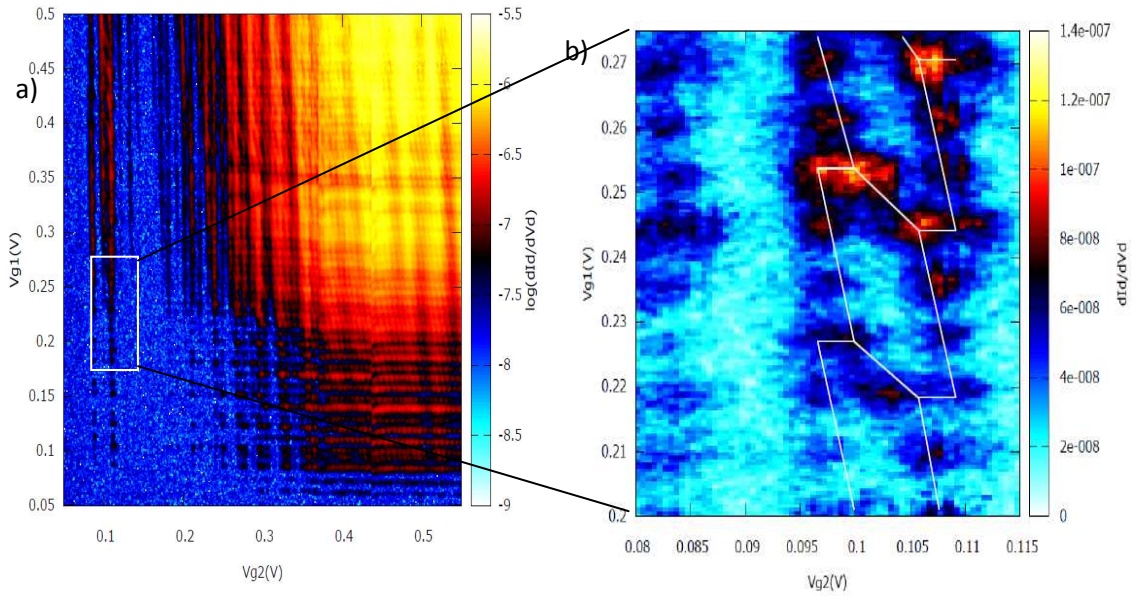


Figure3.5: Charge stability measurement at 4.2 K. a) Large range of V_{g1}-V_{g2}, b) small region of (a) which shows honeycomb pattern.

The charging diagram of this double gate device is shown in fig.3.5, where for low gate voltages the rectangular pattern of the conductance data, formed due to weak interdot coupling, evolves gradually into a honeycomb pattern for larger gate voltages. In addition there is a wealth of fine detail which is due to the fine interplay of charging energy scales in this multiple dot device. To understand this complex configuration simulations were performed for the region of fig. 3.5b) and a comparison between the experimental data and the simulated data is shown in fig. 3.6.

In order to simulate the observed conductance data it is necessary to assume that the central dot is strongly coupled to dot2 and that the electron number of the central dot is tuned via the potential on gate1. Physically this suggests that the dopants in the central region between gate1 and gate2 have diffused more towards gate2. Furthermore we believe that the reason for the stronger capacitative coupling between the central dot and gate1 is related to a smaller effective gate length for gate2.

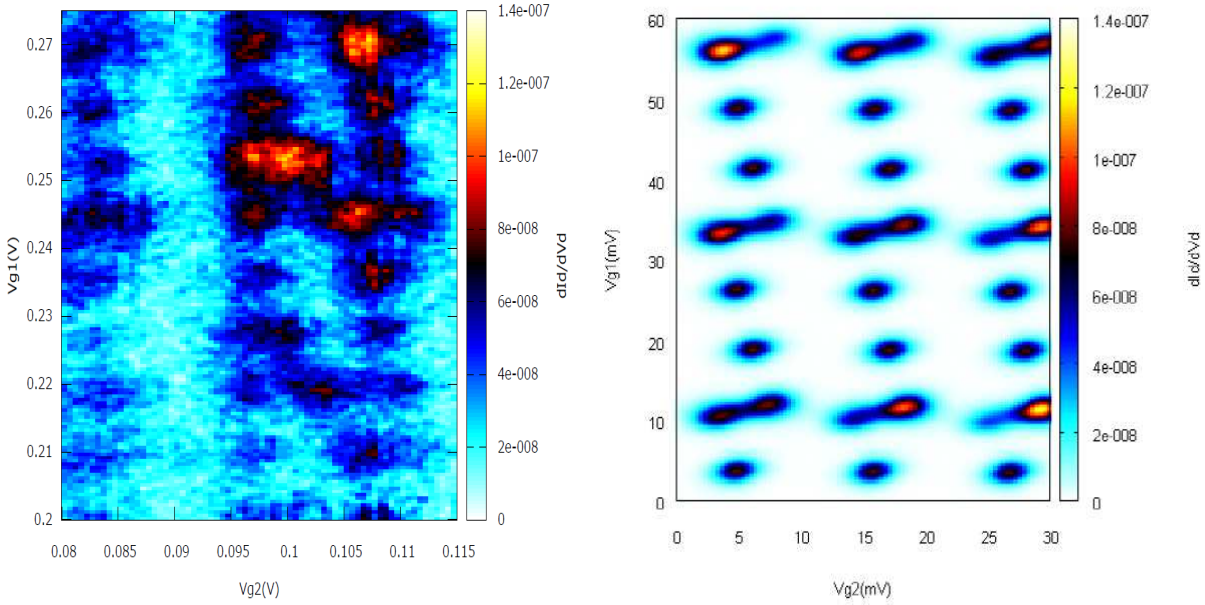


Figure3.6: Measured data at 4.2K (left) and simulated data at 4.2K (right).

This can be seen from the room temperature data, where the subthreshold slope of the gate2 is less than that of gate1as shown in fig. 3.7.

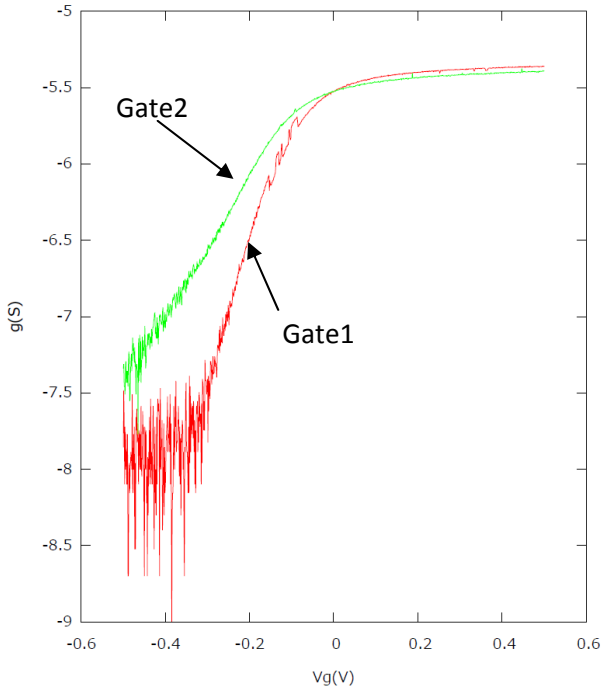


Figure3.7: Room temperature I_d-V_g measurement of gate1 and gate2 at V_{ac}=50µV and V_{dc}=0V.

A further triple dot configuration has been realized in a device with three top gates on scribe NTLSH3 of Wafer 1 (Batch 1) with dimensions L=40nm, W=40nm, Tsi=20nm, spacer=40nm. A schematic design of the device is shown in figure below.

Low temperature conductance measurements were performed for each dot separately by ensuring that the other series dots were sufficiently well conducting.

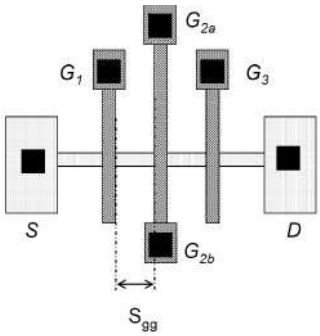


Figure 3.8: Schematic design of the triple top gate device.

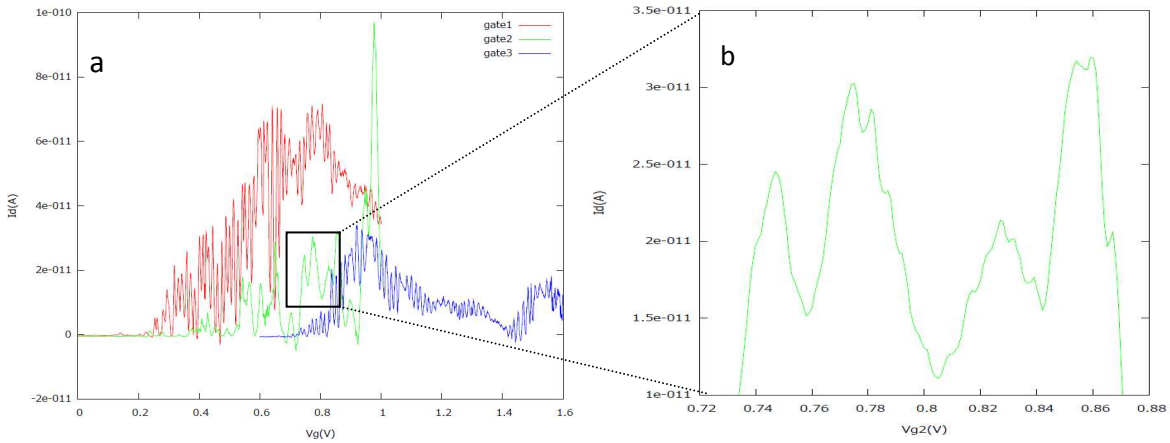


Figure 3.9: Linear response at 4.2K. a) Each dot characterized as SET holding the other two gates at 0.8V. b) Magnified region of small region marked in a.

The observed periods of oscillation for gate1 and gate3 are similar (approx. 15mV) while the period of oscillation for gate2 is 64mV. Fig.3.9b shows the magnified region of gate2 oscillations between Vg2=0.72-0.88V. We can see two periods of oscillation; the fast oscillation may be attributed to gate2 tuning dot2 while the slow oscillation may be attributed to gate2 tuning dot1 and dot3. Interactions between the dots were studied as before by keeping the remaining dot in a conducting state. Fig.3.10 shows the charge stability measurements for each combination of gates considered.

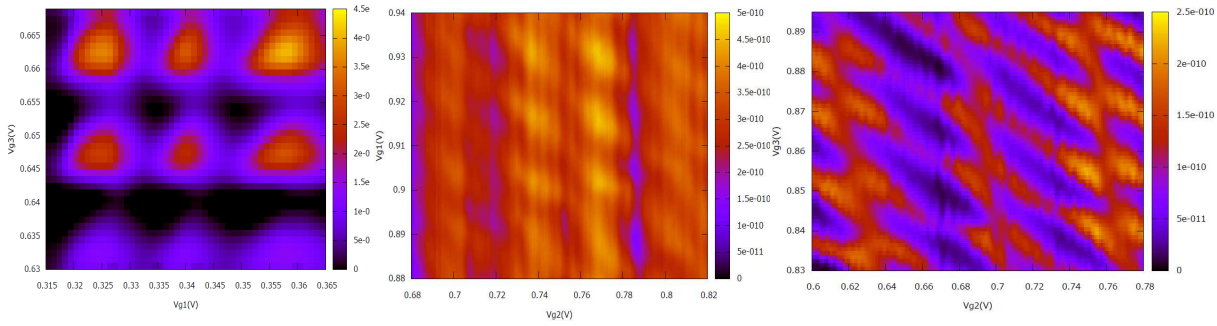


Figure 3.10: Charge stability measurement at 4.2K for different combination of gates while holding the third gate at 1V (left) Vg1-Vg3, (center) Vg2-Vg1, (right) Vg2-Vg3.

In fig. 3.10 left the weak coupling between dot1 and dot 3 is clearly shown as expected for two dots separated by a distance of 140nm. From fig. 3.10 center and right we see that whenever gate2 is swept in addition to a honeycomb pattern a fast oscillation is observed along the gate2 direction. These data may be explained by considering a three dot system with a strongly asymmetric tuning of the dots via the central gate electrode. Based on this model we have undertaken simulations which yield good qualitative agreement with the measured charge stability data (cf. fig. 3.10 right and fig. 3.11).

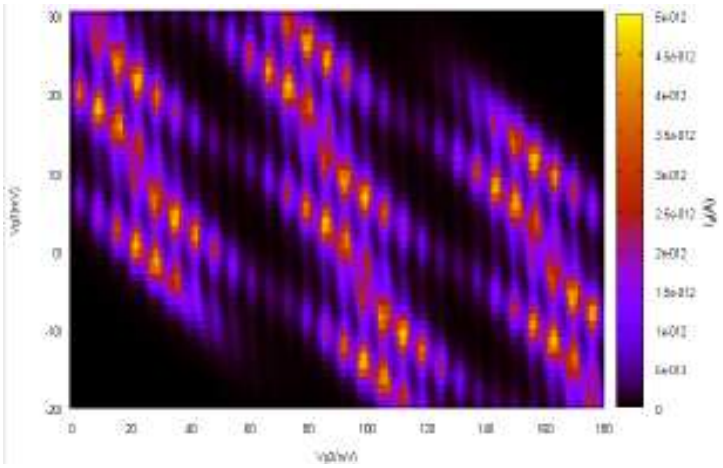


Figure 3.11: Simulated Charge stability to fit the experimental data in fig. 3.10 right.

4. Realization of a Silicon RF-SET (radio frequency SET) working at 750 MHz with application as a detector of charging effects in ultimate poly-silicon gates.

The MOS-SET is a very sensitive detector, but its bandwidth is limited by its intrinsic large output resistance. Combined with large capacitances due to typical wiring in cryostats, the time constant is limited to a few ms. In order to fully exploit its sensitivity, the RF-SET concept has been proposed and proved for various SETs. The principle of the RF-SET and its realization at Grenoble is shown on figure 4.1.

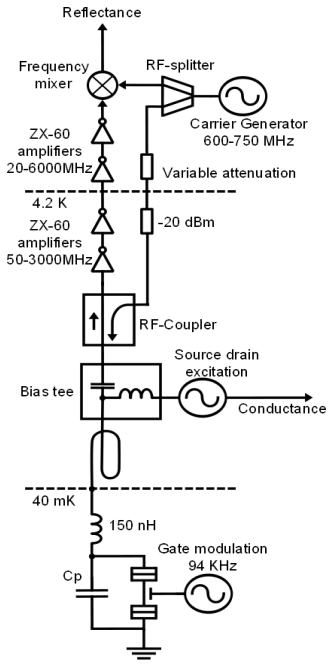


Figure 4.1. Electrical layout for the RF-SET: The MOS-SET at the bottom is included in a LC tank circuit. The modulation of the reflection coefficient versus gate voltage @750Mhz is recorded. The advantage is a large bandwidth detection (as compared to the DC SET).

The RF-SET has been successfully used to detect a fine charge granularity in the polysilicon gate which appears below T=1K. Of course the principle is relevant to a wide range of applications, in particular to increase the bandwidth for detecting spin after a spin-charge conversion.

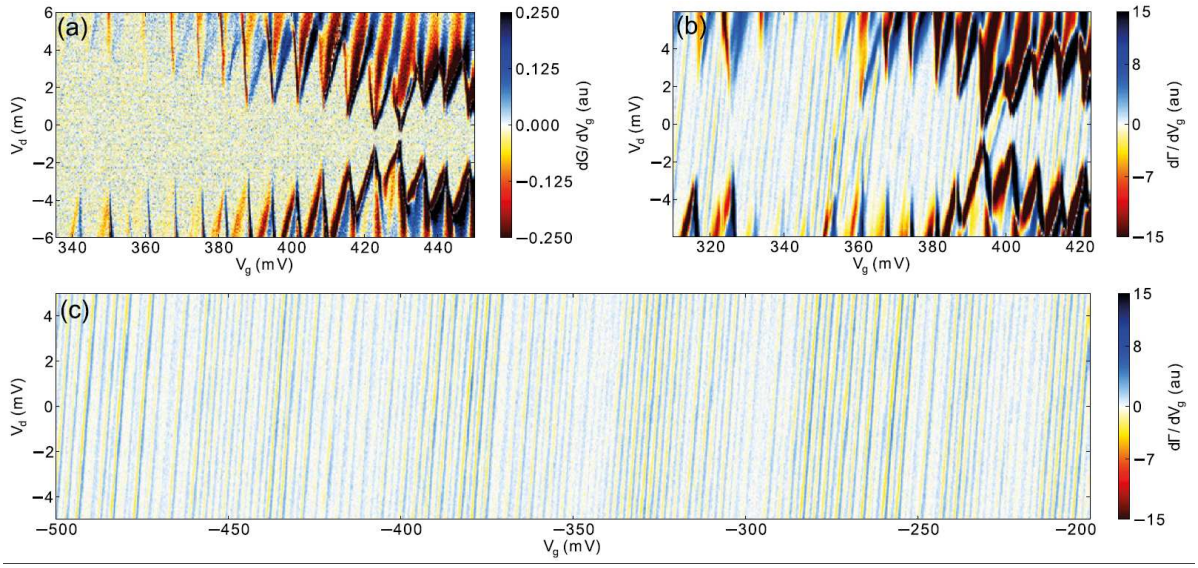


Figure 4.2. Coulomb stability diagram at T=40mK is recorded for a MOS-SET: in a): standard DC measurement. In b) and c) reflectometry measurements. Additional lines are detected in the Coulomb blockade diamonds (b) and also at gate voltages where the MOS-SET is completely empty of carriers (c). The lines are due to a charging effect in the polysilicon gate which appears below T=1K. It is well accounted for in the model presented on figure 4.3 (submitted to APL).

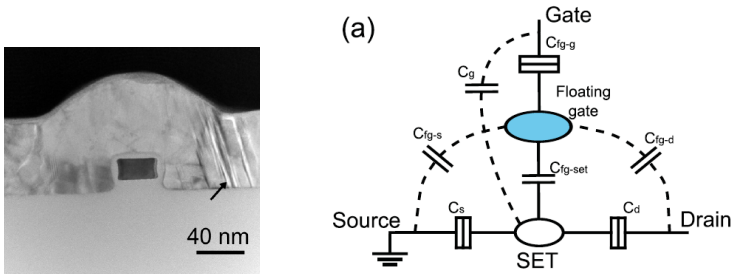


Figure 4.3: SEM cross section of the MOS-SET showing imperfection in the polysilicon gate responsible for charge granularity below T=1K and detected by the RF-SET reflectometry. The model presented on the right panel, where the floating gate is the part of the gate overlapping the nanowire, accounts for the observation of figure 4.2. This effect disappears by using metallic gate (TiN) which is less resistive (submitted to APL).

5. The identification of floating gate effects due to discrete charging in poly-silicon gates

In Tübingen, several single gate devices were investigated at low temperature (70mK) where modified Coulomb diamonds due to the charging of additional features were observed (as shown in fig. 5.1 below). Some of the modifications are marked by arrows in the figure.

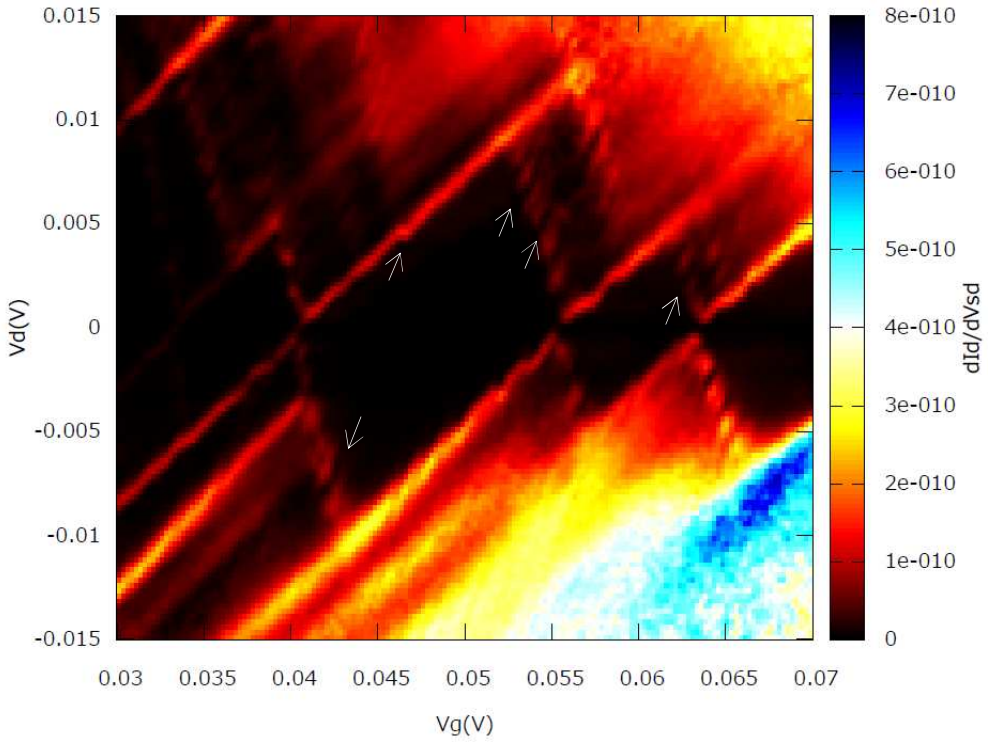


Figure 5.1. Charge stability measurement of single gate device with dimensions L = 50nm, W =60nm T_{si} = 8nm at T = 70mk.

Transconductance measurements of these devices show the clear evolution of these features. In addition to the usual Coulomb diamond structure, a large number of conductance lines are visible (shown in fig. 5.2). In most of the measurements the slopes of these lines are close to 2. From the measured data, we can see that with increasing gate voltage there are features being charged which modify the Coulomb diamonds. From fig. 5.2 we may conclude that the feature is not present in the

wire because with increasing source-drain bias we would see increasing conductance through it. Secondly, the feature is capacitively coupled to source and drain and we may show that these lines have slope = 2 due to a symmetric coupling to source and drain leads.

To understand the measured data we propose a model which assumes a poly-silicon grain (dot 2) capacitively coupled to source and drain electrodes and tunnel coupled to the gate electrode. This configuration resembles a Single Electron Box (SEB), which in our case is capacitively couples to the single electron transistor (SET).
The period of the conductance lines with slope = 2 suggests that the poly-silicon grain is large compared to the dot formed in the silicon wire (dot 1). Hence, the effect of charging dot 1 on dot 2 is small. Therefore, to simplify the problem we solve the electrostatics for the SEB independently.

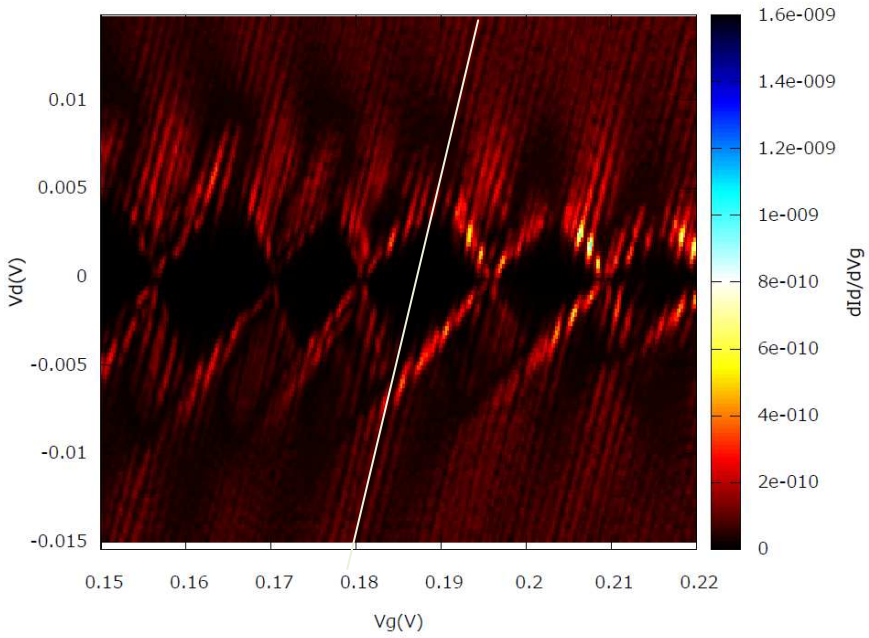


Figure 5.2: Transconductance measurement of single gate device with dimensions L = 30nm, W= 60nm, T_{si} = 8nm and T = 70mk. White line with slope 2 aligns with the conductance lines due to charging of the traps.

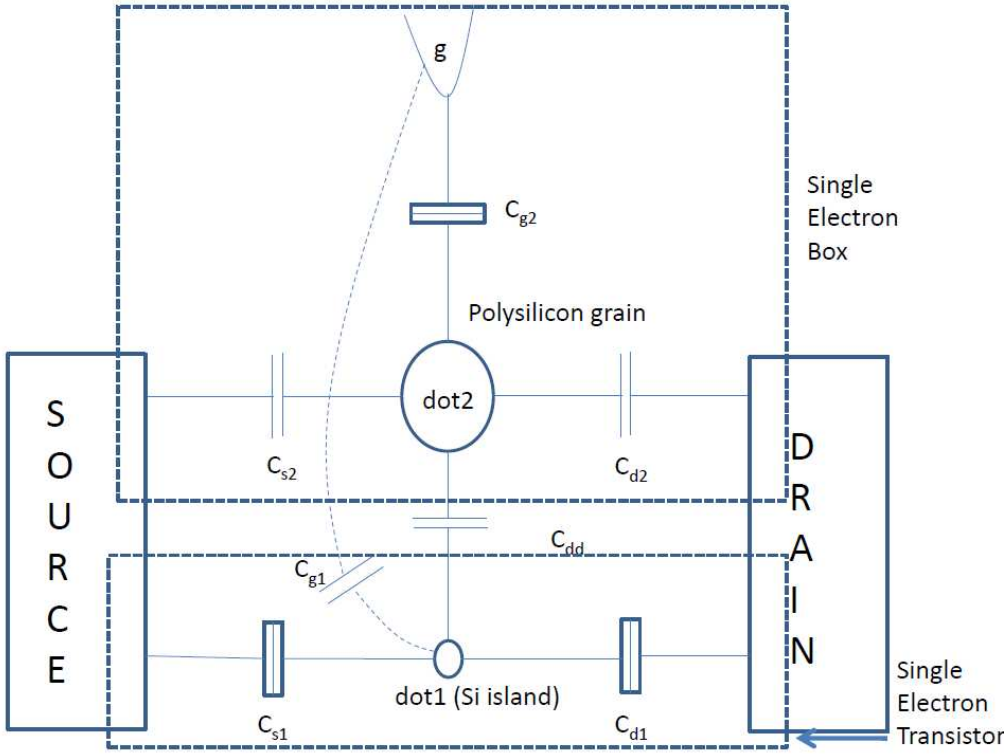


Figure 5.3. Model assumed for the simulation of a poly-silicon grain (SEB) capacitively coupled to source, drain and SET and tunnel coupled to gate.

The electrochemical potential of the poly-silicon grain (dot2) is given by:

$$\mu_{N2} = \frac{(eN)^2}{C_{\Sigma 2}} - \frac{e}{C_{\Sigma 2}}(C_{s2}V_s + C_{d2}V_d + C_{g2}V_g)$$

where $C_{\Sigma 2} = C_{d2} + C_{s2} + C_{g2}$

The electron number on the poly-silicon grain can fluctuate only if the electrochemical potential of the gate (μ_g) ≥ electrochemical potential of the dot2.

$$\mu_g \geq \mu_{N2}$$

Therefore, the condition to change the electron number on dot 2 is:

$$\mu_{g0} - eV_g = \frac{(eN)^2}{C_{\Sigma 2}} - \frac{e}{C_{\Sigma 2}}(C_{s2}V_s + C_{d2}V_d + C_{g2}V_g)$$

where μ_{g0} = electrochemical potential of the dot2 when no gate voltage is applied.

Rearranging the equation and differentiating with respect to V_d gives us the slope of the boundary line where the charge on dot2 can fluctuate.

$$\frac{dV_d}{dV_g} = \frac{C_{d2} + C_{s2}}{C_{d2}} \quad \ldots\ldots\ldots (1)$$

From the above equation it can be seen that for symmetric capacitive coupling of the dot2 to source and drain a slope = 2 should be observed as seen in our measured data. Fig. 5.4 shows a simulation for symmetric capacitance of dot2 to source and drain which gives negative differential conductance (NDC) lines with slope = 2. Capacitance values for SET are C_{s1} = 11.4aF, C_{d1} = 9.2aF, C_{g1}= 7aF and C_{dd} = 9aF.

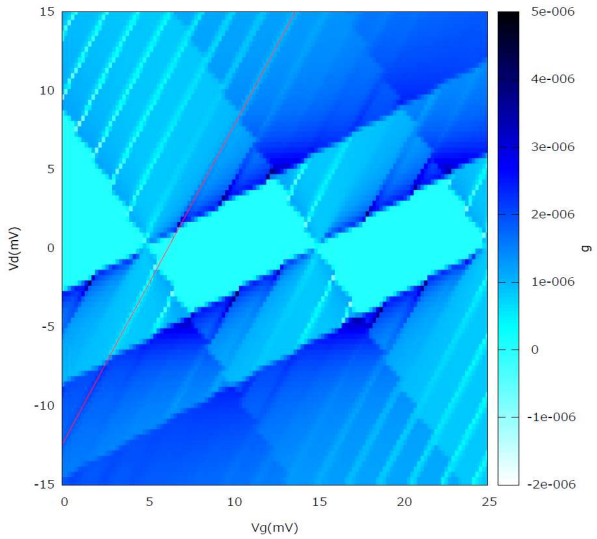


Figure 5.4: Simulation based on model shown in fig. 5.3. Capacitance values of SEB are C_{s2}= C_{d2}= 40aF, C_{g2}= 100aF and T=70mK.

For asymmetric source and drain coupling to dot2 the simulated slopes change from 2 to slope = 2.5 (C_{s2}=60aF and C_{d2}=40aF) and slope = 1.7 (C_{d2}=60aF and C_{s2}=40aF). These results are shown in fig. 5.5.

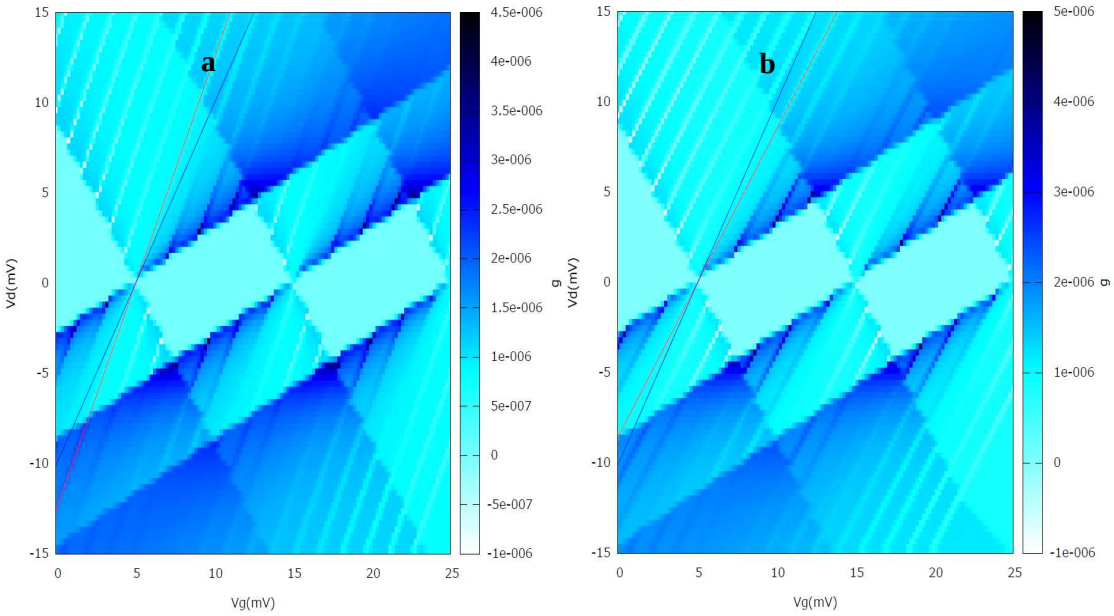


Figure 5.5. Simulation with asymmetric capacitance of SEB to source and drain, and a gate capacitance of 100aF. a) C_{s2} = 60aF C_{d2} = 40aF b) C_{s2} = 40aF, C_{d2} = 60aF. The red line has the slope depending on the value of C_{s2} and C_{d2} and the blue line with slope 2 is shown for reference.

As suggested from eq.1 above the slopes of these lines do not depend on the gate capacitance to the dot2. Fig. 5.6 shows simulations with 3 different values of gate capacitance to dot2 with source and drain symmetrically (C_{s2}=C_{d2}=40aF) capacitively coupled to dot2.

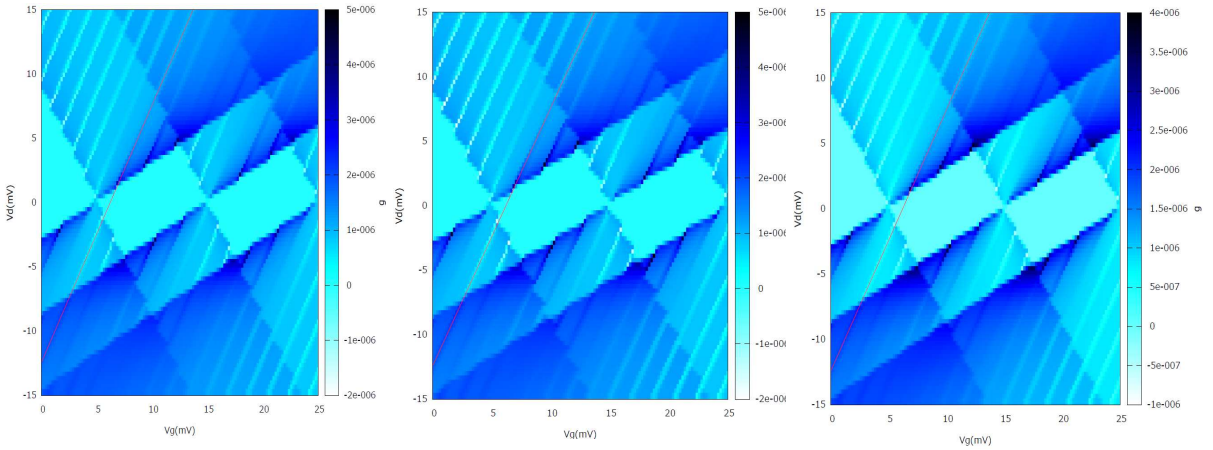


Figure 5.6. Simulation with symmetric capacitance of SEB to source and drain. a) Cg2 = 100aF. b) Cg2 = 50aF. c) Cg2 = 150aF. Red line has slope = 2.

Both the simulations and the measurements show negative and positive differential conductance (PDC) lines along the positive and negative slopes of the Coulomb diamond. A positive slope of the Coulomb diamond corresponds to the electrochemical potential of the dot1 aligning with the electrochemical potential of the source. In this situation when the dot2 is charged with an electron, due to the capacitive coupling the electrochemical potential of the dot1 moves within the transport window which results in an increased current (as shown in fig. 5.7 right). This gives lines of positive differential conductance along the positive slopes of the Coulomb diamonds. Similarly, for negative slope, the electrochemical potential of the dot1 aligns with the electrochemical potential of the drain. Again when the charge state of dot2 is changed this moves the electrochemical potential of the dot1 outside of the transport window, which results in a negative differential conductance. In the inset of fig. 5.7 right, the solid line corresponds to the state before charging of the dot2 and dotted line corresponds to the state after the charging of the dot 2.

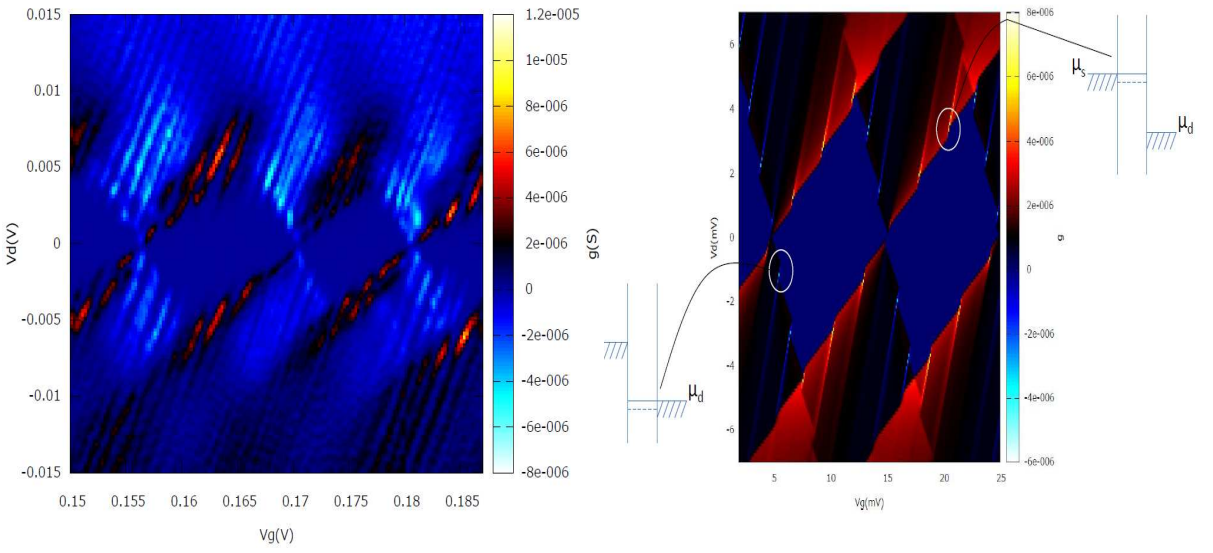


Figure 5.7. Charge stability diagram at 70mK. (left) Measured data showing NDC and PDC along the positive and negative edge of the Coulomb diamond. (right) Simulation with schematic explanation for the origin of these NDC and PDC lines along the edges of the Coulomb diamonds.

A careful examination of the measured data shows that these lines are not exactly periodic (as shown in more detail in fig. 5.8 left). This feature can be explained by assuming multiple grains within the poly-silicon gate which capacitively couple to the dot1 and also to source and drain. Fig. 5.8 right shows the simulated data with two dots in the poly-silicon gate.

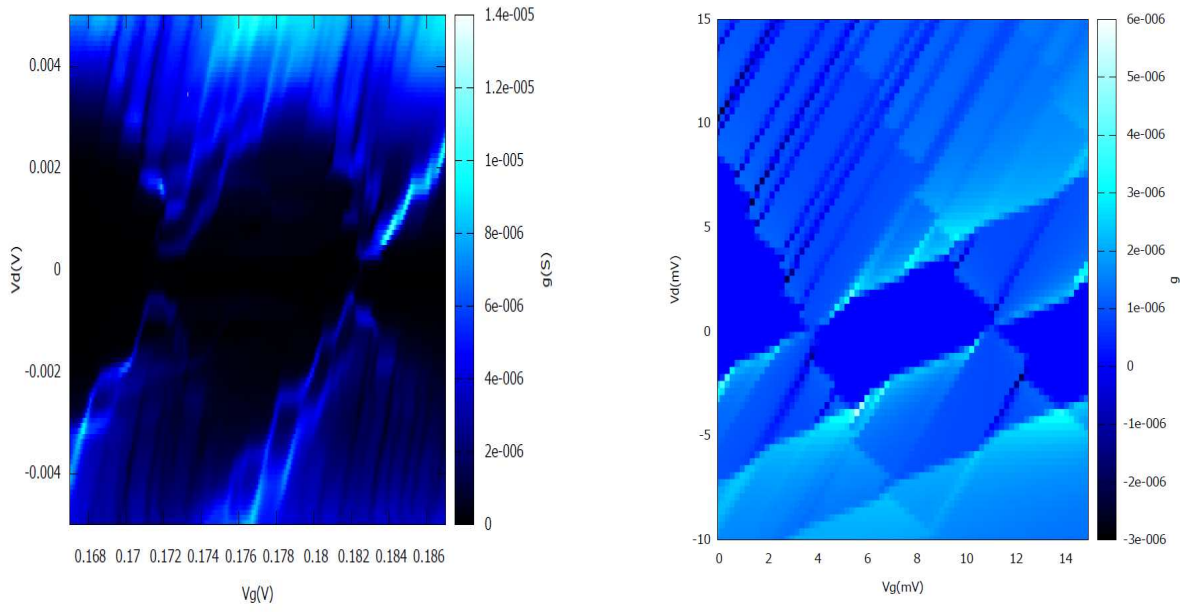


Figure 5.8. (left) Measured data at 70mK. Conductance lines with slope ~ 2 and with an irregular period are clearly visible. (right) Simulation with multiple grains in the poly-silicon gate.

Fig. 5.9 shows the model assumed for the simulation of fig. 5.8. Although in the simulation a parallel configuration of the multiple dots in the poly-silicon gate has been assumed, the generic features of the simulations remain unchanged for alternative (e.g. series) geometries. The important feature of the simulation is the existence of multiple dots in the poly-silicon which result in the observed aperiodic behavior and is highly reminiscent of the features observed in the so-called stochastic Coulomb blockade.

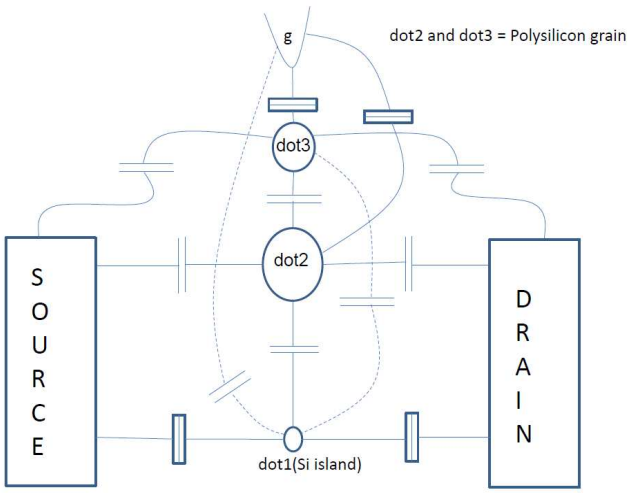


Figure 5.9. Model used for the simulation to provide an explanation for the irregularity in the periodicity of lines with slope ~ 2.

6. Realization of a silicon electron pump working at 100MHz

A prototype of devices using MOS-SETs is the electron pump, which is a device which permit to transfer electrons at a given rate from the source to drain even if no drain-source (or even negative drain source) voltage is applied. The realization of such a device is very important to prove AFSiD has reached the state-of-art and also is potentially interesting to be included in CMOS circuits. Envisioned application is metrology where the need for a reliable silicon pump is strong. Also shuttling of electrons by small packets (eventually one-by-one) can be useful for test analysis in CMOS circuits or advanced qubits (flying qubits, adiabatic transfer of charge etc…). The results presented in this section have been presented as an invited contribution to the main metrology conference CPEM2010.

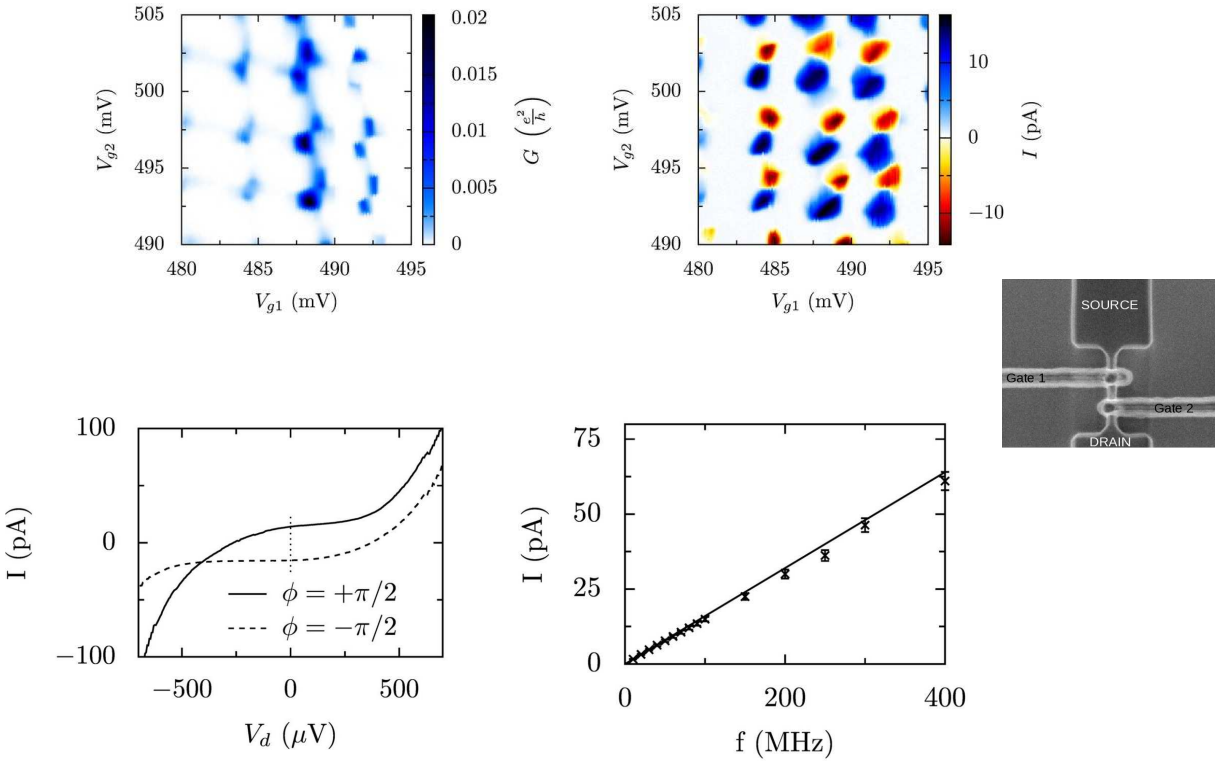


Figure 6.1: a full silicon electron pump: the rightmost panel is a SEM micrograph of the sample used: A modulation signal at frequency between few MHz up to 400MHz is applied to Vg1 and Vg2, with a controlled dephasing. Electrons are successively attracted from the source into the first MOS-SET then transferred in the second one, then to the drain- or vice versa depending on the dephasing. The top left panel shows the honeycomb diagram typical of coupled SET in series. The middle top panel shows the pumped current for a given dephasing. Depending on triple points a current is pumped from the source to drain ("electron" triple point) or from drain to source ("hole" triple point). No Vds is applied. The bottom left panel shows the current plateaus versus drain voltage for 2 dephasing. The bottom center panel shows the drain source current for a given triple point and dephasing as function of the modulation frequency: the observed current obeys to I=ef up to f=400MHz.

7. Realization of tunable SET-to-FET device using the substrate polarization of a silicon nanowire FET

The versatility of our MOS-SETs is very well illustrated by the possibility to turn a MOS-SET into a standard MOS-FET by using the substrate bias. This effect was not anticipated at the beginning of the AFSiD project and is one of the main results of the last period. This opportunity fully exploits the SOI technological choice and the convergence between the MOS-FET and the MOS-SET concepts especially for low power devices.

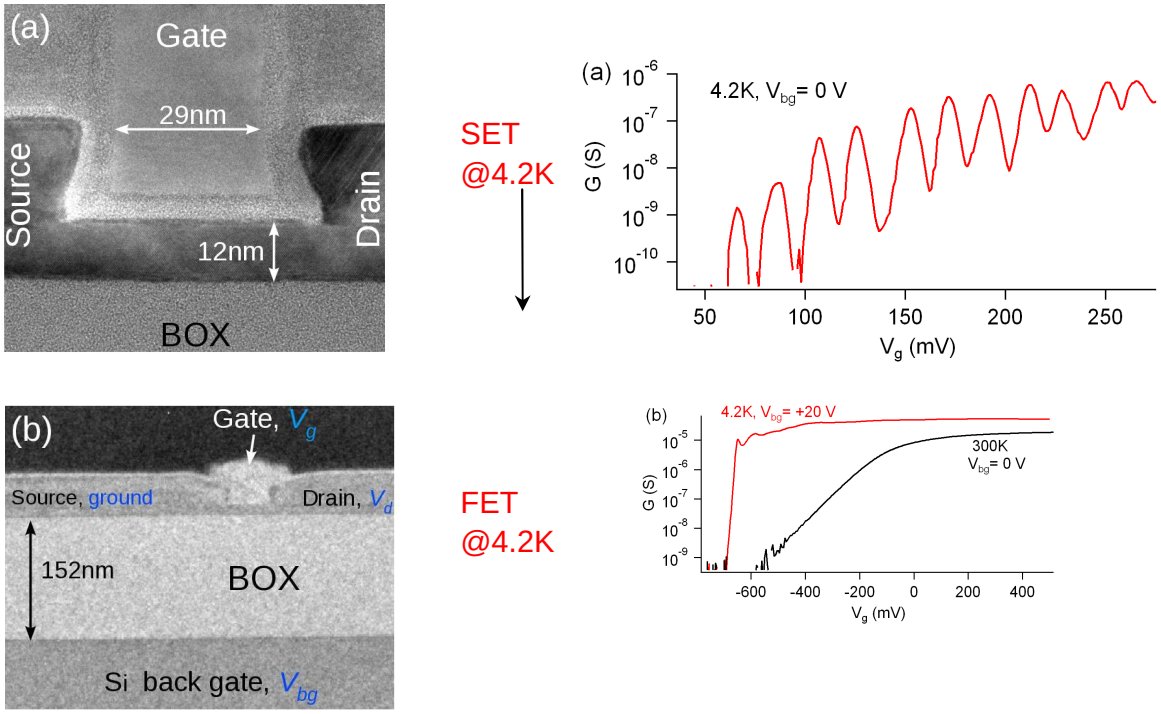


Figure 7.1: A single gate MOS-SET from batch 2 is turned into an excellent MOS-FET by applying a strong positive substrate bias of +20V. Let panels show SEM picture of the studied sample with a gate length of 30 nm and Tsi=12 nm (undoped). As for the other samples of AFSiD a substrate bias can be applied through a 150 nm thick buried oxide. Because the silicon substrate is undoped a special procedure has been fixed during the last period of the project to vary the backgate voltage under shining the sample with a LED at low temperature. The top right panel shows the MOS-SET oscillation recorded at T=4.2K. This is one of the multiple examples for the controlled realization of MOS-SET with AFSID. No substrate bias is applied. The bottom right panel shows the same sample with Vb=+20V (red curve) at T=4.2K. The effect of the backgate voltage is to reduce strongly- the tunnel resistance of the SOI below the nitride spacers by attracting electrons (mostly at the buried interface). As a result the access resistances decrease below the quantum of resistance and the SET effect vanishes. For comparison the 300k characteristic with no backgate applied is shown in black: as identified several times within AFSiD the crossover between the SET and the FET regime happens when the (almost temperature independent) source-drain conductance well above the threshold is comparable to 4 10^{-5} Siemens , means the quantum of conductance. The obtained FET at large substrate bias exhibit a record subthreshold slope of 8 mV/dec (over 3-4 decades) which is nevertheless larger than expected fro pure thermal activation in the conduction band at T=4.2K, for perfect gate control.

8. Analysis of a MOS-SET tunnel coupled to a single donor

In the first 2 years of AFSiD we have extensively studied the capacitive coupling of a MOS-SET with a donor located in the silicon nanowire. This capacitive coupling has profound implication for our MOS-SET, modifying the stability diagram for instance but also more generally for the analysis of the stability diagram of any quantum dot (Hofheinz 2006, Pierre 2009).

During the last period of AFSiD we have extended the analysis to the case of a donor which is tunnel coupled to the MOS-SET, in other words through the electronic levels of which a source-drain current can transit. The results are published in “Single-dopant resonance in a single-electron transistor” V. N. Golovach, X. Jehl, M. Houzet, M. Pierre, B. Roche, M. Sanquer, and L. I. Glazman, PRB 83, 075401 (2011)

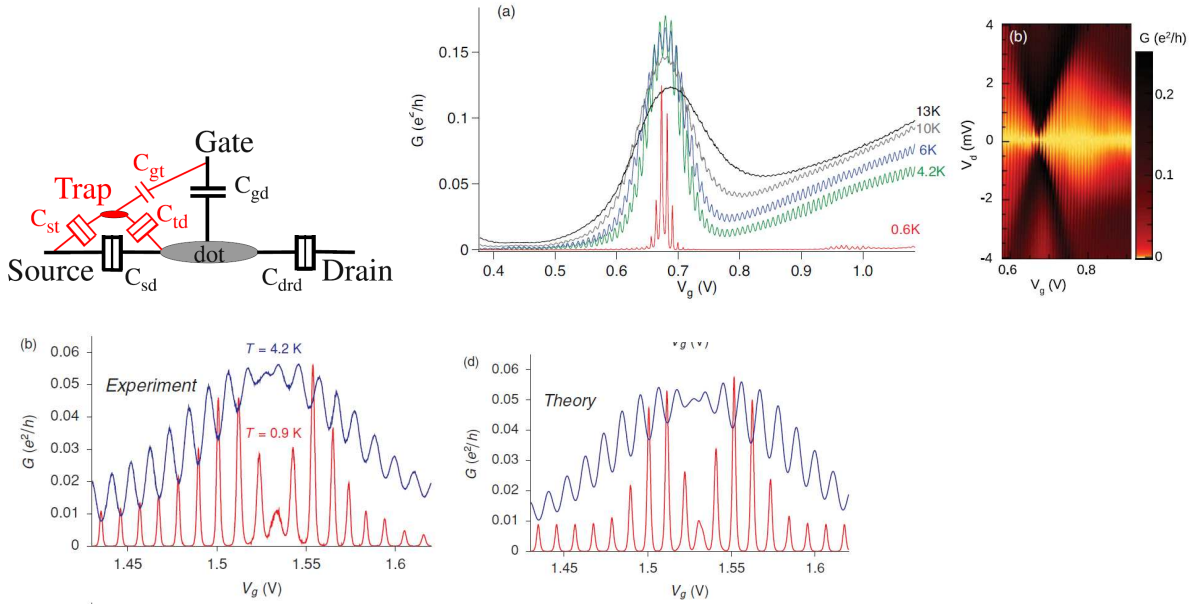


Figure 8.1: A tunnel coupled trap-SET model and the comparison with the experiment. The left top panel shows the model which differs from previous model where the trap cannot carry any current. The top right panel shows the Coulomb stability diagram recorded at low temperature. The Coulomb oscillations are barely visible at this scale. A big structure appears indicating the resonance of the trap-probably an arsenic donor in the nanowire between the source and the channel. The big resonance near Vds=0V is modulated by the SET oscillations. A full quantum model is able to feature the experiment in details as shown at the bottom panel, in particular the loss of contrast when the trap is at resonance. This very specific signature can be used for detection of single donor.

9. Hysteresis effects in coupled SET-FET

The investigated SET-FET devices consist of an FET with SETs built into the gate wire, as indicated in fig. 9.1. The device dimensions are W=L=60 nm for the SETs and W=500 nm, L=60 nm for the FET. There is an additional connection C_S on the FET-gate which enables independent characterization of the double gate SET and of the FET. In our SET-FET measurements G_1 is set to a high potential (~1V), so that this device is always on while G_2 is forming the SET under investigation. Thus the relevant parameters are V_S and V_{G2}. Mainly the behaviour of I_{FET} as a function of V_S is studied for different V_{G2} by comparing up- and down sweeps.
In a first series of experiments gates G_1 and G_2 are referenced to gate S as shown in fig. 9.1 (left), which results in a fixed potential between the dot under gate G_2 and the gate wire S for a given V_{G2}. Therefore changing V_S moves S and G_2 in parallel (cf. fig. 9.2). Fig. 9.3 shows the I_d-V_S characteristic of the FET when a high positive voltage is applied to the gates such that the SETs are completely open.

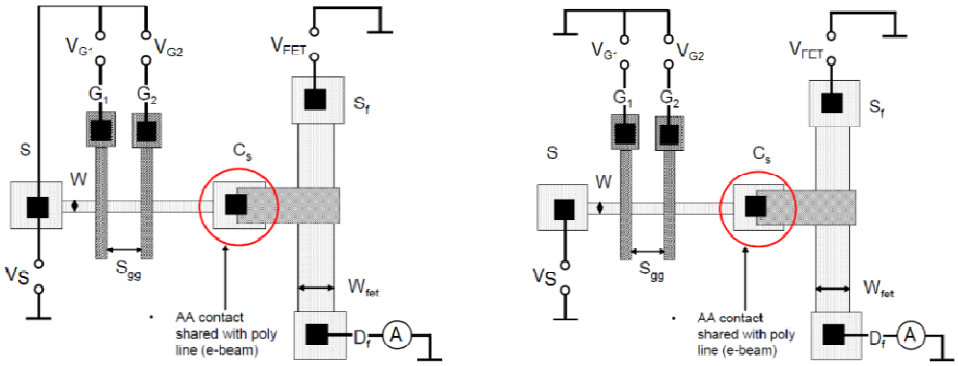


Figure 9.1: Sketch of the hybrid SET/FET device with different gate connections. Gate G_1 and gate G_2 referenced to gate S (left), both gates (1+2) referenced to ground (right).

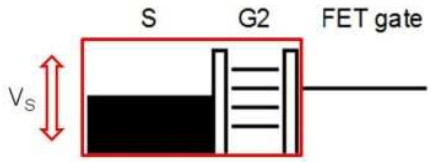


Figure 9.2: Referencing gate G_1 & G_2 to gate S (cf. fig. 3.2.38, left) leads to fixed potential between S and G_2. G_1 is kept at high positive voltage and considered "open" and therefore not drawn.

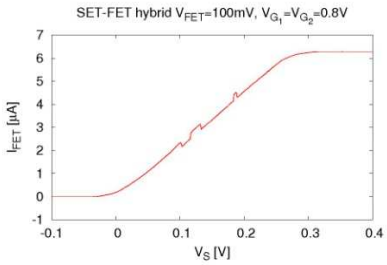


Figure 9.3: I_{FET}-V_S characteristic with open SET gates (V_{G1} = V_{G2} = 0.8 V, V_{FET} = 0.1 V)

Decreasing gate voltage V_{G2} means raising G2 with respect to S. Therefore, if we keep V_{G1} at a high positive voltage and decrease V_{G2} the I-V characteristic of the FET remains basically unchanged (cf. fig. 9.4) until the lowest level of G2 is raised above S. This situation is shown in fig. 9.5. First at point a the FET gate is still at a positive potential from the previous sweep and increasing V_S does not change it (except for slight capacitive coupling) as there are no accessible levels in the dot. When the lowest level of the dot is aligned with the FET gate (point b), the FET gate will follow S. A subsequent decrease of V_S raises the lowest dot level above the FET gate and hence the FET gate potential should remain stuck at the respective value. However in fig. 9.5 an FET- current drop for a decreasing V_S is observed. This can be explained by a gradual charging of the FET gate due to leakage currents. In fig. 9.6 two up-sweeps of the I-V-characteristics of the FET are shown for different values of V_{G2}. From the shift of point b to the right the change of the lowest level of dot2 due to the change of V_{G2} can be derived to $\Delta V_S = -0.54 \Delta V_{G2}$.

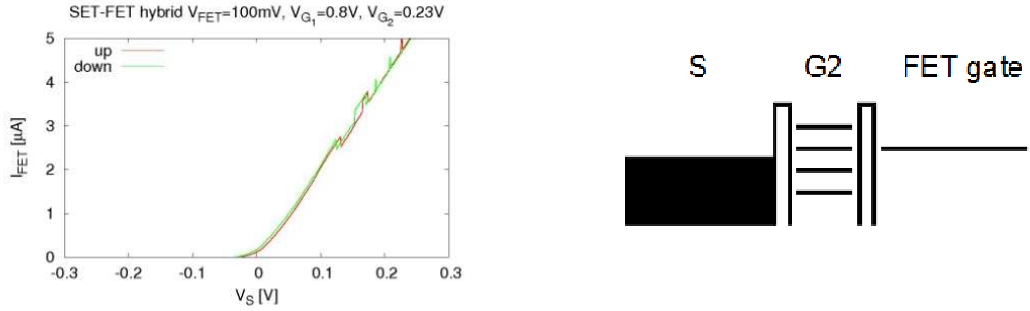


Figure 9.4: I_{FET}-V_S characteristic (V_{G1} = 0.8 V, V_{G2} = 0.23 V, V_{FET} = 0.1 V). The FET gate is aligned with a level of the dot under G_2.

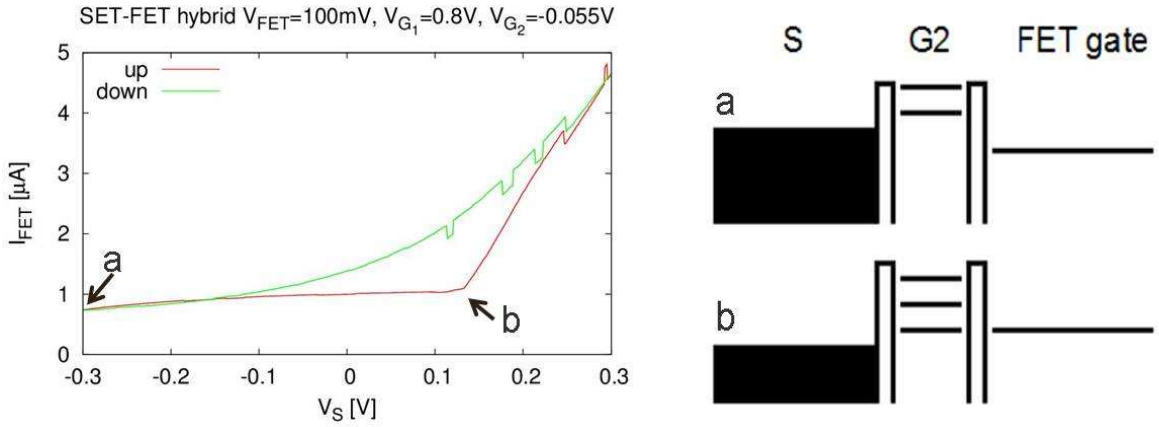


Figure 9.5: I_{FET}-V_S characteristic (V_{G1} = 0.8 V, V_{G2} = -0.055 V, V_{FET} = 0.1 V). In point a the FET gate is still at a positive voltage from the previous sweep, in point b it just aligns with the lowest level of G2.

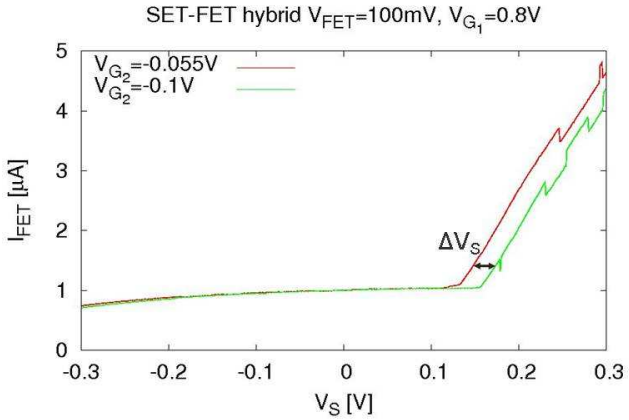


Figure 9.6: I - V characteristic of the FET for two different values of V_{G2}. The shift indicates how much the lowest level of the dot under G_2 has moved due to the change in V_{G2}.

When referencing gates G_1 and G_2 to ground (cf. fig. 9.1 right), the dot potential is fixed for a given gate voltage. Moving S leads to an alignment of the FET gate to the available dot level, as described schematically in more detail in fig. 9.7. In fig. 9.8 the I_{FET} vs V_S characteristics for different V_{G2} values

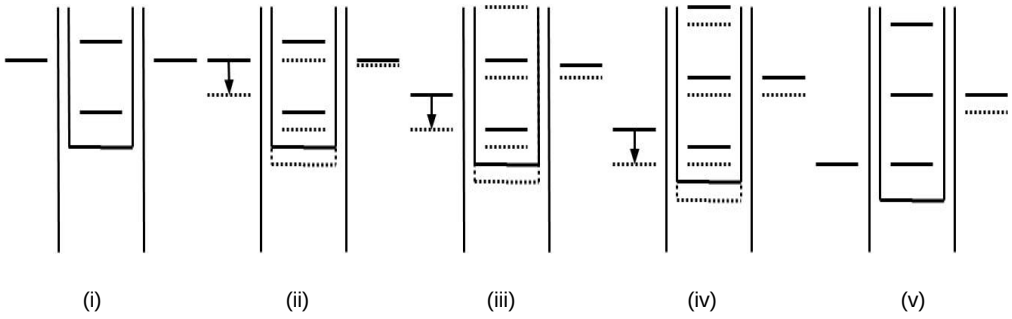


Figure 9.7: Alignment of FET gate to dot levels. from left to right: (i) initial state – source and FET gate at ground potential, dot just defined; (ii) increasing source voltage leads to shifts in potential due to capacitive coupling; (iii) dot potential comes into resonance with FET gate, electrons may flow from gate to source; (iv) FET gate now moves with dot potential until (v) source aligns with next dot level and electrons are able to leave the FET gate and its potential finally aligns again with dot. As (de-)charging currents are limited by the tunnel barriers, this may take some time.

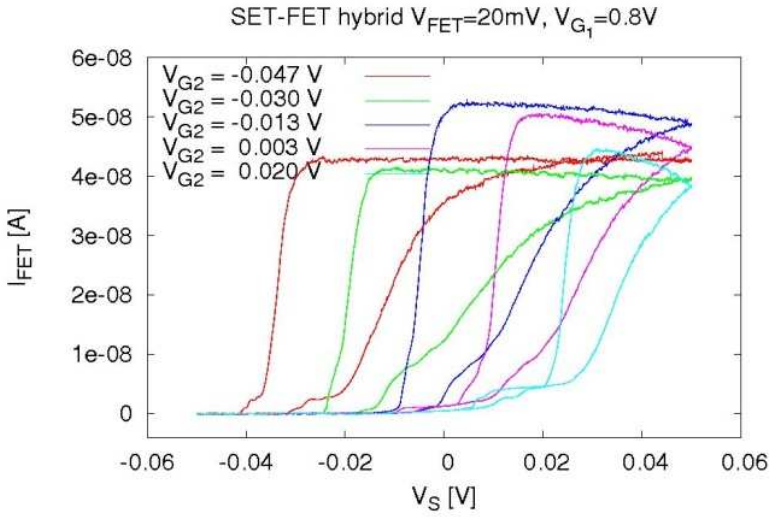


Figure 9.8: Hysteresis of I_{FET} for different V_{G2}.

are presented. V_{G1} is held at a high positive voltage and V_S is swept from -0.05 V to 0.05 V and back to -0.05 V. For all traces a clear hysteresis in the FET current is visible. This effect occurs when S reaches the lowest level of the dot under G_2 so that only capacitive coupling remains to raise the FET gate to a positive potential. The FET gate remains at this positive potential even when the gate V_S is swept back to negative values until S aligns again with the lowest level of the dot. At this point the FET gate will also align with the lowest level and the current in the FET is reduced. This is depicted in more detail in fig. 9.9.

The shift to the right for increasing V_{G2} can be explained by asymmetric tunnel barriers of the dot with a larger one between S and the dot. The tunnel rate depends on the potential difference between the dot and the reservoir. By applying a more positive voltage to G_2 and therefore lowering the potential of the dot, V_S has to reach higher positive values as well before relevant tunneling occurs. Additionally for the traces with more positive V_{G2} the current even increases a bit on the down trace. This indicates a further charging of the FET gate while already raising S, which is also affected by the tunnel barriers by limiting the charge transfer to the FET gate.

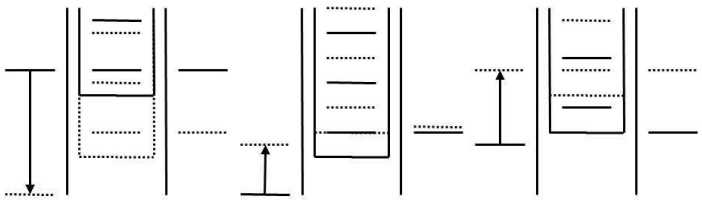


Figure 9.9: Sketch of the energy levels in the SET for the hysteresis in the FET current. Left: when source reaches lowest level action from capacitive coupling remains and FET gate potential increases towards positive values. The FET gate is almost stuck at that voltage (center) until the source aligns again with the lowest level (right).

11. Latch switch

The correlation effect, based on the Coulomb interaction between elementary charges, is exploited in Quantum Cellular Automaton (QCA). For instance, a given drain current resonance depends strongly on the occupation number of other orbitals on the same atom or on capacitively coupled atoms. This could be used as a non-volatile memory cell (indeed it will be the ultimate memory based on charging effect), but also in more elaborate quantum information processing.

One scheme illustrating these correlation effects corresponds to a latching switch which is the building block for neuromorphic type networks[1]. This is a transistor which may be in one of two states, with high or low resistance, corresponding to an ‘‘on’’ or ‘‘off’’ state. The state is determined by another part of the device, a ‘‘single-electron trap’’ which plays the role of a floating gate for the transistor. The trap state, in turn, is controlled by the net voltage applied to the device: a large positive voltage turns the device on, while large negative voltage turns it off. Between these two extremes, the latching switch may be in both states and stay there for a relatively long time.

[1] “Architectures for nanoelectronic implementation of artificial neural networks: new results” O. Turel et al. Neurocomputing 64 271–283 (2005);S. Folling, O. Turel, and K. K. Likharev: Single-electron latching switches as nanoscale synapses, in Proceedings of the 2001 International Joint Conference on Neural Networks (Int. Neural Network Soc., Mount Royal, NY 2001), pp. 216-221; Tûrel, Likharev Int. j. of Circuit Theory Appl. 31, 37 (2003)

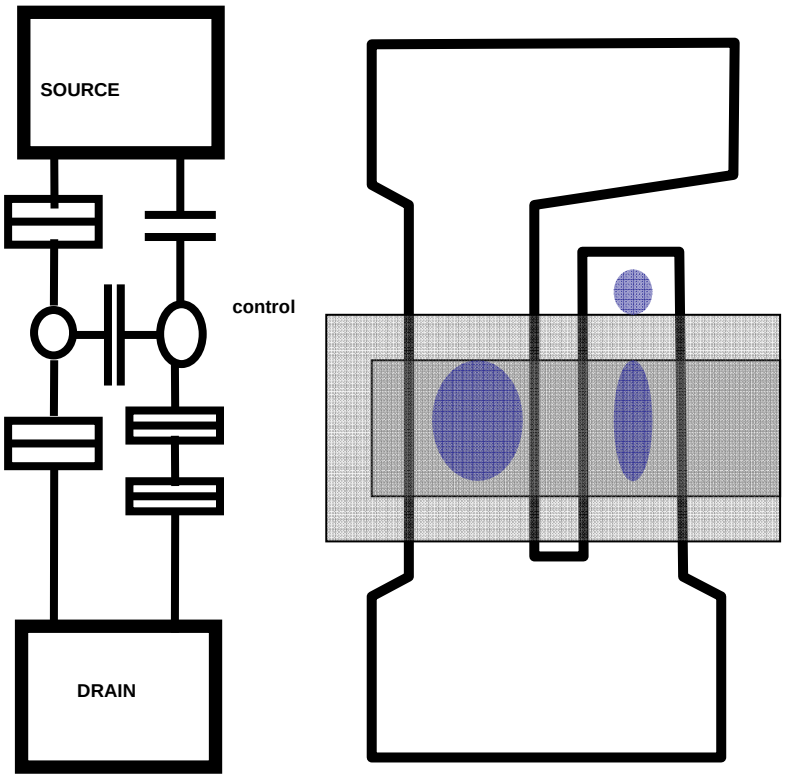


Figure 11.1: a silicon latching switch: a SAT or SET (left arm) is capacitively coupled to an atomic dopant state (real or artificial) in a dead end (control node). At low or negative drain voltage the dopant state is occupied as the energy state is placed below the Fermi level in the drain. The current through the main channel is off. When a sufficient drain voltage is applied the dopant state becomes unoccupied and the source-drain current through the SAT is restored. The right schematic is made for artificial atoms (in blue) with the grey areas representing the gate and spacers

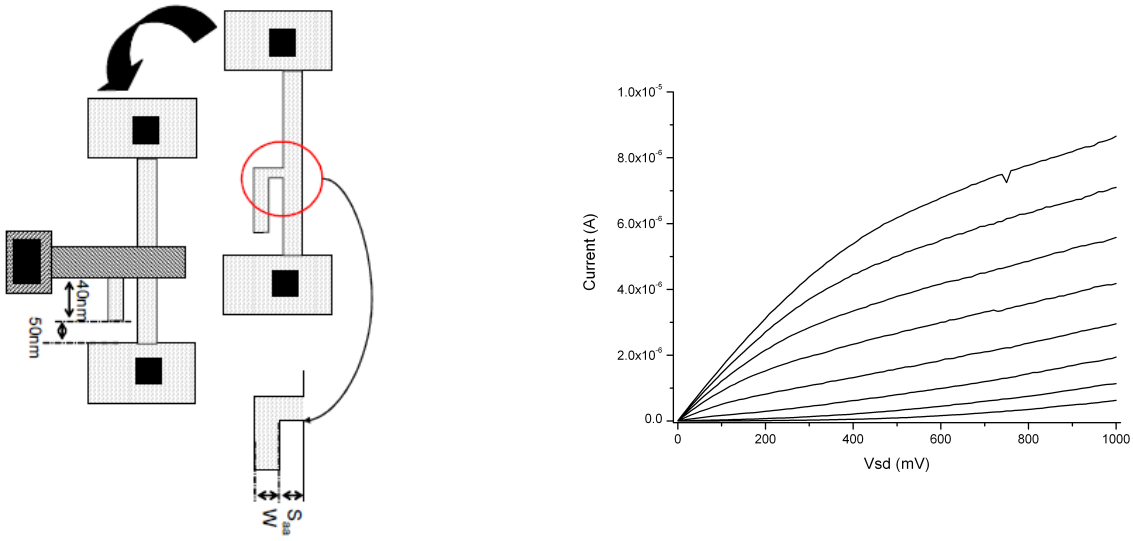
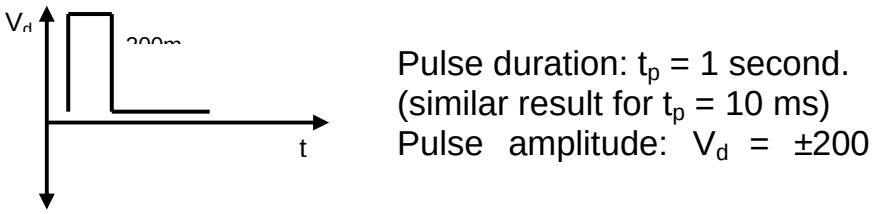


Figure 11.2: Latch switch sample Layout, gate length 40 nm, wire width=40 nm Saa=70 nm. Tsi=20nm As impant of 2.5E11 at 28keV, Rp=1E17 at a depth of 10nm, large 40 nm nitride spacers. A back gate voltage was applied to decrease the access resistances. Room temperature characteristics of the device on the right.

The latch switch has been implemented in AFSiD, in a slightly simpler layout than originally proposed (see figure 11.1). The Latch switch is a two terminal switch (source and drain) with “on” or “off” states controlled by the sequence of applied drain-source voltages (see fig. 11.2). In our implementation the gate and substrate voltages are fixed to particular optimal values. We applied a sequence of drain-source voltages to validate the latch effect at T=4.2K.

At room temperature the device is a MOS-FET (see fig. 11.2 right). When cooled to T=4.2K the latch is put close to its threshold voltage at Vg=-1.4V and Vb=+5V. Figure 11.3 shows that a controllable latch effect has been observed in AFSiD. For a standard nanowire MOS-FET this effect does not occur.



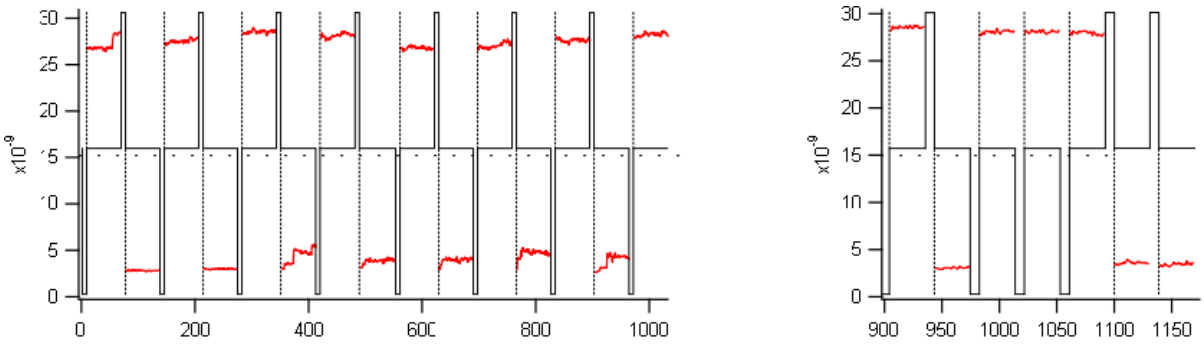


Fig. 11.3: Latch effect implementation at T=4.2K. The Drain-source current (in nA) for Vd=10mv (reading voltage) is plotted as function of time in seconds. The level of current varies between few nA (off state) and 25-30 nA (On-state) depending on the sequence of Vd= +0.2V (writing voltage) or -0.2V (erasing voltage) applied (during 1 sec or less).

12. Conclusion

A large variety of devices with single gates and multiple gates as well as their integration into more complex structures has been designed and built in AFSID many technology splits concerning e.g. spacer width, active silicon thickness, etc.. Characterization of a large number of single gate devices (or single sections of multi-gate devices) showed that excellent MOS-SETs have been realized in the project using optimized nitride spacers. Hundreds of devices have been characterized at low temperature by. Charging energies up to 35 meV (suitable for room temperature) have been identified for smallest functional devices. Modelling was performed for detailed understanding of observed addition spectra.

With multi-gate SETs compact and fully controllable coupled MOS-SETs have been realized and characterized in detail. A floating gate effect in due to discrete charging in poly-silicon gates is identified. Complex and hybrid device configurations have been designed and characterized, leading to an RF-SET configuration working at 750 MHz – with an application as a detector for charging effects in poly-silicon gates, an electron pump working at 100Mhz, a tunable SET-to-FET dvice using substrate polarization, a SET-FET configuration with clear hysteresis effects, a MOS-SET tunnel coupled to a single donor and finally a latch-switch realized with a tunnel coupled dot.