Semiconductor
Equipment
Assessment
Leveraging Innovation

SEVENTH FRAMEWORK PROGRAMME

SEAL PROJECT – BULLETIN

SEAL SP5 – MAPA MAssively PArallel electron beam lithography

AT A GLANCE

Assessment by simulations and experiments

Parallel e-beam lithography for 32nm (22nm logic) node

Integration into mask maker

Assessment of infrastructure (process, data flow and proximity effect correction)

SEAL SP5 – PARTNERS

MAPPER Lithography
CEA/LETI
STMicroelectronics
Toppan Photomasks

Advances in MAPA

The objectives of this sub-project are to support the industrial development of the massively parallel electron beam technology developed by MAPPER to address lithography for 32nm half pitch resolution (22 nm logic node). Furthermore mask making capability are being assessed for the integration into mask maker tool. The assessment of MAPPER technology is done against end users requirements. This sub-project also assesses the necessary infrastructure in terms of process, data flow and proximity effect correction.

FIGURE 1: MAPPER tool at CEA-Leti

MAPPER lithography

Leti

TOPPAN
TOPPAN PHOTOMASKS, INC.

SEAL WEBSITE
www.seal-project.eu

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MAPA – MAssively PArallel electron beam lithography

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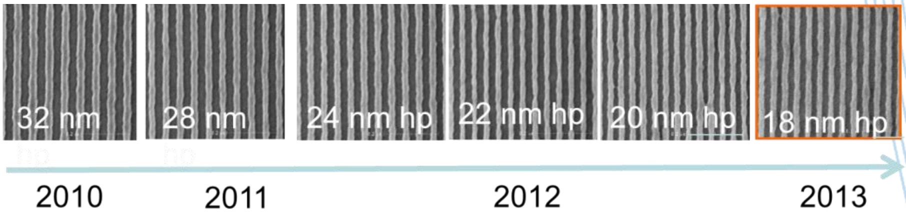
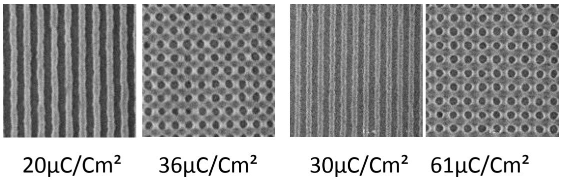
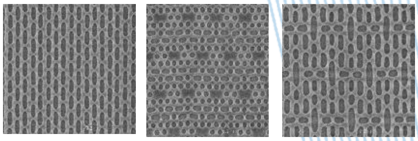
Project Results



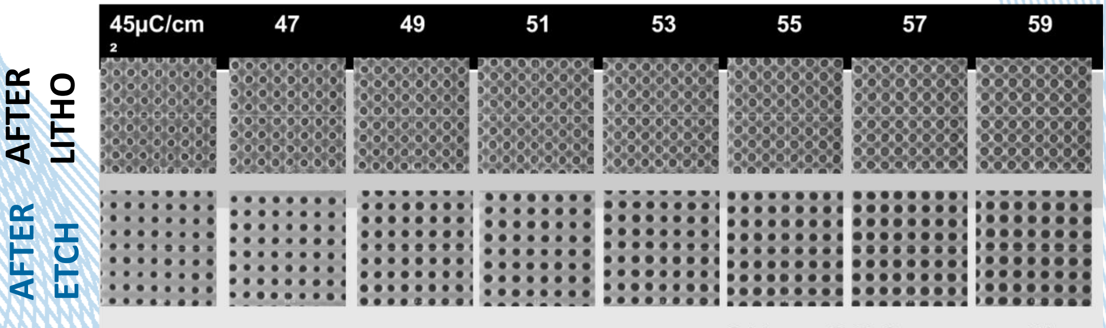
Progress in resolution on the MAPPER tool @ CEA-Leti



Dose target of 30 µC/cm^2 achieved



24 nm hp DRAM, SRAM metal1 & contacts



SiArc+SOC open with standard LETI etch chemistry

Etching of exposed structures demonstrated in standard process

SP5 – CONTACT
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