Multi-Core Execution of Parallelised Hard Real-Time Applications

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http://parmerasa.eu

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Engineers who design hard real-time embedded systems express a need for significant increases in the hardware performance over that available today, but without compromising the safety-critical nature of their software. A breakthrough in performance is expected by parallelising hard real-time applications onto multi-core hardware. parMERASA will provide a timing analysable system of parallel hard real-time applications running on a scalable multi-core processor. Several new scientific and technical challenges will be tackled in the context of timing analysability: parallelisation techniques for industrial applications, operating system virtualisation and efficient synchronisation mechanisms, worst-case execution times (WCET) of parallelised applications, verification and profiling tools, scalable memory hierarchies and I/O systems for multi-core processors.

parMERASA will impact new products for transportation systems and industrial applications. It will impact standards by introducing parallel execution and time predictability as key features. This will contribute to reinforce the EC position in the field of critical computing systems and yield an advantage for European industry in the highly competitive avionics, automotive, and construction machinery markets.
Summary description of the project objectives

The two overall goals of the project are: (1) an increase of the WCET performance of hard real-time embedded systems by targeting time predictable multi-cores; (2) an improvement of performance of legacy code by starting from existing industrial code and migrating it to parallel code preserving time predictability. Additional implicit goals of the project are to provide a significant reduction of the design effort and cost compared to the current state of the art techniques.

Measurable objectives identified to achieve the overall goals:

O1: Develop a software engineering approach targeting WCET-aware parallelisation techniques and parallel design patterns that favour WCET analysis. The software engineering approach should define a development path leading from sequential legacy programs to parallel programs and maximise software reuse. The project will develop at least four patterns that are analysable. These patterns should be applicable to both commercial off-the-shelf (COTS) multi-cores and the parMERASA platform and will be demonstrated during the case studies.

O2: Achieve parallelisation of the industrial case studies by applying the software engineering approach and suitable parallel design patterns. Deliver higher performance than single core processors and achieve at least an eightfold \(^{1}\) WCET speedup (WCET of the sequential program divided by the WCET of the parallel program). This metric will be demonstrated by applying the parMERASA WCET analysis tools on the avionics, automotive, and construction machinery case studies.

O3: Develop on target verification tools, in particular WCET analysis tools with less than 25% pessimism on WCET estimates of parallel programs. Further tools should be developed concerning code coverage and memory analysis as well as parallel program profiling and visualisation. This objective will be demonstrated by review of evidence that can support a certification argument and by applying the tools to the case studies.

O4: Develop a system architecture and system-level SW that supports WCET analysable parallelisation. This will be demonstrated by construction and evaluated during the case studies.

O5: Develop a scalable and timing analysable multi-core processor with at least a 16x\(^{1}\) average speed-up with 64 cores. This objective will be demonstrated by construction of a simulator prototype and evaluated by running the case studies on the simulator. The simulator should be able to simulate at least 500,000 instructions per second.

O6: Contribute to standards. We aim at providing at least four recommendations to either automotive or avionics standards. In particular we will propose a concept for applying the developed parallel design patterns to AUTOSAR and the IMA standard ARINC 653.

O7: Contribute to Open Source software. The software developed at the universities, i.e. the static WCET tool OTAWA, the developed system software and the parMERASA

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\(^{1}\) This is the maximum speed-up to be achieved for some applications while others shall achieve a significant speedup according to the state of the art in their domain.
simulator, will be made publicly available under an Open Source license at the end of the parMERASA project.

**Description of the work performed in the first 14 months of the project**

To reach the objectives work was organised in four technical work package, WP2 Parallelisation of Industrial Hard Real-time Applications, WP3 Verification and Profiling Tools, WP4 System Architecture and System-level Software, and WP5 Predictable Multi-core Processor, accompanied by WP1 Management and WP6 Dissemination and Exploitation. The time plan of the scientific and technological work packages was structured in **three main phases** of which the first was fully completed and the second covered up to the first 5 months in the project reporting period:

**Phase 1: Requirement Specification and Concept** (month 1 until month 9).

**WP2**: A first exploration of the industrial applications and suitable parallel design patterns was conducted. To do so, software engineering methodologies and parallel design patterns known from high-performance computing were evaluated with respect to time analysability of the resulting parallel programs, and a first parallelisation method and pattern catalogue was devised by University of Augsburg. On side of application companies, suitable sequential hard real-time programs were select that will be parallelised and requirements to the other work packages were specified. These applications are: for avionics (Honeywell International s.r.o.) 3D Path Planning algorithm intended for airborne collision avoidance, Stereo Navigation intended for aircraft localization, and Global Navigation Satellite System (GNSS); for automotive (DENSO AUTOMOTIVE Deutschland GmbH) the engine control for diesel fuel injection; and for construction machinery (BAUER Maschinen GmbH) the control algorithm for a dynamic compaction machine.

**WP3**: Requirements to WCET analysis and verification tools were assessed. Timing analysability of parallel design patterns was investigated and synchronisation primitives to implement the patterns were devised [1]. A method to compute worst-case waiting times in combination with an annotation scheme of the parallel source code was proposed. Specifications for verification and profiling tools were developed based on the tool requirements of the project partners.

**WP4**: An overall system architecture [2] was defined based on requirements of the applications. Requirements of TinyAUTOSAR, TinyIMA and construction machinery run-time environments (RTEs) as support for the different industrial application domains were defined. The RTE implementations will be based on a common kernel library.

**WP5**: Current COTS processors were analysed for suitability as a basis for the parMERASA core and the PowerPC ISA was selected. To do so, hardware structures (interconnects, MMU, cache) were investigated with respect to time analysability. Finally, a preliminary usable version of the parMERASA simulator was provided to other WPs.

**Phase 2: Implementation** (month 10 until month 24). The reporting period stretches to month 5 of the 15 months phase 2; so only preliminary results are available.

**WP2**: The industrial applications will be parallelised towards suitable parallel design patterns targeting maximum parallelism. Parallel design patterns will be refined into programming
guidelines, system software requirements, and necessary hardware requirements by University of Augsburg in collaboration with the application companies. The parallelisation method was already refined towards UML modelling (a suggestion of the Industrial Advisory Board). Currently, the application companies are in different stages to prepare parallelisation or already started with preliminary parallelisations. The 3D Path Planning algorithm was parallelized and analysed for P4080 COTS multi-core by Honeywell International s.r.o.. Algorithm patterns were defined for the Stereo Navigation algorithm and the GNSS. The engine control code of DENSO AUTOMOTIVE Deutschland GmbH was made AUTOSAR compatible, most runnables were WCET analysed with OTAWA and RapiTime. Current work concerns dependency analysis and parallelisation. The control algorithm for dynamic compaction machine of BAUER Maschinen GmbH was preliminarily parallelised and a RapiTime analysis is under way.

WP3: Tool support for WCET analysis, verification, and profiling of parallel programs will be developed to assist the applications. Up to now WCET analysis tool OTAWA of University of Toulouse was enhanced by the PowerPC ISA, which was selected as core ISA of the parMERASA multi-core processor, the specification of the annotation format was refined, and a further analysis of synchronisation primitives is in progress. Five verification and parallelisation support tools were selected by Rapita Systems Ltd. based on the application companies’ requirements, and two are in the state of implementation. The identified tools are: (1) Extension of RapiTime to provide on-target timing and WCET analysis tool for parallel programs; (2) Extension of RapiCover to provide on-target code coverage tool for parallel programs; (3) Memory, cache and stack analysis tool for parallel programs; (4) Tool to assist with the parallelisation of existing sequential software; (5) Visualisation and profiling tool for parallel programs. It was decided on basis of application companies’ requirements that tool (4) and (5) are the most urgently required ones in phase 2 of the project.

WP4: The parMERASA system software, i.e. kernel library as common virtualisation platform and individual “Tiny” RTEs for each application domain are under development to assist the applications. Currently, the kernel library is widely implemented and the TinyAUTOSAR implementation started ahead of time by University of Augsburg, because of application company request (the DENSO AUTOMOTIVE Deutschland GmbH application requires TinyAUTOSAR functions to run).

WP5: Time analysable hardware structures (interconnects, MMU, cache, core connect) will be designed and built into the parMERASA simulator. Currently, a clustered multi-core architecture based on simple cores and predictable interconnect is under development by Barcelona Supercomputing Center. We target hard real-time support by guaranteeing full isolation of parallel applications (as required by ISO 26262 and ARINC 653 standards) and bounding the effect of inter-thread interferences among parallel threads belonging to the same application. NoC structures are evaluated and time predictable interconnects were proposed [3]; cache investigations let to a patent application [4] by University of Dortmund. Memory layout is to be defined based on the requirements of the different applications. An improved
version of the simulator was delivered by Barcelona Supercomputing Center to the other work packages and runs at all partner sites.

**Phase 3: Optimisation, Refinement and Evaluation** (month 25 until month 36). This will cover the third project year.

**Conclusions and Description of the Main Results at Month 14 (November 2012)**

parMERASA targets parallelising hard real-time programs to run on predictable multi-/many-core processors. The first project phase (Oct. 2011-June 2012) “Requirement Specification and Concept” has been successfully completed. The project is currently in month 5 of the second project phase (July 2012-September 2013) “Full Specification and Implementation”. Encouraging preliminary results are available.

From application side five use cases were selected for parallelisation: for avionics (Honeywell International s.r.o.) 3D Path Planning, Stereo Navigation, and Global Navigation Satellite System (GNSS); for automotive (DENSO AUTOMOTIVE Deutschland GmbH) the engine control for diesel fuel injection; and for construction machinery (BAUER Maschinen GmbH) the control algorithm for a dynamic compaction machine. A parallelisation method was devised and refined towards UML modelling. The parallelisation method targets parallel design patterns selected together with the application companies. For the static WCET analysis tool OTAWA, source code annotations for parallelisation analysis were defined that are based on the parallel design patterns. Requirements on verification tools were defined and five verification and profiling tools selected, which will be implemented based on Rapita Systems’ RVS tools. The overall system architecture, common microkernel library functions and the required functionalities for TinyAUTOSAR, TinyIMA, and construction machinery RTEs are defined. The microkernel library and TinyAUTOSAR functions are partly implemented. Multi-core architecture design space exploration was done based on the requirements of the applications, system architecture and WCET analysis. A consolidated version of parMERASA multi-core simulator was made available.

**References**


