PowerSWIPE (Project no. 318529)

"POWER SoC With Integrated PassivEs"

Deliverable 6.1.1

"First Annual Management Report"

Dissemination level: PU

Responsible Beneficiary
Tyndall

Due Date
30th September 2013

Submission Date
31st October 2013

Summary					
No and name	**D6.1.1 – First Annual Management Report**[1]				
Status	Released	**Due**	Month 12	**Date**	30-September-2013
Author(s)	Nicolás Cordero				
Editor	Cian Ó Mathúna				
DoW	Report on Project Management from Oct 2012 to September 2013				
Dissemination Level	**PU - Public**				
Nature	Report				

Document history			
V	**Date**	**Author**	**Description**
Draft	18-Oct-2013	N.C.	Draft
1.0	25-Oct-2013	N.C. et al.	Inputs from all partners for WP reports
2.0	29-Oct-2013	N.C.	Small corrections, formatting, “typos”.

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1. Table of Contents

2. PROJECT PERIODIC REPORT

Grant Agreement number: 318529

Project acronym: POWERSWIPE

Project title: Power System-on-Chip (SoC) with Integrated Passives

Funding Scheme: FP7-ICT-2011-8

Date of latest version of Annex I against which the assessment will be made: 4th September 2012

Periodic report: **1st** ■ **2nd** □ **3rd** □

Period covered: **from** 1st October 2012 **to** 30th September 2013

Name, title and organisation of the scientific representative of the project's coordinator[2]:

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Project website[3] address: www.powerswipe.eu

[2] Usually the contact person of the coordinator as specified in Art. 8.1. of the Grant Agreement.

[3] The home page of the website should contain the generic European flag and the FP7 logo which are available in electronic format at the Europa website (logo of the European flag: http://europa.eu/abc/symbols/emblem/index_en.htm logo of the 7th FP: http://ec.europa.eu/research/fp7/index_en.cfm?pg=logos). The area of activity of the project should also be mentioned.

3. Declaration by the scientific representative of the project coordinator

I, as scientific representative of the coordinator of this project and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;
- The project (tick as appropriate) [4]:
  - ■ has fully achieved its objectives and technical goals for the period;
  - □ has achieved most of its objectives and technical goals for the period with relatively minor deviations.
  - □ has failed to achieve critical objectives and/or is not at all on schedule.
- The public website, if applicable
  - ■ is up to date
  - □ is not up to date
- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project (section 3.4) and if applicable with the certificate on financial statement.
- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 3.2.3 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

Name of scientific representative of the Coordinator: .....

Date: ...../ ...../ .....

For most of the projects, the signature of this declaration could be done directly via the IT reporting tool through an adapted IT mechanism and in that case, no signed paper form needs to be sent

[4] If either of these boxes below is ticked, the report should reflect these and any remedial actions taken.

3.1 Publishable summary

3.1.1 Description of project context and objectives

Combing high efficiency with cost-effective but high level of integration is the major driver in power electronics today. PowerSwipe responds to the call for "advanced More-than-Moore elements" and "their integration and interfacing with existing technology" by aiming to develop innovative Power Supply in Package (PwrSiP) and Power Supply on Chip(PwrSoC) technology platforms through highly integrated passives and advanced CMOS. The PowerSwipe concept addresses the key challenges of "systemability", "integratability" and "manufacturability" for System on Chip (SoC) power management platforms.

An advanced design optimization tool will be developed with both component and system perspective. PowerSwipe will leverage the existing expertise of the consortium in the area of integrated passive and power management design to achieve a first integrated system-level design tool for SoC applications. Additionally, High-volume MEMS manufacturing processes for the monolithic power passives will be developed to enable deployment of the technologies in commercial applications. A custom PwrSiP/PwrSoC will be developed to maximise the system performance in high volume silicon technology. On-chip intelligence will enable system performance to be optimised for different applications. A top-down system design approach will take full advantage of the benefits of the integrated magnetic and capacitive components while resolving issues due to smaller absolute component values, higher switching losses and increased on-chip interference and coupling.

Two intermediate test Vehicles and two demonstrators will address a target applications (e.g. automotive) and system requirements (efficiency, performance, reliability/lifetime, cost, size). The project aims to establish Europe as the leading global player over the coming decade in this emerging space by creating a competitive, European supply chain in Power Supply platform for System on Chip applications with no major missing links.

3.1.2 Description of work performed since the beginning of the project and main results achieved so far

Tasks performed since the beginning of the project:

- Definition of target application requirements
- System architecture, block-level optimisation and integrated circuit design
- System level analysis and optimisation
- Analysis and optimisation of integrated passives
- Passives (inductor, capacitor and interposer) process development
- Inductor technology transfer
- Development of project Web site

Achieved milestones:

- Ms1.1 – Application requirements defined (Month 3)

- Ms1.2 – First system architecture (Month 9)
- Ms2.1 – Architecture analysis and evaluation (Month 12)
- Ms2.2 – Analysis and optimisation of integrated passives (Month 12)

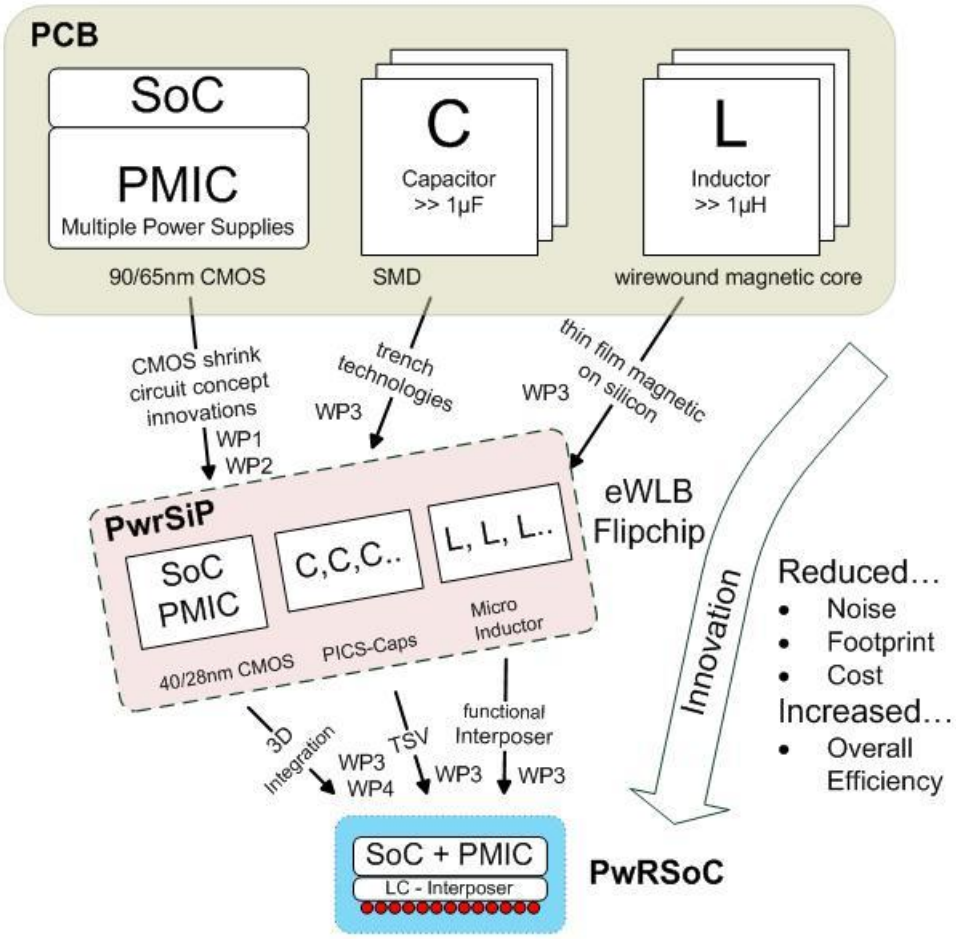
Completed and submitted deliverables:

- D5.1 – Project Web site (Month 3)
- D3.1 – Inductor process documentation ready for transfer (Month 6)
- D1.1 – First system architecture description (Month 12)
- D1.2 – Target block-level specification (Month 12)
- D2.1 – Analysis and evaluation of first system architecture (Month 12)
- D2.2 – Analysis and optimisation of integrated passives (Month 12)

3.1.3 Expected final results and their potential impact and use (including the socio-economic impact and the wider societal implications of the project so far)

PowerSwipe will develop ...

- ... a demonstrator, consisting of multi-component LC (inductor-capacitor) interposer, which can be combined in a 3D heterogeneous stack together with the SoC/PMIC chip
- ... integrated passive components fulfilling the stringent temperature (125deg) and quality requirements required by the automotive market and thus closing today’s gap in availability of components
- ... inductor and capacitor based very high-frequency DC-DC converters in 40nm CMOS operating at 5V supply, ready for 3D integration with power passives
- ... integrated very high-frequency DC-DC converters allowing PCB footprint reduction by ~100mm² per module, without compromising converter efficiency at 90%
- ... missing system and component level optimization tools to achieve optimum system configuration and efficiency for different operating modes
- ... a demonstrator system targeted for Automotive Microcontroller, with optimized complete chain from car battery (5...48V) down to the core voltage domain (1V)



System level schematic of the PowerSwipe project innovations

3.1.4 Project website, logos and partners

Project Website:

www.powerswipe.eu

Project logo:

Project banner:

Project partners:

Participant no. *	Participant organisation name	Part. short name	Country
1 (Coordinator)	University College Cork, National University of Ireland, Cork	Tyndall-UCC	IE
2	Infineon Technologies AG	IFX	DE
3	Infineon Technologies Austria AG - Villach	IFAT	AT
4	IPDiA	IPDiA	FR
5	Universidad Politécnica de Madrid	UPM	ES
6	Robert Bosch GmbH	Bosch	DE
7	Université de Lyon, Claude Bernard	UCBL	FR

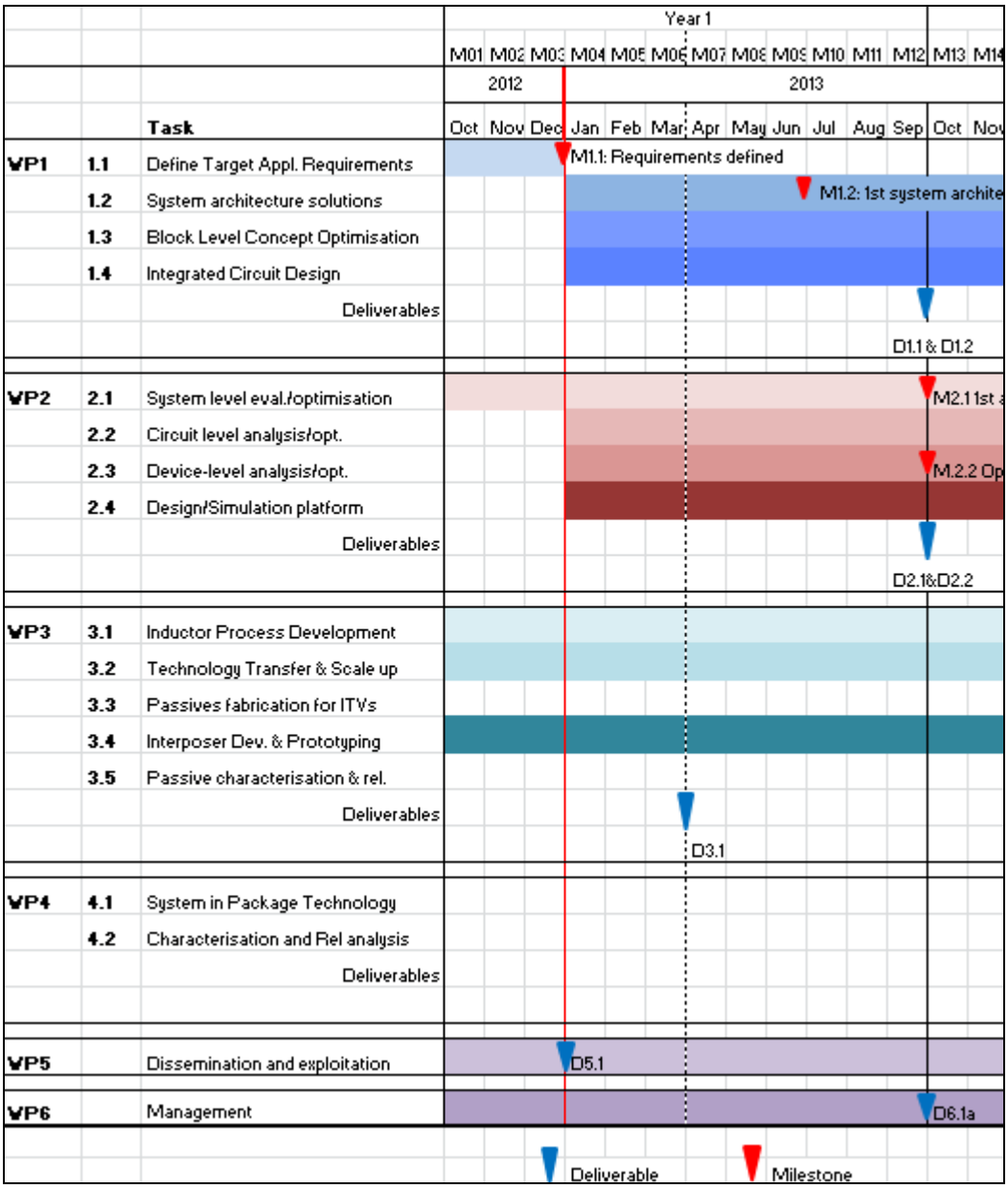
3.2 Core of the report for the period: Project objectives, work progress and achievements, project management

3.2.1 Project objectives for the period

The main objectives of the PowerSwipe project for Year 1 for were:

- Definition of target application requirements
- System architecture, block-level optimisation and integrated circuit design
- System level analysis and optimisation
- Analysis and optimisation of integrated passives
- Passives (inductor, capacitor and interposer) process development
- Inductor technology transfer
- Development of project Web site

The following figure shows the Gantt chart with the tasks, deliverables and milestones for the period.



There were no recommendations from previous reviews as this is the first year of the project.

3.2.2 Work progress and achievements during the period

Please provide a concise overview of the progress of the work in line with the structure of Annex I to the Grant Agreement.

WP1 – System Specifications and Design

WP Objectives for Year 1

- Define the overall target requirements from application level down to component level
- Circuit Concept and Design of integrated circuits

Work Progress

Tasks finished

Milestone 1.1 Define Target Application Requirements

- Identify and define all relevant requirements for PwrSoc and PwrSiP integration of power management systems within a defined load power range of a few Watt (load currents up to 1.5Amp).
- Map these requirements to an envisioned demonstrator in the automotive uC application range (based on 12V car battery system with embedded uC subsystem, consider quality requirements like AEC-Q200)

Milestone 1.2 Propose and evaluate system architecture solutions

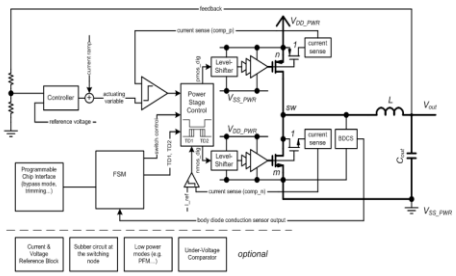
- Holistic optimization of power management system architecture from Vbattery to Vcore:
  - Number of conversion stages/distribution, consider thermal budget in package
  - Define required sub blocks
- Standby/startup modes
- Define architecture for demonstrator system of WP4
- Investigate 200MHz+ operation, countermeasures on expected efficiency loss, benchmark with moderate switching frequency increase

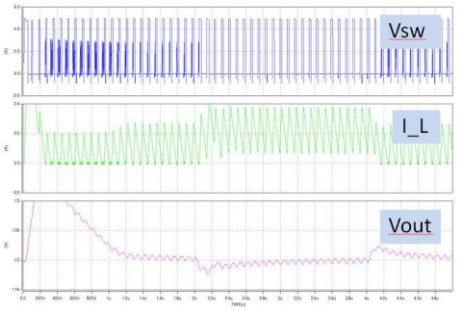
- **Deliverable 1.1 First System Architecture Description**
- **Deliverable 1.2 Target Bloc-Level Specification**

Significant Results

Low Voltage (LV) DC-DC converter design

- General
  - L: 250nH
  - Cin/Cout: 400nF
  - fsw: 11MHz
- Controller
  - Analogue peak current control
  - Automatic PWM-CCM <-> PWM-DCM handover
  - Artificial ramp generator to avoid steady state oscillation
- Blocks
  - Output stage with TOX transistors
  - Automatic dead time optimization during normal converter operation
  - Digital state machine to control the over all converter behaviour and the interface





- First spice simulation results of the whole output stage with the controller available, it includes the blocks:
  - Power stage
  - High/Low side current sense
  - Level shifters
  - Power stage control with dead time generation
  - Automatic dead time reduction
  - Peak current controller
- Simulation with 100mA/2ns load jumps
  - Converter changes automatically from PWM-CCM to PWM-DCM and back
  - Voltage drop on the converter output: about 25mV

High Frequency (HF) DC-DC converter design

- General
  - E_0 = 3.3 V
  - L: 30 nH
  - Cin: 20 nF + 2 x 10 nF
  - Cout: 10 nF
  - Fsw: 200 MHz
  - Final demonstrator will have 2 coupled phases
- Controller
  - 1st version in open loop
  - Final demonstrator with voltage controlled PWM
  - CCM and DCM control modes
- Blocks
  - Output stage with cascoded REG transistors
  - Drivers with stacked power supply
  - Voltage control feedback
  - Level shifting

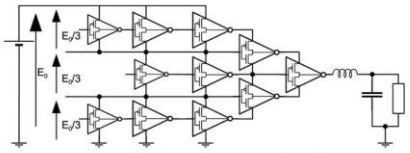


Fig. 2: 1st demonstrator concept schematic

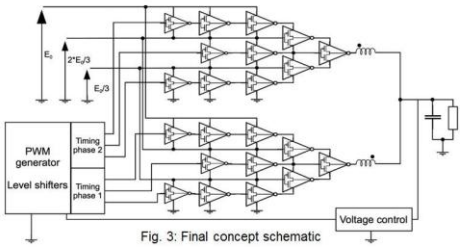
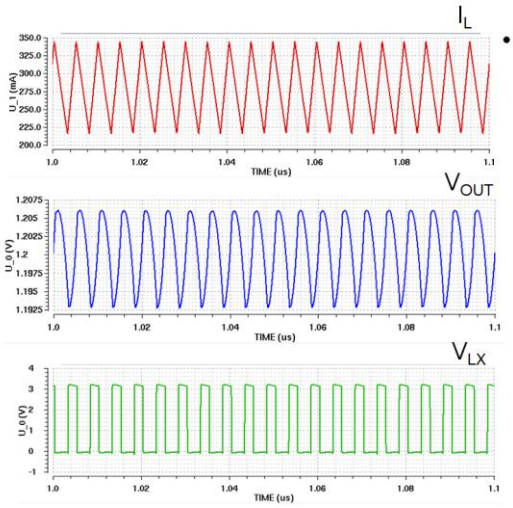


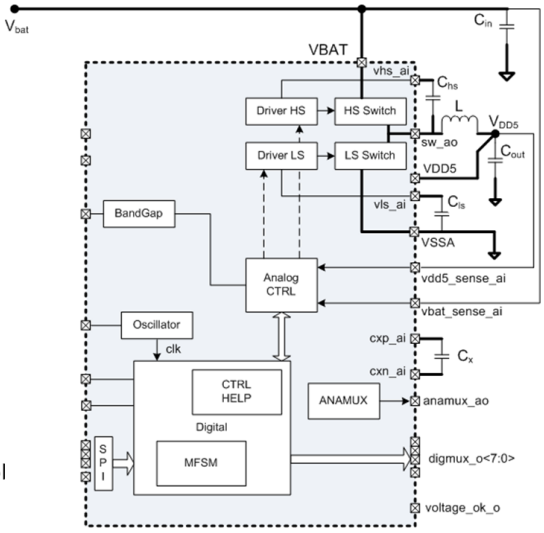
Fig. 3: Final concept schematic



- Power stage simulations (single phase)
  - Efficiency evaluation @ 200 MHz (nominal power point):
    - Single phase standard power stage: 75 %
    - Single phase cascoded power stage: 85 %
    - Polarisation power (E_0/3 and 2*E_0/3): 5 mW
  - Functional evaluation (1 phase):
    - 1 phase static current ripple: 128 mA
    - Static output voltage ripple: 15 mV (± 0.7 %)
    - Dynamic output voltage ripple (load jump: ± 50 mA / 2 ns): ± 80 mV (± 6 %)

High Voltage (HV) DC-DC converter design

- General
  - L: 1uH
  - Cin/Cout: 200nF/500nF
  - fsw: 10MHz
  - Newest generation Smart Power technology
- Controller
  - Analogue sliding mode control
  - Soft start
- Blocks
  - Nmos/Nmos output stage
  - Low voltage output supplied push pull drivers
  - Voltage sensing and current reconstruction for analogue control
  - Digital interface and master state machine



WP2 – Computer-aided Optimisation and Analysis

Work Package Objectives

The objectives for WP1 for year 1 were:

1) To develop basic models and optimisation tools from the system to the component to design the demonstrators of the project based on:
   - Electrical specifications defined in WP1 (M1.1 Requirements)
   - Technological constraints of passives provided by Tyndall and IPDIA
   - Semiconductor Power Device characteristics provided by Infineon
   - Geometrical constraints provided in WP3 regarding the layout
   - Different converter topologies (single phase buck, multiphase buck and multiphase with coupled inductors)
   - Different operation modes: Continuous Conduction Mode, Discontinuous Conduction Mode and Burst Mode.
   - Different control strategies that affect the size of the passives to meet dynamic requirements (voltage mode control, peak current mode control)
2) Analyse and optimise different topologies for Low Voltage and very high switching frequency converter (200MHz)
   - Electrical specifications defined in WP1 (M1.1 Requirements)
   - Technological constraints of passives provided by Tyndall and IPDIA
   - Semiconductor Power Device characteristics provided by Infineon Design Kit
   - Different power cells (standard and cascoded)
   - Different converter topologies (single phase buck, multiphase buck and multiphase with coupled inductors)
   - Simple control strategy

As a result of this optimization:

- The topology and control for the power stages has been selected.
- the PMIC power devices have been designed
- The optimum values for the power inductors have been selected at system level
- A device level optimization of the inductors have been done based
- The optimum values for the IPDIA trench capacitor have been selected for the application

Work Progress

Regarding WP2 all the objectives for the first year has been met.

- A system level optimization tool has been designed that allows selecting the best topology, the control and optimize the passive components and power devices
- MOSFETs performance has been evaluated with respect to efficiency and conclusions regarding possible solutions in line with specifications
- Alternative power stage that enhance efficiency has been analyzed through simulation
- A device level optimization tool for the optimization of the magnetic components has been developed. The optimization is based on the combination of analytical and finite element models.
- Accurate models for the optimization of integrated capacitors have been developed.
- Population of landscapes as a representation of the state-of-the-art. Situation of project objectives with quantitative indicators.

Significant Results

- System level optimization tool based on models of the main components (magnetics, capacitive, parasitic interconnections and power devices). This tool allows optimizing and analysing:
  - Different topologies (single phase buck converter, two phase interleaved buck converter and two phase interleaved buck converter with coupled inductors)
  - Different operation modes: Continuous Conduction Mode, Discontinuous Conduction Mode and Burst Mode for improving energy efficiency at light load
  - Different control algorithms: Voltage Mode Control and Peak Current Mode Control
- Characterization procedure of the power semiconductor devices based on accurate CADENCE simulations to estimate conduction and dynamic losses in the system level optimization.
- Power Inductor optimization tool. This tool helps on the detailed optimization of the power inductor selected by the System Level optimization tool. The tool accounts for the technological constraints of the manufacturing process (metal thicknesses, form factors, laminations, core materials, etc.) and the size constraints of the layout.
- Integrated Capacitor SPICE model development to account for parasitic effect.
- Accurate equivalent circuit of integrated capacitor to account for the losses and ripple in the system level optimization
- Placement of VHF DC-DC converter on state-of-the-art landscapes to highlight novelties and challenges of the design
- Technology performance analysis for VHF DC-DC converter resulting in the choice of a device and power stage
- Different topologies (single phase buck converter, two phases interleaved buck converter, two phases interleaved buck converter with coupled inductors, 3-levels converter) have been analysed in system level simulations for VHF DC-DC converter, highlighting the interest of coupled inductors
- Development of cascoded power cell
- Providing specifications for capacitors interposer for ITV2
- PMIC design
- Investigation on cascoded power stage on detailed switching losses and deadtime optimization

Documentation for the system level optimization: **D2.1” First architecture: Analysis and evaluation”**
Documentation for the magnetics: **D2.2*” Analysis and optimization of the integrated passives*”**

WP3 – Technology Development

Work Package Objectives

The objectives for WP3 for Year 1 were (also to continue in Year 2):

1) Inductor and capacitor process development, continue until the end of project (M1-M36)
   - Tyndall will continue to develop an optimised inductor manufacturing process.
   - IPDIA will develop specific capacitor process to fulfil voltage/reliability requirements (i.e. 6V/48V).
2) Technology transfer and scale up (to complete by M20)
   - Tyndall will provide process documentation(existing process) for technology transfer and a documentation on the technology improvements
   - IFX to scale up the inductor process to 200mm and co-develop to adapt to IFX magnetic fabrication facility by M24.
3) Interposer development (to complete by M26)
   - Integrated LC interposers will be developed.
   - IPDIA to optimize and upgrade passive interposer substrate with integrated capacitors, RDL and TSVs for power applications (for Demo1).
   - IFX to fabricate inductors on reconstituted interposer wafers from IPDIA containing capacitors, RDL and TSV for Demo1.
   - IPDIA to produce PICs and cohabitate µbump over PICS in preparation of Demo2
   - Tyndall and IPDIA to cohabitate inductor on PICS (for D2).

Work Progress

All the objectives for WP3 for the first year have been met.

- Process development for integrated inductors enabling lower winding resistance and reduction of core loss have been identified and is being investigated:
  - MEMS processing for high aspect ratio copper conductor. A process to build a higher aspect ratio conductor has been explored with thicknesses up to 50 µm (currently 30µm), with the potential to nearly half the coil resistance.
  - High resistivity magnetic material and multilayer laminated cores: the magnetic material $Ni_{45}Fe_{55}$ will be used to avail its relatively higher resistivity and higher saturation compared to $Ni_{81}Fe_{19}$. A laminated core approach using sputtering techniques is also being developed to reduce the magnetic core eddy current loss at high frequencies.
- Process development for trench capacitors
  - To meet ESR and LV stage requirements
    - Develop a concept of quasi-fractal capacitor to adapt ESR/ESL requirements for DCDC conversion.
    - Implement fractal structures on IPDIA internal Multi Project Wafer (MPW1) run (Q1 2013).
    - Extract numeric and lumped element models in the range 300kHz – 1GHz (Q2 2013) to demonstrate viability.
    - Design specific capacitive components upon WP1/WP2 requirements for ITV1/ITV2 (Q3 2013).
    - Implement ITV1/ITV2 capacitive components + extended characterization structures on a second MPW (MPW2 -September2013).
    - MPW2 silicon is available since W4 October and will be characterized in November.
  - To meet HV stage requirements
    - Preliminary reliability study on candidates for HV dielectric (Al_2O_3)
    - Remark: fractal concept will be re-usable for HV stage

- Transferring Tyndall's Magnetics processing technology to Infineon through 'Powerswipe' project is progressing as planned:
    - The first stage in this task was process documentation, which was completed in December 2012, reviewed by Infineon process team, followed by discussions around key issues including deposition of magnetic layers, dielectric insulation, etc.
    - Final process transfer document was completed and submitted as deliverable D3.1 in April 2013.
    - Further, the two teams met again during Consortium's 6-month review held in Regensburg in April 2013.
    - Alternate magnetic deposition technique such as sputtering has been selected to suit Infineon facilities.
    - Tyndall have sourced appropriate NiFe target and successfully completed trials for sputtering NiFe thin films.
    - Tyndall team is presently looking at sputtering in magnetic field. Infineon is investigating potential for annealing sputtered wafers in magnetic field to further improve magnetic properties.
- Process development for integrated LC interposer
    - Process flows for Demos have been streamlined and agreed.
    - The feasibility of cohabiting integrated inductors on trench capacitor substrate is undergoing, with the process trials started in July 2013.
    - The EMI issue associated with cohabitated inductor and capacitor has been studied. Based on the simulation results, approaches to minimize the EMI have been identified, which will be implemented in LC interposer fabrication.

Significant Results

- Process development for integrated inductors:
    - A higher aspect ratio conductor has been achieved based on a newly developed process with Cu thickness up to 35µm and a spacing of 10µm.
    - Sputtering of magnetic material with higher saturation density and higher resistivity has been completed. Insulation materials for isolation to achieve core lamination have been identified.
    - Specific deposition fixture to facilitate sputtering magnetic materials with applied magnetic field has been constructed. Initial deposition trial on sputtering magnetic material with magnetic field has been complete, which is critical for achieving low loss at high frequencies.
- Process development for trench capacitors:
    - Proved that low ESR/ESL requirements can be met on LV stage with specific design style.
    - Delivered corresponding model to WP1 and delivered silicon for extended characterization.
    - Delivered silicon for ITV1/ITV2.
- Transferring Tyndall's Magnetics processing technology to Infineon:
    - 1st draft of process transfer documentation was completed in December 2012,
    - Infineon confirmed that their existing fabrication facility meet the inductor process scale-up requirements (except that deposition of magnetic core needs to be sputtering).
    - Final process transfer document was finalised and submitted as deliverable D3.1 in April 2013.
    - Alternate magnetic deposition technique has been demonstrated using Tyndall fabrication facility.

- Process development for integrated LC interposer

- EMI issue on LC interposer was studied. Approaches to minimise/eliminate EMI have been identified and confirmed by numerical simulations.

WP4 – System Integration

The activities of WP4 are not planned to start until Month 19.

WP5 - Dissemination

The main dissemination objective during the period was the development of a project Web site. For more details, please check Deliverable D5.1., or go to http://www.powerswipe.eu

As part of the Web development, a project logo and a project banner were also designed.

To give a uniform and easily recognisable project appearance, standard templates for both reports and presentations were also set up.

A LinkedIn group dealing with PowerSoc was also created, with both members and non-member of the PowerSwipe consortium taking part in rewarding discussions on the topic.

Several papers were submitted/presented at relevant conferences: Compel'13, CIPS'14, APEC'14. The consortium is also actively pursuing the preparation of Professional Seminars in conjunction with some of these conferences. The IEEE Trans. On Power Electronics published a special issue on PowerSoc in Sep'13, with the Cian Ó Mathúna –PowerSwipe project co-ordinator- acting as Guest Editor.

Deviations from plan and corrective actions

No deviation from plan for Year 1

3.2.3 Project management during the period

Management tasks included the organising of consortium meetings, internal reporting on work progress (monthly) and submission of deliverables.

Project meetings were organised on a regular basis, as well as WP specific meetings and discussions:

- Consortium meetings were carried out on the first Tuesday of every month via teleconference with the support of multimedia sharing facilities (WebEx)
- Consortium meetings every six months:
  - Kick-off meeting: Cork, 15-16 October 2012
  - 1st Six-monthly meeting: Regensburg, 16-17 April 2013
  - 2nd Six-monthly meeting: Madrid, 9-10 October 2013
- WP-specific meetings were organised when required:
  - WP2: Tyndall visit to CEI-UPM in May 2013

The project consortium kept a Document Repository where all common documents and internal reports are shared.

All required legal, administrative and financial documents and procedures were taken care of. The Consortium Agreement was negotiated and the final agreed document signed in October 2013.

Changes in consortium

No changes

Impact of possible deviations from the planned milestones and deliverables

No deviations during Year 1.

3.3 Deliverables and milestones tables

Deliverables

TABLE 1. DELIVERABLES										
Del. no.	**Deliverable name**	**Version**	**WP no.**	**Lead beneficiary**	**Nature**	**Dissemination level[5]**	**Delivery date from Annex I**	**Actual / Forecast delivery date**	**Status No submitted/ Submitted**	**Comments**
D5.1	Project Web Site	1.1	5	Tyndall	O	PU	M3	M4	Submitted	
D3.1	Inductor process documentation ready for transfer	Final	3	Tyndall	R	PU	M6	M7	Submitted	
D1.1	First system architecture description	Final	1	IFAT	R	CO	M12	M13	Submitted	
D1.2	Target block-level specification	Final	1	IFAT	R	CO	M12	M13	Submitted	
D2.1	Analysis and evaluation of first system architecture	Final	2	CEI-UPM	R	PU	M12	M13	Submitted	
D2.2	Analysis and optimisation of integrated passives	Final	2	CEI-UPM	R	PU	M12	M13	Submitted	
D6.1.1	First Annual Management Report	2.0	6	Tyndall	R	PU	M12	M13	Submitted	

[5] **PU** = Public
PP = Restricted to other programme participants (including the Commission Services).
RE = Restricted to a group specified by the consortium (including the Commission Services).
CO = Confidential, only for members of the consortium (including the Commission Services).
Make sure that you are using the correct following label when your project has classified deliverables.
EU restricted = Classified with the mention of the classification level restricted "EU Restricted"
EU confidential = Classified with the mention of the classification level confidential " EU Confidential "
EU secret = Classified with the mention of the classification level secret "EU Secret "

Milestones

TABLE 2. MILESTONES							
Milestone no.	**Milestone name**	**Work package no**	**Lead beneficiary**	**Delivery date from Annex I dd/mm/yyyy**	**Achieved Yes/No**	**Actual / Forecast achievement date dd/mm/yyyy**	**Comments**
Ms1.1	Application requirements defined	**1**	**IFAT**	**31/12/2012**	**YES**	**31/12/2012**	
Ms1.2	First system architecture	**1**	**IFAT**	**30/06/2013**	**YES**	**30/06/2013**	
Ms2.1	Architecture analysis and evaluation	**2**	**UPM**	**30/09/2013**	**YES**	**30/09/2013**	
Ms2.2	Analysis and optimisation of integrated passives	**2**	**UPM**	**30/09/2013**	**YES**	**30/09/2013**	