Platform for European CMOS Imagers

ICT-284487

Space critical technologies
Small or medium-scale focused research project

Final public report

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PP	Restricted to other programme participants (including the Commission Services	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

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Abbreviations

ADC	Analog to Digital
ARC	Antireflective coating
CDS	Correlated double Sampling
CIS	CMOS Image Sensor
CMP	Chemical Mechanical Polishing
DSiE	Deep Si Etching
EPI	Epitaxial
FPA	Focal Plane Array
FS	Frontside
IC	Integrated Circuit
IMD	Inter Metal Dielectric
KOM	Kick-Off Meeting
LTA	Laser Thermal Annealing
MBI	Monolithic Back Side (Module)
PDK	Process Design Kit
PMD	Pre Metal Dielectric
PPD	Pinned-Photodiode
QE	Quantum Efficiency
RTD	Research and Technological Development
SAM	Scanning Acoustic Microscopy
STI	Shallow Trench Isolation
TTV	Total Thickness Variation
WP	Work Package
XT	Crosstalk

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Project Objectives

The main goal of this project is the creation of a European supply chain for state-of-the art CMOS image sensors (CIS). As identified by both ESA and the EC, there is a need for such a supply chain for CMOS imagers for space applications which uses solely European (and ITAR-free) sources. This goal will be realized using the proposed consortium as all partners have excellent know-how and track record in the expertise fields required.

A second goal of the project is to push the performance of CMOS imagers and match the requirements for the (typically very demanding) space applications. Hence large area (much larger than commercial imagers) high sensitivity imagers will be developed using stitching technology and backside thinning. A key element here is the backside passivation process using laser annealing.

The project used a 3 phase approach: first typical space imagers requirements will be collected. Based on these requirements, then the imager platform will be built, i.e. all necessary blocks will be brought to maturity. In the last phase this platform will be validated by the realization and qualification of a state-of-the-art imager.

The outcome of this project is a CMOS imager design and manufacturing platform that can be used by the space industry (ESA, CNES, satellite manufacturers, ...) for their future space imager needs. However, it will as well serve (and will be open for) other high-end imager needs in e.g. medical or security applications.

Partners

In order to reach the goals of the project, a complete and competent consortium has been set-up:

- **SELEX ES (previously SELEX GALILEO)** is a prime space equipment builder and has therefore extensive experience in handling space requirements for imagers. Also SELEX Galileo has the right competences to perform imager characterization and space qualification.
- **Imec** has a known track record in development of both CMOS electronics as well as imagers, and is expanding its activities towards dedicated development on demand and small volume production of high-end devices (such as imagers) in its 'CMORE' activities..
- **TNO** has relevant experience in optical coatings and filters for space use, as they are involved in multiple space projects.
- **Excico (now LASSE)** is specialized in the manufacturing of laser annealing equipment, which is key to the realization of high performance backside illuminated imagers

Specifications Definition

For EUROCIS detector requirements definition, the following route was pursued :

- To survey the actual space detector market
- To identify the detector types according to the possible space missions
- To identify the possible future missions
- To select one or more possible missions and select the detector type
- To prepare the first version of the specification
- To open the discussion on the finalization of the requirements

The results of the above investigations and discussions lead to the issue of EUROCIS demonstrator imager requirement specification, which served as input for EUROCIS chip design performed by IMEC.

Table 1 General system Specifications for the EUROCIS IC

Name	Min	Typ	Max	Unit	Comment
Number of rows	1024	2048			See section 8.1 for a more detailed explanation.
Number of columns	1024	2048			See section 8.1 for a more detailed explanation.
Frame Rate	---	20	t.b.d.	f.p.s.	Accepted target after discussion with ESA (Original spec was 300.)
Integration time	1		1000	ms	
Power consumption			1.5	W	At maximum frame rate
Temperature rage	-40	20	85	deg C	In vacuum
FPN			500	e-	Calculated at 1 sigma over the whole array. Corresponds to 2.2 mV_{rms}. Cannot be ensured as statistical models are not available. Best effort.
PRNU			±3	%	Of the mean, 1 sigma, averaged over the waveband.
Temporal noise			50	e-	For a 250ke- FWC. In dark illumination condition at 1σ, calculated rms, over the whole array.
Linearity			±2	%	See [11] for detailed explanation of this specification.
Shutter	Rolling shutter				Accepted target after discussion with ESA (Original spec was snapshot)
Programmability	Windowing, Integration time				Done at "control and data acquisition".
Windowing	In steps of 8 rows				Spec not defined in [11].
Detector temperature	Built-in sensor				Measurement done off-chip.
Pixel pitch		14		µm	
Pixel pitch tolerance		±1		µm	
Full Well Charge (FWC)			250k	e-	Trade-off with pixel area
Spectral range	400		1000	nm	
Global QE	80			%	This is the target for 400-800nm
MTF		50		%	
Image lag			0.1	%	
Average Dark Current			1500	e-/s	At 25 degrees C over all pixels.

Demonstrator imager design

The demonstrator imager design included the finalization of the electronic component models and the process design kit. Based on those results, the analog and digital electronics design and the pixel design took place and the corresponding masks were taped-out. Milestone2 at M14 defines the conclusion of the imager platform development.

During the first year of the project the PDK (process design kit) was finalized. The PDK consists of:

- the transistor models (typically SPICE simulation models),
- the standard cell library,
- the design rules and,
- the layout rules.

Pixel design

The choice was made to implement a 4T-PPD pixel (4 transistor pinned photodiode). 4T-PPD pixels are today widely used in industry, especially in consumer applications. By separating the light-to-charge conversion (& collection) region (PPD) from the charge-to-voltage conversion node (FD), both can be optimized individually for their specific purpose. Both nodes are connected via a 4th pixel transistor called transfer gate. Immediately prior to transfer and read-out of the signal, the FD node is reset and the reset signal read. Both reset and signal are from the same integration time (thus correlated) and converted on the FD node with minimal delay in time (lowering low-frequency noise).

Read-out electronics design

A conceptual architecture for the EUROCIS chip was identified.

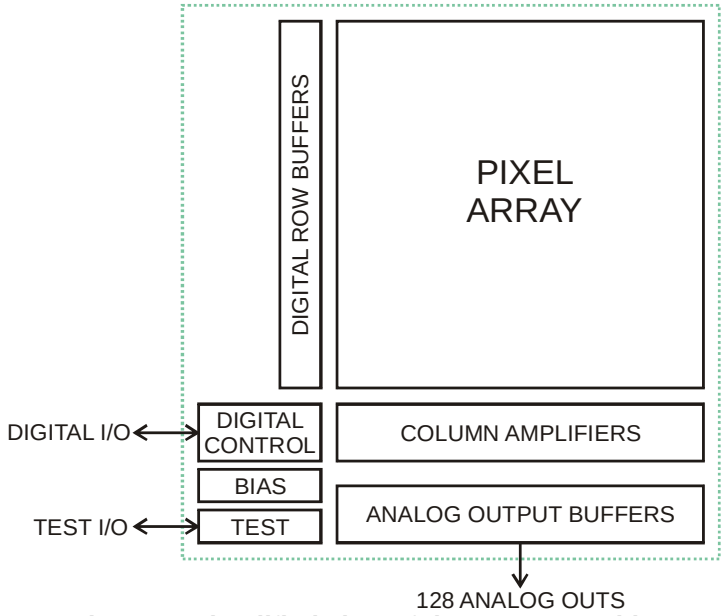


Figure 1: Simplified view of the EUROCIS chip

A “digital control” block buffers the control signals to the row buffers, the column amplifiers and the analog output buffers. The “bias” block generates the bias currents and voltages needed for the analog readout. The “block” includes some circuitry to perform some basic tests and to access internal digital and analog signals for debugging purposes. The “digital row buffers” control the operation of the pixels during integration and readout. The “column amplifiers” read the pixel values row by row and perform correlated double sampling (CDS) to reduce the noise. The “pixel array” consists of an array of 2048 rows by 2048 columns of pixels. The “analog output buffers” buffer and multiplex the output of the column amplifiers to 128 analog output pins. This means that each sixteen columns are multiplexed to one output buffer.

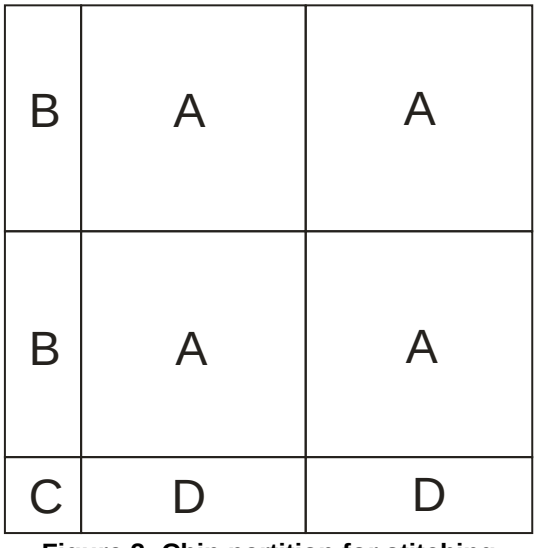


Figure 2: Chip partition for stitching

According to the specifications, the pixel array consists of 2048 x 2048 pixels, of 14 µm x 14 µm each. That means that the pixel array would occupy an area of approximately 30 mm by 30 mm. This is not possible to realize in a single reticle with the photolithographic tools. This means that the chip will be split into different sections that will be joined by stitching to realize the complete chip. Figure 2 shows the simplified partition of the chip for stitching.
The mask design of EUROCIS chip was more complex that the standard process and required experienced designers and application of time consuming techniques because of the stitching requirements.

CIS Fabrication

First the imager process platform was finalized. In the second phase (validation) the actual imager manufacturing took place.

Front side CMOS imager platform

Setting up a CIS (CMOS image sensor) process required several additions and/or modifications as compared to a standard CMOS process. Specifically for the pixel, today's industry standard makes use of a so called 4T-PPD arrangement. Every pixel requires a low dark current PPD (pinned photodiode) in addition to 4 special transistors. In order to maximize photosensitive and charge collection area, 3 out of these 4 transistors can potentially be shared between 2 to 4 pixels. Each of these transistors needs to be optimized qua dimensions and process conditions for its specific task and operating condition. Also the PPD needs to be optimized to achieve, in its reset condition, a state of full depletion at a designed-for pinning voltage.
The full CMOS image sensor (CIS) module was enabled in the standard 0.13 um imec technology using 200 mm wafers, including a MIM module, dual gate transistors (1.2V and 3.3 V).

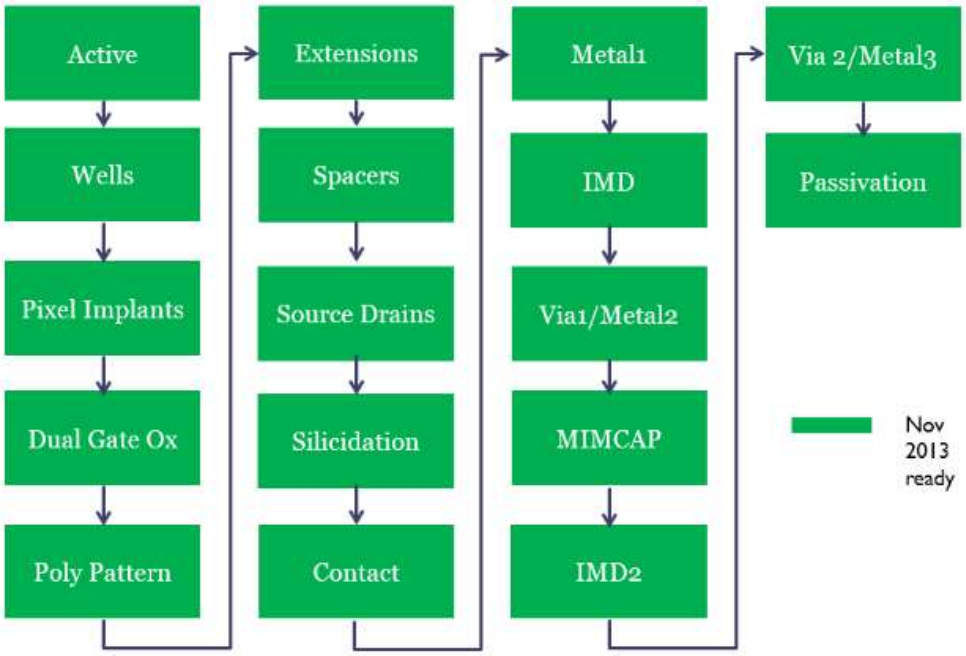


Fig. 3: summary of the CIS/CMOS 0.13 um imec process modules

Back side CMOS imager platform

Concerning backside illumination, although imec has been working for some years on backside illuminated imagers, the approach was based on hybridization rather than on a monolithic backside illuminated integration. Therefore the technology development of a monolithic backside illuminated platform was necessary.

The three extra MBI (monolithic backside illumination) modules are the bonding, the thinning & passivation and the opening of the bond pads.

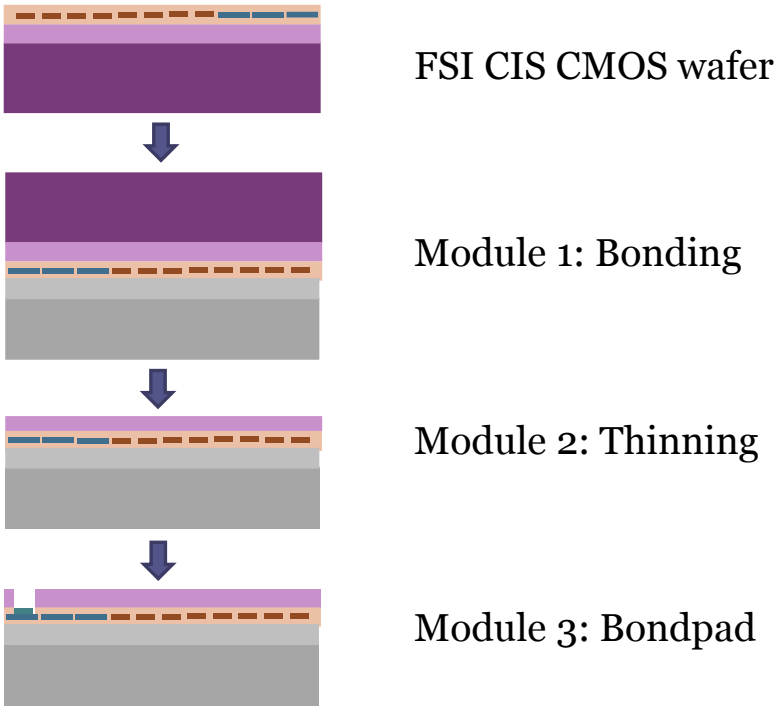


Figure 4: Backside CIS process flow modules

One of the most critical modules in the development of backside imagers is the choice of the appropriate Si substrate wafers. The structure of the epitaxial layers (thickness, dopant concentration, profile) needs to be specifically designed according to the required specifications of the final product.
During the platform development period regarding the module of wafer bonding, several test runs have been performed. At first, blanket wafers with different oxide types were used as testing material. The oxide types were thermal oxide, PECVD, O3TEOS or native oxide. The test goal was to identify whether bonding of wafers with similar oxide type or with native oxide is better. The results of the bonding were evaluated by direct inspection using scanning acoustic microscopy (SAM). Figure 5 shows the result of the bonding optimization. Apart from very limited regions of defects, the wafers are uniformly bonded to the carrier.
Imec studied various types of methods for the bond pad opening from the back. The selected process flow is based on a deep Si Etching of the bondpad cavity and re-metalllization using an Aluminium later. The result is a bondpad that is fully wire bond compatible.

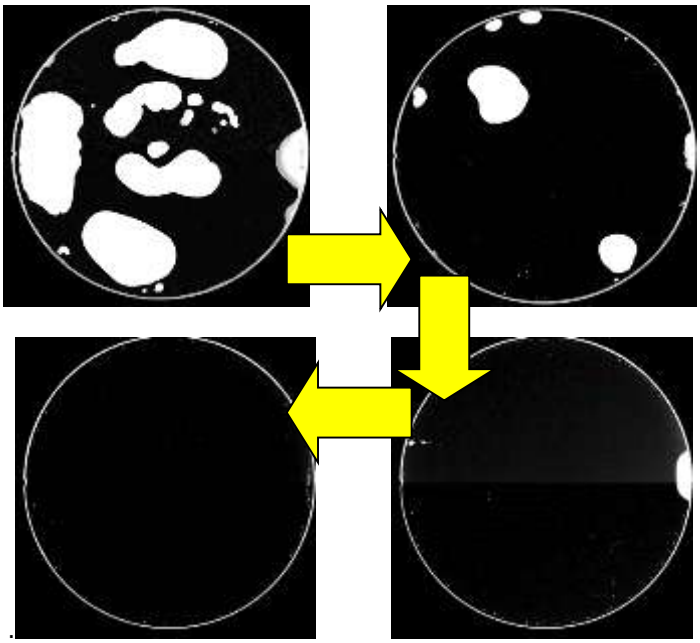


Figure 5: Optimization of the wafer-to-wafer bonding process

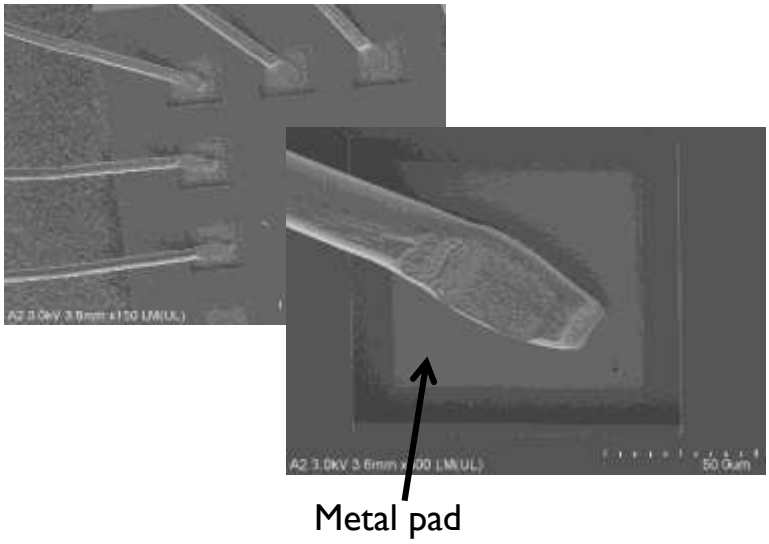


Figure 6: Scanning electron microscopy picture of a BSI bond pad.

For the platformization of the Backside process modules, a specific test vehicle has been designed, named “Kolibrie”. This consists of various PN photodiodes, of different sizes. In Figure 7 is presented a fully processed backside wafer with the Kolibre photodiodes and the packaged die which is used for the measurements of e.g. quantum efficiency (QE).

Using the Kolibrie design, all the 3 backside modules have been optimized and reached a level of maturity that enables them to be applied in the fabrication of the EUROCIS final imager and future BSI imagers.

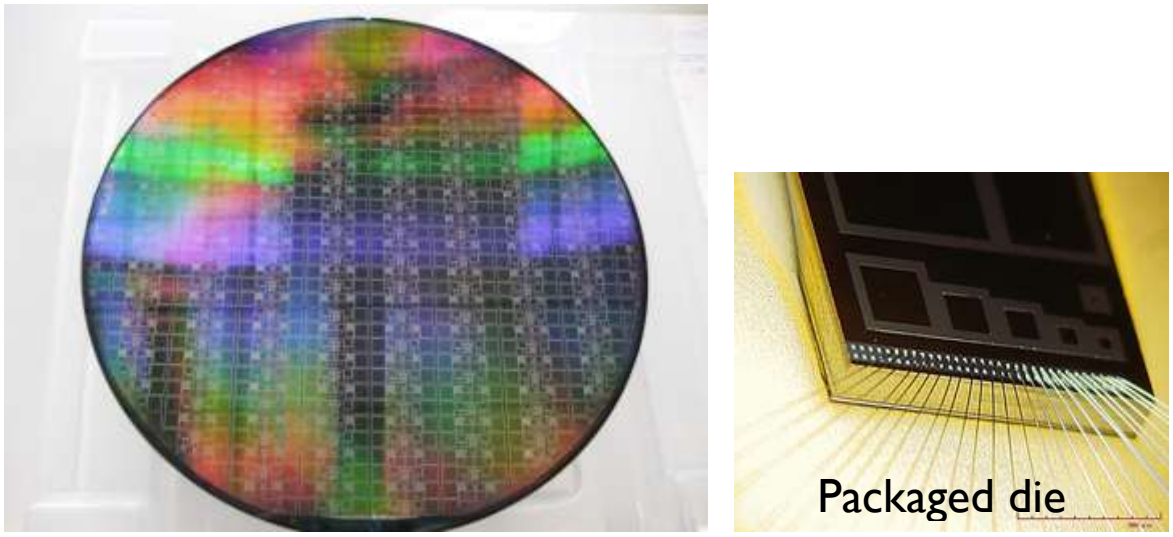


Figure 7: Backside thinned wafer with the Kolibrie test vehicle design (left) and packaged single die (right)

Regarding the backside passivation, numerous experiments have been performed using the Kolibrie wafers which were targeting the evaluation of different implantations and laser annealing conditions on the performance of the photodiodes (measurements of dark current and quantum efficiency). In figure 8 are shown the measurements of the quantum efficiency of Kolibrie packaged samples, coming from different wafers. The wafers were processed with different implantation (at imec) and laser annealing conditions at Excico. It is evident that there is one laser condition identified to bring an increase of 10% in the blue QE response of the photodiodes.

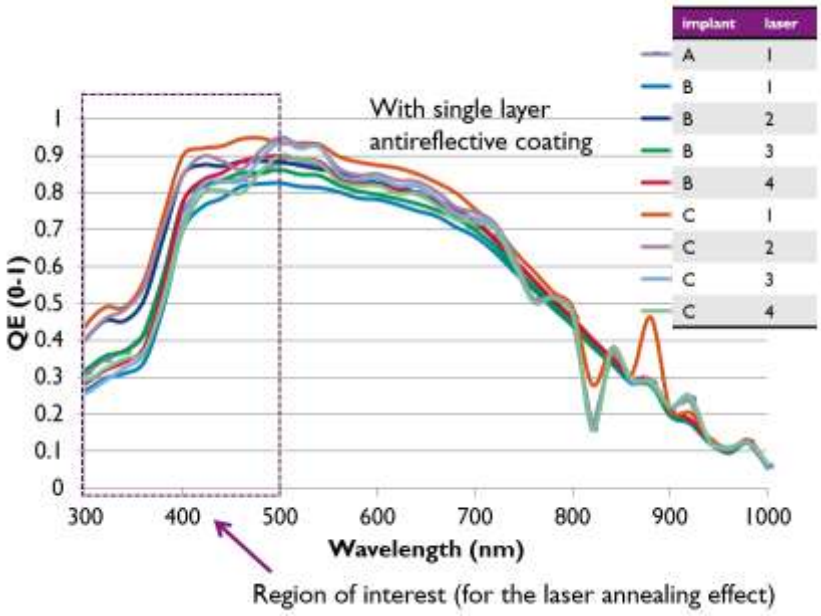


Figure 8: Quantum efficiency measured on the Kolibrie photodiodes, comparing different implantation and laser annealing conditions

Finally, regarding the ARC process step, Kolibrie samples have been sent to TNO and were deposited with different ARC layers.

CMOS Imager Demonstrator FSI process

Two lots of the EuroCIS imager demonstrator have been processed. Unfortunately, both lots suffered from unexpected process issues: in the first lot the low voltage NMOS transistors featured a large gate leakage. In the second lot the combination of process marginality and design (i.e. the absence of dummies in a part of the design) lead to a short at metal 3 level.
The conclusions and lessons learned from the process are:
• Separate test structures should have been placed to test the effect of dummies on the MiM capacitors to avoid needing modifications in the actual imager.
• Additional design for test pads and circuits should have been placed for the digital pixel control logic.

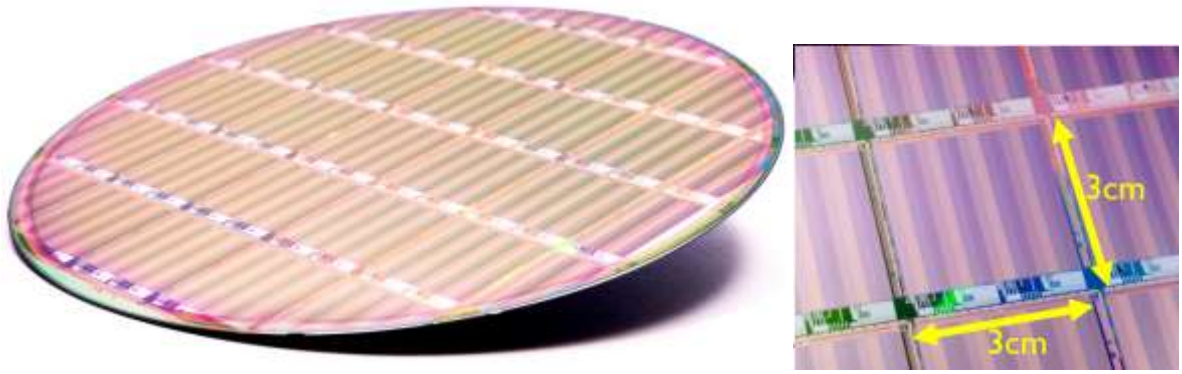


Figure 9: The EUROCIS wafer with the frontside process finished (left) and zoom-in on one chip (right)

CMOS Imager Demonstrator BSI process

Both lots have finished the backside processing, including laser annealing at Excico and ARC depostion at TNO. A backside wafer and the zoom-in on one chip is shown in **Error! Reference source not found.**. The devices have been packaged using a chip-on-board (COB) approach.

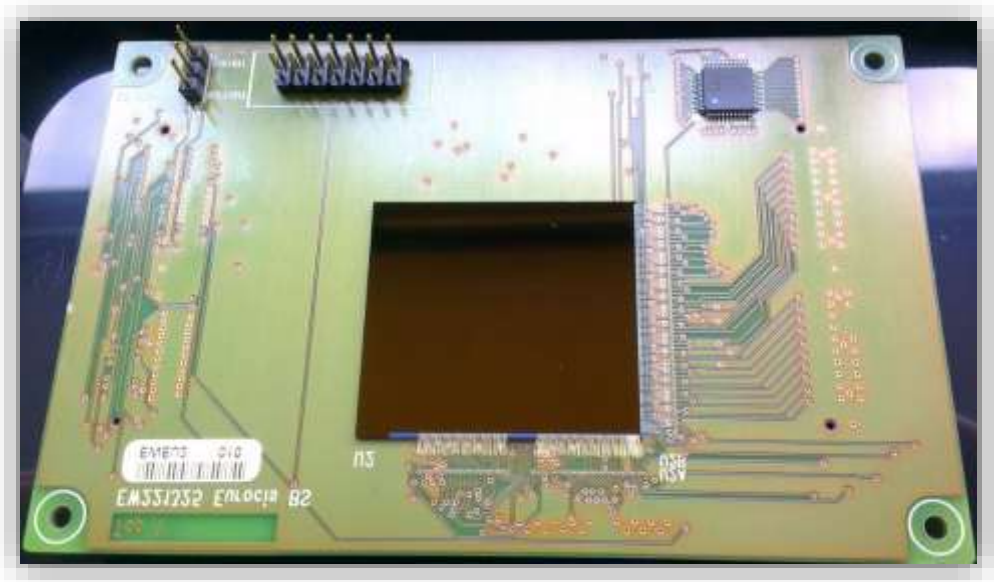


Figure 10 Packaged backside EUROCIS chip

Laser Annealing

The Backside CMOS Imaging sensor Market is a growing Market. Before EuroCIS project, LASSE equipment and process was optimized for small area imagers. But specialty sensors as larger imagers and UV detectors represent a very attractive market (DSC, SLR, scientific, industrial, security, aerospace, automotive,…) and LASSE was not able to access to these markets. The project has helped enabling LASSE to access to this high added value market segment. The knowledge on process integration acquired through the project will also be valued for other markets accessible to LASSE.

In order to solve LTA limitation and extend LASSE capability to anneal larger sensor as EuroCIS sensors, two main solutions has been investigated

The first path is a new laser scanning approach able to cover larger die size independently from the sensor dimension. This new approach consists in the optimization of the stitching (or overlap rate) between smaller shots to reduce the non-uniformity induced by the shot border to an acceptable level. The early results on blanket wafers were promising in this regard using 90% overlap rate. This solution was retained as the initial results were confirmed.

The second is a hardware upgrade of the previous tool able to cover the full die with a single irradiation. This upgrade consists in two main challenges: A new optic system enlarging the previous beam area from 20 x 20 mm² to the 33 x 33 mm² required for EuroCIS sensor and an improvement of laser energy on the wafer from ~ 10 Joules available before, to 13,5-18 Joules (1.5-2 J/cm²) required for EuroCIS sensor.
A detailed conceptual study has been performed to assess and compare multiple technical paths to achieve a larger beam size than the current 20x20mm². Several optical designs have been modeled using Zemax, in particular 23x23mm², 28.3x28.3mm² and 33x33mm². Each design has an increased complexity compared to the current system but maintains high optical performance. The new optic system for larger beam size is on LASSE roadmap and will be implemented in the industrial tool.
Concerning the energy limitation, three paths are investigated in parallel. The first path is optimizing the non-melt anneal (or solid phase anneal), which requires less energy and an increased number of shots per location. The early results show that sufficient activation could be achieved with 10 shots at 1.4J/cm². Tests at lower energy density and increased number of shots are yet to be performed. The second path is to improve the coupling between the laser light and the silicon using an appropriate coating. The early results using thermal oxide or PVD high-k material are yet to be fully interpreted, although a reduction of the required energy by a factor of 2 was successfully achieved. Alternative deposition methods and optimization of surface preparation are yet to be evaluated. The third is increasing the laser output energy through a hardware upgrade. The first prototype of a new generation of high voltage system based on a solid state switch and a magnetic compression modulator has been developed, assembled and tested on a reduced scale laser. This is a key enabler for future increase of the laser energy. In parallel, a new gas circulation loop enabling higher repetition rate of the laser has been designed and first prototype is now functional.

In the project the different solutions has been explored and laser anneal step has been tested in several process flow solutions. Advantages and issues have been analyzed for the different flow and the final process has been identified. The performances of the devices have been studied as a function of the laser annealing conditions. The conditions that maximize the final performances of EUROCIS devices have been identified in terms of laser beam size, ED, number of pulse and overlap. The new laser scanning approach in sub-melting annealing conditions has been retained after comparison of different laser condition on blanket and test vehicle.

The new capabilities have already been helping Lasse to have a better position in the market of large sensors where request has increased toward such applications (APS-C and Full frame sensors)Initial demos have been done with good results.

Optical post-process

The aim of this work package is to provide coatings to be applied in a CMOS image sensor demonstrator. Several coatings have been designed: a broadband anti-reflection coating (AR coating) for visible light and near infrared (400-1000nm) and a broadband AR coating for ultra-violet (200-400). Because of the mediocre performance of the later several coatings with a more narrow anti-reflection band have been designed as well. Additionally, AR coating for fused silica windows and a black absorber coating have been designed.
The impact of these coatings on a camera system consisting of a detector with a protective fused silica window has been calculated. The analysis shows that the sensitivity can be increased by 47% for the Vis/NIR range and by 115% for the UV range. Ghost reflections can be reduced by 95%. The black coating is expected to absorb close to 99% of incident light.
The Vis/NIR AR coating and a UV coating for 260-350nm have been manufactured and applied on a number imager dies. In addition to the optical performance two other aspects are important: avoiding coating of bond pads and preventing particle deposition on the dies. The ARC is applied after manufacture of the bond pads but prior to bonding. This means that the bond pads are opened during coating. Therefore, care has to be taken to avoid coating of the bond pads. A strip around three sides of the perimeter of the die, including the bond pads, has been masked. The width of the masked strip is 0.9mm. After coating a very sharp edge between the coated and non-coated are of the die was observed.
During coating deposition, the dies were protected from particles in the deposition system. Experiments showed that handling of the dies did not add particles with a size larger that 1µm to the surface. Up to 40 1µm particles per square centimetre were generated by the deposition process itself. After optimisation of the process, this number was 20/cm^2. Recommendation for further reduction of particulate contamination have been made.

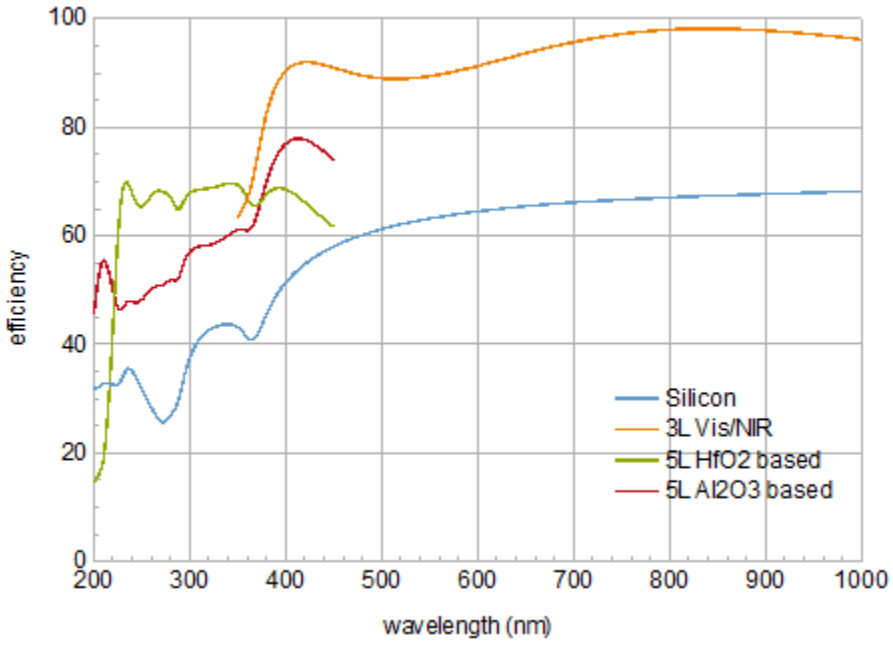


Figure 31: efficiency of three broadband ARC for Si: a 3 layer Vis/NIR coating (orange), five layers UV coatings based on HfO2 (green) and Al2O3 (red), compared to the performance of uncoated silicon (blue)

CIS characterization

Selex ES prepared the test jig to build the characterization set up. The set up is mainly composed by an Electrical Ground Support Equipment (EGSE) and by an Optical Ground Support Equipment (OGSE).
EGSE function is to provide power supplies and timing digital signals to the detector under test as well as to read and store the information provided by the detector analog outputs. The EGSE is composed by several PXI modules (from National Instruments) and by an electronic board (so called adapter board) for signal routing and bias currents generation. EGSE software was developed in such a way that 3 functional modes and 5 panels for detector management can be selected.
The OGSE function is to provide optical stimulus to the unit under test through various sources, depending on the parameters that it is needed to measure.
For a complete detector characterization, 6 set up different types were individuated and built in Selex ES facilities (see Figure 2 for an overview of set up).

Figure 12: EUROCIS test set up overview

The EGSE and OGSE were tested to verify their functionality and to validate the design.
EGSE tests consisted of power supply and bias lines verification as well as digital lines and analog channels verification. Analog channels verification consisted on providing an external electrical stimulus to the EGSE (through Adapter board) simulating the output coming from the detector: the test is considered successful, as the EGSE output resulted the one expected (vertical band visualized on the monitor in correspondence of the stimulated analog channel, see Figure 3).

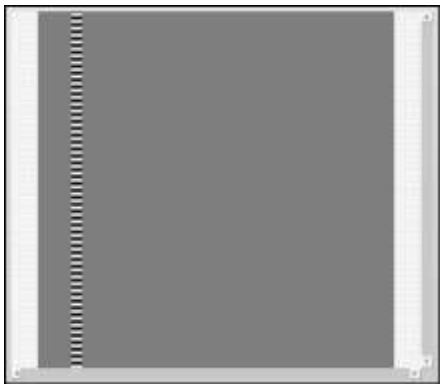


Figure 13: Analog channel 4 image acquisition

Vibration test was performed on a mechanically representative sample provided by IMEC, using SES internal vibration facilities: test was aimed mainly to evaluate wire bonds resistance to vibration. Two vibrations level (20g,30g) with initial, intermediate and final visual inspection in clean room was performed. Test was successfully complete: no broken wire bonding was noticed during each visual inspection step.

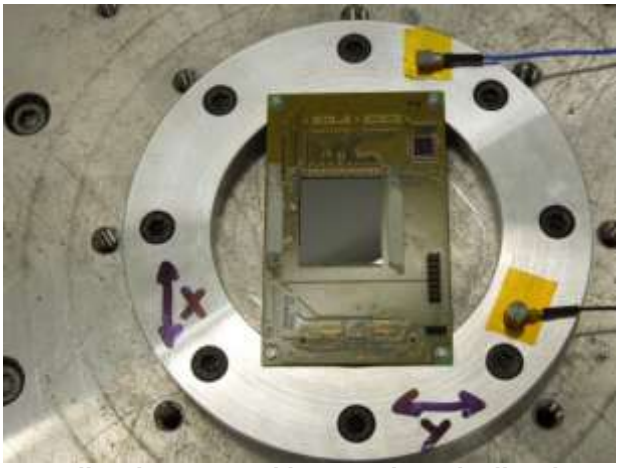


Figure 14: Vibration set up (detector board vibration test jig)

Imager device samples from the 2 lots processed were characterized. We can summarize the results from the measurements of the first lot samples:

- There is a known problem with the nMOS thin oxide devices, measured in the control devices.
- These devices are used in the digital logic which controls the pixels and the column selection.
- DC and bias measurements, as well as on the analog test structures show that the thick oxide devices and the circuits built with them work as expected.
- The digital test outputs do not toggle as expected from simulations, but this is consistent with problems in the digital logic.
- The analog outputs do not show a consistent behavior, but this is consistent with an unknown state of the pixels (due to unknown state of their control logic) and of the column selection.

The results of the measurements of the second lot samples can be summarized as:

- There is a clear short in the bias line of the column CDS amplifiers. This is easy to see from the DC measurements.
- The digital test outputs do not behave as expected (they seem to be floating).
- The analog test structures do not work as expected. A short only on the column bias cannot be the only responsible for this.
- The analog outputs behave a bit more consistently than in the first lot, but not as expected (i.e. no reaction to control signals or pixel illumination.
- Investigation on the samples shows that the lack of metal dummy structures in part of the circuitry caused problems with the CMP process which in turn could easily lead to the short een in the column bias and possibly other issues in the column and output buffer areas.

Dissemination and exploitation

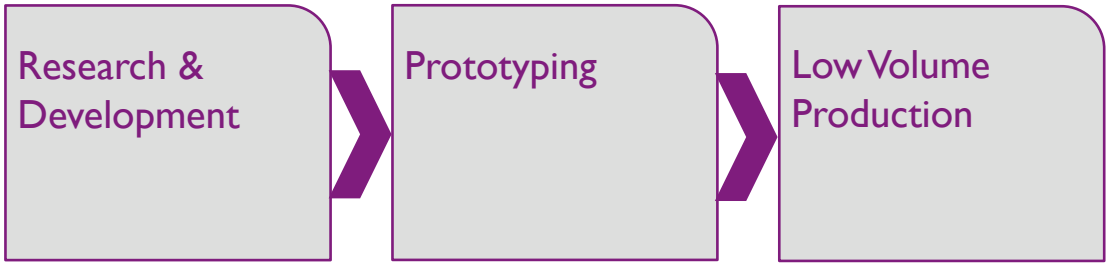
Imec presented a paper on the “Evaluation of backside passivation using laser annealing in backside illuminated image sensors” at the Workshop on “CMOS Image Sensors for High Performance Applications” organized by CNES in Toulouse, Nov. 2013

The submission of ‘A platform for European CMOS image sensors for space applications’ with first author K. Minoglou and co-authors from the complete EuroCIS consortium, was accepted for oral presentation and a proceedings article at ICOS 2014 (International Conference on Space Optics) in Tenerife, October 2014. After the presentation, there were many questions and interest from different attendees.

As the EuroCIS concept breaks open the design space of imaging technology, a number of new high-end imagers will become possible. EuroCIS does offer additional degrees of freedom in imager design (i.e. large area and stitching) which make it a definite enabling technology for existing and new applications.

Until recently imagers (mainly for visible light detection) used CCD technologies, which are still available in Europe. However, following the trend in consumer imagers, also space imaging devices are using CMOS technology, because e.g. of system integration advantages. Typically these high-end CMOS imagers are being designed in Europe, using in 0.18 um CMOS/CIS technology. However, the fabrication is typically outsourced to non-European foundries (such as TowerJazz Israel). Post-processing imager for BSI was not available as a service in Europe at all.

Exploitation by imec



Based on its state-of-the-art infrastructure and process technology capabilities (see above) on the one hand, as well as a whole range of additional capabilities and expertise (such as advanced packaging and heterogeneous integration technologies, reliability and failure analysis, modeling and design know-how for digital, analog, RF and MEMS) on the other hand, IMEC is strengthening its offering of development-on-demand projects leading to demonstration of concepts through prototyping and small scale production.

Recent evolutions, both technical and market evolutions, indicate that a sustainable IC production basis in Europe could be at risk which would jeopardize the policy goal of a European independence for critical space technologies. IMEC proposes an answer to these risks by offering a European based, independent, flexible and sustainable production facility to ESA and the space industry.

Exploitation by SELEX ES (formerly Selex Galileo)

SELEX Galileo, as an electro-optical instrument manufacturing company, will benefit from this collaboration because the output of this activity will be an imager platform with many possible applications within a number of space projects/satellites. This will simplify the satellite design and will ease the independence from export licensing constraints for the most critical element (i.e. the imager).

Exploitation by LASSE (formerly Excico)

The upgrade realized on the present LTA equipment will allow Excico to access and penetrate other markets where a larger area laser beam is required. As a unique already patented key selling point of our present product, it will reinforce this asset and strengthen the positioning of the company on the present and future markets of Excico.

During the course of the project, Excico has been acquired by DNS and is now named LASSE,; as a Division , Lasse will continue developing and manufacturing the Tools in Gennevilliers (France) with additional support from DNS.
This will allow Lasse to develop the company and product much faster and address the time to market requirements.

Exploitation by TNO

It's a part of the mission of TNO to strengthen the innovative power of companies. In EuroCIS TNO is contributing to the arrangement of an (independent) European manufacturing line of imagers, not only qualified for space applications but also for medical and other industrial applications.

Conclusions

The aim of the EuroCIS project was ambitious: establish a European platform for large area backside illuminated CMOS imagers and design, process and characterize an imager demonstrator.

Unfortunately the goal of a demonstrator has not been achieved. The unforeseen and extra (second) lot that was completely processed, but didn't yield any operational imager devices, and the project didn't allow for a re-design and re-process both in terms of funding and of timing.

Nevertheless there are a number of lessons learned: the process design kit (PDK) was updated with new design rules that will minimize the future failure risk that was observed with the Eurocis devices. Also future designs should be made with a test strategy in mind, so that they are easier to de-bug.

However, the main result of the EuroCIS project iss the successful setup of a European platform for large area backside illuminated imagers. All the necessary building blocks have been established: stitching technology, the complete backside illumination post-process module including laser annealing, and different anti-reflection coating options for both visible and near- ultraviolet light. The optical performance of this platform has been demonstrated using test devices.

The relevance of this platform cannot be underestimated. Already at the time of writing, several projects for both ESA, EC and industrial use with need backside illuminated imagers and/or stitching are initiated, and many others will follow, both for space and non-space application.