FRONT PAGE

PROJECT FINAL REPORT

Grant Agreement number: 604169

Project acronym: SiNERGY

Project title: Silicon friendly materials and device solutions for microenergy applications

Funding Scheme: Small

Period covered: from *1 November 2013* to *31 October 2016*

Name of the scientific representative of the project's co-ordinator[1], Title and Organisation:

Dr. Luis Fonseca, IMB-CNM (CSIC)

Tel: +34935947700 (ext 2104)

Fax: +34935800267

E-mail: luis.fonseca@imb-cnm.csic.es

Project website[2] address: www.SiNERGY-project.eu

[1] Usually the contact person of the coordinator as specified in Art. 8.1. of the Grant Agreement.

[2] The home page of the website should contain the generic European flag and the FP7 logo which are available in electronic format at the Europa website (logo of the European flag: http://europa.eu/abc/symbols/emblem/index_en.htm logo of the 7th FP: http://ec.europa.eu/research/fp7/index_en.cfm?pg=logos). The area of activity of the project should also be mentioned.

4.1 Final publishable summary report

Energy autonomy keeps being one of the most desired enabling functionalities in the context of off-grid applications, such as continuous monitoring scenarios and distributed intelligence paradigms (Internet of Things, Trillion Sensors). SiNERGY has focused on silicon and silicon friendly materials and technologies to explore energy harvesting and storage concepts for powering microsensors nodes. Harvesting energy, tapping into environmentally available sources such as heat and vibrations, may be a good powering solution in man-made scenarios applications. 10-100µW/cm^2 power densities seem appropriate for many such applications. Coupling those harvester devices to secondary batteries to buffer enough energy to account for the power demand peaks required by wireless nodes would be an enabling energy autonomy solution.

SiNERGY has selected relevant examples of power microgeneration and storage (thermoelectric generators, mechanical harvesters and microstructured batteries) pushing them further into their performance and development maturity. Emphasis has been placed on thin films and nanostructured materials and their integration into mechanically and thermally optimized microstructures. For bringing the eventual solutions closer to an exploitable phase, silicon technology compatible materials have been considered. Silicon micro and nanotechnologies provide an enabling path to miniaturization, 3D architectures (improved energy densities), mass production with economy of scale, and the possibility of easy integration with other microchip based devices (sensors & actuators, power management circuits, communication units...)

Silicon friendly materials and device solutions for thermoelectric harvesting. Thermoelectric microharvesters able to convert heat flows into small, yet high added value, amounts of electric power have been pursued. The activity has focused in successfully integrating silicon nanowires as low thermal conductivity material into devices with optimized thermal and electric design. Both, bottom-up and top-down approaches for nano-objects integration have been explored.

Silicon friendly materials and device solutions for mechanical energy harvesting. Electrostatic and piezoelectric harvesters have been explored to convert small vibrations into a useful power. In the first case, an optimized silicon based electret material has been integrated in a robust laterally moving microstructure. In the second, the integration in vertically moving microcantilevers of a piezoelectric composite based on ZnO nano-objects has been attempted, and a hybrid fabrication approach combining silicon and printing technology has been shown promising.

Silicon friendly materials and device solutions for solid-state microbatteries. Material and interface optimization (from a fast charge/discharge perspective) has led to the fabrication of a functional thin-film planar microbattery for on-package energy storage. Translation of this knowledge into 3D microbatteries, fully compatible with Si technology, for increased capacity and power has been attempted. Failure to identify a good solid electrolyte has prevented full success, but a hybrid 3D battery has been assembled.

Integration feasibility. Even though SiNERGY focuses in materials and technologies, attention has been paid to real applications. As a consequence, system integration issues have been tackled at different levels for the above microenergy devices. A gas fryer scenario has been explored for the deployment of thermal harvesters, piezoelectric devices have shown appropriate for powering remote nodes at useful duty cycles (e.g. for preventive maintenance), and the electrostatic harvester has been shown functional in a Tire Pressure Monitoring application.

Summary description: SiNERGY in a nutshell

The project addresses the development of **energy harvesting and storage devices** suitable for solving energy autonomy issues of unwired powered devices working in low-power and/or pulsed regimes that will be required in continuous monitoring scenarios. The combination of an energy harvester with a small-sized rechargeable battery is the best universal approach to enable energy autonomy in those applications.

The microenergy elements of interest for SiNERGY are then **harvesters** and **solid-state batteries**. In the case of harvesting, **thermoelectric** and **mechanical** harvesters have been considered given that temperature **differences** and **vibrations** are the most common environmental energy sources in manmade scenarios. The focus of the proposal is placed on the **microdomain** to obtain small size devices with high energy density features, and on the **silicon technology friendliness** of materials (and approaches) to assure the eventual manufacturability, integration and cost effectiveness of the related devices/solutions.

When resorting to silicon technologies, the material issue cannot be dissociated from the architectural issue, which unavoidably brings the focus closer to the device level. This is an added value because the development and exploitation of the devices is moved one step further into maturity. For this reason, not only different low dimensional **material options** (crystalline and polycrystalline Si nanowires, Si-Ge nanowires, ZnO nanoobjects, and oxide, nitride and metal thin-films) are considered, but also different **technological fabrication approaches** (bottom-up or top-down approaches), and **device architectural alternatives** (micromachined thermally isolated platforms, micromachined in-plane or out-of-plane movable platforms).

The high volume, cost-effective and sustainable fabrication enabled by micro and nanotechnologies will support the advent of energy autonomy solutions required by the eventual success of numerous applications. Three of these applications have considered as a frame of reference for our developments: **tire pressure monitoring systems**, **smart cooking appliances** (as an example of machine condition monitoring), and generic **preventive maintenance**. As a test case, each presents a different harvesting scenario: vibration in the first, hot surfaces in the second, both in the third (always it will be used for vibrations in our case) and a different motivation for going into the microdomain (physical space constraints in the first and the second and multiplication of nodes in the third case).

SiNERGY context (1): microenergy *vs* macroenergy

We are talking here of **microenergy**, tiny bits of energy and a few microwatts of power, not of the 10^{16} TW that yearly are produced worldwide. Society of today needs **abundant** energy to power our cars, factories and homes, but society of tomorrow will also need **abundantly distributed** energy to power the billions of sensors that will be deployed in the Internet of Things to come.

We are not referring either to 'microgrids' (which is an abuse of language for designing locally redistributed macro energy sources). We use the term micro to really refer to **miniaturized cm-size devices**. Silicon technologies are the techniques of choice in SiNERGY. Other large volume, cost effective technologies exists that are also miniaturization-prone to some extent, such as lamination or printing technologies. They even excel over Si Technologies when producing cheap large area devices or flexible devices, but Silicon technologies are the ones better situated to obtain devices with **internal micro and nanofeatures**. If the Internet of Thing is going to bring us billions of sensors, they will be probably small, and, consequently, the harvesters/batteries supporting their energy needs should also be small. However, the only way of capturing enough energy from low density harvesting sources with such small devices is that those devices have high internal features density (for instance **3D internal architectures** where to integrate large surface-to-volume ratio nanomaterials if need be). Silicon technologies are also the only ones producing (by means of micromachining) small scale **free surfaces and volumes** that allow those devices to effectively couple to environmental stimuli.

SiNERGY context (2): off-grid energy autonomy

As we know, **off-grid energy autonomy** is one of the most demanded functionalities since it enables a wide range of interesting disposable, portable and deployable applications. In all these cases, energy is usually provided by batteries. SiNERGY focuses in deployable solutions, where periodic battery recharge or replacement will be unpractical when faced with such a large number of devices.

Energy harvesting, tapping onto environmental sources of energy, such as **vibrations or waste heat**, can be a way of directly powering the sensors, or keeping continuously charged an auxiliary battery that will be a pretty **universal energy autonomy solution**.

SiNERGY objectives

Thermoelectric harvester

Since waste heat is one of the most recurrent environmental energy sources, one of the harvesting options considered is the development of a thermal microharvester, which given the philosophy of SiNERGY will be attempted using silicon technology friendly materials and architectures. High density features are needed to overcome the trade-off of silicon being an enabling technological material but a poor/modest thermoelectric material

The main objective, for this purpose, is:

- the integration of **silicon based nanowire** (NW) **arrays** as thermoelectric material into a **silicon micromachined structure**. This structure shall enable an internal thermal contrast to develop between two isolated silicon regions, which once bridged with the Si NWs, will be the basis of an **all-silicon microthermoelectric generator.**

Intermediate objectives for achieving this goal are then:

- Obtaining **high density** arrays of (arbitrarily) **long nanowires** at wafer level, considering different **bottom-up** and **top-down** synthesis/definition processes
- Obtaining a microstructured platform with **compact quasi three-dimensional features** with two distinct areas of thermal contrast, one in contact with the silicon bulk, the other in contact with a **microradiato**r to be integrated on top.
- Devising a **fabrication technological route** that makes compatible the integration of above three elements (Si NWs, microplatform, microradiator), and enable power output densities in the 10-100 $\mu W/cm^2$ range
- **Avoiding the use of extreme lithography / nanolithography** in the process sequence, thus decreasing the technological complexity and cost of the resulting devices and easing their large-scale replication
- Choosing an architectural arrangement in which the arbitrary long, high density nanowires arrays are integrated in the microstructure platform in a way that **good thermal and electrical connection is assured at no extra technological cost.**

Mechanical energy harvester

Another possibility of energy harvesting is using mechanical energy, e.g. vibrations. There are three main methods to convert mechanical energy into electrical energy: electromagnetic, piezoelectric, and electrostatic. For many small autonomous sensor systems, miniaturisation and cost effective manufacturability are important requirements. Silicon technology is the way to go to reach those requirements, but this rules out the use of electromagnetic transduction - It turns out to be virtually impossible to efficiently scale down and integrate pick-up coils and magnets into silicon technology.

Therefore, SiNERGY focuses in:

- Developing **electrostatic** as well as **piezoelectric** energy harvesters based on Silicon technology with high power output and good reliability.

Intermediate objectives to achieve these goals are:

Electrostatic energy harvester:

- Material development and optimisation for silicon-based **electrets** (the polarisation source for electrostatic energy harvesters).
- Integration schemes for these electrets, with high surface voltages and long charge retention times (10 years @100°C) into out-of-plane mass-spring MEMS platforms.
- Device optimisation with increasing capacitance variation and minimizing parasitic capacitance. The power output goal for the electrostatic energy harvester is 500 μW for $1cm^2$ area.
- Reliable devices with shock resistance up to 5000 G.

Piezoelectric energy harvester:

- Fabrication of out-of-plane cantilever type Silicon MEMS structures
- Adaptation of compatible MEMS processes for reliable synthesis and integration of piezoelectric ZnO nano-objects onto silicon microstructures

- Device design which optimizes the strain/stress of nano-objects under short displacement vibrations, in order to achieve power densities beyond 25 $\mu W/cm^2$

Solid State Li-ion microbatteries.

For the application of autonomous systems powered by harvesters, on-board energy storage devices are required to ensure a stable current supply and cover peak demands. In particular, lithium and lithium ion batteries (LIB) have the highest energy density of all known systems and thus represent the best choice for rechargeable batteries. Since liquid electrolyte based batteries present safety issues and limitations in size and design, pure solid state devices are gaining ground particularly for miniaturisation.

The main objective of this project is to develop high performing **thin-film all-solid-state lithium-ion microbatteries compatible with silicon technology**. In order to significantly increase the power density and capacity of the State of the Art microbatteries, a double approach based on **improving kinetics of ion transport at the interfaces and increasing the effective surface area** will be followed.

Two different architectures will be developed in order to face up the main goal of the project, namely:

- **Thin-film planar structures** to specifically implement strategies for improving ion transfer at the interfaces, i.e. current density, by multilayer deposition of all-based spinel microbatteries.
- **Three-dimensional geometries** to increase the current density, power capability and energy storage capacity by simply increasing the surface area.

In the planar configuration, performance will be the main target measured in form of *rate capability* (power) and *lifetime* (cyclability). In the 3D configuration, emphasis will be put on battery *capacity* (energy-density) and issues of *mechanical integrity* (reliability).

Intrinsically linked to the development of these two architectures, intermediate objectives of the project can be listed as follows:

- Deposition of **defect-free thin-film electrolytes** with high-enough ionic conductivity and reduced thickness (low internal resistance).
- Deposition of crystalline multilayers (cathode/electrolyte/anode) **all-based on the spinel** structure with **continuous and smooth interfaces**.
- Microfabrication of **high density three-dimensional structures based on dry etched Si pillars** fully compatible with silicon technology.
- Deposition of **high quality conformal electrolyte/electrode multilayers** (to be applied in 3D structured substrates)**.**

Main S&T results/foregrounds

Si NWs based micro thermal harvesters

Bottom-up approach

The bottom-up approach sketched in Figure 1 is based on the integration of arrays of Si NWs as active material in a previously fabricated Si microplatform able to endure the hard requirements of NWs growth process (high T). During SiNERGY project the efforts have been focused on the optimization of both elements, with the aim of increase the harvested power per unit area and accomplish the requirements foreseen for powering a wireless sensor node.

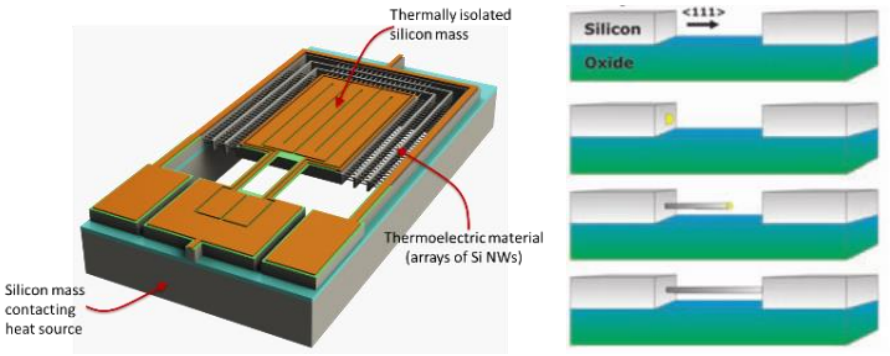


Figure 1: Left) Sketch of the bottom-up thermal harvesters, built on SOI substrates, namely a microstructure able to sustain a spatial temperature difference. Right) Bottom-up Si NWs are integrated as thermoelectric material using Au nanoparticles as seeds for the VLS method.

Si NWs optimization

The first goal in Si NWs development was the reduction of the high temperature required for the growth process, so as to limit the suffering and potential breakdown of Si microplatforms during the NW integration step. This was attained by changing the chemistry of the VLS process used for NWs growth, moving from silicon tetrachloride ($SiCl_4$) to silane (SiH_4) as silicon precursor gas. Process temperature was reduced from a 750-800 °C range to just 630ºC. The process was completed with the addition of diborane (B_2H_6) for ex-situ doping of the NWs and hydrogen chloride (HCl) to prevent the deposition of added polysilicon thin films.

Galvanic displacement method used for selective deposition of Au nanoparticles in bared Si walls (vertical <111> planes in trenches) was totally revised to allow a tighter control of nanoparticle size, the key parameter governing NWs diameter, and, therefore, overall array resistance. A comprehensive study determined how to use different process parameters to obtain statistical control of nanoparticle size distribution and deposition density. Figure 2 shows the archetypal diameter distribution and areal density for NWs obtained with this optimized process. The required pre- and post-processes involving wet steps were adjusted for suitability with new microplatforms.

A complete set of test structures (Figure 3), and specific measurement methods were developed to determine the material properties of NWs. Electrical and thermal conductivity and Seebeck coefficient were measured making use of ad-hoc test structures for single or several NWs. Values obtained, 200 S/cm for electrical conductivity, 6.5 W/m·K for thermal conductivity and 331 μV/K for Seebeck coefficient result in a figure of merit ZT≈0.11 for Si NWs used as thermoelectric material in bottom-up based μTEGs, obtained with NWs with a 113nm mean diameter. This ZT value exceeds that of bulk silicon by a factor of 10 and is the first reported for Si NW arrays epitaxially integrated in micro-thermoelectric harvesters. The thermal conductivity was determined with a novel method based on thermal AFM and fitting to a thermal model.

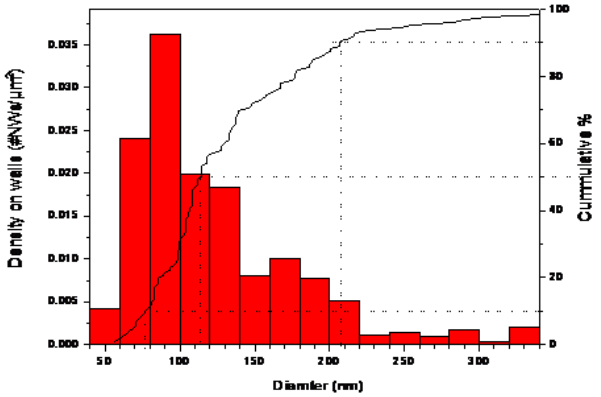


Figure 2: Diameter distribution and areal density of bottom up Si NWs grown within microplatform trenches. Cumulative count of NWs shows that mean diameter is 113 nm, and 80% of NWs have diameters between 76 and 207 nm.

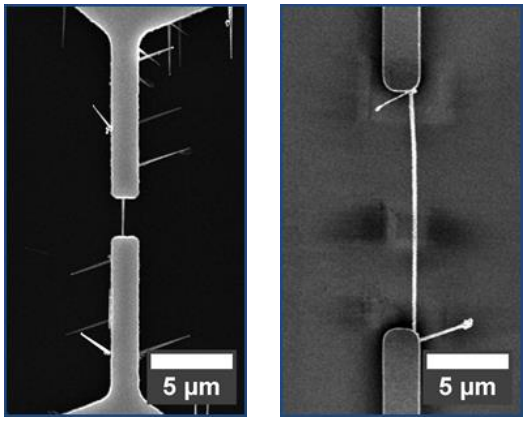


Figure 3: SEM images of test structures used in electrical and thermal conductivity measurements, which feature 15 µm thick Si bars exposing <111> opposing walls that are bridged by single NWs grow from side to side during CVD growth. Si NWs in 15 and 2 µm bridge, respectively

Si microplatform optimization

The key goal in the development of Si microplatforms shown in Figure 4 was the improvement of the thermal isolation between hot and cold parts to boost the thermal gradient obtained from a waste heat source. New designs implemented in SiNERGY kept the use of successive trenches to attain a longer effective NWs length between hot and cold parts, and introduced a new type of low thermal conductivity supports for the metal lines. In this way, after Si NWs integration, microplatform parts are linked only by thermocouple active materials, avoiding other parasitic heat paths. The designs adopted for these parts allow arbitrarily long features, which can be dimensioned to the optimal values required by the Si NWs properties.

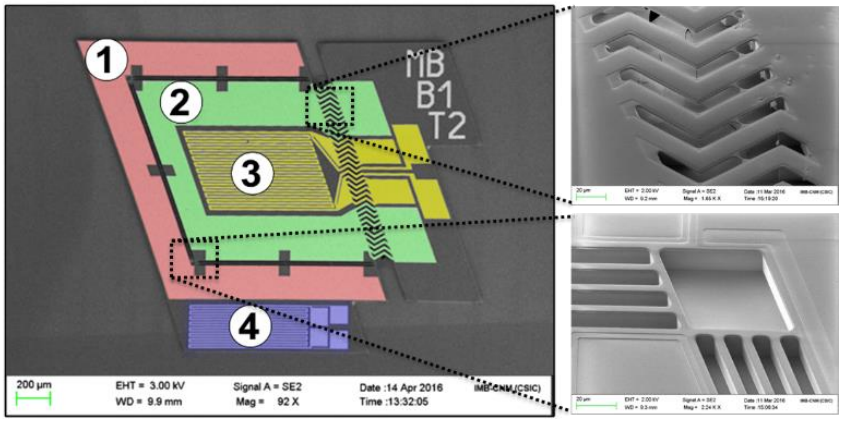


Figure 4: SEM images of actual microplatforms before Si NWs growth. Left image shows a design with 100µm long zig-zag Si_3N_4 supports. Key elements are labelled: (1) U-shaped external collector, (2) U-shaped internal collector, (3) integrated meandering heater for test purposes and (4) Si bulk temperature sensor. Right images show details of the Si_3N_4 metal supports, and a corner of the platform with four trenches. Each one has a 10 µm gap and Si bars are 6 µm wide.

The Si microplatform fabrication process was revised to enhance power levels provided by µTEGs. The metallization and the metal-Si contacts were improved in order to not degrade the low internal resistance provided by the dense Si NWs arrays (large amounts of highly B doped Si NWs connected in parallel). TiW was selected for electrical interconnections, using a preceding boron doping step and a subsequent thermal annealing process to ensure the formation of a silicide layer in contact areas.

The thermal contact with the environment (heat removal in the cold side) was identified as the key limiting factor in performance. A process displayed in Figure 5 was envisaged to fabricate a thermal interface structure in current devices, linking the isolated suspended platforms with a standard metallic thermal heat dissipater. Although integration was not yet accomplished, conservative estimates show that demo application power targets can be attained using a reasonable device area (a few cm^2 at most).

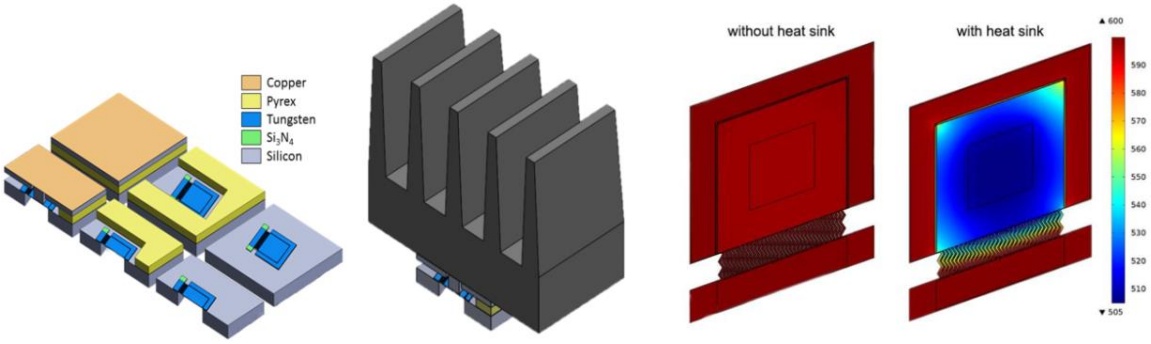


Figure 5: Left) Route devised for the heat sink integration in SiNERGY devices. A Pyrex spacer is used to place a silicon adapter on top of device, with a silicon column to properly contact suspended platform and a top copper film as interface with the metallic heat sink. Right) Temperature distribution with and without the heat sink obtained from FEM simulations. Device bottom temperature is fixed at 600 K and top surface has a natural convection to an ambient temperature of 300 K. Temperature span without a heat sink is only 3 K, while with the heat sink it reaches almost 100 K.

Other advances adopted in the course of SiNERGY project, both on the design and fabrication of the Si microplatforms, were intended to increase production yield. The platform robustness was enhanced using thick Si bars to hold the suspended platform in the most critical phase, i.e. before the integration of the Si NWs. The membranes supporting the metal connections were redesigned to match with square apertures for the DRIE in the backside, leading to a steadier etch process. The passivation thickness was increased and a partial etch was performed in bond pads location to avoid the exposure of whole metal surface after NWs integration. Finally, the whole fabrication sequence was rearranged to avoid the critical interferences between the different micromachining steps involved.

µTEG performance

The integration of improved bottom-up Si NWS in microplatforms was achieved, as shown in Figure 6, and harvested power with resulting µTEGs was assessed in different conditions. Measurements performed in still air show low thermo-voltages (hundreds of µV) comparable to the Seebeck coefficient measured for Si NWs arrays. Thus, in this condition the ΔTs achieved from the hot surface are in the 1-5 °C range, resulting in quite low harvested powers (10 nW) as shown in Figure 7. Therefore, the integration of a heat exchanger seems to be mandatory for having efficient devices. However, measurements performed using forced convection to emulate the effect of a heat exchanger provide ΔTs in the 10-40ºC range, still lower than values attainable with a passive heat exchanger according to simulations).

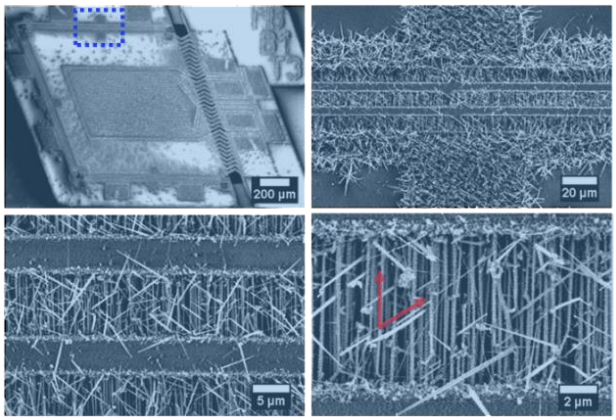


Figure 6: False-color SEM images of Si NWs grown in a mircoplatform with four trenches, with details of the NWs inside one of the 10µm gap.

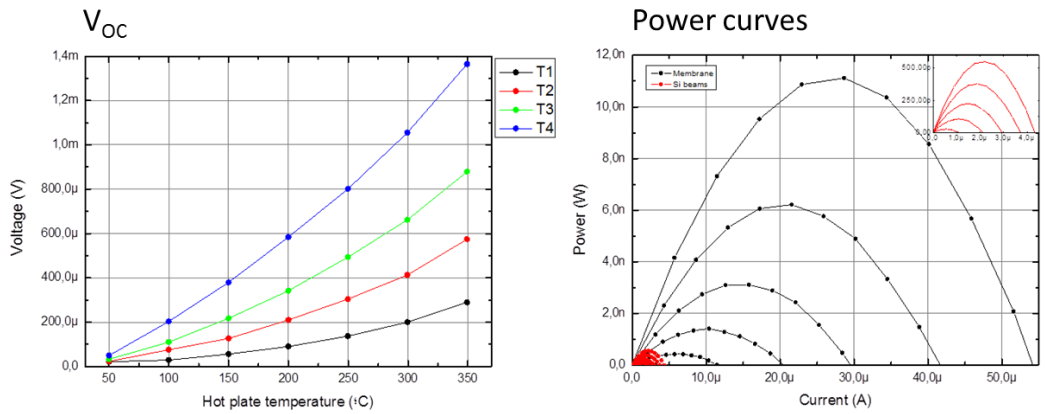


Figure 7: Left) Thermovoltage obtained with SiNERGY devices placed on a hot surface. Impact of the NWs effective length (1 to 4 trenches). Right) Power curves for devices with three NWs trenches using SiNERGY optimized platforms (dotted line) or a previous design with Si beams (detailed in the inset). Curves were obtained at different temperatures (50 to 300°C, in 50°C steps).

Data obtained with forced convection, shown in Figure 8, allow the estimation of the power expected from such devices in realistic operative conditions. The 2nd generation best samples show maximum generated powers around 0.07 µW from a device surface of 4 mm^2 (1.75 $\mu W/cm^2$) with open-circuit voltages around 3 mV, obtained with a hot-surface temperature of 120 °C. Thus, the ≈ 10 µW target needed for practical application on demo scenario can be basically reached with a device area of 2.5×2.5 cm^2.

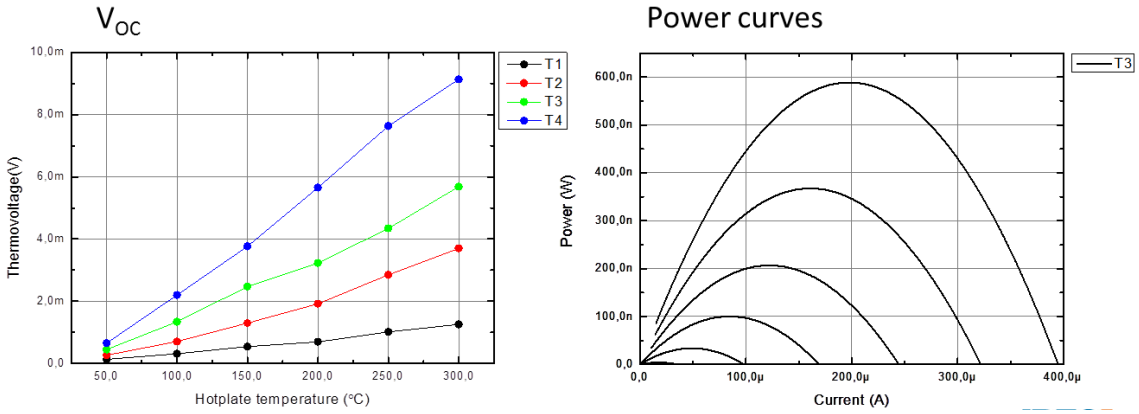


Figure 8: Left) Thermovoltage generated by SiNERGY devices placed on a hot surface when using force convection to emulate the effect of a heat sink. Voltage increases by a factor 8 with respect to the still air case. Right) Power curves

Future development

Despite the appropriate results achieved with the bottom-up µTEGs developed in SiNERGY, in line with the power requirements agreed for an autonomous wireless sensor node, there is still room for performance improvement. Future efforts will be focused on the integration of proposed heat spreader element in current microplatforms, in order to remove heat from cold parts to the ambient and procure higher ΔTs from available waste heat sources. The design of the microplatforms can also be optimised in terms of power density, which in current devices was waived to allow the integration of the self-test heating element. There is also room for improvement of the active material ZT. Work will focus on a further reduction of the NWs diameter to approach the 50 nm target, to get an extra reduction of NWs thermal conductivity. Other active materials with potential better thermoelectric properties, like the SiGe, will be investigated to be used with the bottom-up VLS growth process. This activity will be conducted in the framework a national research project recently granted by Spanish Ministry of Economy and Competitiveness.

Top-down approach

In the top-down approach, lateral architectures (using silicon NWs) were obtained. Lateral thermoelectric harvesters were designed to be fabricated in stacks, enclosing LPCVD grown SiNWs within a SiO_2/Si_3N_4 mould. Heavily doped p- and n-type polysilicon legs were fabricated. Figure 9 shows a schematic of the device. Figure 10 displays instead the sample structures at different stages of production.

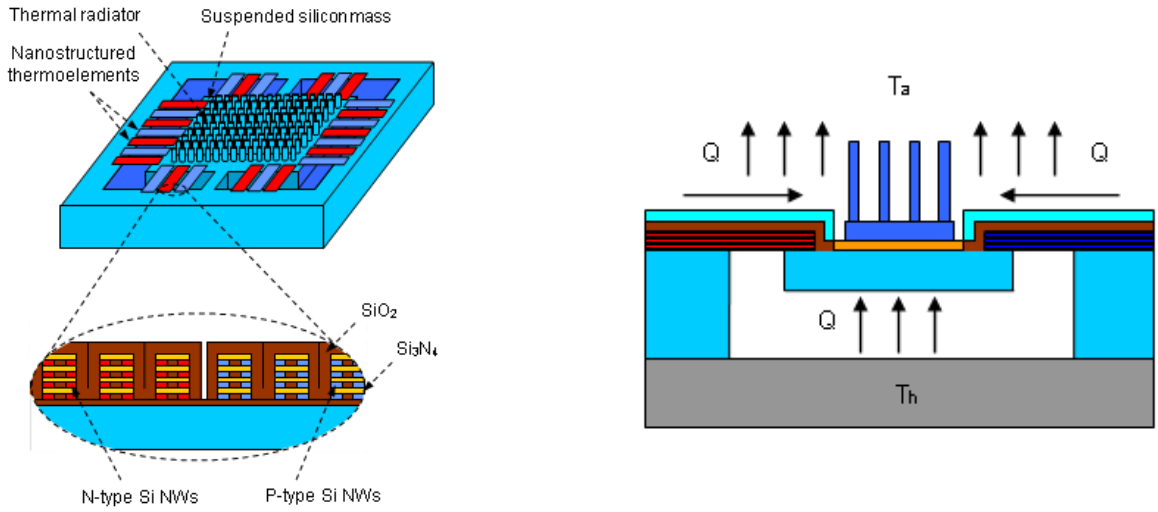


Figure 9: Prospective and side view of the top-down TEG

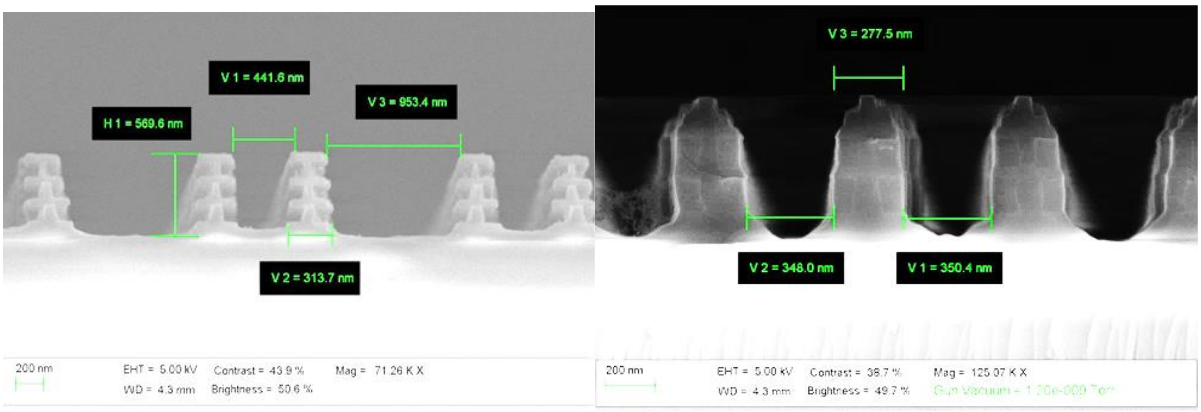


Figure 10: SEM micrographs of the mold (top) and of the grown encapsulated SiNWs

Tests were carried out on to evaluate the yield of the manufacturing process and the thermoelectric properties of the fabricated nanostructures. In the first-generation top-down devices the electrical resistance was found to scale correctly with the number of nanowires in parallel. Moreover, from the measurements, resistivity values were found typical of the high-doping range (around 10^{20} atoms/cm^3) required for high-performance thermoelectric conversion. Specific test structures were utilized to estimate the Seebeck coefficient of the n and p-type NWs (Figure 11). An approximately linear growth of the Seebeck voltage with the temperature difference was obtained. The Seebeck coefficient of the nanowires was around 150 µV/K for both doping types, as expected considering the high-doping level of these nanostructures.

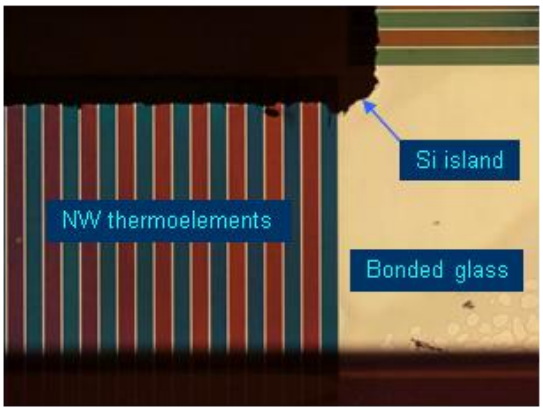


Figure 11: Details of a test structure

Simulated tests of operation were also carried out using a hotplate to check the produced thermoelectric voltage in conditions close to the real application foreseen for the devices, using a commercial radiator fixed using a special double-side adhesive tape sold with the radiator. Devices appeared to promptly respond to the temperature variation, with produced voltage in the order of 300 mV for heating temperatures as low as 80 °C (Figure 12, right).

The weak point of the first-generation devices was the fabrication yield, showing a critical at the wafer-boding step. However, numerical simulations showed that the performance gain using vacuum packaging was significant only for NW stacks with a high number of levels. On the contrary, for stacks of nanowires composed by a reduced number of levels, the performance of the device working in air can be comparable if not better than the vacuum packaged devices. This enabled a major simplification of the manufacturing process. The process flow could be modified by replacing the wafer bonding procedure with a plain SU-8 lithography followed by a backside etching of the entire thickness of the substrate up to the membrane constituted by Si_3N_4, SiO_2 and by the nanowires. This made the dielectric membrane containing the nanowires more robust, allowing to mount on it a metal heat sink. A commercial anodized aluminium heat sink could then be fixed manually on the suspended masses, achieving high fabrication yields.

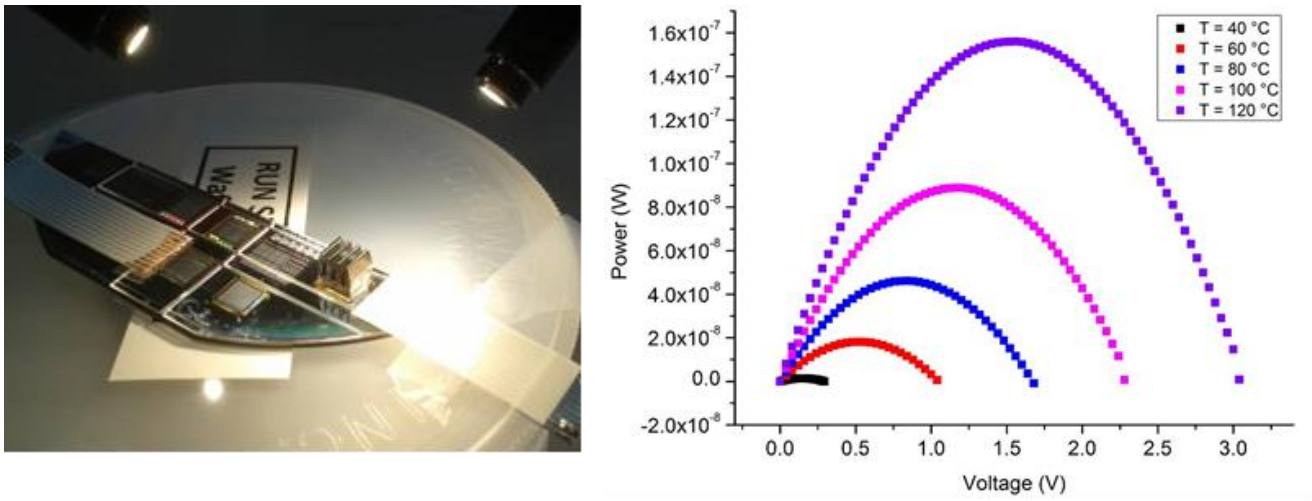


Figure 12: (left) Thermovoltage measurement setup and (right) Power voltage characteristics of the top-downTEG in response to variations of the applied temperature difference.

The conversion rate of the second-generation top-down devices was tested under simulated operative conditions. A maximum generated power around 0.16 µW from a total device surface of 0.64 cm^2 (0.25 $\mu W/cm^2$) with an open-circuit voltage around 3 V was obtained at a hot-sink temperature of 120 °C (Figure 12b). Thus, the target of ≈ 10 µW needed for the practical application on the demo application is basically reached with an exchange area of 6.3×6.3 cm^2, also considering that the modification of the doping process for n-type nanowires allowed to obtain a ≈ 10× reduction of the electrical resistance of the devices.

Mechanical energy harvesters

Electrostatic approach

Layout, materials and process flow of the 1st generation electrostatic devices

The basic configuration of an electrostatic energy harvester consists of five key elements: a seismic mass, suspension/springs, a set of electrodes, a charged electret and a packaging. We chose an in-plane sliding capacitor with a large usable mass and electret/electrode area and thus potentially the largest output power. The integration of the five key components in this configuration is depicted in Figure 13.

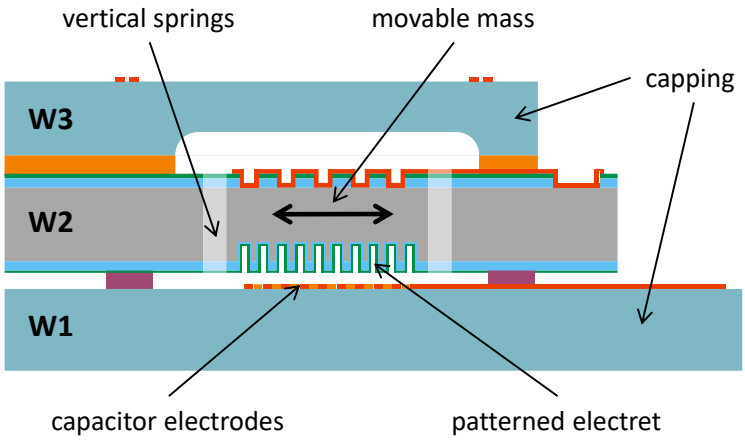


Figure 13: schematic cross-section of the 1st generation electrostatic energy harvester, showing the key components of the device.

The active part of the harvester consists of a variable capacitor, created by two sets of interdigitated electrodes on the glass wafer W1 and the charged, patterned electret on the Si wafer W2. Upon movement of the mass, the overlap (capacitance) changes periodically, resulting in a generated AC output voltage. The flexible springs allow for an in-plane movement of the mass. The micro-fabrication possibilities in bulk silicon, together with its high stiffness and low susceptibility to fatigue, make Si the ideal material to fabricate the springs. The mass and the spring system can therefore be integrated in the one Si wafer. Important for the long term functioning of the harvester is the stability of the electrostatic charge on the electret. We chose for an inorganic SiO_2/Si_3N_4 layer because of the good charge retention and for patterning of the electret by pre-structuring the substrate by DRIE prior to the deposition of electret layer. This has as major advantage that the nitride layer is continuous, which eliminates the possibility of charge diffusion.

Apart from carrying the capacitor electrodes, the packaging has different functions: first, it provides protection for the (fragile) Si mass/spring structure, limiting the out-of-plane mass displacement and therefore increasing the reliability. Second, in case of a hermetic vacuum packaging, the lifetime of the electret is extended by excluding influences from moisture and third, the vacuum eliminates the power loss due to air damping during mass movement. We chose to use a wafer-scale adhesive bonding process, where in case of the W1-W2 waferbond, the structured adhesive polymer also defines the capacitor distance. A stepped dicing process allows access to the electrodes on the bottom wafers. The 1st generation devices were successfully produced via the described route. The output power of the devices was measured using a shaker setup with sinusoidal input vibrations, showing the characteristic resonance curves of output power versus frequency, and a quadratic relation between the output power and the input acceleration. The maximum generated output power was in the order of 600 µW for an input acceleration of 3.5 G (maximal mass amplitude) at a resonance frequency of around 1100 Hz (Figure 14).

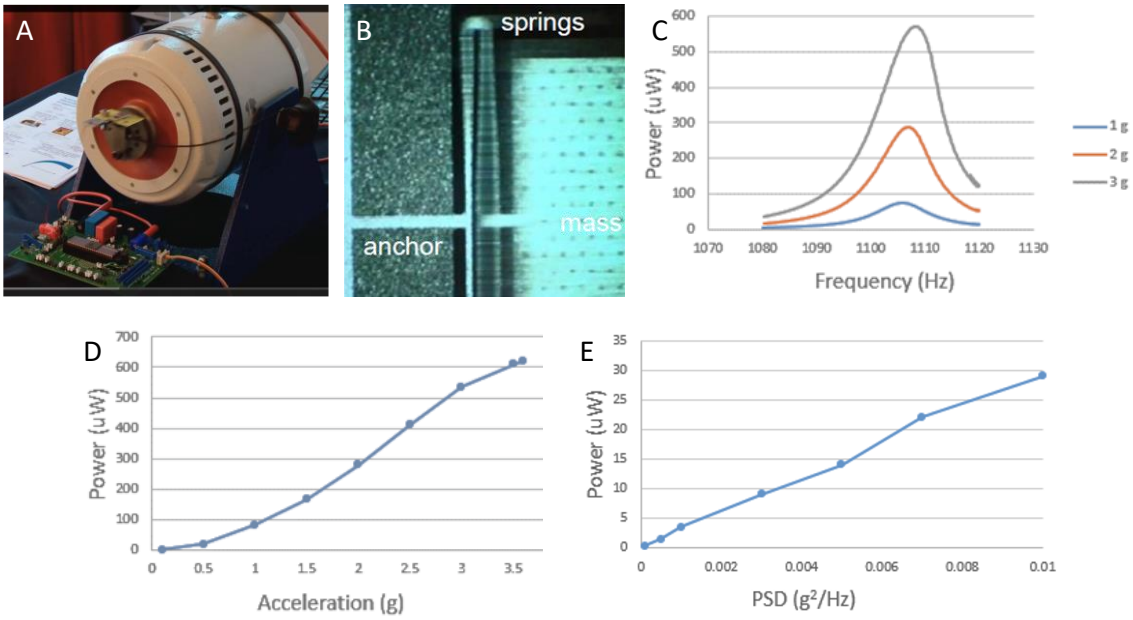


Figure 14: A) shaker setup with harvester; B) visualization of mass movement; C) resonance curves for different input accelerations; D) output power as function of sinusoidal input acceleration; E) output power as function of white noise input

Improved 2nd generation electrostatic energy harvester layout and process flow

Although successful in terms of output power, the thin silicon springs of the 1st generation devices were mechanically not robust enough for the targeted application in a TPMS. Improving the mechanical reliability was therefore the main point for the 2nd improved device generation, to facilitate the ease of integration in the TPMS. The most important changes in device layout and process flow were:

- Integration of the flexible silicon stoppers to improve the shock resilience. These could be integrated in the device layout using the two existing DRIE steps for the Si wafer (electret etch and spring etch) without adapting the processing.
- Integration of cavities with dimples in the capping wafers, reducing the out-of-plane movements of the mass, while maintaining the freedom of movement.
- An improved waferbond between the bottom capping wafer with electrodes and the Si device wafer with the electret: replacing the lithographically patterned thick BCB bond polymer by a thin layer of SU-8 around the cavity in the capping wafer, results in an increased bond strength (reliability) and simultaneously improves the hermeticity of the device, providing a better vacuum (output power) and moisture barrier (lifetime).

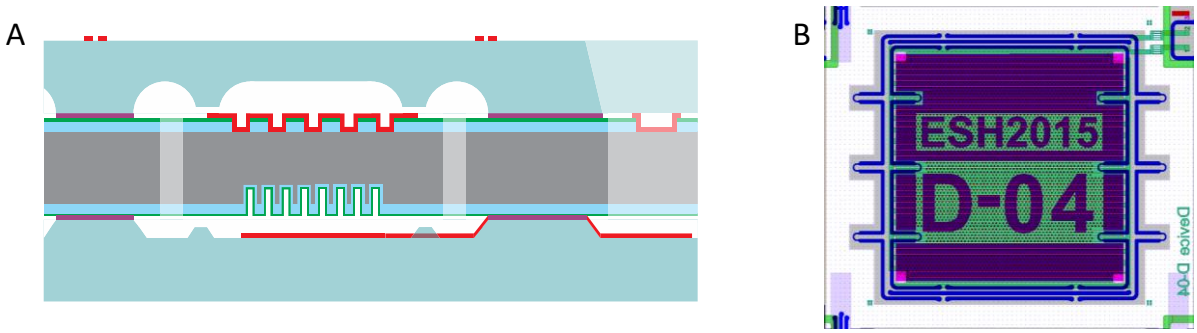


Figure 15: A) schematic cross-section of the 2nd generation electrostatic harvester with thin SU-8 bond and cavities with dimples and B) top view mask layout showing the 6 long flexible Si bumpers

These proposed layout and processing improvements were all successfully implemented during the fabrication of a batch (5 wafers) of 2nd generation electrostatic energy harvesters (Figure 16), resulting in a high yield and devices without visual errors.

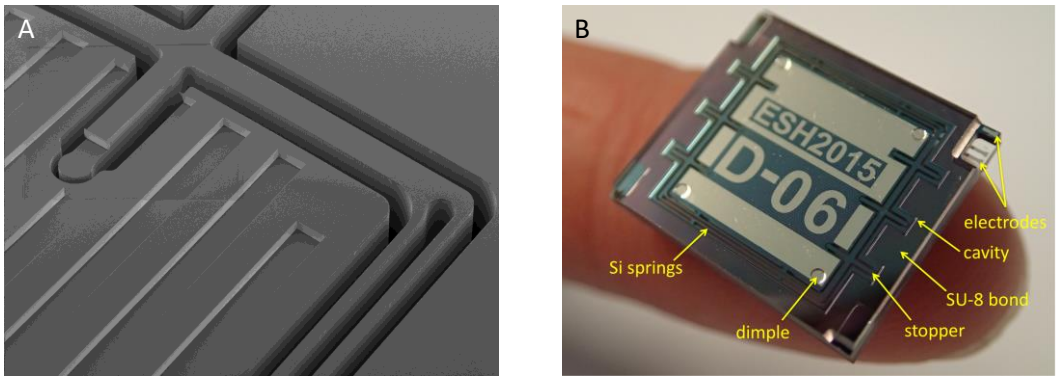
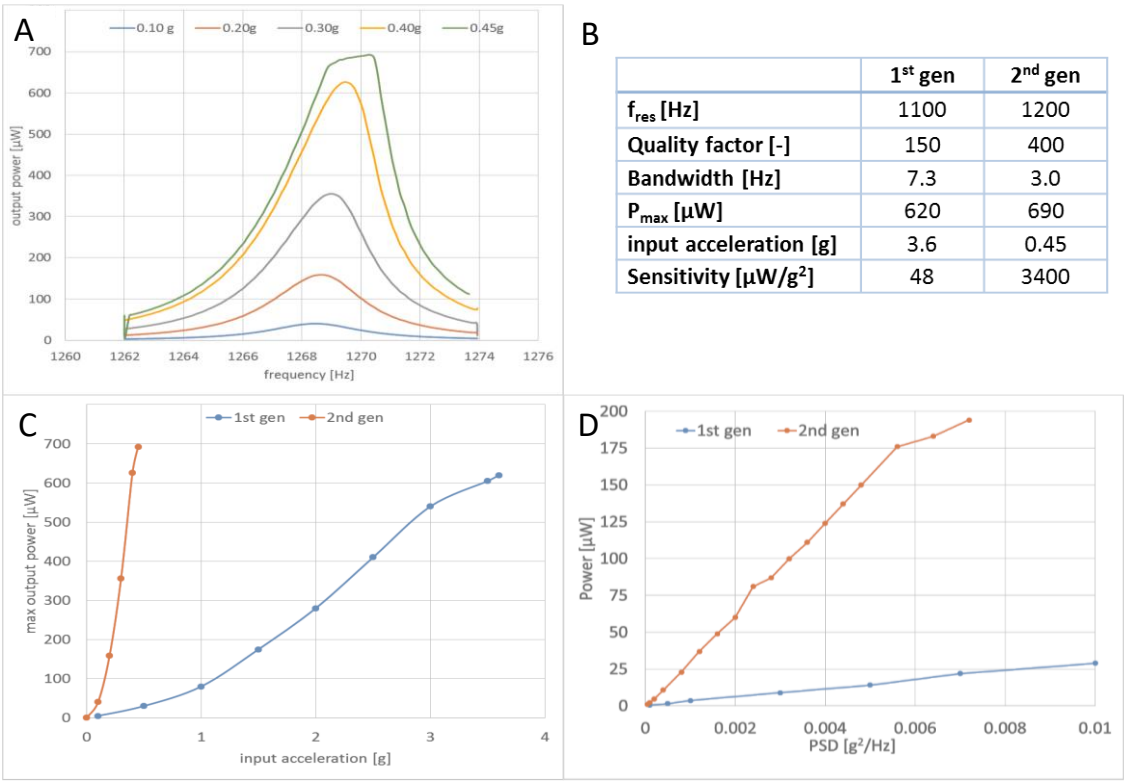


Figure 16: A) SEM picture showing the DRIE etched springs, flexible stopper and electret lines; B) finalized 2nd generation electrostatic energy harvester

2nd generation electrostatic energy harvester device characterization

Devices mounted on PCB were characterized on the shaker setup sinusoidal input vibrations and the output power was determined using the generated AC voltage signal, as well as in DC mode by charging a storage capacitor after rectification. The devices showed a power output of up to 700 µW at 0.5 G input acceleration. While this level of output power was comparable to the 1st generation devices, the low input acceleration necessary to obtain this, is remarkable. Due to the high vacuum SU-8 waferbond, the energy loss due to air damping was reduced and the sensitivity of the 2nd generation devices increased dramatically (3000 vs 50 µW/g^2).



	1st gen	2nd gen
f_{res} [Hz]	1100	1200
Quality factor [-]	150	400
Bandwidth [Hz]	7.3	3.0
P_{max} [µW]	620	690
input acceleration [g]	3.6	0.45
Sensitivity [µW/g^2]	48	3400

Figure 17: A) resonance curves for different input accelerations; B) table with mechanical characteristics of the 1st and 2nd generation devices; Output power as function of the sinusoidal (C) and noise (D) input acceleration, showing the very high sensitivity of the 2nd generation devices

For a more application oriented characterization, band-limited white noise with a PSD in the range of what is to be expected in a car tire (10^{-4} to 10^{-2} g^2/Hz) was used as input on the shaker system. The generated output power increased from 30 µW for the 1st generation devices to almost 200 µW for the improved 2nd one.

In conclusion several reliability improvements were integrated in the layout and in the process flow for the 2nd generation electrostatic energy harvesters, leading not only to mechanically robust devices, but also to very low losses due to air damping. As a result, the 2nd generation devices are very sensitive, which means that already at low driving speeds, sufficient output power for the TPMS application will be generated.

Piezoelectric approach

Layout, materials and process flow of the 1st generation of piezoelectric harvesters

Piezoelectric material has the property of generating a voltage along it when mechanically strained. It is well-known that microelectronic technology can be used to build tiny mechanical structures able to move and interact with integrated electronics. With these two premises, we have been working on the development of energy harvesters compatible with silicon technologies. The use of novel piezoelectric nanostructures and the way of easing their integration with silicon have been explored in this project. In our case, the configuration selected for the energy harvested is based on a cantilever structure, covered by the piezoelectric material, with a tip mass (Figure 18). However, in contrast to the electrostatic case, the work done in this project about piezoelectric technology has been more focused on discovering these new materials than in obtaining an operational device.

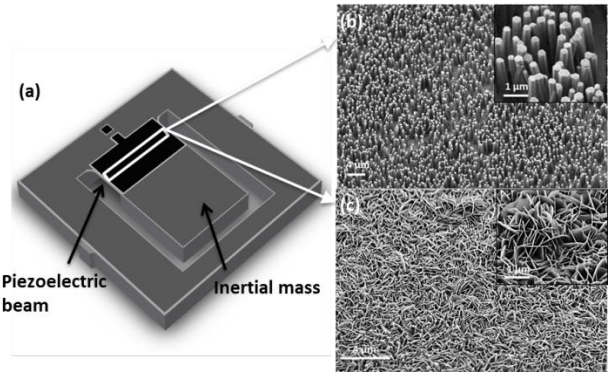


Figure 18: Functional device configuration. (a) A cantilever structure for mechanical out-of-plane motions, with the two different ZnO nanostructures for piezoelectric transduction: nanosheets (b) and nanowires (c)

From the point of view of materials, we have invented a way to control the selective-area growth of ZnO planar nanostructures. They can be grown much faster than the typical nanowire, better reproducibility and high quality and coverage (Figure 19). An electrochemical method to activate gold seed layer has been also created to improve the reproducibility and uniformity of the growth of nanowires.

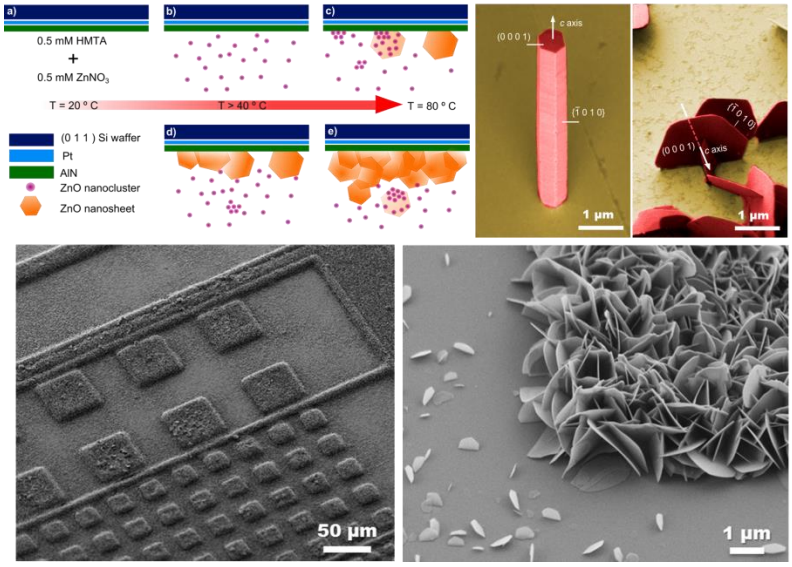


Figure 19: Hydrothermal growth of ZnO nanosheets (a). Comparison between nanowire an nanosheet orientation (b) and patterning of areas where nanosheets have been grown (c and d).

An in-depth characterization including, SEM, TEM, XRD, in-situ picoindentation and piezoresponse AFM have been carried out with excellent results. In addition, the following three hybrid devices were developed to gather an independent knowledge on the MEMS structure, the piezoelectric nanomaterial and polymer encapsulation and electronic integration:

AlN-based device mounted on an ad-hoc PCB:

The same MEMS technology and identical design have been used to fabricate a piezoelectric energy harvester of 25 mm^2 based on an AlN thin-film (Figure 20). A generated voltage of 0.2 V at a resonant frequency of 688 Hz was measured for an acceleration of 0.1G and a load resistor of 1MΩ (Figure 20b-c).

Flexible generator based on ZnO NS embedded in polymer:

The piezoresponse of the whole structure comprised of metal-polymer-ZnO-AlN-metal has been measured by PFM (Piezoresponse Atomic Force Microscopy) obtaining an effective piezoelectric coefficient of 2.7 pm/V. Also, in order to demonstrate the capability of using ZnO NSs for energy harvesting, a flexible test structure comprised of a stack of metal-polymer-ZnO-AlN-metal was fabricated and characterized under periodic bending and a constant vibration (Figure 21).

cm-scale energy harvester based on PDVF and attached tip mass:

We have manufactured several devices based by integrating PVDF, polystyrene, silver ink, acrylic adhesive, and epoxy. The 1st generation prototype had a resonance frequency around 32 Hz, a maximum RMS open-circuit voltage of 17.5 V at an optimum load resistance of ~10 MΩ, and a generated power of ~30 µW for an input harmonic acceleration of 1 G (Figure 22). It can be translated to a power density of ~10 µW/cm^3. Thanks to an optimized design, the new prototype exhibits a resonance frequency of 50 Hz, a peak-to-peak voltage of 80 V with a load resistance of ~10 MΩ for an input harmonic acceleration of 2 G. It can be translated into a generated RMS power of ~80 µW (more than 4 times higher).

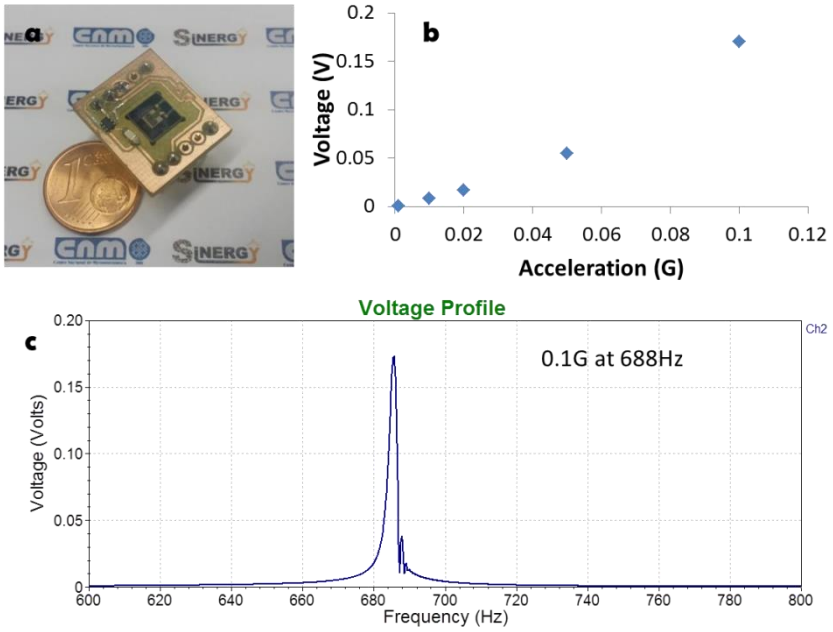


Figure 20: *Image of AlN-based device mounted on ad-hoc PCB (a), dependence of generated open-circuit voltage with input acceleration value (b) and frequency response with a load resistance of 1 MΩ at 0.1 G to find the resonance frequency at 688 Hz (c)*

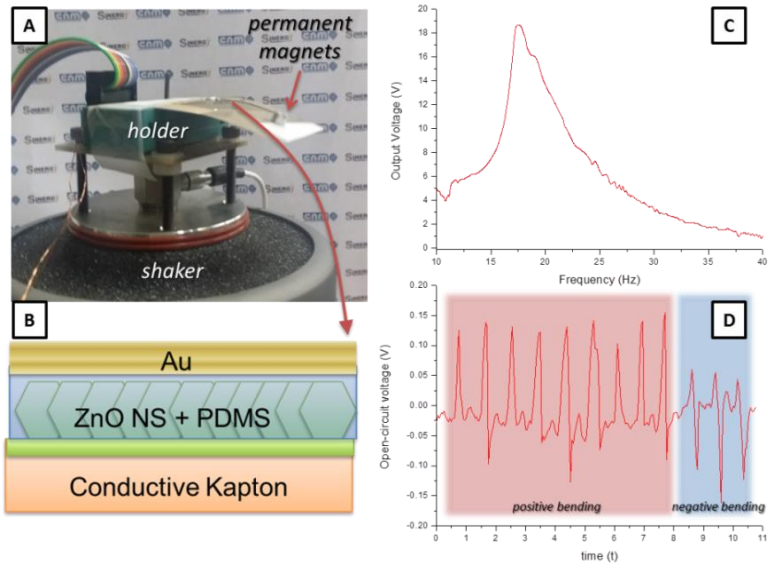


Figure 21: Flexible device mounted on top of an electromagnetic shaker to be tested at a controlled vibration at a certain frequency and acceleration (a), cross section showing the materials used in the thin film (b), output voltage generated by the test device showing a resonance peak at 17.5 Hz for an acceleration of 0.5 G (c) and open-circuit voltage generated by the test device when applying a positive and negative bending to the film (d)

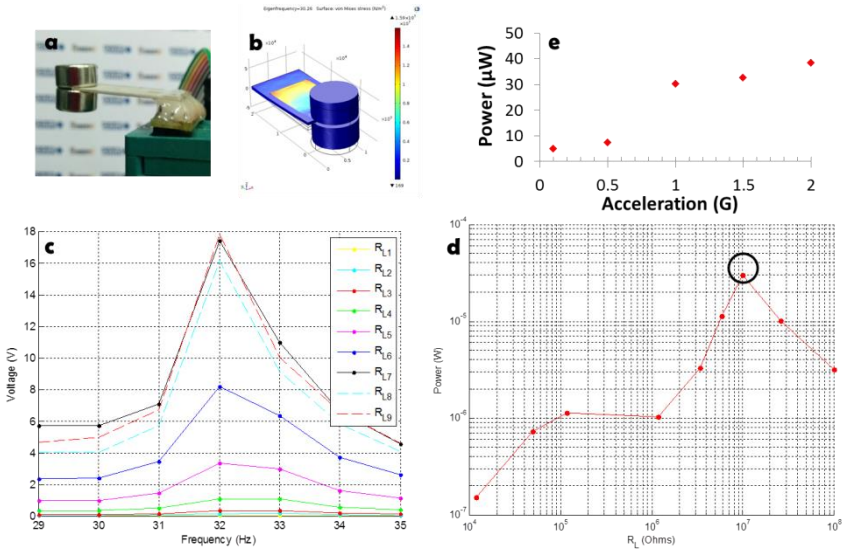


Figure 22: Image of fabricated 1st generation prototype (a), FEM simulations used to optimize the generator (b), voltage generated by the device vs. vibration frequency (c), extracted power vs. load resistance (d) and generated power versus acceleration magnitude (e).

Layout, materials and process flow of the 2nd generation of piezoelectric harvesters

A batch of 8 wafers with piezoelectric energy harvesters has been just fabricated according to the improved 2nd generation device architecture and process flow. Several optimizations have been performed regarding the designs of the 1st generation devices:

- 90-degree corners have been filleted to avoid lines of high stress that could lead to premature fracture at resonance.
- Dependence between mass-beam lengths has been optimized to maximize power output.

- Several novel designs with multifrequency resonance or tri-axial motions have been added.
- A frame patterned by DRIE has been defined around each chip perimeter to allow the dicing of the wafer with tweezers.

In addition, several process versions have been run in parallel. Specifically, a simplified run has been used to create MEMS platforms with the same designs but without piezoelectric layer or top electrode. This allows performing the deposition of the ZnO nanostructures and the protective polymer by means of a hydrothermal growth followed by inkjet printing of SU8 and silver/gold inks.

Preliminary experiments show a good covering of the NSs, good adhesion of the SU8 to the wafer, and successfully metallization of the SU8 top surface with silver ink to create the second electrode.

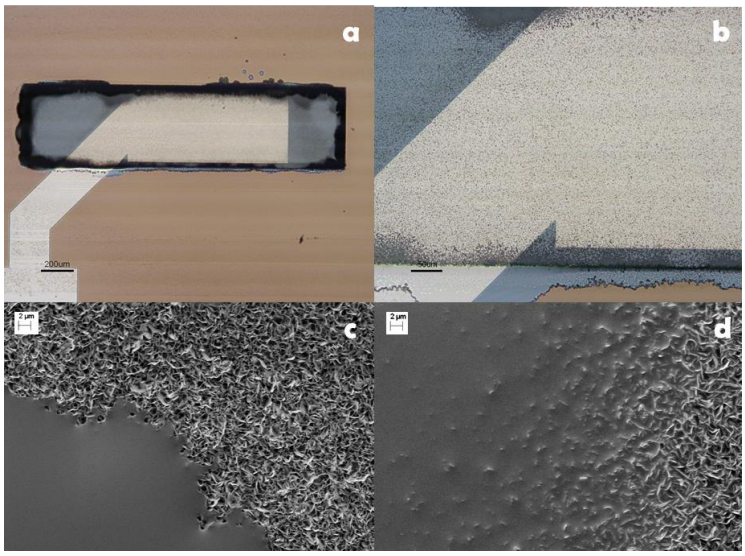


Figure 23: Optical image of ZnO NSs embedded by inkjet-printed SU8 on top of a device bottom electrode and higher magnification image showing detail of different layer edges (b). SEM images of ZnO NSs partly covered by inkjet-printed SU8 to validate the successful SU8 percolation (c and d).

In conclusion, several process versions have been run in parallel including a simplified run which will results in the creation of MEMS platforms that allows depositing the piezoelectric layer and the top electrode as post-processes by using hydrothermal growth followed by inkjet printing of SU8 and silver/gold inks. This is considered a highlight of the project since it may lead to a great simplification of the fabrication of such devices. These devices and their characterization will be finished after the project, but in the meantime several hybrid prototypes have been characterized: (1) *AlN-based device mounted on an ad-hoc PCB* with a power of 0.2 µW for 0.1 G of acceleration, (2) a f*lexible generator based on ZnO NS embedded in polymer*, measured by PFM to obtain an effective piezoelectric coefficient of 2.7 pm/V and (3) an *cm-scale energy harvester based on PDVF film and attached tip,* with an RMS power of around 130 µW (and 76 Vpp) at 2 G for an optimum load impedance of 10 MΩ. The team responsible has secured the follow-up of these developments through a recently granted a new project (ENSO –Energy for Smart Objects of the ECSEL JU).

Thin film solid state batteries

LiMn2O4 based battery

$LiMn_2O_4$ (LMO) has been first considered to be used as an intercalation electrode for a high voltage cathode material. This material has been grown using RF-sputtering, pulsed laser deposition (PLD) and a solid state reaction (SSR) process. The material holds a theoretical capacity of around ~154 mAh/g 3.5-4.5V. Thin layers of LMO have been characterised in detailed within the SiNERGY project. IMEC has prepared LMO films through RF-sputtering to be considered for full stack planar battery cell development and through electrochemical deposition of MnO_2 and post-lithiation conversion through SSR which is a compatible process towards a 3D solid state battery cell assembly. IREC has fabricated LMO layers trough PLD.

Planar full-stack battery cells were fabricated. Battery stacks based on LMO cathode electrode, LiPON solid electrolyte and Lithium anode electrode have been characterized and tested. This thin film solid state battery stack shows 92% of the theoretical capacity. This battery stack delivers a potential of 4.1V and can achieve a power of 0.24 mWh/cm^2 at 0.1 C rate. The battery stack is encapsulated in a 2 x 3 cm glass. The encapsulated battery is taken out of the glovebox to ambient air and still an open circuit potential of 4.1 V can be measured.

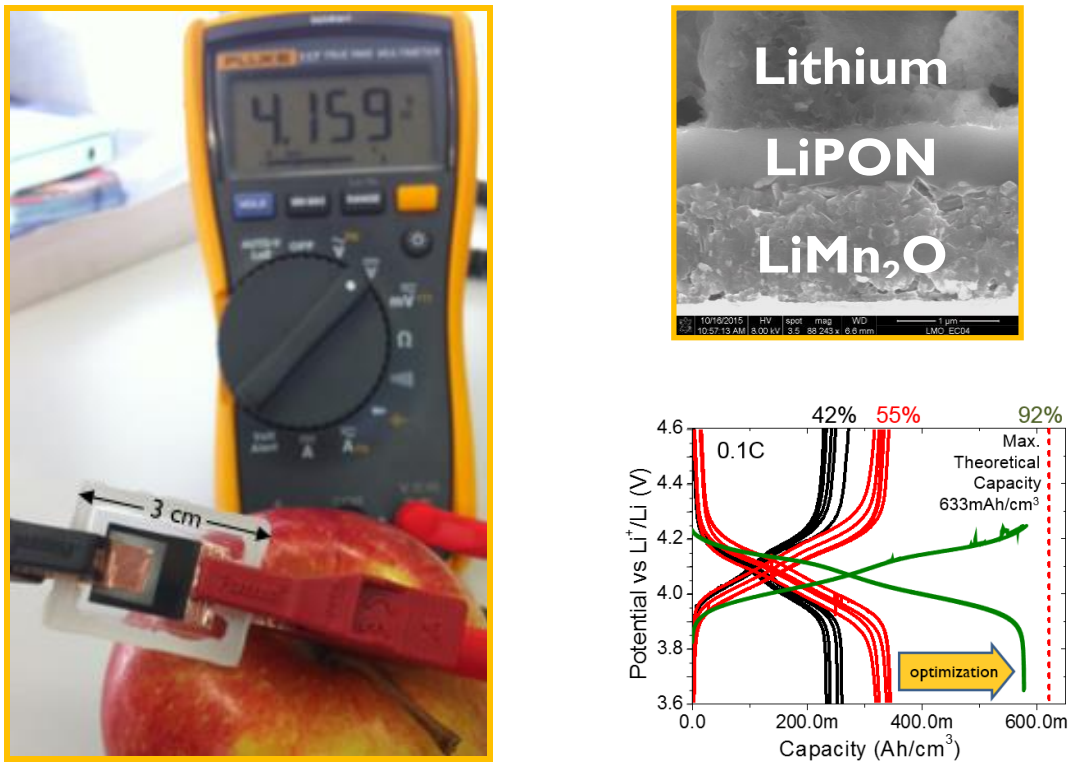


Figure 24: a) Battery stack glass encapsulation. b) Cross section SEM of a full battery stack of ***LMO/LiPON/Lithium*** *c) Charge/Discharge measurement and optimization of battery stack.*

IREC has explored a novel approach for the fabrication of a full battery stack exploiting the exceptional capabilities of the spinel $LiMn_2O_4$ optimized cathodes. This advance is presented here as an alternative full battery stack, which can be useful in some applications due to its extremely fast performance and simplicity of fabrication. The stack is formed by a $LiMn_2O_4$ cathode, aqueous liquid electrolytes (that do not have the safety drawbacks of organic electrolytes) and Zinc foil. The thickness of the battery based on its three components (cathode, separator and anode) is lower than 30 µm, considerably inferior to the 500 µm of the

silicon substrate. A full cell comprising 1 µm LMO as cathode, a Zn foil with 1 µm of thickness as counter electrode and a Celgard separator with thickness of 25 µm soaked with 1 M Li_2SO_4: 20 mM Zn SO_4 solution, was tested.

As it can be seen in Figure 25 the capacity reaches a value of 50 µAcm^{-2} under a current rate of 0.7 C (the cell is cycled in less than 42 minutes). The cell maintains 70% of this capacity after an increment of the current rate of 43 times, (the cell is cycled in less than 2 minutes). The potential delivered by the battery is close to 1.9 volts because to the contribution of the LMO cathode and Zn anode electrodes.

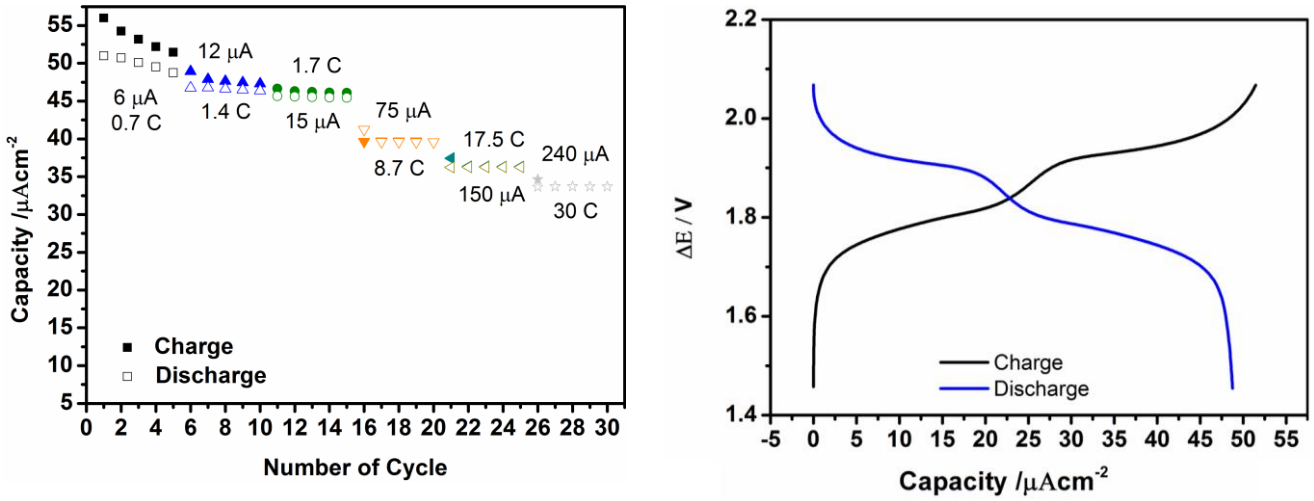


Figure 25: Rate capability under different current rates and Charge/discharge cycle at 15µA of a full battery based on ***LMO/Li_2SO_4:$ZnSO_4$/Zinc***

Li4Ti5O12 based battery

$Li_4Ti_5O_{12}$ (LTO) is a competitive candidate as an electrode material for Lithium ion batteries since it has a stable operating voltage vs lithium (1.55V), very small structural change (negligible volume expansion) and it can be easily obtained by several routes. IMEC has prepared LTO films through RF-sputtering to be considered for full stack planar battery cell development and post-lithiation conversion of TiO_2 which is a compatible process towards a 3D solid state battery cell assembly, IREC has fabricated LTO layers trough pulse laser deposition.

Planar full-stack battery cells were fabricated. Battery stacks based on LTO cathode electrode, LiPON solid electrolyte and Lithium anode electrode have been characterized and tested. In order to increase the capacity of the battery, LTO thicker films have been used to develop a full battery stack. 500nm LTO films have been deposited by means of RF-sputtering. Figure 26 shows the electrochemical performance of this stack. Cyclic voltammetry (Figure 26b) shows the characteristic peaks for LTO and charge/discharge cycles show a flat plateau at 1.55V. This battery stack achieves full theoretical capacity at 1C. At 10 C rate (300 µAh/cm^2) the battery stack reaches 50% of its capacity with a 99% coulombic efficiency. This battery stack delivers a potential of 1.5V and for the first battery stack delivered we could achieve a power of ~0.225 mWh/cm^2 (500nm LTO film).

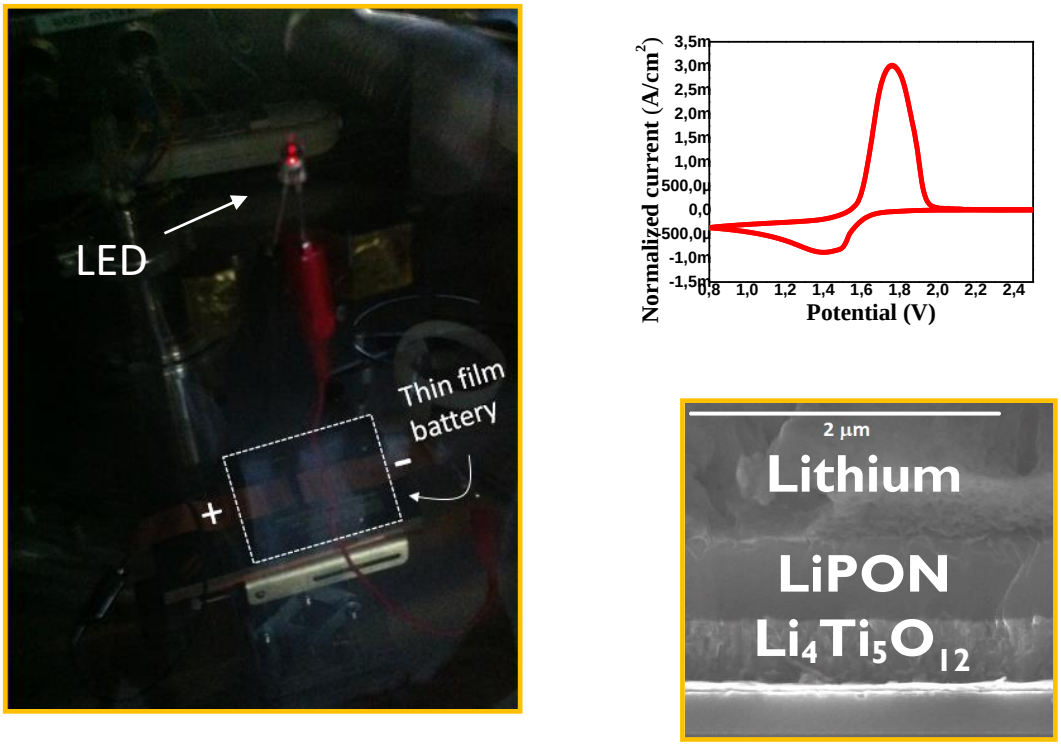


*Figure 26: a) Full battery stack **LTO/LiPON/Lithium** able to light an LED for several minutes. b) Cyclic voltammogram of the battery stack. c) Cross section SEM of battery stack*

3D thin film battery proof of concept

For 3D geometries and Si compatible stacks several materials have been investigated in order to explore conformal depositions and post-lithiation of individual films towards a 3D solid state thin film battery. The 3D architectures contemplated are based on a hexagonally arranged array of Si pillars etched into the Si substrate with pillar diameter of 2 µm, an inter-pillar distance of 2 µm and a pillar length between 60 µm-100 µm.

Lithiation schemes have been established for electrode layers. Manganese Oxide, MnO_2 (~3 V) has been used to do a post-lithiation step through a solid state reaction (SSR) to create LMO electrode layers (~4.2 V). The growth of the initial films is done through 3D compatible deposition techniques called Electrochemical deposition (ECD). Film deposition and post-deposition lithiation of individual thin films and half cells were evaluated in planar geometry. Moreover, MnO_2 has been deposited conformally in 3D geometries with high aspect ratio and has proven to be a well suited material to work as a positive electrode material for the next generation thin film batteries. This LMO electrode has shown promising results to be used in 3D micro-batteries. Recent results have shown that MnO_2 can be easily platted on 3D structures showing good conformal deposition and electrochemical behavior. The next figure shows and ECD grown MnO_2 film post-lithiated to LMO on 3D pillar structures. The 3D electrode shows an enhancement of a factor of 20 compared to a planar LMO thin film of the same thickness (~350 nm).

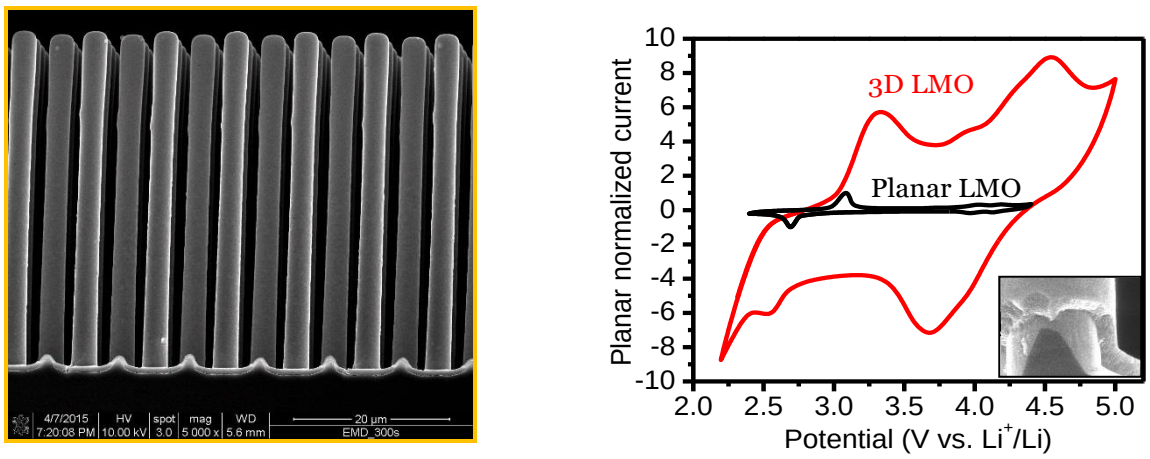


Figure 27: SEM image (cross section) of a 350nm MnO2 film grown by ECD on 3D pillar structures b) Cyclic voltammogram of a 3D electrode compared to a planar electrode.

The preparation of conformal electrolyte layers through a solid state reaction (SSR) have shown to be challenging. $LiTaO_3$, $Li_2NiGe_3O_8$ and $Li_4Al_{4-3x}SiO_4$ electrolytes have failed to provide the ionic conductivity and morphology needed for battery stack development and for 3D structuring. For planar thin film batteries SiNERGY has considered the solid electrolyte Lithium Phosphorous Oxynitride (LiPON) as backup material. This material is at the moment not compatible for 3D thin film battery technology. Hence, it is not trivial to think of an adequate solid state electrolyte which shows conformality and high ionic conductivity. At this point, IMEC has taken the knowledge they have in battery technology and specially in solid composite electrolyte (SCE) components and has implemented this type of materials within the SiNERGY project as an alternative. The SCE is based on a matrix which conducts Li-ions very easily and can be used as a filler for the 3D pillar arrays. This approach has led to a 3D thin film proof of concept device: LMO/SCE/Li (~4.2 V).

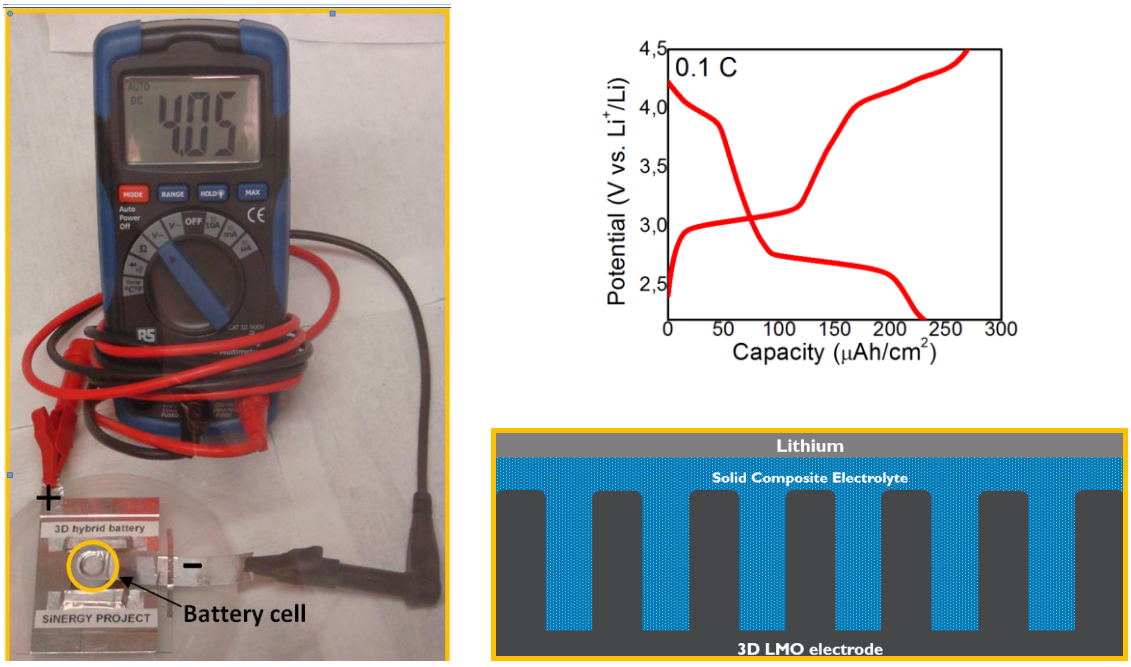


*Figure 28: a) 3D hybrid battery **LMO/SCE/Li** showing a stable potential around 4 V. b) Charge/Discharge measurement at 0.1 C of the 3D battery. C) Schematic representing the different layers in the stack.*

Feasibility integration in application scenarios

Fully autonomous tire pressure monitoring system (TPMS) demonstrator

Tire pressure monitoring systems (TPMS) are mandatory in USA and Europe in new cars since 2008 and 2012 respectively. The main parameters to sense are pressure and temperature of the air inside a tire. The measurement frequency depends on how fast is necessary to detect a possible puncture; usually a 5 to 10 second measurement rate is acceptable. For the autonomy of this TPMS demonstrator vibrations and shocks generated at the inner-liner of the tire will be used. There are two reasons to transfer from the standard TPMS on the valve to the inner-liner of the tire: much higher vibration levels and possible added functionality beyond pressure, resulting in a so-called 'intelligent tire' (see Figure 29). Small, cheap and robust vibration energy harvesters made with silicon processing are used to obtain autonomy without using batteries.

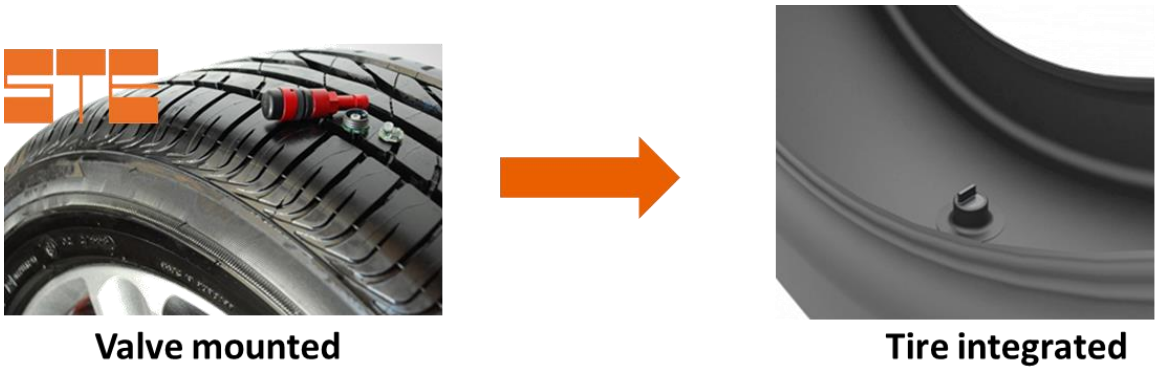


Figure 29: TPMS module transfer from valve mounted towards tire integration

The electrostatic vibration energy harvester developed by Imec-NL was combined with the ultra-low power TPMS module of STE, as shown in Figure 30. The module did not contain a battery and only the power generated by the harvester was used. The energy harvester improvements obtained in SiNERGY resulted in higher power generation at lower excitations and much better reliability. Especially, the reliability is known to be the challenge of using brittle silicon in applications with high impact shocks. Shocks in the tire at normal driving conditions can already amount up to 150G for 60km/h. Much higher accelerations can occur during driving on e.g. bad roads and TPMS integrated in the tire should withstand acceleration exceeding 2000 G. The silicon based harvester was improved by optimizing the springs and introducing efficient damping by introducing flexible silicon bumpers. In Figure 31, it is shown that 2nd generation devices with reliability improvements do not break up to 2000 G.

The system was tested in the lab and was fully operational at very low vibration levels. At those low vibration level (~10^{-4} g^2/Hz) the pressure was measured and sent every 10 seconds. The power needed was only ~4µW!! It scales linearly with noise level and at 2 times higher level, the pressure measurement was sent every 5 seconds. This result was possible due to development of STE's ultra-low power TPMS module and the improvements on the energy harvester.

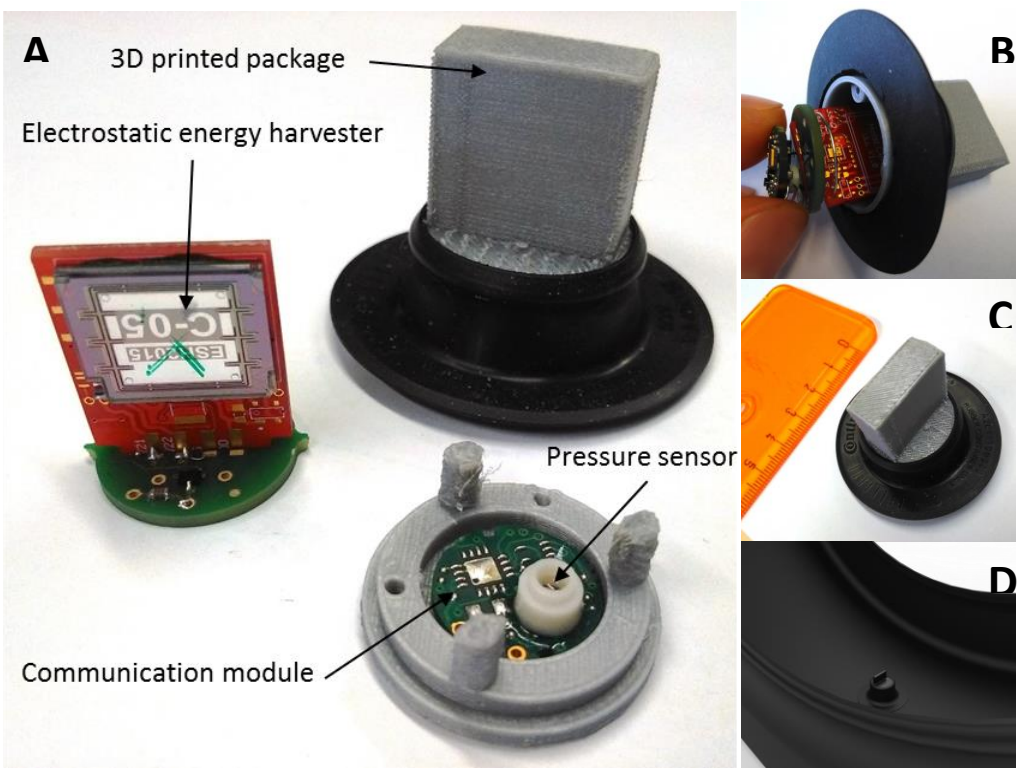


Figure 30: A) Components of the TPMS patch, consisting of PCB board with electrostatic energy harvester and direct charge PM, board with communication module and sensors and 3D printed package. B) PCB boards inserted in TPMS patch. C) size indication of the TPMS patch. D) impression of new TPMS demonstrator mounted inside tire

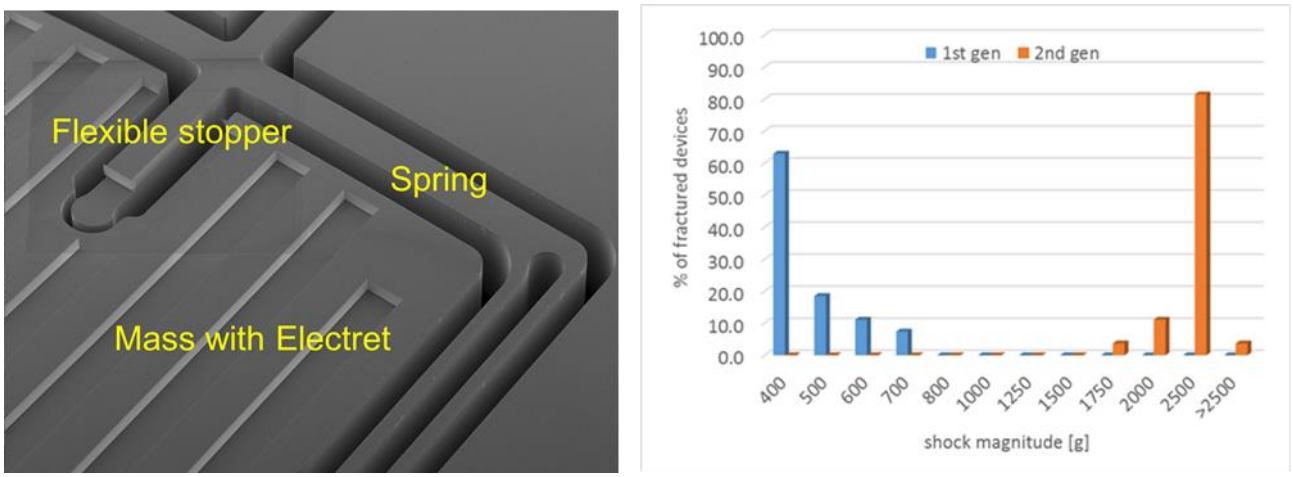


Figure 31: (left) SEM picture of electrostatic energy harvester with flexible silicon stopper of 2nd generation device. (right) drop tester results showing improvement for 2nd generation device.

Thermal electric generator (TEG) demonstrator

The temperature measurement in Foodservice Industry is extremely important for two reasons:

i. **Food safety**. Time and temperature are the two most important factors to control and monitor in the prevention of food borne illnesses.
ii. **Quality and performances.** Temperature is a parameter equally critical to obtain the desired quality of the cooking. For perfectly fried foods, it is critical to keep the oil at the correct temperature.

Industrial fryers are gas-powered, unplugged industrial appliances. EC regulations require oil quality to be monitored using a log of oil temperature as a function of time. Thermal harvester may then supply the power needed to monitor oil temperature and to transmit data through a wireless connection to a remote data logging system without the burden of wiring the fryer to the electric net. Such device is accomplished as shown schematically in Figure 32. The industrial fryer was used as a waste heat resource for a commercial in order to test the feasibility of the system.

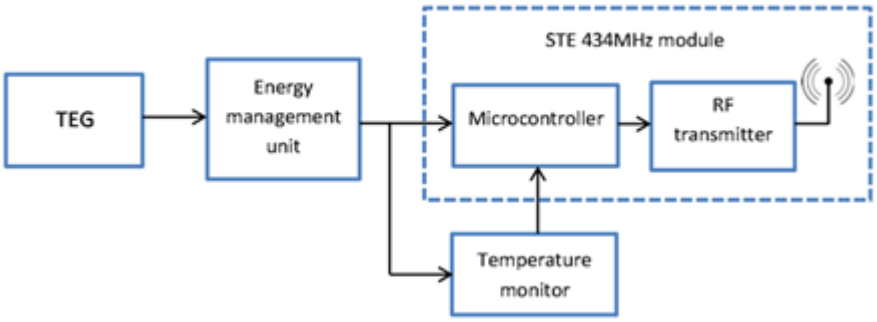


Figure 32: Block diagram showing the system design for the autonomous wireless temperature sensor for the gas powered fryer

The signal is transmitted by an ultra-low power 434 MHz RF module with pulse-based transmission, provided with a microcontroller from MSP430 family. A J-type thermocouple was used as a temperature monitor connected directly with the microcontroller. Integration tests were performed to anticipate assembly issue that might show up at the module level in the demo application using a commercial off-the-shelf TEG by Marlow Inc. using Bi_2Te_3 thermoelectrics with a nominal power output 5 times larger than the SiNERGY top-down thermal harvester. They led to identify the optimal hot point on the fryer metallic framework to be used to collect heat, to set a proper module assembly, and to define a suitable heat dissipation strategy. Results showed that the assembly allowed the RF transmitter to be powered and to transmit data with a frequency larger than 0.5 Hz with less than 5 seconds of initial latency without any need for a battery to accumulate power. This implies that the SiNERGY thermal harvester may provide a sufficient power output out of a surface of about 60 cm^2, largely compatible with the available hot wall size. Tests also provided clear evidence of the importance of an efficient heat dissipater to prevent temperature equilibration across the TEG after a few minutes of operation.

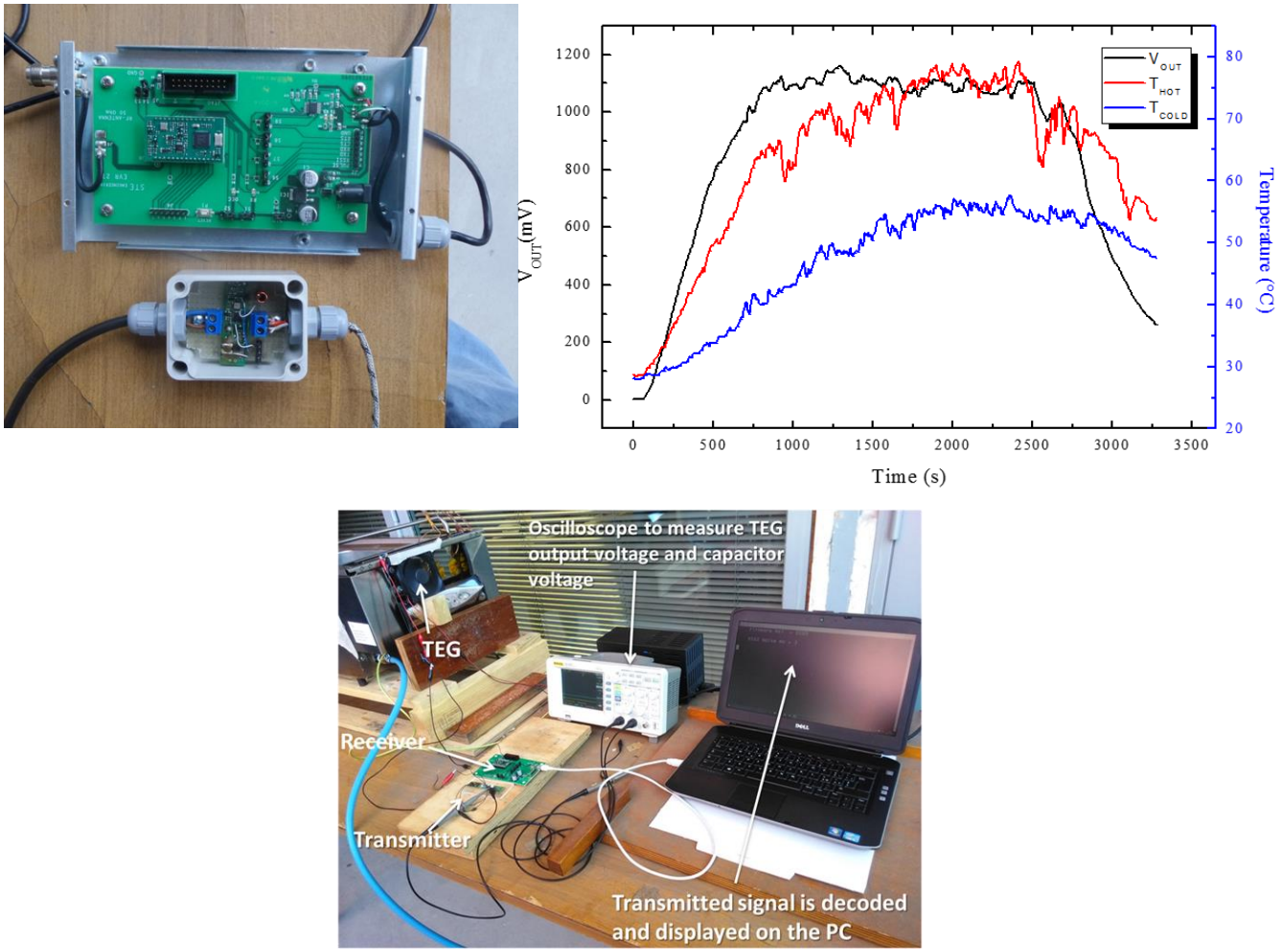


Figure 33: Thermal harvester setup: (top left) Details of the RF receiver and of the power management unit: (top, right) Thermovoltage measured under operative conditions; (bottom) overview of the system.

Piezoelectric energy harvester (PEH) demonstrator

Finally, a third integration exercise has been performed to cover one of the use cases projected at the beginning of this project. This use case focused on predictive maintenance, which is a novel concept on industrial maintenance based on the idea of predicting a machine failure before it occurs by means of the monitoring of several parameters, such as vibrations or temperature, to find precise patterns that are faithfully related to the imminent failure. Therefore, the environments of application are industries, factories or vehicles, where ambient vibrations are present. Therefore, we decided to use vibration-driven piezoelectric energy harvesters to cover this application.

The technology used to fabricate this demonstrator is based on piezoelectric polymer, instead of a silicon based devices, due to the higher degree of maturity and higher power generation. We have used a kit EZ430 (Texas Instruments), which contains a full-equipped sensor node with wireless connection and different sensors (temperature, pressure and 3-axes accelerometer). Several power management circuitries have been utilized to rectify and manage the power scavenged. The choice of using one or other depends on the application. Basically, the current generated has to be rectified, the charge accumulated and the subsequent voltage adapted to the requirements of the node of application.

We have configured a characterization setup that allows applying controlled vibrations to the energy harvesters (Figure 34). The energy harvester has been designed to resonate at 50 Hz, obtaining a peak-to-peak voltage of 80 V for a load resistance of ~10 MΩ, and an input sinusoidal acceleration of 2 G. Therefore, this means a generated RMS power of ~80 µW. After using a power management circuit, an effective power of 22 µW can be generated, corresponding to an efficiency of ~20%. It allows the operation of the EZ430, which requires less than 100 µW for a normal operation of waking-up, sensing, transmission and going to sleep mode again. For instance, for the case of the rotor of a helicopter or the train wheel set, where a vibration of around 20-60 Hz and 1-2 gG is present, 1 min of charge will allow 1 second of operation, which should be enough to allow continuous unassisted operation of the node.

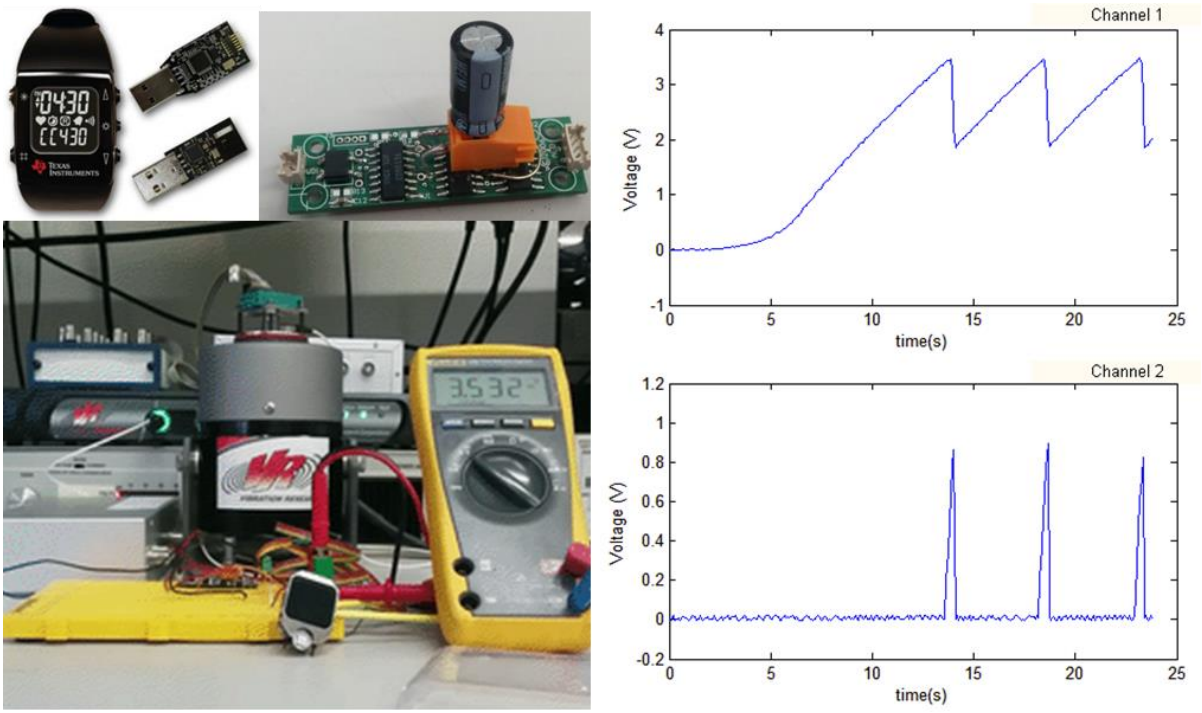


Figure 34: EZ430 kit and EH300 kits used for the PEH demonstrator. Characterization setup of PEH demonstrator. Output voltage generated by the energy harvester and current pulses generated when the application circuit is powered.