Diagnosis, Error Modelling and Correction for Reliable Systems Design

The DIAMOND project is set to cut development costs for Europe’s semiconductor and electronics industries by simplifying error diagnosis and correction in semiconductor and electronic systems. The consortium includes universities from Estonia, Sweden, Germany and Austria as well as large companies like IBM, Ericsson and two SMEs TransEDA and Testonica.

Main Objectives

Growing design costs are the main challenge facing the semiconductor community today. Therefore assuring the correctness of the design is of increasing importance. Electronics manufacturers currently spend a lot of time and efforts checking their products for errors. However, to date there has been little research into tools that diagnose and correct errors automatically, and current tools that identify errors in electronics systems are not up to the task.

Another, orthogonal, threat to the progress is the rapidly increasing vulnerability of nanoelectronic devices towards so called soft errors caused by radiation effects. Soft errors in sequential logic are becoming a more severe issue than in memories. The design community is currently not ready for this challenge as existing soft error escape identification methods for logic are inadequate.

Outline

The DIAMOND project develops a series of tools to help the semiconductor and electronics industries to diagnose and correct errors more efficiently. The tools include a diagnostic model for design errors, soft errors and physical errors, as well as automated error location and correction techniques. DIAMOND reaches beyond current state of the art by taking an integrated approach to the localisation and correction of different kinds of errors at all levels. Therefore the project results will have a significant impact on European nanoelectronics design industry.

DIAMOND’s consortium includes a wide range of competences required for developing a coherent solution for error diagnosis and correction. From the academic side, top-level research groups from universities of Tallinn, Linköping, Bremen and Graz are involved. Industry partners list large companies such as IBM - a leading microprocessor manufacturer, and Ericsson - a leader in the telecom field. Supported by electronics CAD vendors TransEDA Systems and Testonica Lab, the project team covers the full spectrum of the manufacturing chain from the tool development to the systems design and technology.
Technical Approach

The work is structured in six work packages as follows:

- WP1: Extension to Diagnostic Modelling – Development of a holistic diagnostic model for design errors and soft errors;
- WP2: Error Analysis and Diagnostic Techniques - Automated pre- and post-silicon localisation techniques based on the model from WP1;
- WP3: Error Correction Techniques - A robust reasoning framework for error correction at the transaction, implementation and post-silicon levels;
- WP4: Validation of the DIAMOND flow - definition of system requirements and end-user needs; validation of the tool prototypes on selected designs; final evaluation.
- WP5: Dissemination and Exploitation
- WP6: Management

The following Figure illustrates the DIAMOND development flow.

![DIAMOND Development Flow](image)

**Key Issues**

**Design error debugging.** DIAMOND is increasing the scalability of existing automated debugging methods, and is providing source-level readable and small repairs for the design engineer. Readability of correction enables keeping the user in the loop by allowing easier interaction with the debugging tools.

**Soft error analysis.** An essential aspect of soft errors verification is obtaining measures for detection logic coverage and proving its correctness. Today most of the verification process is carried out manually, which is time consuming. Therefore the automation provided by DIAMOND is very important.

**Post-silicon and in situ debugging.** Existing techniques for post-silicon and in situ test, diagnosis and repair are primitive. The infrastructure for access and control of such features is designed manually and ad hoc, which is inefficient and error prone. The automated solutions of DIAMOND are a promising alternative to this.

**Expected Impact**

Europe has actually a stronger position in design than in manufacturing. However, the electronics design costs are growing at an alarming pace.

The following figure shows the amount of time taken for specification, design implementation, fault detection, localisation, and correction in a typical chip development process. It is seen that about two thirds of the overall development time is spent on verification. When we find a fault in the detection phase, the localisation and correction phases entail manual analysis of complex bug traces to narrow down the source of the problem.

This means that two thirds of the verification time, or almost half of the development time, is spent on localisation and correction, i.e. debugging.

It is expected that the DIAMOND design flow will bring about:

- 50% reduction in time on fault debugging;
- 25% reduction in time to identify soft errors;
- 30% increase in identified unprotected soft errors.

According to the European Design Automation Roadmap, chip design costs have reached more than 60 M€ by 2010. Fault localisation and correction for each chip would cost nearly 30 M€. Therefore, reduction of localisation and correction effort by 50%, would cut down development costs by 15 M€ per chip project.

Reducing the time spent on debugging will also result in significantly shorter time to market. Reducing of soft error identification time and increasing the number of identified unprotected soft errors will improve the reliability and the productivity of future electronics' systems.