Implementation of widespread IC design skills in advanced deep submicron technologies at European Academia

The two IDESA projects by partners in seven European countries bring didactic course material and recorded tutorials to European academia for reuse in their engineering curricula in the field of implementing advanced integrated circuits.

Main Objectives

The purpose of the two IDESA Support Actions is to make available didactic training material on the design flow for integrated circuits (IC) for advanced deep sub-micron technologies, free of intellectual property rights, for the benefit of European academia. The projects goal is to make sure that academia can close the widening gap between the current state-of-the-art at the modal European academy and the state-of-the-art in leading industry. These projects do not have a scientific research component and, except for perhaps academic recognition, do not bring benefit to any of the project partners.

Outline

Didactic material was developed in IDESA project and made available for reuse in the course portfolio of bachelor and master engineering curricula, under IDESA-2. Training is organized in class-based hands-on sessions and advanced seminars using state-of-the-art multimedia technology over the web or on DVD.

Technical Approach

There are 4 different advanced implementation courses that tour different sites in Europe. These courses are hands-on courses using a train-the-trainer philosophy. Each of these courses is repeated 7 times. All of these courses address the advanced implementation issues relating to the 90 nm process node. This brings the universities to a more advanced level of implementation skills to start engaging in 65- and 45-nm issues. These courses are:

- Advanced analog implementation flow
- Advanced RF implementation flow
- Advanced digital physical implementation flow
- Design-for-manufacturing

The full details of the courses listed below can be found on http://www.mtc-online.be/mtc/idesa/Courses.html.
The portfolio of existing recorded tutorials, developed under IDESA, are expanded with 8 new tutorials in IDESA-2. These will be defined in collaboration with the IDESA Program Board that is operational since December 2007. The expanded portfolio will continue to be disseminated free-of-charge to all academia in Europe, either in bulk download-format for storage on the local academic intranets, of in video-on-demand format.

**Key Issues**

The IDESA consortium has built a portfolio of **public domain didactic seminars**, addressing issues that are not addressed in the design flow courses but that are of dominant importance for the 65 and 45 nm generation design flows.

1. Low Power Digital Design in Sub-90nm CMOS Technologies by Wim De Haene (KULeuven)
2. Component matching: best practices and fundamental limits by Marcel Pelgrom and Maarten Vertregt (NXP Research)
3. Automotive Interferences: EMC and Transients by Herman Casier
4. Reliability of future advanced CMOS circuits and technologies by Guido Groeseneken (IMEC)
5. Two important transistor innovations: strained silicon and FinFETs by Geert Eneman - Nadine Collaert (IMEC)
6. Risk free, 65 nm and beyond, digital low power design by François Thomas (Cadence)
7. Variability Aware Modeling and Yield Aspects by Bart Dierickx (IMEC)
8. Variability and Litho-aware digital implementation by François Thomas (Cadence)
9. Leakage physics and modeling by Wieslaw Kuzmicz (Warsaw University of Technology)
10. Techniques to control leakage power at technology and device level : application to a fully power aware SoC design by Edith Beigné (CEA)
11. Compact models for DSM by Christian Enz (EPFL)
12. Statistical Static Timing Analysis and Optimization - François Thomas (Cadence)
13. CMOS front-end design at millimetre wave frequencies - Alexandre Siligaris (CEA LETI)
14. Analog design in scaled technologies - Andrea Baschirotto (University of Lecce)
15. Design of ADC in advanced technologies - Andrea Baschirotto (University of Lecce)
16. Design of analog filters in advanced technologies - Andrea Baschirotto (University of Lecce)
17. Low power CMOS 65 and 45 nm industrial technologies - Thomas Skotnicki (STMicroelectronics)
18. ESD and Latchup - Fabrice Blanc (ARM)
19. DFT to meet Nanometer Test Challenges - Philippe Rossant (Synopsys)
21. Advanced circuit design in emerging 2D & 3D SOI technologies - Thierry Poiroux (CEA LETI)
22. SOI and multiple gate transistors - Thierry Poiroux (CEA LETI)
23. Thermal issues in nanoscale VLSI devices and circuits - Nicolo Rinaldi (University of Naples)
24. Statistical Memory Analysis for robust SRAM design - Paul Zuber, Petr Dobrovolny (imec)
25. Metric Driven Verification - Hans Zander (Cadence)
26. Assertion-based verification - Kawe Fatouhi (Cadence)
27. A guided tour of the Interconnect road map from 90 nm down to 32 nm designs in the analog and digital domains - Roberto Suaya
28. Electrostatic discharge protection for DSM RF circuits - Dimitri Linten
29. Fundamentals of digitally-assisted RF - Robert Staszewski
30. SOC in 65 nm and below. Concepts, design, implementation and application - Fabien Clermidy, CEA-LETI
31. Heterogeneous Design - Nicolas Delorme, Asygn
32. Millimeter-wave Design in Silicon Technologies - Didier Belot (STMicroelectronics)
33. CMOS Radio Wave Design for MM-Wave applications - Piet Wambacq
34. Nonlinear distortion analysis in circuits and systems - Prof. dr. ir. Gerd Vandersteen – Dr. ir. Ludwig De Locht (Vrije Universiteit Brussel)
35. On-chip Passive Components and Deep Submicron RF IC Design - John R. Long (Delft University of Technology)

**Expected Impact**

IDESA projects bring research results outside the industry/research consortia through a framework that embraces dissemination, training and education and access to supported project results, tools and methodologies, with the objective to increase capability in Europe to design in a reliable manner products that use the most advanced IC manufacturing and integration processes, and maintain leading position of Europe in product innovation and design for major application fields.