Key Innovation

The shift to parallel architectures is not at all the consequence of a scientific breakthrough. It is a consequence of hitting the technology walls that prevented from pushing forward the efficient implementation of traditional uniprocessor designs in silicon: (1) Voltage scaling and power reduction techniques, or Power Wall; (2) Instruction-level parallelism, or Complexity Wall; (3) Memory latency hiding techniques, or Memory Wall; (4) Reliable and low-variability silicon technology, or Yield Wall.

All these above-mentioned walls must be broken into to maintain the growth rate of embedded computing in terms of computational efficiency. Such a challenge requires a holistic approach ranging from programming manycores, to 3D architecture exploration and fabrication technologies. Furthermore, manycores will benefit tremendously from 3-dimensional (3D) integration technology that enables distribution in space of computational and storage functions to achieve unprecedented performance levels.

PRO3D will innovate in both hardware and software technologies and demonstrate the effectiveness of manycores by an integrated and concerted effort in key aspects of hardware and software design: memory hierarchies and thermal management.

The key outcome of PRO3D will be a holistic system design methodology and associated tools that will bring a drastic 20-25% improvement of productivity to reduce development cost and time to market for future embedded computing.

Technical approach

PRO3D will show that embedded applications can benefit from the advance of integration by exploring design avenues offered by 3D opportunities and address its main challenge: thermal management.
These opportunities and challenges will be addressed while preserving strong requirements on software quality like composability and distribution.

PRO3D will: (1) investigate 3D design based on Through Silicon Vias (TSVs) and micro-channels for liquid cooling; (2) develop a system software flow that can operate transparently on parallel manycore platforms; (3) develop formal methods for software design guaranteeing the composability and correct operation of both hardware and software; (4) explore the impact of 3D integration for new computing architectures.

The software tool chain will be used first to explore the 3D manycore architecture design space and to select the most promising alternatives while taking into account the key issues of 3D stacking: memory and thermal management. The tool chain will be further extended to provide several pre-computed application-on-manycore mappings with performance and temperature considerations. With the help of an accurate thermal simulator the runtime will be designed to provide active cooling and thermal monitoring of the 3D stack.

**Demonstration and Use**

The project will demonstrate several market enablers from the PRO3D tool chain for future 3D manycore architectures. These will include 3D platform exploration based on memory and thermal analyses, as well as thermal- and performance-aware application mapping, compilation and execution. At execution time, the runtime will activate cooling according to the thermal conditions of the 3D stack, to preserve the thermal integrity of the 3D stack. This will ultimately be demonstrated by a multimedia application running atop a virtual prototype based on STMicroelectronics’ “Platform 2012”.

**Scientific, Economic and Societal Impact**

Although the PRO3D consortium brings together world-class leaders in their related fields with competencies to cover software, architecture and 3D integration, its key differentiator is access to and input from an industrial many core System on Chip, named “Platform 2012” provided by STM. By developing several market enablers in cooperation with STM for manycore based, heavy-duty embedded applications, PRO3D will reinforce the competitiveness of the EU industries in the global embedded system market, and will ultimately lead to new high technology jobs for European workers. Moreover, PRO3D will allow its scientific partners to enhance European curricula for embedded system design and further their world-class research leadership in programming and exploration challenges raised by upcoming 3D multicore architectures.

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<th>Project partners</th>
<th>Country</th>
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<tr>
<td>CEA</td>
<td>Commissariat à l'énergie atomique et aux énergies alternatives</td>
</tr>
<tr>
<td>VERIMAG (represented by) Université Joseph Fourier Grenoble 1</td>
<td>Fr</td>
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<tr>
<td>ETHZ</td>
<td>Eidgenössische Technische Hochschule Zürich</td>
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<td>UNIBO</td>
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<td>STM</td>
<td>STMicroelectronics</td>
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<td>EPFL</td>
<td>École polytechnique fédérale de Lausanne</td>
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**First achievements made during Y1 (2010)**

- A realistic 3D manufacturing flow based on CEA-LETI's Through Silicon Via (TSV) and EPFL's micro channels has been designed for the 3D stacking, together with a reference thermal model.
- The MPARM virtual prototype and DOL have been extended for 3D: L1 & L2 memories, intra-cluster crossbar, Network-on-Chip (NoC), and connection to thermal models.
- System Model & Code Generation: The BIP modeling approach has been extended for the System Model, connected to DOL3D, and the code generation for MPARM has been started.
- The application has been ported to the PRO3D programming model, and characterized.