Brain-Inspired Hardware Architectures

What
Why
The HPC-NC Convergence
Technologies
Collaboration and Integration

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presented by Karlheinz Meier, Heidelberg University
WHAT?

Brain: Subject of basic science ➔ Neuroscience
(Part of) ourselves ➔ Neuromedicine
Information processing ➔ Brain-like computing

Two evident links to future emerging technologies:

High performance computing (HPC) simulations
Peta- to exascale von-Neumann Maschines
$10^{15} – 10^{18}$ flop/s

Synthetic circuits as physical models
neuromorphic computing (NC)
Micro- to nanoscale circuit components

Exploit: Low power, fault tolerance, learning,
Aim for: Cognition, prediction making
WHY?

Neuroscience Research Tool
- **Exploit** real-time or beyond real-time performance
- Understand wide range of relevant time scales in one experiment (ms to years)
- Systematically develop, verify, falsify theories for development, learning and plasticity
- **Transfer** results to neuromedicine, neuropharmacy, neuropsychology

Large Scale System Demonstrator for Nanoscale Devices
- **Exploit** small size of nanoscale devices – tolerate imperfections and lack of precision
- Establish industry standard manufacturing technology as CMOS backend
- Approach $>10^{15}$ dynamic storage cells (synapses)
- **Transfer** results to device manufacturing

Novel Computing Architecture
- **Exploit** key features: low power, scalability, speed, fault tolerance, learning
- Demonstrate ability to process noisy, unexpected data to make predictions
- Systematically develop, verify, falsify multiscale theories for neural computation
- **Transfer** results to process non-biological information

Downscale to Low-Cost, Low-Power Devices
- **Exploit** research results on principles of neural computation
- Simplify and minimize circuits for specific consumer oriented applications
- **Transfer** to low-cost, low-power consumer appliances
The HPC – NC Convergence

Exascale meets Nanoscale – Computers become brainlike

Synthesize a system of $10^{11}$ neurons, $10^{14}$ compartments, $10^{15}$ synapses, $10^{18}$ Bytes/s, ms-resolution, months timespan ... :

The power problem

The connection problem

The software problem

The runtime problem

The reliability problem

The size problem

⇒ Specialised cores (analogue)

⇒ Protocolls, bandwidth, 3D

⇒ Learning and plasticity

⇒ Massive parallelism

⇒ Fault tolerance

⇒ Component miniaturisation

Some are common concepts for future HPC and NC systems

Current differences: Numerical vs. analogue cores, asynchronous operation mode, degree of parallelism
Technologies

Low power circuits
Mixed-signal circuits
High bandwidth communication
Wafer-scale-integration
3D-integration
Packaging
Connections
System integration
Design tools
Deep-submicron manufacturing
CMOS postprocessing
Nanoscale non-CMOS components
Large-scale software development

Technologies evolve in parallel to Neuroscience
NC may well drive the development in the future
NC Concept example

Base Facility
24 crates with 312 wafer assemblies

With current 60 nm technology

$10^9$ Multic. Neurons

$10^{13}$ dynamic synapses

Estimated Material Cost for Base Unit : 20 M€

Technology Upgrades
- Increase Number of Base Facilities
- Increase Component Density
Collaboration

Neuromorphic Systems should be developed as one pillar in a coordinated large scale effort to understand, simulate and exploit the brain.

Integration

Integration in a multi-pillar project involving neuroscience, engineering, computing, medicine and others.

Coordination of neuromorphic computing and HPC development through common technological challenges.