



ICT - Nanoelectronics FP7 Workprogramme



EXTRACT FROM WORKPROGRAMME 2011-2012

Challenge 3: Components, systems, engineering

Challenge 3 covers electronic and photonic components, integrated micro/nanosystems, multicore computing systems, embedded systems and their monitoring & control and cooperating complex systems. It complements the developments undertaken in the ENIAC and ARTEMIS JTI's.

More specifically, Challenge 3 focuses on:

- The deep miniaturisation, energy-efficiency, performance increase and manufacturability of **nano-electronic** devices using alternative solutions to the traditional miniaturisation path, for information and communication systems and other applications in 2020 and beyond.
- The integration of new functionalities for the next generation of application-specific **components and smart systems** through the convergence of microelectronics, nanomaterials, biochemistry, measurement technology and ICT.
- The design, modelling and operation of systems composed of a large number of independent, heterogeneous and interacting **embedded systems** as well as their monitoring and control; and the management of interconnected large, yet autonomous systems ("Systems of Systems").
- The parallelisation and programmability methods to allow the adaptation of existing software to **multicore computing architectures and systems**, from embedded devices to general-purpose and to high performance computing.

- The further development of **core and disruptive photonic technologies** (lasers, waveguides, photodetectors, amplifiers, LEDs, optical fibres, etc), fundamental in strategic applications such as medicine, biology, communications, lighting, sensing and measurement, and manufacturing.

- The development of advanced, low temperature processing, and potentially printable devices and systems on **large area and/or flexible substrates**, such as light emitting and sensing devices, photovoltaics, displays, printed electronics for smart tags, or wearable smart textiles.

Research addressing this Challenge in particular will encourage international cooperation under the Intelligent Manufacturing Systems (IMS) scheme¹.

Objective ICT-2011.3.1: Very advanced nanoelectronic components: design, engineering, technology and manufacturability

This objective covers the combination and convergence of advanced More-than-Moore elements with Beyond-CMOS devices and their

¹ IMS member countries include South Korea, Mexico and the USA, see Agreement under: <http://eur-lex.europa.eu/JOHtml.do?uri=OJ:L:2008:053:SOM:EN:HTML>

integration and interfacing with existing technology. It addresses research from a "System Perspective", i.e. linking new advanced component technologies with advanced system design to support miniaturised electronic systems for 2020 and beyond. Developed components and technologies need to fulfil the criteria of "systemability", "integratability" and "manufacturability" where appropriate.

The interaction of circuit, device and technology research communities will be stimulated. Research for disruptive approaches and holistic research solutions to address new levels of miniaturisation at component and system level are targeted as well as related novel manufacturing solutions and access to manufacturing and integration platforms for European equipment and material suppliers.

The activities under this objective are complementary to the activities in the ENIAC JTI².

Target outcome

a) Beyond CMOS technology

- New switches and interconnects which offer scalability, performance and energy efficiency gains, operational reliability and room temperature operation with preferably CMOS process and architectural compatibility.
- Advanced system integration technology and new methods for computation.
- Emerging memories targeting the concept of non-volatile universal memory.
- Nano-phonic devices & interconnects integrated with nano- and Beyond-CMOS.
- Carbon based electronic devices.
- Novel materials for interconnects, nano-packaging, Beyond-CMOS (logic and memory).
- Understanding fundamental artefacts and limits: nano-scale thermal processes; computational material and device science.

b) Circuit-technology solutions, addressing in a *combined manner*:

- Architectures including energy efficiency, spin devices; silicon with molecular

switches; ferromagnetic logic; heterogeneous and morphic system architectures.

- Circuit design, methodology and tools addressing e.g. power dissipation constraints; SRAM stability; digital-analogue convergence; device variability, model accuracy; reliability and novel functionality.
- Technology addressing e.g. device leakage current, power dissipation, process variability; monolithic as well as 3D integration of Beyond-CMOS and advanced More-than-Moore; co-integration of photon and electron based devices.
- Modelling and simulation: e.g. quantum and atomic scale effects; electro-thermo-mechanical effects; band-to-band tunnelling; drift diffusion effects; variability; modelling for new materials, processes and devices, and higher abstraction level models for cross technology cross IP level simulation.
- Design-technology solutions for energy efficiency, high reliability and robustness including ultra low power techniques and zero-power concepts; thermal aware design, solutions for complex single or multi-technology systems; reuse and standardisation with respect to IPs, design for self-testing, self-healing and self-configuring.

c) Nano-manufacturing and Joint Equipment Assessment,

comprising the complete manufacturing supply chain for flexible and customised manufacturing of integrated nano and Beyond-CMOS components:

- Manufacturing approaches to Beyond-CMOS and advanced More-than-Moore', and to their integration with nanoCMOS including 3D integration.
- Enhanced variability control; integrated metrology/inspection/analysis concepts and tools to support 3D approaches; functionalised assembly and packaging (also at wafer level).
- Joint Assessments of (combined) equipment/metrology/process solutions ranging from proof of concept for 'disruptive' approaches and for 450 mm to prototype testing with suppliers and users;
- 200/300 mm wafer integration platforms and short user-supplier feedback loops.

² The JTI addresses application-guided industrial cooperative research in the 'More Moore' and 'More than Moore' domains for the next generation components and systems and targets large strategic initiatives. In manufacturing, the JTI targets larger volume fabrication with emphasis on generic manufacturing and equipment development. See <http://www.eniac.eu>

d) Coordination and Support Actions

- Broker services to offer European researchers and SMEs access to training, to CAD tools and to advanced technologies, design kits and IP blocks for education, prototyping and small volume production.
- Roadmaps; benchmarks; strategy papers; studies of limits of Beyond-CMOS and advanced More-than-Moore processes, devices and architectures w.r.t systemability, integrability, energy efficiency, scalability and manufacturability.
- Stimulation of young people towards electronics careers; training and education for high school students; access for students and PhDs to production lines and research labs.
- International cooperation, in particular with the USA, Taiwan, Korea and Japan.
- Support, coordination and standardisation actions including preparatory work for 450 mm wafer processing targeting material and equipment companies.

Expected impact

- Increased European knowledge, resources and skills at the frontier of nanoelectronics technology and miniaturised electronic systems, enabling further European partnerships in world-wide collaborations. European research organisations in leading positions.
- A more integrated nano-electronics technology, device and design research community, better targeted to the business strategy of the European industry.
- Increased attractiveness for investments in components miniaturisation, functionalisation and manufacturing in Europe; increased business opportunities and market share.
- New electronic applications of high economic and socio-economic relevance.
- Strengthened competitiveness of the European foodchain for the nanoelectronics industry (materials, equipment and component suppliers, academia and institutes).

Funding schemes

a): STREP; b): IP, STREP; c): IP, STREP; d): CSA

Indicative budget distribution

- IP/STREP: EUR 55 million; the objective is to support at least one IP under b) and at least one IP under c) in addition to STREPs.
- CSA: EUR 5 million

Call: ICT call 8

- Call identifier: FP7-ICT-2011-8
- Date of publication³: 26 July 2011
- Deadline⁴: 17 January 2012, at 17:00.00 Brussels local time

For further information:

http://cordis.europa.eu/fp7/ict/nanoelectronics/home_en.html

info-nanoelectronics@ec.europa.eu

³ The Director-General responsible for the call may publish it up to one month prior to or after the envisaged date of publication.

⁴ The Director-General responsible may delay this deadline by up to two months.