Let us define the future calls for 'Embedded Systems Design' together!

ICODES project outcomes and future issues

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Outline of this talk

- ICODES:
  - Mission statement
  - Results
  - Project evaluation
- Future issues
EC Goal for Embedded System Flow

Objectives of IST-2002-2.3.2.5 – “Embedded Systems”:

“To develop the next generation of technologies and tools for modelling, design, implementation and operation of hardware/software systems embedded in intelligent devices. An end-to-end systems vision should allow to build cost-efficient systems with optimal performance, high confidence, reduced time to market and faster deployment.”

ICODEES Mission

Efficient design methodology for Communication dominated HW/SW systems

Application model

Seamless flow: No re-coding exploration

Communication Metrics and tool for analysis

Integration of IP-components

Modell uses OO techniques
Outline of this talk

- **ICODES:**
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Industrial Evaluation

Mobile Devices (JPEG 2000)
- Parser
- Data Ordering
- Arithmetic Decoder
- Coefficient bit modelling

Communication Infrastructure (Part of Base Station Controller)
- Data Protocol Elaboration Module
- Line Module
- Circuit switching protocol stack
- Ethernet Switch

Decoded Image

Automotive Electronic ("Night View" Video Processing)

Evaluation: OSSS/FOSSY Synthesis
- Use of arbitrary Software compiler
- Use of standard VHDL synthesis tools

OO hardware synthesis

3rd party tools
- C++
- MSS
- gcc
- LibGen
- Linker
- MHS
- PlatGen
- XST/Synplify
- Xilinx IPs
- DDR RAM
- Memory Controller
- Arbiter
- Xilinx MicroBlaze
- Hardware Block
- Object Socket

Flow

S Flow
Summary: ICODES Key Outcomes

- An analysis framework
  - Analysis of communication dependencies inside OSCI TLM v1 models
- A modelling framework
  - Method based communication (method invocations as transactions) in application model
  - Communication refinement from application to VTA level
  - Support for IP component integration
- A synthesis framework
  - Accepts refined VTA models
  - FOSSY generates RT level SystemC or VHDL
  - Integration scripts for Xilinx EDK
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Lessons Learned and Future Issues (1)

**Challenge 1: Multi-X software**

*Just having an operating system model and isolated tasks is not sufficient*

We need to address:
- Software-to-software communication
- Communication topology
- Transparency of communication partners: HW or SW
- Communication timing
- Blocking behavior
- Bus load
Lessons Learned and Future Issues (2)

- There are mixed-timing accuracy modelling frameworks (cycle accurate, I/O accurate, programmers view, ...)
- There are system description frameworks with implementation path

Challenge 2:

We need an integrated solution!

Further Information

fossy
http://fossy.offis.de

ICODES
http://icodes.offis.de

ANDRES
http://andres.offis.de

Thank you for your attention!

Funded by the EC
ICODES results: Polimi

Politecnico di Milano:
• Metrics for bandwidth in transaction level models
• Early estimation based on application structure, not target architecture
• Tool prototype to aid designer

Lessons learned and future issues (3)

Challenge 2: Transaction Level Modelling etc.

It is not sufficient to identify a suitable model!

We need a synthesis path. Otherwise we have to re-code at lower levels of abstraction.
• Where do we take the time to code again and eliminate the errors? This means: a longer time to market!
• How can we be sure that the new model is a refinement of the abstract model? Does the abstract model still help us?
We really built it!